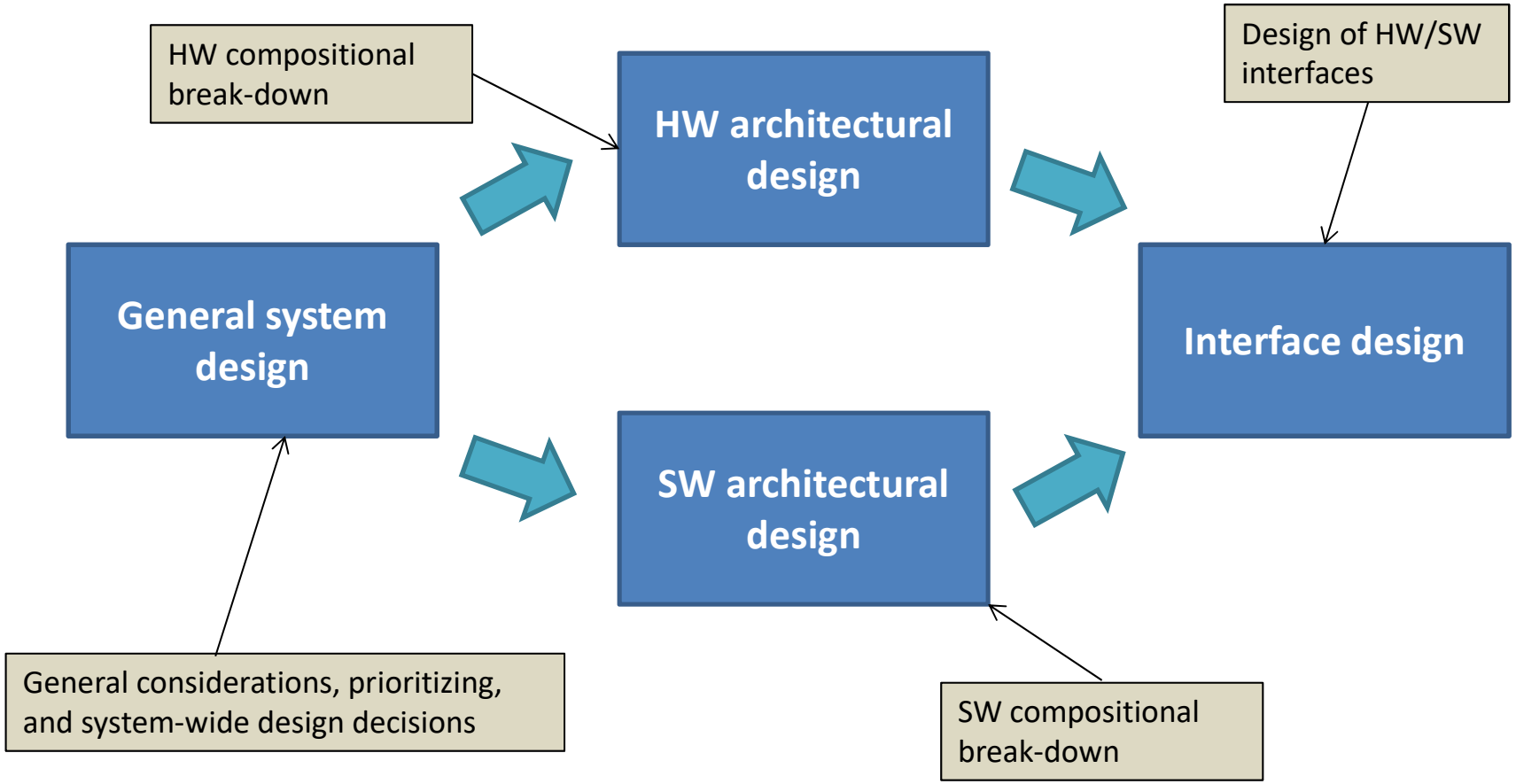
System Design and Interfaces (SysML and Hardware)

I2ISE

It is essential to know the specification of interfaces being able to design, test and develop a system.

HW/SW architectural design

- Today, we look at *HW architectural design and interfaces*



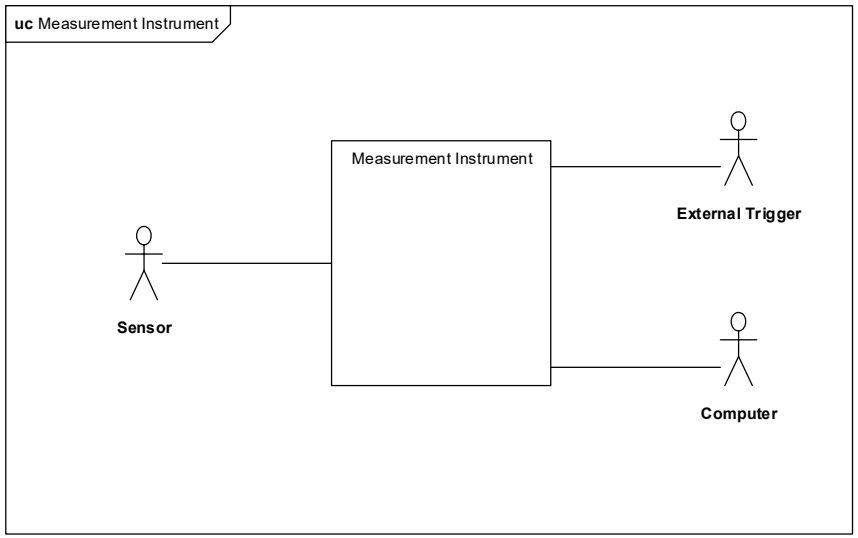
Interfaces

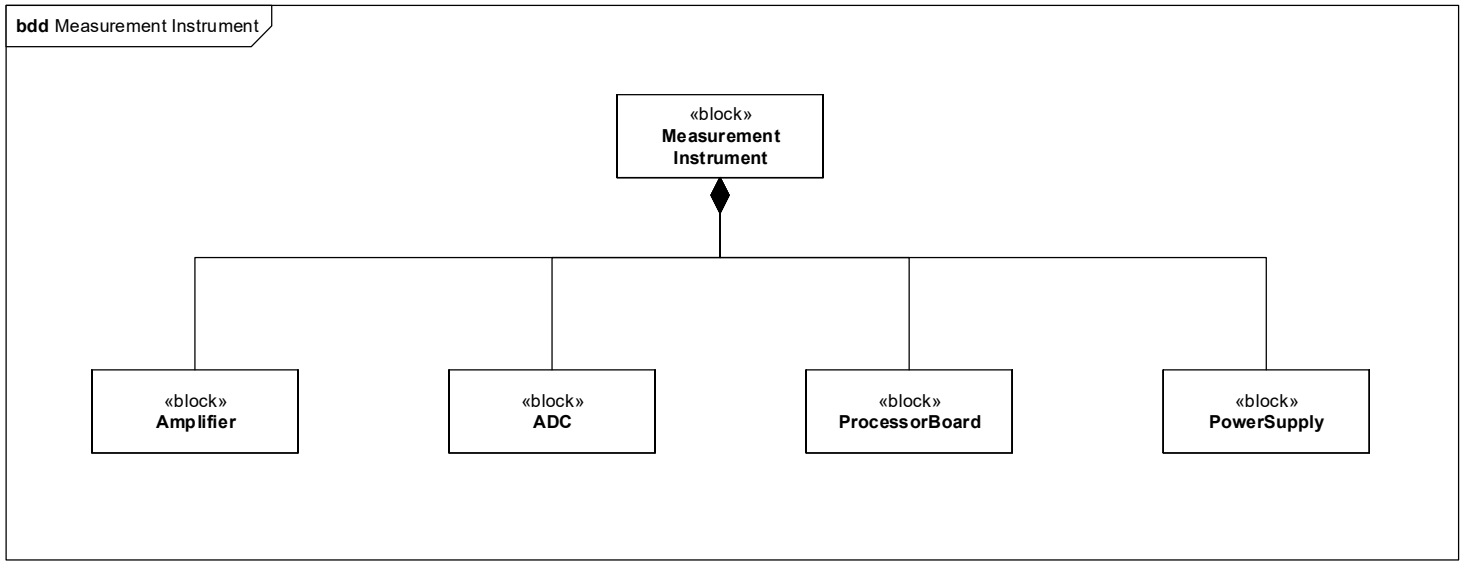
- Today, we will look at *interfaces*:
  - **Interfaces in SysML**
  - **Specifying HW interfaces in detail**
  - *Specifying SW interfaces – later in course*
  - *Specifying protocols – later in course*
  - …

How to specify interfaces using SysML

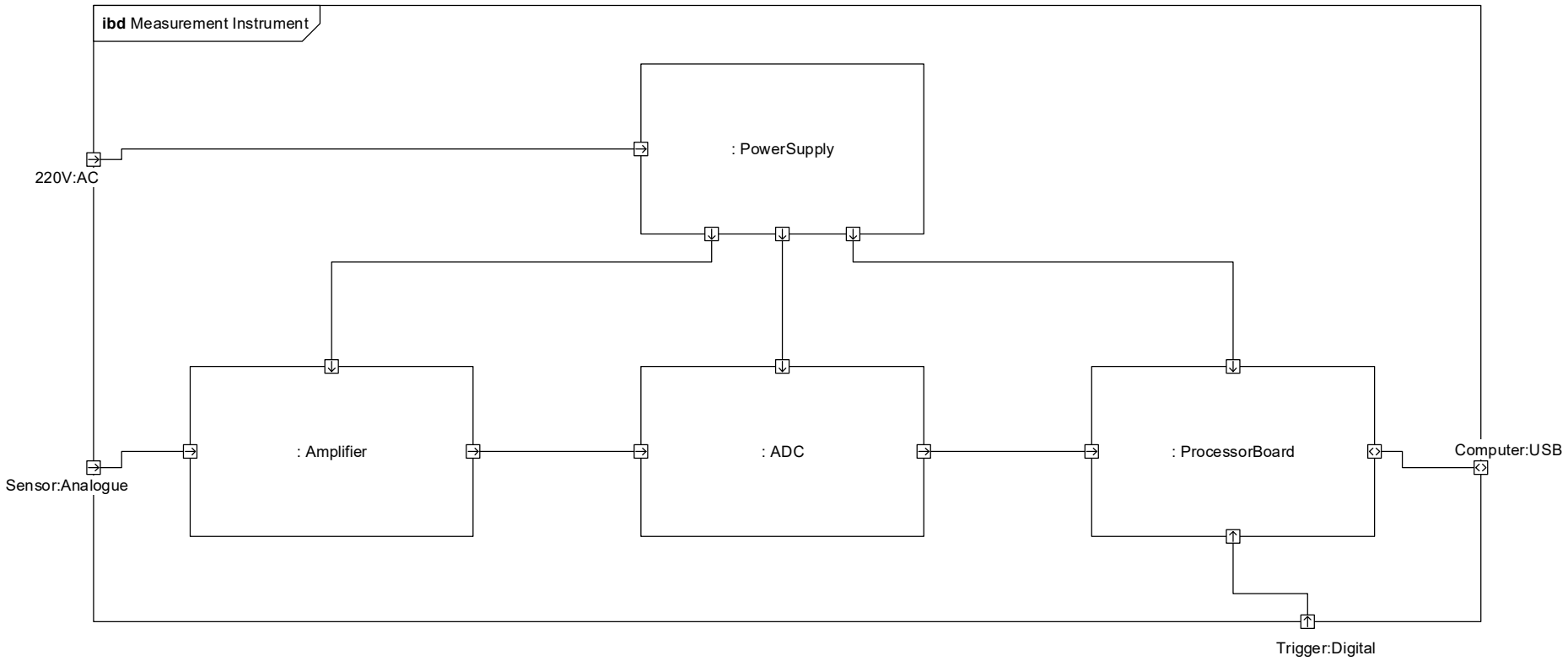
1. Start with context and BDD and IBD diagrams
2. Define external ports on the IBD diagram
3. Define internal ports on the IBD diagram
4. Describe functionality for every block
5. Specify requirements to interfaces between parts - describe electrical requirements for all ports of all blocks in a table – ensure they fit together

1. Measurement Instrument – Context /BDD





2. Measurement Instrument – IBD External Ports



2. External Ports Requirements

Name of Block	Description of function	Port Name	Type	Port Specification
Measurement Instrument	Instrument to measure low voltage sensor signals. The sensor signal is digitized and data stored in memory whenever the input trigger signal is high. Measured sensor data can be transfer to a connect computer over the USB port.	220V	AC	200 – 250 V RMS, 50 Hz Input current limiter of 100 mA
		Sensor	Analogue	Differential Input Signal Voltage Range -100 to +100 uV peak Impedance 50 Ohm
		Trigger	Digital	5 V trigger input Low when < 0.8 V High when > 2.0 V
		Computer	USB	USB 2.0

Examples of different **type** categories

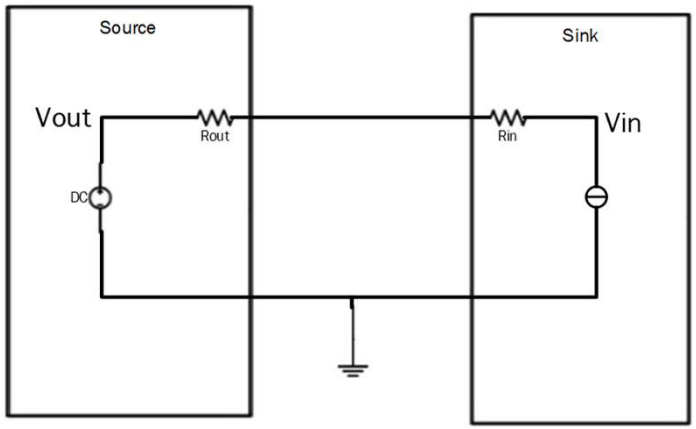
(Mainly used in the course)

Signals (Electrical)	Standards (Physical, Protocol)	Network (Protocol)	Information (Software)	Supply (Power)	Others
Analogue	USB	Ethernet	File	DC	Force
Digital	RS232	Wireless	Image	AC	Light
	HDMI	Internet	String		Sound
	SPI	Profinet	Barcode		Noise
	I2C		Bytes		Liquid
	TTL		Data		
	CMOS		Bool		

Signals (Electrical)

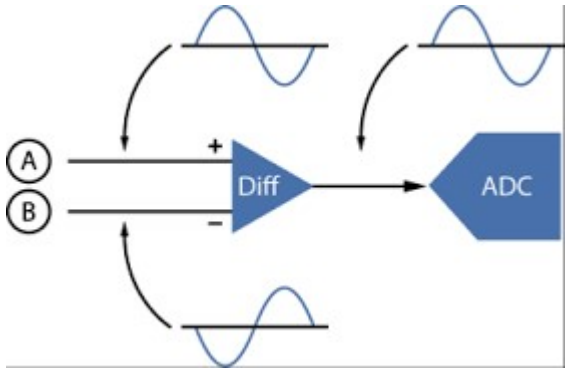
- Ouput voltage with tolerances and maximum current
- Input voltage with tolerances and maximum current
- Output and input impedance has to fit together

Single Ended Interface

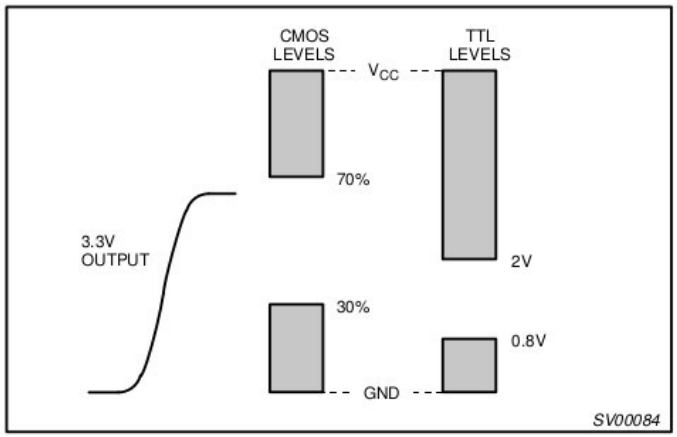


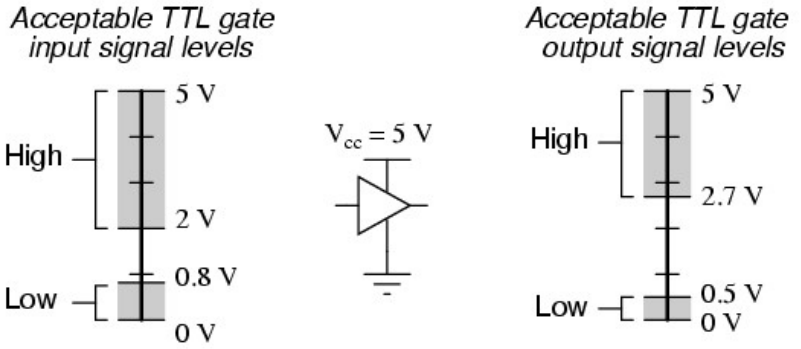
Rin = Rout is best

Differential Input

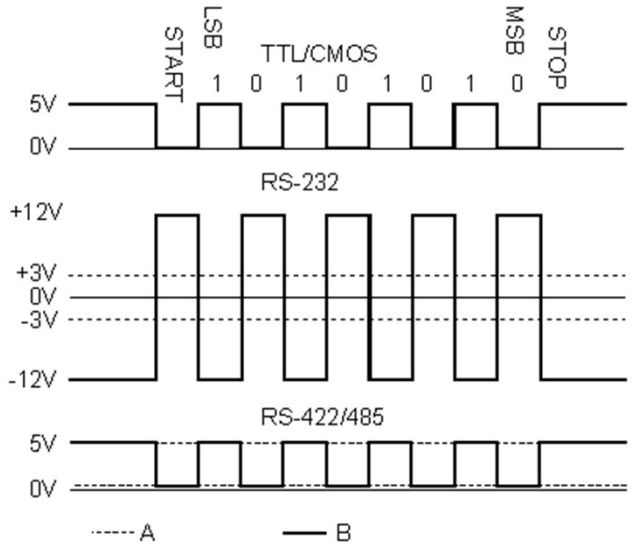


Interface with Digital Signals (Standards TTL or CMOS)

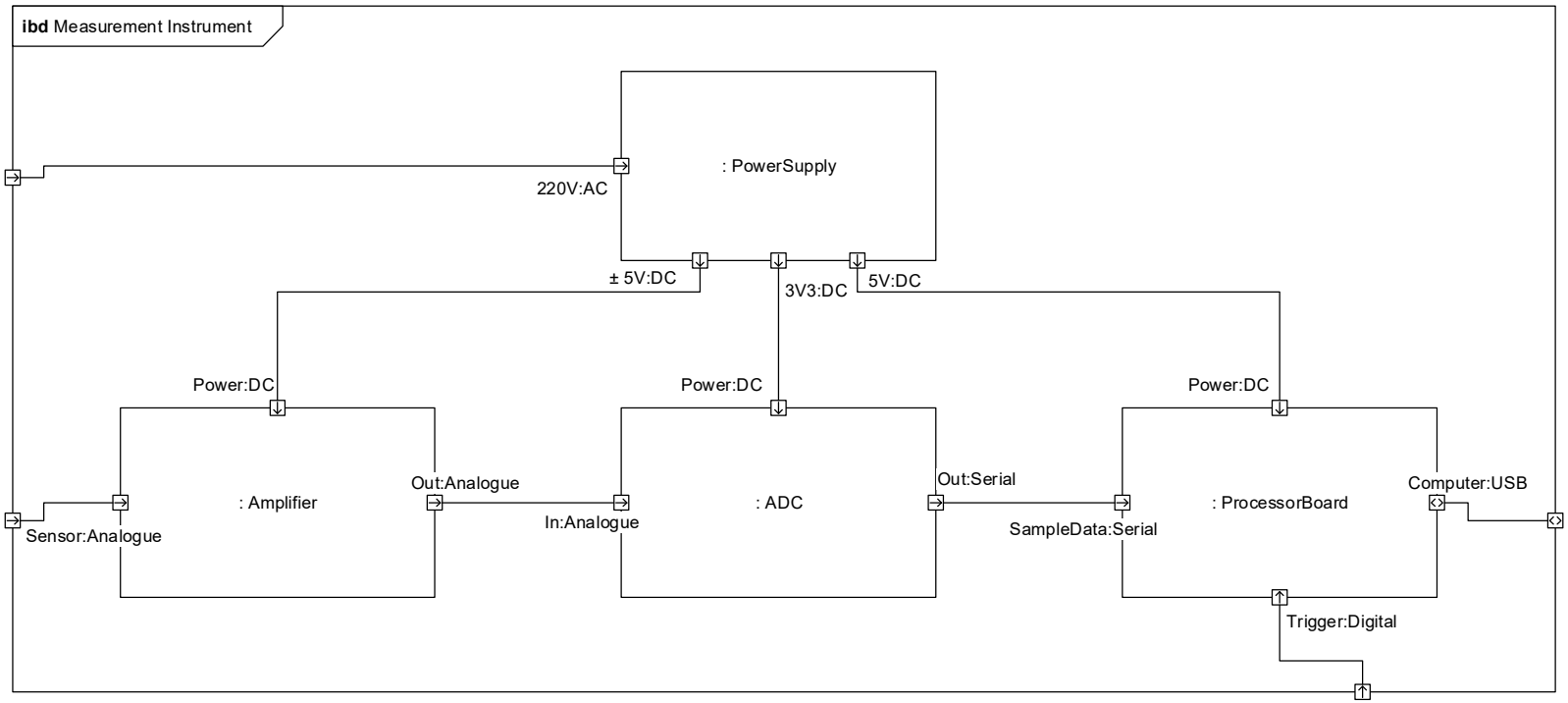




ASCII "U" = 85 Decimal = 55 Hexidecimal = 01010101 Binary



3. Internal Connections – Ports <**name:type**>



4-6. Example of block description and ports (Power Supply, Amplifier)

Name of Block	Description of function	Port Name	Type	Port Specification
Power Supply	Converts input AC power to internal DC power supplies	220V	AC	200 – 250 V RMS, 50 Hz Input current limiter of 100 mA
		±5V	DC	Dual Supply Voltage Tolerance ±0.2 V, Max. 250 mA
		3V3	DC	Single Supply Voltage Tolerance ±0.3 V, Max. 250 mA
		5V	DC	Single Supply Voltage Tolerance ±0.2 V, Max. 500 mA
Amplifier	Amplifies sensor input signal • 5000 times amplification • Frequency range 0 – 3 kHz • Signal to Noise Ratio better than 65 dBFS	Power	DC	±5V, Tolerance ±0.3 V, Max. 200 mA
		Sensor	Analogue	Differential Input Signal Voltage Range -100 to +100 uV peak Impedance 50 Ohm
		Out	Analogue	Single Ended Output Signal Voltage Range –500 to +500 mV peak Impedance 500 Ohm

Your turn!

- Specify requirements to **ADC and ProcessorBoard**
  - Specify requirement to all ports with ?

Name of Block	Description of function	Port Name	Type	Port Specification
ADC	Analogue to digital converter • 8 kHz sample rate • 24 bits sample	Power	DC	?
		In	Analogue	?
		Out	Serial	SPI or I2S
Processor Board	Collects digitized sensor signals and store data in memory when trigger input is high. Possible to transfer sensor data over USB port. • Memory 1 GByte • Processor ADI BF706	Power	DC	?
		Sample Data	Serial	SPI or I2S
		Trigger	Digital	?
		Computer	USB	USB 2.0

Questions

- Verify that the internal DC power interfaces are correct?
- Can you see any problems with the port specifications?

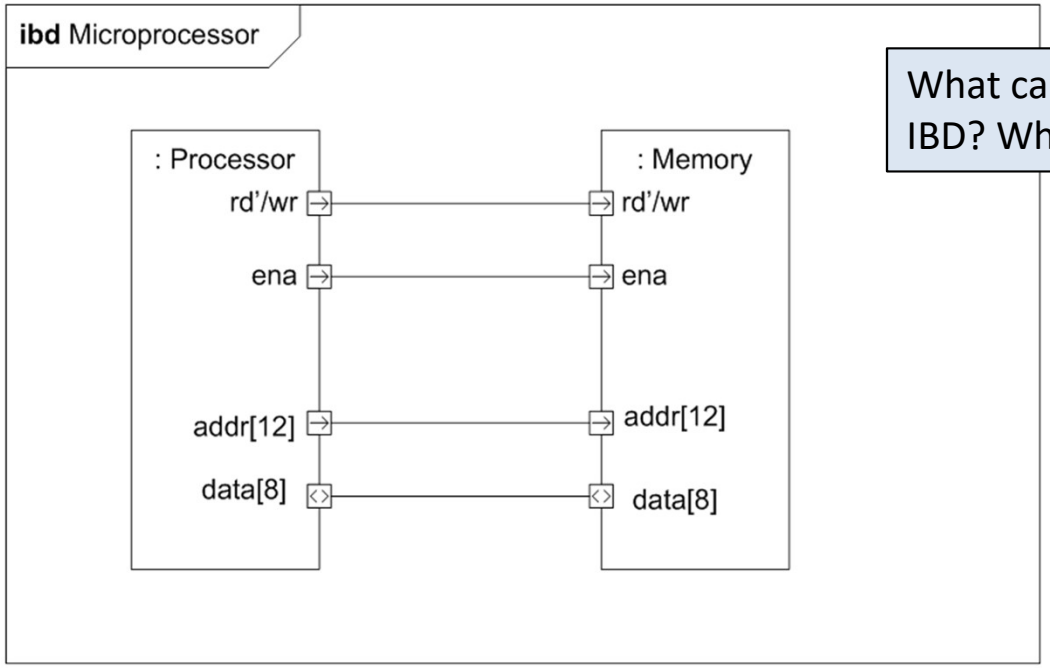
(Processor Board -> Power:DC - max. 600 mA!)

- Verify that the amplifier output fits with the ADC input?
- Can you see any problems with the interface?

(ADC -> In:Analouge – 5 Ohm!)

Interfaces: Specifying in detail

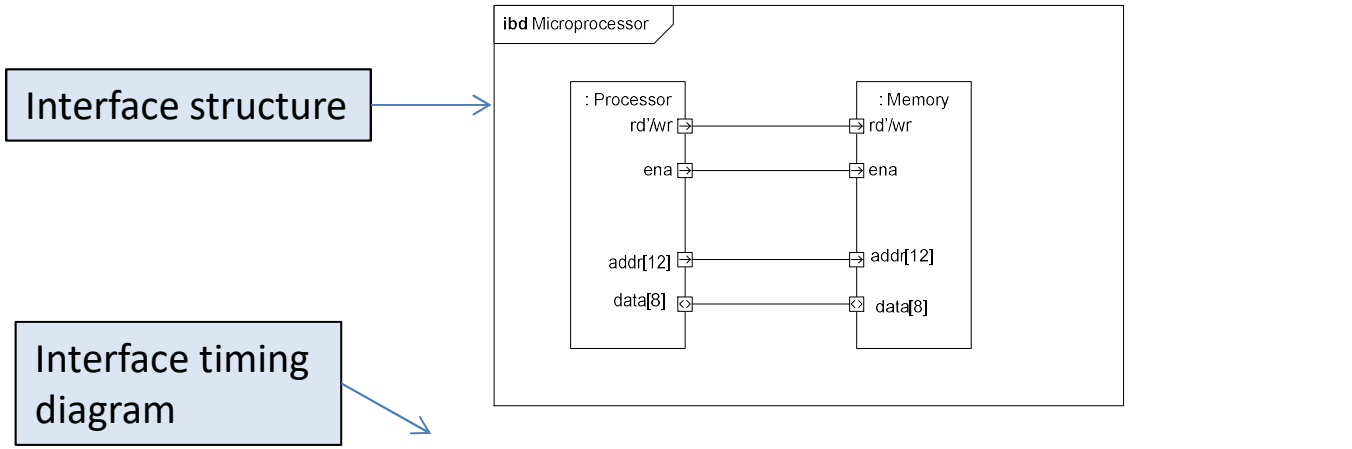
- SysML interface descriptions using flow specifications are ”fine”.



- However, at some point, the interface must be described in complete and unambiguous detail.

Specifying in detail: Example

- All information related to timing etc. are absent, so we need a timing diagram to create the HW-SW interface



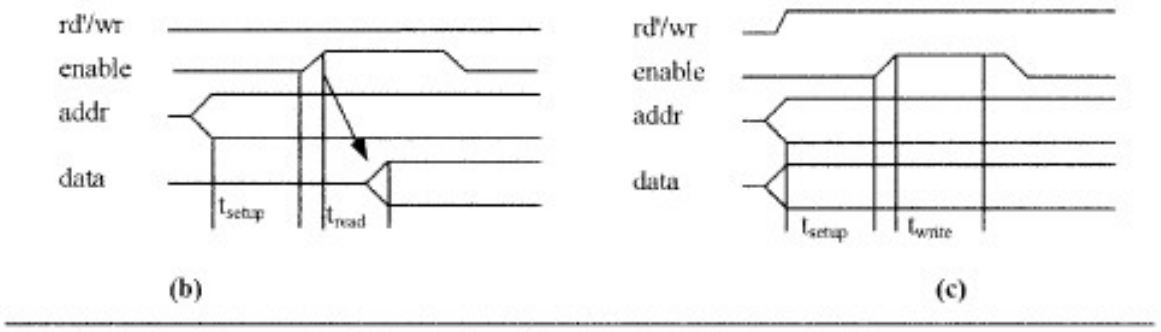
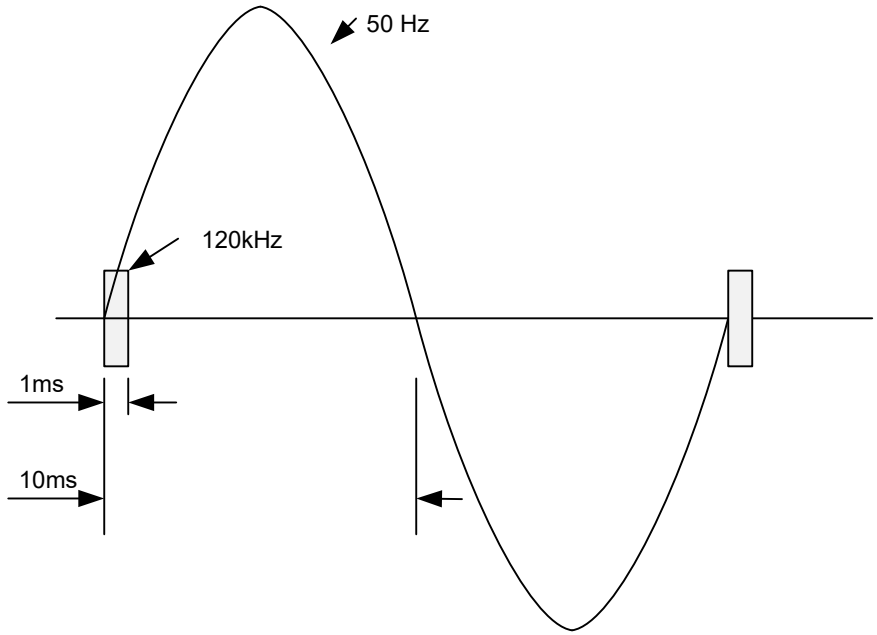


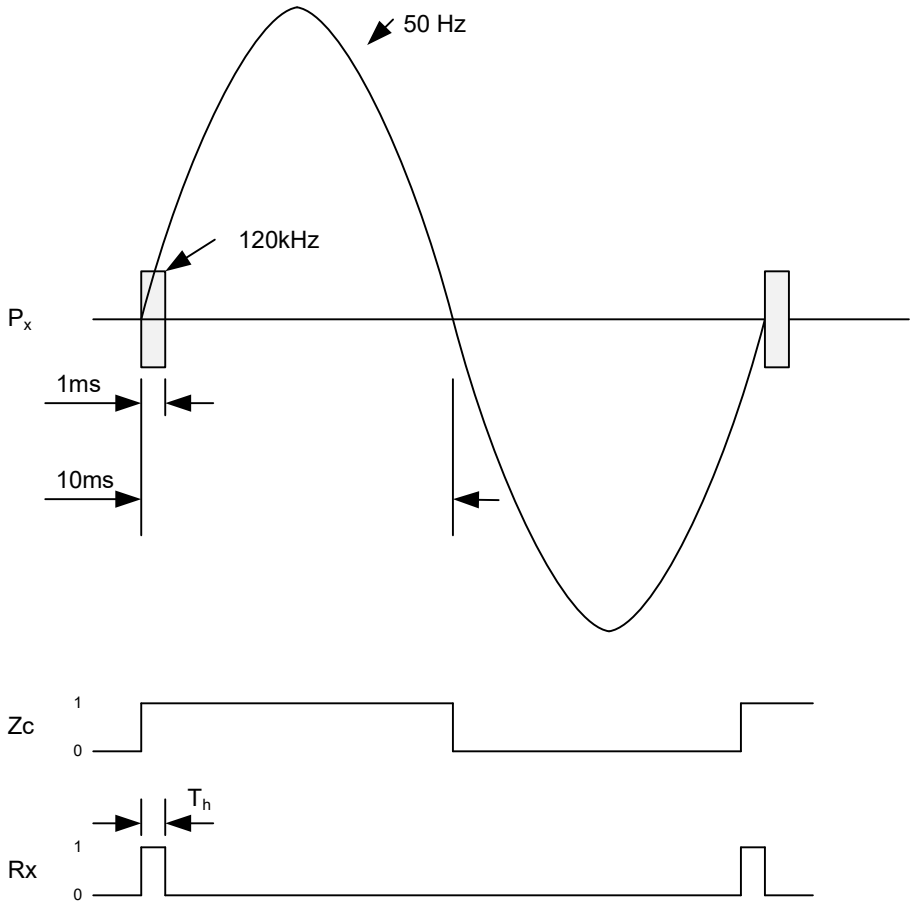
Figure 6.1: A simple bus example: (a) bus structure, (b) read protocol, (c) write protocol.

Specifying in detail: Timing diagram
Your turn

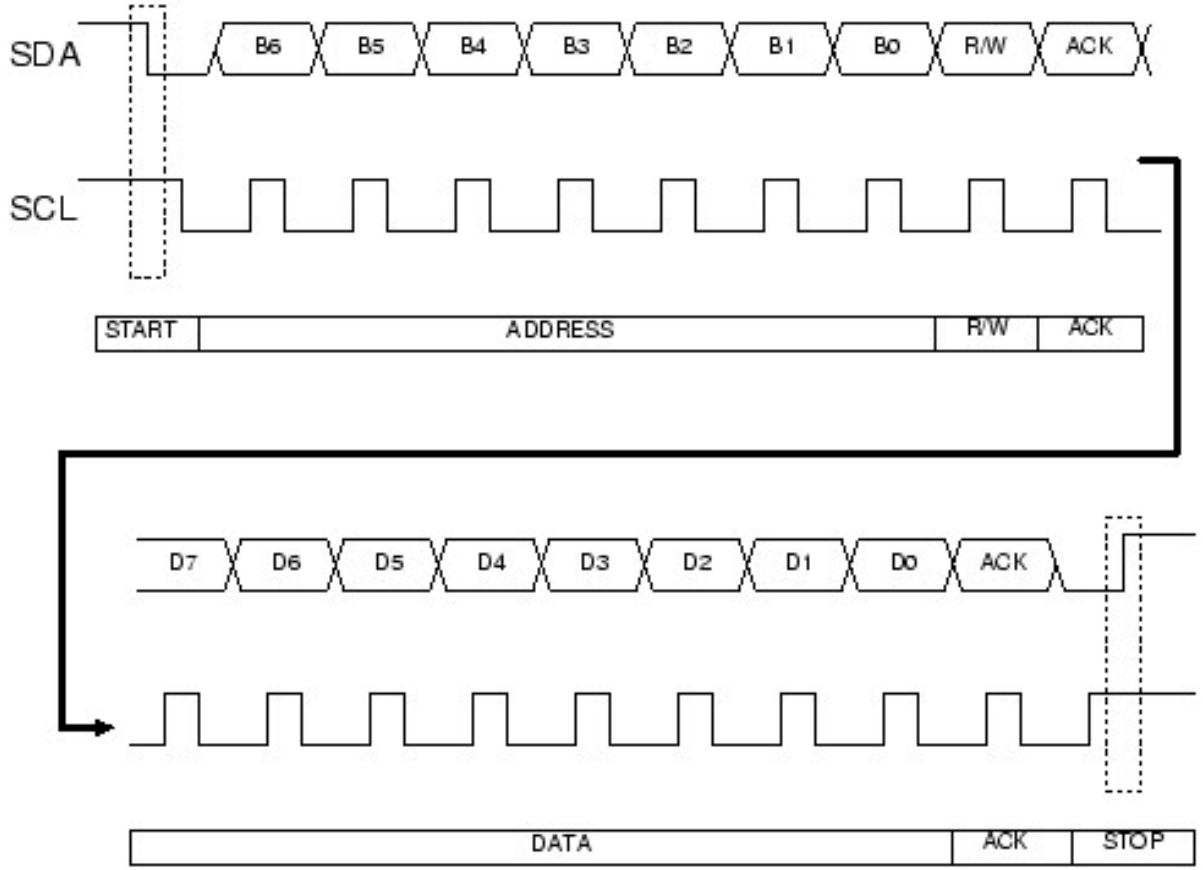
- Specify a timing diagram for an X.10 receiver, including:
  - The 50Hz power signal P_x
  - An signal that toggles when a zero crossing in 50Hz signal is detected (Z_c)
  - A signal which is active whenever 120kHz signal is detected (Rx)
  - Requirements for hold time (T_h)



Specifying in detail: Timing diagram
Your turn



Specifying in detail: Another example: I^2C



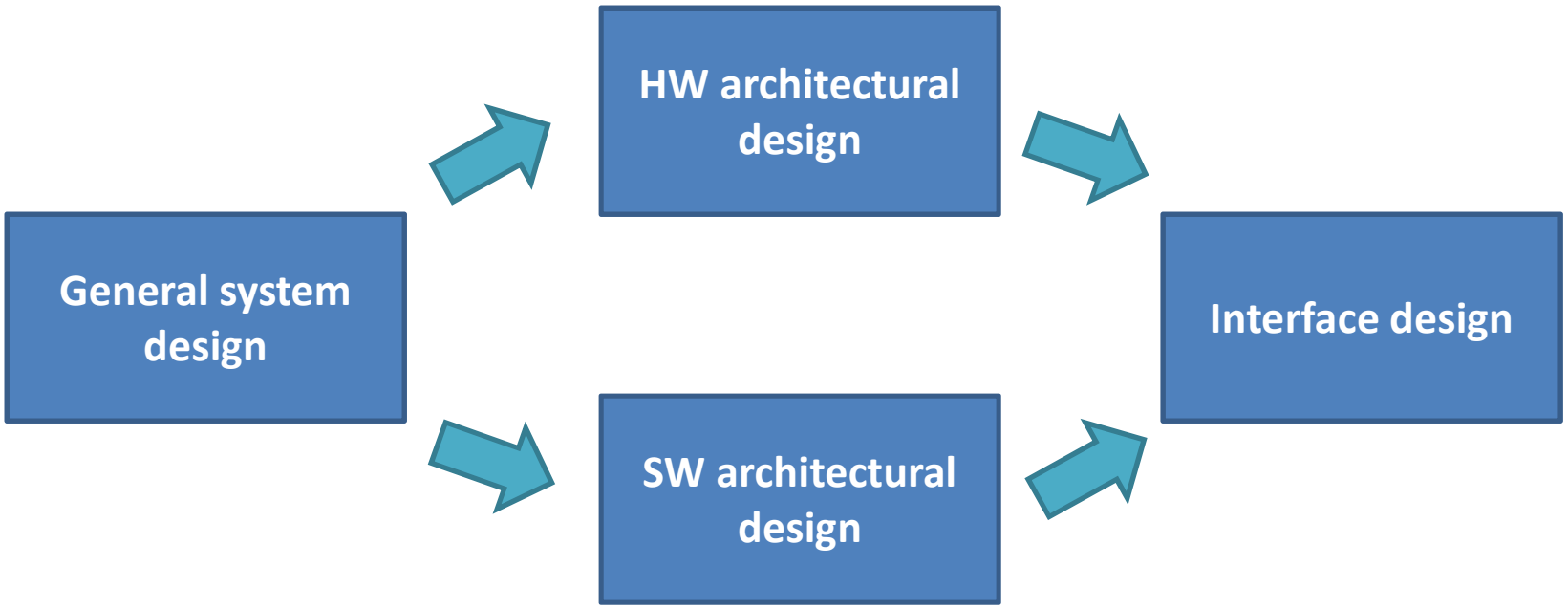
What you can't read from this is…

Specifying in detail: More details

- Specifying a hardware interface in detail will also require a load of other things to be specified:
  - Physical signals and boundaries
  - Inputs and outputs
  - Voltage and frequency limits
  - Standards
  - …

System sample rates	
Internal sample rate	192 and 176.4 via Dual Wire (optional Digital Card required) and
	96, 88.2, 64, 48, 44.1 or 32 kHz
AIR Masters only	
I/O Connectors	XLR (2 channels AES/EBU in) 3 x RJ45 proprietary TC LINK
Formats	AES/EBU (24 bit)
Word clock input	BNC, 75 ohm, 0.6 to 10 Vpp
Display	2 x 16 character dot matrix
Operation	Menu system / four buttons
Analog input option	
Input connectors	XLR balanced (pin 2+, pin 3-)
Impedance	10/3 k Ohm (Balanced/unbalanced)
Selectable full scale input level	+9, +15, +21, +27 dBu
Dynamic Range	> 113 dB typ. (unweighted), BW: 20-20kHz
THD+N	< -105 dB typ. @ 1 kHz, -3 dBFS
Crosstalk	< -120 dB, 20 Hz to 20 kHz
A to D Conversion	24 bit (Dual bit delta sigma sampling at 4.1/5.6/6.1/6.1 MHz)
AIR Slaves only	
I/O Connectors	2 x RJ45 proprietary TC LINK

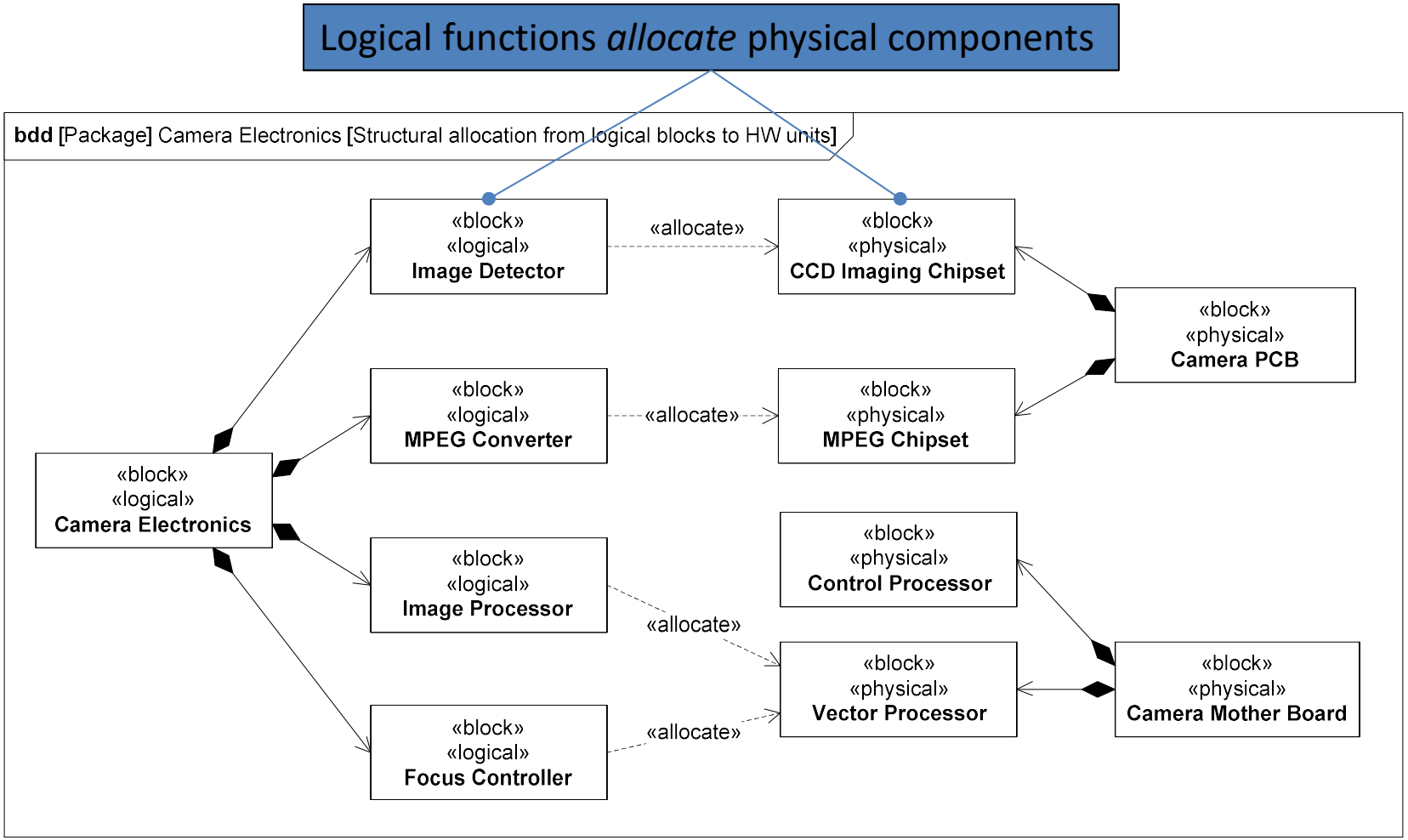
Hardware architectural design



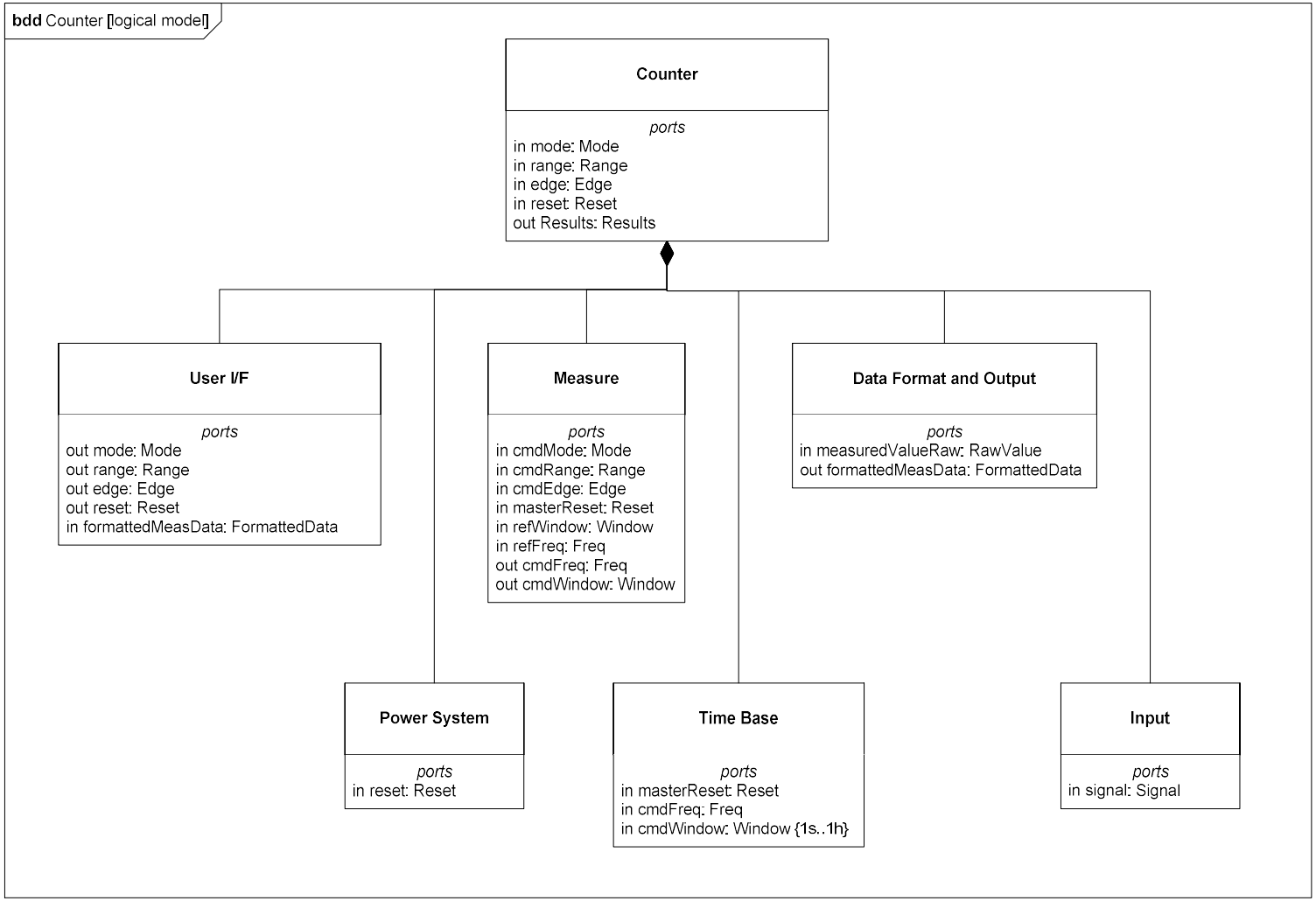
HW architectural design

- An attempt at a”cookbook” for HW architectural design:
  1. Create a *logical model* of the system (logical blocks)
  2. Investigate the *logical* interfaces
  3. Create a *HW model* of the system (physical blocks)
  4. Allocate the logical blocks to the *physical blocks*
  5. Define the *physical* interface between the blocks and to the environment

bdd: Logical to physical



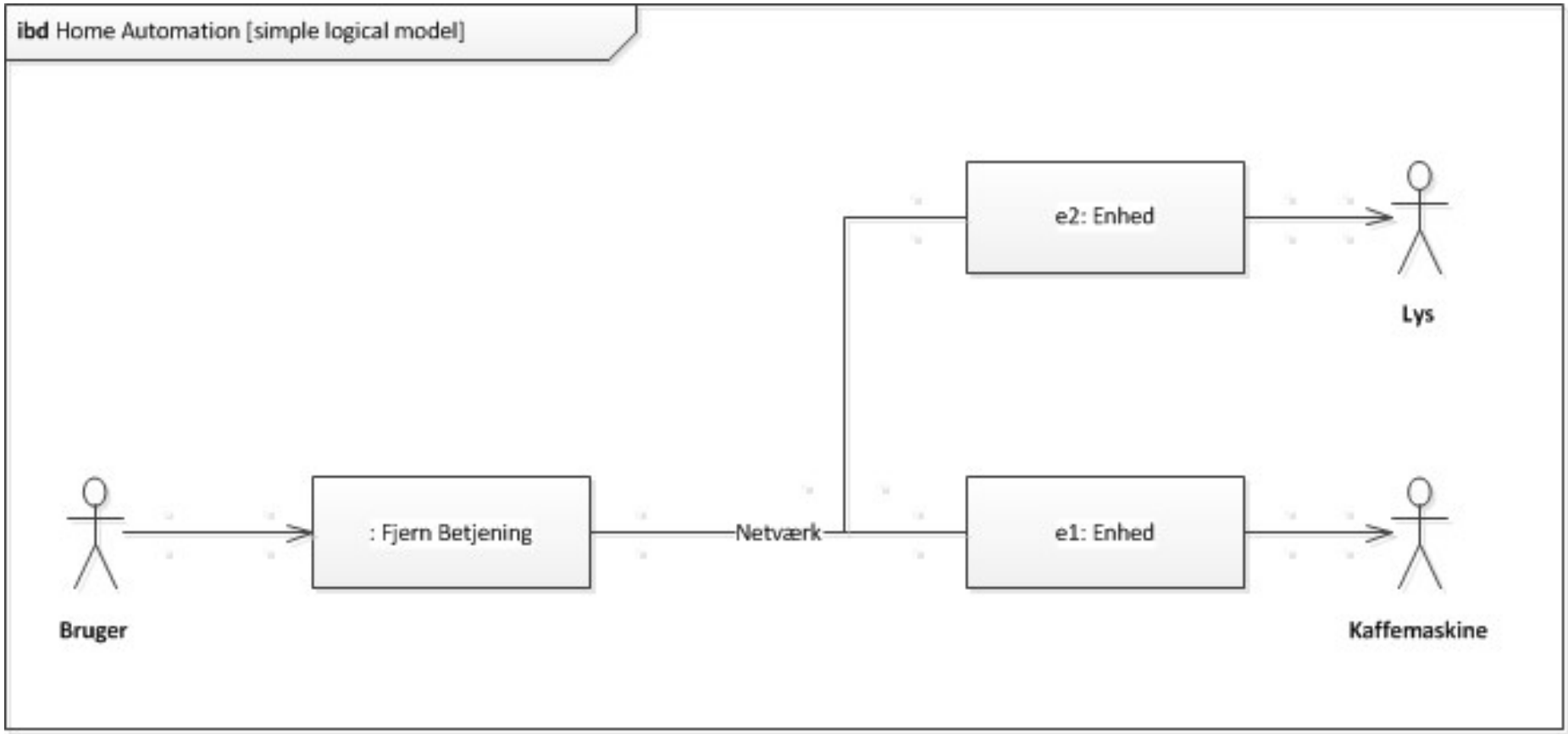
Counter example – *logical* blocks and interfaces



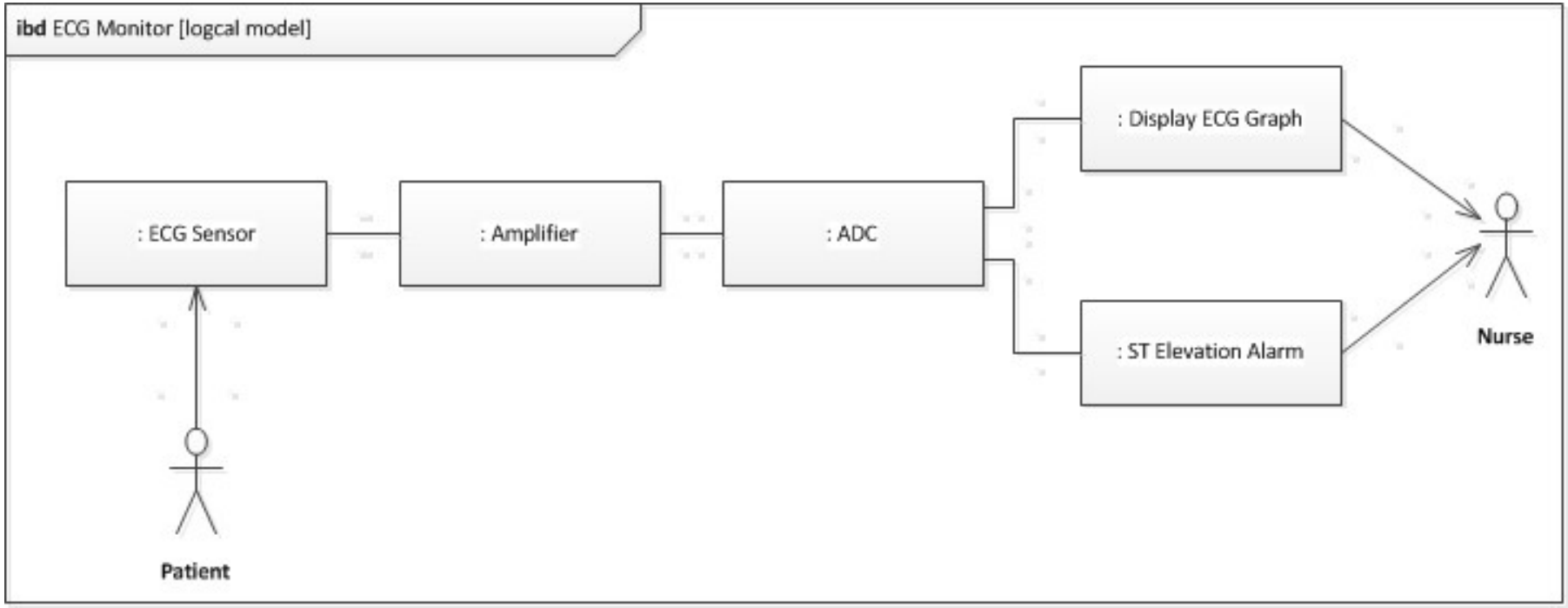
Logical structure of your semester project?

- Spend the few minutes discussing a logical structure for your semester project
  - Logical blocks?
  - Logical system interfaces?
  - Logical internal interfaces?

Home Automation



ECG Monitor


ibd ECG Monitor [logcal model]
: ECG Sensor
: Amplifier
: ADC
: Display ECG Graph
: ST Elevation Alarm
Patient
Nurse

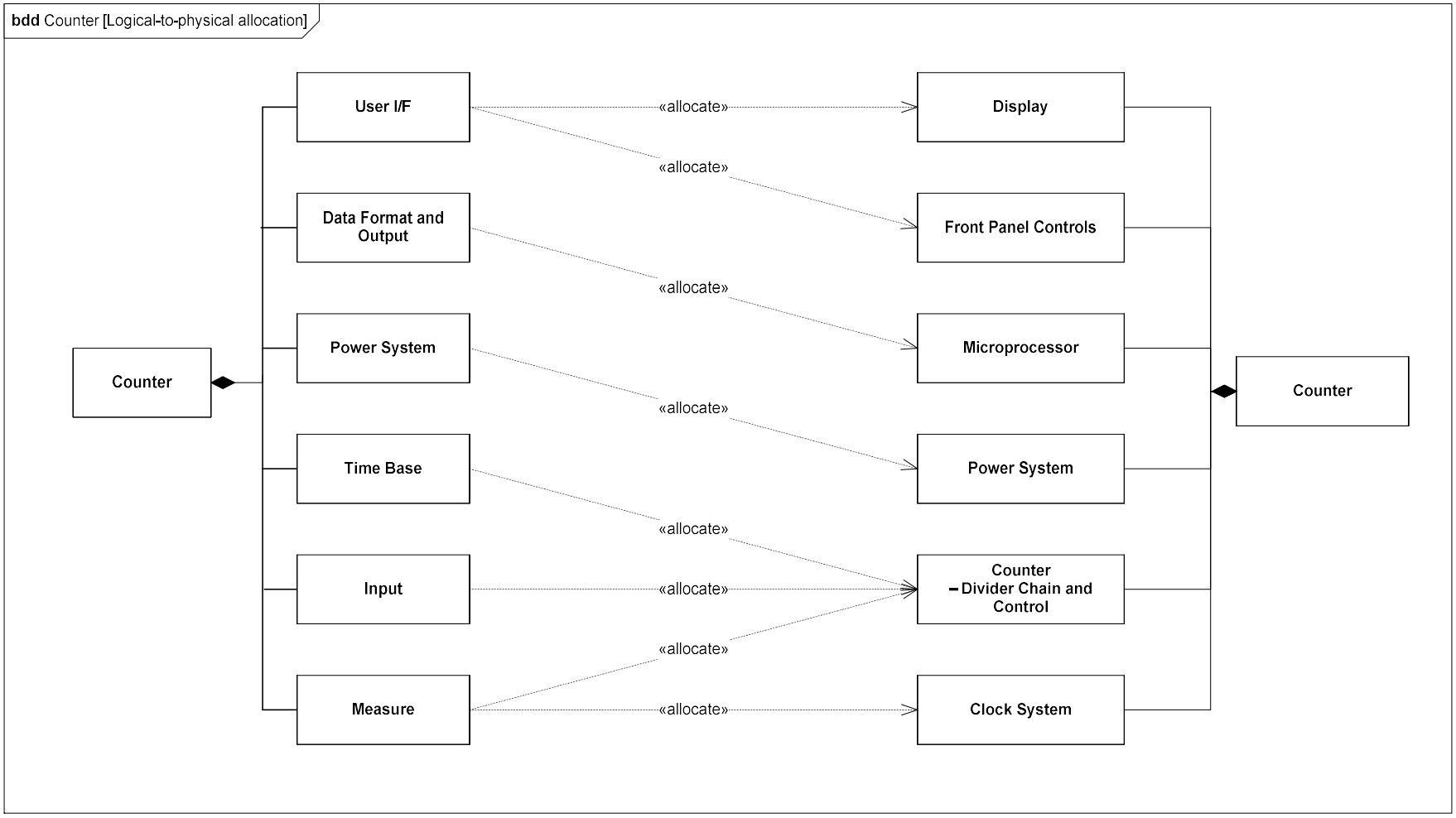
Mapping logical blocks to physical blocks

- From the logical system structure and the requirements[1], we derive a HW architecture with a suitable set of HW blocks
  - Processors, peripherals, buses, etc.

- Then, we (iteratively) allocate the logical blocks , i.e. *functions*, to the physical blocks, i.e. *hardware*

1: And from available, required or desired HW, experience, cost, and a score of other sources…

Mapping logical blocks to physical blocks «allocates»



Physical structure of your semester project?

- Spend the few minutes discussing a pyhsical structure for your semester project
  - Physical blocks?

- Then, discuss how the logical blocks map to the physical blocks you have defined.