Pulpino SoC

SPI Master Registers Specification

2022-Feb-10

Table of Contents

1 SPI Master Top

SPI Master Registers

Base Address: 32'h1A10_2000
Size(bytes): 0x28

Registers List

Offset	Identifier	Name
32'h0000_0000	STATUS	STATUS
32'h0000_0004	CLKDIV	CLKDIV
32'h0000_0008	SPICMD	SPICMD
32'h0000_000C	SPIADR	SPIADR
32'h0000_0010	SPILEN	SPILEN
32'h0000_0014	SPIDUM	SPIDUM
32'h0000_0018	TXFIFO	TXFIFO
32'h0000_001C	-	-
32'h0000_0020	RXFIFO	RXFIFO
32'h0000_0024	INTCFG	INTCFG

1.1 STATUS

SPI Status Register

Defines the mode of operation

Absolute Address: 32'h1A10_2000
Base Offset: 32'h0000_0000
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:12]	RESERVED12	RO	20'h0_0000	Reserved12 Reserved for further usage
[11:8]	CS	RW	4'h0	Chip Select Specify the chip select signal that should be used for the next transfer
[7:5]	RESERVED5	RO	3'h0	Reserved5 Reserved for further usage
[4]	SRST	RW	1'h0	Software Reset Clear FIFOs and abort active transfers
[3]	QWR	RW	1'h0	Quad Write Command Perform a write using Quad SPI mode
[2]	QRD	RW	1'h0	Quad Read Command Perform a read using Quad SPI mode
[1]	WR	RW	1'h0	Write Command Perform a write using standard SPI mode
[0]	RD	RW	1'h0	Read Command Perform a read using standard SPI mode

1.2 CLKDIV

Clock Divider Register

Defines the clock divider value

Absolute Address: 32'h1A10_2004
Base Offset: 32'h0000_0004
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:8]	RESERVED8	RO	24'h0_0000	Reserved8 Reserved for further usage
[7:0]	CLKDIV	RW	8'h00	Clock Divider Clock divider value used to divide the SOC clock for the SPI transfers. This register should not be modified whil a transfer is in progress.

1.3 SPICMD

SPI Command Register

Specifies the SPI command value

Absolute Address: 32'h1A10_2008
Base Offset: 32'h0000_0008
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:0]	SPICMD	RW	32'h0000_0000	SPI Command When performing a read or write transfer the SPI command is sent first before any data is read or written. The lenght of the SPI command can be controlled with the SPILEN register

1.4 SPIADR

SPI Address Register

Specifies the SPI address value

Absolute Address: 32'h1A10_200C
Base Offset: 32'h0000_000C
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:0]	SPIADR	RW	32'h0000_0000	SPI Address When performing a read or write transfer the SPI command is sent first before any data is read or written, after this the SPI address is sent. The lenght of the SPI command can be controlled with the SPILEN register

1.5 SPILEN

SPI Transfer Length Register

Defines the number of bits to be sent or received over SPI interface

Absolute Address: 32'h1A10_2010
Base Offset: 32'h0000_0010
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:16]	DATALEN	RW	16'h0000	SPI Data Length The number of bits read or written. Note that first the SPI command and address are written to an SPI slave device.
[15:14]	RESERVED14	RO	2'h0	Reserved14 Reserved for further usage
[13:8]	ADDRLEN	RW	6'h0	SPI Address Length The number of bits of the SPI Address that should be sent.
[7:6]	RESERVED6	RO	2'h0	Reserved6 Reserved for further usage
[5:0]	CMDLEN	RW	6'h0	SPI Command Length The number of bits of the SPI command that should be sent.

1.6 SPIDUM

SPI Dummy Cycles Register

Defines the dummy cycles between each spi transfer

Absolute Address: 32'h1A10_2014
Base Offset: 32'h0000_0014
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:16]	DUMMYWR	RW	16'h0000	Write Dummy Cycles Dummy cycles (nothing being written or read) between sending the SPI command + SPI address + writing the SPI data
[15:0]	DUMMYRD	RW	16'h0000	Read Dummy Cycles Dummy cycles (nothing being written or read) between sending the SPI command + SPI address + reading the SPI data

1.7 TXFIFO

SPI Transmit FIFO Register

Used for storing the data that'll be written into the FIFO

Absolute Address: 32'h1A10_2018
Base Offset: 32'h0000_0018
Reset: 32'h0000_0000
Access: WO
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:0]	TX	WO	32'h0000_0000	Transmit data Write data into the FIFO

1.8 RXFIFO

SPI Receive FIFO Register

Used for reading the data read from the FIFO

Absolute Address: 32'h1A10_2020
Base Offset: 32'h0000_0020
Reset: 32'h0000_0000
Access: RO
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31:0]	RX	RO	32'h0000_0000	Receive data Read data from the FIFO

1.9 INTCFG

SPI Interrupt Configuration Register

Defines the interrupt configuration for SPI module

Absolute Address: 32'h1A10_2024
Base Offset: 32'h0000_0024
Reset: 32'h0000_0000
Access: RW
Size(bytes): 0x4

Fields List

Bits	Identifier	Access	Reset	Name / Description
[31]	EN	RW	1'h0	Interrupt Enable Used for enabling the interrupts. TODO: Fill this based on the better RTL understanding
[30]	CNTEN	RW	1'h0	Count Enable Used for enabling the counters. TODO: Fill this based on the better RTL understanding
[29]	RESERVED29	RO	1'h0	Reserved29 Reserved bits for further usage. It is 1bit wide based on RTL BUFFER_DEPTH=10
[28:24]	CNTRX	RW	5'h0	Counter Receive The value of the receive counter to be specified. TODO: Fill this based on the better RTL understanding It is 5bits wide based on RTL BUFFER_DEPTH=10
[23:21]	RESERVED21	RO	3'h0	Reserved21 Reserved bits for further usage. It is 3bits wide based on RTL BUFFER_DEPTH=10
[20:16]	CNTTX	RW	5'h0	Counter Transmit The value of the transmit counter to be specified. TODO: Fill this based on the better RTL understanding It is 5bits wide based on RTL BUFFER_DEPTH=10
[15:13]	RESERVED13	RO	3'h0	Reserved13 Reserved bits for further usage. It is 3bits wide based on RTL BUFFER_DEPTH=10

Bits	Identifier	Access	Reset	Name / Description
[12:8]	RHTX	RW	5'h0	Receive Threshold The receive fifo threshold at which the event is generated. TODO: Fill this based on the better RTL understanding It is 5bits wide based on RTL BUFFER_DEPTH=10
[7:5]	RESERVED5	RO	3'h0	Reserved5 Reserved bits for further usage. It is 3bits wide based on RTL BUFFER_DEPTH=10
[4:0]	THTX	RW	5'h0	Transmit Threshold The transmit fifo threshold at which the event is generated. TODO: Fill this based on the better RTL understanding It is 5bits wide based on RTL BUFFER_DEPTH=10