Lab 2 – COVID version

Objectives

- Make sure Quartus Prime and tools are installed
- Verify joystick and buttons work with DE10-Lite board
- Understand how to get a project setup in Quartus Prime Lite.
- Understand how to use pin planner and assignment editor and configuration settings
- Understand how to use ADC IP.
- Understand terminology for ADC IP

Note

You should use the datasheets and course materials first. You can also use the internet, but your final work should be your own. If you copy and paste from the internet you will receive a zero for the entire assignment.

Here's a couple items that might be useful in answering the questions in this lab.

DE10-Lite User Manual

https://www.terasic.com.tw/cgi-bin/page/archive_download.pl?Language=English&No=1021&FID=a13a2782811152b477e60203d34b1baa

Intel® MAX® 10 Analog to Digital Converter User Guide

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/max-10/ug_m10_adc.pdf

Intel MAX 10 FPGA Device Overview

https://www.intel.com/content/www/us/en/programmable/documentation/myt1396938463674.html

Intel MAX 10 General Purpose I/O User Guide

https://www.intel.com/content/www/us/en/programmable/documentation/sam1393999966669.html

Intel MAX 10 FPGA Device Datasheet

https://www.intel.com/content/www/us/en/programmable/documentation/mcn1397700832153.html#mcn1397644005799

MAX 10 FPGA Device Architecture

https://www.intel.com/content/www/us/en/programmable/documentation/sss1397439908414.html

Initial Setup & Pin planner

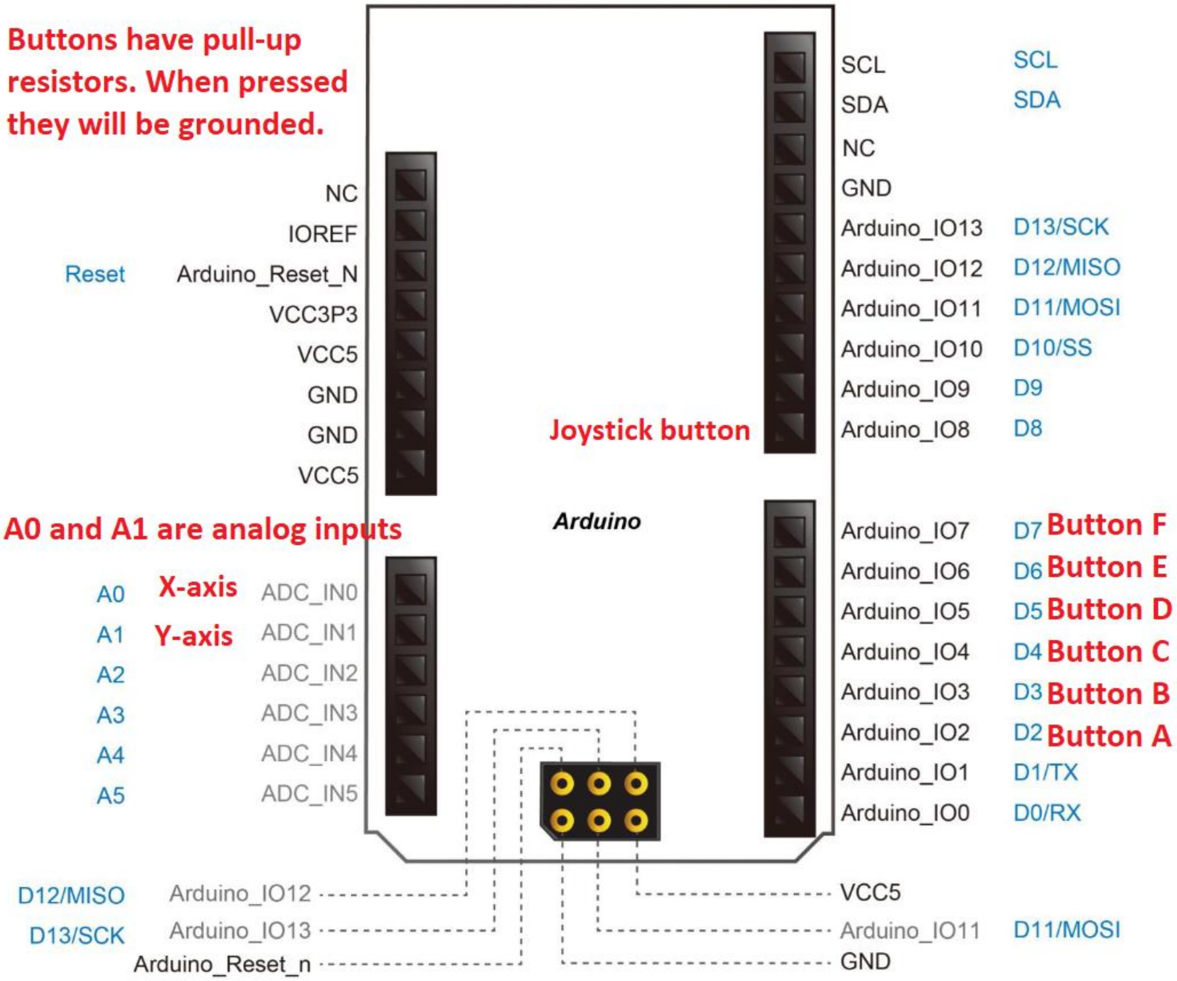
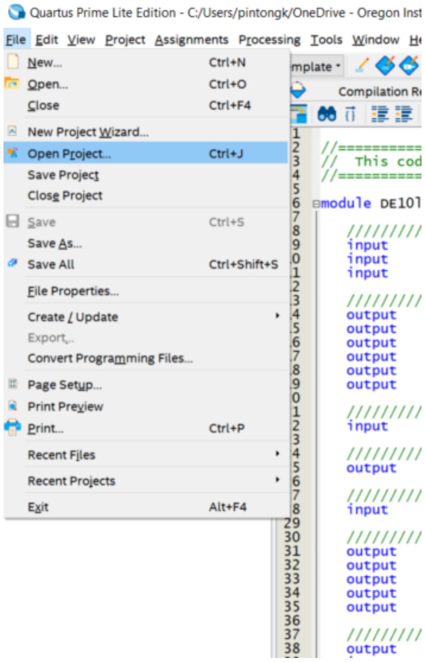


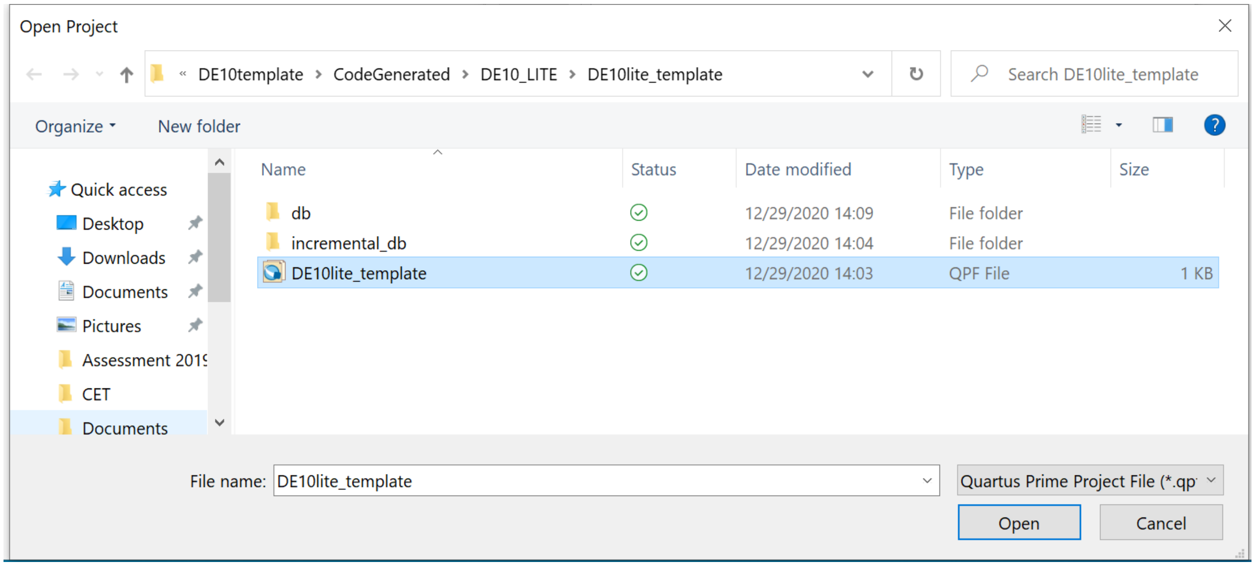
Figure 3-19 lists the all the pin-out signal name of the Arduino Uno connector. The blue font represents the Arduino pin-out definition.

1. Unzip the template folder to a location you can save.
2. Open Quartus Prime Lite
3. Go to File and open project.



```
//==========
//  This cod
//==========

module DE10l

    ////////
    input
    input
    input

    ////////
    output
    output
    output
    output
    output
    output

    ////////
    input

    ////////
    output

    ////////
    input

    ////////
    output
    output
    output
    output
    output

    ////////
    output
```

4. Open up the QPF template file.

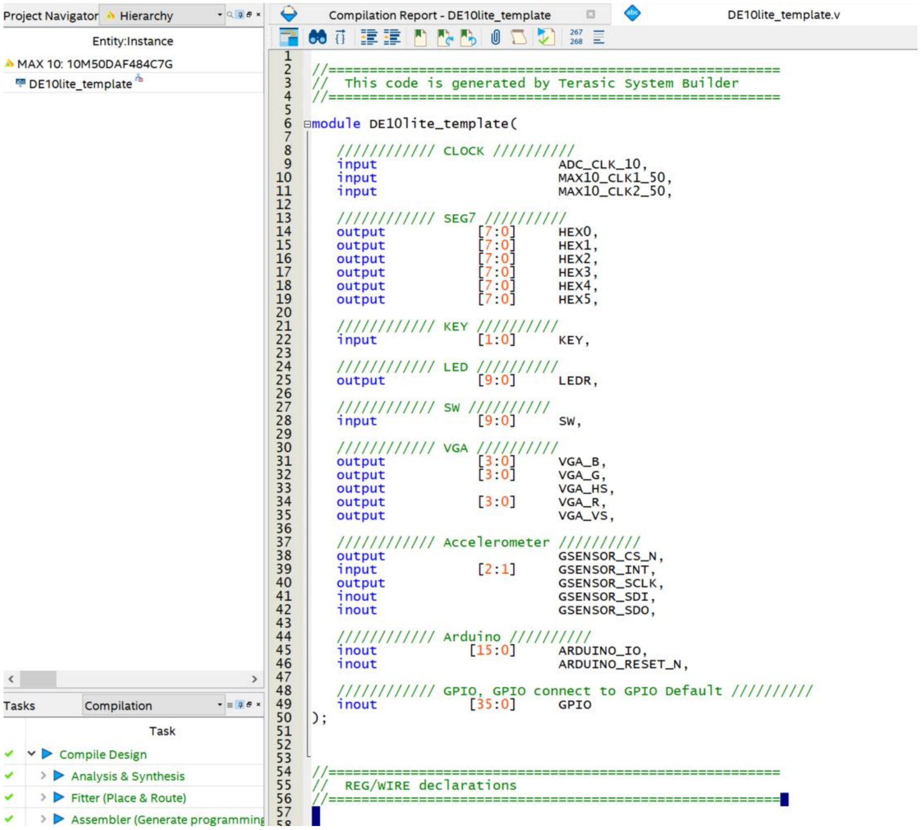


Name	Status	Date modified	Type	Size
db	✓	12/29/2020 14:09	File folder	
incremental_db	✓	12/29/2020 14:04	File folder	
DE10lite_template	✓	12/29/2020 14:03	QPF File	1 KB

File name: DE10lite_template

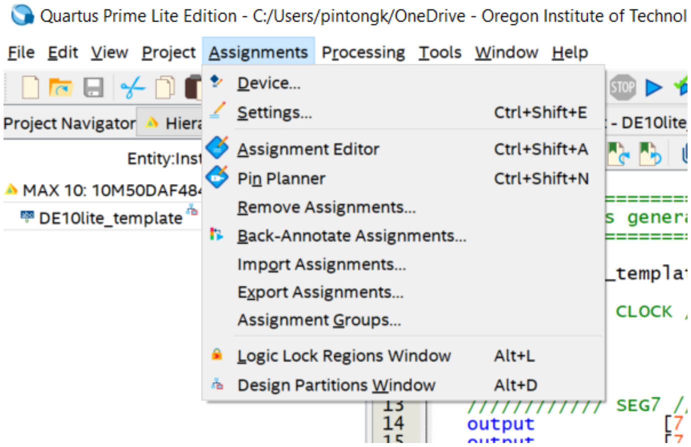
Quartus Prime Project File (*.qp

5. It should launch the template with the DE10lite_template. Double click on it and it should launch the DE10lite_template.v file.

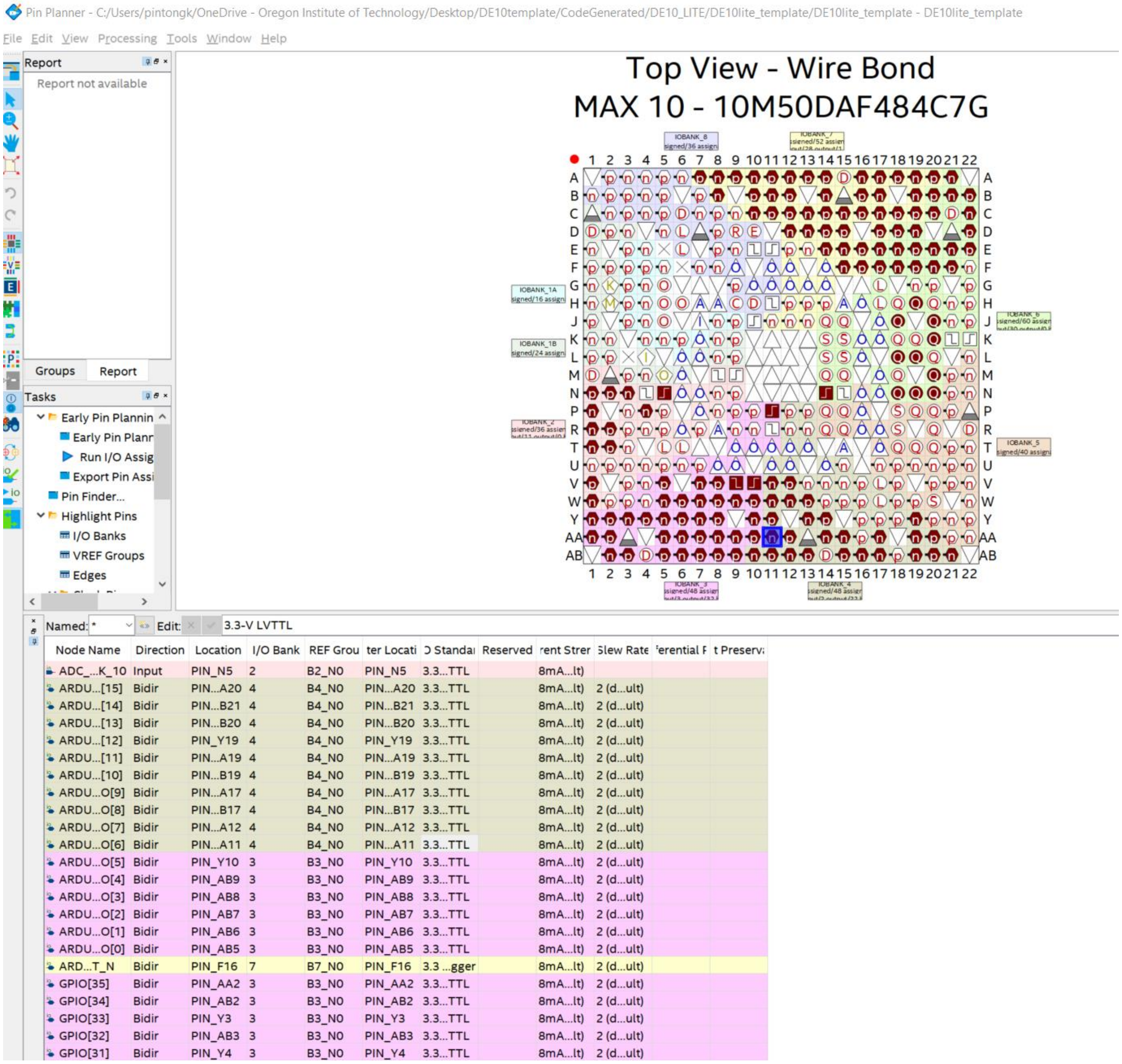


```

//=======================================================
//  This code is generated by Terasic System Builder
//=======================================================

module DE10lite_template(

   //////////// CLOCK //////////
   input                           ADC_CLK_10,
   input                           MAX10_CLK1_50,
   input                           MAX10_CLK2_50,

   //////////// SEG7 //////////
   output               [7:0]      HEX0,
   output               [7:0]      HEX1,
   output               [7:0]      HEX2,
   output               [7:0]      HEX3,
   output               [7:0]      HEX4,
   output               [7:0]      HEX5,

   //////////// KEY //////////
   input                [1:0]      KEY,

   //////////// LED //////////
   output               [9:0]      LEDR,

   //////////// SW //////////
   input                [9:0]      SW,

   //////////// VGA //////////
   output               [3:0]      VGA_B,
   output               [3:0]      VGA_G,
   output                          VGA_HS,
   output               [3:0]      VGA_R,
   output                          VGA_VS,

   //////////// Accelerometer //////////
   output                          GSENSOR_CS_N,
   input                [2:1]      GSENSOR_INT,
   output                          GSENSOR_SCLK,
   inout                           GSENSOR_SDI,
   inout                           GSENSOR_SDO,

   //////////// Arduino //////////
   inout               [15:0]      ARDUINO_IO,
   inout                           ARDUINO_RESET_N,

   //////////// GPIO, GPIO connect to GPIO Default //////////
   inout               [35:0]      GPIO
);


//=======================================================
//  REG/WIRE declarations
//=======================================================
```

6. Click on Assignments > Pin Planner


Quartus Prime Lite Edition - C:/Users/pintongk/OneDrive - Oregon Institute of Technol
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hiera
Entity:Inst
MAX 10: 10M50DAF48
DE10lite_template
Device...
Settings... Ctrl+Shift+E
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
Logic Lock Regions Window Alt+L
Design Partitions Window Alt+D
- DE10lite
s generi
_templa
CLOCK
SEG7
output
[7

7. Something like this should launch. This is essentially the pinout on the BGA of the MAX10 device on the DE10-Lite board. You can see there are different pins such as ground, differential pair, and different power banks.



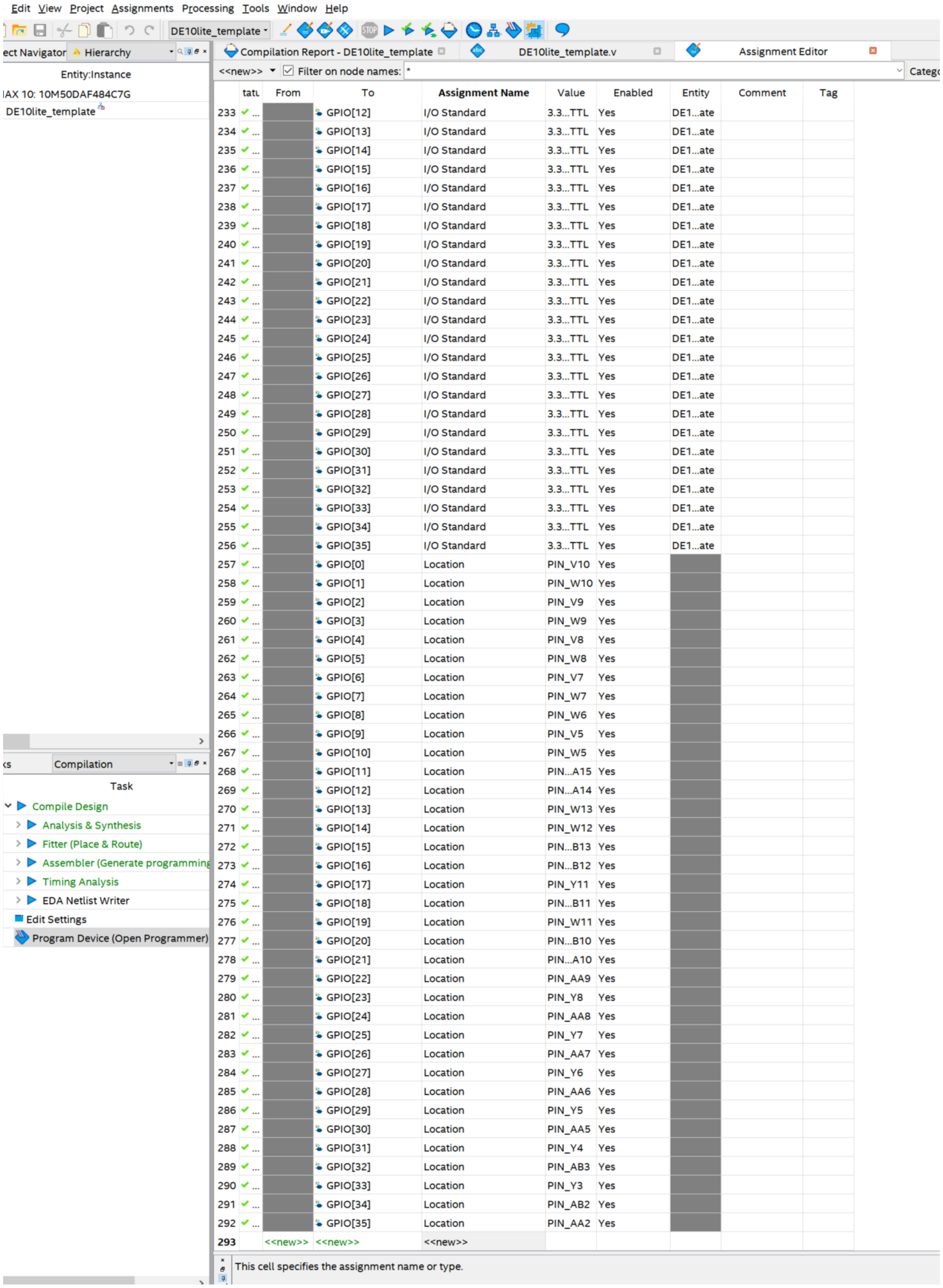
Pin Planner - C:/Users/pintongk/OneDrive - Oregon Institute of Technology/Desktop/DE10template/CodeGenerated/DE10_LITE/DE10lite_template/DE10lite_template - DE10lite_template

Named: * Edit: 3.3-V LVTTL

Node Name	Direction	Location	I/O Bank	REF Grou	ter Locati	⊃ Standa	Reserved	rent Strer	Slew Rate	ferential F	t Preserv
ADC_...K_10	Input	PIN_N5	2	B2_N0	PIN_N5	3.3...TTL		8mA...lt)			
ARDU...[15]	Bidir	PIN...A20	4	B4_N0	PIN...A20	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...[14]	Bidir	PIN...B21	4	B4_N0	PIN...B21	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...[13]	Bidir	PIN...B20	4	B4_N0	PIN...B20	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...[12]	Bidir	PIN_Y19	4	B4_N0	PIN_Y19	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...[11]	Bidir	PIN...A19	4	B4_N0	PIN...A19	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...[10]	Bidir	PIN...B19	4	B4_N0	PIN...B19	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[9]	Bidir	PIN...A17	4	B4_N0	PIN...A17	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[8]	Bidir	PIN...B17	4	B4_N0	PIN...B17	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[7]	Bidir	PIN...A12	4	B4_N0	PIN...A12	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[6]	Bidir	PIN...A11	4	B4_N0	PIN...A11	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[5]	Bidir	PIN_Y10	3	B3_N0	PIN_Y10	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[4]	Bidir	PIN_AB9	3	B3_N0	PIN_AB9	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[3]	Bidir	PIN_AB8	3	B3_N0	PIN_AB8	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[2]	Bidir	PIN_AB7	3	B3_N0	PIN_AB7	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[1]	Bidir	PIN_AB6	3	B3_N0	PIN_AB6	3.3...TTL		8mA...lt)	2 (d...ult)		
ARDU...O[0]	Bidir	PIN_AB5	3	B3_N0	PIN_AB5	3.3...TTL		8mA...lt)	2 (d...ult)		
ARD...T_N	Bidir	PIN_F16	7	B7_N0	PIN_F16	3.3 ...gger		8mA...lt)	2 (d...ult)		
GPIO[35]	Bidir	PIN_AA2	3	B3_N0	PIN_AA2	3.3...TTL		8mA...lt)	2 (d...ult)		
GPIO[34]	Bidir	PIN_AB2	3	B3_N0	PIN_AB2	3.3...TTL		8mA...lt)	2 (d...ult)		
GPIO[33]	Bidir	PIN_Y3	3	B3_N0	PIN_Y3	3.3...TTL		8mA...lt)	2 (d...ult)		
GPIO[32]	Bidir	PIN_AB3	3	B3_N0	PIN_AB3	3.3...TTL		8mA...lt)	2 (d...ult)		
GPIO[31]	Bidir	PIN_Y4	3	B3_N0	PIN_Y4	3.3...TTL		8mA...lt)	2 (d...ult)		

8. This is where you can change Node names, change the pin that you map a specific name to, change the direction (input, output, bidirectional), change the IO standard, slew rate.

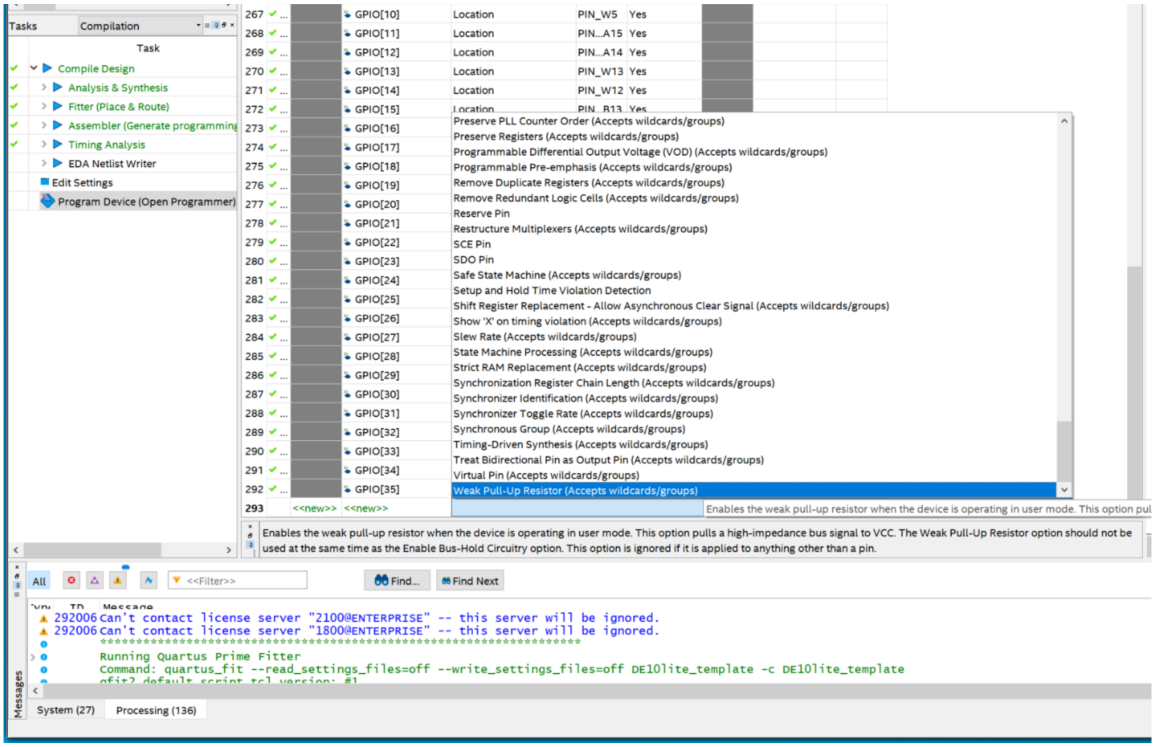
9. Now, let’s exit out of Pin Planner and go to Assignments > Assignment Editor in the main quartus window.



	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
233	✓ ...		GPIO[12]	I/O Standard	3.3...TTL	Yes	DE1...ate		
234	✓ ...		GPIO[13]	I/O Standard	3.3...TTL	Yes	DE1...ate		
235	✓ ...		GPIO[14]	I/O Standard	3.3...TTL	Yes	DE1...ate		
236	✓ ...		GPIO[15]	I/O Standard	3.3...TTL	Yes	DE1...ate		
237	✓ ...		GPIO[16]	I/O Standard	3.3...TTL	Yes	DE1...ate		
238	✓ ...		GPIO[17]	I/O Standard	3.3...TTL	Yes	DE1...ate		
239	✓ ...		GPIO[18]	I/O Standard	3.3...TTL	Yes	DE1...ate		
240	✓ ...		GPIO[19]	I/O Standard	3.3...TTL	Yes	DE1...ate		
241	✓ ...		GPIO[20]	I/O Standard	3.3...TTL	Yes	DE1...ate		
242	✓ ...		GPIO[21]	I/O Standard	3.3...TTL	Yes	DE1...ate		
243	✓ ...		GPIO[22]	I/O Standard	3.3...TTL	Yes	DE1...ate		
244	✓ ...		GPIO[23]	I/O Standard	3.3...TTL	Yes	DE1...ate		
245	✓ ...		GPIO[24]	I/O Standard	3.3...TTL	Yes	DE1...ate		
246	✓ ...		GPIO[25]	I/O Standard	3.3...TTL	Yes	DE1...ate		
247	✓ ...		GPIO[26]	I/O Standard	3.3...TTL	Yes	DE1...ate		
248	✓ ...		GPIO[27]	I/O Standard	3.3...TTL	Yes	DE1...ate		
249	✓ ...		GPIO[28]	I/O Standard	3.3...TTL	Yes	DE1...ate		
250	✓ ...		GPIO[29]	I/O Standard	3.3...TTL	Yes	DE1...ate		
251	✓ ...		GPIO[30]	I/O Standard	3.3...TTL	Yes	DE1...ate		
252	✓ ...		GPIO[31]	I/O Standard	3.3...TTL	Yes	DE1...ate		
253	✓ ...		GPIO[32]	I/O Standard	3.3...TTL	Yes	DE1...ate		
254	✓ ...		GPIO[33]	I/O Standard	3.3...TTL	Yes	DE1...ate		
255	✓ ...		GPIO[34]	I/O Standard	3.3...TTL	Yes	DE1...ate		
256	✓ ...		GPIO[35]	I/O Standard	3.3...TTL	Yes	DE1...ate		
257	✓ ...		GPIO[0]	Location	PIN_V10	Yes			
258	✓ ...		GPIO[1]	Location	PIN_W10	Yes			
259	✓ ...		GPIO[2]	Location	PIN_V9	Yes			
260	✓ ...		GPIO[3]	Location	PIN_W9	Yes			
261	✓ ...		GPIO[4]	Location	PIN_V8	Yes			
262	✓ ...		GPIO[5]	Location	PIN_W8	Yes			
263	✓ ...		GPIO[6]	Location	PIN_V7	Yes			
264	✓ ...		GPIO[7]	Location	PIN_W7	Yes			
265	✓ ...		GPIO[8]	Location	PIN_W6	Yes			
266	✓ ...		GPIO[9]	Location	PIN_V5	Yes			
267	✓ ...		GPIO[10]	Location	PIN_W5	Yes			
268	✓ ...		GPIO[11]	Location	PIN...A15	Yes			
269	✓ ...		GPIO[12]	Location	PIN...A14	Yes			
270	✓ ...		GPIO[13]	Location	PIN_W13	Yes			
271	✓ ...		GPIO[14]	Location	PIN_W12	Yes			
272	✓ ...		GPIO[15]	Location	PIN...B13	Yes			
273	✓ ...		GPIO[16]	Location	PIN...B12	Yes			
274	✓ ...		GPIO[17]	Location	PIN_Y11	Yes			
275	✓ ...		GPIO[18]	Location	PIN...B11	Yes			
276	✓ ...		GPIO[19]	Location	PIN_W11	Yes			
277	✓ ...		GPIO[20]	Location	PIN...B10	Yes			
278	✓ ...		GPIO[21]	Location	PIN...A10	Yes			
279	✓ ...		GPIO[22]	Location	PIN_AA9	Yes			
280	✓ ...		GPIO[23]	Location	PIN_Y8	Yes			
281	✓ ...		GPIO[24]	Location	PIN_AA8	Yes			
282	✓ ...		GPIO[25]	Location	PIN_Y7	Yes			
283	✓ ...		GPIO[26]	Location	PIN_AA7	Yes			
284	✓ ...		GPIO[27]	Location	PIN_Y6	Yes			
285	✓ ...		GPIO[28]	Location	PIN_AA6	Yes			
286	✓ ...		GPIO[29]	Location	PIN_Y5	Yes			
287	✓ ...		GPIO[30]	Location	PIN_AA5	Yes			
288	✓ ...		GPIO[31]	Location	PIN_Y4	Yes			
289	✓ ...		GPIO[32]	Location	PIN_AB3	Yes			
290	✓ ...		GPIO[33]	Location	PIN_Y3	Yes			
291	✓ ...		GPIO[34]	Location	PIN_AB2	Yes			
292	✓ ...		GPIO[35]	Location	PIN_AA2	Yes			
293		<<new>>	<<new>>	<<new>>					

This cell specifies the assignment name or type.

10. You can configure pins using Assignment Editor as well. For instance, if you need to apply a pull-up or pull-down resistor to GPIO[24], you could go under new and program it. (Don't do it.)



Tasks Compilation

Task

- ✓ Compile Design
  - ✓ Analysis & Synthesis
  - ✓ Fitter (Place & Route)
  - ✓ Assembler (Generate programming
  - ✓ Timing Analysis
  - EDA Netlist Writer
- Edit Settings
- Program Device (Open Programmer)

267	✓ ...		GPIO[10]	Location	PIN_W5	Yes
268	✓ ...		GPIO[11]	Location	PIN...A15	Yes
269	✓ ...		GPIO[12]	Location	PIN...A14	Yes
270	✓ ...		GPIO[13]	Location	PIN_W13	Yes
271	✓ ...		GPIO[14]	Location	PIN_W12	Yes
272	✓ ...		GPIO[15]	Location	PIN_B13	Yes
273	✓ ...		GPIO[16]			
274	✓ ...		GPIO[17]			
275	✓ ...		GPIO[18]			
276	✓ ...		GPIO[19]			
277	✓ ...		GPIO[20]			
278	✓ ...		GPIO[21]			
279	✓ ...		GPIO[22]			
280	✓ ...		GPIO[23]			
281	✓ ...		GPIO[24]			
282	✓ ...		GPIO[25]			
283	✓ ...		GPIO[26]			
284	✓ ...		GPIO[27]			
285	✓ ...		GPIO[28]			
286	✓ ...		GPIO[29]			
287	✓ ...		GPIO[30]			
288	✓ ...		GPIO[31]			
289	✓ ...		GPIO[32]			
290	✓ ...		GPIO[33]			
291	✓ ...		GPIO[34]			
292	✓ ...		GPIO[35]			
293		<<new>>	<<new>>			

Preserve PLL Counter Order (Accepts wildcards/groups)
Preserve Registers (Accepts wildcards/groups)
Programmable Differential Output Voltage (VOD) (Accepts wildcards/groups)
Programmable Pre-emphasis (Accepts wildcards/groups)
Remove Duplicate Registers (Accepts wildcards/groups)
Remove Redundant Logic Cells (Accepts wildcards/groups)
Reserve Pin
Restructure Multiplexers (Accepts wildcards/groups)
SCE Pin
SDO Pin
Safe State Machine (Accepts wildcards/groups)
Setup and Hold Time Violation Detection
Shift Register Replacement - Allow Asynchronous Clear Signal (Accepts wildcards/groups)
Show 'X' on timing violation (Accepts wildcards/groups)
Slew Rate (Accepts wildcards/groups)
State Machine Processing (Accepts wildcards/groups)
Strict RAM Replacement (Accepts wildcards/groups)
Synchronization Register Chain Length (Accepts wildcards/groups)
Synchronizer Identification (Accepts wildcards/groups)
Synchronizer Toggle Rate (Accepts wildcards/groups)
Synchronous Group (Accepts wildcards/groups)
Timing-Driven Synthesis (Accepts wildcards/groups)
Treat Bidirectional Pin as Output Pin (Accepts wildcards/groups)
Virtual Pin (Accepts wildcards/groups)
Weak Pull-Up Resistor (Accepts wildcards/groups)

Enables the weak pull-up resistor when the device is operating in user mode. This option pul

Enables the weak pull-up resistor when the device is operating in user mode. This option pulls a high-impedance bus signal to VCC. The Weak Pull-Up Resistor option should not be used at the same time as the Enable Bus-Hold Circuitry option. This option is ignored if it is applied to anything other than a pin.

```
Type ID     Message
  292006 Can't contact license server "2100@ENTERPRISE" -- this server will be ignored.
  292006 Can't contact license server "1800@ENTERPRISE" -- this server will be ignored.
         ******************************************************************
         Running Quartus Prime Fitter
         Command: quartus_fit --read_settings_files=off --write_settings_files=off DE10lite_template -c DE10lite_template
         qfit2_default_script.tcl version: #1
```

System (27)   Processing (136)

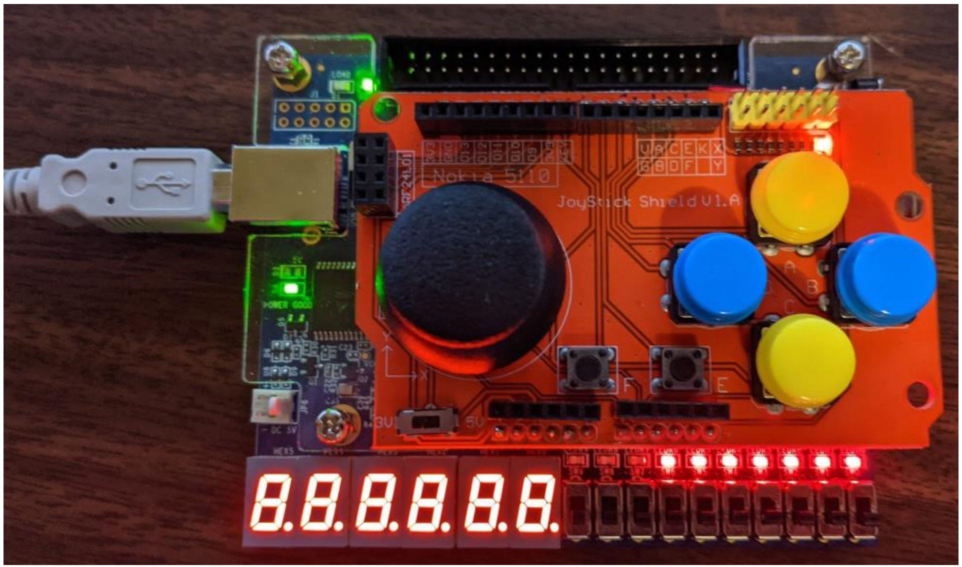
11. Please answer the following in a new word document.
    a. What is banking? How many banks are on this FPGA? Why is having different banks useful?
    b. There is an I/O standard setting that you can change. What's the difference between 3.3V TTL and 3.3 V LVCMOS?
    c. What does changing the current strength do? Why would you want to increase or decrease the current strength?
    d. What does changing the slew rate do? Why would you want to change it?
    e. Do you always want the most current and highest slew rate? Why or why not?

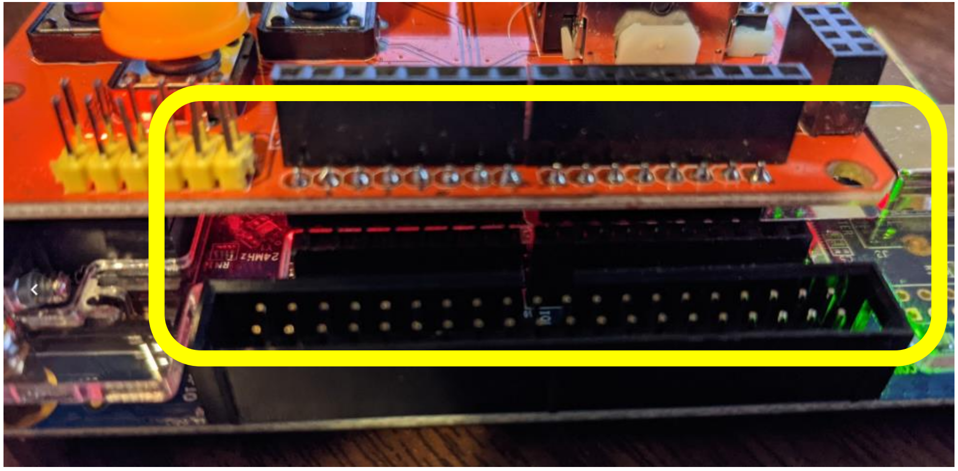
Pull-up/Pull-down testing the digital inputs on the DE10-Lite and Joystick board

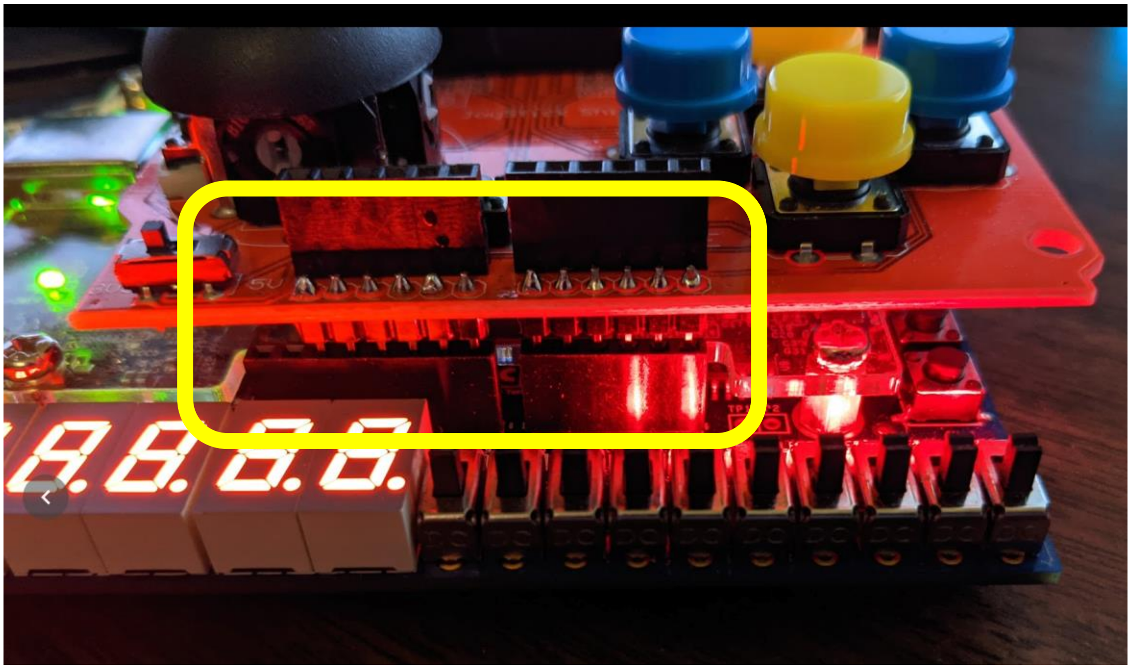
1. **WARNING**! You need to turn off the board before plugging in the joystick shield to prevent damage to the board.

   WARNING! You need to make sure you align the shield in the correct positions.

   WARNING! There are no replacement shields. You will be responsible for ordering replacements on your own if you break your shield.
   Correctly plug the joystick shield into the board.



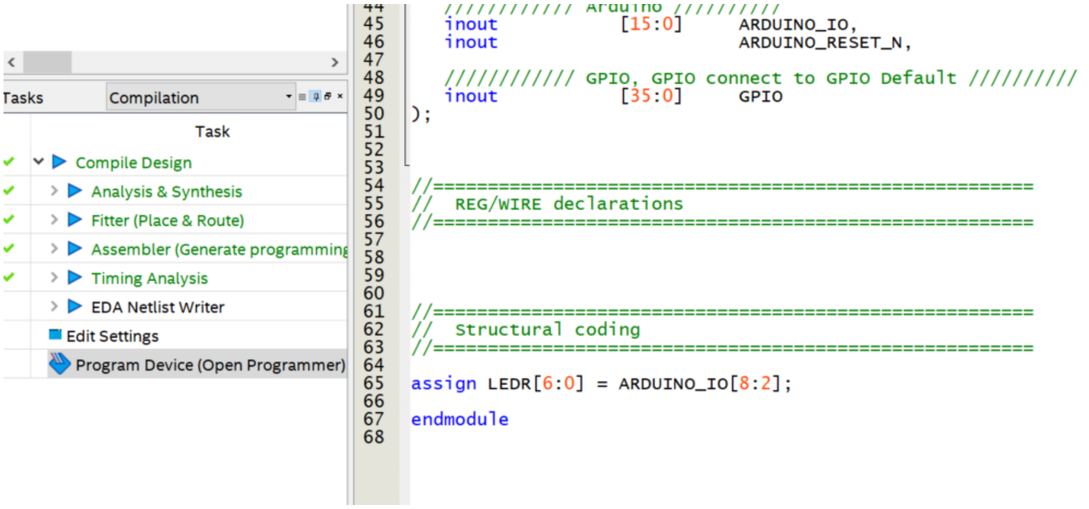




2. In the code section, let’s test that your buttons work.

   Type in the following assign statement on line 65 to connect the LEDR[6:0] to the Arduino_IO headers. The ArduinoIO pins 2,3,4,5,6,7,8 are connected to the buttons. These buttons are active low. When pressed, they will pull to ground (logic 0), and when left alone they will be pulled up to the voltage source (3.3 V) (logic 1).

   You need to also go to line 45 and 46, and change the arduinoIO into inputs only for now.

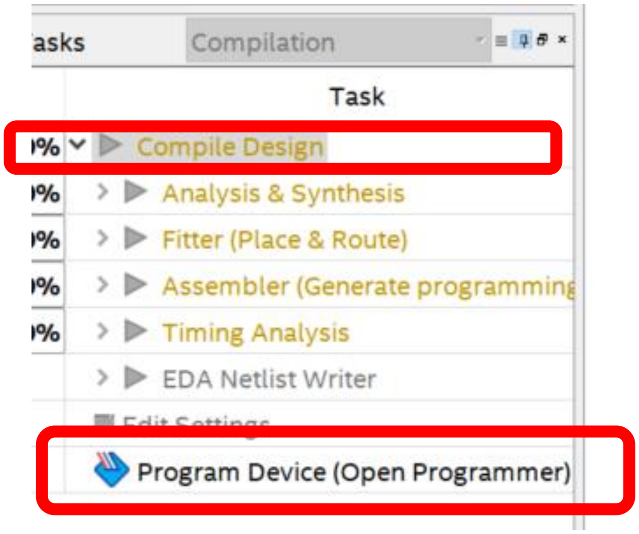


```
44     //////////// Arduino //////////
45     inout          [15:0]      ARDUINO_IO,
46     inout                      ARDUINO_RESET_N,
47
48     //////////// GPIO, GPIO connect to GPIO Default //////////
49     inout          [35:0]      GPIO
50  );
51
52
53
54  //=======================================================
55  //  REG/WIRE declarations
56  //=======================================================
57
58
59
60
61  //=======================================================
62  //  Structural coding
63  //=======================================================
64
65  assign LEDR[6:0] = ARDUINO_IO[8:2];
66
67  endmodule
68
```

3. Questions: Please draw how a single button is connected to the FPGA using a pull-up resistor.
4. Question: What is the difference between pullup and pulldown? Please draw a single button using pull-down.
5. Question: Does the MAX10 FPGA have both internal pullups and pulldowns available? Where in the datasheet does it describe this functionality? Link or snipping is fine.

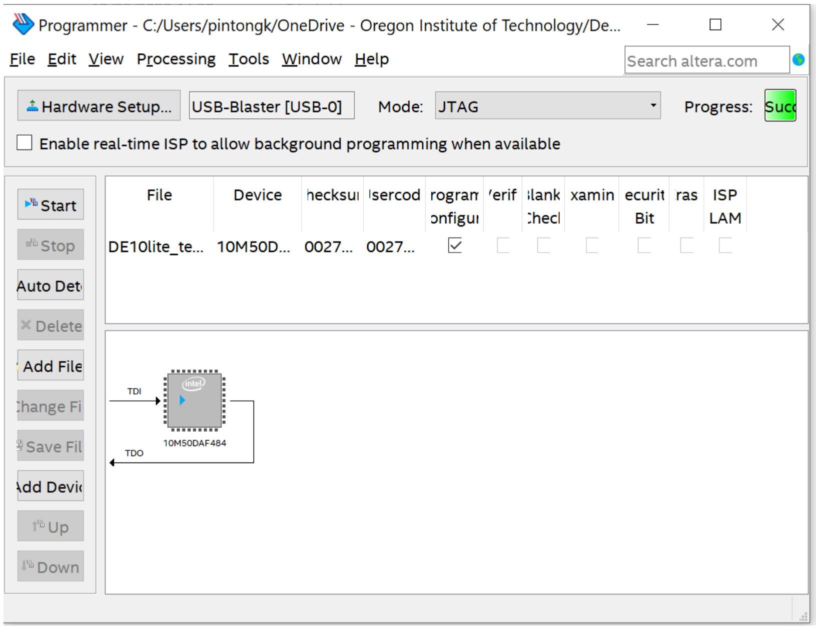
6. How would you enable an internal pull-up or pull-down?

7. Ok, now double-click compile design and program the device.



8. After it's successful (If it's red, it is not successful.) Double click on Program Device.

9. This window should launch. If you do not see USB-Blaster, might need to click on Hardware Setup and double click on the USB-Blaster.


Programmer - C:/Users/pintongk/OneDrive - Oregon Institute of Technology/De...
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
Start
Stop
Auto Det
Delete
Add File
Change Fi
Save Fil
Add Devic
Up
Down
TDI
TDO
10M50DAF484

USB-Blaster [USB-0] Mode: JTAG Progress: Succ

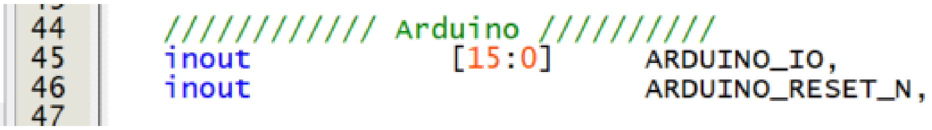
□ Enable real-time ISP to allow background programming when available

File	Device	hecksu	Isercod	rogran onfigu	'erif	ilank Checl	xamin	ecurit Bit	ras	ISP LAM
DE10lite_te...	10M50D...	0027...	0027...	☑	□	□	□	□	□	□

10. Click Start and then test that LEDS 6:0 are on. Press each button including the joystick. Each button should turn off the LED as it is pressed. Verify that this is the case and show instructor.

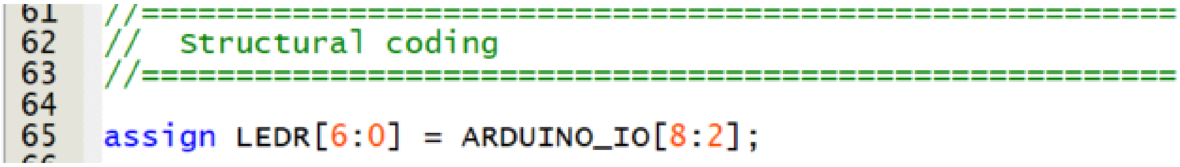
Tristate usage

1. Let’s go back to line 45 and 46 and change them back to inout. Changing them to inout allows us to use the pins as inputs or outputs. But earlier, if you left them that way, it would not work. How to use tri-state?



```
44      //////////// Arduino //////////
45      inout           [15:0]      ARDUINO_IO,
46      inout                       ARDUINO_RESET_N,
47
```

2. We can’t just use the code below with the inout. It may not work.



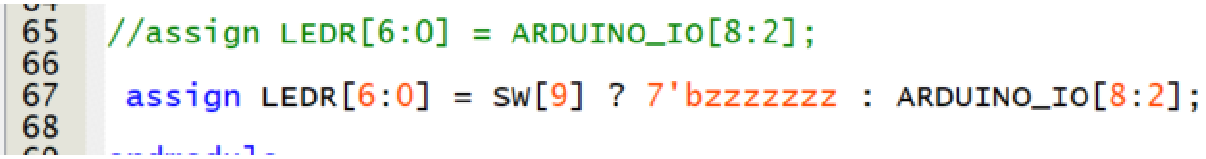
```
61   //=======================================================
62   //  Structural coding
63   //=======================================================
64
65   assign LEDR[6:0] = ARDUINO_IO[8:2];
```

3. So what do we do? We need to implement tristate buffer.

4. Please draw one tristate buffer below and explain in your own words what tristate buffer is, and how tri-state works. This should have been covered in CST 133 and CST 162, but you can use the internet if you wish. **Just make sure that your answer is in your own words or drawing.**

   1. Draw the tristate buffer
   2. Explain what is tristate?
   3. How does tristate work?
   4. What could it be used for?

5. So, how does it work in Verilog? Copy and paste the code below and compile.



```
65   //assign LEDR[6:0] = ARDUINO_IO[8:2];
66
67    assign LEDR[6:0] = SW[9] ? 7'bzzzzzzz : ARDUINO_IO[8:2];
68
```

6. Please explain what line 67 is doing.
7. Ok, now demonstrate to your instructor tristate functionality.

Configuring ADC IP

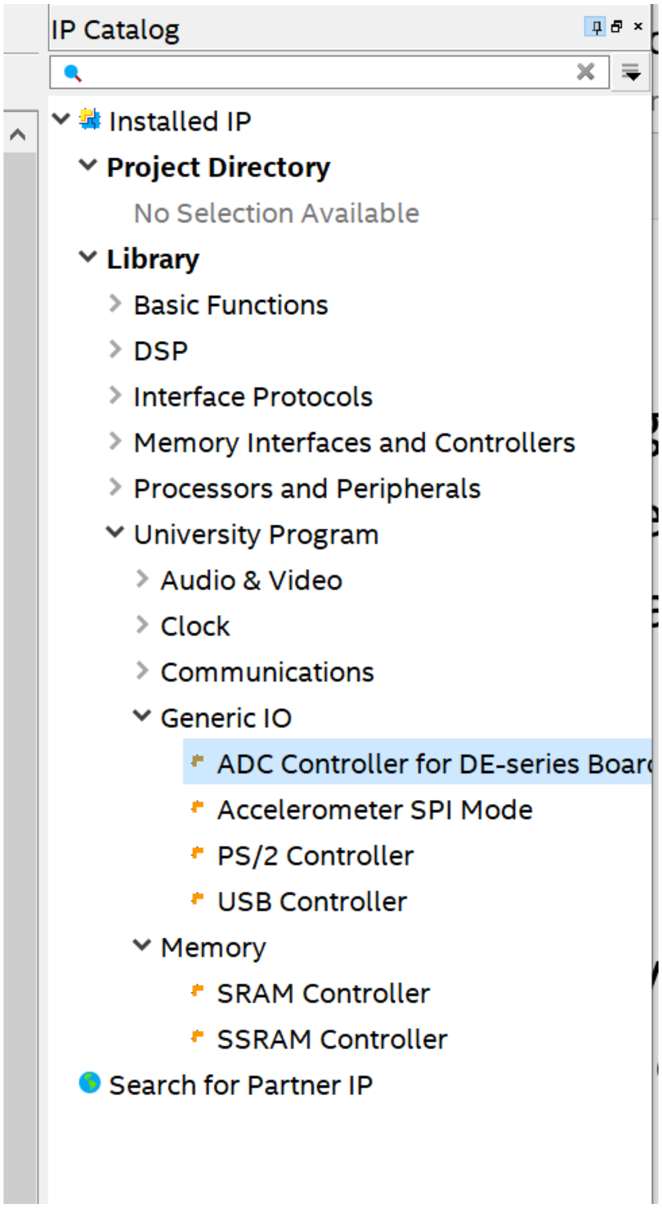
1. We discussed what IP was in class, and the ADC IP as well. The Joystick interfacing requires the use of an ADC because the joystick outputs two analog values. One is X0, the other is Y0, and they are assigned to A0 and A1 respectively. The ADC IP will read the value of X0 and Y0.

2. Answer the following
   a. How many bits ADC is the MAX10 built in ADC, and what is the sampling rate for this ADC? Give me a link to where you found this.

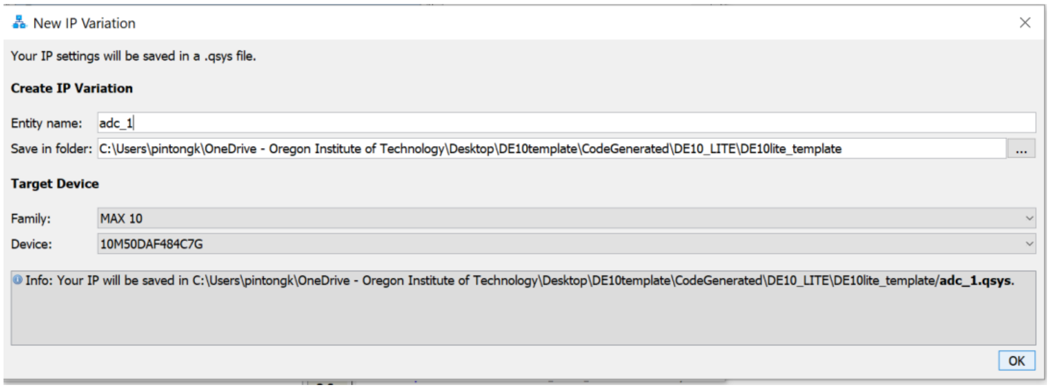
   b. How many channels does the MAX10 device on the DE10-Lite board support? Give me a link to where you found this.

   c. If an ADC is 10-bit resolution and the voltage range is 10 V, what is the step size of each value?

3. Go to IP catalog and double click on ADC Controller for DE-series Board IP core.



4. Call your ADC adc_1 and make sure you have the Target device selected as below.



Your IP settings will be saved in a .qsys file.

Create IP Variation

Entity name: adc_1

Save in folder: C:\Users\pintongk\OneDrive - Oregon Institute of Technology\Desktop\DE10template\CodeGenerated\DE10_LITE\DE10lite_template

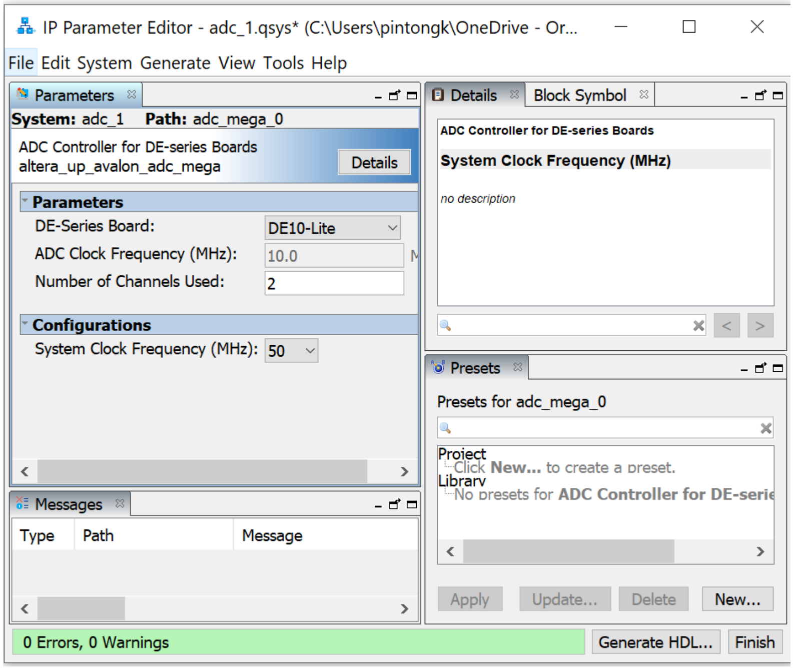
Target Device

Family: MAX 10

Device: 10M50DAF484C7G

Info: Your IP will be saved in C:\Users\pintongk\OneDrive - Oregon Institute of Technology\Desktop\DE10template\CodeGenerated\DE10_LITE\DE10lite_template/**adc_1.qsys**.

5. 5. Select the DE10-Lite board and make sure you select 2 channels, and 50 MHz system clock frequency. Then click Generate HDL.



IP Parameter Editor - adc_1.qsys* (C:\Users\pintongk\OneDrive - Or...

System: adc_1 Path: adc_mega_0

ADC Controller for DE-series Boards
altera_up_avalon_adc_mega

Parameters

DE-Series Board:	DE10-Lite
ADC Clock Frequency (MHz):	10.0
Number of Channels Used:	2

Configurations

System Clock Frequency (MHz):	50

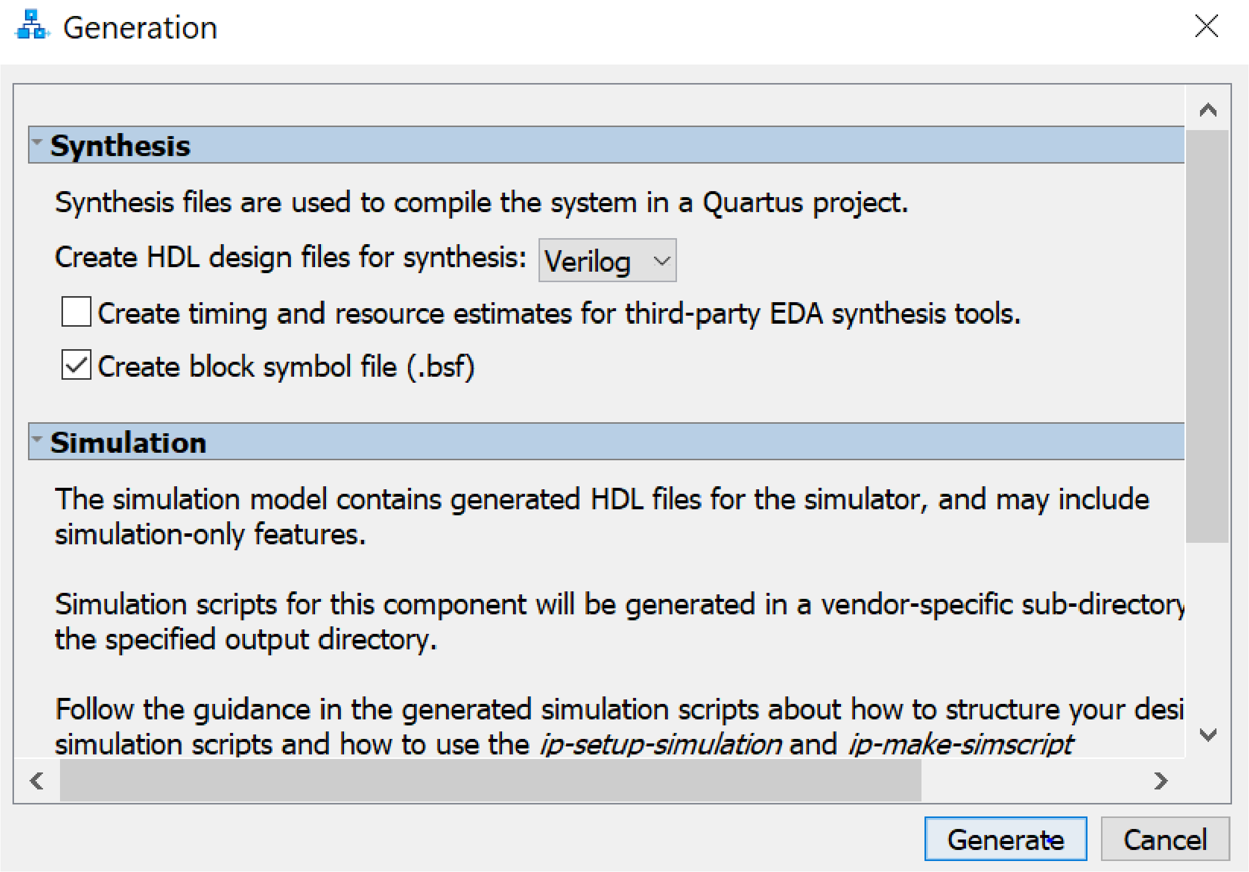
ADC Controller for DE-series Boards
System Clock Frequency (MHz)
no description

Presets for adc_mega_0

Project
Click **New...** to create a preset.
Library
No presets for **ADC Controller for DE-serie**

0 Errors, 0 Warnings

6. Make sure you select Verilog.



Generation

Synthesis

Synthesis files are used to compile the system in a Quartus project.

Create HDL design files for synthesis: Verilog

□ Create timing and resource estimates for third-party EDA synthesis tools.

☑ Create block symbol file (.bsf)

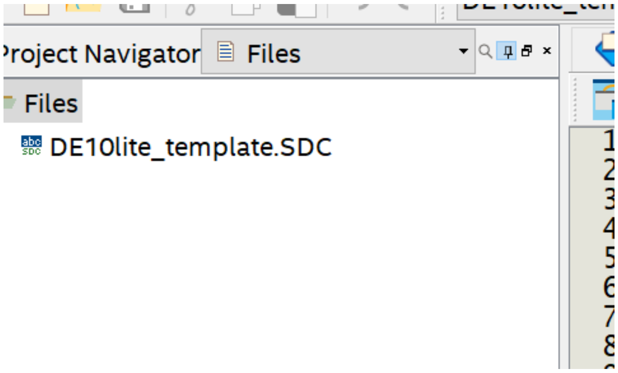
Simulation

The simulation model contains generated HDL files for the simulator, and may include simulation-only features.

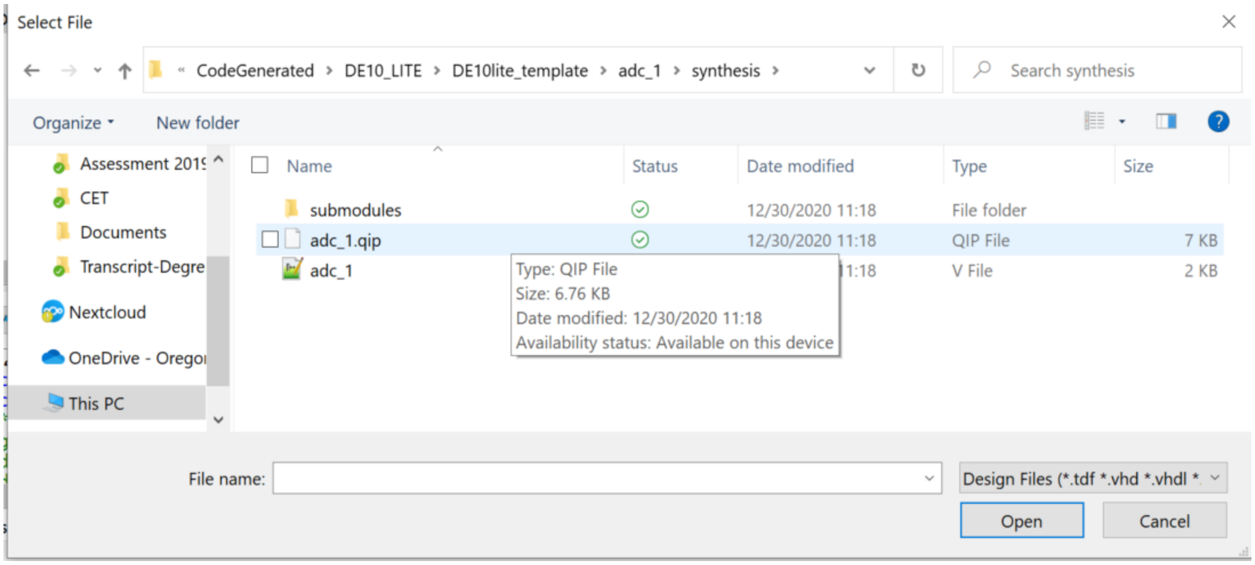
Simulation scripts for this component will be generated in a vendor-specific sub-directory the specified output directory.

Follow the guidance in the generated simulation scripts about how to structure your desi simulation scripts and how to use the *ip-setup-simulation* and *ip-make-simscript*

7. Go to project navigator and right click on the Files menu. Add the QIP file.



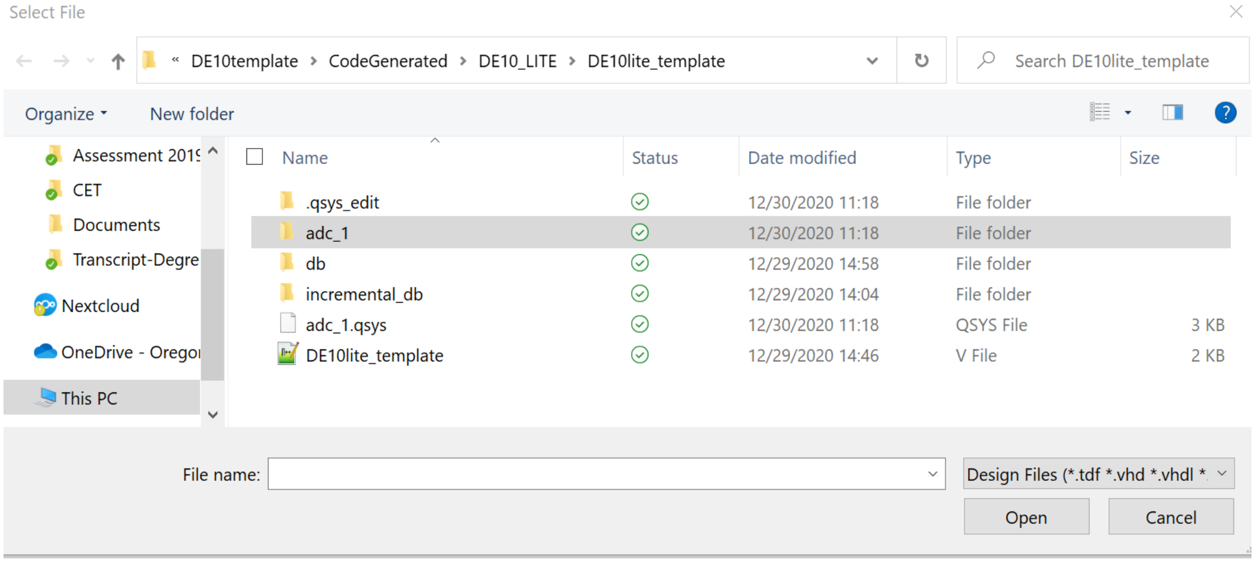
8. See the adc_1.qip file below? Add it. See the adc_1.v file below as well? Don't add it, but go and open the file. It will be a template showing you what the Verilog module is called, and what needs to be fed in and out of the module.



Name	Status	Date modified	Type	Size
submodules	✓	12/30/2020 11:18	File folder	
adc_1.qip	✓	12/30/2020 11:18	QIP File	7 KB
adc_1		11:18	V File	2 KB

Type: QIP File
Size: 6.76 KB
Date modified: 12/30/2020 11:18
Availability status: Available on this device

9. If you need to modify the IP core, you can open the qsys file using Platform Designer.



Select File

« DE10template › CodeGenerated › DE10_LITE › DE10lite_template

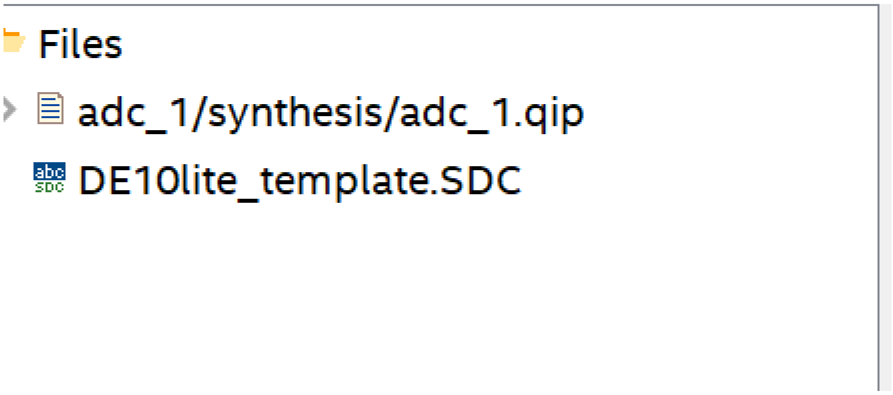
Search DE10lite_template

Name	Status	Date modified	Type	Size
.qsys_edit	✓	12/30/2020 11:18	File folder	
adc_1	✓	12/30/2020 11:18	File folder	
db	✓	12/29/2020 14:58	File folder	
incremental_db	✓	12/29/2020 14:04	File folder	
adc_1.qsys	✓	12/30/2020 11:18	QSYS File	3 KB
DE10lite_template	✓	12/29/2020 14:46	V File	2 KB

File name:

Design Files (*.tdf *.vhd *.vhdl *.

10. After adding, make sure the adc_1.qip shows up in the Project Navigator.

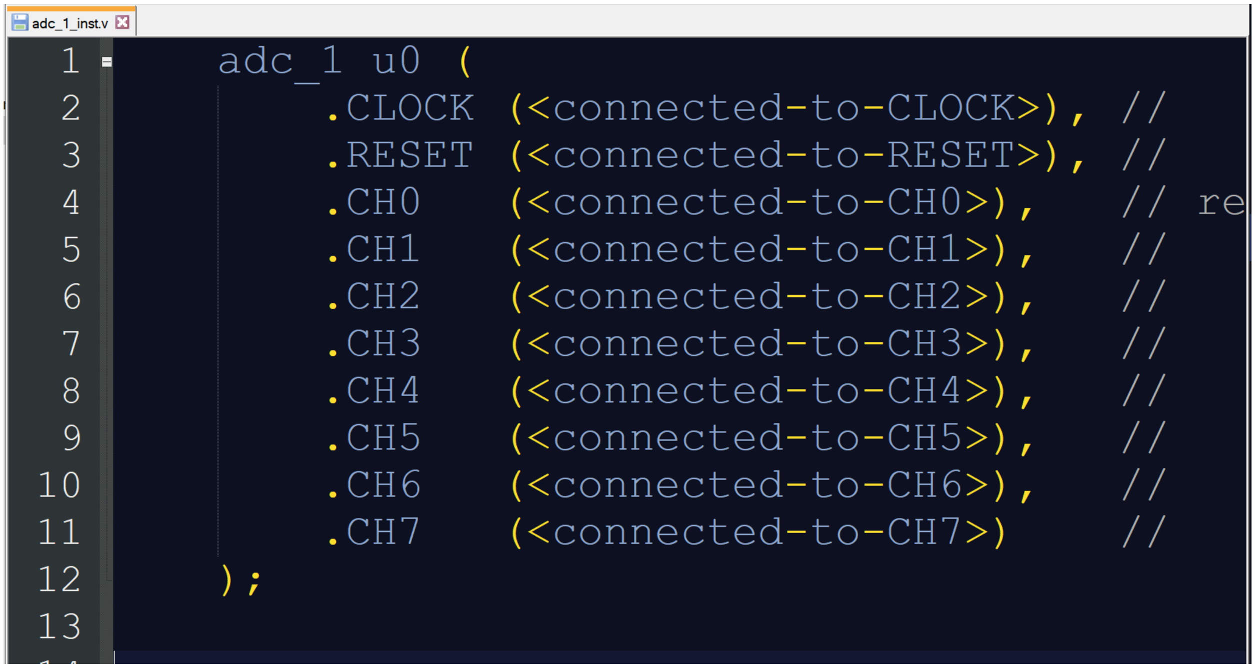


Files

adc_1/synthesis/adc_1.qip

DE10lite_template.SDC

11. This is an example of how to instantiate the file. In this case, we need to feed signals into CLOCK and RESET. The X and Y axis will come out of CH0 and CH1 of the joystick. A0 and A1 are connected to X and Y axes respectively. CH0 and CH1 are both outputting 12 bits.



```
    adc_1 u0 (
        .CLOCK (<connected-to-CLOCK>), //
        .RESET (<connected-to-RESET>), //
        .CH0   (<connected-to-CH0>),   // re
        .CH1   (<connected-to-CH1>),   //
        .CH2   (<connected-to-CH2>),   //
        .CH3   (<connected-to-CH3>),   //
        .CH4   (<connected-to-CH4>),   //
        .CH5   (<connected-to-CH5>),   //
        .CH6   (<connected-to-CH6>),   //
        .CH7   (<connected-to-CH7>)    //
    );
```

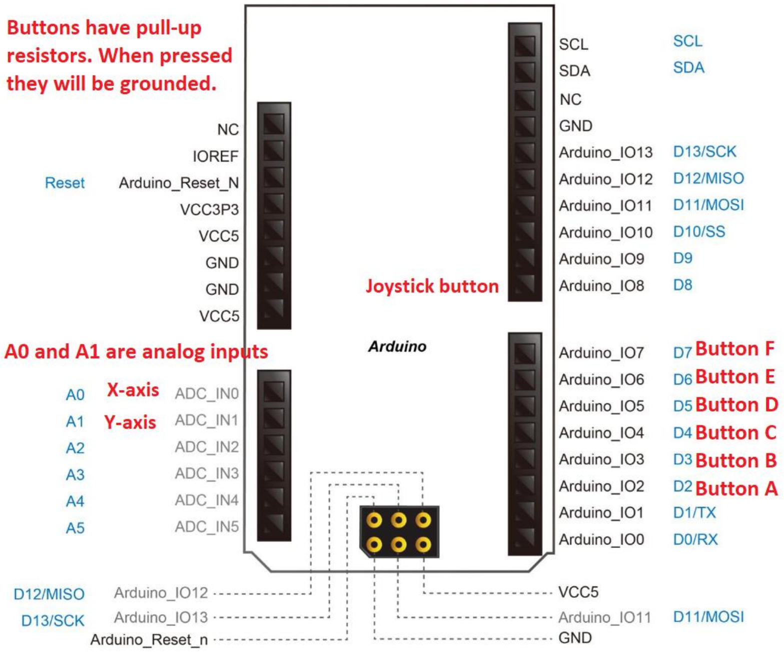


Figure 3-19 lists the all the pin-out signal name of the Arduino Uno connector. The blue font represents the Arduino pin-out definition.

Wire up the ADC IP.

1. In DE10lite_template.v (Or your top level file), instantiate a copy of adc_1 and wire it to ADC_CLK_10 and the respective reset, CH0, and CH1 signals. CLOCK is an input, RESET is an input. CH0 and CH1 are connected to the X and Y axis of the joystick on the board. CH0 and CH1 are 12-bit inputs to our module.
   a. You will need to feed the ADC_CLK_10 into CLOCK.
   b. You will need to make a 12-bit wire called X0 and connect to CH0.
   c. You will need to make a 12-bit wire called Y0 and connect to CH1.
2. Configure the board such that SW[6] selects between the X axis and Y axis. Since the ADC is returning a 12-bit value and we only have 10 LEDs on the board, use only the top 10 values.
   a. In other words, your signal is X0[11:0] coming from CH0. However, since LEDR[9:0] is only 10 bits, ignore the two LSB on X0 and Y0.
3. Record the values (Remembering that you can't see the two LSB bits- just set them to zeros.)
   a. Right movement of joystick maximum value: ________________
   b. Centre (idle) joystick value for X axis: ________________
   c. Left movement of joystick maximum value________________
   d. Centre (idle) joystick value for X axis: ________________
   e. Up movement of joystick maximum value________________
   f. Down movement of joystick maximum value________________
4. Demo to instructor the joystick functionality (indicated using LED and switch 6)
5. Question: What is the step size of each increment assuming 12 bit resolution and 5 V range?

6. Question: Jostling the board slightly will change the values slightly on the LSB side. Pressing the buttons will also cause the value seen on the LEDs to change. Why is this the case? Think in terms of step size and noise.

7. Question: It seems that the ADC can be somewhat noisy. If we were feeding the joystick input into another system (such as controlling a cursor or something), this could prove to be noisy. What ways can you think of to eliminate or filter noise?

8. Question: IP cores are pre-fabricated modules which allow us to access functionality of the board. Convenient. Any disadvantages to using IP cores in our design? Please highlight two disadvantages.

Submission

1. Go to Project > Clean Project.
2. Zip up your project and submit to Canvas.
3. Upload the answers highlighted in magenta to canvas. Please maintain the numbering assigned.