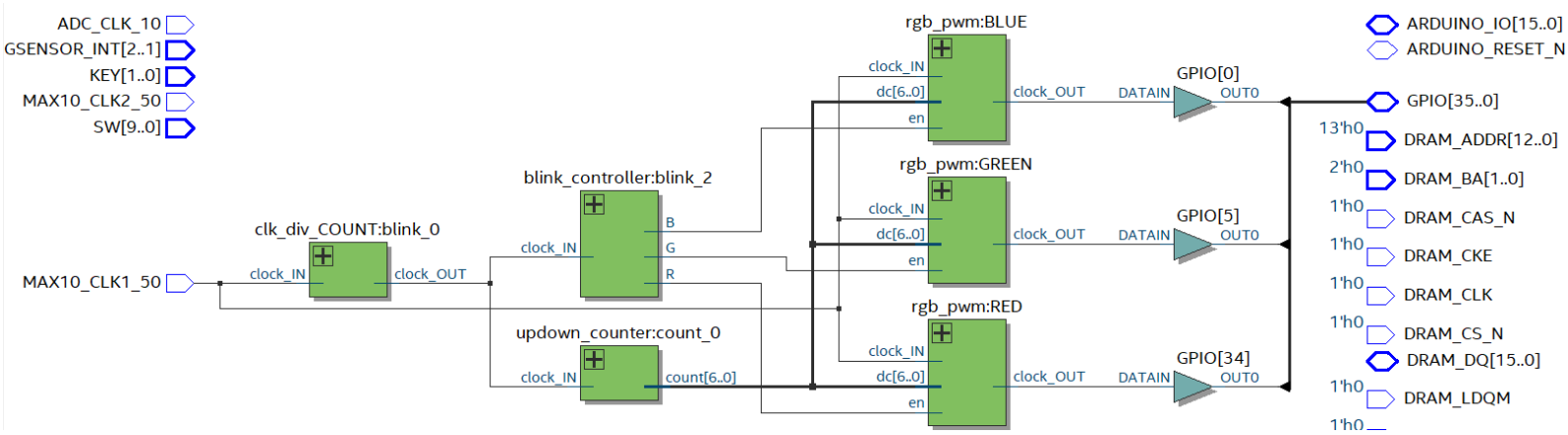
RTL SCHEMATIC



CLOCK DIVIDER AND SWTCHING FREQUENCIES

Counter Clock Divider

50 MHz / 15 Hz = 3,333,332 [ratio]

3,333,332 / 2 = 1,666,666 [50% duty cycle value]

1,666,666 = 0001_1001_0110_1110_0110_1010

= 21 bits for duty cycle register

Switching Frequencies

Modular duty cycle from counter is 7 bits.

0111_1111 = 127

One up-down cycle from 0 to 127 and then from 127 back down to 0 takes 254 clock cycles. After 254 cycles, the next color is enabled and the current color is disabled. After 3 up-down cycles, repeat process starting at original color.

3 * 254 = 762

762 = 0010_1111_1010

= 10 bits for internal controller counter

DESIGN SUMMARY

The RGB LED anode is held high while the color cathodes each receive their own pulse-width modulated clock signal, so long as they are enabled. The clock signals to the color cathodes are held high, disabling a particular color, while each respective PWM module is disabled. Only one PWM module is enabled at a time, allowing for only pure red, blue, or green color on the LED. The modulated duty cycle comes directly from the current value of the up-down counter. Each PWM module has its own internal counter which is compared against the incoming duty cycle value to determine the clock value being sent to each color. With the duty cycle changing incrementally each clock cycle, the amount of power being supplied to the current color is either increased or decreased, causing the "breathing" effect seen on the LED.