

Note: All questions that I require a response for are highlighted in magenta.

1. Please review the datasheet for the DE10-Lite to see how each single digit hexadecimal display is used.

a. What is the page number of the information?

Pgs. 28 – 29 of the DE10-Lite User Manual.

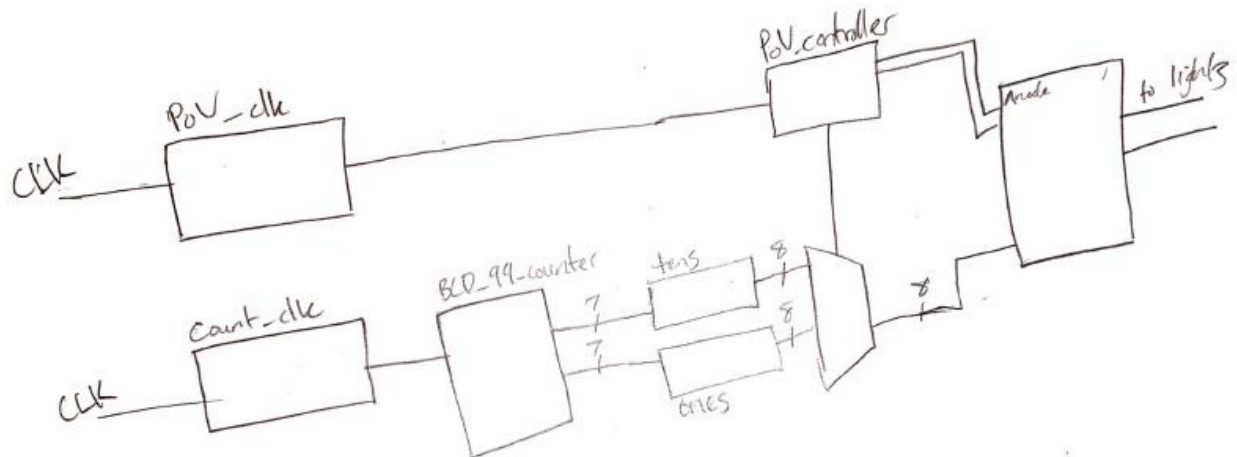
b. Is it configured as common cathode or anode?

Common anode.

c. Is it active high or low?

Each individual segment of a single digit display is active low.

2. Initial block diagram. Given that the end goal is to design a system to automatically count up from 0-99 given a 50 MHz input clock and 2-digit 7-segment display, please draw out the block diagram of modules that you require.



5. Now we need to implement a module that will allow us to show two different values on the 7-segment display at the same time.

b. You'll need a clock divider for this part. Note that your system clock is 48 MHz, 50 MHz, or 100 MHz, so you will most likely need to divide the clock down to the KHz range (Revisit the multiplexing slides for more information, or just ask me.)

i. Please show your math for this.

$$ratio = \frac{50 \text{ MHz}}{500 \text{ Hz}} = \frac{50,000,000 \text{ Hz}}{500 \text{ Hz}} = 100 \text{ KHz}$$

$$count = 0.5 * ratio = 0.5 * 100 \text{ KHz} = 50 \text{ KHz} = 50,000 \text{ Hz}$$

$$bits = floor\left(\frac{\log(50,000)}{\log(2)}\right) + 1 = 16$$

ii. What is your desired output frequency and duty cycle? Why?

500 Hz at 50% duty cycle for equally long periods of each digit being lit, alternating back and forth. Each digit displayed for 0.002 seconds (1/500), repeating faster than the "refresh" period of the eye at 0.016, allowing for persistence of vision.

iii. What is your input clock frequency?

50 MHz from system clock.

iv. What is the ratio, and what is your count up value? Please justify this.

Ratio is 100 KHz, count up value is 50,000.

Desired frequency is 500 Hz. Period is 1/500 Hz = 0.002 seconds.

The output clock signal should toggle after every half a period (50% duty cycle).

$$0.002 / 2 = 0.001 \text{ seconds.}$$

System clock frequency is 50 MHz. Period is 1/50 MHz = 0.00000002 seconds.

Every 0.001 seconds, output clock toggles.

Using system clock period to count to duty cycle period means:

$$.001 / .00000002 = 50,000 \text{ cycles}$$

It will take 50,000 cycles of the system clock before output clock signal toggles.

v. What is the clock period of your input and output clocks?

Input: System clock @ 50 MHz

Output: 2-digit SSEG MUX clock @ 500 Hz

8. If you were to use the 50 MHz clock or the multiplex clock for your counter module above, you would not be able to actually see anything. Please implement a clock divider specifically for the counter module above and write the specifications below.

vi. Please show your math for this.

$$\begin{aligned} ratio &= \frac{50 \text{ MHz}}{50 \text{ Hz}} = \frac{50,000,000 \text{ Hz}}{50 \text{ Hz}} = 1 \text{ MHz} \\ count &= 0.5 * ratio = 0.5 * 1 \text{ MHz} = 500 \text{ KHz} = 500,000 \text{ Hz} \\ bits &= floor\left(\frac{\log(500,000)}{\log(2)}\right) + 1 = 19 \end{aligned}$$

vii. What is your desired output frequency and duty cycle? Why?

50 Hz at a 50% duty cycle to allow for display numbers to count slower than the 60 Hz PoV limit, enough time for the display to show each distinct value, otherwise the digits count too quickly to be seen.

viii. What is your input clock frequency?

50 MHz from system clock.

ix. What is the ratio, and what is your count up value? Please justify this.

Desired frequency is 50 Hz. Period is $1/50 \text{ Hz} = 0.02$ seconds

50% duty cycle means clock signal swaps every half period:

$$0.02 / 2 = 0.01 \text{ seconds}$$

System clock period is 0.00000002 seconds, meaning 0.01 seconds pass after:

$$0.01 / 0.00000002 = 500,000 \text{ cycles}$$

It will take 500,000 system clock cycles before the output clock signal swaps.

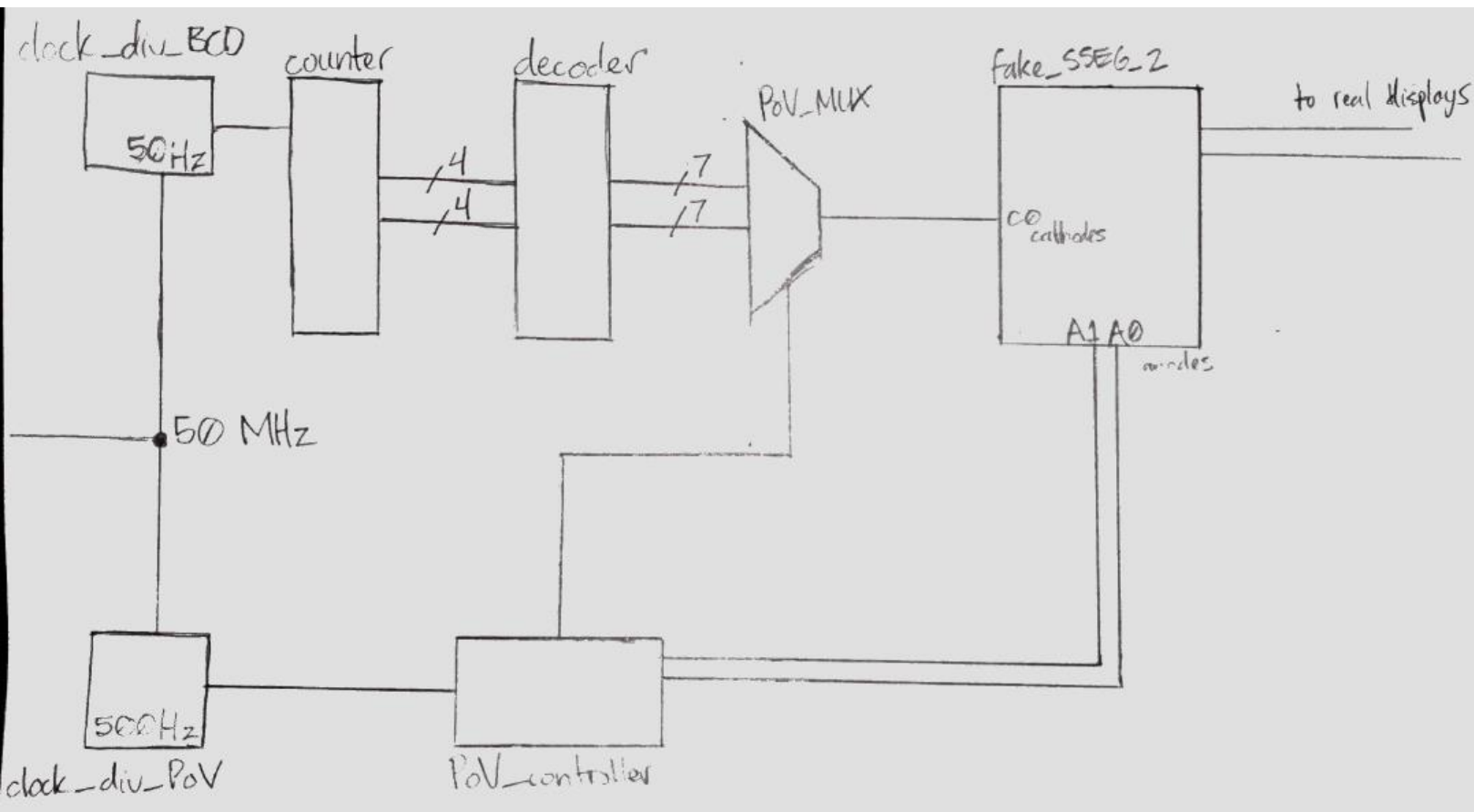
x. What is the clock period of your input and output clocks?

Input: System clock @ 50 MHz

Output: 2-digit BCD Count clock @ 50 Hz

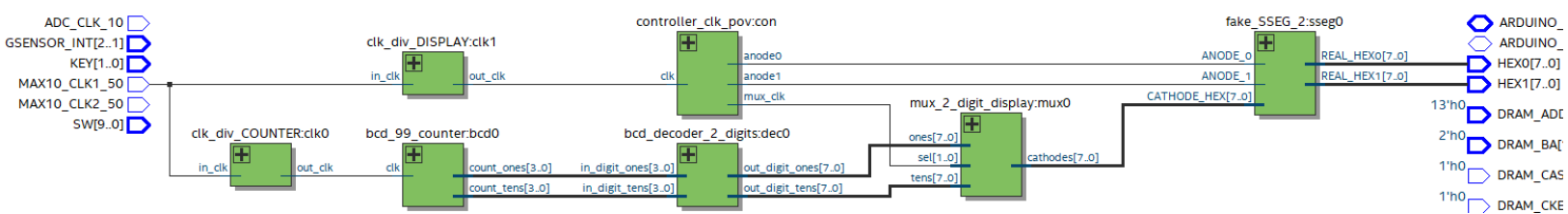
NOTE: In practice, counting clock was too fast for the multiplex clock, and the duty count value was incrementally doubled (halving the divided frequency) and tested until 6.25 Hz was found to work. Above calculations do not reflect the values found in the .v

11. After you are done with the above, please draw out a block diagram of your system by hand or using a computer program.



[signal coming out of multiplexer should have 8-bit data path to match cathodes]

12. Please go to Tools > Netlist Viewer > RTL Viewer. Take a screenshot of the expanded design (Ask me if you are not sure what to take screenshot of).



13. Please ask a colleague for their design and compare your RTL viewer. See any differences in how they implemented their design?

I didn't get to ask colleague, but I did notice some differences in block diagrams when reviewing the lab videos. I saw some examples where the BCD decoding occurred after the multiplexer.

This would just mean make for a design where only a single 1-digit BCD-to-HEX module is required while my design used a 2-digit BCD-to-HEX module made up from two 1-digit modules. Compared to mine, the prior design would be somewhat simpler, more so when it comes to expanding the fake 2-digit SSEG to four digits. [this was written *after* implementing unfortunately]

14. Last part- take my fake_SSEG_2 module. Copy it to a new file and expand it to 4 displays. Show me four displays counting. (Note- Do not change your counter. Just show that the two new displays can duplicate content of old displays

d. What is the new clock frequency you used to multiplex this four display module? Why is this most likely higher than the previous clock frequency?

New clock frequency is double that of the 2-digit clock, halving the count from 50,000 cycles of the system clock to 25,000. The clock being twice as fast as the signal multiplexing the 2-digit display allows it to multiplex double the digits.

e. What is the bare minimum clock frequency to maintain persistence of vision on four displays assuming 60 Hz is the persistence of vision threshold. Please show calculations relative to clock period. (Winter 2021- I sent an email with my calculations with example frequencies).

Minimum frequency should be four times the 60 Hz PoV threshold. $4 * 60 = 240 \text{ Hz}$
 $1 / 240 = 0.0041667 = 4.16 \text{ ms per digit}$. All four digits will be lit up once each within the 16.7 ms PoV period.