

CLOCK DIVIDER CALCULATIONS

Receiving a 9600 baud UART tx signal.

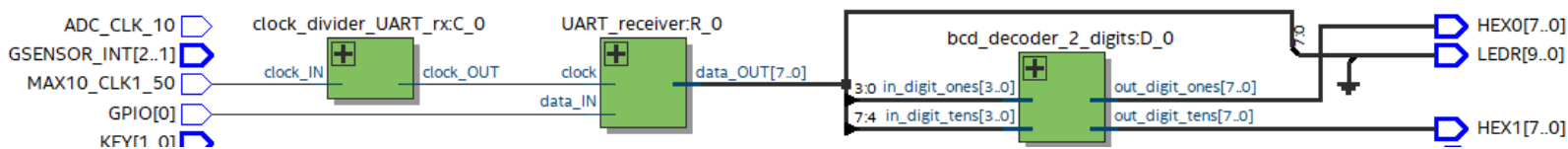
Must oversample at: $8 * 9600 \text{ Hz} = 76,800 \text{ Hz}$

$50 \text{ MHz} / 76,800 \text{ Hz} = 651.0416$ [ratio]

$651.0416 / 2 = 325.5208 \sim 326$ [duty cycle :: 50%]

$326 == 9'b101000110$ [9 bit dc reg]

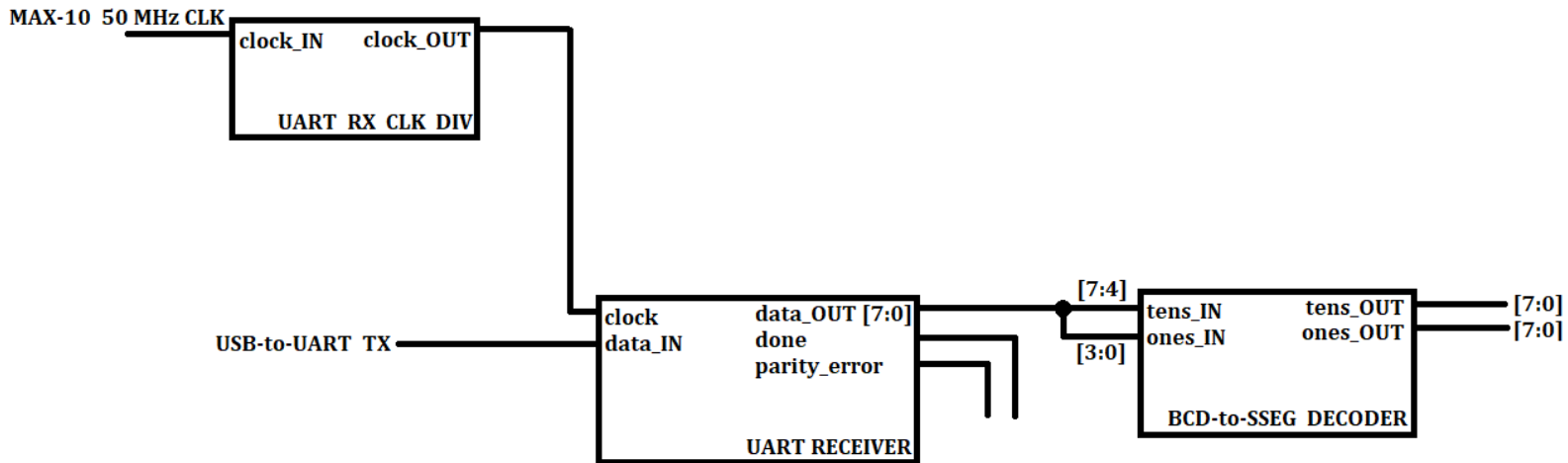
RTL SCHEMATIC



DESIGN FUNCTION

The receiver module has two inputs: a one-bit 9600 baud serial line, and a clock signal (running eight times faster than the serial input) at 76,800 Hz. The clock signal comes from clock divider module while the serial input comes from the TX line of a USB-to-UART converter. When the TX signal drops low, indicating the start bit of a transmission, the “done” output of the receiver is set low and the module begins counting cycles until 12 have passed. Because the divided clock signal coming into the receiver module is eight times faster than the baud rate of the TX signal, counting 12 cycles ensures the value being sampled is in the “middle” of the first bit being transmitted (the LSB, *after* the start bit). From there, the module continues counting off 8 cycles at a time, sampling at the mid-bit position until 9 bits have been read in (8 data bits, 1 parity bit). The 8 data bits are then pushed into an output register; parity is calculated and checked against the received parity bit, with a mismatch setting the parity error flag high. Finally, 12 more cycles are counted off, 8 for the first stop bit, and 4 for the second stop bit (returning the sampled signal to its original offset) and the done signal is set high before returning to idle.

BLOCK DIAGRAM



RECEIVER STATE MACHINE DIAGRAM

