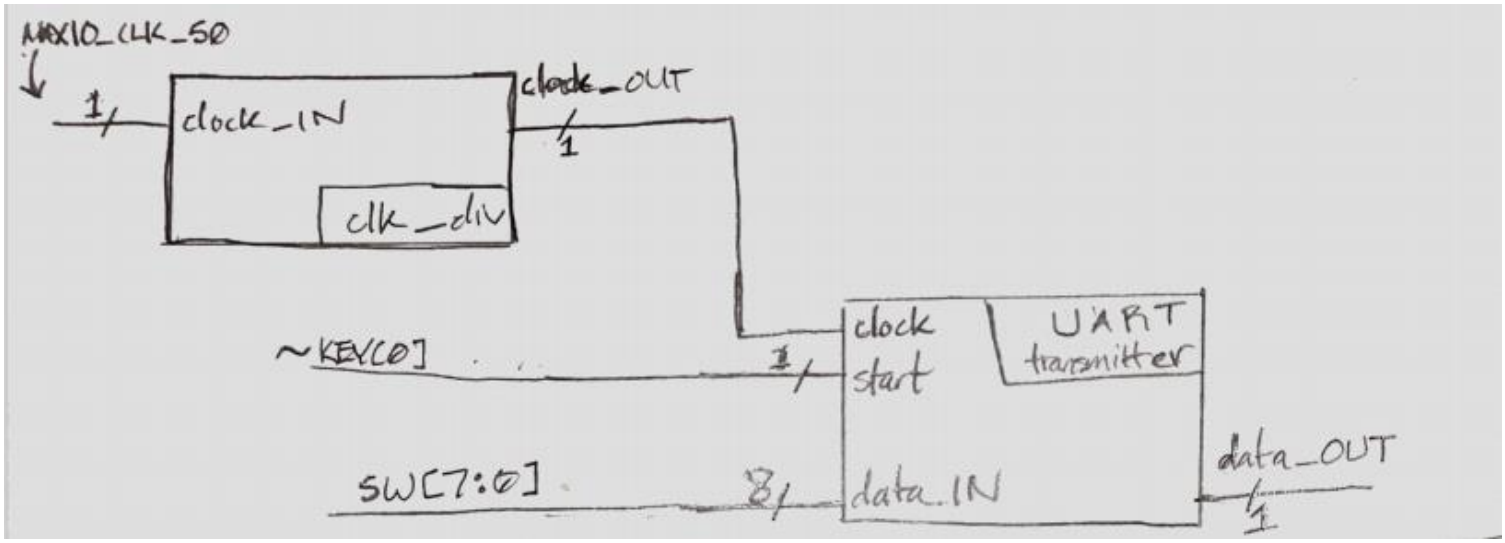
CLOCK DIVIDER CALCULATIONS

9600 Hz baud rate

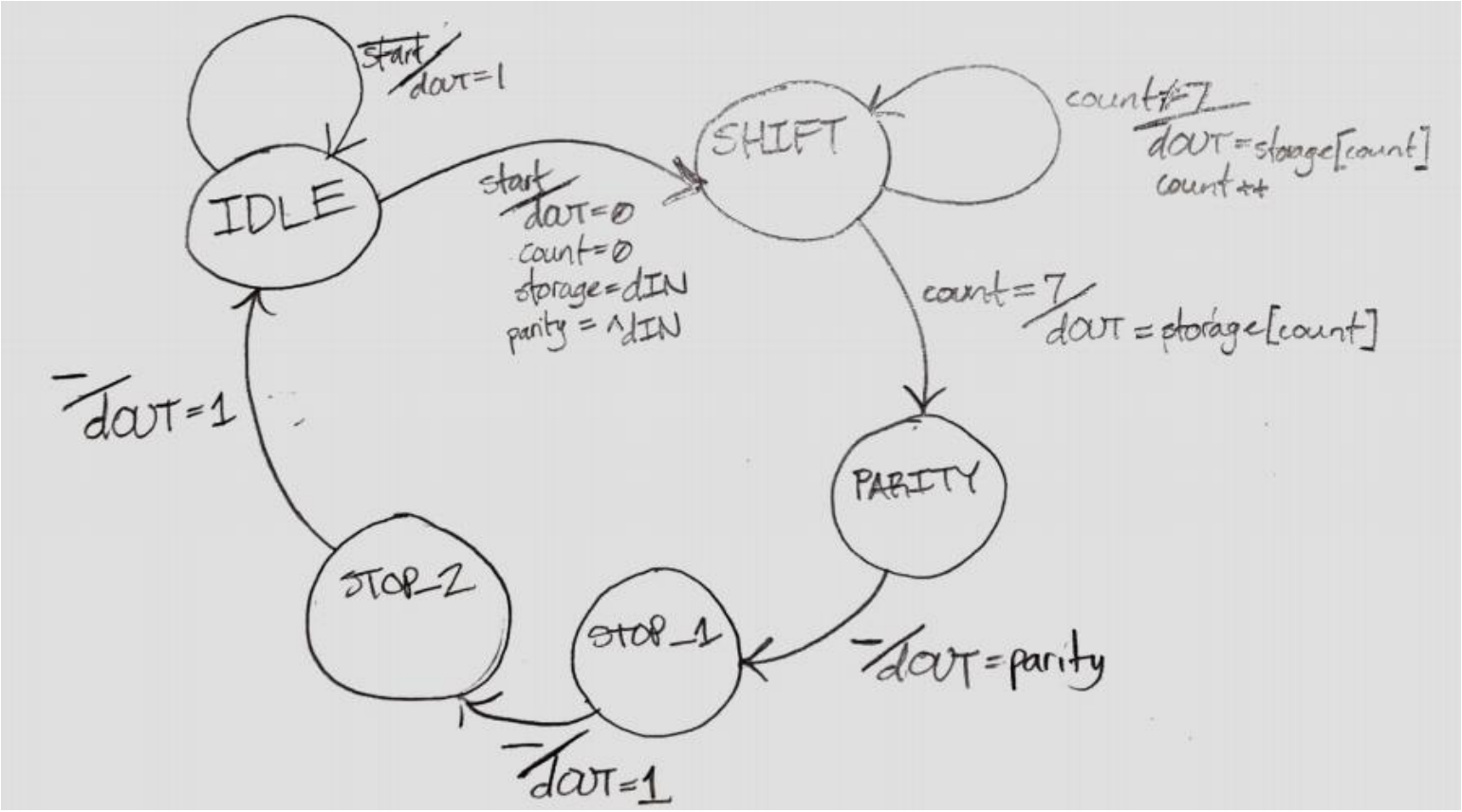
50 MHz / 9600 Hz = 5208 [ratio]
5208 / 2 = 2604 [duty cycle :: 50%]

2604 == 12'b1010 0010 1100 [12 bit dc reg]

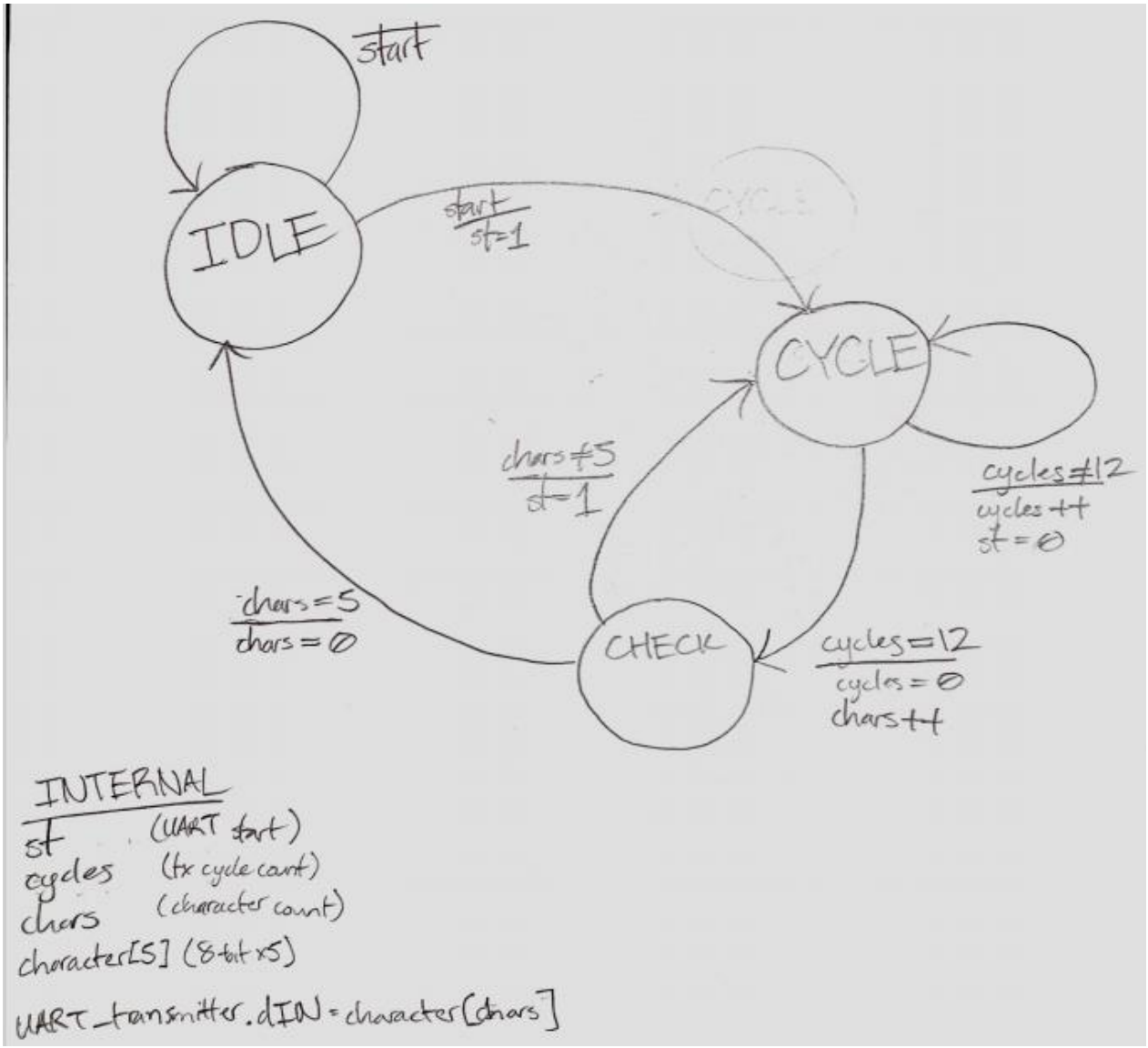
TRANSMITTER BLOCK MODEL



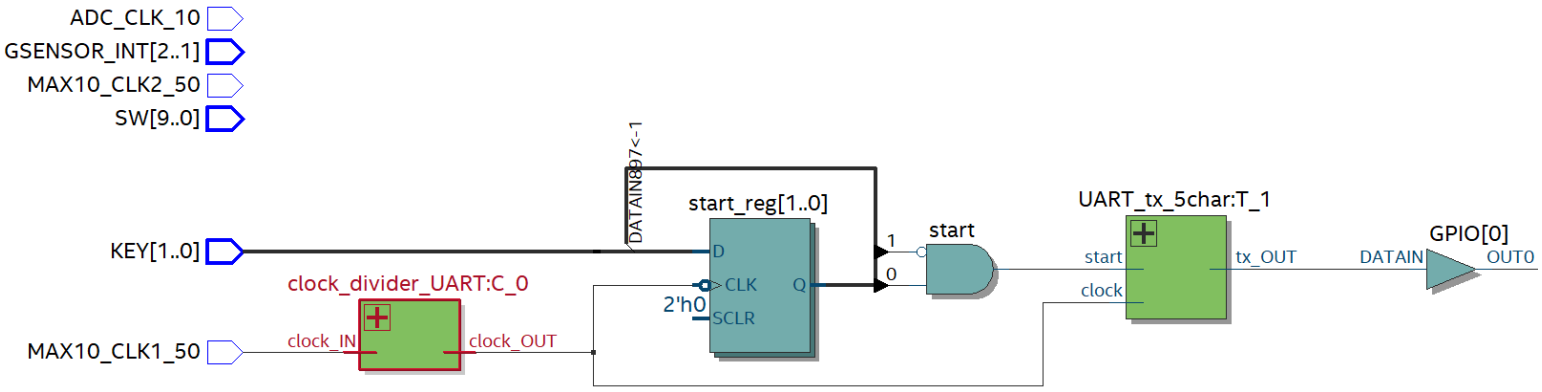
TRANSMITTER STATE MACHINE



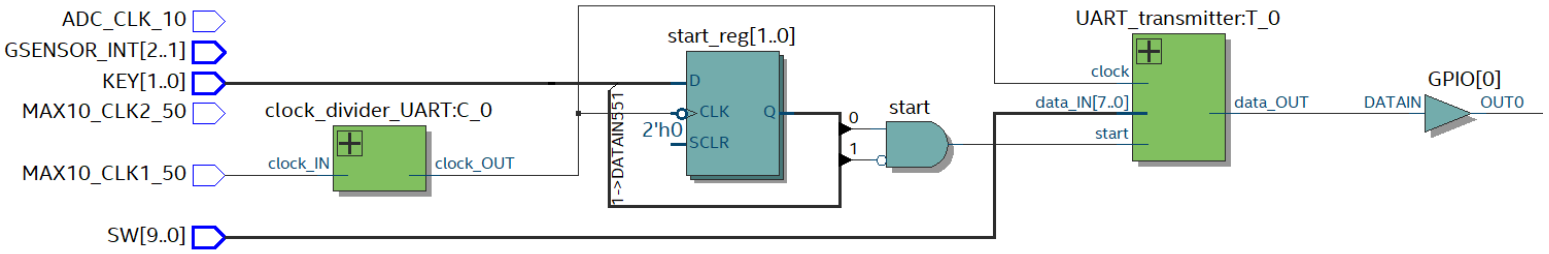
5-CHARACTER TRANSMITTER STATE MACHINE



TRANSMITTER RTL SCHEMATIC



5-CHARACTER TRANSMITTER RTL SCHEMATIC



RESOURCE ALLOCATION (FLOW SUMMARY)

Flow Summary

<<Filter>>

Flow Status	Successful - Tue Feb 16 19:39:37 2021
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	lab5
Top-level Entity Name	DE10_LITE_Golden_Top
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	51 / 49,760 (< 1 %)
Total registers	34
Total pins	185 / 360 (51 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

[*51 logic elements used*]