*CLOCK DIVIDER CALCULATIONS*

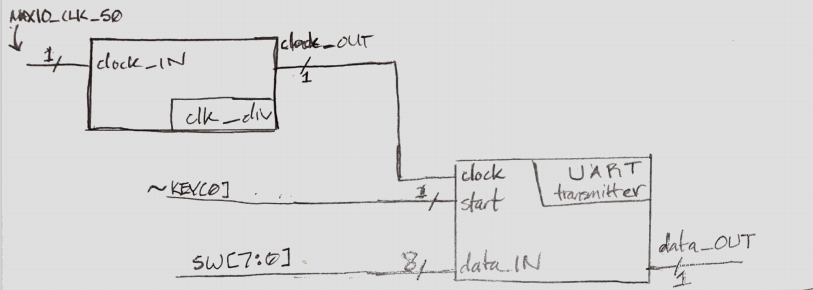
**9600 Hz baud rate**

**50 MHz / 9600 Hz = 5208 [ratio]**

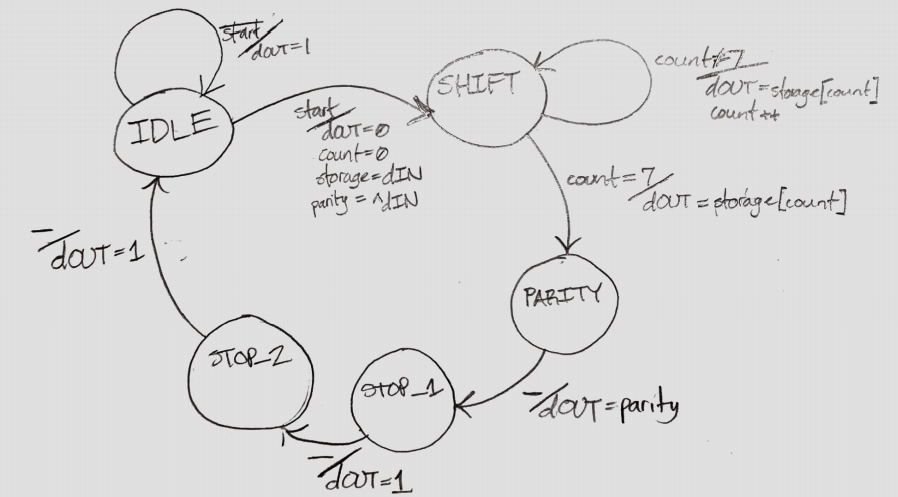
**5208 / 2 = 2604 [duty cycle :: 50%]**

**2604 == 12'b1010 0010 1100 [12 bit dc reg]**

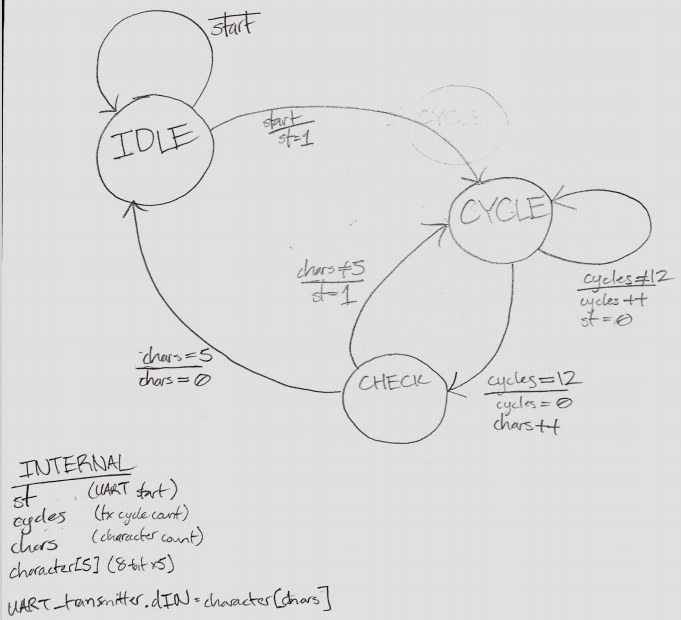
*TRANSMITTER BLOCK MODEL*



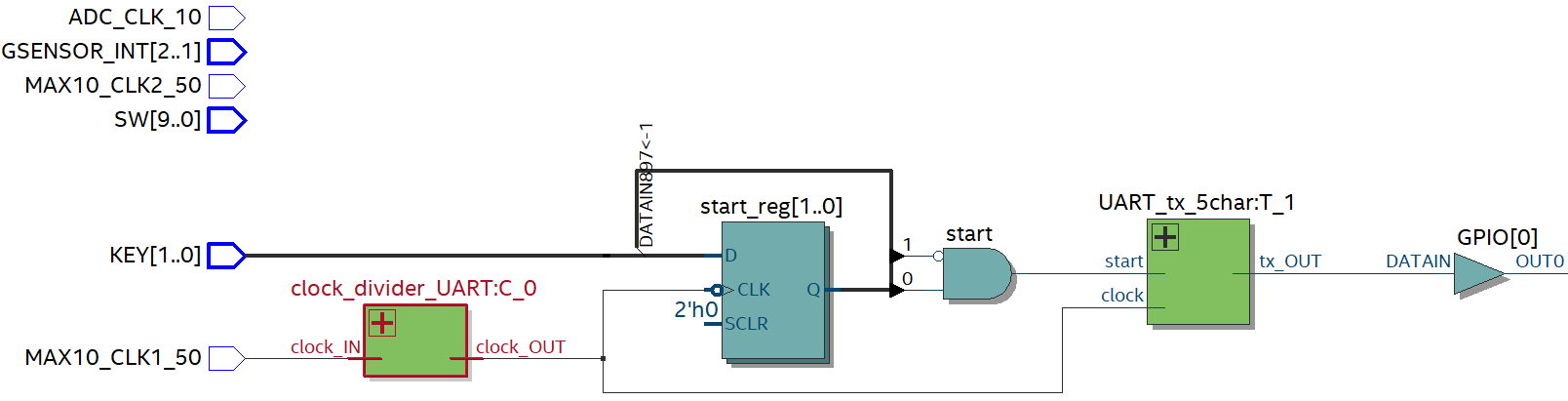
*TRANSMITTER STATE MACHINE*



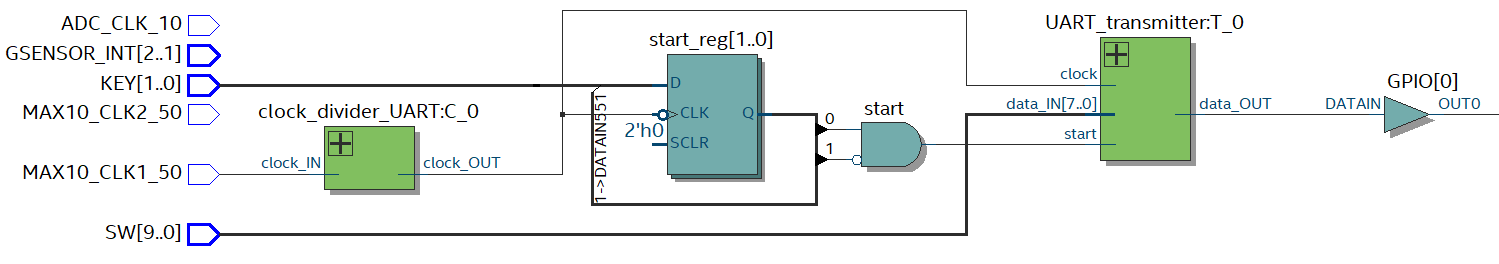
*5-CHARACTER TRANSMITTER STATE MACHINE*

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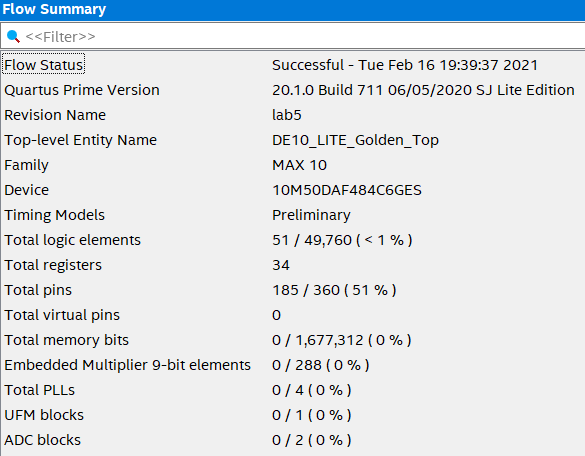
*TRANSMITTER RTL SCHEMATIC*



*5-CHARACTER TRANSMITTER RTL SCHEMATIC*



*RESOURCE ALLOCATION (FLOW SUMMARY)*



**[***51 logic elements used***]**