

Power Stage for Radio-Frequency Body and Local Array Coils for 7-Tesla MRI Systems Using Class-D Amplifier Topology

Master Thesis

Mahmoud Bagheri

10 January 2020

Supervised by: Prof. Dr. Holger Hirsch
Submitted in: University of Duisburg-Essen

In cooperation with: Erwin L. Hahn Institute for Magnetic
Resonance Imaging
Prof. Dr. Harald H. Quick, Dr. Stephan Orzada

Acknowledgement

This work would not have been possible without the support of the *Erwin L. Hahn Institute*. I am especially indebted to *Prof. Dr. Harald H. Quick*, Director of the Erwin L. Hahn Institute, and *Dr. Stephan Orzada*, the first supervisor of this master thesis, who have been supportive of my career goals and who worked actively to provide me with the protected academic time to pursue those goals.

I am grateful to the scientists and staff of Erwin L. Hahn Institute, with whom I have had the pleasure to work during this and other related projects. Each of the members of Erwin L. Hahn Institute has provided me extensive personal and professional guidance and taught me a great deal about both scientific research and life in general.

Nobody has been more important to me in the pursuit of this project than the members of my family. I would like to thank my parents, whose love and guidance are with me in whatever I pursue. They are the ultimate role models.

Abstract

Magnetic resonance imaging (MRI) combines physics, mechanical and electrical engineering as well as informatics and is an active research field to further improve diagnostic imaging. The main aspect of MRI is the ability to measure the effect of magnetic fields on the nuclear spins inside body tissues. One of the most important developments in MRI is the increase of the main magnetic field used to align the nuclear spins. With higher magnetic field strength, the signal to noise ratio can be increased, but at the same time, the resonance frequency of the nuclear spins is increased, leading to the need of high power radiofrequency RF amplifiers which need to have a high peak power, but also the ability to achieve a high duty cycle at low output powers.

In this thesis a power amplifier is designed which is intended to provide the drain current for the output stage of a 1 kW RF amplifier operating at 300 MHz.

Contents

Acknowledgement	i
Abstract	ii
1 Introduction	4
2 MRI Basics	6
2.1 Larmor Equation	6
2.2 Detecting the magnetization of the system	7
2.3 Magnetic Resonance Imaging	7
2.4 Building Block of MRI	7
3 Power Amplifiers	9
3.1 Introduction	9
3.2 Linear Power Amplifiers	10
3.2.1 Class A PA	10
3.2.2 Class B,C and AB PA	11
3.3 Switching Power Amplifiers	12
3.3.1 Class D	12
3.3.2 Class E	13
3.3.3 Class DE	14
3.3.4 Class F	15
3.4 Hybrid Power Amplifiers	16
4 Development of Class D Power Amplifier	18
4.1 Introduction	18
4.2 Important Parameters	19
4.3 GaN MOSFETs vs Ordinary MOSFETs	22
4.4 CDPA Gate Circuit - Input Circuit	23
4.4.1 Gate Driver Inegrated Circuit:	24
4.4.2 Gate Resistance (Turn-OFF):	24
4.4.3 MOSFET Turning On Sequence	26
4.4.4 Calculating Required Drive for the MOSFET:	28
4.4.5 Gate Power Loss:	30
4.4.6 Gate Resistance (Turn-ON):	30
4.4.7 Gate Resistance and Parasitic Oscillations:	31
4.4.8 Dead-Time Calculation:	32

4.5	CDPA Power Section	33
4.5.1	Sequence of Operation:	33
4.5.2	Two Challenges: $\frac{di}{dt}$ and $\frac{dv}{dt}$	35
4.5.3	Body Diode:	36
4.6	Losses in MOSFET	38
4.7	Hard-Switching Topologies and Switching Losses	38
4.8	Ohmic Losses	39
4.9	GaN MOSFET Switching Losses	39
4.9.1	P_{oss} Output Capacitance Losses	42
4.9.2	P_G Gate Charge Losses	43
4.9.3	P_{SD} Reverse Conduction Losses	43
4.9.4	P_{RR} Reverse Recovery Losses	43
4.10	Switching Losses	43
4.10.1	Transistor Switching Behavior:	44
4.11	Output Capacitance C_{OSS} Losses	47
4.12	Gate Charge Q_G Losses:	47
4.13	Reverse Conduction Losses P_{SD} :	48
4.14	Total Hard-Switching Losses	49
4.15	Heat Dissipation:	49
4.16	The Necessity of Line Filter	50
4.17	Type of High Frequency Emitted Components	50
4.18	Line Impedance Stabilization Network (LISN)	51
4.19	Proposed Filter	51
4.20	Design Steps	52
4.20.1	Differential Mode Conducted Emission Filter	52
4.20.2	Common Mode Conducted Emission Filter	53
4.20.3	EMI and EMC Filter	53
4.21	EMI Filter and Stability according to Dr. Middlebrook Criterion	54
4.22	How to select π – Capacitor:	54
4.23	Design Procedure:	54
4.23.1	Use Case 1: Line Filter for CDPA:	55
4.23.2	Use Case 2: Line Filter for Auxiliary Power Supply:	57
4.24	Simulation	59
4.25	Computer Simulation of Power Conversion Systems	60
4.26	Average-Modeling of Converters	60
4.27	Implementation in PSpice	64
4.28	Proposing a Controller	64
4.28.1	Average Current Mode	65
4.28.2	Voltage Mode Control	66
4.29	Layer Stack-up Assignment	71
4.30	Four-layer Stack-up	71
4.31	Six-layer Stack-up	72
4.32	Approach in This Project	72
4.33	Zones in PCB	72
4.33.1	Zone 1:	73

4.33.2 Zone 2:	73
4.33.3 Zone 3:	73
4.34 How many layers do we need?	75
5 Prototyping and Results	76
5.1 Introduction	76
5.2 Construction	76
5.2.1 Next Version Suggestions	78
5.3 EMI/EMC Filter	78
5.3.1 Next Version Suggestions	79
5.4 Oscillator	79
5.4.1 Next Version Suggestions	81
5.5 Power Section	81
5.5.1 Gate Driver	81
5.5.2 MOSFET Half-Bridge Leg	84
5.5.3 Next Version Suggestions:	88
5.6 Control Section	88
5.6.1 Next Version Suggestions:	89
6 Summary and Outlook	91
Bibliography	92

List of Tables

4.1	GaN MOSFET vs Silicon MOSFET	23
-----	--	----

List of Figures

3.1	Class A RF power amplifier	10
3.2	Class B push-pull RF power amplifier	11
3.3	Class D half-bridge power amplifier	13
3.4	Class E half-bridge power amplifier	14
3.5	Class DE power amplifier	15
3.6	Class F RF power amplifier	16
3.7	Classification of hybrid power amplifier	17
4.1	Equivalent circuit of class D power amplifier	20
4.2	Frequency response of the filter	21
4.3	CDPA and synchronous buck converter	22
4.4	Miller Capacitance	24
4.5	Equivalent circuit of the circuit in off-period	25
4.6	MOSFET Turning-On Sequence	27
4.7	Equivalent Circuit of Gate	29
4.8	Timing characteristics vs resistance in gate	31
4.9	High-frequency equivalent circuit of the gate of MOSFET	32
4.10	High-frequency equivalent circuit of the CDPA	33
4.11	CDPA sequences of operation	34
4.12	Spike voltage vs inductance	36
4.13	Spike current vs inductance	37
4.14	Ideal MOSFET Current and Voltage shapes	39
4.15	Real MOSFET Current and Voltage shapes	40
4.16	Ohmic Losses per MOSFET	41
4.17	Ohmic Losses per MOSFET versus Current	41
4.18	Ohmic Losses per MOSFET versus Duty-Cycle	42
4.19	Turn-Off Loss	44
4.20	Turn-On Loss	44
4.21	Impact of drain-source voltage and drain current on gate charge and gate voltage	45
4.22	Impact of drain current on the gate plateau voltage	46
4.23	Device capacitances as a function of drain-to-source voltage	47
4.24	Switch-node voltage commutation with the same load current for various dead-times: (a) partial ZVS, (b) ZVS, and (c) ZVS plus diode conduction	48
4.25	Effective dead-time definition for turn-on	49
4.26	Proposed line filter	51
4.27	DM filter	52

4.28 CM filter with additional zero	52
4.29 CM with DM line filter	53
4.30 Typical line filter	53
4.31 Proposed line filter	55
4.32 Internal; the noise source is in the SMPS and the output signal is at the supply line	59
4.33 External; the noise source is in the power line input, and the output signal is at the input of the power supply	59
4.34 Buck converter	60
4.35 Modeling the switching element in a buck converter	61
4.36 Proposed model for a switching element in a buck converter	61
4.37 Proposed model for switching element in a buck converter, using CCS	61
4.38 Proposed model for inductance and output in buck converter, using VCS	62
4.39 Average-modeling of buck converter, using CCs and VCS	62
4.40 Buck converter	63
4.41 Average-modeling of buck converter, using CCs and VCS	63
4.42 Average-modeling of buck converter, simplified	63
4.43 Implemented Model in LTSPICE	64
4.44 Bode Plot of $\frac{V_{out}}{V_{in}}$	65
4.45 ACM current feedback	66
4.46 Open Loop converter; Bode Diagram	67
4.47 Modeling Open Loop converter; Bode Diagram	68
4.48 Proposed Controller; Bode Diagram	69
4.49 Proposed Controller; Schematic	69
4.50 Proposed Controller; Bode Diagram	70
4.51 Closed Loop System; AC Analysis	70
4.52 Total overview of circuit	73
4.53 Different Zones on Circuit	74
4.54 Proposed Layer Configuration	75
 5.1 PCB of the project	77
5.2 PCB after assembly	77
5.3 Probe of Oscilloscope used for measurement the signals in 100 MHz bandwidth	78
5.4 Bode Plot - Main EMI/EMC filter - Forward Path	79
5.5 Bode Plot - Main EMI/EMC filter - Forward Path	80
5.6 Bode Plot - Auxiliary EMI/EMC filter - Forward Path	80
5.7 Bode Plot - Auxiliary EMI/EMC filter - Forward Path	81
5.8 Oscillator & Triangular wave generator, simulated in LTSpice	82
5.9 Oscillator & Triangular wave generator, Waveform by LTSpice	82
5.10 Oscillator - square wave generator, Waveform by Oscilloscope	83
5.11 Oscillator - triangular wave generator, Waveform by Oscilloscope	83
5.12 Lower MOSFET - Gate Pulse	84
5.13 Upper MOSFET - Gate Pulse	85
5.14 Gate of MOSFET - Threshold and Gate Plateau Voltage	85

List of Figures

5.15	Gate of MOSFET - Threshold and Gate Plateau Voltage	86
5.16	Output Point of Half-Bridge Leg without Snubber	87
5.17	Output Point of Half-Bridge Leg without Snubber	87
5.18	Output Point of Half-Bridge Leg with Snubber	88
5.19	Output Signal and Input Sinusoidal Reference- Load less than 20 Watt-Upper: Input, Lower: Output	89
5.20	Output Signal and Input Triangular Reference- Load less than 20 Watt-Upper: Input, Lower: Output	90
5.21	Output Signal and Input Pulse Reference- Load less than 20 Watt-Upper: Input, Lower: Output	90

List of Symbols

<i>AC</i>	Alternative Current
<i>ACM</i>	Average Current Mode
<i>AM</i>	Amplitude Modulation
<i>BGA</i>	Ball Grid Array
<i>CAPA</i>	Class-A Power Amplifier
<i>CBPA</i>	Class-B Power Amplifier
<i>CCM</i>	Continuous Conduction Mode
<i>CCPA</i>	Class-C Power Amplifier
<i>CCS</i>	Current-Controlled Source
<i>CDPA</i>	Class-D Power Amplifier
<i>CEST</i>	Chemical Exchange Saturation Transfer
<i>CM</i>	Current Mode
<i>CT</i>	Computed Tomography
<i>DC</i>	Direct Current
<i>DCM</i>	Discontinuous Conduction Mode
<i>DUT</i>	Device Under Test
<i>EMC</i>	Electromagnetic Compatibility
<i>EMI</i>	Electromagnetic Interference
<i>ESR</i>	Equivalent Series Resistance
<i>ESL</i>	Equivalent Series Inductance
<i>EUT</i>	Equipment Under Test
<i>GaN</i>	Gallium Nitride
<i>GND</i>	Ground
<i>HEMT</i>	High-Electron-Mobility Transistor
<i>IC</i>	Integrated Circuit
<i>IGBT</i>	Insulated Gate BT
<i>LDMOS</i>	Laterally-Diffused Metal Oxide Semiconductor
<i>LISN</i>	Line Impedance Stabilization Network
<i>LPA</i>	Linear Power Amplifier
<i>MOSFET</i>	Metal Oxide Semiconductor Field Effect Transistor
<i>MRI</i>	Magnetic Resonance Imaging
<i>PA</i>	Power Amplifier
<i>PCB</i>	Printed Circuit Board
<i>PCM</i>	Pulse Code Modulation, Peak Current Mode
<i>PSRR</i>	Power Supply Rejection Ratio
<i>RF</i>	Radiofrequency
<i>RMS</i>	Root Mean Square
<i>Si</i>	Silicon
<i>SIM</i>	Switched Inductor Model
<i>SMA</i>	SubMiniature version A
<i>SMPS</i>	Switched Mode Power Supply
<i>SAR</i>	Specific Absorption Rate
<i>SNR</i>	Signal to Noise Ratio

List of Symbols - Continue

<i>SMD</i>	Surface-Mounted Device
<i>SOA</i>	Safe Operating Area
<i>T</i>	Tesla
<i>VCS</i>	Vurrent-Controlled Source
<i>VM</i>	Voltage Mode
<i>ZCS</i>	Zero Current Switching
<i>ZVS</i>	Zero Voltage Switching

1 Introduction

Magnetic resonance imaging (MRI) is one of the most versatile imaging technologies in clinical use. It provides superb soft tissue contrast and does not need ionizing radiation like computed tomography (CT). Although 1.5 Tesla (T) and 3T MRI systems are most commonly used in the clinic environment, 7T MRI has recently been approved for clinical usage and MRI systems with even higher field strengths up to 11.7T are used for scientific experiments. The reason for increasing the main magnetic field strength is the gain in signal to noise ratio.

According to the Larmor equation, increasing the static magnetic field strength in an MRI experiment increases the frequency of precession of the spins and, therefore , the frequency of the radio-frequency (RF) wave needed to excite the spins. Since higher frequency also means shorter wavelength, severe wave effects can affect the transmit field at high field strengths. To cope with this problem, ultra high-field systems ($\geq 7\text{ T}$) use multichannel transmit systems with 8 and more channels for their transmit arrays (mostly referred to as “coils” in MRI), while standard clinical systems only have a single transmit channel.

Transmit pulses in MRI can vary strongly in their demands in duty cycle and peak amplitude, while the time averaged root mean square (RMS) output power is limited by the maximum allowed specific absorption rate (SAR) for and minute averages.

Commercial MRI systems usually have more than 30 kW peak output power for their body coils, and local array coils at 7 T are driven with $1-2\text{ kW}$ peak per channel [1],[2],[3],[4].

Modern MRI imaging and spectroscopy sequences can contain a multitude of different transmit pulses with very different demands on amplitude and duty cycle.

Spin echo sequences in abdominal imaging demand high peak power for short pulses around 1 ms and the duty cycle is limited by the SAR limits, leading to small duty cycles, while standard gradient echo imaging sequences may have lower peak power demands but higher duty cycles up to 20%. Power demands can increase through the use of adiabatic pulses, which can have a length in the order of 10 ms with high power demands [5], [6].

Parallel transmission with selective excitation [7], [8] can produce long pulses, even longer than 10 ms , with strongly varying amplitude within these pulses [9], [10].

On the other hand, chemical exchange saturation transfer (CEST) imaging [11] for example demands very long low power pulses, resulting in very high duty cycles nearing 100%. All in all, this shows the need for versatile transmit amplifiers that can run high duty cycles and have high peak output power, but do not need to have high average output power.

Furthermore the bandwidth of the transmit pulses can be as high as 1 MHz . The transmit system at the Erwin L. Hahn Institute for MRI is comprised of 32 transmit channels. The power stages are LDMOS class AB amplifiers in push-pull topology with a peak output of 1 kW . These amplifiers have a low efficiency especially at low output powers and are therefore limited in duty cycle. To cope with this problem, while retaining the bandwidth, the drain voltage of the LDMOS stage is to be modulated according to the envelope of the input signal of the RF amplifier.

For such a configuration of a power amplifier, there are several recommended designs; 1-Linear PA, 2-Switch-Mode PA, and 3-Hybrid PA. Linear PAs benefit from high linearity, but on the other hand they suffer from the low efficiency, especially at low and medium power loads. Switch-Mode PAs have two major advantages over linear PAs. Firstly, they have a much higher efficiency than other topologies and in full-load can reach to more than efficiency. Secondly, the power per cubic meter of such a converter is much higher than for other amplifier topologies. Moreover, controlling is simpler. Nevertheless, the relation between input and output voltage is not as linear as it is for linear PA. The last design is the best one in terms of power and linearity, however it suffers from the complexity and difficulty of the control of such converter.

In this thesis, the switch-mode PA has been selected as the PA and in order to increase the linearity of the relation between the input and output, a high switching frequency has been selected. In order to reduce the losses, which originate from the high switching frequency, the GaN family of MOSFET transistors has been selected. Due to their fast switching speed, this family of MOSFET has less switching losses which play an important role in high frequency application. Moreover, the DC losses are tremendously lower in comparison with silicon counterparts [12].

In the following chapter, a short introduction into MR physics is presented, the later chapters describe the design of the amplifier from scratch and illustrate the test results.

2 MRI Basics

Since the first MRI images were acquired by Paul Lauterbur for which he later received the Nobel prize, MRI has undergone significant developments making it one of the most versatile imaging methods in modern medicine. The availability of MRI is now synonymous with quality of medical care, even within the rural hospital settings, and 1.5 Tesla scanner has become a workhorse of the modern radiological exam. With the exception of computed tomography CT, no other radiological modality can compete with MRI, not only in terms of the breadth of exams currently possible, but also in the future promise of the technique [13].

MRI is a powerful imaging modality, which is used vastly because of its flexibility and sensitivity to a broad range of tissue properties. Moreover, its relative safety (noninvasive nature of the magnetic field, no ionizing radiation) permits repeated examination without adverse effects.

In MRI, there is an assortment of magnetic fields, which exploit the resonance phenomenon. The strong and static main magnetic field aligns the spins, the gradient fields change the magnetic field as a function of position in 3D space, and the radio frequency fields are used to excite the spins of nuclei so that the signal they produce by their precession is measurable from the outside. The most commonly used nuclei is that of hydrogen [14].

2.1 Larmor Equation

The interaction of the proton's spin, with the magnetic field produces torque, causing it to precess about \vec{B}_0 as the fixed axis. In MRI context, $\vec{\mu}$, is the *Magnetic Dipole Moment Vector*, whose direction is non other than the spin axis itself. Similar to a compass needle, the magnetic moment vector will tend to align itself along any external static magnetic field \vec{B}_0 . Instead of falling along the field direction, the *magnetic moment vector* will precess around the field direction. The speed of this precession can be expressed by the *Larmor Equation*:

$$\omega_0 = \gamma * B_0$$

ω_0 is the precession frequency, which is referred to the *larmor frequency*. γ is the *gyromagnetic ratio*, which is different for different nuclei. For the hydrogen proton, $\gamma = 42.6 \frac{MHz}{T}$. This equation is the building block of MRI physics [14].

2.2 Detecting the magnetization of the system

As long as the spins are aligned with the main magnetic field, their magnetization does not produce a measurable RF signal, but they do, if their magnetization is tipped away from the direction of the main magnetic field. The magnetization of the spins can be rotated away from its alignment along the \vec{B}_0 axis (i.e. from its *longitudinal* direction), by applying a radio frequency magnetic field (an RF pulse) orthogonal to the magnetization vector. The RF pulse is transmitted by a nearby *transmit coil*. The resulting transverse magnetization vector has the magnitude M_0 and begins to precess clockwise in the x-y plane (\vec{B}_0 in z direction) [14].

2.3 Magnetic Resonance Imaging

The goal of imaging is to correlate a series of signal measurements with the spatial locations of the various signal sources. All protons are represented by just one chemical species, such as water. The addition of a spatially varying magnetic field across the sample produces a signal with spatially varying frequency components, according to the *Larmor equation*:

$$\omega(x) = \gamma * B(x)$$

This is done by introducing an additional coil (*a linear gradient coil*) that changes the original field \vec{B}_0 linearly in a single direction. Mapping back and forth between the signal space and the image position space can be done with the *fourier transform*. With more *gradient coils*, data reconstruction by inverse Fourier transformation can be carried out in more spatial dimensions. The application of a finite bandwidth RF excitation centered at the *Larmor frequency* of the combined static field plus a gradient field, leads to the excitation of a layer, or slice, of spins orthogonal to that gradient with a defined slice thickness.

2.4 Building Block of MRI

There are three main families of coils in MRI:

1. Main Magnet Coil
2. Gradient Coils
3. RF Coils

The main magnet coil is responsible for generating the high intensity magnetic field in the range of several Tesla (e.g. 1.5, 3.0 or 7 T), in order to align the spins of the elements in the body. The main magnet coil consists of windings of a superconducting wire, like *niobium-titanium* or *niobium-tin*. These windings are placed in liquid helium, in order to

keep the temperature of the windings about $4\text{ }^{\circ}\text{K}$. Such superconducting magnets work like a permanent magnet, due to the zero resistance of the superconducting materials [15],[16].

Gradient coils are responsible for generating the gradient field. This gradient field slightly distorts the main magnetic field in a predictable pattern, causing the resonance frequency of protons to vary as a function of position. The primary function of gradients, therefore, is to allow spatial encoding of the MR signal. Three sets of gradient coils are used in nearly all MR systems: the x-, y-, and z- gradients. Each gradient coil set is driven by an independent power amplifier and creates a gradient field, whose z-component varies linearly along the x-, y-, and z-directions, respectively [15],[16].

The RF coil is the component of the MRI system, which is responsible for stimulation and reception of the MRI signal. The design of this coil is important not only due to the quality and precision of the resulting image, but also in terms of the safety issues which originate from applying high power radiofrequency pulses to the human body. New designs of RF coils take advantage of multi-channel transceivers, which lead to better precision [17].

The different coil groups are placed in a layered structure within an MRI system. The outer layer is formed by the superconducting main magnet coil, along with shimming coils for magnetic field homogenization. The next layer is formed by the gradient coil sets for spatial encoding of the signals in three spatial dimensions. The third and innermost layer is formed by the RF coil. The Gradient coils and the RF transmit coil are located within the magnet bore, a tunnel with about 60 cm inner diameter, where the patient is placed during an MRI examination.

3 Power Amplifiers

3.1 Introduction

In the world of apparatuses, there is an ever growing need for increasing the power and frequency. By these two important factors, some aspects of the apparatus, such as size and precision, can be improved which tends to enhance the functionality and performance of the device. Due to this fact, a converter which generates enough power and works especially at higher frequencies is always desirable. At the beginning of electronics industry, linear power amplifiers were dominant. However, they suffer from lower efficiency and generate harmonics. Later, other amplifiers were developed, which take advantages of resonance and notwithstanding the linear essence, the efficiency of some of them has reached to 78.5% as the modified topology used by Doherty [18].

Reducing distortion and increasing efficiency of amplifiers are important factors, which are pursued to be improved in every version of the amplifier. Although some linear amplifiers can reach high efficiencies, it is difficult to keep the distortion of such types of amplifiers low. As rule of thumb, there is a trade-off between these two factors, distortions and efficiency. That means, to mitigate one factor would aggravate another factor and vice versa, and in an application where the bandwidth is not restricted, the usage of a linear power amplifier influences the operation of the circuit.

Switching amplifiers started with the usage in audio circuits and then extended to other areas. They were first proposed by *Alec H. Reeves* in 1950s pulse code modulation (PCM), and then the technology was quickly applied to other areas where it was found useful [19].

Notwithstanding many developments and inventions in the area of amplifiers, resonance and switching are the main factors in every amplifier which increase the efficiency and reduce the size of the amplifiers [20].

In this chapter, firstly, linear power amplifiers are briefly introduced, then switching power amplifiers, as a new generation of amplifiers are discussed. Lastly, hybrid amplifiers are introduced, which are the most technological and up-to-date design for spread-spectrum power amplifiers, and can be found on the power stage of most instrumental amplifiers.

3.2 Linear Power Amplifiers

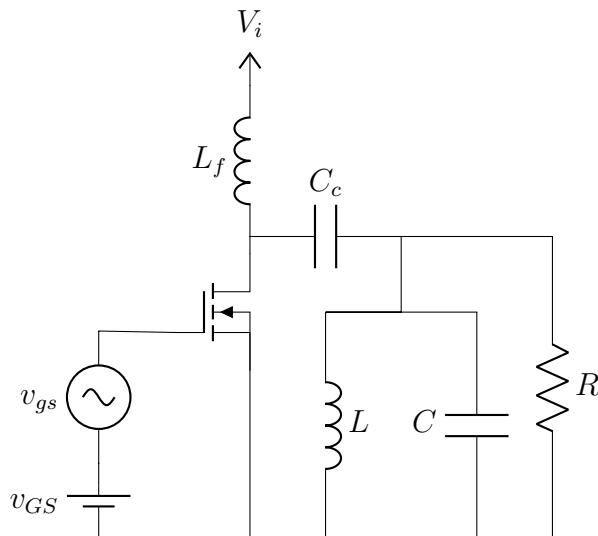
Linear power amplifiers *LPA* were the first amplifier topology that was used by electronics engineers in order to increase some aspects of the signal; voltage, current or both. The general topology of such amplifiers is divided into four sub categories:

1. *Class A*
2. *Class B*
3. *Class C*
4. *Class AB*

These will be discussed in the following.

3.2.1 Class A PA

The Class A power amplifier *CAPA* is the best amplifier in terms of linearity. It makes a replica from the input voltage or current at its output and there is high-similarity between input and output. The transistor in this stage which is always a single transistor works in 360° . The efficiency of this type of amplifier can maximally reach to 25% and it is commonly used for pre-amplification stages. Since the transistor operates in large-signal mode, the non-linearity essence of the transistor would insert some additional harmonics to the output, such as *square law for MOSFET drain current* which inserts the second harmonic of the input into the spectrum of the output [21],[20].



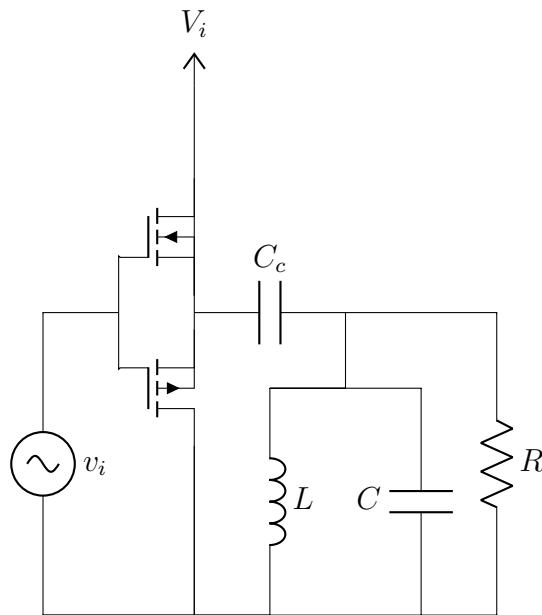
Figures 3.1: Class A RF power amplifier

Current and voltage of the drain of the transistor oscillate around a bias point and in an ideal transistor there will be theoretically no distortion on the voltage and current of the output voltage and current. The bias point is created by the bias circuit. In most of the cases this bias voltage causes high losses, whenever the difference between the output voltage and the voltage imposed on the drain of the MOSFET is high. Then the losses are very high especially on high current loads. Linear amplifiers are divided theoretically into 4 or sometimes 3 subcategories, but it would be better to be categorized into 2 sub-categories: 1-full-wave conducted amplifiers 2-half-semi wave conducted amplifiers [20].

3.2.2 Class B,C and AB PA

Class B,C and AB PA have in common, that they only conduct some degrees of the input voltage. By this technique, the induced losses will be decreased. Class B amplifiers consist of a single switch for half-wave conduction and two switches for full-wave conduction. The second topology of the class-B PA is always known as *push-pull* power amplifier. The efficiency theoretically can be up to 78.5% [21].

Some parallel-resonant circuit to the switch is sometimes mandatory. The efficiency of the Class B power amplifier is higher than that of the Class A power amplifier. The circuit of the Class C power amplifier is the same as that of the Class B amplifier. However, the operating point is such that the conduction angle of the drain current is less than 180° which is 180° by class B. The conduction angle of the drain current in the Class AB power amplifier is between 180° and 360°. Just like in the Class A amplifier, this leads to losses, even when no input signal is applied [20].



Figures 3.2: Class B push-pull RF power amplifier

3.3 Switching Power Amplifiers

The idea of switching power amplifiers comes from switching power supplies. In the 1950's, the first idea of this amplification came to commercial environment by invention of the PCM modulation in audio systems. Later, the usage of those amplifiers has been increased from audio signal till RF signals. The main idea of these converters is considering the signal as a fixed value (*sample and hold mechanism*) in a small piece of time(*PWM frequency*), and then convert this value to a width of pulse instead of conduction of the transistor. Most of the time, the transistor will stay on (low resistance) or off (high resistance). This reduces the losses in the transistor, leading to reduction of to an increase of the efficiency of the amplifier in comparison to its linear counterpart [19].

Early switching power amplifiers were mainly based on well-known buck converters, but later, many more types of the switching amplifiers have been invented. Besides the mentioned advantages, this type of amplifier suffers from some disadvantages. The control mechanisms of this amplifiers are somehow difficult to design and implement due to the non-linear essence of these topologies. Moreover, many advanced designs amplifiers take advantage of resonance, which make them harder to control in a large bandwidth [22].

The classification of the switching amplifier is not simple. Since all different switching topologies can be mixed together and make a new topology. However, the basic group of the amplifier, as following to the documentation and books in this area, are:

1. Class D
2. Class E
3. Class DE
4. Class F

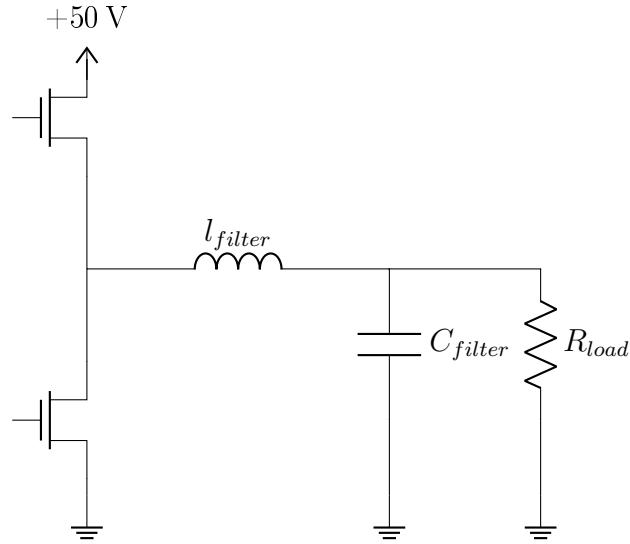
It should be noted, that in an RF environment, all topologies of amplifiers are designed in resonance mode, which reduces the losses and increases the life of transistors. However, in audio bandwidth or less than 1 *MHz* input frequency, it is possible to design a switching power amplifier, using the hard-switching scheme which stands against the resonance-mode scheme.

3.3.1 Class D

The invention of this type of the amplifier in hard-switching scheme belongs to the PCM environment and audio signals and was invented by *Reeves*, moreover, the usage of soft-switching scheme and resonance was invented by *Baxandall* in an oscillator. Similar to switching DC-DC converter, two fundamental aspect of operations are also imaginable for this DC-AC converter [22],[19] :

1. Class D voltage-switching (or voltage-source) amplifiers
2. Class D current-switching (or current-source) amplifiers

in the next chapter, most of the features of this type of the amplifier will be explained and a design based on this type of amplifier will be fulfilled. The basic topology of this converter is almost half-bridge which can be seen in *Figure 3.3*, however, due to the necessity of more output power, the full-bridge topology is also recommended.



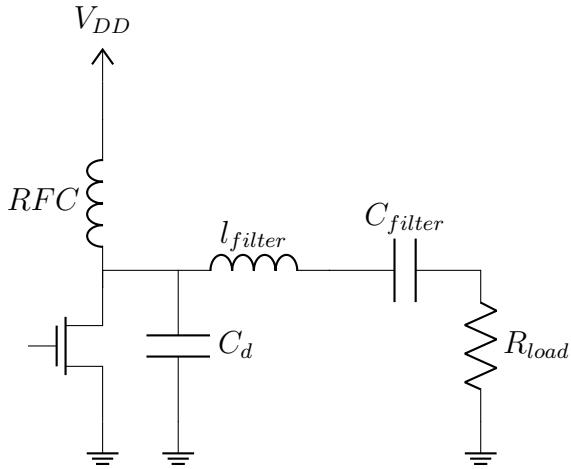
Figures 3.3: Class D half-bridge power amplifier

3.3.2 Class E

Class E power amplifiers are single switch amplifiers which are used in resonant mode. There are two variances of this amplifier:

1. Class E zero voltage switching (ZVS)
2. Class E zero current switching (ZCS)

The transistor in such an amplifier works as a switch. So far, class E ZVS power amplifier is the most efficient amplifier known. The first scheme of this amplifier was introduced by Ewing [23]



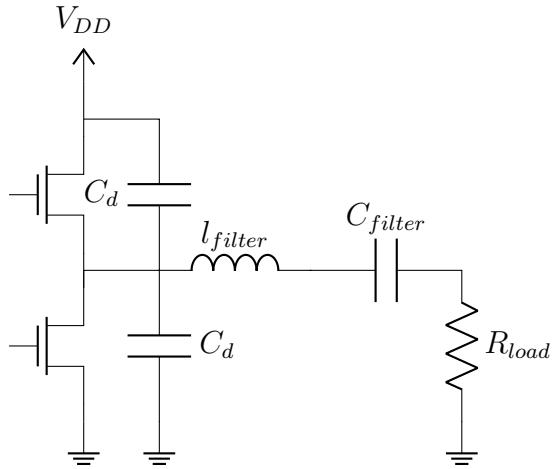
Figures 3.4: Class E half-bridge power amplifier

There is a difference in operation between class E in ZVS and ZCS mode, however the mechanism of operation is similar. By substituting voltage and current, and using the duality theorem, it can be understood. The gate of the transistor is turned on for very short periods, repeated with the main operating frequency. The RFC provides the fixed current to charge the C_d . The voltage on the drain of the MOSFET will normally be several times higher than V_{DD} . However, by selecting the proper circuit elements, it is pursued to limit the voltage at about $3 * V_{DD}$.

The filter circuit which is resonant at the main operating frequency will make the output sinusoidal. The output voltage will be several times as high as the input voltage, based on the quality factor of the circuit. The main clue for this type of amplifier is tuning the value in such a way that the drain of the MOSFET in all of cases works in semi sinusoidal manner. By this configuration, the efficiency of the amplifier can reach about 100%.

3.3.3 Class DE

The class DE power amplifier is also denoted as class D_{ZVS} RF power amplifier. It consists of two switches, one series-resonant circuit, and two shunt capacitors, which are connected in parallel with the switches. The advantage of this amplifier is the combination of the low voltage stress of class D amplifier and zero voltage switching scheme of class E amplifier. Theoretically, switching loss in class DE amplifier is zero, yielding high efficiency. The most important point of operation of such amplifiers is dead-time, when both of the switches on the leg of the converter are off. Dead time can be long in contrast to the normal dead-time in an half-bridge converter, due to prevention of short circuits in the leg of the switches. The main topology of this amplifier can be seen in *Figure 3.5* [20].



Figures 3.5: Class DE power amplifier

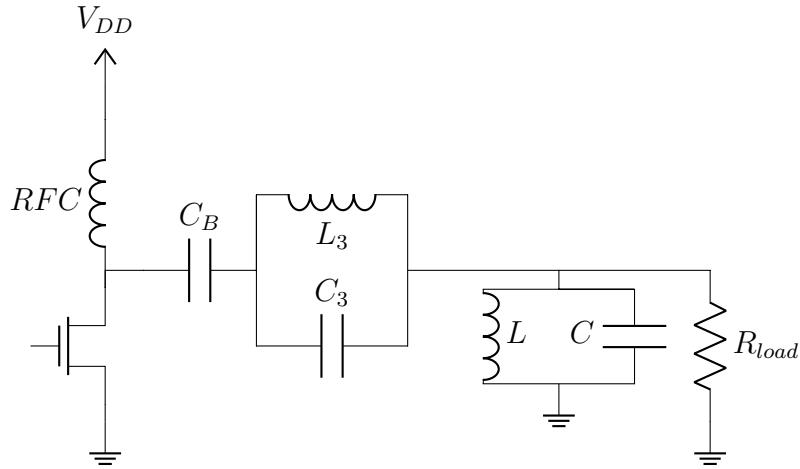
3.3.4 Class F

Class F RF power amplifiers, are rather complicated amplifiers, and they utilize multiple-harmonic resonators in the output network to shape the drain-source voltage, in order to reduce loss in the switch and to increase the efficiency. This amplifier is sometimes called polyharmonic or multi-resonant power amplifier. The drain current flows when V_{ds} is flat and low, and reciprocally, the V_{ds} is high when the drain current is zero. This results in low losses for the transistor. Class F power amplifiers, with resonant circuits, tuned to the third harmonic or to the third and fifth harmonics have been widely used in high-power amplitude-modulation (AM) broadcast radio transmitters in low, medium, and high frequency bands.

There are two groups of Class F RF power amplifiers:

1. Odd harmonic Class F power amplifiers.
2. Even harmonic Class F power amplifiers.

In Class F amplifiers with odd harmonics, the drain-to-source voltage contains only odd harmonics and the drain current contains only even harmonics. Therefore, the input impedance of the load network represents an open circuit at odd harmonics and a short circuit at even harmonics. The drain-to-source voltage v_{DS} of Class F amplifiers with odd harmonics is symmetrical for the lower and upper halves of the cycle. The basic topology of this converter, can be seen in *Figure 3.6*.



Figures 3.6: Class F RF power amplifier

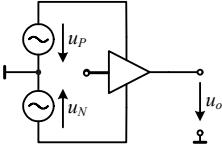
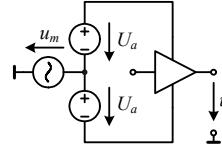
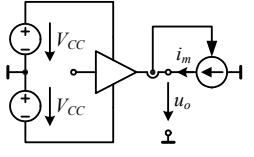
3.4 Hybrid Power Amplifiers

Hybrid power amplifiers are a new generation of amplifiers, which can be operated in a large bandwidth and work from no-load till full-load condition with the highest quality of output voltage and current, in terms of pursuing the input reference. This type of power supply, inherited from the AM power amplifiers, consists of two parts, one for the main carrier frequency, and one for the smaller bandwidth in base-band, which has the smaller power ability. In this type of amplifier, on one side, the big advantage is linearity and efficiency, however, on other side, there is a big disadvantage; complexity and difficulty of control mechanisms. However, in most industrial amplifiers, which are designed to work in a large bandwidth, the first choice is this type of the amplifier [24].

Most of these amplifiers use a network of amplifiers, which are connected in a variety of structures. Normally, one linear power amplifier *LPA* is used in order to shape the output power for the output voltage voltage and a network of switching elements is used to inject the current, and respectively provide the output power for the output voltage. There is not exactly one classification for this type of amplifiers, however, we can simply put them in 3 different categories [24]:

1. Envelope configuration
2. Series configuration
3. Parallel configuration

The idea behind this type of amplifier is reducing the voltage drop across the linear power amplifier section by supplying the power to the output stage in relation to the envelope of the signal to be amplified [24].

Type I	Type II	Type III
Envelope Configuration	Series Configuration	Parallel Configuration
		
Reduce voltage drops across LPA power transistors	Reduce voltage drops across LPA power transistors	Reduce output current of LPA power transistors

Figures 3.7: Classification of hybrid power amplifier

4 Development of Class D Power Amplifier

4.1 Introduction

Class-D power amplifiers, abbreviated as **CDPA**, are easy to implement power amplifiers, which have been used for decades in the area of audio-signal power amplifiers. High power per volume, acceptable linearity and high efficiency make it the first choice for many designs. In addition to previously mentioned advantages, the inductive nature of the speaker as the load of such amplifiers makes them the first essential selection for audio power amplifiers. Only when the main focus is on linearity, they are outperformed by analog linear amplifiers.

In this chapter, the main goal is to design a class-D power amplifier, which can be fit into the power section of an existing MRI amplifier unit. Firstly, in this chapter, the important parameters of a class-D power amplifiers are listed, then GaN technology MOSFET is compared to ordinary Si MOSFETs. Then, the gate driver of a GaN MOSFET is studied in addition to the losses which burden the MOSFET under turning-on and turning-off conditions. Thereafter, the power section of a class-D power amplifier and the mechanism of operation are discussed, and moreover the challenges of the half-bridge topology. As a final step in this chapter, the losses of the amplifier static- and dynamic- are calculated.

For heat dissipation, according to the losses of the converter in full-load, a heat-sink is designed. Due to the medical devices requirement, the usage of a line filter at the input of the amplifier is an obligation when there is a source for high-frequency signals. Two different line filters are proposed in order to diminish the noises from outside to inside and vice-versa. Though the current-mode converter is the most stable one, however, the implementation of such converter for a spread spectrum amplifier is quite complicated and beyond the scope of this master thesis. Therefore, voltage-mode techniques are used for this converter as mechanism of control. An average-modeling scheme is used to simulate the converter in long-time operation in comparison to cycle-by-cycle model, which is used for calculating the exact response of a converter. Finally, the layer's stack-up for this amplifier is studied and a six-layer stack-up is proposed.

4.2 Important Parameters

In designing the CDPA, there are some important input parameters, which should firstly be determined. Furthermore, there are also some criteria, which should always be considered.

1. **Bandwidth of V_{in} :** In this special use case, the frequency is between 0 Hz and 500 kHz . Though in the analog environment there is no fixed power gain for such a range, however, in this design, it is tried to reduce the dependence of the gain on the input frequency. Since the highest frequency of the input voltage is 500 kHz , the switching frequency should be minimum twice of that. In this design, 5 MHz is selected as the PWM frequency.

$$BW = [DC \text{ } 500 \text{ } kHz]$$

$$f_{PWM} = 5 \text{ } MHz$$

2. **Output Power P_{out} :** Represents the maximum power of the PA. This power is active power and does not contain any reactive elements.

$$P_{out} = 1 \text{ } kW$$

3. **Maximum Output Voltage V_{out} :** The maximum output voltage is the required voltage for the second stage of the MRI RF amplifier.

$$V_{out} = 50 \text{ } V$$

4. **Equivalent Load Resistance R_{load} :** The minimum amount of the resistance - maximum load- which can be placed at the output of the power amplifier the MRI HF amplifier.

$$R_{load} = \frac{(V_{max})^2}{P_{out}} = \frac{(50 \text{ } V)^2}{1 \text{ } kW} = 2.5 \Omega$$

5. **Quality Factor of Output Filter (Q)** Since the filter has two poles(L and C), there is the quality factor for the filter. As a rule of thumb, it will be selected to 0,707. The reason for this number is to avoid the working-conditions of filter called *overdamped* or *underdamped*, which respectively leads to *losses in high frequency* or *overshoots*.

$$Q = 0.707$$

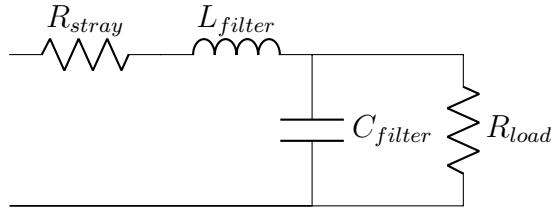
6. **Inductance and Capacitance of Filter ($L\&C$):** According to the R_{load} and PWM frequency of the operation, by the rule of the thumb, the inductance and the capacitance of the filter can be calculated easily. However, due to the behaviour of filter near the cut-off frequency, the cut-off frequency is selected a little higher than

the required cut-off frequency. (required cut-off frequency is 500 kHz , the calculated cut-off is 1 MHz) [25]

$$L = \frac{R_{load}}{Q * \omega_0} = 563 \text{ nH}$$

$$C = \frac{Q}{R_{load} * \omega_0} = 45 \text{ nF}$$

7. **Equivalent circuit:** The Equivalent circuit of the output stage of the CDPA can be shown in *Figure 4.1*.



Figures 4.1: Equivalent circuit of class D power amplifier

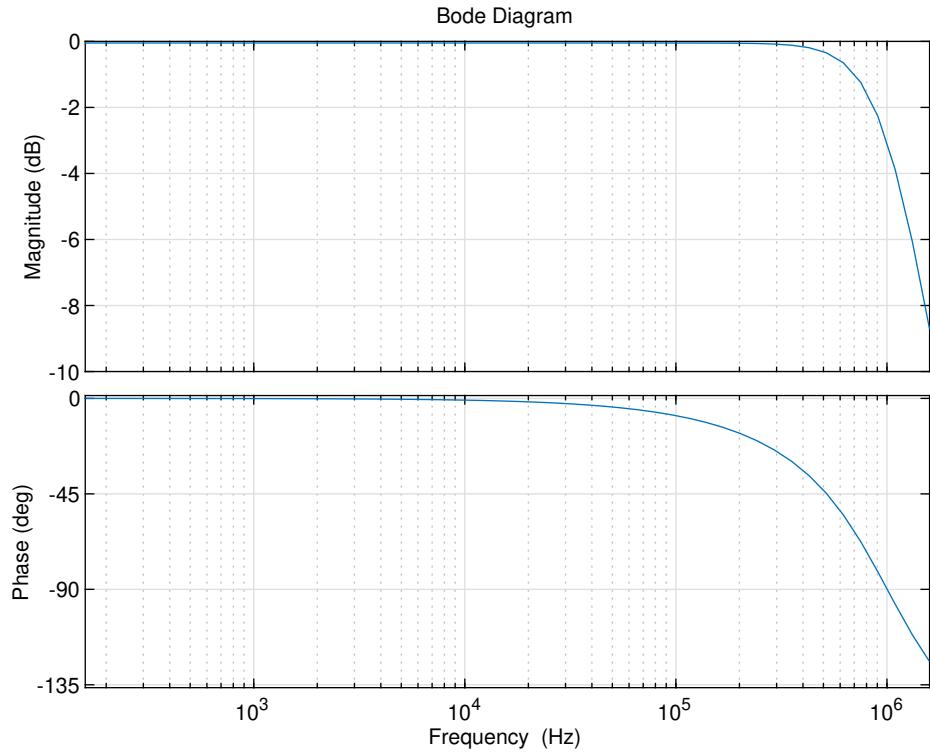
In this figure, R_{stray} represents the R_{on} of the MOSFETs, plus the PCB track resistances. The value of this resistance depends on the topology of the CDPA as well as the PCB. It should be noted, that there are small stray inductances due to the track of the PCB, which participate mainly in the ringing and oscillation of voltages at the drains of the MOSFETs. Since we want to use the half-bridge topology and GaN MOSFETs, so we would have:

$$2 * R_{on} = 14 \text{ m}\Omega$$

Without loss of generality, the amount of stray resistances can be neglected (a track with 300 mil width and 1oz thickness, the resistance will be $1 \frac{\text{m}\Omega}{\text{inch}}$), since this amount will normally be less than the 10% of the $2 * R_{on}$.

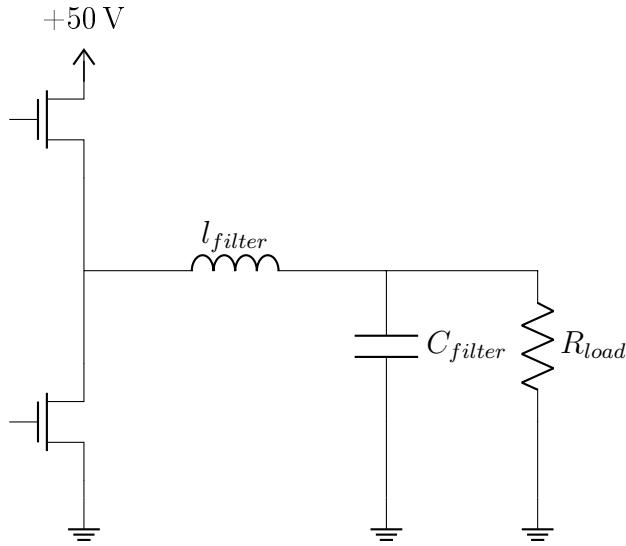
8. **Frequency Response of the Filter:** Using the calculated values of the R_{stray} , R_{load} , C_{filter} and L_{filter} , the frequency response of the filter can be calculated and the bode plot of the transfer function is shown on *Figure 4.2*. In the bode plot, it can be noted, that the filter operates well in terms of amplitude in frequencies less than 500 kHz . There is a change in the phase shift of the output voltage in comparison to the input, however, by selecting the cut-off frequency, very near to the PWM frequency, it would be alleviated. Moreover, the filter should mitigate all components of PWM switching frequency, which are far beyond the cut-off frequency.

$$\frac{V_{out}}{V_{in}} = \frac{4,5 * 10^{-8}s + 0,4}{1,14 * 10^{-21}s^3 + 2,03 * 10^{-14}s^2 + 1,356 * 10^{-7}s + 0,4022}$$



Figures 4.2: Frequency response of the filter

9. **Gain in CDPA:** With Linear amplifiers the gain is constant irrespective of bus voltage variations, with CDPA, however, the gain is proportional to the bus voltage. This means that the power supply rejection ratio (PSRR) of a CDPA is 0dB, whereas the PSRR of a linear amplifier is very good. It is common in CDPA to use feedback to compensate for the bus voltage variations.
10. **Energy Flow:** In linear amplifiers the energy flow is always from supply to the load, and in Full bridge CDPA this is also true. A half-bridge CDPA however is different, as the energy flow can be bi-directional, which leads to the “***Bus pumping***” phenomenon, which causes the bus capacitors to be charged up by the energy flow from the load back to the supply. This occurs mainly at the low audio frequencies i.e. below 100 Hz.
11. **Analogy to a Synchronous Buck Converter:** A simple analogy can be made between a CDPA and a synchronous buck converter. Topologies are essentially the same as can be seen below in *Figure 4.3*.



Figures 4.3: CDPA and synchronous buck converter

The main difference between the two circuits is, that the reference signal for the synchronous buck converter is a slow changing signal, from the feedback circuit(a fixed voltage). However, in the case of CDPA, the reference signal is an audio input signal which is a continuously changing signal. This means that the duty cycle is relatively fixed in the synchronous buck converter, whereas the duty is continuously changing in the CDPA with an average duty of 50%. In the synchronous buck converter the load current direction is always towards the load, but in CDPA the current flows in both directions. The final difference is in the way the MOSFETs are optimized. The synchronous buck converter is optimized differently for the high and low side MOSFETs, with lower $R_{DS(on)}$ for longer duty and low Q_g for short duty. The Class D amplifier has the same optimization for both of the MOSFETs, with the same $R_{DS(on)}$ for high and low side.

12. **Half-Bridge or Full-Bridge CDPA:** The most important beneficial part of full-bridge CDPA is using the 3 levels of PWM instead of 2 levels of PWM, which is used in half-bridge. The pumping-effect is the characteristic of the half-bridge CDPA. Obviously, the number of the components in the half-bridge CDPA is less than its full-bridge counterpart.

4.3 GaN MOSFETs vs Ordinary MOSFETs

GaN MOSFETs are the edge-of-technology MOSFETs, which are used extensively in switching converters, where there is a demand on using a higher switching frequency. The structure of this MOSFET, allows the designer to increase the frequency much compared to common Si MOSFET and take benefit of this higher switching frequency. Nonetheless, this increment of the frequency would be simply influenced by the parasitic elements of the circuit. In other words, the placement of the circuit components at this high frequency and

the connection of the signal tracks and also power tracks should be precisely considered. In order to demonstrate the differences, *Table 4.1* shows specifications of a GaN MOSFET and an ordinary MOSFET has been shown.

Table 4.1: GaN MOSFET vs Silicon MOSFET

Characteristic	GaN MOSFET	Si MOSFET
<i>Manufacturer</i>	GaN Systems	IRF-Infineon
<i>Part Number</i>	GS61008T	BSB056N10NN3
I_D	90 A ($7 \text{ m}\Omega$)	83 A ($5.6 \text{ m}\Omega$)
$I_{D,pulse}$	170 A (100 us)	332 A
$P_{tot,diss}$	225 W	78 W
T_i	-55 to 150	-40 to 150
Q_{oss}	21.4 nC	73 nC
$Q_{g.typ}$	12 nC	56 nC
C_{iss}	590 pF	4100 pF
C_{oss}	280 pF	750 pF
C_{rss}	12.4 pF	27 pF
$t_{d(on)}$		15 ns
t_r		9 ns
$t_{d(off)}$		25 ns
t_f		8 ns

In addition, GaN MOSFETs have zero Q_{RR} , which make them the best choice for the *Half-Bridge Hard Switching* converters.

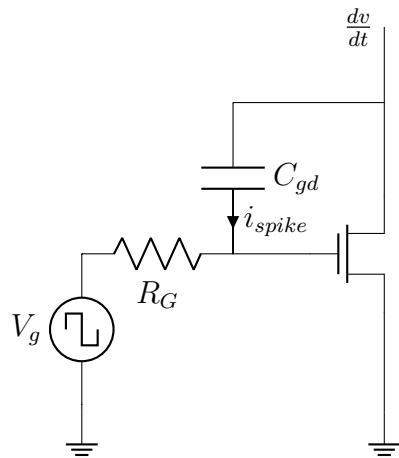
4.4 CDPA Gate Circuit - Input Circuit

As the GaN MOSFET **GS61008T** has been selected for the CDPA, due to the need of the high-frequency operating, some considerations should be noted in the design of gate-driving stage:

1. Parasitic elements due to PCB tracks
2. Turn-on resistance
3. Turn-off resistance
4. Minimum current of the driver IC

In GaN MOSFETs, C_{iss} and $V_{G(th)}$ are lower in comparison to their counterparts. This means, that beside the ability for switching in very high frequencies, thanks to lower C_{iss} and $V_{G(th)}$, there is also a vulnerability to unexpected spikes on gates, which originate from the high $\frac{di}{dt}$ or $\frac{dv}{dt}$ and come from the drain of the MOSFET to the gate through C_{gd} , which

is known as *Miller Capacitance* and can be seen in *Figure 4.4*. In all topologies for gate driving, the gate resistance is a fundamental part, which should be considered. However due to the Miller capacitance, two different resistances in turn-on and turn-off cycles should be used, to mitigate spikes on the gate, and to prevent turning on the MOSFET in off periods. In off periods, the gate pin is equivalently connected to ground through the R_G . This means that the gate voltage is zero, however, normally when one transistor is off, another transistor should be turned-on, which changes the voltage on the drain of MOSFET. This $\frac{dv}{dt}$ over the drain of the off-transistor, creates a small amount of current and will be going to ground through the R_G , and if this R_G is big enough, produces a voltage variation on the gate, which can turn on the off-MOSFET. This scenario leads to destruction of the MOSFETs due to short-circuiting. In this case, two scenarios should be considered: 1- *Damage to the gate of the MOSFET by feeding excessive voltages* and 2-*Unexpected turning-on of MOSFET, which leads to cross conduction*



Figures 4.4: Miller Capacitance

4.4.1 Gate Driver Integrated Circuit:

Since the MOSFET from *GaN systems* has been selected, the recommended gate driver for the frequency near to 10 MHz is *pe29102* from *pSemi*. The small size of the ball grid array (BGA) package makes it an ideal choice for higher frequencies operation.

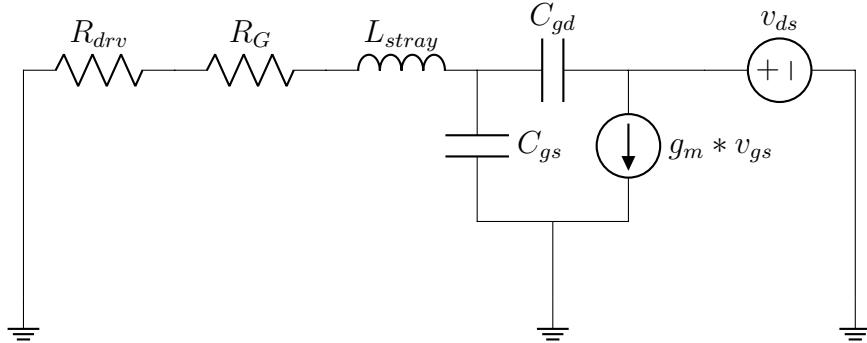
4.4.2 Gate Resistance (Turn-OFF):

By considering the equivalent circuit of the MOSFET during the off period on one switch, which can be seen in *Figure 4.5*, the spike current of the gate and consequently, the voltage on the gate during the off period can be calculated.

$$C_{gd} = C_{rss} = 12.4 \text{ pF}$$

$$C_{gs} = C_{iss} - C_{rss} = 577.6 \text{ pF}$$

$$C_{ds} = C_{oss} - C_{rss} = 267.6 \text{ pF}$$



Figures 4.5: Equivalent circuit of the circuit in off-period

According to the datasheet of the PE29102 the R_{drv} for on-period and off-period is different as below:

$$R_{drv,On} = 1.9 \Omega$$

$$R_{drv,Off} = 1.3 \Omega$$

In the equivalent circuit, the L_{stray} stands for all the parasitic inductances of the signal path between output of the driver and the gate of the MOSFET. This inductance plays an important role on the fringing on the gate of the MOSFET, and can make the driver unstable. However, thanks to the BGA package of the MOSFET and the driver, these inductances are lower than for through-hole or also surface-mounted device (SMD) counterparts, but the tracks on PCB should be minimal in length and wide enough to carry the necessary current.

In this project, V_{DD} is selected as 75 V, the supply voltage for the gate driver is 6 V and the negative voltage for the driver is selected to be 0 V. Thus, the variance on the drain of every MOSFET, due to the 5 MHz operating frequency can reach a maximum of:

$$\frac{dv}{dt}_{max} = \frac{V_{DD}}{t_{rise}} = \frac{75 \text{ V}}{2 \text{ ns}}$$

in this case (off period of the MOSFET), the current which is injected by this change of voltage on the drain of the MOSFET:

$$i_{gate} = C_{gd} * \frac{dv}{dt}_{max}$$

$$i_{gate} = 12.4 \text{ pF} * \frac{75 \text{ V}}{2 \text{ ns}} = 465 \text{ mA}$$

This amount of current changes the voltage on R_G and R_{drv} , influencing the gate.

$$v_{gate} = 465 \text{ mA} * (R_G + R_{drv})$$

As the threshold gate voltage of the *GS61008T* is 1.6 V , for staying switched off during the off period:

$$v_{gate} = 465\text{ mA} * (R_G + 1.3\text{ }\Omega) < V_{G(th)} = 1.3\text{ V}$$

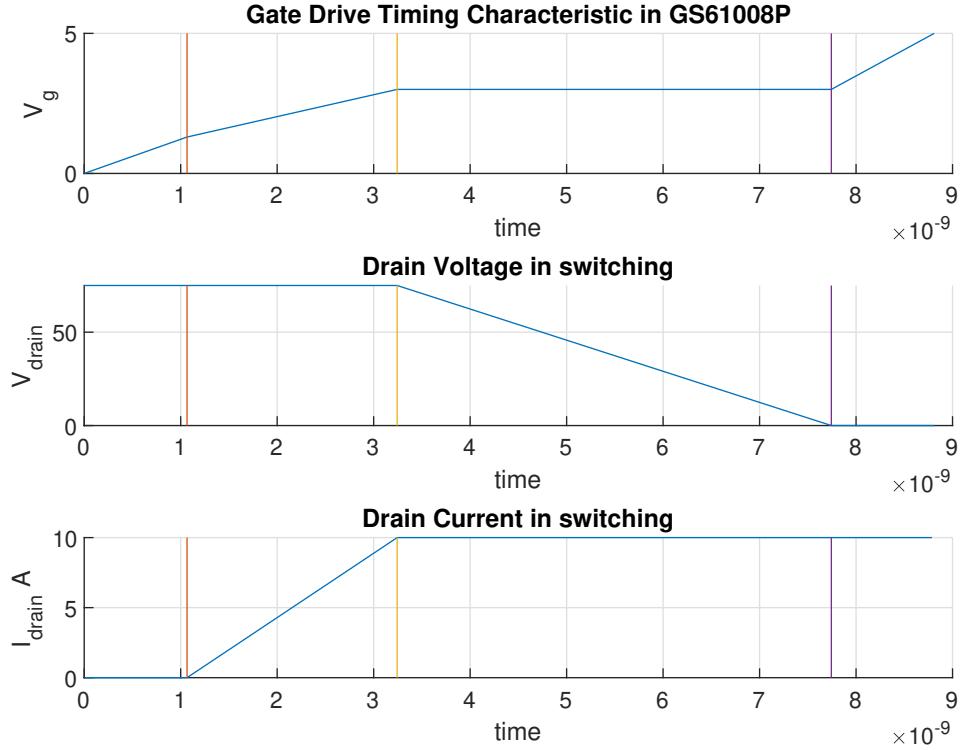
$$R_{G,max} = 1.49\text{ }\Omega$$

This voltage, which is produced at the gate of MOSFET, is due to the positive $\frac{dv}{dt}$. During the negative edge of the drain voltage, the scenario is the same with this difference that the direction of the current is reversed and the voltage at the gate will be negative. If this voltage crosses the safety margin of the gate voltage, the transistor will be damaged. The tolerable range of the gate voltage is in between -10 V to $+7\text{ V}$. This voltage depends on the $R_{G,on}$ and should be calculated. However, using a TVS diode in between gate and source of the MOSFET to clamp this voltage is recommended.

This resistance, calculated above, is the external off-resistance of the driver. The *pe29102* comes with the capability of having different paths for turning on and turning off the MOSFET. For turning on the R_G , the criterion of selection is a trade-off between the robustness and stability of the MOSFET by bigger R_G , and higher speed and lower switching losses by smaller R_G . Gate ringing or sustained oscillation is the big risk of reduction of the R_G . In single-ended topologies or in resonant topologies the $\frac{dv}{dt}$ or $\frac{di}{dt}$ are lower than their hard-switching counterparts which leads to lighter design criteria.

4.4.3 MOSFET Turning On Sequence

Generally, for the turning-on sequence there are four steps, which are shown in *Figure 4.6*.



Figures 4.6: MOSFET Turning-On Sequence

Whenever the high speed driver alternates V_g from 0 V to 5 V, this change would not be directly imposed to MOSFET due to the resistance and the input capacitances of the gate of the MOSFET, and it would make a delay. This sequence can be divided into 4 steps:

- Step1:** During this step the gate of MOSFET starts with absorbing the charge through R_G . However, the shape of this current is strongly related to the type of load, which is connected to the drain of MOSFET. This effect has been neglected to simplify the calculation. This step starts at the time, when the voltage at the gate of MOSFET is 0 V until the time that the gate of MOSFET reaches the gate threshold voltage $V_{g(th)}$. During this stage both equivalent capacitors of the MOSFET, C_{gd} and C_{gs} , will be charged simultaneously.

$$time : 0 \rightarrow t_1$$

$$V_G : 0 \rightarrow V_{GS(th)}$$

$$V_{GS(th)} = V_G * (1 - e^{(-t \frac{R_G}{C_{gs} + C_{gd}})})$$

$$t_1 = R_G * (C_{gs} + C_{gd}) \ln(\frac{V_G}{V_G - V_{th}})$$

Since during this stage there is no conduction of current in the MOSFET, the loss during this stage is *zero*.

2. **Step2:** During this step, the gate of MOSFET experiences a voltage beyond its threshold, which indicates the starting point of conduction for the MOSFET. A current will flow in the drain of the MOSFET and as the gate voltage increases, the drain current also increases ($g_m \cdot v_{gs}$). In this stage C_{gs} and C_{gd} continue charging until the voltage of the MOSFET reaches to the **plateau voltage**. Due to the current flowing in the drain and the drain voltage, the MOSFET suffers from the **switching loss** during this step.

time : $t_1 \rightarrow t_2$

$$V_G : 0 \rightarrow V_{GS(pl)}$$

$$t_2 = R_G * (C_{gs} + C_{gd}) \ln\left(\frac{V_G}{V_G - V_{pl}}\right)$$

3. **Step3:** During this step, due to the **Miller effect**, V_{GS} remains constant at the plateau voltage. In this stage the drain voltage starts to decrease, until reaching its turn-on voltage. In this stage the gate driver only charges the C_{gd} . The Drain voltage decreases, meanwhile the current remains constant on its final value. The **switching loss**, here in this step is important because of its longer duration.

time : $t_2 \rightarrow t_3$

$$V_G : 0 \rightarrow V_{GS(pl)}$$

$$t_3 - t_2 = \frac{Q_{gd} \cdot R_G}{V_G - V_{GS(pl)}}$$

4. **Step4:** In this stage, gate is charged to over-saturated state. Both C_{gd} and C_{gs} continue to charge until reaching to their driving voltage. Since in this stage, there is no voltage transition, there is no switching loss.

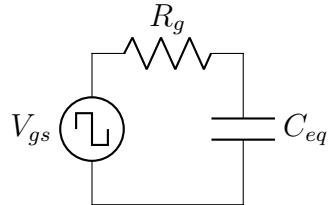
It is obvious that, if a fast driver drives a GaN MOSFET, the gate of the MOSFET plays an important role in injection of the delay into the drain voltage, due to the intrinsic capacitors of the gate.

4.4.4 Calculating Required Drive for the MOSFET:

There are some methods to calculate the required drive for the gate of a MOSFET. Two of them will be briefly introduced here: **1-Equivalent Capacitor Method** and **2-Gate Input Charge**

Equivalent Capacitor Method:

In this method, the amount of the current to turn-on or turn-off the transistor will be investigated. The equivalent model of the transistor is illustrated in *Figure 4.7* and in this model the values of the capacitors of the MOSFET are considered constant.



Figures 4.7: Equivalent Circuit of Gate

$$\begin{aligned}
 V_{C_{gs}} &= 0, \Delta V_{C_{gs}} = V_{gs,max} \\
 V_{C_{gd}} &= -V_{out}, \Delta V_{C_{gd}} = V_{gs,max} \\
 Q_{total} &= V_{gs} \cdot C_{gs} + (V_{gs} + V_{out}) \cdot C_{gd} \\
 C_{eq} &= \frac{Q_{total}}{V_{gs,max}} = C_{gs} + C_{gd} \left(1 + \frac{V_{out}}{V_{gs,max}}\right) \\
 Q_{total} &= I_g * t_{on} = C_{eq} * V_{gs,max} \\
 \Rightarrow I_g &= \frac{C_{eq} \cdot V_{gs,max}}{t_{on}}
 \end{aligned}$$

Since there are two capacitors connected to the gate of the MOSFET- C_{gs} and C_{gd} - the C_{eq} contains these two capacitors. However, C_{gd} behaves as a miller capacitance between input and output of the MOSFET, therefore the effect of this capacitor on loading the gate-driver is very important. For the MOSFET **GS61008T**, the C_{gd} and C_{gs} and the maximum drain voltage are:

$$\begin{aligned}
 V_{DD} &= 75 \text{ V and } V_{gs,max} = 5 \text{ V} \\
 C_{gs} &= 578 \text{ pF and } C_{gd} = 12.5 \text{ pF} \\
 C_{eq} &= C_{gs} + C_{gd} \left(1 + \frac{V_{out}}{V_{gs,max}}\right) \\
 C_{eq} &= 578 + 12.5 * \left(1 + \frac{75}{5}\right) = 778 \text{ pF} \\
 I_g * t_{on} &= C_{eq} \cdot V_{gs,max} = 778 * 10^{-12} * 5 = 3.89 * 10^{-9} \\
 I_g * t_{on} &= 3.89 * 10^{-9}
 \end{aligned}$$

Here, t_{on} mainly represents the rise time of the signal, when capacitors drain the current in order to be fully charged. Therefore, if we limit the current of gate by R_g to 1 A, consequently we would have about 3.89 ns rise time. Reciprocally, to reach a rise-time of 7 ns, we need less than 0.5 A to drive the MOSFET.

$$I_g = \frac{3.89 * 10^{-9}}{7 * 10^{-9}} < 0.5 \text{ A}$$

Gate Input charge:

In this method, the current to drive the gate of MOSFET is simplified by using the total electrical charge needed to turn on the MOSFET. It is assumed, that during charging the current of gate is constant:

$$Q_{total} = I_g * t_{on} \Rightarrow I_g = \frac{Q_{total}}{t_{on}}$$

$$I_g = \frac{12 * 10^{-9}}{7 * 10^{-9}} \simeq 1.7 \text{ A}$$

For the discharging (falling edge of the gate pulse) we can use the same calculation.

4.4.5 Gate Power Loss:

The energy-transfer from the gate-driver to the gate of the MOSFET, involves power dissipation. This dissipation is the energy stored in the capacitances:

$$E_{C_e} = \frac{(V_{GS})^2 * C_e}{2} \rightarrow \text{Energy loss for } \uparrow \text{ or } \downarrow \text{ edge}$$

$$\begin{aligned} \text{Total } E_{C_e} &= (V_{GS})^2 * C_e \\ \text{and } Q &= \frac{\text{Energy}}{\text{Voltage}} \\ \Rightarrow P_{g,Loss} &= V_{gs} * Q_g * f_s \\ \Rightarrow P_{g,Loss} &= 5 * 12 * 10^{-9} * 5 * 10^6 = 0.3 \text{ W} \end{aligned}$$

Though this amount of power-loss is quite low, it is important however and will be considered in the calculation of the heat-sink.

4.4.6 Gate Resistance (Turn-ON):

As previously mentioned, the selection of gate resistance is a trade-off between robustness and speed. Since in the current project the priority is speed, the resistance is as high as possible, while still in compliance with the timing characteristics. The gate driver **PE29102** can only provide 2 A at its output while the internal resistance of the driver is 1.9 Ω. This means, that it is not permitted to connect the output of this driver, directly to the MOSFET, since gate of MOSFET behaves as a big capacitor in high frequency.

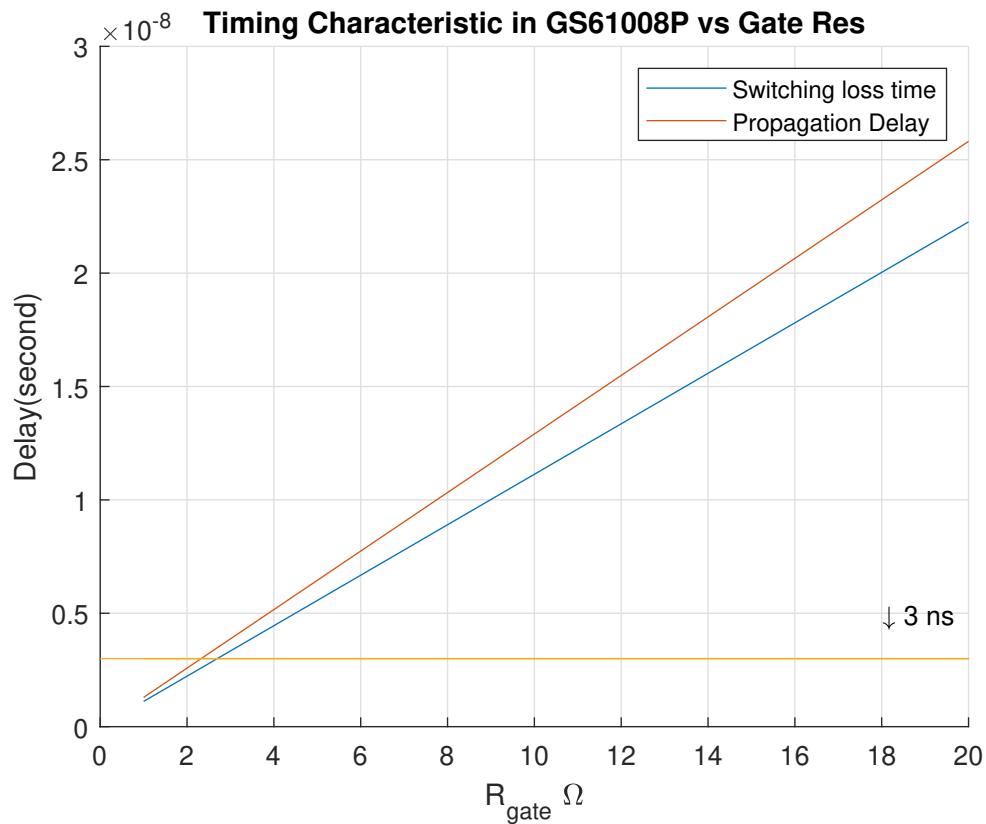
$$i_g = \frac{v_g}{R_{drv} + R_g} = \frac{5 \text{ V}}{1.9 \Omega} = 2.65 \text{ A} > 2 \text{ A}$$

$$R_G = 2.5 \Omega \Rightarrow R_{g,min} = 0.6 \Omega$$

Therefore, there is a necessity for a resistance to limit the current of the gate. In addition, any resistances at the gate will aggravate the switching characteristics of a MOSFET. In *Figure 4.8*, gate-resistances versus propagation delay and duration of switching loss are illustrated. The higher the resistance at the gate, the more duration of the switching loss and the more propagation delay. For example, at about 10Ω , the propagation delay is about 13 ns and duration of the switching loss is about 11 ns . For 2.5Ω gate resistor, the propagation delay is about 4 ns and duration of the losses is about 3 ns . For safe operation an external $4,7 \Omega$ for the gate driver has been used, which leads to this amount of propagation delay:

$$R_g = 4.7 \Omega \Rightarrow R_g = 6.6 \Omega$$

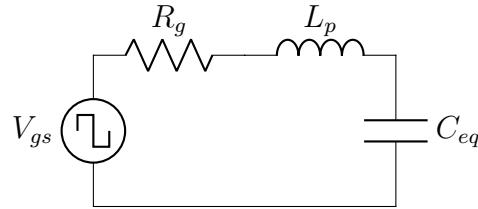
$$t_{prop} = 8 \text{ ns}, t_{loss} = 7 \text{ ns}$$



Figures 4.8: Timing characteristics vs resistance in gate

4.4.7 Gate Resistance and Parasitic Oscillations:

As it was previously mentioned, the selection of the gate resistance is a trade-off between robustness and speed. In this section the robustness of the gate of the MOSFET and its relation with the gate resistance will be explained.



Figures 4.9: High-frequency equivalent circuit of the gate of MOSFET

Due to the parasitic inductance between the gate of the MOSFET and the output of the gate-driver, an RLC series circuit is constructed(*Figure 4.8*), which would oscillate at a certain frequency. The amplitude of this oscillation, which affects the operation of the MOSFET, is important and should be canceled out. Sometimes, the amplitude of oscillation becomes larger and puts the MOSFET into on-off mode, which causes damage to the MOSFET. This oscillation is always considered as the merit of robustness of the gate and it should be kept as low as possible. The RLC loop has a Q-factor and by controlling this Q-factor, the ringing and oscillation can be canceled out.

$$Q = \frac{Z_r}{R_g} = \sqrt{\frac{L_p}{C_e}} / R_g$$

The important point here is that if the Q-factor was high, the RLC circuit would simply oscillate(resonance). A higher Q is equivalent with a lower R_g . Therefore, a lower R_g will lead to higher Q and respectively more oscillation and less robustness. Unfortunately there is no rule to specify the exact value of Q, since there is no exact definition for the robustness of the gate of the MOSFET. However to damp the most induced oscillation $Q \approx 1$ is fairly enough. $Q \approx 1$

$$\begin{aligned} L_p &\approx 2 \text{ nH} \\ C_e &\approx 778 \text{ pF} \\ R_{g,min} &= \frac{\sqrt{\frac{L_p}{C_e}}}{Q} = \sqrt{\frac{2 * 10^{-9}}{778 * 10^{-12}}} \approx 1.6 \Omega \\ R_{g,min} &= 1.6 \Omega \end{aligned}$$

4.4.8 Dead-Time Calculation:

The half-bridge topology consists of two MOSFETs in a leg, which connects V_{DD} to GND . In order to avoid ***cross conduction*** of the MOSFETs, some considerations should be adhered. One of them, is ***dead-time*** between high and low pulses, which are oscillating in an inverted manner. Since the propagation delay of the used driver at minimum dead-time is 9 ns and the rise-times and fall-times of the pulse at the output pin of the driver is about 2 ns, while the propagation delay of every MOSFET is about 8 ns, we set

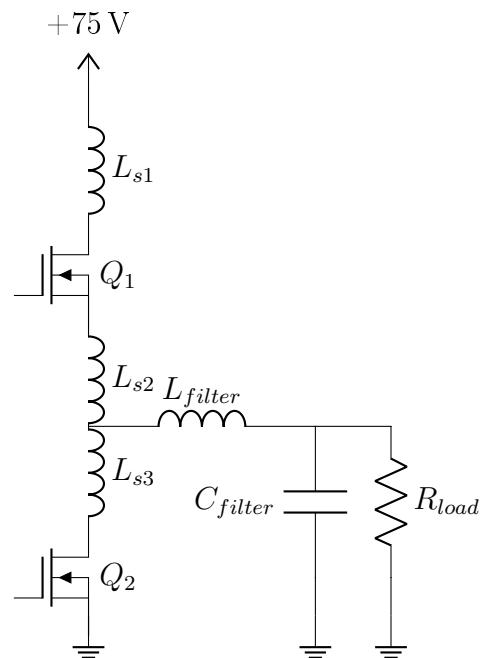
$$t_{deadtime} = 9 + 2 + 8 = 19 \text{ ns}$$

4.5 CDPA Power Section

A CDPA behaves like a synchronous buck converter with the cut-off frequency of its low-pass filter beyond the band-width of input signal. Furthermore, a CDPA operates in hard-switching mode to provide the exact wave-shape at its output. Since the operating frequency of the converter is high(5 MHz), the parasitic elements of the semiconductors, as well as the PCB tracks play important roles. In other words, using soft-switching techniques may be theoretically introduced but it should be experimentally tested, since in this frequency, RLC branches constructed by parasitic elements are considerable.

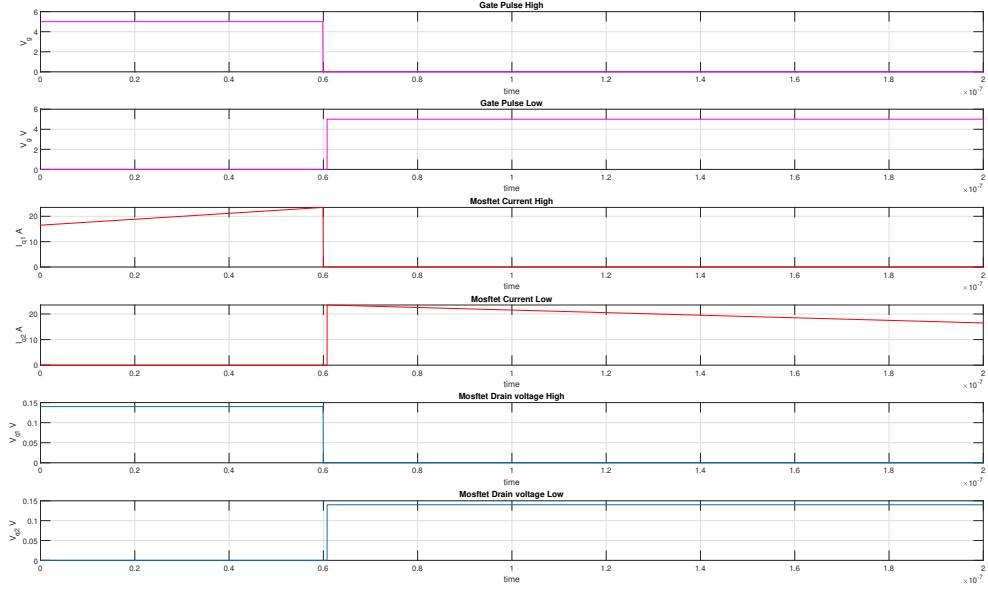
4.5.1 Sequence of Operation:

The CDPA operates much like a synchronous buck converter. The high side transistor Q_1 injects the current to the output stage by connecting the load to V_{DD} , and the lower transistor inject the current to output stage by connecting the load to GND . The device is operating in hard-switching mode, which means voltages and currents, without any barriers of soft-switching, start to increase or decrease. To avoid shoot-through, due to the rise-time and fall-time of the current and voltage, a dead-time between high-pulse and low-pulses has been introduced.



Figures 4.10: High-frequency equivalent circuit of the CDPA

In order to clarify the sequence of operation, it is divided into 3 stages (*Figure 4.11*):



Figures 4.11: CDPA sequences of operation

1. **Q_1 ON and Q_2 OFF:** In this stage, after turning on the upper MOSFET, the current flows through the Q_1 to the output load. This means, that in this stage the voltage across the drain-source V_{ds} drops to a voltage near to zero ($R_{ds} * I_d$). The current of MOSFET, in the steady state of operation is not a fixed value and has variation. In other words, there is an average part of the current of inductance, and an ac-part which will be indiscriminately considered.
2. **Q_1 OFF and Q_2 OFF:** Due to the non-ideal nature of MOSFET, even GaN MOSFET, a dead-time between high-pulse and low-pulse should be inserted to avoid shoot-through of MOSFETs, which would suddenly lead to damage of the MOSFETs. The duration of this dead-time should be short enough, as to affect the wave-shape of converter. Since the current of output-inductance should be continuous, there should be a path for conducting this current when a switch is turned-off. Although MOSFETs behave similar to an ideal switch, however they have an intrinsic body diode, which is an anti-parallel diode, connected inversely and used to conduct this reverse current. The body diode of the selected GaN MOSFET **GS61008T** is not a normal body diode; It is a combination of an ultra-fast diode and a resistor. Although the problem of reverse-recovery of the diode is a little bit mitigated, it is recommended to use an external super-fast diode in parallel with that MOSFET in order to improve the efficiency of the converter.
3. **Q_1 OFF and Q_2 ON:** In order to change the output voltage to a desired level, the output load R_L through an L-C filter will be connected to V_{DD} and GND . The connection to V_{DD} is done by the upper MOSFET and connection to the GND is done by the lower MOSFET. When the upper MOSFET is turned on, the energy of

the output load and also the energy in the inductance will be provided through V_{DD} , therefore, the current in the inductance, due to the positive voltage, will start to increase and respectively the energy in the inductance will also increase. When the lower transistor is turned on, the required energy for the load will be provided by the stored energy of the inductance. In this stage, the current of inductance decreases with the rate of $-\frac{V_{out}}{L_{filter}}$

4.5.2 Two Challenges: $\frac{di}{dt}$ and $\frac{dv}{dt}$

There are two major causes of risk in the CDPAs, which together with high-frequency operation make a potential point of failure for the converter: *The parasitic inductances*, which originate from the PCB tracks and the connection to the MOSFETs to the PCB and silicon-die, are vulnerable to $\frac{di}{dt}$, and by an abrupt change, they will produce spikes on the drain of the MOSFET which is usually accompanied by ringing phenomenon. This ringing is due to resonance circuit of this parasitic inductance and other capacitances.

$$V = L * \frac{di}{dt}$$

$$di = 20 \text{ A} \quad dt = 7 \text{ ns}$$

$$1 \text{ nH} \leq L \leq 100 \text{ nH}$$

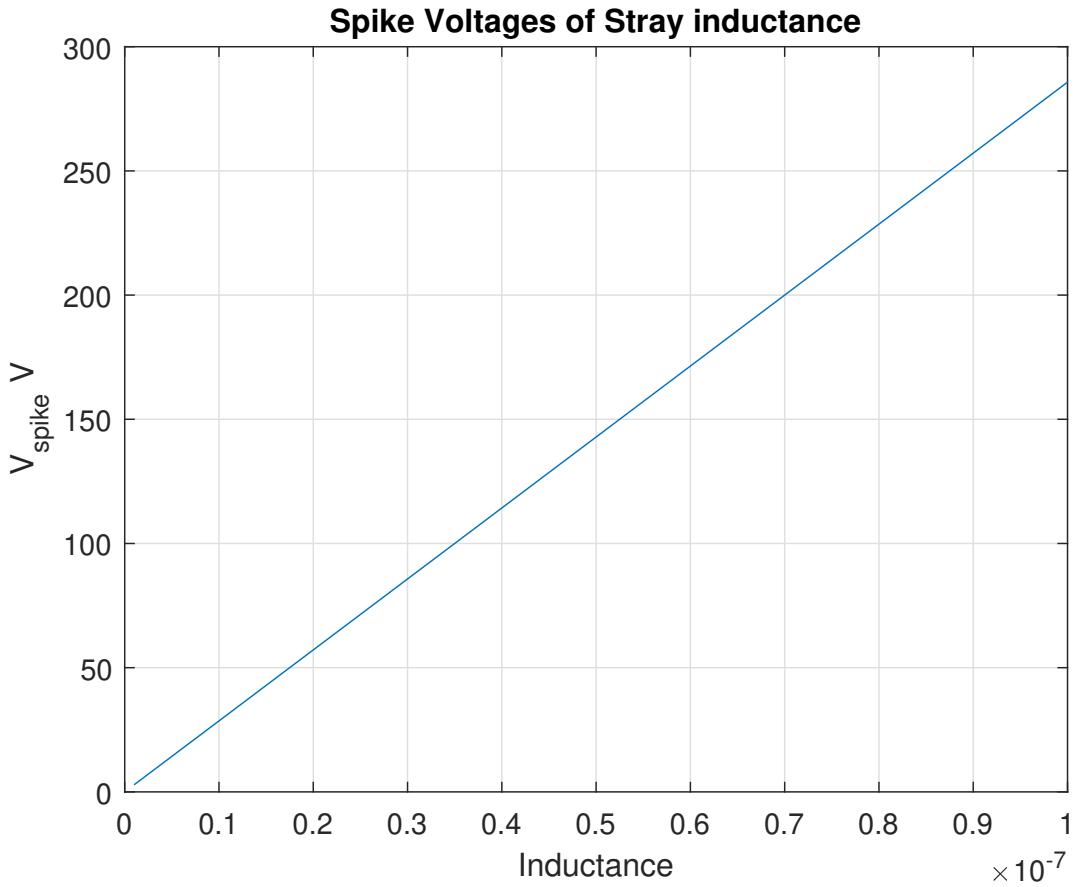
As can be seen in *Figure 4.12*, by increasing stray inductance, the spike voltage will be increased, which in the long-term affects the efficiency and lifetime of the MOSFET. The common solutions for these spikes are using soft-switching and resonant techniques, which are not subject of this work. Keeping the distance between the components in the circuit as low as possible, is the simplest step to mitigate this problem.

There is a similar story for the *capacitors* (*Figure 4.13*), when they experience a high $\frac{dv}{dt}$. This change will lead to a high spike of the current, and this spike of current becomes important, when these capacitors are parts of the MOSFET, since these currents can overheat the MOSFET and affect the lifetime and efficiency. Paths, which have small amount of the resistance, are vulnerable to this effect. A treatment against these spikes on voltage and current is designing the PCB of the circuit as condensed as possible and selecting bypass capacitors to take out this current from the semiconductor into the capacitor at the price of reduced speed.

$$I = C * \frac{dv}{dt}$$

$$dv = 75 \text{ V} \quad dt = 7 \text{ ns}$$

$$10 \text{ pF} \leq C \leq 1000 \text{ pF}$$

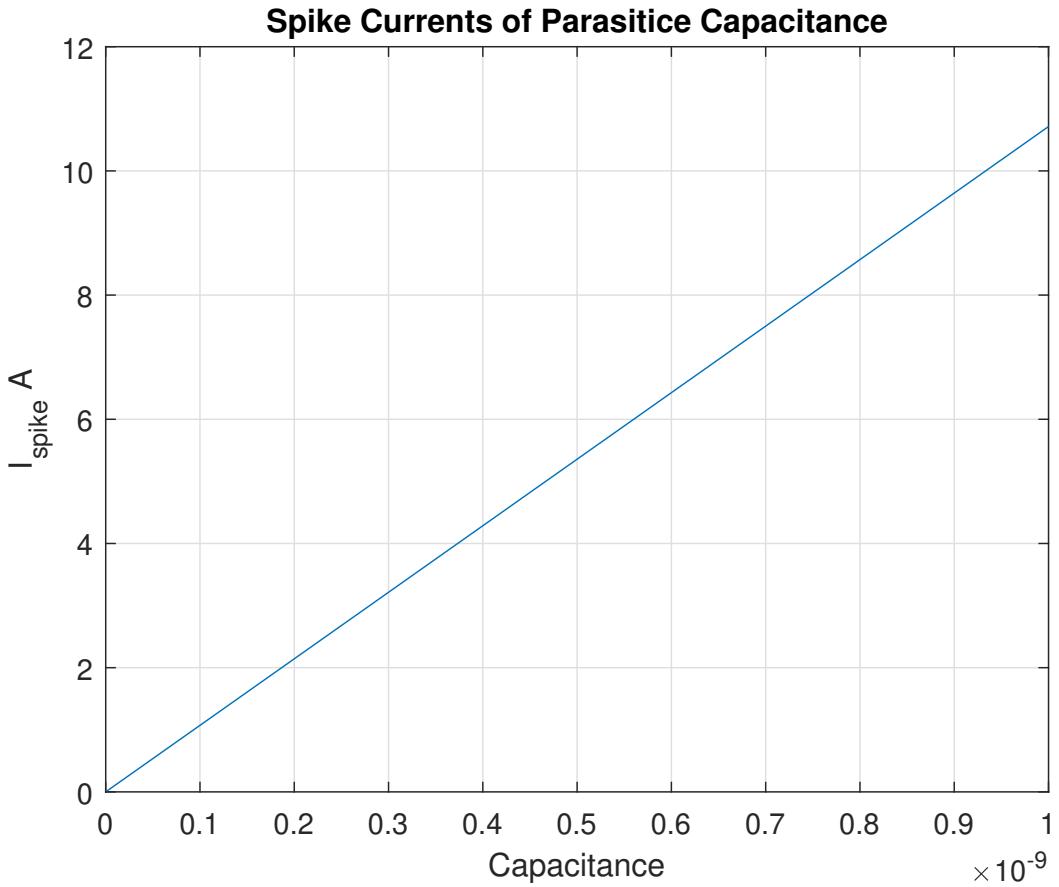


Figures 4.12: Spike voltage vs inductance

4.5.3 Body Diode:

The weak point of the traditional power MOSFET is the body diode and its weak timing characteristics, which leads to some bad phenomena; such as high current spikes and ringing of the drain voltage, which are unwanted and should be well mitigated. The high spikes of the current are the main culprit for electromagnetic interference(EMI). The body diode of a MOSFET is compatible with the MOSFET. For example, if the MOSFET is rated for a drain current $I_D = 10 A$ then the rating of this body diode is the same as for the MOSFET.

In comparison to normal power MOSFETs the GaN transistors have a different structure. MOSFET **GS61008T** is an enhancement mode HEMTs, which does not need an intrinsic body diode and there is zero reverse recovery charge. These devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.



Figures 4.13: Spike current vs inductance

On-state condition ($V_{GS} = +6 \text{ V}$):

The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition ($V_{GS} \leq 0 \text{ V}$):

The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{gd} , exceeds the gate threshold voltage. At this point, the device exhibits a channel resistance. This condition can be modeled as a “body diode” with slightly higher V_F and no reverse recovery charge. If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)} + V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop V_F and hence increase the reverse conduction loss.

4.6 Losses in MOSFET

In every MOSFET, two main categories of losses can be considered:

1. *Ohmic Losses*
2. *Switching Losses.*

Ohmic Losses originate from the resistive essence of the MOSFET, the $R_{DS(ON)}$ plays the main role here; the lower $R_{DS(ON)}$, the lower the ohmic losses. The *Switching Losses* are part of a big family of losses, which have some subsets, which will be mentioned here. Losses of a MOSFET should be precisely calculated for the worst case - ohmic and switching. The losses in a MOSFET are decisive on designing the heat-sink for the MOSFETs, in order to keep the temperature of the junction of the MOSFET in an acceptable region. Moreover, the calculation of the losses for every project, is important and for the high-frequency converters these calculations are vital.

4.7 Hard-Switching Topologies and Switching Losses

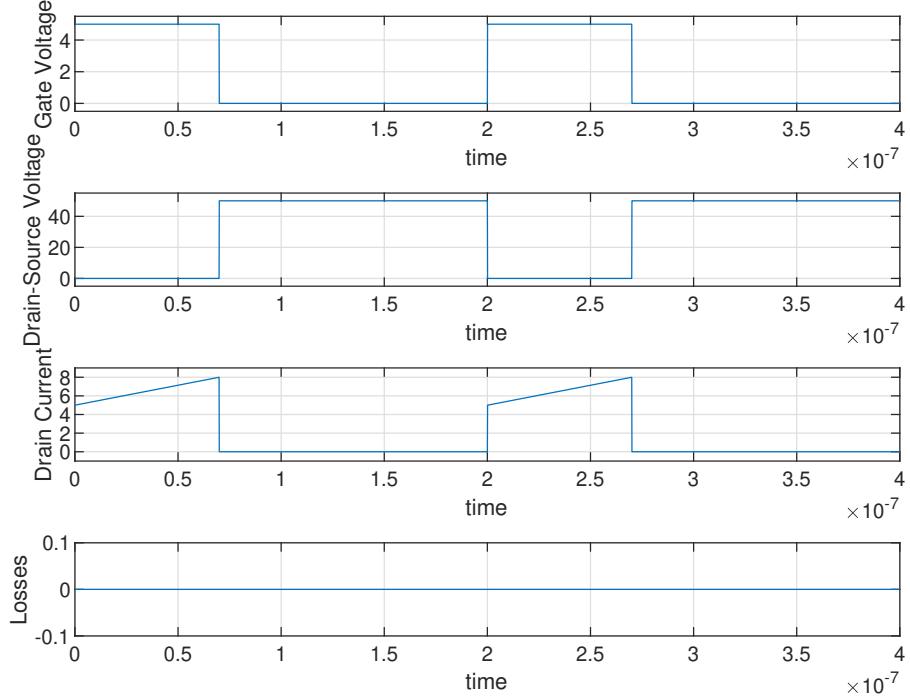
In hard switching topologies, the transistor is turned on and off without additional circuitry, which limits the current or voltage of the transistor at turning-on or turning-off points. In ideal MOSFETs, as shown in *Figure 4.14*, there is no overlap between the current and voltage on these two points, therefore the loss, which is calculated

$$P_{loss} = V_{ds} * I_d$$

is zero. However, due to the non-ideal behavior of a real MOSFET and also its intrinsic parasitic elements, the current and voltage of the MOSFET on turn-on and turn-off points overlap each other, which leads to losses. These losses obviously depend on amount of current and voltage at the MOSFET in these points, as well as the frequency of the switching.

In *Figure 4.15*, losses at turn-on and turn-off points are illustrated with good approximation. The losses, which a MOSFET can tolerate, are different for rising and falling edges. While, the current and voltage of the MOSFET should be kept less than the maximum rating, which can be found in its datasheet, the combination of these losses and the imposed time, should also be kept in the *Safe Operating Area, SOA* of the MOSFET, which can as well be found on the datasheet of the MOSFET. It should be guaranteed, that the MOSFET can not reach the bounds of its limitation and for every design a guard-band distance from these limitation should be considered.

All the losses in electronic devices dissipate as heat, and for the heat the appropriated number is the *Root-Mean-Square RMS* of a wave-shape. For the *Figure 4.15* the RMS value, which is calculated by *Matlab*, is about 12 Watt.



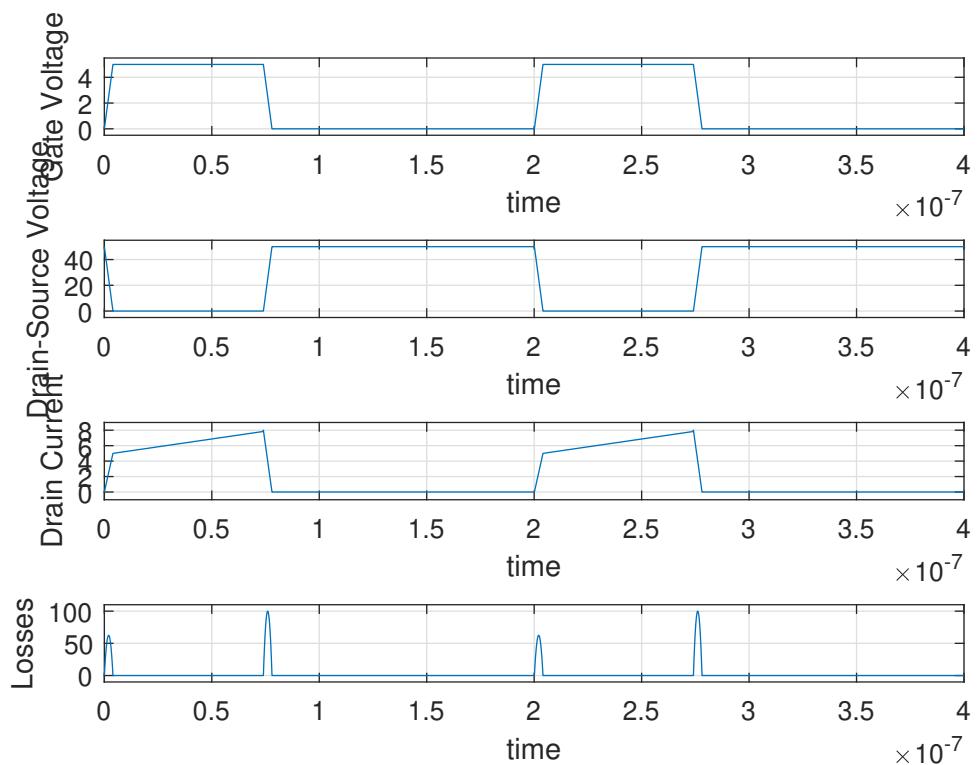
Figures 4.14: Ideal MOSFET Current and Voltage shapes

4.8 Ohmic Losses

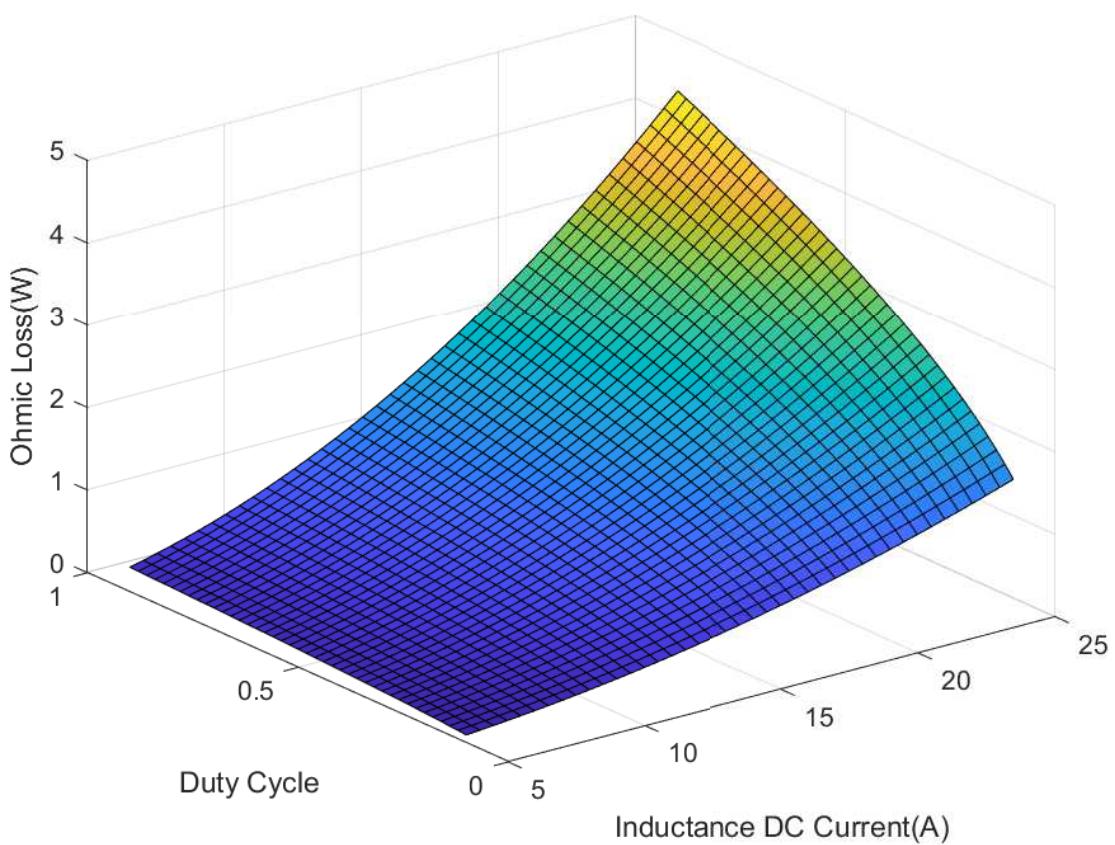
As previously mentioned, the ohmic losses depend directly on the $R_{DS(ON)}$. For this project, every MOSFET GS61008T has $7 \text{ m}\Omega R_{DS(ON)}$. Since the generated heat depends on the RMS value of the power, we neglect the switching losses in this section. With regard to *Figure 4.14*, we can calculate this loss. Since in this project, we do not intend to design a DC power supply and we want an AC power amplifier, we put our restriction only on the output current and we restrict it to 20 A. As can be observed in *Figure 4.16*, the maximum ohmic losses are then restricted to 5 W. It is also clear, that there is no relation between the supply voltage V_{DD} and the ohmic Losses. Duty cycle and output current of the amplifier are decisive parameters of a converter in ohmic losses. Another point, which is clear to witness in *Figure 4.16*, is quasi-2nd-power increment behavior of the MOSFET RMS losses in comparison to current which can be viewed on *Figure 4.17*, moreover, the output power has quasi-exponential behaviour as $K_1(1 - e^{-k_2*t})$ *Figure 4.18*.

4.9 GaN MOSFET Switching Losses

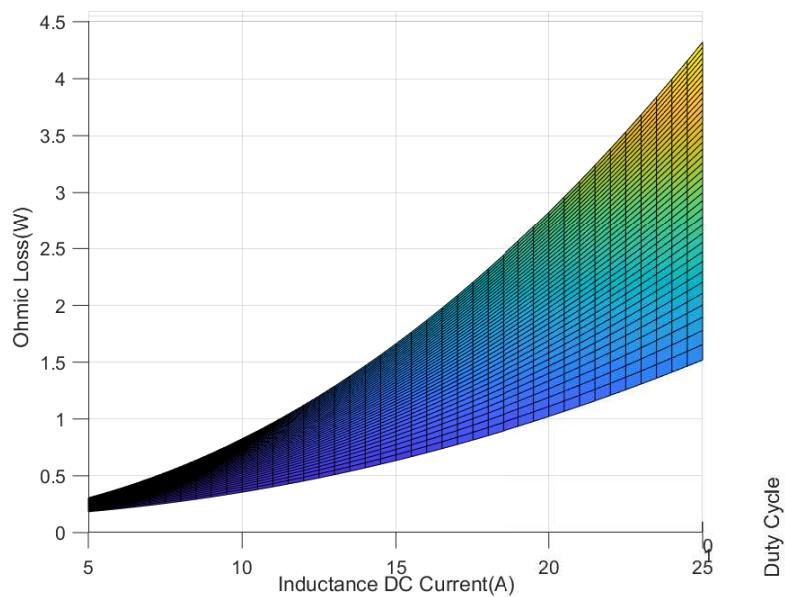
Switching transistors exhibit significant power losses during the transition event. The criterion of performance of a converter can be listed as below [12]:



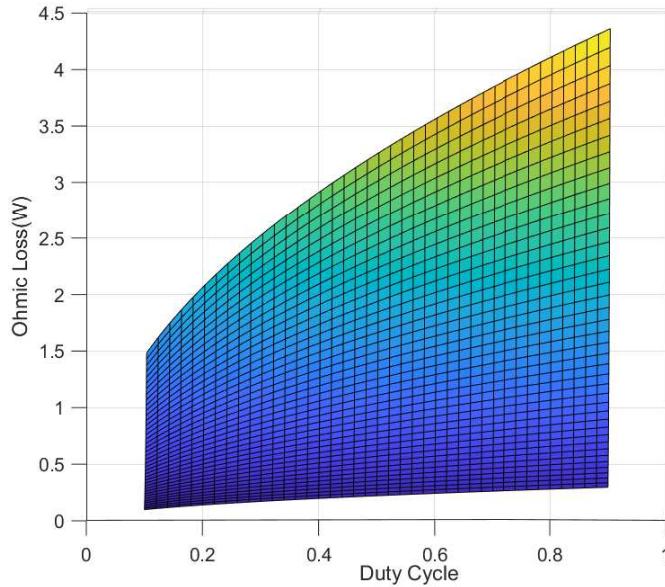
Figures 4.15: Real MOSFET Current and Voltage shapes



Figures 4.16: Ohmic Losses per MOSFET



Figures 4.17: Ohmic Losses per MOSFET versus Current



Figures 4.18: Ohmic Losses per MOSFET versus Duty-Cycle

1. *Efficiency*: higher is better
2. *Size*: smaller is better
3. *cost*: lower is better

Efficiency can be increased through improvements in the switching (frequency of switching - dynamic) and conduction (ohmic loss of a transistor-static) characteristics of devices. By designing a device for higher switching frequencies, the magnitude of the inductance and capacitance will be decreased, which in turn leads to a size reduction, which also can tend to lower cost. In order to use higher frequency in switching the device, the transistor must have very low dynamic losses. The factors, which are playing role in the dynamic behavior of a MOSFET, are as below: [12]

1. P_{oss} : Output capacitance losses
2. P_G : Gate charge losses
3. P_{SD} : Reverse conduction losses
4. P_{RR} : Reverse recovery losses

4.9.1 P_{oss} Output Capacitance Losses

This loss is related to the output capacitance of the transistor. The charging or discharging of this capacitor, requires energy [12].

4.9.2 P_G Gate Charge Losses

Every gate of a transistor has a capacitance, which similarly to the output capacitance, needs energy for charging and discharging [12].

4.9.3 P_{SD} Reverse Conduction Losses

An anti-parallel diode which can be found across the drain-to-source terminals of the device. It is inherent to the device structure, such as in MOSFETs. In the case of enhancement-mode GaN transistors, there is a mechanism to conduct reverse current when the device is off, allowing operation similar to a diode. Diode conduction is a function of the switching transient, therefore they are included in the hard-switching loss calculation. These losses are defined as reverse conduction losses (P_{SD}) [12].

4.9.4 P_{RR} Reverse Recovery Losses

Reverse recovery losses are not applicable to GaN HEMT, since there are no minority carriers involved in conduction in an enhancement mode GaN HEMT. Therefore Q_{RR} is zero, which is a significant advantage compared with power MOSFETS [12].

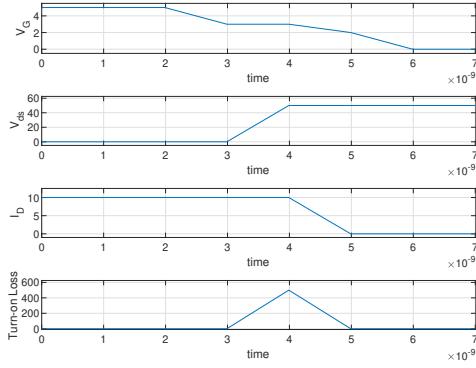
4.10 Switching Losses

Summing the voltage transition power losses P_{vt} and the current transition power losses P_{ct} will give us the total switching losses P_{sw}

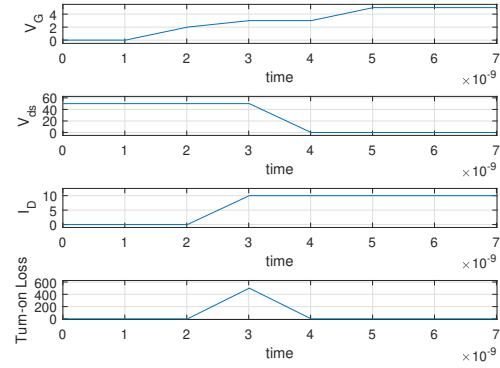
$$P_{sw} = P_{ct} + P_{vt}$$

$$\Rightarrow P_{sw} = \frac{1}{2} \cdot V_{BUS} \cdot I_L \cdot (t_{xR} + t_{xF}) \cdot f_{sw}$$

As can be seen in *Figure 4.20* and *Figure 4.19*, the t_{xR} can be t_{cR} or t_{vR} , which represent the rise time of the drain-source voltage on turning-off the transistor and the rise time of the drain current on turning-on the transistor. Respectively, t_{xF} stands for fall time of the voltage or current. These two times, t_{xR} and t_{xF} , are not given in the datasheet and shall be calculated from the gate charge Q_G characteristics of device based on the circuit operating conditions [12].



Figures 4.19: Turn-Off Loss



Figures 4.20: Turn-On Loss

4.10.1 Transistor Switching Behavior:

Transistor switching behavior can be segmented into four different regions as is illustrated in *Figure 4.21*.

1. Q_{GS1} : The charge required to bring the gate electrode up to device threshold.
2. Q_{GS2} : The charge required to transition the current from zero to the load current
3. Miller Charge Q_{GD} : The charge required to transition the drain-to-source voltage
4. $Q_G - (Q_{GS1} + Q_{GS2} + Q_{GD})$: The incremental additional charge to overdrive the gate

Miller Charge Q_{GD} :

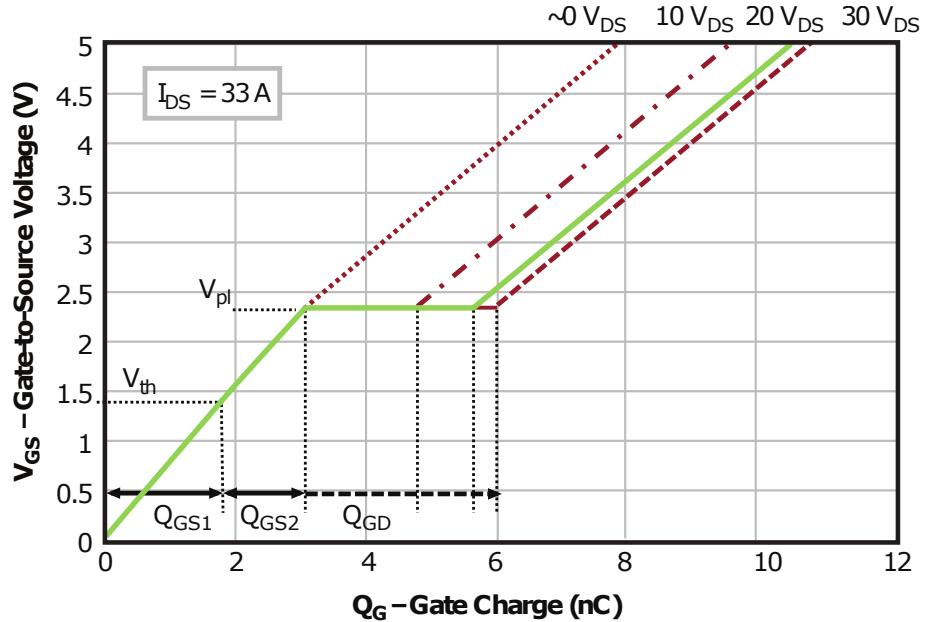
The voltage commutation period of a traditional hard-switching commutation is due to the Miller charge. The Miller charge is expressed by the plateau voltage on the gate of the MOSFET and can be used to calculate the switching losses during the voltage transition period. At turn-on, the period waits till the current has fully transitioned, and is finished when the drain-to-source voltage has reached zero. The reverse process happens for turn-off. "The larger the voltage swing, the longer it will take for the transition, and the higher the losses" [12].

$$P_{Vt} = \frac{V_{BUS} \cdot I_L}{2} \cdot t_{vX} \cdot f_{sw}$$

$$\Rightarrow P_{Vt} = \frac{V_{BUS} \cdot I_L}{2} \cdot \frac{Q_{GD}}{I_G} \cdot f_{sw}$$

The gate current ($I_{G,v_{on}}$) during the turn-on voltage transition period (t_{vF}) can be estimated as; Where V_{DR} is the gate driver on-state output voltage.:

$$I_{G,v_{on}} = \frac{V_{DR} - V_{PL}}{R_{G,on}}$$



Figures 4.21: Impact of drain-source voltage and drain current on gate charge and gate voltage

The gate current ($I_{G,v_{off}}$) during the turn-off voltage transition period (t_{vR}) can be estimated

$$I_{G,v_{off}} = \frac{V_{PL}}{R_{G,off}}$$

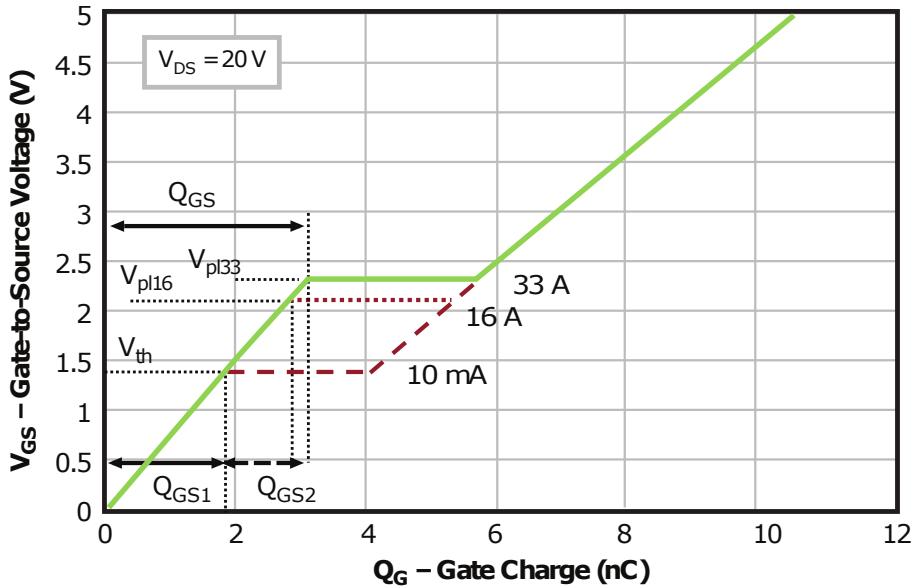
Gate Charge (Q_{GS2}): The Current Transition Period

The charge that determines the current transition time is Q_{GS2} . For the turn-on point, the period begins after the gate voltage reaches the threshold voltage V_{th} and then current begins to flow. It is complete when the drain-to-source voltage V_{ds} begins to transition. For turn-off, the sequence happens in reverse. *"The larger the current swing, the longer it will take for the transition, and power losses will increase"*. The higher the drain current, the longer the period lasts [12].

The relationship between the gate voltage and drain current is non-linear and therefore with normal method cannot be estimated and requires a graphical technique to estimate Q_{GS2} . Q_{GS1} can be generally calculated using

$$Q_{GS1} = \left(\frac{Q_{GS}}{V_{pl}} \right) \cdot V_{th}$$

Since Q_{GS} and V_{pl} both vary proportionally with current and drain-source voltage, their ratio is virtually constant. Therefore, Q_{GS1} is a fixed value regardless of operating conditions.



Figures 4.22: Impact of drain current on the gate plateau voltage

The $Q_{GS(op)}$, which is the Q_{GS} at the operating value of I_{DS} , can also be calculated for the operating conditions by reading the plateau voltage $V_{pl(op)}$ from the transfer characteristic.

$$Q_{GS(op)} = \left(\frac{Q_{GS}}{V_{pl}} \right) \cdot V_{pl(op)}$$

$$Q_{GS2} = Q_{GS(op)} - Q_{GS1}$$

$$\begin{aligned} P_{ct} &\approx \left(\frac{V_{BUS} \cdot I_{DS}}{2} \right) \cdot t_{Cx} \cdot f_{sw} \\ &= \left(\frac{V_{BUS} \cdot I_{DS}}{2} \right) \cdot \frac{Q_{GS2}}{I_G} \cdot f_{sw} \end{aligned}$$

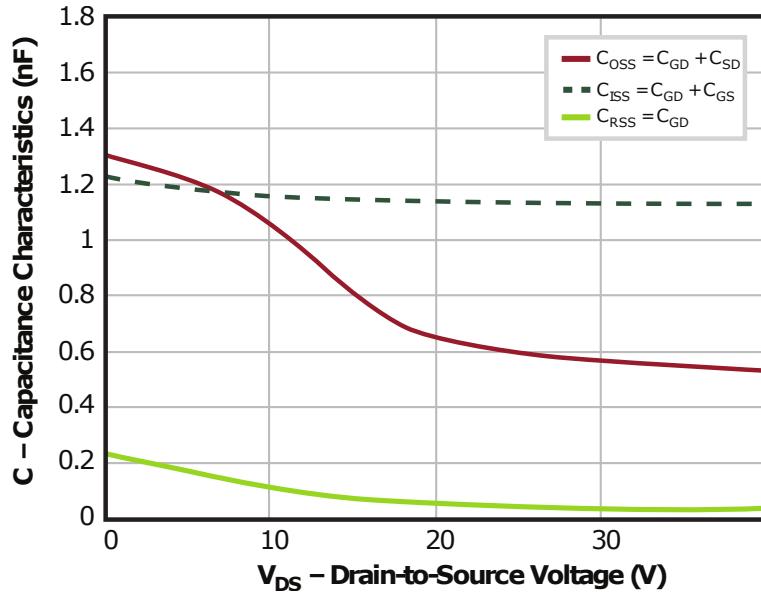
Then the total switching losses can be calculated :

$$P_{sw} = P_{on} + P_{off}$$

$$P_{on} = P_{Vt} + P_{Ct}$$

$$= \frac{V_{BUS} \cdot I_{DS} \cdot f_{sw} \cdot R_{G_{on}}}{2} \cdot \left(\frac{Q_{GD}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}}{V_{DR} - \left(\frac{V_{pl} + V_{th}}{2} \right)} \right)$$

$$\begin{aligned} P_{off} &= P_{Vt} + P_{Ct} \\ &= \frac{V_{BUS} \cdot I_{DS} \cdot f_{sw} \cdot R_{G_{off}}}{2} \cdot \left(\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS2}}{\frac{V_{pl} + V_{th}}{2}} \right) \end{aligned}$$



Figures 4.23: Device capacitances as a function of drain-to-source voltage

4.11 Output Capacitance C_{OSS} Losses

The $C_{OSS}(v_{DS})$ function can be captured from the graph typically provided in the datasheet for the part being analyzed. The graph from the datasheet is reproduced in *Figure 4.23*. As an example, self-commutation transitions have zero P_{OSS} losses, however only if the load current is sufficient to completely charge C_{OSS} to V_{dd} or discharge to zero, and if the time to finish the self-commutation transition is longer than the current transition time of the device itself [12].

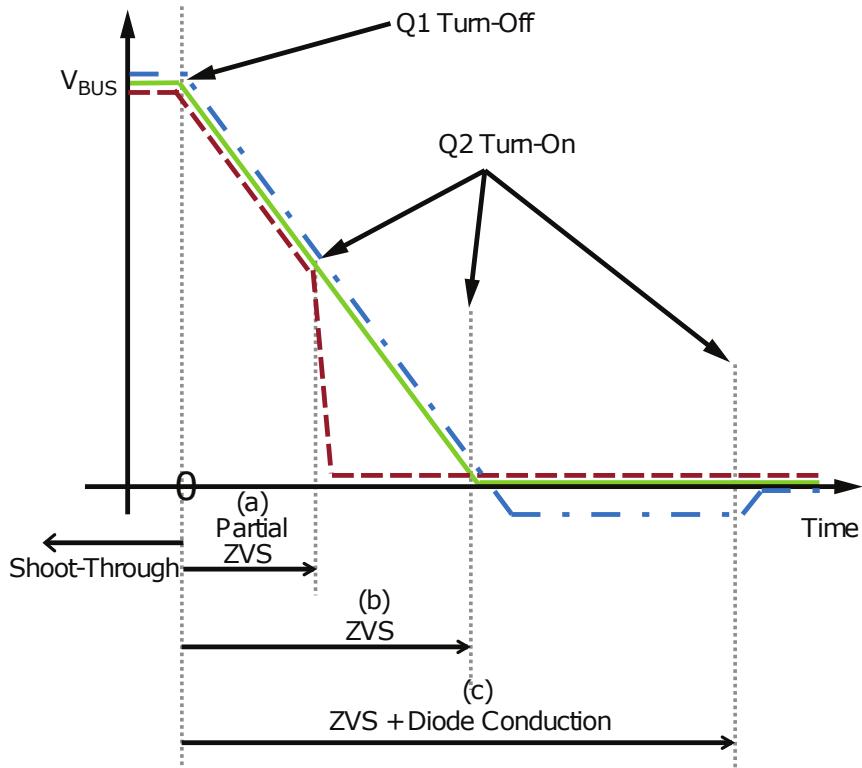
$$P_{OSS} = f_{sw} \cdot E_{OSS}$$

$$= f_{sw} \cdot \int_0^{V_{BUS}} v_{DS} \cdot C_{OSS}(v_{DS}) dv_{DS}$$

4.12 Gate Charge Q_G Losses:

The gate power losses are an important factor at higher frequencies and at lower output power levels. It is important to note that all the gate energy is absorbed during the charging phase, half of which is consumed, and during the discharge phase the remaining half of the energy is consumed [12].

$$P_G = Q_G \cdot V_{DR} \cdot f_{sw}$$



Figures 4.24: Switch-node voltage commutation with the same load current for various dead-times: (a) partial ZVS, (b) ZVS, and (c) ZVS plus diode conduction

4.13 Reverse Conduction Losses P_{SD} :

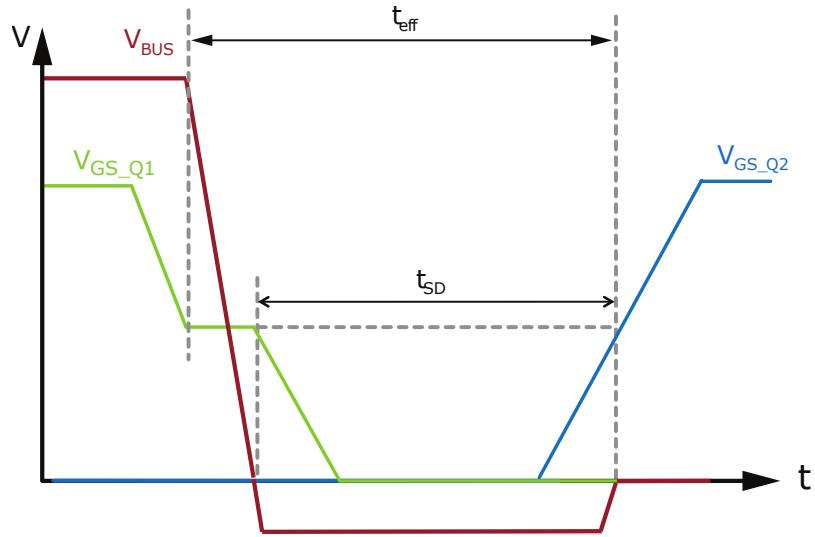
Reverse or diode conduction occurs when the current in the device turning on goes among the body diode before the switch conducts the current, and is a consequence of dead-time between when one device turns off and the next device turns on. Reverse conduction pursues a self-commutation transition and will only occur if the timing between the transitions is longer than needed to establish zero-voltage switching (ZVS) [12].

$$P_{SD} = V_{SD} \cdot I_{DS} \cdot t_{SD} \cdot f_{sw}$$

The reverse conduction time t_{SD} needs to be determined from the operating conditions as it is dependent on load current, supply voltage and device parameters. To perform this, a definition of effective dead-time is needed.

$$Q_{OSS} = \int_0^{V_{BUS}} C_{OSS(v_{DS})} dv_{DS}$$

$$t_{ZVS} = \frac{Q_{OSS_Q_1} + Q_{OSS_Q_2}}{I_{Turn-off}}$$



Figures 4.25: Effective dead-time definition for turn-on

$$t_{SD} = t_{eff} - t_{ZVS}$$

$$V_{PZVS} = \frac{I_{Turn-off}.t_{eff}.V_{BUS}}{Q_{OSS_Q_1} + Q_{OSS_Q_2}}$$

4.14 Total Hard-Switching Losses

$$P_{DYN} = (P_{SW} + P_{OSS} + P_G + P_{SD} + P_{RR})$$

Calculating all the aforementioned losses for this project, we reach 23.5 W per MOSFET in addition to ohmic losses of the MOSFET due to the $R_{DS_{ON}}$.

4.15 Heat Dissipation:

The best choice for power electronic supplies, is using a heat-sink without a fan, which is known as passive-cooling. Since, the duty cycle of the output power is limited, we can consider even a small heat-sink for this power amplifier.

As has been calculated in the previous section, the power dissipation of every MOSFET is about 23.5 W and if we consider one heat-sink for both MOSFETS in the leg, we need to consider 47 W power dissipation.

The proposed GaN MOSFET GS61008T has two package versions, one which is cooled from the bottom side and other one which cool down from the top side. Since an FR4 PCB instead of Aluminum PCB is used in this project, it is recommended to use the package, which cool down from top side, and a separated heat-sink will be used which can be installed on the MOSFETs.

If we refer to the datasheet of the *GS61008T*, two ways of heat dissipation are considered, *one* is from junction to upper copper-pad, which is designed as a heat exhaust with low thermal resistivity $R_{\theta jc} = 0.55 \frac{K}{W}$. The *second* is from junction to lower copper-pin-pad, which is not designed for heat exhaust, however, according to the datasheet, it is recommended to design fairly big tracks $R_{\theta jc} = 5.5 \frac{K}{W}$

According to the datasheet of the MOSFET, the maximum operating temperature of the MOSFET is $150^{\circ}C$. In the best case, and not worst case, we can consider the ambient temperature to be $25^{\circ}C$. The higher the junction temperature, the more the life time as well as the efficiency of the converter will be reduced. Therefore, a maximum junction temperature of $100^{\circ}C$ will be considered in the heat-sink calculations

$$R_{\theta IM} = 1.49 \frac{K}{W} \quad \text{good heat-conductive material(silicon filler)}$$

$$R_{\theta jc} = 0.55 \frac{K}{W}$$

$$R_{\theta hsA} = \text{To be Calculated}$$

$$(0.55 + R_{\theta hsA} + 1.49) * 47 \leq 100^{\circ}$$

$$\Rightarrow R_{\theta hsA} \leq 0.09 \frac{K}{W}$$

4.16 The Necessity of Line Filter

A line filter is a kind of electronic filter, that is placed between a part of electronic equipment and a line external to it, to attenuate conducted radio frequencies signals known as EMI (electromagnetic interference). On the input current which drains from the source, low frequency components plus the high frequency components are present. The main function of the line filter is mitigation of this high frequency component by limiting them to be below a certain threshold, which is described in different directives. The bandwidth of the wave-shape for this high-frequency component is limited from 150 kHz to 30 MHz

4.17 Type of High Frequency Emitted Components

The high-frequency components are divided into two sub categories:

- 1. Differential Mode Conducted Emission:** This type of noise, is the noise which can be found on both input wires with positive and negative sign, with the same amplitude. The source of this noise is switching element of the circuit and this type of the noise should be kept in a allowed range. The mitigation of this type of noise is implementable using an L-C filter.

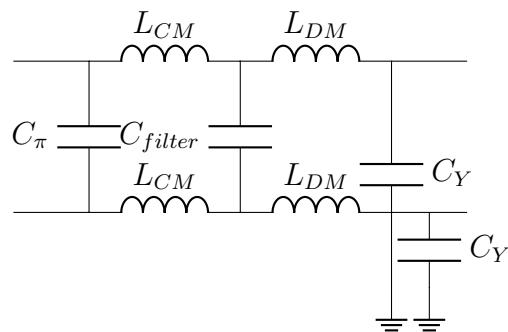
2. **Common Mode Conducted Emission:** This type of the noise, is the noise which can be found on only either one wire(Line) and earth or two wires(Line and Null) and earth. The direction of current can be different and it can be dealt with by using an inductance which can stop this noise from entering to the circuit.

4.18 Line Impedance Stabilization Network (LISN)

A LISN is a low-pass filter typically placed between an AC or DC power source and the EUT (equipment under test) to create a known impedance and to provide an RF noise measurement port. It also isolates the unwanted RF signals from the power source. In addition, LISNs can be used to predict conducted emission for diagnostic and pre-compliance testing. LISN is used to measure the generated *Differential Mode Conducted Emission* of a circuit with the help of a spectrum-analyzer. According to this measurement, the design of input filter could be much easier and the required attenuation on different bandwidth can be witnessed [26].

4.19 Proposed Filter

For the input stage of the power amplifier, the circuit in *Figure 4.26* is a stereotype of a line filter. It is a commonly design for AC input lines. However, it is also suited for DC-fed power supplies. For the line filter, because of the asymmetrical essence of the noises, it is recommended to have a symmetrical circuit to influence noises in any directions.

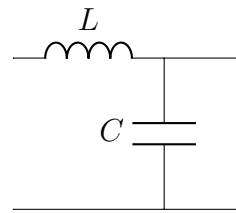


Figures 4.26: Proposed line filter

4.20 Design Steps

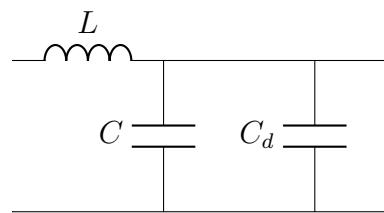
4.20.1 Differential Mode Conducted Emission Filter

As previously mentioned, the differential mode conducted emission is originated from the switching components of the circuit. The origin for this type of emission is the power supply and its load, so in this project it is a *Class AB amplifier 300 MHz* in addition to the *5 MHz of the switching frequency*. For this case, due to the ease of use and lower cost, a simple L-C filter is recommended (*Figure 4.27*).



Figures 4.27: DM filter

It is recommended, that the line filter is symmetrical. Therefore, the inductance should be divided into two $\frac{1}{2}L$. Moreover, the L-C low pass filter has a characteristic on a small bandwidth around the cut-off frequency, where according to the Q-factor of a filter, the output voltage is increased. In order to mitigate this phenomenon, the best solution is adding a resistance to this circuit. Adding a resistance means putting a zero into a transfer function, which decreases the efficiency of the filter. Another solution is adding a capacitance with high ESR, with a capacitance value 5 times bigger than the capacitance of the filter (*Figure 4.28*).

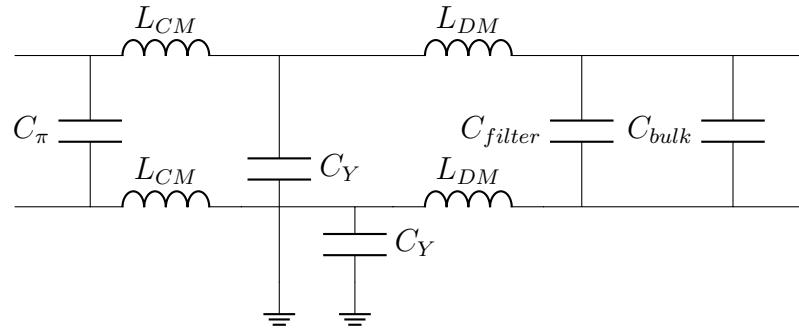


Figures 4.28: CM filter with additional zero

As a rule of thumb, we want to have -80 dB attenuation at the switching frequency 5 MHz . This means that the cut-off frequency of this filter should be 50 kHz .

4.20.2 Common Mode Conducted Emission Filter

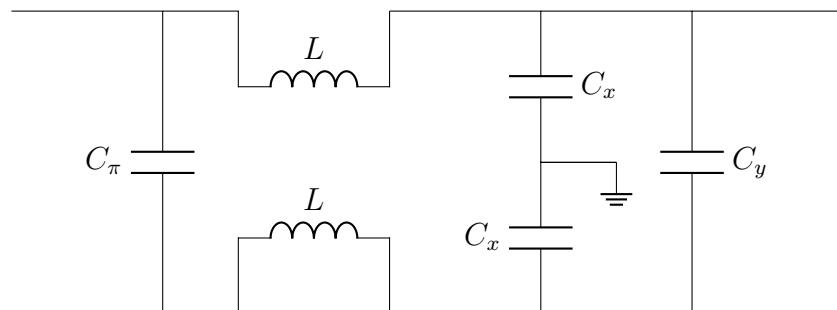
Normally, the common mode conducted emission filter consists of one common mode choke and two similar capacitors connected to ground (*Figure 4.29*).



Figures 4.29: CM with DM line filter

4.20.3 EMI and EMC Filter

To save cost, we can combine the differential mode inductance and common mode inductance into one common mode choke. The leakage inductance of the choke, represent the L_{DM} and normal inductance of every line represent the L_{CM} (*Figure 4.30*).



Figures 4.30: Typical line filter

In common mode noise, when either two currents enter the dot lines of the line-filter in same way or just one current flows into the line filter, the constructed flux on the core of the choke intensify each other, therefore, a big inductance is witnessed by both currents. This means that *for the common mode noise the common mode choke behaves like a big inductance*. In differential mode noise, since the currents are inverse and have the same magnitude, the generated flux on the core of the choke will be canceled out, however the leakage inductance will be observed by these differential mode noise currents.

4.21 EMI Filter and Stability according to Dr. Middlebrook Criterion

Adding an EMI/EMC filter to the input section of a power supply can have the adverse effect, that the stability of the system can be influenced by the poles and zeros of the filter. As a rule of thumb, the input impedance of the power section Z_{in} should be much higher than the output impedance Z_{out} of the filter [27].

$$Z_{out} \ll Z_{in}$$

$$\begin{aligned} Z_{in} &= \sqrt{\frac{L}{C}} \\ Z_{out} &= \frac{V_{in}^2 \cdot \eta}{P_{out}} \\ f_{cut-off} &= \frac{1}{2\pi\sqrt{LC}} \end{aligned}$$

As rule of thumb, we select factor 10 for the difference in magnitude of Z_{in} and Z_{out} .

$$Z_{out} = \frac{1}{10} Z_{in}$$

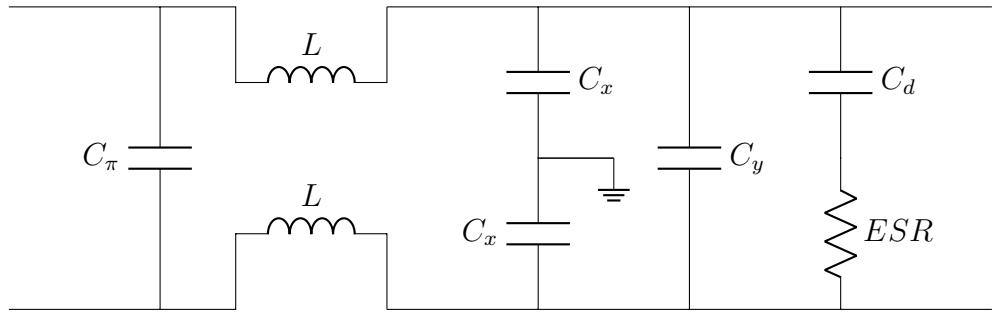
4.22 How to select π – Capacitor:

C_π capacitor forms an additional attenuation (low-pass filter) with the line impedance (approximately 100 μH) and is useful for the differently conducted emission noise. Three conditions should be met for the value of this capacitance [28]:

1. $C_\pi < \frac{C_y}{5}$
2. $C_\pi \gg \frac{1}{(L_{source} \| L_1)(\pi F_s)^2}$ OR $C_\pi \ll \frac{1}{(L_{source} \| L_1)(4\pi F_s)^2}$
3. $C_\pi > \frac{1}{10\pi F_s}$

4.23 Design Procedure:

The general EMI/EMC filter for our switching supply is shown in *Figure 4.31*:



Figures 4.31: Proposed line filter

4.23.1 Use Case 1: Line Filter for CDPA:

In the first step, we concentrate on the switching frequency of the SMPS, and as rule of thumb, we try to have 80 dB attenuation at this switching frequency. Since, we have a two poles low-pass filter, we have:

$$-80 \text{ db} \rightarrow 5 \text{ MHz} \Rightarrow f_{cutt-off} = 50 \text{ kHz}$$

For the Dr. Middlebrook criteria, we should calculate the input impedance of the converter. By a good estimation we can say [27]:

$$Z_{in} = \frac{V_{in}^2 * \eta}{P_{out}}$$

For this criterion, the minimal Z_{in} should be calculated. This minimum is reached for maximum P_{out} and minimum permitted V_{in} .

$$\min(V_{in}) = 50 \text{ V}$$

$$\max(P_{out}) = 1 \text{ kW}$$

$$\eta = 70\%$$

$$\Rightarrow Z_{in,min} = 1.75 \Omega$$

According to the criteria of Middlebrook, we should have $Z_{out} \ll Z_{in}$, [27]

$$Z_{out} = \frac{1}{10} * 1.75 = 0.175 \Omega$$

At this moment, we have two constraints; firstly the *output impedance of the filter* Z_{out} and secondly the *cut-off frequency of the filter*.

$$Z_{out} \leq 0.175 \Omega \Rightarrow \sqrt{\frac{L}{C}} \leq 0.175 \Omega$$

$$f_{cutt-off} = 50 \text{ kHz} \Rightarrow \frac{1}{2\pi\sqrt{LC}} = 50 \text{ kHz}$$

For finding the C_{min} we multiply the two upper equations, then we find the C_{min} .

$$C_{min} = \frac{1}{2\pi * 0.175 * 50^3} \approx 18 \text{ uF}$$

Usually $C_{max} = 100 \text{ uF}$ is considered, due to the DC bias points of these capacitors.

$$C_{max} = 100 \text{ uF}$$

Corresponding inductance for every value of C is:

$$C_{min} = 18 \text{ uF} \Rightarrow L_{max} = 0.56 \text{ uH}$$

$$C_{max} = 100 \text{ uF} \Rightarrow L_{min} = 0.10 \text{ uH}$$

To mitigate the spikes at the resonance frequency about 5 kHz inserting a bigger capacitor with a high ESR is recommended. The ESR of the capacitor dampen the spikes and with inserting a pole, the side-effect of the zero from the ESR is compensated. The best choice is to select the Q-factor as 1:

$$Q = \frac{1}{ESR} \sqrt{\frac{L}{C}}$$

$$\Rightarrow ESR = \sqrt{\frac{L}{C}}$$

We select the inductance and capacitance of the filter as below:

$$C_1 = 20 \text{ uF} \Rightarrow L_1 = 560 \text{ nH}$$

Iterate: Therefore we should look for a line-filter which can withstand 20 A with the leakage inductance of 560 nH (*See the begining of this chapter*). If we go to the product list of the *Pulse Electronics (Yageo, Taiwan)*, the minimum leakage inductance that we can find is 700 nH. So we choose the **PA5140.105NL** common mode choke and the common mode inductance of 140 uH. In total we have:

$$L_{leakage} = 700 \text{ nH} \& C_y = 20 \text{ uF}$$

$$C_d = 100 \text{ uF} \& ESR = 187 \text{ m}\Omega$$

Now that we know the value of the common mode impedance $L_{CM} = 140 \text{ uH}$, we can simply calculate the value of C_x according to the cut-off frequency of 50 kHz. this leads to:

$$C_x = 72 \text{ nF} \approx 47 \text{ nF} + 22 \text{ nF}$$

It should be noted, that in this project the return current of the RF path, go to the return path of the circuit using these capacitors. Special control on this return path can be implemented according to the necessities.

Only C_π remains to be calculated. As we have already calculated L1 is $L_{leakage} = 700 \text{ nH}$ and $L_{leakage} \parallel L_{source} \approx 700 \text{ nH}$

1. $C_\pi < \frac{20\mu F}{5} = 4 \mu F$
2. $C_\pi \gg \frac{1}{(L_{source}\|L_1)(\pi F_s)^2} = 5.789 \text{ nF OR } C_\pi \ll \frac{1}{(L_{source}\|L_1)(4\pi F_s)^2} = 361.861 \text{ pF}$
3. $C_\pi > \frac{1}{10\pi F_s} = \frac{1}{10\pi 5*10^6} = 6.366 \text{ nF}$

Therefore we select $C_\pi = 47 \text{ nF}$.

4.23.2 Use Case 2: Line Filter for Auxiliary Power Supply:

In the first step, we concentrate on the switching frequency of the SMPS. As a rule of thumb, we try to have 80dB attenuation at this switching frequency. Since we have a two poles low-pass filter, we can calculate:

$$-80 \text{ dB} \rightarrow 300 \text{ kHz} \Rightarrow f_{cut-off} = 3 \text{ kHz}$$

For the Dr. Middlebrook criteria, we should calculate the input impedance of the converter. By a good estimation we can say: [27]

$$Z_{in} = \frac{V_{in}^2 * \eta}{P_{out}}$$

For this criterion, the minimal Z_{in} should be calculated. This minimum occurs at maximum P_{out} and minimum permitted V_{in} .

$$\min(V_{in}) = 50 \text{ V}$$

$$\max(P_{out}) = 30 \text{ W}$$

$$\eta = 70\%$$

$$\Rightarrow Z_{in,min} = 58.33 \Omega$$

According to the criteria of Middlebrook, we should have $Z_{out} \ll Z_{in}$ [27]

$$Z_{out} = \frac{1}{10} * 58.33 = 5.833 \Omega$$

At this moment, we have two constraints; firstly the *output impedance of the filter* Z_{out} and secondly the *cut-off frequency of the filter*.

$$Z_{out} \leq 5.833 \Omega \Rightarrow \sqrt{\frac{L}{C}} \leq 5.833 \Omega$$

$$f_{cut-off} = 3 \text{ kHz} \Rightarrow \frac{1}{2\pi\sqrt{LC}} = 3 \text{ kHz}$$

For finding the C_{min} we multiply the two upper equations, then we find the C_{min} .

$$C_{min} = \frac{1}{2\pi * 5.833 * 3000} \approx 9 \text{ } uF$$

Commonly $C_{max} = 100 \text{ } uF$ is used, due to the DC bias points of these capacitors.

$$C_{max} = 100 \text{ } uF$$

The corresponding inductance for each value of C is:

$$C_{min} = 9 \text{ } uF \Rightarrow L_{max} = 312.72 \text{ } uH$$

$$C_{max} = 100 \text{ } uF \Rightarrow L_{min} = 28 \text{ } uH$$

To mitigate the spikes at the resonance frequency around 3 kHz inserting a bigger capacitor with a high ESR is recommended. The ESR of the capacitor dampens the spikes and with inserting a pole, the side-effect of the zero from the ESR is compensated. The best approach is selecting the Q-factor as 1:

$$Q = \frac{1}{ESR} \sqrt{\frac{L}{C}}$$

$$\Rightarrow ESR = \sqrt{\frac{L}{C}}$$

We select the inductance and capacitance of the filter as below:

$$C_1 = 20 \text{ } uF \Rightarrow L_1 = 140 \text{ } uH$$

Iterate: Therefore we should look after a line-filter which can stand approximately 1 A with the leakage inductance of $140 \text{ } uH$. If we go to the product list of *Coilcraft (Coilcraft Inc., IL, USA)*, we find the most appropriate leakage inductance in the part **CMT1-8.0-1L** with the values of $125 \text{ } uH$ and the common mode inductance is 8 mH . In total we have:

$$L_{leakage} = 125 \text{ } uH \text{ & } C_y = 22.5 \text{ } uF$$

$$C_d = 112.5 \text{ } uF \text{ & } ESR = 2.356 \text{ } \Omega$$

Now we know the value of the common mode impedance $L_{CM} = 8 \text{ mH}$, therefore we can simply calculate the value of C_x according to the cut-off frequency of 3 kHz , which leads us to:

$$C_x = 703.62 \text{ } nF \approx 680 \text{ } nF + 22 \text{ } nF$$

It should be noted that in this project the return current of the RF path, go to the return path of the circuit using these capacitors. Special control on this return path can be implemented according to the necessities.

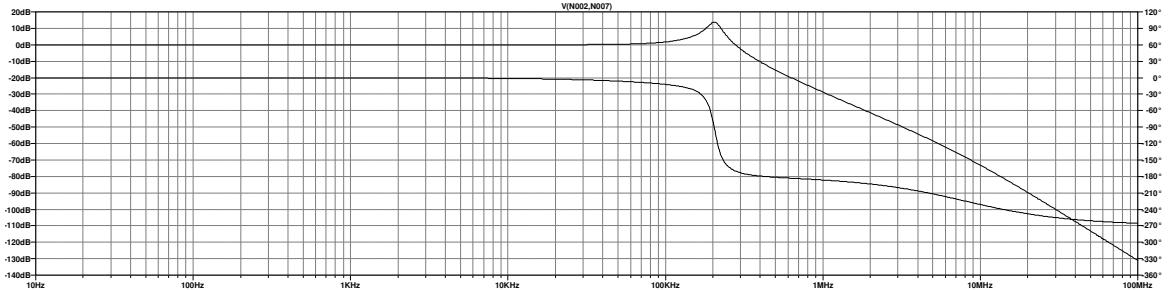
Only C_π remains to be calculated. As we calculated L1 is $L_{leakage} = 125 \text{ } uH$ and $L_{leakage} \parallel L_{source} \approx 55 \text{ } uH$

1. $C_{\pi} < \frac{22.5 \text{ } \mu\text{F}}{5} = 4.5 \text{ } \mu\text{F}$
2. $C_{\pi} \gg \frac{1}{(L_{source} \| L_1)(\pi F_s)^2} = 20.469 \text{ } n\text{F}$ OR $C_{\pi} \ll \frac{1}{(L_{source} \| L_1)(4\pi F_s)^2} = 1.279 \text{ } n\text{F}$
3. $C_{\pi} > \frac{1}{10\pi F_s} = \frac{1}{10\pi 300*10^6} = 106.10 \text{ } n\text{F}$

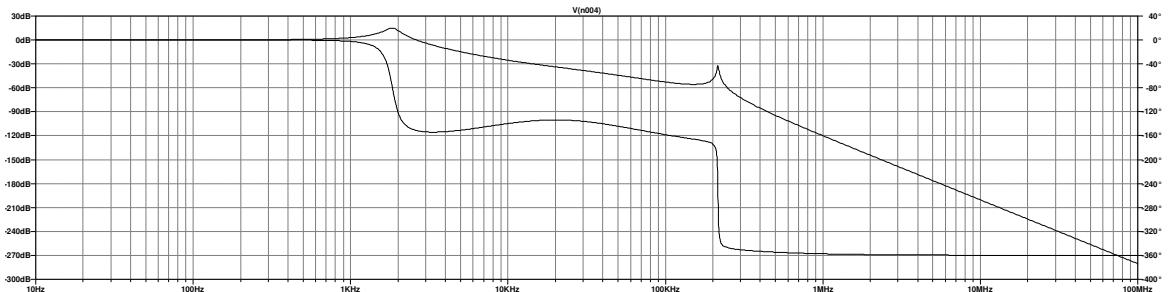
Therefore we select $C_{\pi} = 47 \text{ } n\text{F}$.

4.24 Simulation

To simulate the circuit it was implemented in *LTS spice* and an AC analysis was used to find out the characteristic of the filter in both ways, firstly from input to output and then vice versa. For both cases the results show that the attenuation of the filter at 5 MHz is less than 80 dB, as per requirement, in both ways. It should be noted, that only the differential mode signal has been inspected [29].



Figures 4.32: Internal; the noise source is in the SMPS and the output signal is at the supply line



Figures 4.33: External; the noise source is in the power line input, and the output signal is at the input of the power supply

4.25 Computer Simulation of Power Conversion Systems

There are fundamentally two main ways for modeling the converters, which are working in switch-mode: *1-Average-Modeling* and *2-Cycle-by-Cycle*. Each of which has advantages and disadvantages, however for the steady-state behavior, we use average modeling and for the transient-state, we use cycle-by-cycle modeling. The detailed information from this chapter has been extracted from the article of Dr. Sam Ben-Yaakov [30].

4.26 Average-Modeling of Converters

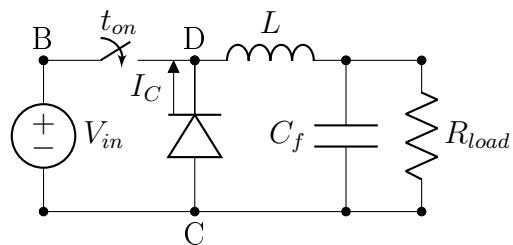
The emphasis in the average-modeling is on the two main points:

1. Small and large signal responses
2. Control loop design

Applications of the average-modeling are DC transfer functions, transient of large signal in time domain, and also the small signal transfer function. Nevertheless, this modeling is not applicable to the switching details, such as rise and fall times and spikes, moreover, the device characteristics, losses and sub-harmonic oscillations are meaningless for this type of modeling.

The strategy for average-modeling of a converter is modeling the inductor in switching way, which is known as *Switched Inductor Model (SIM)*. First of all we should identify the switching mechanism of the converter, and then replace it by an analog (continuous) equivalent circuit. If we use the analog counterpart of the switching-inductor mechanism, the simulation of the converter will be fast and easy, and even the control rule can be easily imposed to the converter.

Class-D amplifier is in fact a synchronous buck converter, therefore, we can use the proposed model of the buck converter for this type of converter (See *Figure 4.34*).

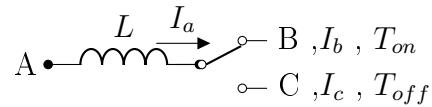


Figures 4.34: Buck converter



Figures 4.35: Modeling the switching element in a buck converter

As a simplified model for the buck converter, *Figure 4.35* can be proposed; left side is the converter and right side is the model. In this model the inductor conducts three types of current, firstly, the increasing current, when the switch is on, secondly, the decreasing current, when the switch is off, and lastly, the state when the switch is off, but there is no current to conduct. This state happens in the discontinuous conduction mode (DCM) of operation, which depends on the load.

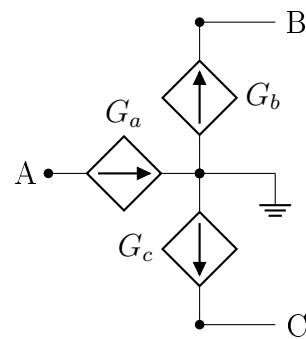


Figures 4.36: Proposed model for a switching element in a buck converter

We can simply write the average current below, instead of the instantaneous current:

$$\bar{I}_b = \bar{I}_L \cdot D_{ON}$$

$$\bar{I}_c = \bar{I}_L \cdot D_{OFF}$$



Figures 4.37: Proposed model for switching element in a buck converter, using CCS

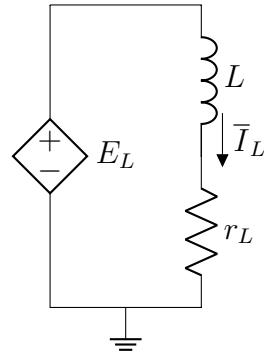
$$G_a \equiv \bar{I}_L$$

$$G_b \equiv \bar{I}_L \cdot D_{ON}$$

$$G_c \equiv \bar{I}_L \cdot D_{OFF}$$

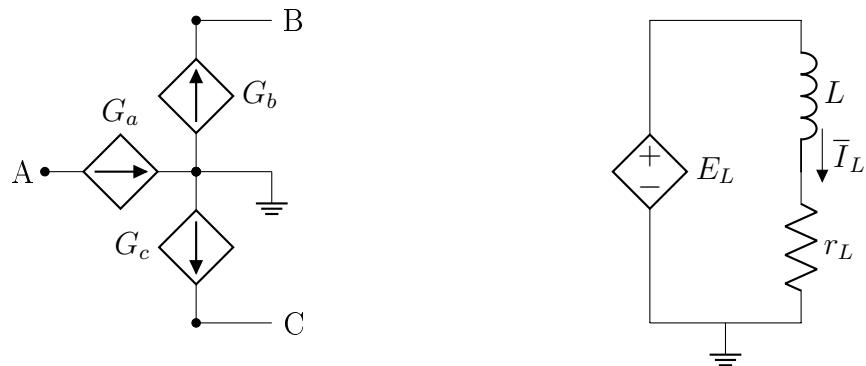
On other side, we can also write the following expression

$$\bar{V}_L = V_{(a,b)} \cdot D_{ON} + V_{(a,c)} \cdot D_{OFF}$$



Figures 4.38: Proposed model for inductance and output in buck converter, using VCS

therefore, the model in *Figure 4.41* can be used for average-modeling:



Figures 4.39: Average-modeling of buck converter, using CCs and VCS

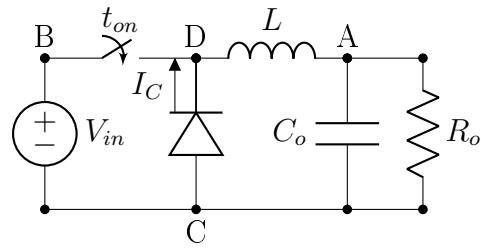
$$G_a = I(L)$$

$$G_b = I(L) \cdot D_{ON}$$

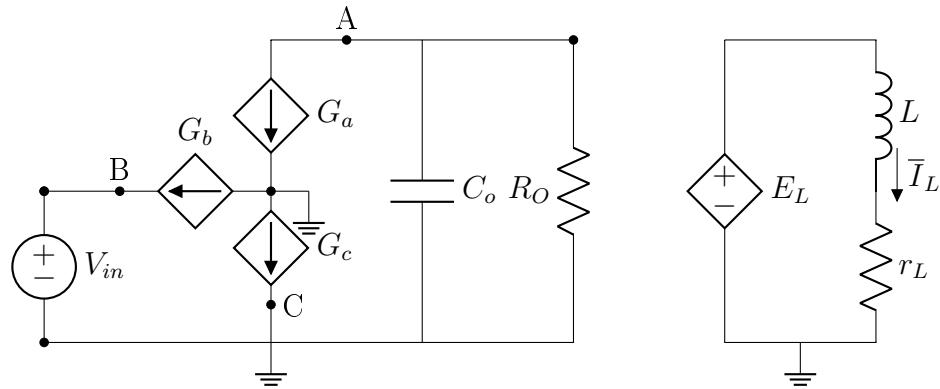
$$G_c = I(L) \cdot D_{OFF}$$

$$E_L = [V_o - V_{in}] \cdot D_{ON} + [V_o - 0] \cdot D_{OFF}$$

By imposing the model to the buck converter we obtain the approach below:



Figures 4.40: Buck converter



Figures 4.41: Average-modeling of buck converter, using CCs and VCS

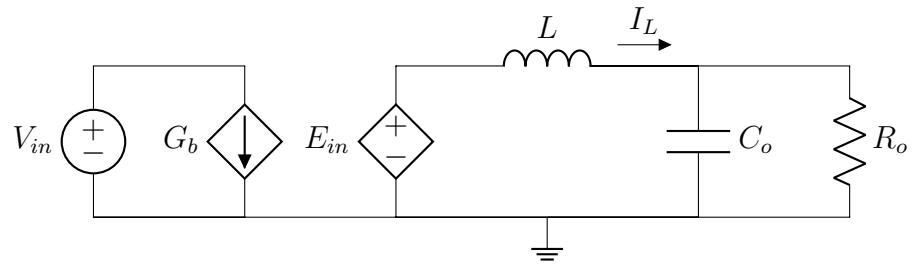
$$G_a = I(L)$$

$$G_b = I(L) \cdot D_{ON}$$

$$G_c = I(L) \cdot D_{OFF}$$

$$E_L = [V_o - V_{in}] \cdot D_{ON} + [V_o - 0] \cdot D_{OFF}$$

After some simplification, we will obtain the following model:

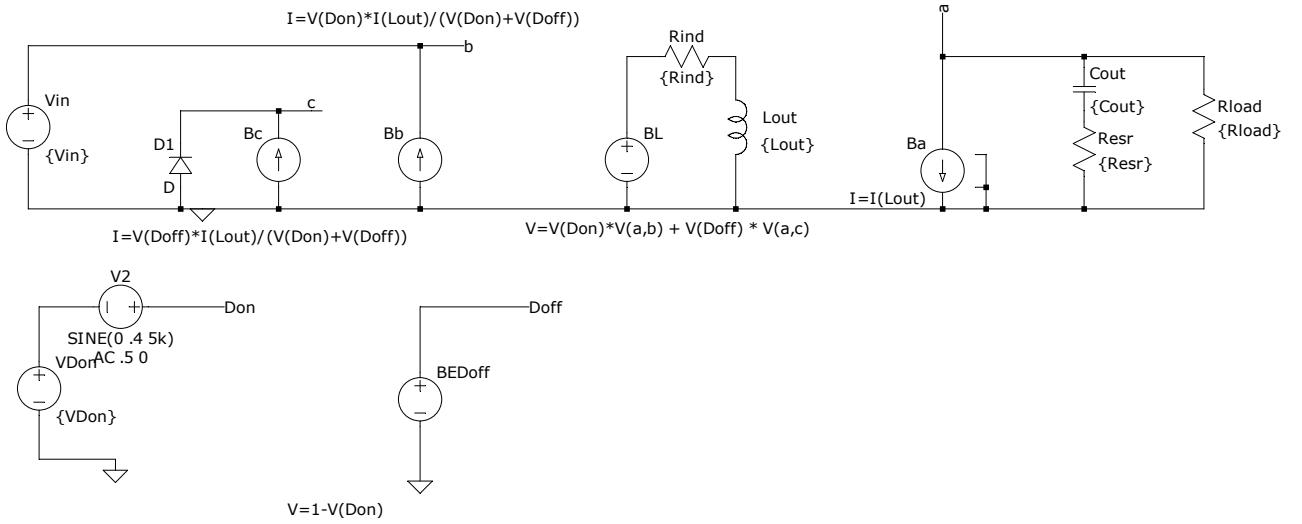


Figures 4.42: Average-modeling of buck converter, simplified

$$E_{in} = V_{in} \cdot D_{ON}$$

$$G_b = \bar{I}_L \cdot D_{ON}$$

$$E_{in} + V_o \rightarrow \bar{V}_L$$



Figures 4.43: Implemented Model in LTSPICE

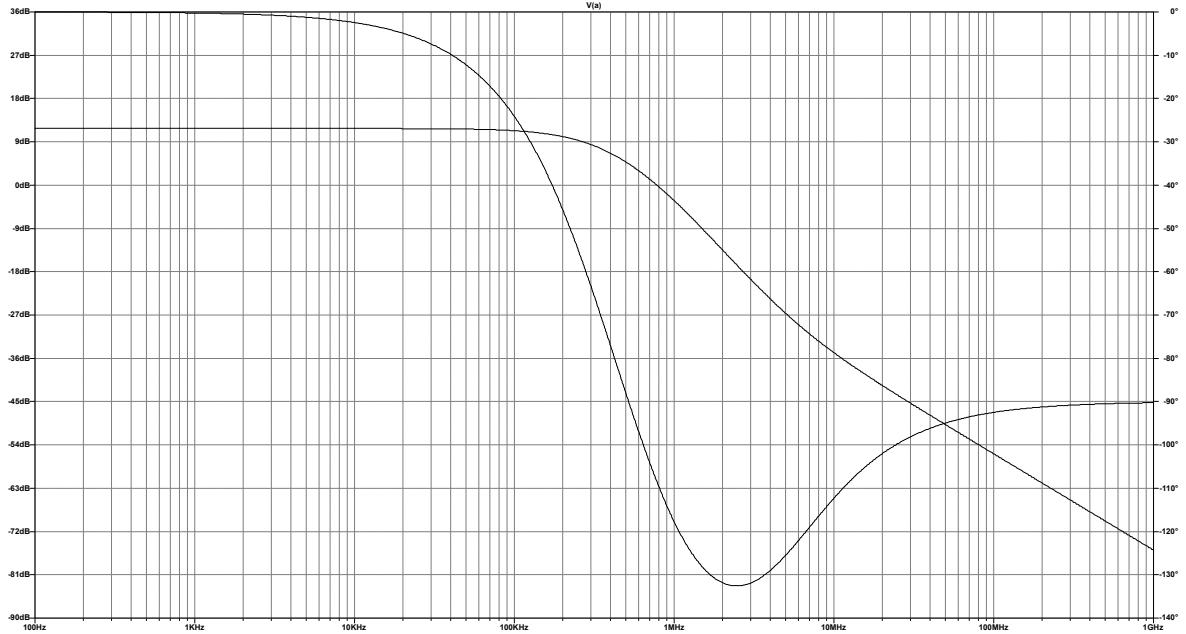
4.27 Implementation in PSpice

The above model, can be simply implemented by LTSPICE. LTSPICE does the linearization automatically. With this model, different types of simulation can be done. First of all, we obtain the bode diagram of the converter with the help of the *AC analysis*. In the *Figure 4.44*, the bode plot of $\frac{V_{out}}{V_{in}}$ is illustrated. From the DC frequency till about 500 kHz the gain is almost constant. After the cut-off frequency, due to the nature of second-order filter, the gain starts to drop with the slope of $-40 \frac{dB}{dec}$. However, due to the existence of the *ESR* of the capacitance, one zero has been added to the transfer function of the converter, and this zero at a frequency of about 7 MHz , changes the slope from $-40 \frac{dB}{dec}$ to $-20 \frac{dB}{dec}$.

4.28 Proposing a Controller

In the control environment, there is a variety of methods to control a switch-mode power converter. Generally the switch-mode power converters are used in DC power supply, and all efforts have put on constantly keeping the output of the power supply in a predetermined range, as has already mentioned in the design requirements. For the AC power supply it is more challenging; since the larger the bandwidth, the more complicated the design. Two main modes of control are proposed for the switch-mode converters, each of which has some advantages and disadvantages [31].

1. Voltage mode control
2. Current mode control



Figures 4.44: Bode Plot of $\frac{V_{out}}{V_{in}}$

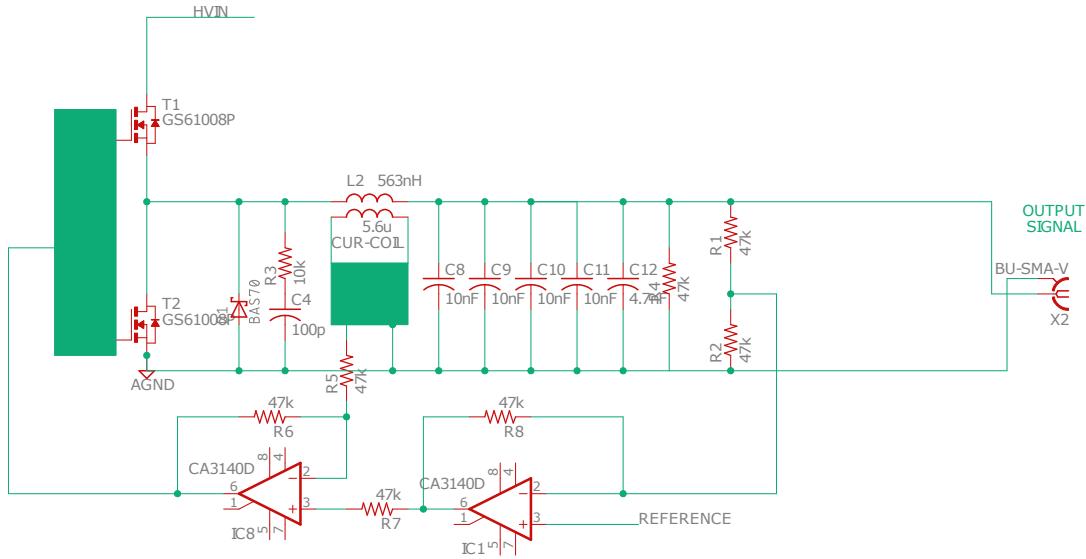
As previously mentioned, the *CDPA* which acts as a buck converter, behaves like a second order filter. Nonetheless, due to the ESR of the output capacitance of the filter, one zero is added to the transfer-function of the filter, which changes the slope of the gain from $-40 \frac{dB}{dec}$ to $-20 \frac{dB}{dec}$.

In this *CDPA*, we implement a tracking voltage amplifier, therefore the shape of the output is always the most important thing to maintain. Nevertheless, a current feedback can simply improve the stability and dynamics of a voltage regulator. Dual loop control essence makes an attractive design for controlling the instantaneous response of the converter. The most important reason for using current feedback is its ability of *short circuit protection*. Besides, voltage feedback suffers severely from the second-order transfer function of the converter. By using the current feedback, theoretically, the degree of the system would be decreased one order, and a second-order filter would act as first-order filter [31].

Current feedback come in different varieties, which the most important one is the *PCM* (*Peak Current Mode*) and *ACM* (*Average Current Mode*). These two methodologies have respective some pros and cons, however, due to the essence of the large bandwidth of this converter, it is preferred to use ACM, which acts more linearly than PCM.

4.28.1 Average Current Mode

In this method, there are two loops of control. One loop is the inner, and one is the outer loop. The outer loop is the voltage loop, which differentiates the output voltage of the converter with the reference. This reference for this CDPA is a small signal with



Figures 4.45: ACM current feedback

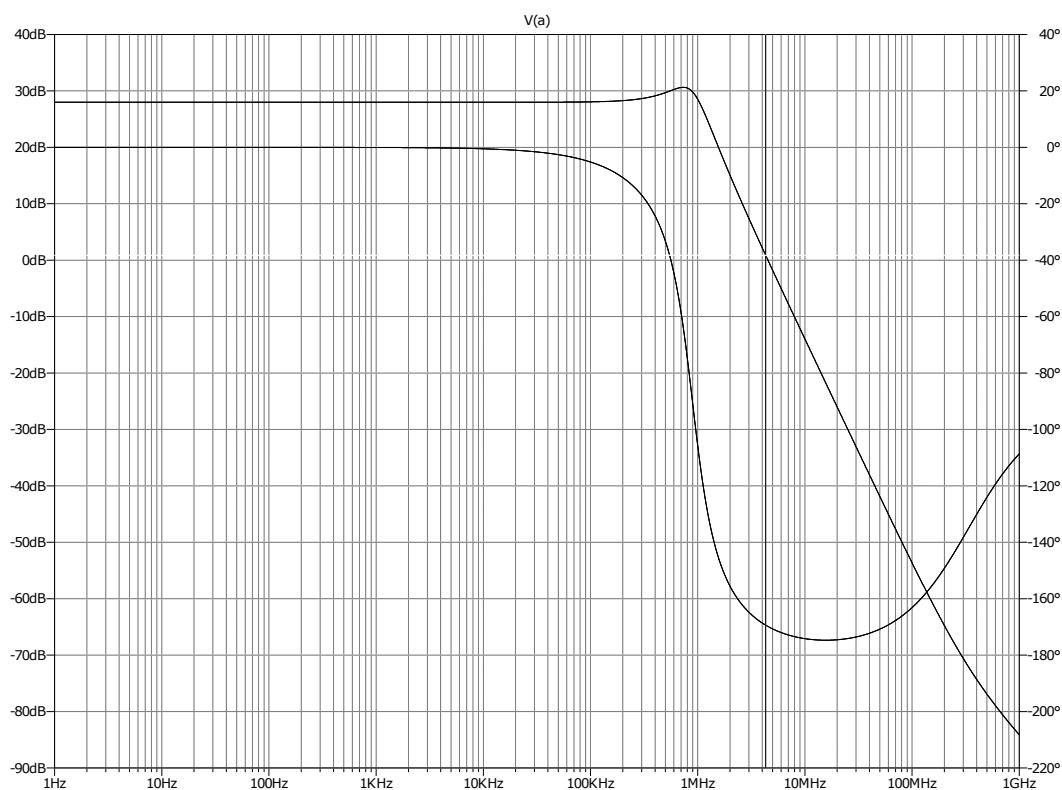
a bandwidth of 500 kHz. The output of this amplifier is an error voltage, which will be compared to the switch-mode current of the converter. This second error voltage will create the reference for the PWM converter, which generates the PWM pulses at the gate of the MOSFETs.

The operational mechanism of the current feedback in ACM is robust against failure, since the current of the amplifier is the main parameter to control the converter. Firstly, the output voltage of the converter will be compared to the reference voltage, the result, which is an error voltage, will be fed to another error amplifier. This error amplifier will change the current of the converter, till the output of the error amplifier would be zero.

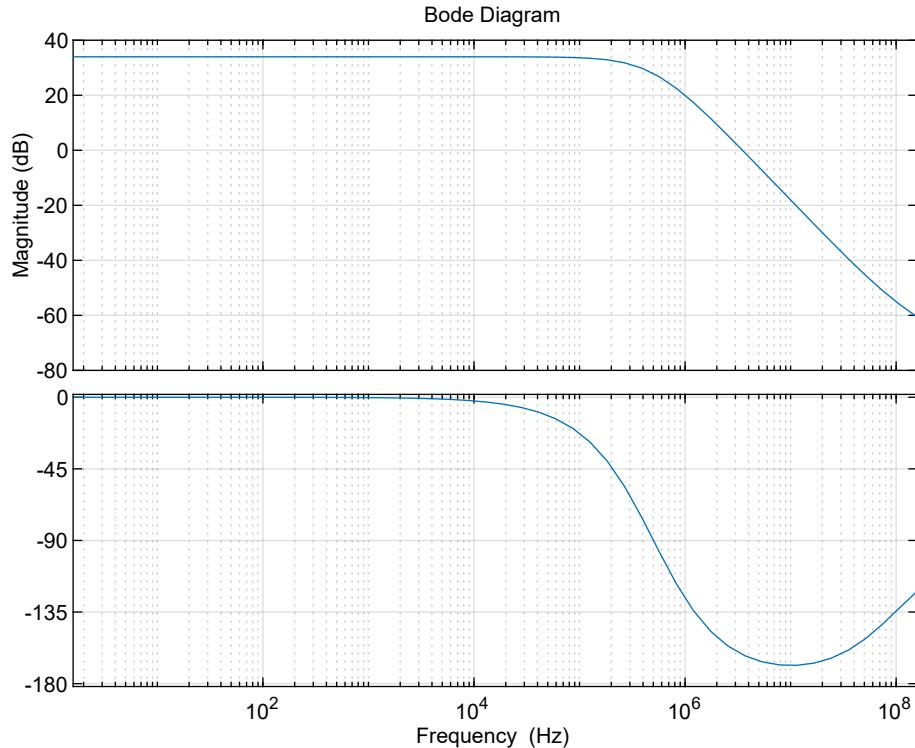
The output voltage of the converter, which is attenuated by a resistive voltage divider network, is the first input control variable in this control methodology. Nonetheless, the selection of the position for sensing the current of converter is a bit sensitive. Moreover, sensing a wide-bandwidth large amplitude-range current is not a simple task. A good choice for this current is the current of the inductance, since it contains the currents of high side and low side MOSFETS. This current will be rectified and amplified.

4.28.2 Voltage Mode Control

In voltage mode control, the reference is voltage and also the feedback loop is formed with only the output voltage of the converter. When considering bandwidth AC power amplifiers, there are many factors to be considered. The phase difference, as well as the ability of tracking the input reference is very important. Minimum distortion should be added to the output by the converter.



Figures 4.46: Open Loop converter; Bode Diagram



Figures 4.47: Modeling Open Loop converter; Bode Diagram

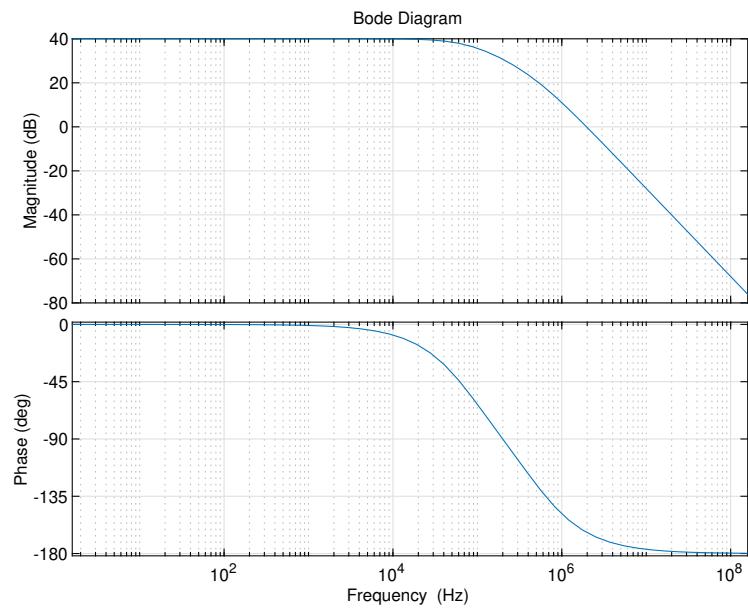
The phase margin as a criterion for the stability of the converter is about 10° , which is positive and shows that the system is stable, however for the reason of stability and to have a fixed voltage on the output of the amplifier, we use a combination of the voltage mode feedback and peak-current limiter. In order to reduce the ringing and overshoot on the output of the converter, as a rule of thumb, we will, with the aid of a feedback loop, increase the phase margin from 10° to more than 45° .

For improved simulation, according to the shape of the bode plot, we propose a transfer function in Matlab, *Figure 4.47*, with a single zero and double pole. With this modeled transfer function, we can simply propose a controller, and check the behavior of that, before implementing it into the average model of the circuit.

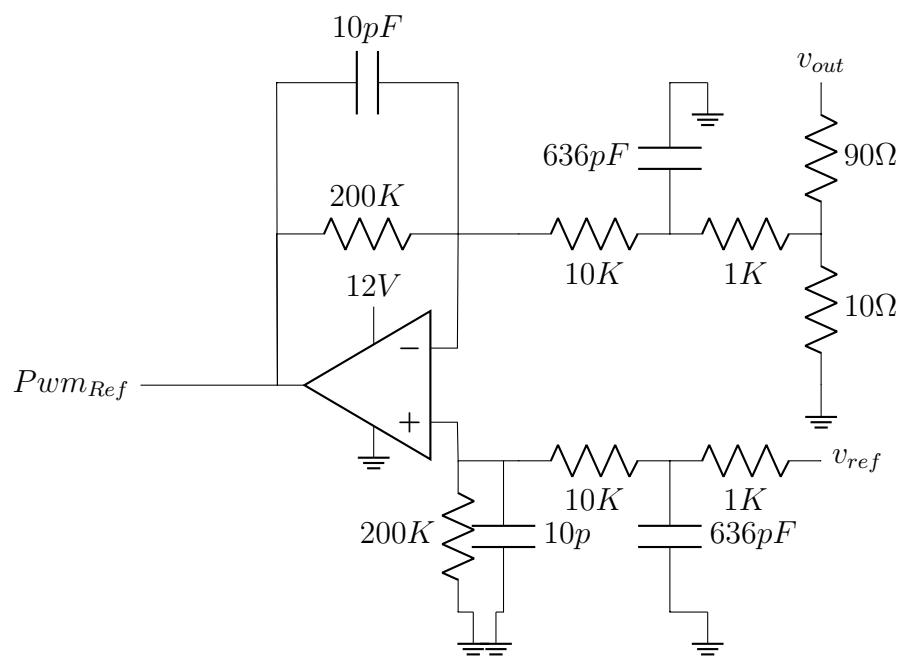
The proposed controller is shown in *Figure 4.49* and the bode plot of this controller can be seen in *Figure 4.48*. The proposed feedback compensator has two near poles, at about 500 kHz and 3 MHz .

Figure 4.50 shows that by using this controller, the bandwidth of the system has been increased and the also the phase margin of the system has been increased. The controller feedback does not change the phase of the output signal, such as feedback controller.

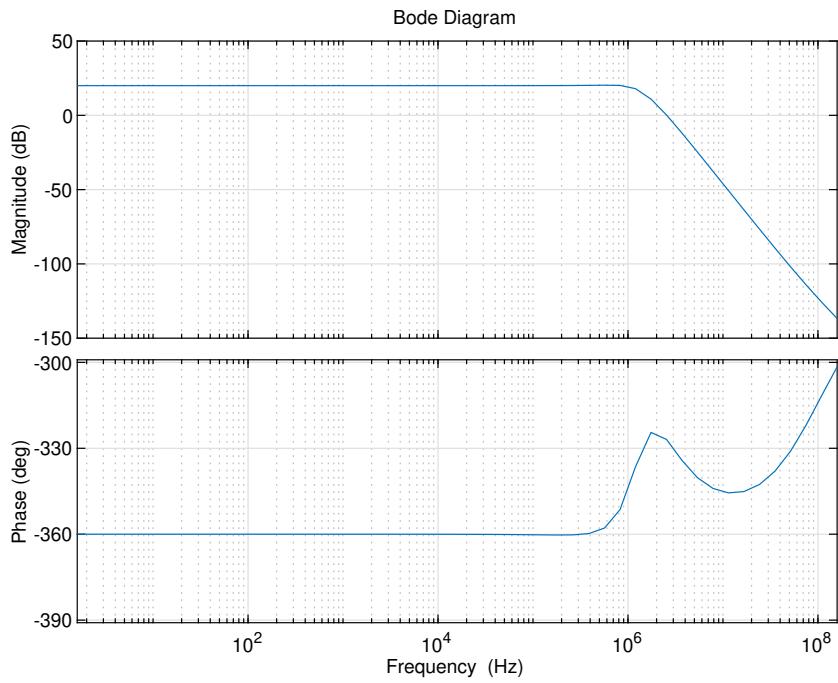
By simulating the controller using LTSpice, we obtain the results shown in *Figure 4.51*. As it could be estimated, the behavior of the system with the controller is similar to the proposed model in Matlab.



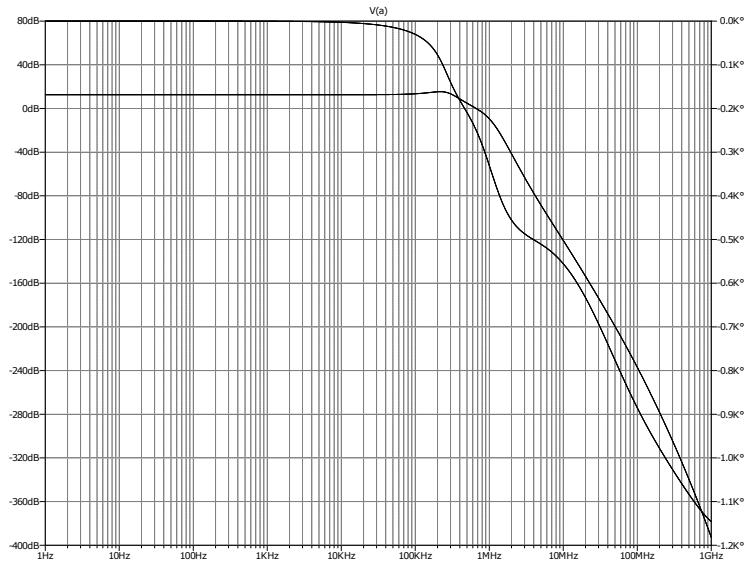
Figures 4.48: Proposed Controller; Bode Diagram



Figures 4.49: Proposed Controller; Schematic



Figures 4.50: Proposed Controller; Bode Diagram



Figures 4.51: Closed Loop System; AC Analysis

4.29 Layer Stack-up Assignment

The number of required routing layers and power planes are determined by functional specification, noise immunity (with the aid of power planes), signal category separation and number of nets. Proper use of microstrip and stripline is really important. The use of planes (supply and ground) embedded in the PCB is one of the most important methods of suppressing common-mode RF energy developed internally to the board. Each and every routing layer is adjacent to a reference(image) plane (power or ground). As a rule of thumb, the outer microstrip layer must contain only slower speed traces without periodic signals or high frequency clocks. It is recommended to put the high speed signal traces near to 0v planes [32].

4.30 Four-layer Stack-up

Four-layer stack-up can help to mitigate the radiated EMC. 4L stack-up can be realized in two different configurations :*1-Symmetrical* and *2-Asymmetrical*. The usage of reference planes enhances the ability for flux cancellation of RF current. Since the distance from a single layer to the reference plane is much less than double-side boards, the radiated RF-energy is reduced. A 4-layer assembly can still not be optimal for flux cancellation of RF currents, which is generated by circuits and traces, because the distance spacing between space trace and return path can still be excessively large. In symmetrical distance spacing, the layers are distributed equally along the PCB thickness. However, in asymmetrical configuration, the distance between the layers are not equal. Two layers are on one side of the PCB and two remaining layers are on the other side.

In *symmetrical topology*, signals will have a higher impedance ($105 - 130 \Omega$), interplane decoupling is moderate for removing the switching energy from the power and ground planes, RF return currents do not have the ability to return their source, unless a ground trace is routed on the signal layer adjacent to power plane [32].

In *asymmetrical topology*, the impedance of routing layers can be specified and set to a desired value, interplane decoupling benefits are basically nonexistent. The reference return currents do not have the ability to return to their source, unless a ground trace is routed on the signal layer adjacent to the power plane.

In 4L stack-up, moreover, there are 2 different layer configuration, firstly the signals would be either internal layers or external layers. Difficulty for debugging and repairing damaged tracks is the biggest disadvantage of selecting internal layers as signal layers. The biggest advantage of internal signal layers, is reduction of radiated RF energy through the air by tracks [32].

4.31 Six-layer Stack-up

Normally, in 6L stack-up, two layers are used for reference planes and 4 other layers are used as routing layers. It could be 2 microstrip layers, 2 stripline layers and two internal reference layers. The main advantage of 6L over 4L is lower power/ground plane impedance, which leads to improvement of overall decoupling for components. 2 stripline layers are very appropriate for routing signals with higher RF spectral density. It is recommended that in stripline layers, for every high-frequency high threat signal one discriminated return path is considered. Outer layers are not suited for routing any traces susceptible to externally induced RF events [32].

For a six layers PCB board, there are different configurations, however, the most interesting ones are *1- 2 external microstrip component layers, 2 mid layers as reference layers, and 2 internal layers as stripline layers* and also *2- 2 external microstrip component layers, 2 mid layers as stripline layers, and 2 internal layers as reference layers* [32].

Advantages of config 1 over config 2 are lower impedance value between routing layers, and the added shielding effects of the planes from allowing RF energy to propagate to the environment. A disadvantage for this configuration is the lack of decoupling between the reference planes [32].

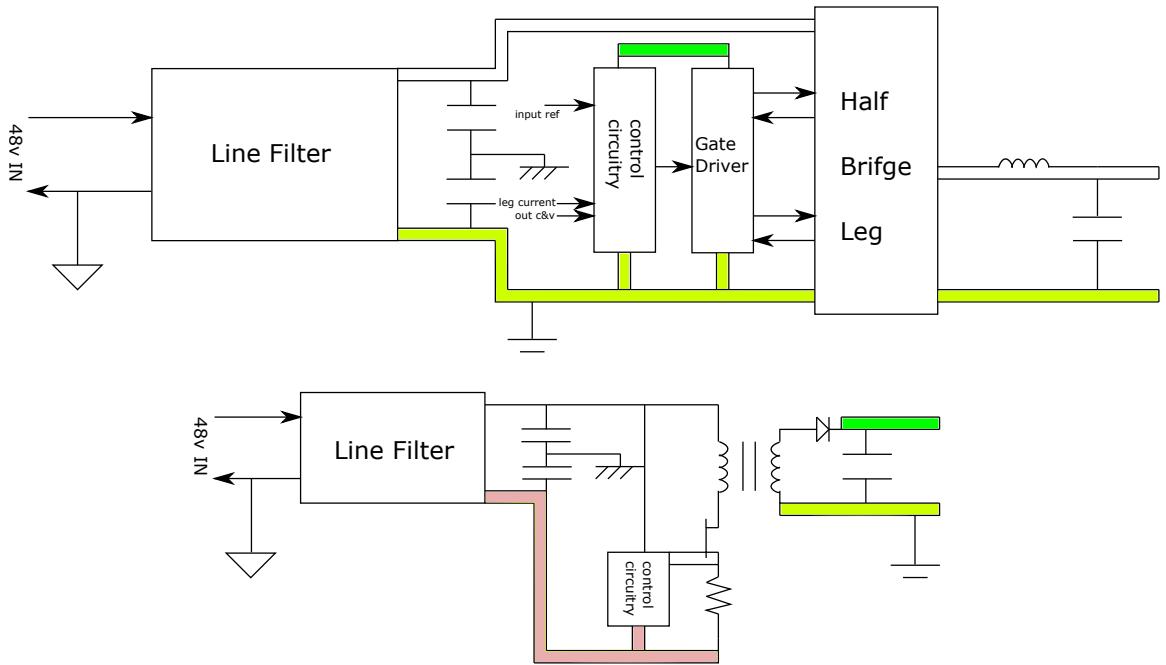
In configuration 1 a significant number of discrete capacitors will be required, and component radiation is still present. As a rule of thumb it should be noted that a smaller spacing between routing layers and a reference plane will reduce the impedance for the transmission lines when jumping layers [32].

4.32 Approach in This Project

In this project, the overview of the circuit can be seen in *Figure 4.52*. In this circuit we have one auxiliary power supply which generates 2 different voltages 6 V and 5 V from 12 V. The ground of this auxiliary power supply is the same as the main output power current. Since there are two different switching frequencies, two different line filters were designed for this project. These two line filters create two different grounds, and although these grounds are not isolated and DC-connected, however in terms of AC-signal, they are not directly connected.

4.33 Zones in PCB

Since there are different grounding systems in this circuit, discrimination between parts is strongly recommended. The parts which have the same grounding system are categorized as one zone. These zones will determine placement of components and also the routing of the PCB. In *Figure 4.53*, three zones have been selected and are described below.



Figures 4.52: Total overview of circuit

4.33.1 Zone 1:

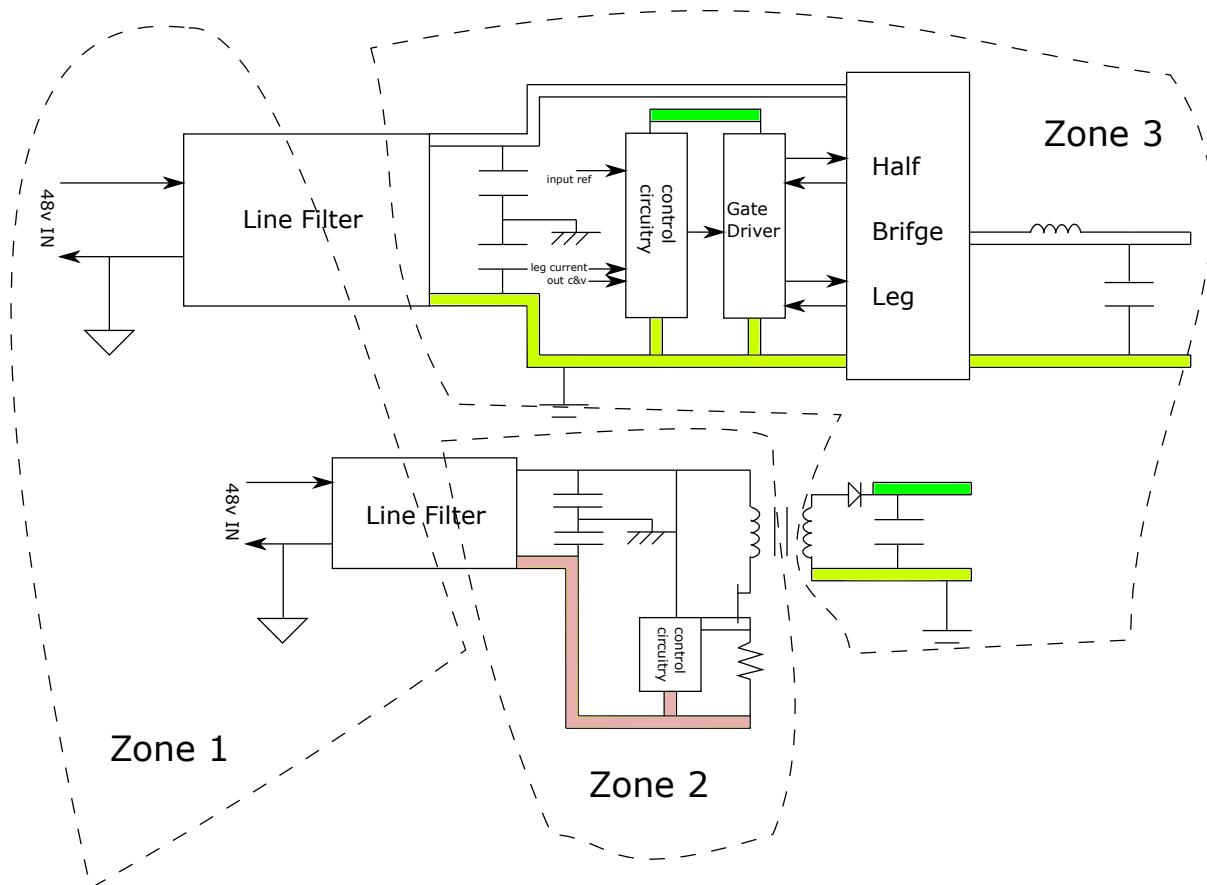
The first zone is the input circuit and EMI filter zone. In this zone, there is a low-pass filter barrier for incoming and also outgoing noises. Since every PCB layer below these parts behaves as a capacitor, the plane below this zone should not be the plane of the other zones.

4.33.2 Zone 2:

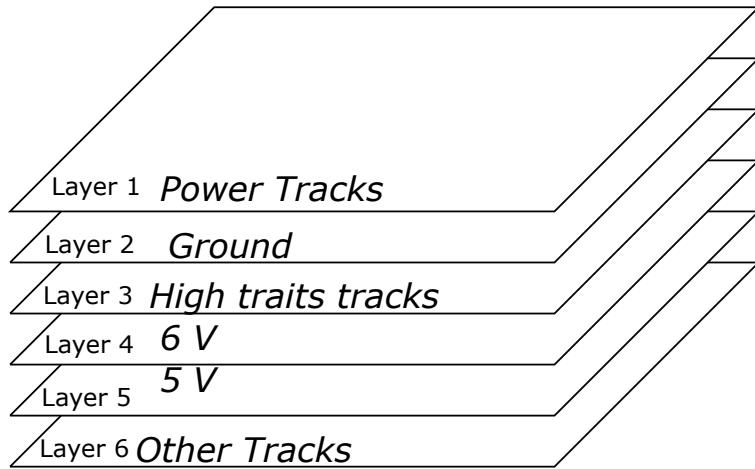
The second zone belongs to the auxiliary filter. This zone is galvanically isolated. Since the gate-driver and the control-circuit need a high quality and immune voltage source, an isolated flyback power supply is proposed. This power source will generate 10 V by its own feedback and 6 V by an additional linear regulator. The output of this power supply does not belong to the zone 2. The planes under zone 2 should not be the same planes as the planes of the other zones. The clearance to the planes of different zones should be large.

4.33.3 Zone 3:

The third zone is the biggest zone of the circuit, which contains very important signals, as well as the output power lines. This zone should be isolated galvanically from zone 2 and also should be considered in connection with zone 1.



Figures 4.53: Different Zones on Circuit



Figures 4.54: Proposed Layer Configuration

4.34 How many layers do we need?

In this project, our main frequency is 5 MHz , and the rise-time and fall-time, which equipment can generate is about $2 - 5 \text{ ns}$, i.e. the system is extremely vulnerable to unbalanced signal routes. Distortion and delay in turning on or turning off a gate signal will lead to permanent damage to the MOSFETs. Since zone 3 spans the largest area of this circuit which contains different voltage supplies the number of the required layers of this zone is decisive for the whole PCB.

A 6-layers PCB is proposed, as shown in *Figure 4.54*, since it provides a good protection of the high traits signals, such as the gate drive tracks and the control lines. The configuration of the ground layer, signal layer, and power supply layer construct a coaxial cable-like protection for high trait signals. In this project, due to the high current of the power tracks, and also the PCB package of the MOSFETs (BGA), we use the top layer for placement of the high current tracks. We also embed a discriminate ground return track on top layer, which is connected by *vias* in a regular distance to layer 2, since we want to have this high current on the top layer.

5 Prototyping and Results

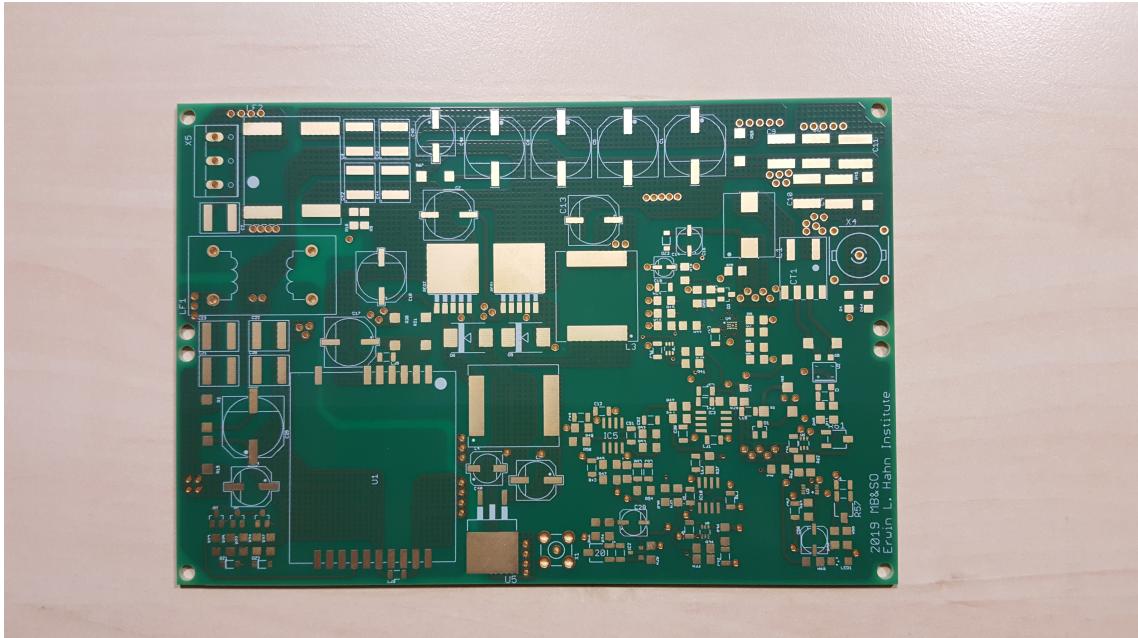
5.1 Introduction

In this chapter, the process of construction and inspection of the PCB board will be described. Since this PCB should be working with a 5 MHz PWM signal, and the maximum expected input signal is 500 KHz , there is a ratio of 10 is between the input signal and PWM signal frequency, i.e. there are minimum 10 PWM signal pulses per input signal cycle. Moreover, the rise time and fall time of the PWM signal, respectively, the high-gate and low-gate signal, in order to reduce the switching losses are designed to be less than 3 ns , therefore the PCB should work in a bandwidth of at least 100 MHz . Consequently, the PCB behaves like an RF board. In this chapter, firstly, the construction of the board will be described, then, the different sections will be inspected and the wave shapes will be illustrated. Finally, the next steps for improvements to become an edge-of-technology-class-D amplifier will be proposed.

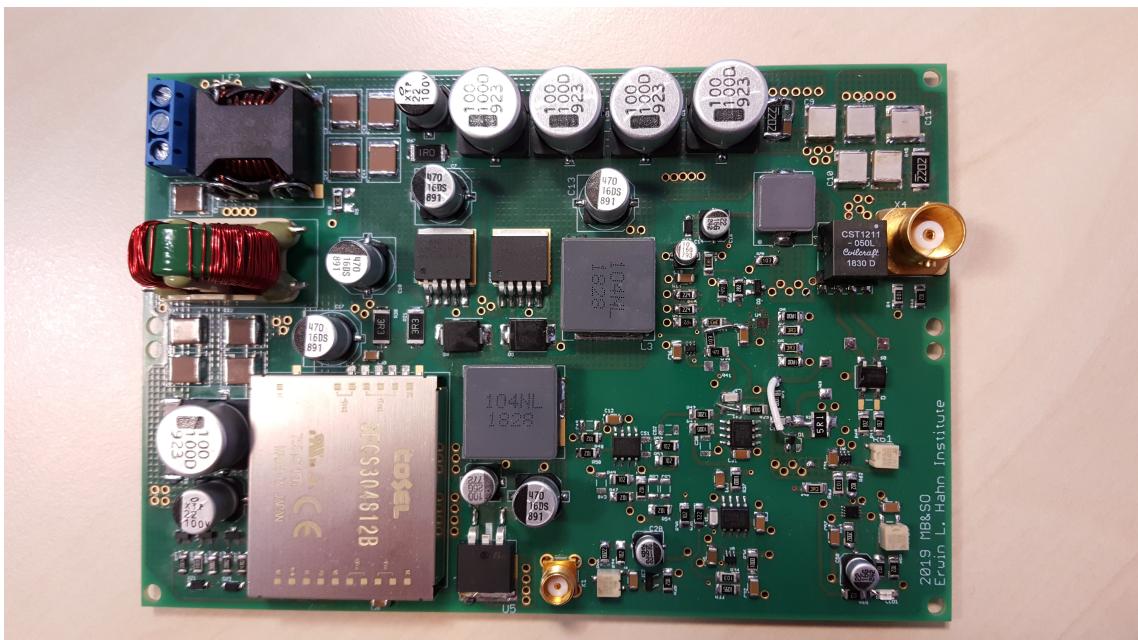
5.2 Construction

Due to so many restrictions in constructing PCB boards, multiple requirements had to be considered. Apart from optimizing the size of the vias and the clearances between *vias* and tracks, it is important to avoid the placement of the signal and high-current tracks near each other. Moreover, as another role of thumb, the board is divided into different sections, in which all same-task components are placed. This does not only help finding errors faster during testing, but also decreases the track length which influences the operation of the circuit in high-frequency. Apart from helping to decrease the overall size, the six-layers structure brings the advantage immunizing the PCB against external interference (refer to section 4.29 for more detail). In *Figure 5.1* and *Figure 5.2* the PCB before and after assembly of the components is shown. Due to the high bandwidth of the circuitry, there is a strong obligation to use a high-frequency probe for the oscilloscope. Moreover, in order to reduce the effect of inductance of GND wire, a strip of wire with the shortest possible length has been used to observe the exact waveform of the component as shown in *Figure 5.3*.

5 Prototyping and Results



Figures 5.1: PCB of the project



Figures 5.2: PCB after assembly



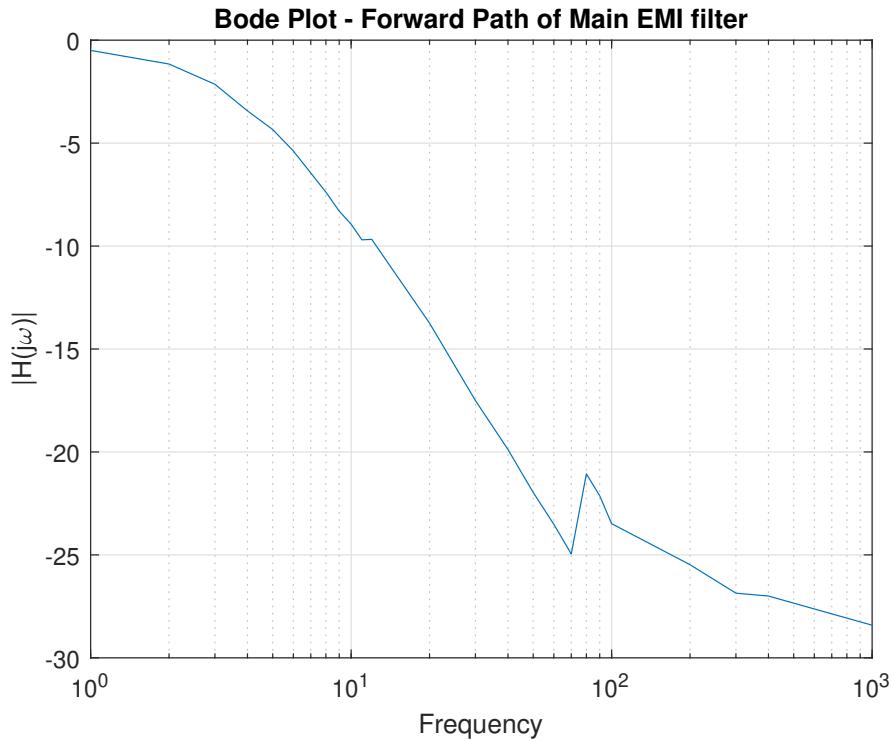
Figures 5.3: Probe of Oscilloscope used for measurement the signals in 100 MHz bandwidth

5.2.1 Next Version Suggestions

For the next version, it is strongly recommended to use the smaller and more compact packages in order to take benefits of operation of the PCB in higher frequencies as efficient as possible. Especially, the components which are pulsating high amount of current should be placed near each other as tight as possible. The resistance footprint should be changed from 1206 to 0402 in order to reduce the track size. Moreover, the half-bridge leg should be placed as close as possible together. The track in between the source of upper-MOSFET and the drain of lower-MOSFET should be as small as possible. Moreover, it should tolerate 20 A current. In the current version, the PCB suffers from the length of the track in between the source and drain, which imposes about 50 nH to the circuit as will be calculated in the section *Power Section*

5.3 EMI/EMC Filter

The results for the EMI/EMC filter correlated well to the expectations drawn from the design process. The properties of the EMI-filter were measured using *Signal Generator (Sony-Tektronix AFG320)* and *Oscilloscope (LeCroy-wavepro 7200A 2GHz)* for different scenarios. It should be mentioned, that in order to avoid negative bias of the capacitance, in all test voltages DC offset has been added to the input waveform to avoid negative voltages on the positive pin of the polar capacitance. Furthermore, the inspection for both directions-input toward output and output toward input- has been done. In *Figure 5.4* and *Figure 5.5* illustrate that the results are satisfactory. The main input filter reduces



Figures 5.4: Bode Plot - Main EMI/EMC filter - Forward Path

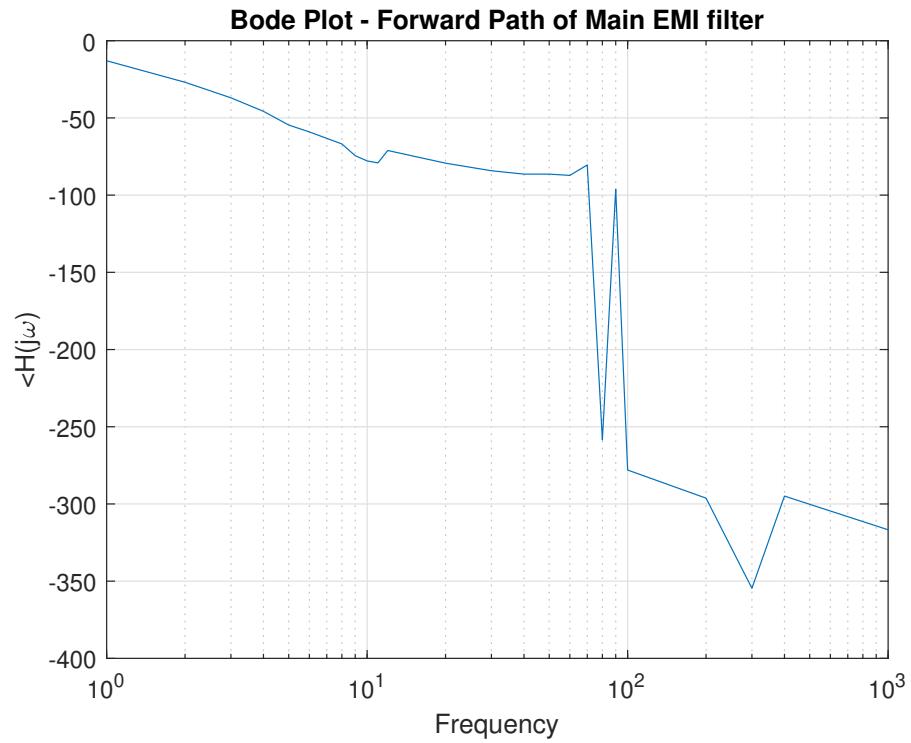
the unwanted signal in the forward path by about -20 dB for the frequency range above 10 KHz . This is a requirement for biomedical devices, which need to meet the *IEC60601* standard. Moreover, for the EMI filter which is used in the input of the auxiliary power supply, in *Figure 5.6* and *Figure 5.7*, it is visible, that the filter reduces the amplitude of the noise signal above 100 Hz by about -30 dB . In both figures of bode plot, the amplitude of the output has a slope of $-40 \frac{\text{dB}}{\text{dec}}$, and after the imposed zero in the transfer function of the filter by the ESR of the capacitors, the slope is degraded to $-20 \frac{\text{dB}}{\text{dec}}$.

5.3.1 Next Version Suggestions

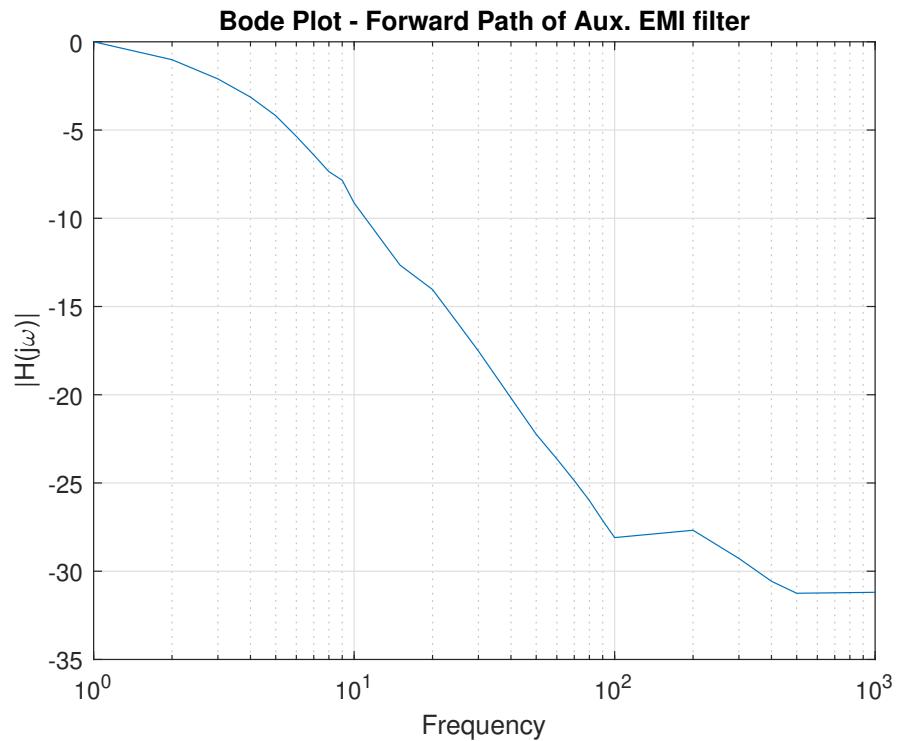
Though, the filter blocks noise signal as expected the size could be reduced in future versions to reduce the overall size of the circuitry. Usage of only one EMI/EMC filter is another suggestion. However, a more robust auxiliary power supply should then be used to withstand the noise, which is generated during the pulsating by the main power stage.

5.4 Oscillator

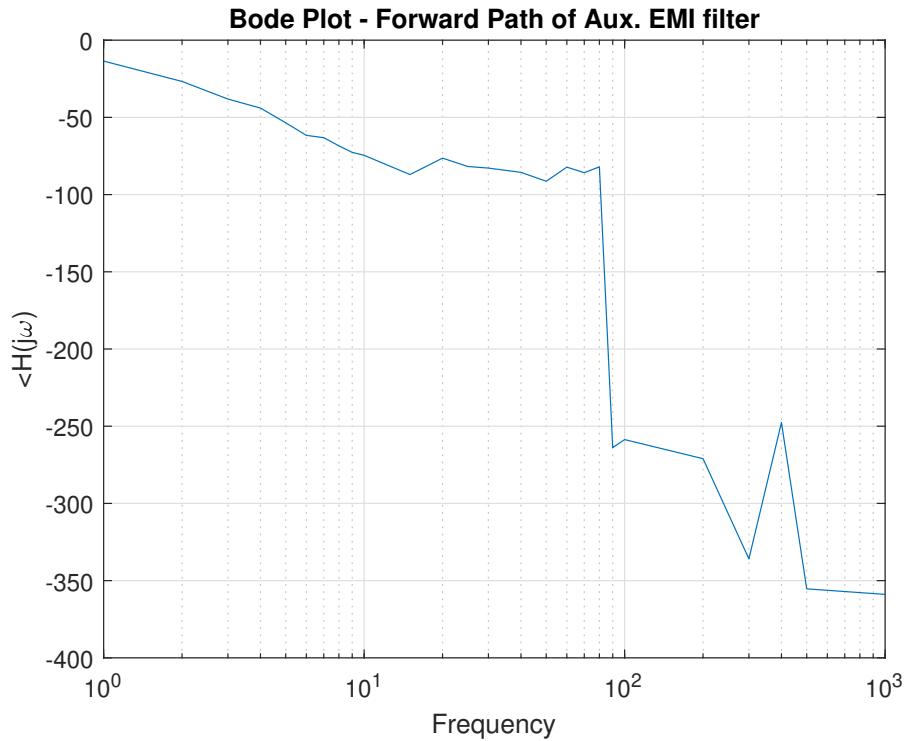
The proposed design of the oscillator generates a frequency about 4.5 MHz . The operation is stable, and the waveform from square wave generator and of the dual slope triangle are



Figures 5.5: Bode Plot - Main EMI/EMC filter - Forward Path



Figures 5.6: Bode Plot - Auxiliary EMI/EMC filter - Forward Path



Figures 5.7: Bode Plot - Auxiliary EMI/EMC filter - Forward Path

shown in *Figure 5.8* . The output is acceptable in terms of sharpness and jitter. The comparator and op-amp fulfill the expected task. Generated waveshapes can be viewed in *Figure 5.10* and *Figure 5.11*.

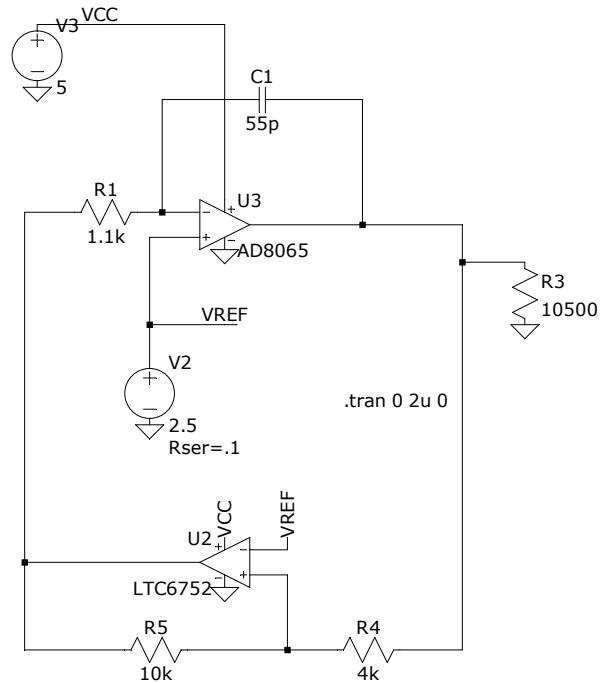
5.4.1 Next Version Suggestions

For next version of the oscillator, it is strongly recommended to use trimmers (potentiometer) for adjusting the frequency of the output, as well as the DC offset for the triangular waveform. Moreover, the immunity of the oscillator toward the noise should be increased by reduction of the magnitude of the resistance in the loop feedback of the oscillator, which can lead to jitter or unwanted pulses. Last but not least, the size of the package could be decreased for the next version of the circuit.

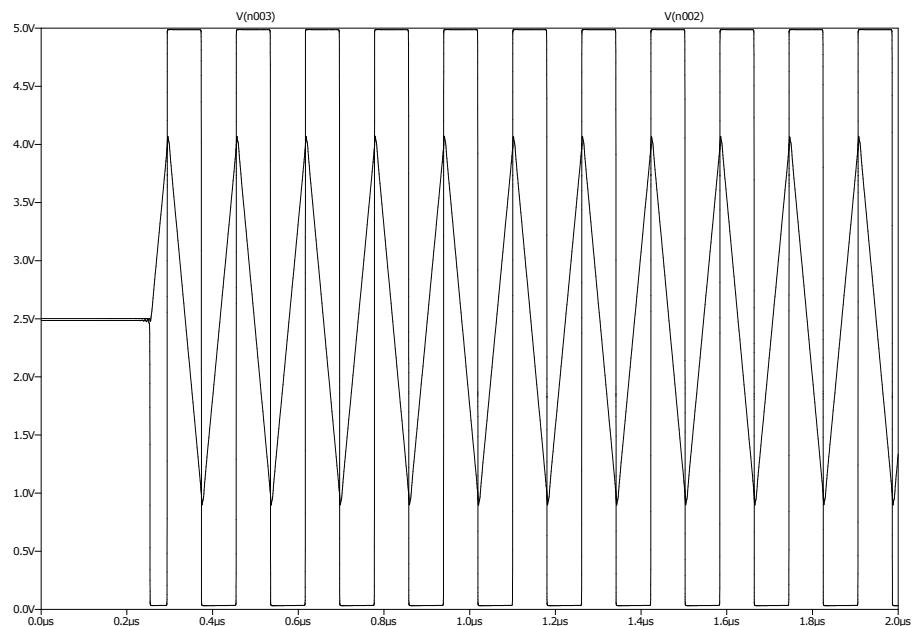
5.5 Power Section

5.5.1 Gate Driver

The Gate driver *PE29101* operates according to expectation and generates high frequency signals with low latency. The output signal of the driver can be seen in *Figure 5.12* and

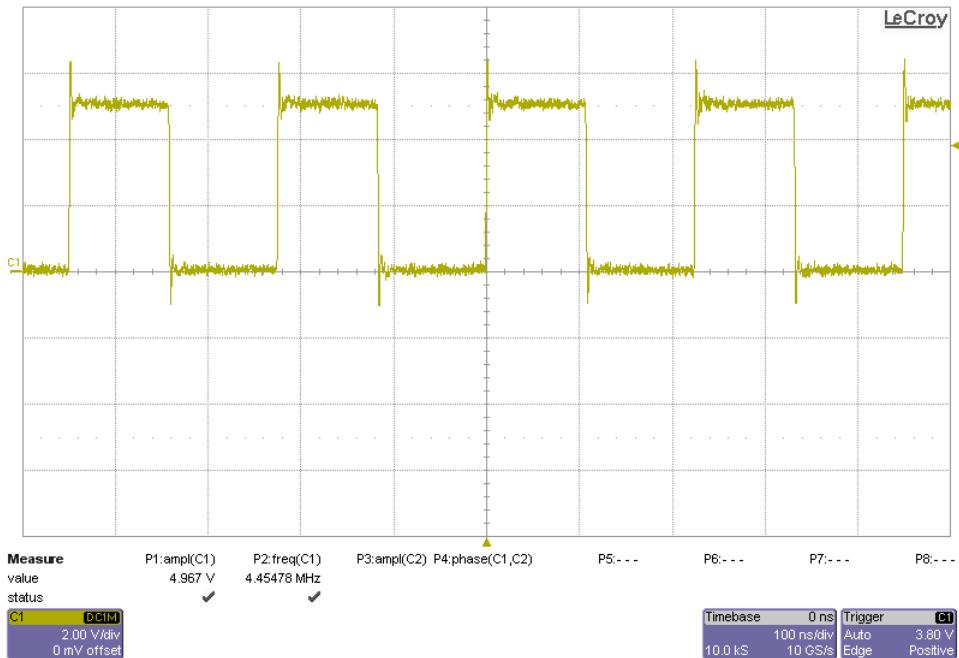


Figures 5.8: Oscillator & Triangular wave generator, simulated in LTSpice

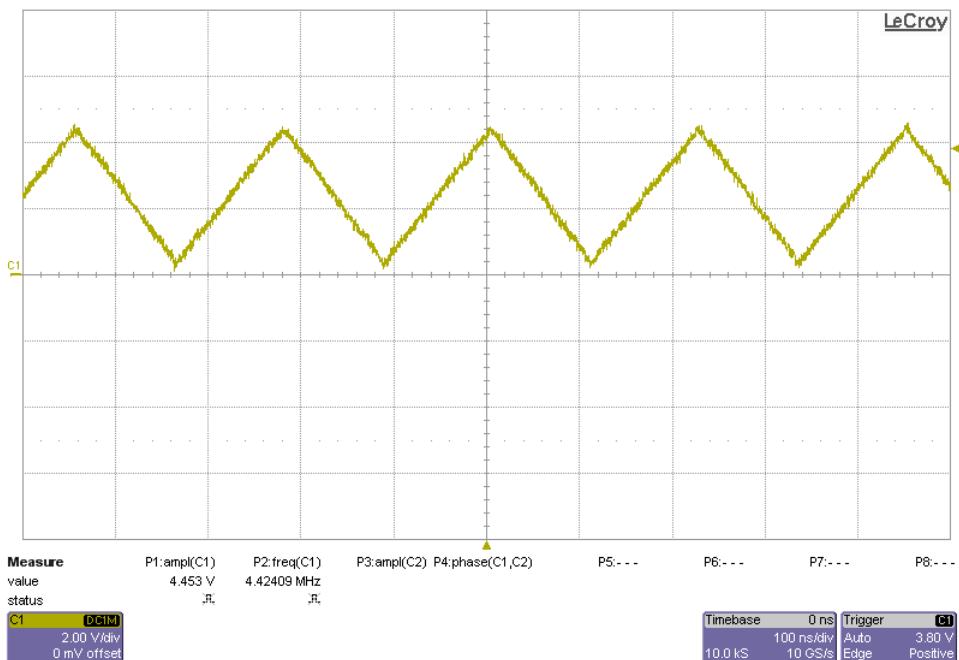


Figures 5.9: Oscillator & Triangular wave generator, Waveform by LTSpice

5 Prototyping and Results



Figures 5.10: Oscillator - square wave generator, Waveform by Oscilloscope



Figures 5.11: Oscillator - triangular wave generator, Waveform by Oscilloscope



Figures 5.12: Lower MOSFET - Gate Pulse

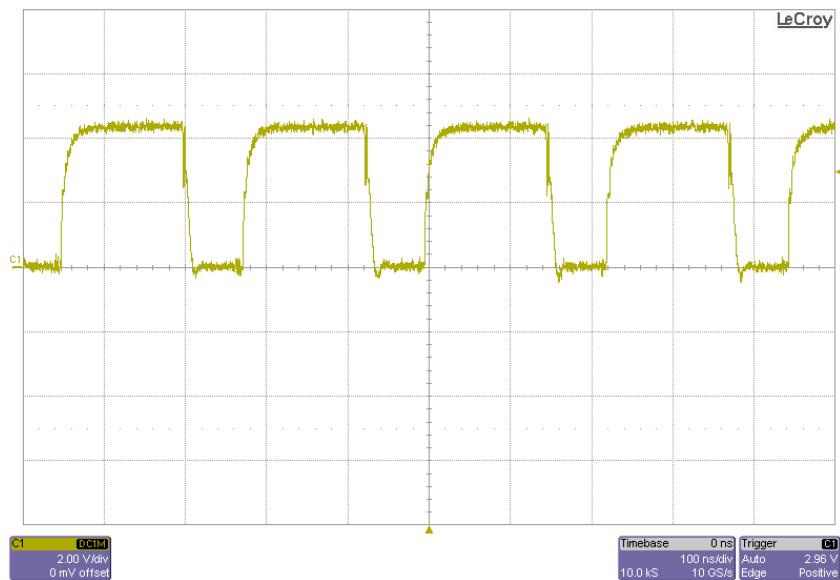
Figure 5.13. It is apparent, that the driver works well, thanks to the small amount of the parasitic inductance of the MOSFET, driver and PCB, as well as the small magnitude of current to power on and off the MOSFET. Therefore, the ringing on the gate wave-shape is little. In *Figure 5.14*, the exact amount of the threshold voltage is 2.5 V, where the gate voltage suddenly starts to decrease due to the LC circuit created by the long track and the parasitic capacitance of the MOSFET. Moreover, around 3 V, the plateau voltage, the gate voltage stays fixed for about 1 ns, and then start to increase again.

In *Figure 5.15*, the effect of Miller capacitor of the GaN MOSFET is observable. Due to the usage of a small resistance in driving the gate, it cannot affect the operation of the gate of the MOSFET. The induced negative voltage is less than the threshold to harm the gate of the MOSFET or even turn it on.

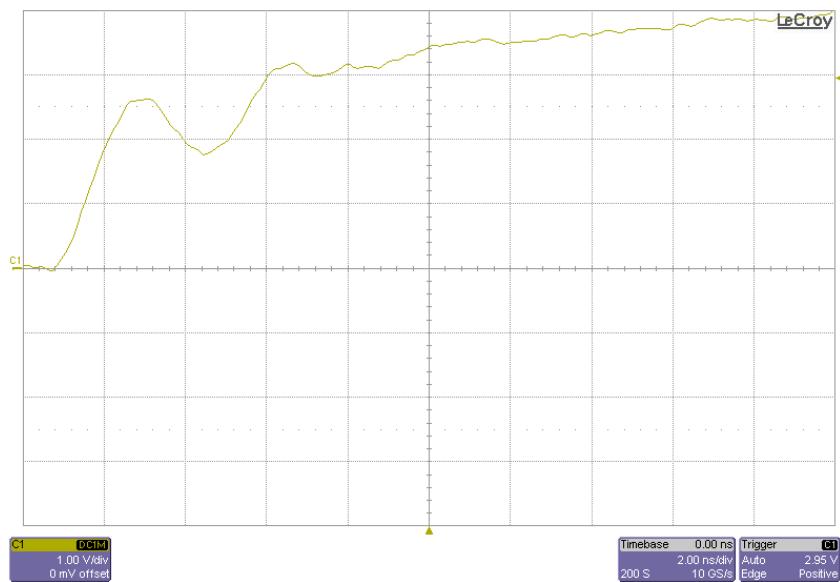
5.5.2 MOSFET Half-Bridge Leg

The most important part of such a converter is the leg of the MOSFETs, which undertakes the task of generation of high-frequency high-power pulses on the input of output-filter. The flawless operation of this part of the converter determines the longevity of the circuit. Two challenging aspects of a leg converter are, firstly, ringing on the drain of MOSFETs due to the reverse recovery effects of their anti-parallel diodes, and secondly, the switching-losses due to the overlap between the on-times of upper and lower MOSFET.

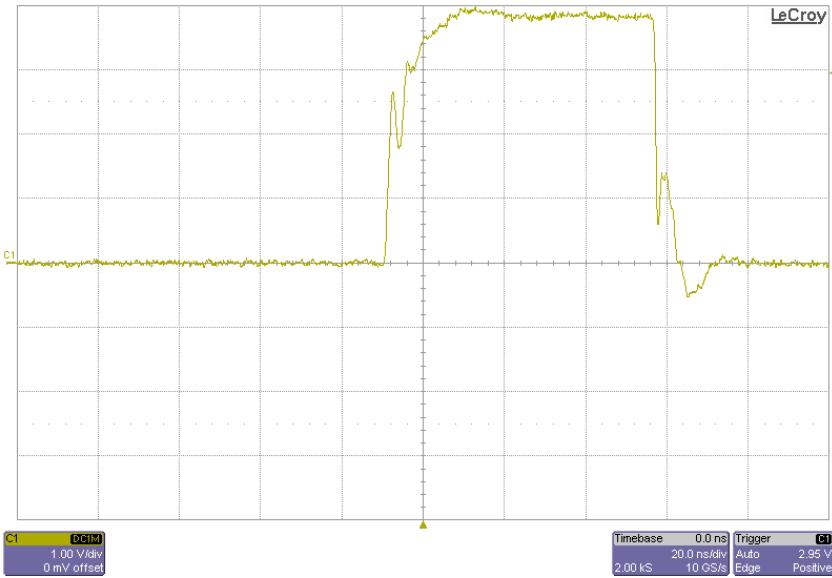
The origin of the ringing on the drain of the MOSFET comes from an LC resonance circuit. The C_{oss} - output capacitance of the MOSFET - and the stray inductance of the PATH between the V_{DD} the H_{SS} for upper MOSFET and H_{SS} and GND for lower MOSFET will oscillate, when the MOSFET turns off, until the energy of the reservoirs (L and C) is dissipated. If the dissipation of this energy was neglected, it would be a conduction-state



Figures 5.13: Upper MOSFET - Gate Pulse



Figures 5.14: Gate of MOSFET - Threshold and Gate Plateau Voltage



Figures 5.15: Gate of MOSFET - Threshold and Gate Plateau Voltage

of MOSFET in the period, when it should be turned off. Therefore, dissipation of this stored energy is important.

To alleviate the problem of the reverse-recovery effect during the design stage, it should be tried to put the elements as closed as together, and the path(track) between the V_{DD} , H_{SS} and GND should be as short as possible.

By observing the frequency of the oscillation (about 66.67 MHz) in *Figure 5.16* and *Figure 5.17*, and C_{OSS} as the main capacitance for this resonance circuit, we can calculate the leakage inductance of the PCB as below:

$$f_{RING} = \frac{1}{2\pi * \sqrt{L_{LK} \cdot C_{LK}}}$$

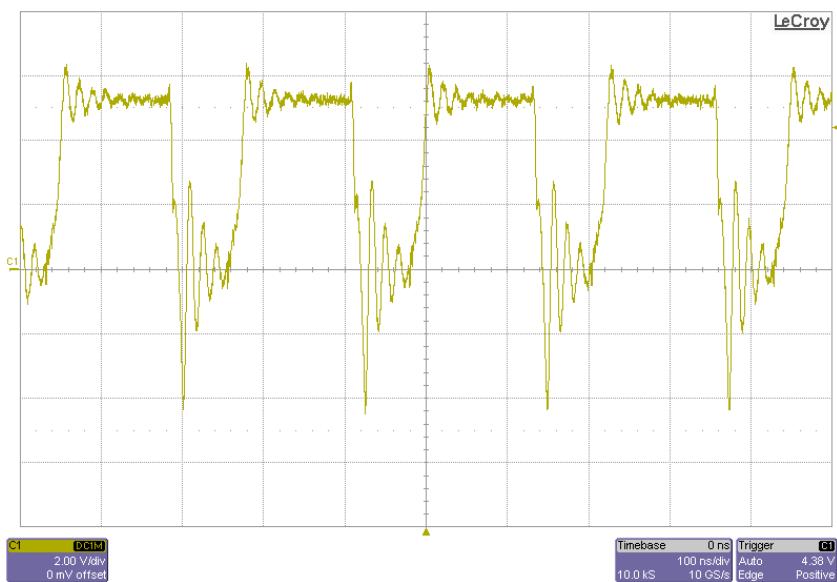
$$\Rightarrow L_{LK} = 20.33\text{ nH}$$

In normal serial RLC resonance circuit, we want to have a critically damped state. Therefore, we set the ζ to 1:

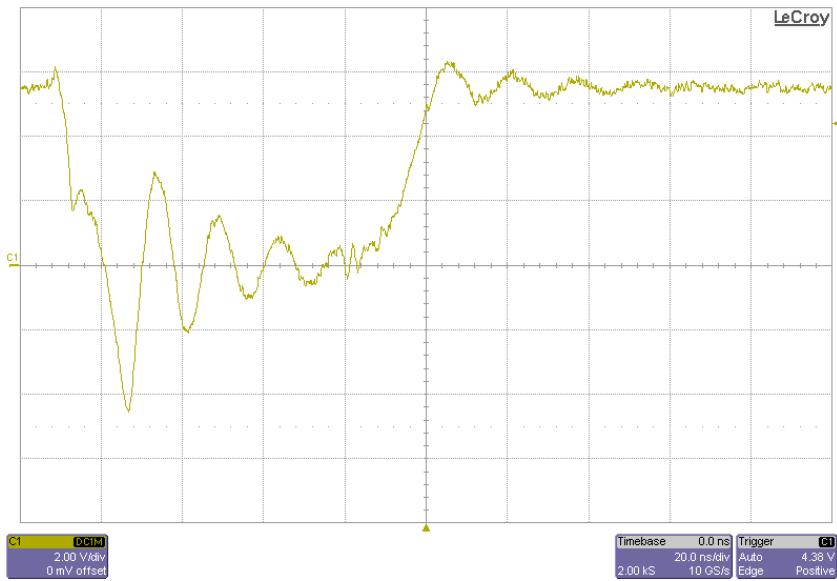
$$\begin{aligned} \zeta &= \left(\frac{1}{2R_s}\right) \sqrt{\frac{L_{LK}}{C_L K}} \\ \Rightarrow R_s &= \left(\frac{1}{2}\right) \sqrt{\frac{20\text{ nH}}{280\text{ pF}}} \\ \Rightarrow R_s &= 4.22\Omega \end{aligned}$$

Since there is an RC snubber circuit available, the capacitor of this snubber should dampen the ringing frequency:

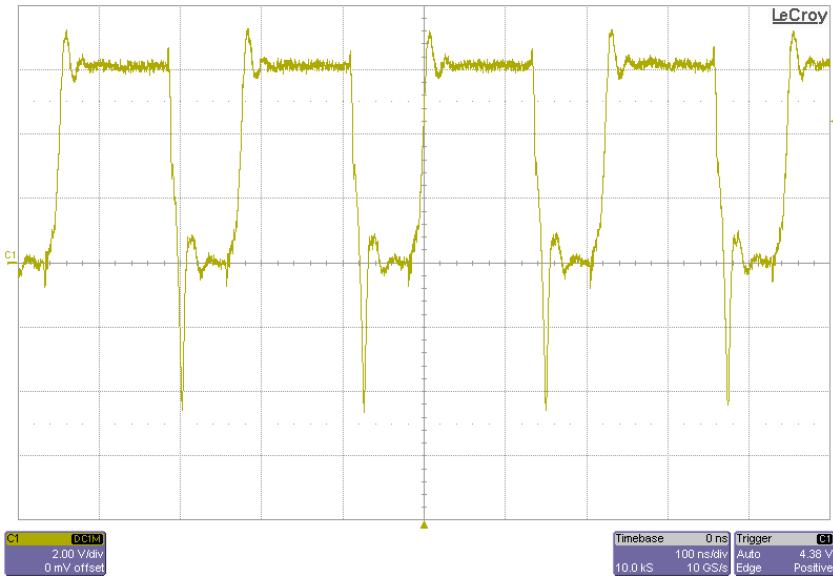
$$\Rightarrow C_s = \frac{1}{2\pi R_s f_{RING}} = \frac{1}{2\pi * 4.22 * 66.67 * 10^6}$$



Figures 5.16: Output Point of Half-Bridge Leg without Snubber



Figures 5.17: Output Point of Half-Bridge Leg without Snubber



Figures 5.18: Output Point of Half-Bridge Leg with Snubber

$$\Rightarrow C_s = 565 \text{ pF}$$

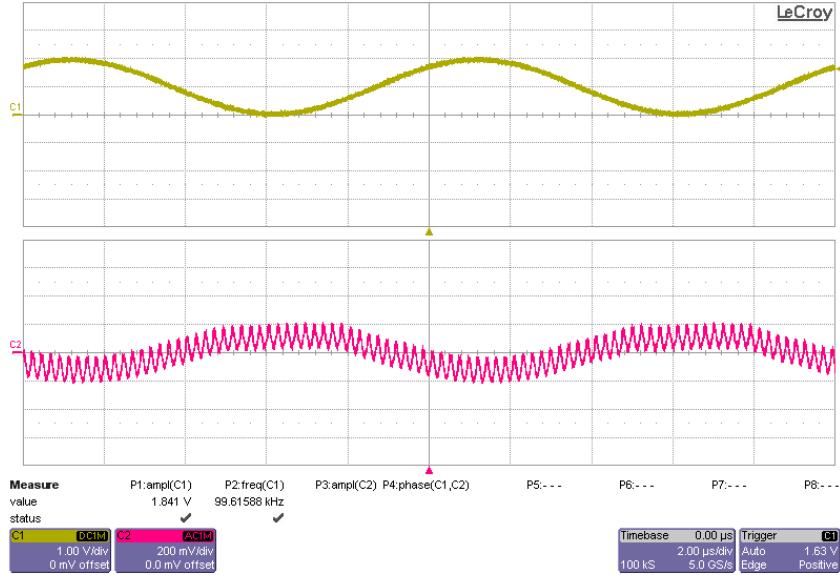
The resulting output waveform after placement of the RC snubber parallel to the MOSFETs can be viewed in *Figure 5.18*. It is visible, that the ringing has been damped. However, the MOSFET suffers from the peak negative and positive voltage, respectively undershoot and overshoot, which is originated from $L_{lk} \frac{di}{dt}$. This inductance is the barrier that disallowes operation at the nominal power of this converter.

5.5.3 Next Version Suggestions:

For the power section, it is recommended to design it modular and to discriminate it from the remaining parts of the circuit. It would be better, if the output filter were placed on a small extra PCB, together with the heat-sink part. The PWM signal should be injected externally to this circuit, using a low inductance connector such as *SMA*, which should pulsate about 5 MHz supporting 2 nS rise- and fall- time .

5.6 Control Section

Due to the lack of time, the control section could not be tested completely. Since, there was a fear of the deficiency of the power section and difficulty in assembling the MOSFET driver which is in *BGA* package. However, this thesis is the starting point for the construction of a high efficiency converter. The remaining activities, such as reaching a higher power per cubic meter, efficiency, robustness and stability, is progressing. In *Figure 5.19*, *Figure 5.20*, and *Figure 5.21*, the operation of the converter, with a light resistive load ($R = 1 \Omega$) is

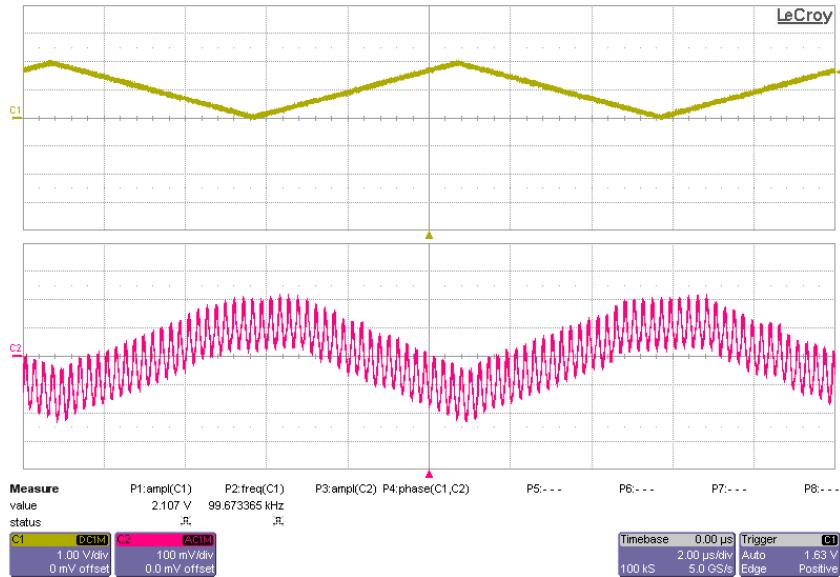


Figures 5.19: Output Signal and Input Sinusoidal Reference- Load less than 20 Watt-
Upper: Input, Lower: Output

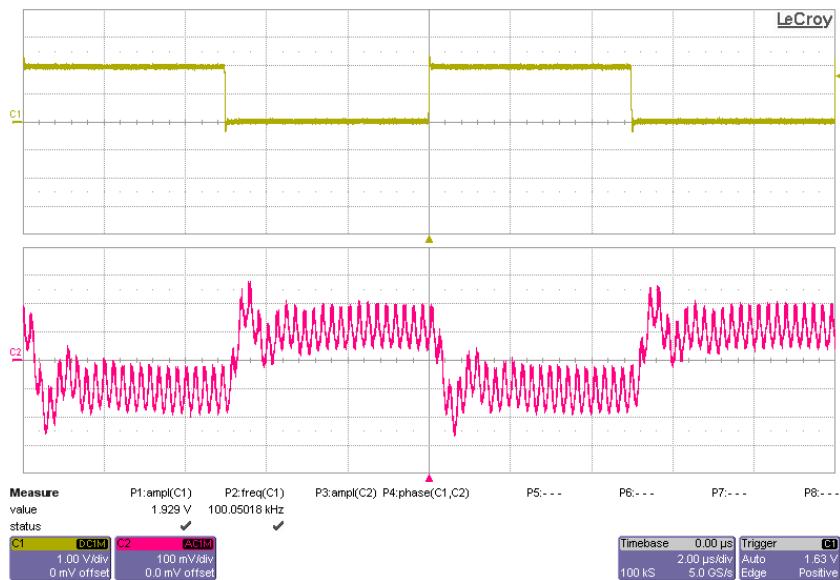
shown. Respectively, sinusoidal, triangular and pulse signals with DC offset, to avoid injecting negative input to the signal section, have been fed to the input of the circuit.

5.6.1 Next Version Suggestions:

The current-mode scheme of the control will be implemented in the next version of the converter. However, the first step is arriving to the nominal power and claimed efficiency of the converter using the current voltage-mode scheme. Peak and average current-mode will be inspected and the most efficient, robust design will be implemented for manufacturing.



Figures 5.20: Output Signal and Input Triangular Reference- Load less than 20 Watt-Upper: Input, Lower: Output



Figures 5.21: Output Signal and Input Pulse Reference- Load less than 20 Watt-Upper: Input, Lower: Output

6 Summary and Outlook

During this project, the design and implementation of a new version of a radiofrequency amplifier has been pursued. This amplifier should operate in the power section of the RF amplifier stage of a *7T MRI system*. For every RF transmit channel of the body and local array coils, one amplifier is needed. For the 7 T MRI system at the *Erwin L. Hahn Institute* altogether 32 amplifiers are needed to supply the 32 independent RF channels.

Due to the essence of high-power large-bandwidth of the input signal, a class D amplifier in half-bridge topology, which operates at 5 MHz , has been proposed, and to solve the reverse recovery problem of the body diode of the MOSFETs, GaN MOSFETs have been used. However, due to the high frequency PWM pulses and stray inductances of the PCB, the resulting circuit suffers from switching losses.

As outlook for the next version, firstly it will be pursued to design an even more compact PCB and secondly, the controller loop will be revised in terms of jitter, noise margins and stability. A sigma-delta modulator will be another choice for reduction of the losses, since it will reduce the clock frequency of the PWM signal. The full-bridge ZVS method is the fundamental solution for this problem of the half-bridge and for the last improvement will be inspected.

Bibliography

- [1] M. Erturk, “A 16-channel combined loop-dipole transceiver array for 7 tesla body mri. magnetic resonance in medicine,” *official journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, vol. 884-94, Feb 2017.
- [2] A. Graessl, “Modular 32-channel transceiver coil array for cardiac mri at 7.0t. magnetic resonance in medicine,” *fficial journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Jul 2014.
- [3] A. Raaijmakers, “The fractionated dipole antenna: A new antenna for body imaging at 7 tesla,” *Magnetic resonance in medicine : official journal of the / Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Mar 2016.
- [4] S. Rietsch, “7t ultra-high field body mr imaging with an 8-channel transmit/32-channel receive radiofrequency coil array,” *Medical physics*, Jul 2018.
- [5] I. van Kalleveen, “Adiabatic turbo spin echo in human applications at 7 t. magnetic resonance in medicine,” *official journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Aug 2012.
- [6] K. Wrede, “Caudal image contrast inversion in mprage at 7 tesla: Problem and solution,” *Academic radiology*, vol. 19, pp. 172–178, Feb 2012.
- [7] W. Grissom, “Spatial domain method for the design of rf pulses in multicoil parallel excitation,” *Magnetic resonance in medicine : official journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Sep 2006.
- [8] U. Katscher, “Transmit sense. magnetic resonance in medicine,” *official journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Jan 2003.
- [9] S. Saekho, “Small tip angle three-dimensional tailored radiofrequency slab-select pulse for reduced b1 inhomogeneity at 3 t. magnetic resonance in medicine,” *official journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Feb 2005.
- [10] K. Setsompop, “Slice-selective rf pulses for in vivo b1+ inhomogeneity mitigation at 7 tesla using parallel rf excitation with a 16-element coil,” *Magnetic resonance in medicine : official journal of the Society of Magnetic Resonance in Medicine / Society of Magnetic Resonance in Medicine*, Dec 2008.

- [11] K. Ward, “A new class of contrast agents for mri based on proton chemical exchange dependent saturation transfer (cest),” *Journal of magnetic resonance*, Mar 2000.
- [12] A. Lidow and J. Strydom, *GaN Transistor for efficient power conversion*. Reading, Massachusetts: John wiley, 1993.
- [13] D. Weishaupt, *How Does MRI work?* Springer, 2008.
- [14] E. Haacke, *Magnetic Resonance Imaging:Physical Principles and Sequence Design*. Wiley Blackwell.
- [15] S. S. Hidalgo-tobon, “Theory of gradient coil design methods for magnetic resonance imaging,” *Wiley InterScience*, pp. 223–242, June 2010.
- [16] P. C. Lauterbur, “Image formation by induced local interactions: examples employing nuclear magnetic resonance,” *Nature*, vol. 242, pp. 190–191, 1973.
- [17] J. T. Vaughan, *RF coils for MRI*. John Wiley & Sons Ltd., 2012.
- [18] W. H. Doherty, “A new high efficiency power amplifier for modulated waves,” *Proceedings of the Institute of Radio Engineers*, vol. 24, pp. 1163–1182, Sep 1956.
- [19] A. H. Reeves, “The 25th anniversary of pulse code modulation,” *IEEE Spectrum*, vol. 2, pp. 56–63, May 1965.
- [20] M. K. Kazimerczuk, *RF Power Amplifiers*. Reading, Massachusetts: John wiley & sons.
- [21] H. L. Krauss, *Solid State Radio Engineering*. Reading, Massachusetts: John wiley & sons.
- [22] S. Cuk, “A conceptually new high-frequency switched-mode power amplifier techniques eliminates current ripple,” *Peoceedings of Powercon*, May 1978.
- [23] E. G. Dean, *High-efficiency radio-frequency power amplifiers*. PhD thesis, Oregon State University, 1965.
- [24] G. Gong, *Hybrid Amplifiers for AC Power Source Applications*. PhD thesis, ETH ZURICH, 2009.
- [25] “Slaa701a - lc filter design,” 10 2016.
- [26] U. M. Standard, “mil std 461e requirements for the control of electromagnetic interference characteristics of subsystems and equipment,” 1999.
- [27] R. D. Middlebrook, “Design techniques for preventing input filter oscillations in switched-mode regulators,” *Proc. Powercon’78*, pp. A3.1–A3.16, 1978.
- [28] R. D. Middlebrook, “Input filter considerations in design and application of switching regulators,” *Conf. Rec. IEEE-IAS Annual Meeting*, pp. 366–382, 1976.

Bibliography

- [29] IEC, “Iec 61000-3-3 electromagnetic compatibility (emc) - part 3-3: Limits - limitation of voltage changes voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current less than 16 a per phase and not subject to conditional connection,” 2017.
- [30] S. Ben-Yakoov, “Average simulation of pwm converters by direct implementation of behavioural relationships,” *Int. J. Electronics*, vol. 77, pp. 731–746, 1994.
- [31] R. B. Ridley, *A new small-signal model for current-mode control*. PhD thesis, Virginia Polytechnic Institute and State University, 1990.
- [32] M. I. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance: A Handbook for Designers*. Wiley-IEEE Press, 2000.
- [33] G. Hanington, “High-efficiency power amplifier using dynamic power-supply voltage for cdma applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, pp. 1471–1497, Aug 1999.
- [34] P. Baxandall, “Transistor sine-wave lc oscillators. some general considerations and new developments,” *Proceedings of the IEE - Part B: Electronic and Communication Engineering*, vol. 106, pp. 748–758, May 1959.