

# 74VHC595; 74VHCT595

8-bit serial-in/serial-out or parallel-out shift register with output latches

Rev. 3 — 25 June 2020

Product data sheet

## 1. General description

The 74VHC595; 74VHCT595 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74VHC595; 74VHCT595 are 8-stage serial shift registers with a storage register and 3-state outputs. The shift registers have separate clocks.

Data is shifted on the positive-going transitions of the shift register clock input (SHCP). The data in each register is transferred to the storage register on a positive-going transition of the storage register clock input (STCP). If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7S) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ( $\overline{OE}$ ) is LOW.

## 2. Features and benefits

- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Inputs accept voltages higher than  $V_{CC}$
- Input levels:
  - For 74VHC595: CMOS level
  - For 74VHCT595: TTL level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

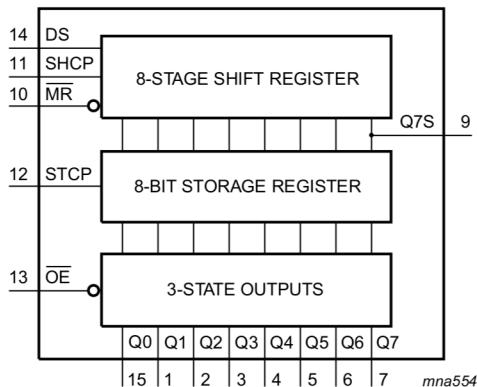
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## 4. Ordering information

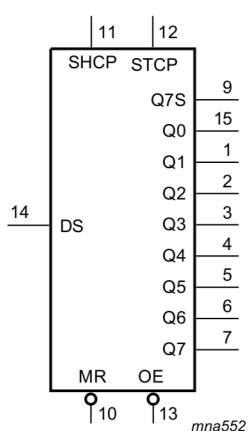
**Table 1. Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74VHC595D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74VHCT595D				
74VHC595PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74VHCT595PW				
74VHC595BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74VHCT595BQ				

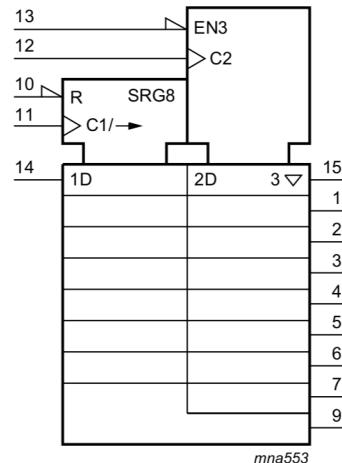
## 5. Functional diagram



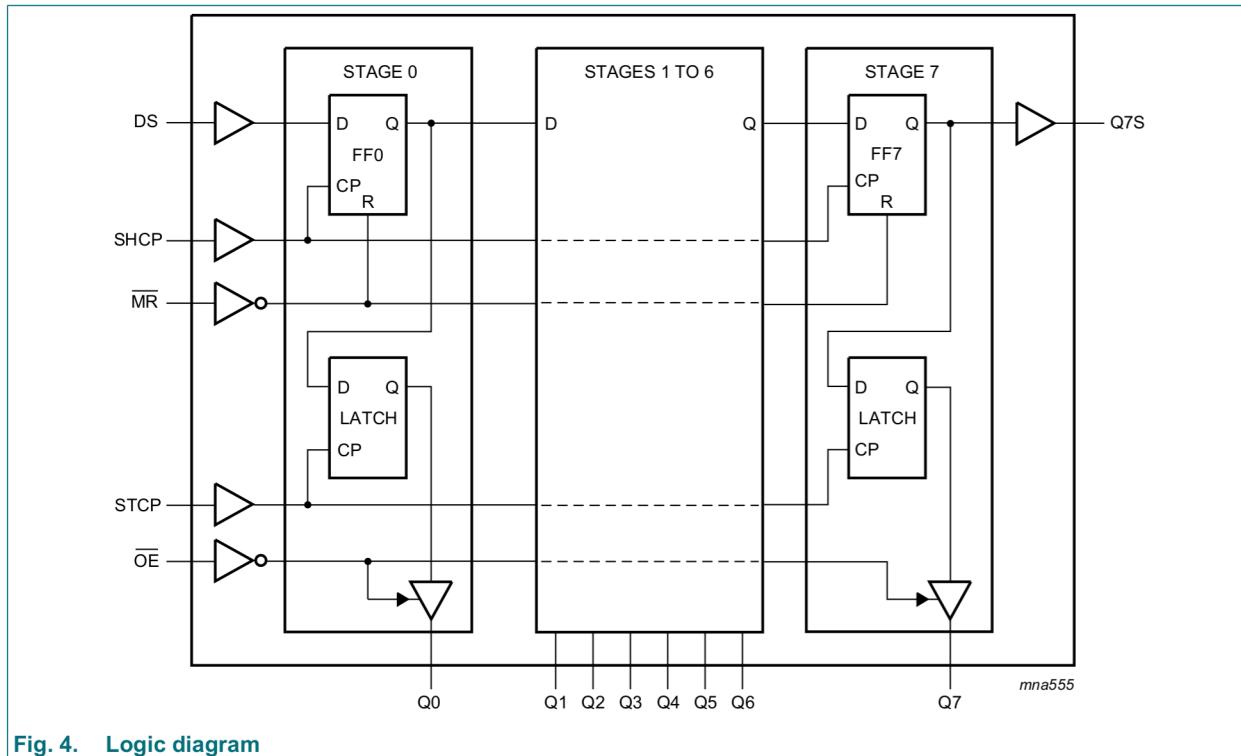
**Fig. 1. Functional diagram**



**Fig. 2. Logic symbol**



**Fig. 3. IEC logic symbol**



## 6. Pinning information

### 6.1. Pinning

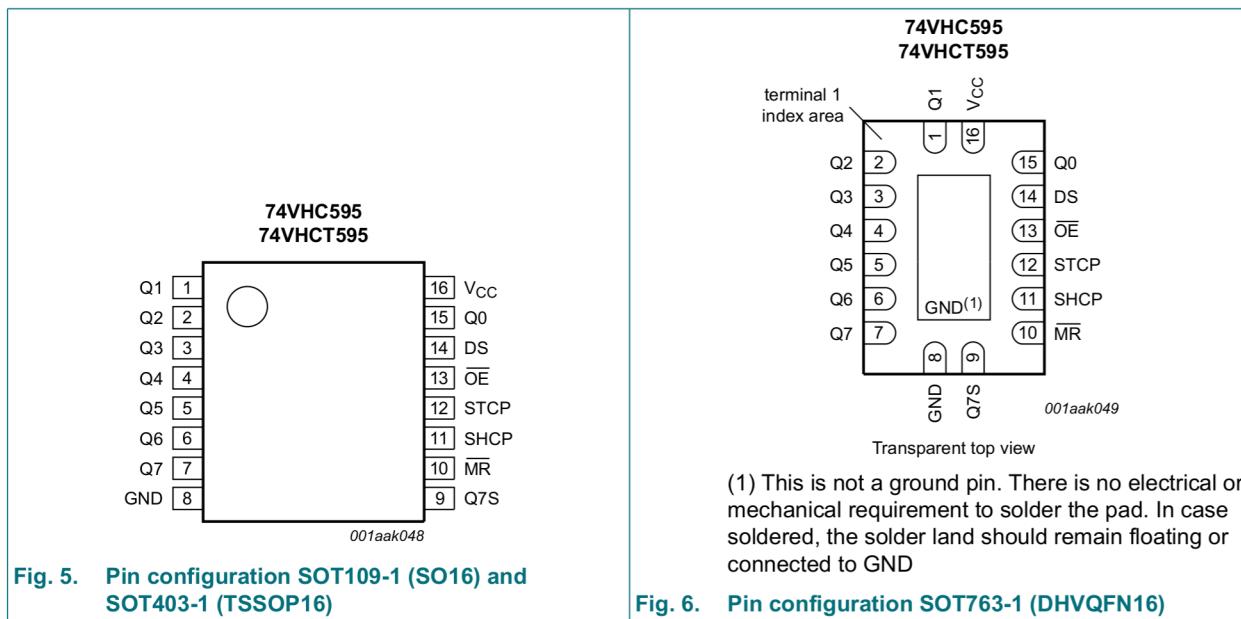


Fig. 5. Pin configuration SOT109-1 (SO16) and SOT403-1 (TSSOP16)

Fig. 6. Pin configuration SOT763-1 (DHVQFN16)

## 6.2. Pin description

**Table 2. Pin description**

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
MR	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
OE	13	output enable input (active LOW)
DS	14	serial data input
V <sub>CC</sub>	16	supply voltage

## 7. Functional description

**Table 3. Function table**

H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change; Z = high-impedance OFF-state.

Control				Input	Output		Function
SHCP	STCP	OE	MR	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on MR only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

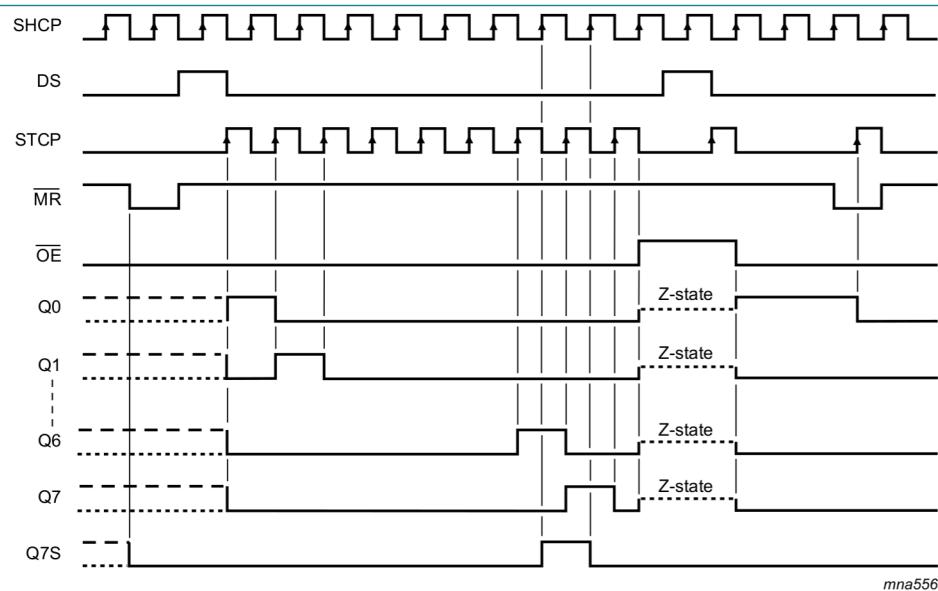


Fig. 7. Timing diagram

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5 \text{ V}$ [1]	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5 \text{ V} \text{ or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-20	+20	mA
$I_O$	output current	$V_O = -0.5 \text{ V} \text{ to } (V_{CC} + 0.5 \text{ V})$	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40 \text{ °C} \text{ to } +125 \text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.

For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

For SOT763-1 (DHVQFN16) package:  $P_{tot}$  derates linearly with 11.2 mW/K above 106 °C.

## 9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	74VHC595			74VHCT595			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	5.5	0	-	5.5	V
V <sub>O</sub>	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	100	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	20	-	-	20	ns/V

## 10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74VHC595</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I <sub>O</sub> = -8.0 mA; V <sub>CC</sub> = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25	-	±2.5	-	±10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	μA
C <sub>I</sub>	input capacitance		-	3	10	-	10	-	10	pF

## 8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74VHCT595</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
$I_I$	input leakage current	$V_I = 5.5 \text{ V or GND}$ ; $V_{CC} = 0 \text{ V to } 5.5 \text{ V}$	-	-	0.1	-	1.0	-	2.0	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	$\pm 0.25$	-	$\pm 2.5$	-	$\pm 10$	$\mu\text{A}$
$I_{CC}$	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	$\mu\text{A}$
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; other inputs at $V_{CC}$ or GND; $I_O = 0 \text{ A}$ ; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance		-	3	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>74VHC595</b>										
$t_{pd}$	propagation delay	SHCP to Q7S; see Fig. 8 [2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	5.7	13.0	1.0	15.0	1.0	16.5	ns
		$C_L = 50 \text{ pF}$	-	7.7	16.5	1.0	18.5	1.0	20.1	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	4.0	8.2	1.0	9.4	1.0	10.5	ns
		$C_L = 50 \text{ pF}$	-	5.4	10.0	1.0	11.4	1.0	12.5	ns
		STCP to Qn; see Fig. 9 [2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	5.9	11.9	1.0	13.5	1.0	15.0	ns
		$C_L = 50 \text{ pF}$	-	7.7	15.4	1.0	17.0	1.0	18.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	4.2	7.4	1.0	8.5	1.0	9.5	ns
		$C_L = 50 \text{ pF}$	-	5.5	9.0	1.0	10.5	1.0	11.5	ns
		$\overline{MR}$ to Q7S; see Fig. 11 [3]								
$t_{en}$	enable time	$\overline{OE}$ to Qn; see Fig. 12 [4]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	5.6	11.5	1.0	13.5	1.0	15.0	ns
		$C_L = 50 \text{ pF}$	-	7.4	15.0	1.0	17.0	1.0	18.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	4.4	8.0	1.0	9.1	1.0	10.0	ns
		$C_L = 50 \text{ pF}$	-	5.6	10.0	1.0	11.1	1.0	12.0	ns
$t_{dis}$	disable time	$\overline{OE}$ to Qn; see Fig. 12 [5]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	5.4	11.0	1.0	13.0	1.0	14.5	ns
		$C_L = 50 \text{ pF}$	-	8.7	15.7	1.0	16.2	1.0	17.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	3.8	8.0	1.0	9.5	1.0	10.5	ns
		$C_L = 50 \text{ pF}$	-	5.8	10.3	1.0	11.0	1.0	12.0	ns

## 8-bit serial-in/serial-out or parallel-out shift register with output latches

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
$f_{max}$	maximum frequency	SHCP or STCP; see Fig. 8 and Fig. 9								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	80	125	-	60	-	40	-	MHz
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	130	170	-	110	-	90	-	MHz
$t_W$	pulse width	SHCP HIGH or LOW; see Fig. 8								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 9								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see Fig. 11								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
$t_{su}$	set-up time	DS to SHCP; see Fig. 10								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.5	-	-	3.5	-	3.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 9								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	8.5	-	-	8.5	-	8.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
$t_h$	hold time	DS to SHCP; see Fig. 10								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	-	-	1.5	-	1.5	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	ns
$t_{rec}$	recovery time	MR to SHCP; see Fig. 11								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.5	-	-	2.5	-	2.5	-	ns
$C_{PD}$	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_i = \text{GND to } V_{CC};$ all 9 outputs switching	[6]	-	180	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>74VHCT595; V<sub>CC</sub> = 4.5 V to 5.5 V</b>										
t <sub>pd</sub>	propagation delay	SHCP to Q7S; see Fig. 8 [2]								
		C <sub>L</sub> = 15 pF	-	3.8	8.2	1.0	9.0	1.0	10.0	ns
		C <sub>L</sub> = 50 pF	-	5.2	10.0	1.0	11.0	1.0	12.0	ns
		STCP to Qn; see Fig. 9 [2]								
		C <sub>L</sub> = 15 pF	-	4.0	7.4	1.0	8.5	1.0	9.5	ns
		C <sub>L</sub> = 50 pF	-	5.3	9.0	1.0	10.5	1.0	11.5	ns
		MR to Q7S; see Fig. 11 [3]								
		C <sub>L</sub> = 15 pF	-	4.6	8.2	1.0	9.5	1.0	10.5	ns
		C <sub>L</sub> = 50 pF	-	5.8	10.5	1.0	11.5	1.0	12.5	ns
t <sub>en</sub>	enable time	OE to Qn; see Fig. 12 [4]								
		C <sub>L</sub> = 15 pF	-	4.8	9.0	1.0	11.0	1.0	12.0	ns
		C <sub>L</sub> = 50 pF	-	6.2	11.6	1.0	13.0	1.0	14.5	ns
t <sub>dis</sub>	disable time	OE to Qn; see Fig. 12 [5]								
		C <sub>L</sub> = 15 pF	-	3.6	6.9	1.0	8.0	1.0	9.0	ns
		C <sub>L</sub> = 50 pF	-	5.8	10.3	1.0	11.0	1.0	12.0	ns
f <sub>max</sub>	maximum frequency	SHCP and STCP; see Fig. 8 and Fig. 9	130	170	-	110	-	90	-	MHz
t <sub>w</sub>	pulse width	SHCP HIGH or LOW; see Fig. 8	5.0	-	-	5.0	-	5.0	-	ns
		STCP HIGH or LOW; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
		MR LOW; see Fig. 11	5.0	-	-	5.0	-	5.0	-	ns
t <sub>su</sub>	set-up time	DS to SHCP; see Fig. 10	3.0	-	-	3.0	-	3.0	-	ns
		SHCP to STCP; see Fig. 9	5.0	-	-	5.0	-	5.0	-	ns
t <sub>h</sub>	hold time	DS to SHCP; see Fig. 10	2.0	-	-	2.0	-	2.0	-	ns
t <sub>rec</sub>	recovery time	MR to SHCP; see Fig. 11	3.0	-	-	3.0	-	3.0	-	ns
C <sub>PD</sub>	power dissipation capacitance	f <sub>i</sub> = 1 MHz; V <sub>i</sub> = GND to V <sub>CC</sub> ; all 9 outputs switching [6]	-	190	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t<sub>pd</sub> is the same as t<sub>PHL</sub> and t<sub>PLH</sub>.

[3] t<sub>pd</sub> is the same as t<sub>PHL</sub> only.

[4] t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

[5] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[6] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

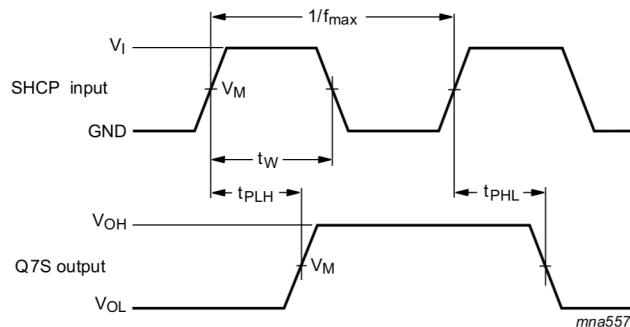
f<sub>o</sub> = output frequency in MHz;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

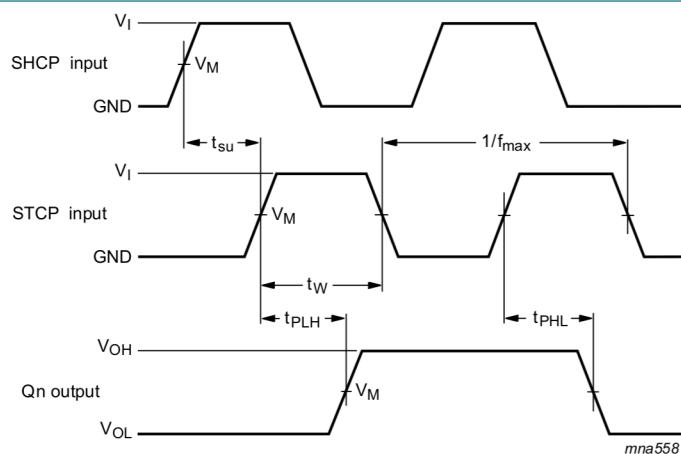
### 11.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

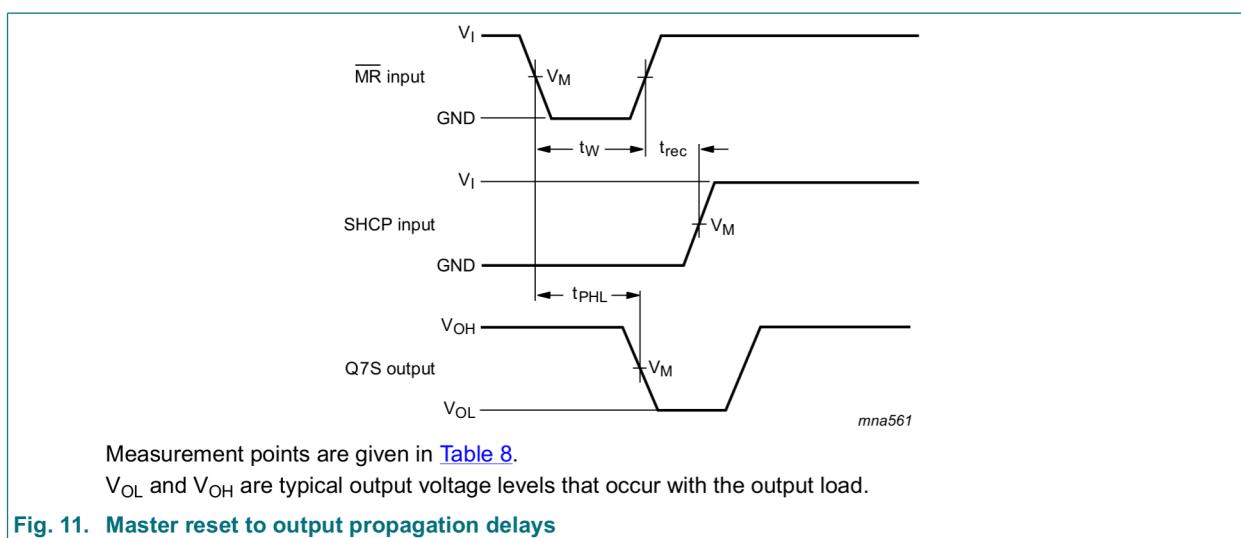
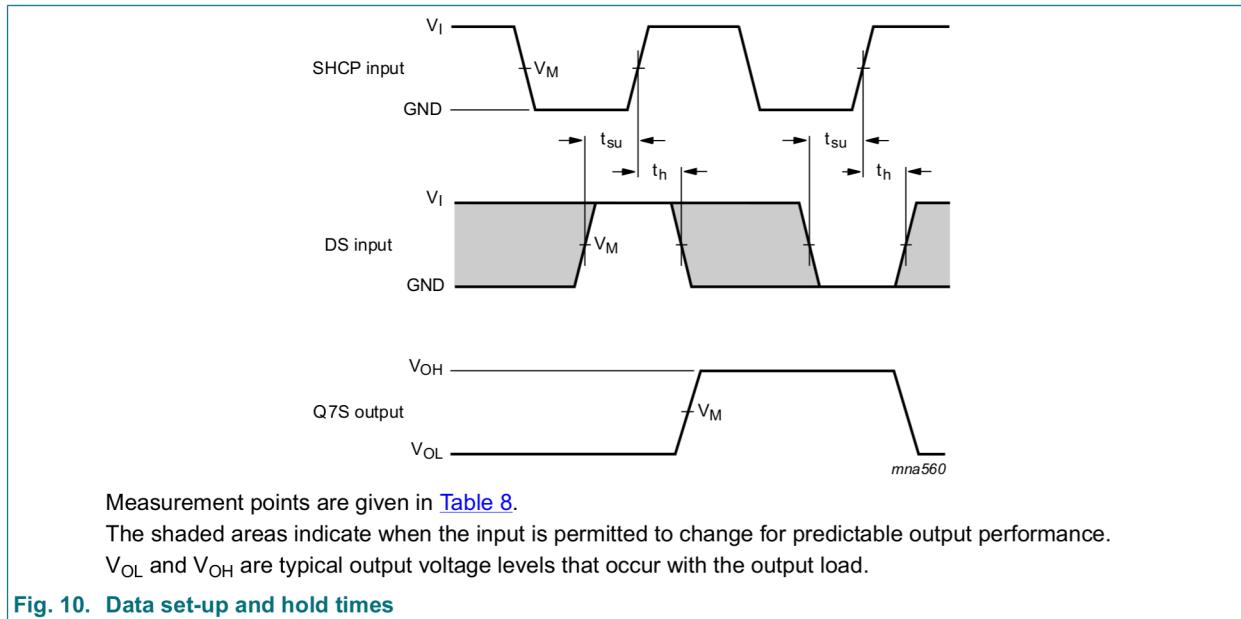
**Fig. 8. Shift clock pulse, maximum frequency and input to output propagation delays**

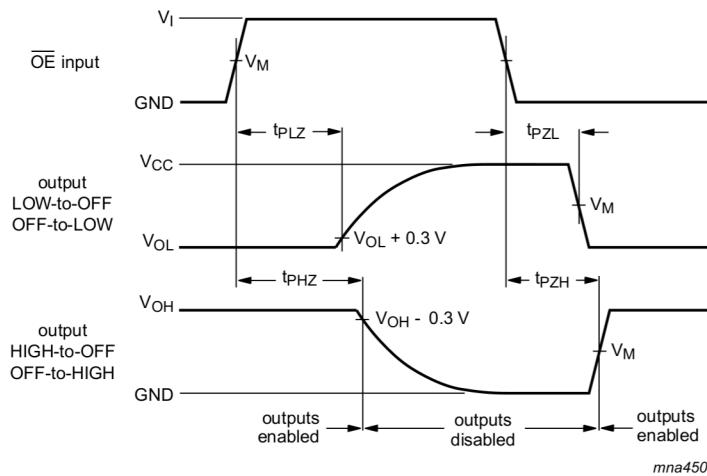


Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 9. Storage clock to output propagation delays**





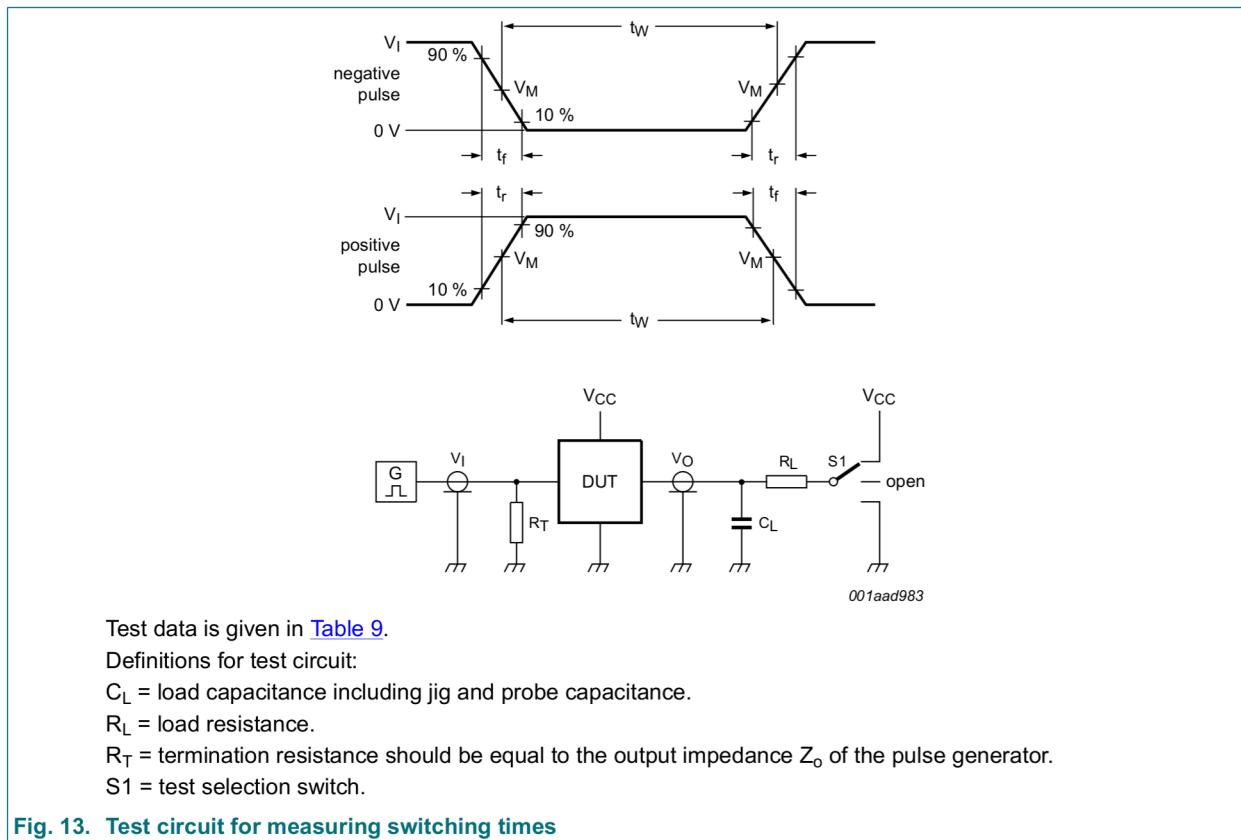
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 12. Enable and disable times**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74VHC595	$0.5V_{CC}$	$0.5V_{CC}$
74VHCT595	1.5 V	$0.5V_{CC}$

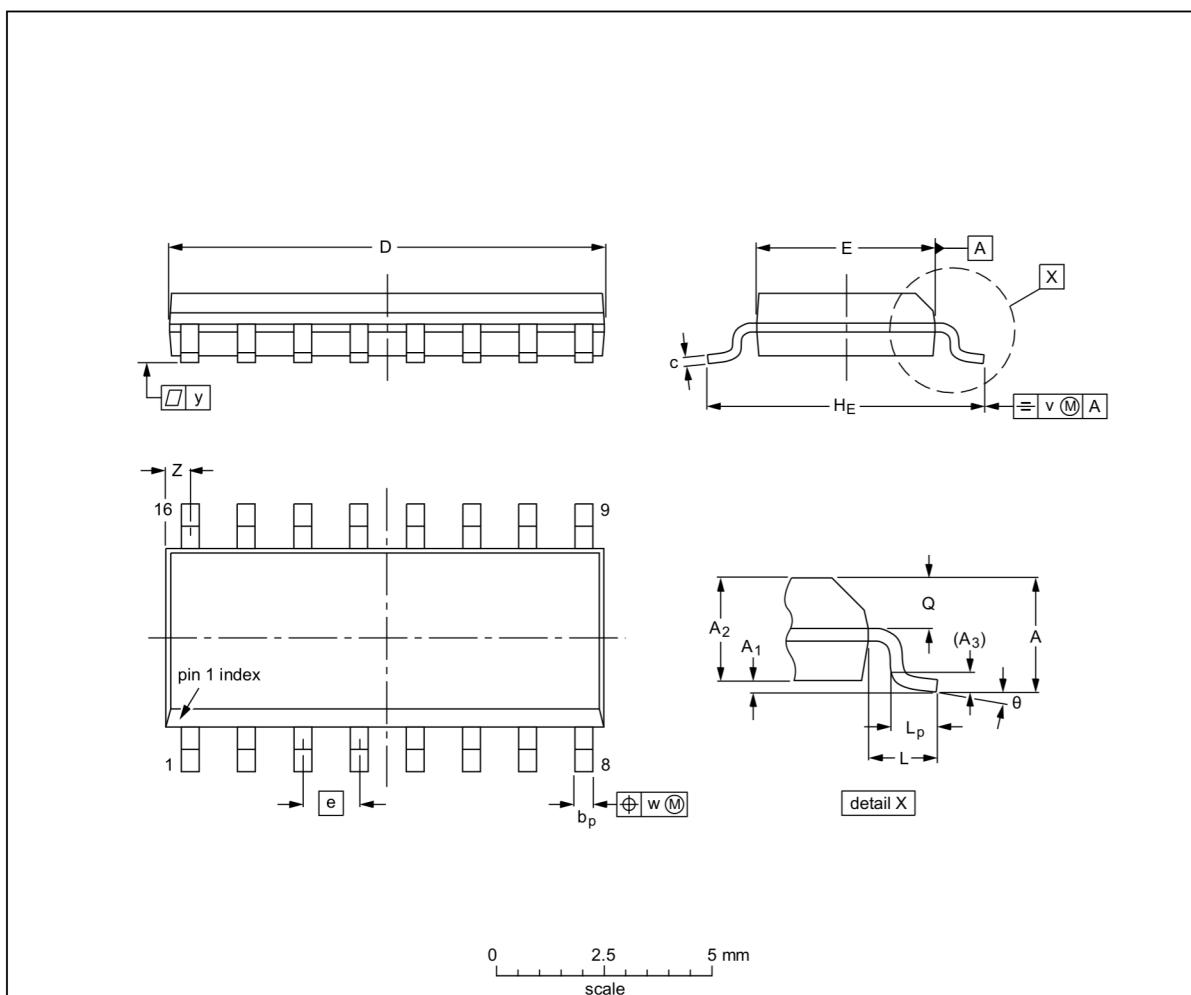
**Table 9. Test data**

Type	Input		Load		S1 position		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
74VHC595	$V_{CC}$	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$
74VHCT595	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	1 k $\Omega$	open	GND	$V_{CC}$

## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75 0.10	0.25 1.25	1.45 0.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

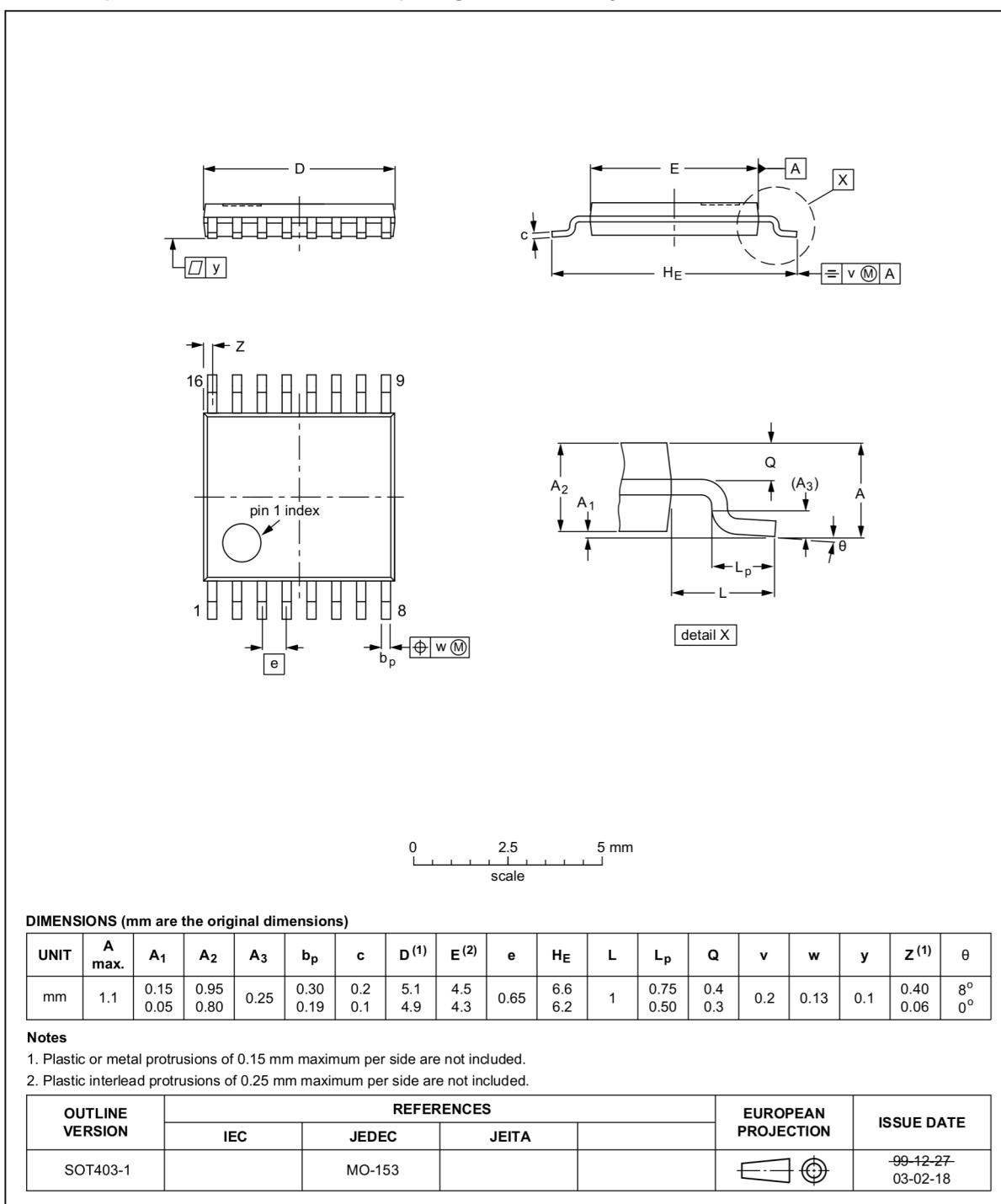


Fig. 15. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;  
16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

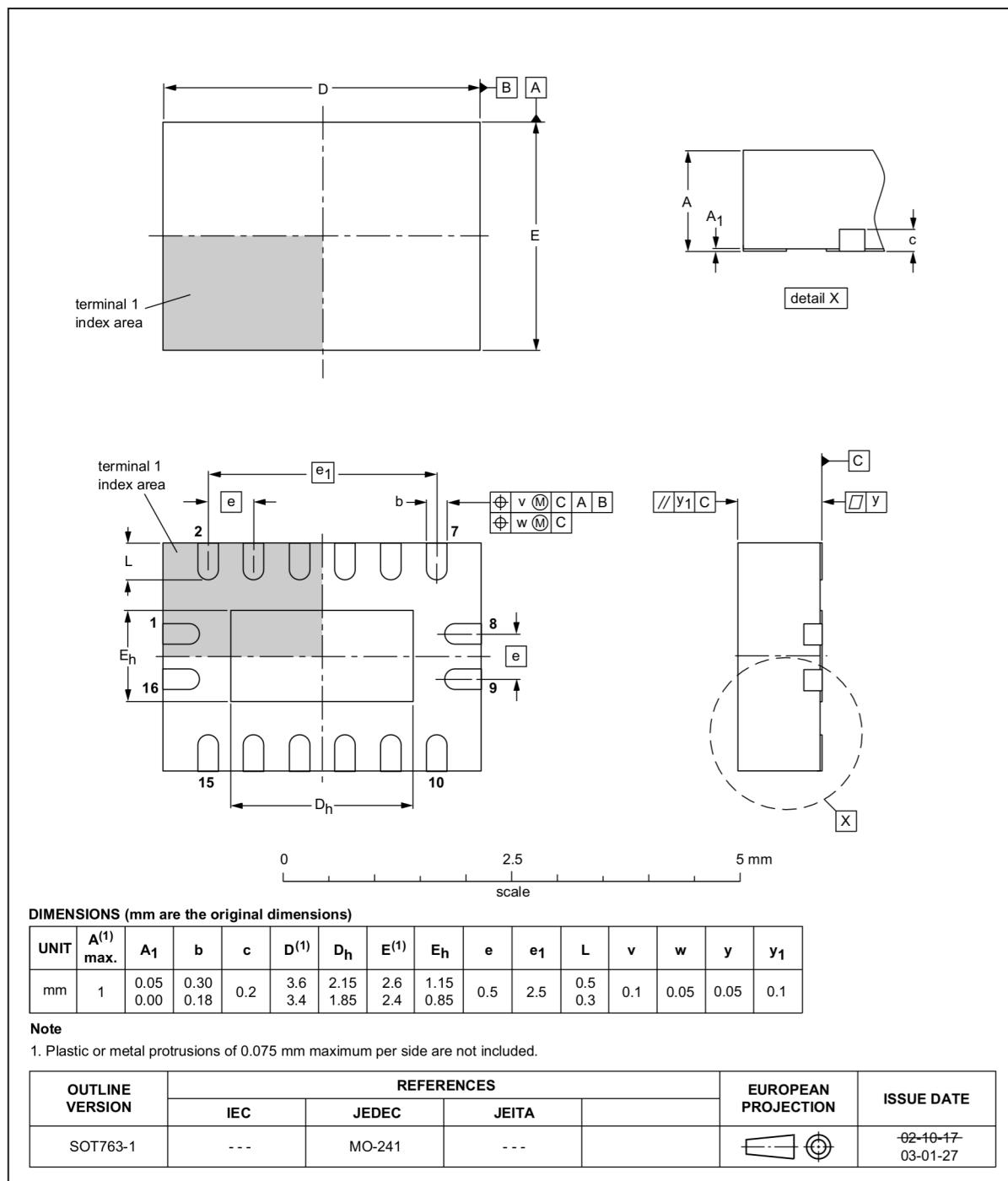


Fig. 16. Package outline SOT763-1 (DHVQFN16)

## 13. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74VHC_VHCT595 v.3	20200625	Product data sheet	-	74VHC_VHCT595 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Fig. 7</a>: updated (SHCP waveform added).</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Table 6</a>: Conditions for <math>I_{OZ}</math> corrected.</li> </ul>			
74VHC_VHCT595 v.2	20120704	Product data sheet	-	74VHC_VHCT595 v.1
Modifications:	<ul style="list-style-type: none"> <li>Added GND in the pin configuration drawing DHVQFN16 (errata)</li> </ul>			
74VHC_VHCT595 v.1	20090811	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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