Metrological Characterization of a PMU Calibrator in the 25 Hz to 3 kHz Range

Daniele Colangelo, Dennis Hoogenboom,
Erik Dierikx and Gert Rietveld
Dutch National Metrology Institute (VSL)
Thijsseweg 11, 2629 JA Delft, The Netherlands
dcolangelo@vsl.nl

Guglielmo Frigo
University of Padua, Padua
frigogug@dei.unipd.it

***Abstract*—The calibration of phasor measurement units (PMUs) and the improvement of the associated normative documents are key points to support the deployment of such devices in the electricity network, especially at the distribution level. In general, the nodal voltage phasors of distribution networks (DNs) are separated by angles that are close to the limits imposed by the current IEEE Standard C37.118-2011 (IEEE Std). Consequently, the metrological characterization of PMUs operating at distribution level is still an open issue and the IEEE Std is not in line with the needs of DN applications. In this paper, we describe the metrological characterization of a PMU calibrator currently being developed at the Dutch National Metrology Institute (VSL). This calibrator can reproduce the static tests of the current IEEE Std with uncertainties way below the actual limits in the IEEE Std. In the current paper, we describe the characterization of the voltage chain of the proposed calibrator and we report the preliminary results.**

***Index Terms*—Phasor Measurement Unit (PMU), PMU calibrator, distribution networks, IEEE C37.118.**

I. Introduction

The rapid evolution of the distribution network from a passive to an active infrastructure, due to the penetration of renewable energy sources (RESs) and distributed generation units, requires a frequent knowledge of the state of system [1] to operate and control the network. In this context, Phasor Measurement Units (PMUs) could play an essential role. Typical DN applications using PMUs include energy flow monitoring, fault location analysis, remote voltage control, and optimal dispatch of RESs [2]–[5]. The IEEE Standard C37.118.1-2011 (henceforth called IEEE Std) for synchrophasor measurements for power systems [6], and its recent amendment [7], defines the performance requirements for PMUs in terms of the total vector error (TVE), frequency error (FE), and rate-of-change-of-frequency (ROCOF) error (RFE). However, the current IEEE Std, which limits the TVE to 1% (phase error of 0.57 degree in a 50 Hz grid with null magnitude error or a magnitude error of 1% with null phase error) is, in general, suitable for transmission network (TN) applications and does not completely reflect the needs of distribution networks (DNs). In general, DNs are characterized by a radial (or weakly meshed) structure with a high number of nodes and relatively short and dominantly resistive lines. Moreover, active DNs often include a large number of highly volatile active RESs and unbalanced loads. Consequently, these grids might have fast dynamics, which the PMUs must follow, and the angle differences of the nodal voltage phasors are way below the limits imposed by the IEEE Std. Therefore, the extension of PMUs in DNs requires, in general, levels of accuracy more stringent of those defined by the IEEE Std, and push PMU manufacturers to develop more accurate devices. From a metrological point of view, the deployment of PMUs in DNs challenges national metrology institutes and research centers on the calibration of such measurement devices [8]–[11]. In continuation with previous studies [12], [13], the Dutch National Metrology Institute (VSL) has developed a PMU calibrator that is able to perform the metrological assessment of commercial PMUs under static conditions traceable to Dutch coordinated universal time (UTC(VSL)) and AC reference standards. The aim of this paper is twofold: we report the latest improvement on a proposed PMU calibrator and we describe the specific techniques used to characterize the frequency response of the calibrator with particular emphasis on the voltage chain. The VSL calibrator is a full three-phase system that can reproduce the static tests defined in the current IEEE Std with high accuracy both in voltage and current. We provide in Section II an overview of the proposed PMU calibrator. In Section III, we describe the methods used to perform the metrological characterization of the voltage path of the calibrator in the 25 Hz to 3 kHz range, and we report the preliminary results in term of on magnitude, phase, frequency and the timing error assessment. In the final Section, we provide some concluding remarks and we discuss the future steps of this research.

The research leading to the results described in this paper is part of the European Metrology Research Program (EMRP), which is jointly funded by the EMRP participating countries within EURAMET and the European Union.

II. Overview of the PMU Calibrator

A. Functionalities of the PMU calibrator

The structure of PMU calibrators nowadays is essentially consolidated [8]–[11]. The PMU calibrator proposed by VSL consists of a generation path that provides the test signals defined by the current IEEE Std to the device under test (DUT), and an acquisition path that accurately measures the test signals and defines the reference synchrophasors (see Fig.

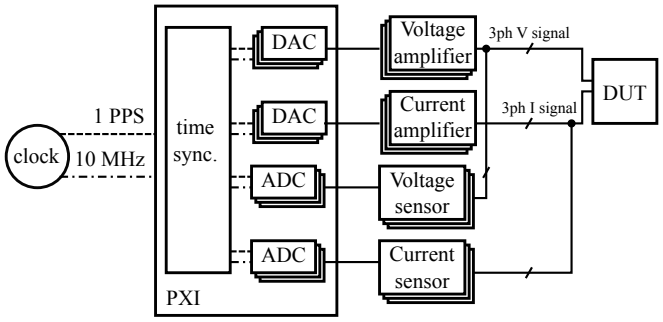

Fig. 1. Hardware architecture of the proposed PMU calibrator.

1). In particular, the basic functionalities of a PMU calibrator are: (i) generation of voltage and current test signals as defined in the IEEE Std in a range compatible with the DUT; (ii) collection of the synchrophasors streamed out by the DUT; (iii) acquisition of the test signals and definition of the reference synchrophasors; (iv) assessment of TVE, FE and RFE and latency time of the DUT.

B. Hardware of the PMU calibrator

We derive directly from UTC(VSL), the official time in the Netherlands, a 10 MHz signal and a pulse-per-second (PPS) signal. We use the 10 MHz signal to override the original clock of a National Instruments (NI) PXI (PCI eXtensions for Instrumentation) 1042Q chassis which represents the core of the calibrator. The 1042Q chassis supplies the 10 MHz signal to the peripheral slots of the PXI with a skew of less than 250 ps [14]. We can then assume all modules on the PXI platform synchronized to the 10 MHz of UTC(VSL). On the PXI platform, a NI PXI-6683H timing and synchronization module is present. The timing module manages the pulse-per-second (PPS) of the UTC(VSL) (VSL-PPS) that is used to trigger the software operations of the calibrator. We generate the test signals using six digital-to-analog converters (DACs) of a NI PXI-6733 module. These DACs have a 16-bit resolution and a maximum output voltage of ± 10 V. We can reach the nominal voltage of 70 Vrms and the nominal current of 10 Arms using a three-phase CMS OMICRON 156 power amplifier. The DUT reports the phasors associated to the applied test signals, and simultaneously we acquire the test signals with the analog-to-digital converters (ADCs) of a PXI-6356 board. These ADCs have a 16-bit resolution over a ± 10 V range. We set the sampling rate of the ADCs to 100 kS/s. The voltage test signals generated by the amplifiers are scaled down to the ADCs input range through three voltage dividers (VDs) and the test current signals are converted to voltage using three wideband resistive shunts. The wideband resistive shunts (MU20ASIQ) have been developed and characterized in the framework of a previous project [15], [16] and, they are not analysed in the current paper. As already mentioned, in the following Sections we discuss mainly the performance and the characterization of the voltage path. The voltage dividers (VDs) have been designed and manufactured at VSL laboratories. They are compensated passive resistive dividers realized with high precision resistors with low inductance and low temperature coefficient. As at high frequency the parasitic elements of VDs and ADCs play an important role (loading effect), resulting in a change of phase and magnitude of the input signal, the compensation of the VDs takes into account the connections to the ADCs which represent the load. The nominal scaling ratio of the VDs is 1:14.

III. Characterization of the PMU Calibrator

A. Magnitude error

We assess the magnitude error (ME) of the VDs including ADCs comparing their reading with the amplifiers outputs which are directly measured using as a reference a commercial voltmeter Fluke 5790B previously characterized at VSL laboratories with an accuracy of 25 ppm up to 300 V.

1) Static nominal: As the test signals of the IEEE Std present only the fundamental tone [6] plus wide-band noises, we can directly calculate the ratio of the VDs dividing the output of the Fluke 5790B by the post-process outcome of the time-series acquired by the ADCs. The Fluke 5790B provides a measurement each second and we process the time-series acquired by the ADCs using an interpolated discrete-Fourier transform (IpDFT) algorithm with a sampling windows of 1 s using Hann window. It is worth mentioning that IpDFT-based algorithms can show critical behaviour in the presence of added out-of-band components closed to the fundamental one [17]. However, as we characterize the hardware analysing sequences of single harmonics using relative long sampling windows (minimum 1 s), we can consider the error introduced by the algorithm negligible. In particular, we characterize voltage signals for each harmonic component in the 25 Hz to 3 kHz range. We vary the voltage of the calibrator in the 7 to 84 Vrms range to verify the input voltage magnitude dependence of the VDs. Figure 2 shows the relative difference of the ratio

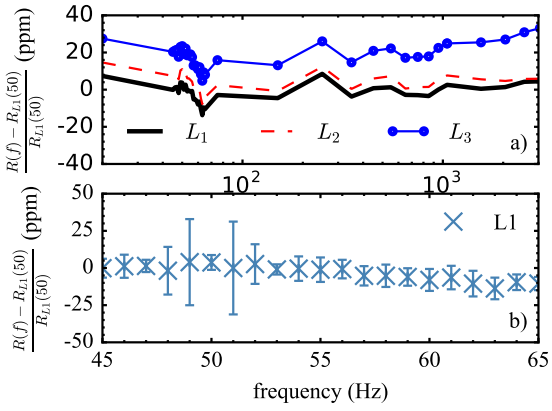

Fig. 2. Voltage magnitude error of the VDs plus ADCs. Relative deviations of L1, L2 and L3 as a function of frequency at 70 V. The values are referred to phase L1 at 50 Hz.

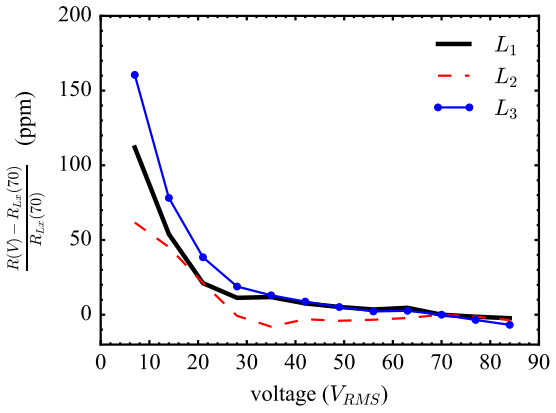

Fig. 3. Relative magnitude deviation of the L1, L2 and L3 voltage chain ratio at 50 Hz as a function of the input voltage, referred to the value at 70 V.

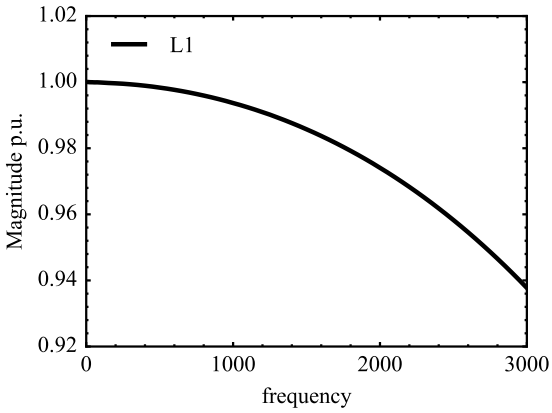

Fig. 4. Magnitude response of L1 of the voltage amplifier up to 3 kHz. At 3 kHz the voltage signal is circa 6% attenuated.

(R) of the three VDs using as a reference the ratio of the first voltage line 1 at 50 Hz ($R_{L1}(50)$). In the 25 Hz to 3 kHz range, the average relative deviation of the three voltage lines is within 30 ppm at nominal voltage (Fig. 2a). As shown in Fig. 2b (only L1 is shown), the type A spread in a single measurement is around 25 ppm. At low voltage the three lines show a non-negligible deviation (Fig. 3). Indeed, the ADCs work in a not optimal range (input range of ADCs is fixed to 10 V). At low voltage (10% of nominal voltage), we can, in principle, circumnavigate the problem operating the calibrator without power amplifiers and VDs. The voltage test signals can be provided to the PMU under test directly using the DACs. In the PMU calibrator software, we compensate the deviation of the three voltage lines from their nominal 1:14 ratio using the measured ratio at 50 Hz at nominal voltage. As a consequence, in a first approximation the expanded combined uncertainty on the ME reference measurements is around 50 ppm at nominal voltage.

2) Harmonic distortion and out of bands: For tests with harmonic distortion and out of band signals, we add to the fundamental tone a single interfering component in the 25 Hz to 3 kHz range [6]. According to the IEEE Std, the magnitude of this interfering component should be 10% of the magnitude of the fundamental component. At high frequency, the amplifiers present a non-flat magnitude frequency response (Fig. 4). However, as we have characterized the acquisition path, we adjust the applied amplitude of the harmonic or out-of-band components according to the actual measured values.

B. Timing error

Commercial PMUs are, in general, GPS synchronized. A typical, GPS uncertainty, referenced to UTC, is about 100 ns. This suggests a typical timing error (TE) uncertainty which gives a contribution to the overall phase error in the order of 30 μrad at 50 Hz. As already mentioned, the proposed calibrator uses directly the UTC(VSL) (10 MHz and PPS) as a time source and trigger line. The major contribution to the TE uncertainty in the reference measurement is then due to the internal circuitry of the PXI and the wiring. We characterize the TE comparing the PPS routed out from the PXI (PXI-PPS), which is used as a trigger in the generation and acquisition stage of the calibrator, and the PPS of the UTC(VSL) (VSL-PPS), using a commercial frequency counter SR620. We override the 10 MHz clock of the SR620 with the UTC(VSL) one. When synchronized to UTC(VSL), in time interval mode, the SR620 has an uncertainty of about 25 ps. In order to ensure a stable synchronization of the PXI, we started recording the TE after 48 hours of operation. Figure 5 shows the TE obtained during a 5 days measurement. The average delay is about 54 ns with a type A experimental standard deviation of 70 ps. In the context of PMU calibration, after correction of the measured delay, the residual TE can be considered negligible.

C. Phase error

As shown in the previous Section, we can consider the contribution of TE of the trigger signals within the PXI unit negligible. As a consequence, the phase error (PE) on

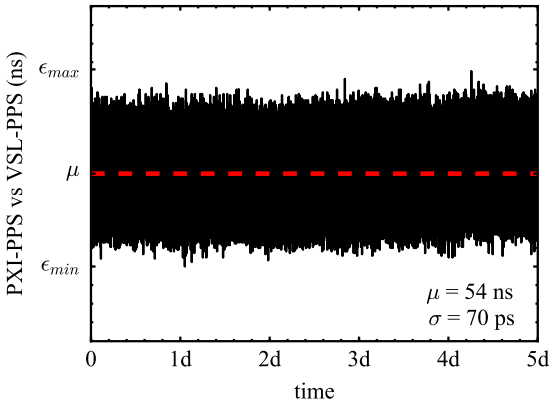

Fig. 5. Comparison between PPS derived from UTC(VSL) (VSL-PPS) and PPS route-out from the PMU calibrator (PXI-PPS).

the reference test signals, in our specific application, is only caused by the delays introduced by the hardware components. In order to determine the PE of the test signals, we need to characterize the phase lags of voltage dividers, as well as delays in the ADCs acquiring the applied test signals. This will be outlined first and followed by the estimation of the initial phase error.

1) Voltage dividers: The VDs have been designed to compensate loading effects both in magnitude and especially in phase. We can determine the phase response of the VDs taking into account the effect of the ADCs implementing the technique here described [18]. The technique consists of two stages: first, we use a calibrated voltage transformer (VT) as a reference at 50 Hz (Fig. 6a) and nominal voltage. The VT has been previously calibrated at VSL up to 150 V in magnitude and phase. In particular, the expanded uncertainty on the phase is 6 μrad. The technique compares the output of two ADCs: the VD is connected to the first ADC and the second ADC is connected to the VT output. We provide the input voltage (Vin) of a single VD using directly the OMICRON amplifier as an AC voltage source and setting Vin to 70 Vrms. We applying, on a sampling window of 1 s the IpDFT algorithm, on the readings of the two ADCs. The two ADCs are both synchronized to the 10 MHz of the UTC(VSL) signal and they share the same trigger. Afterwards, we compute the relative phase difference between the two channels which gives the response of the system at 50 Hz. Two sets of measurements are actually needed to calculate the relative phase difference [18]: a direct measurement where the VD under test is connected to ADC_1 and VT is connected to ADC_2; and an inverse measurement where the VD under test feeds ADC_2 and ADC_1 represents now the load of VT. After simple mathematical manipulation of the direct phase measurement (φ_d) and inverse phase measurement (φ_i) we can get the following system of equations

$$\begin{cases} \varphi_{d1} - \varphi_{d2} = \varphi_{VD} - \varphi_{VT} + \varepsilon \\ \varphi_{i2} - \varphi_{i1} = \varphi_{VT} - \varphi_{VD} + \varepsilon \end{cases} \quad (1)$$

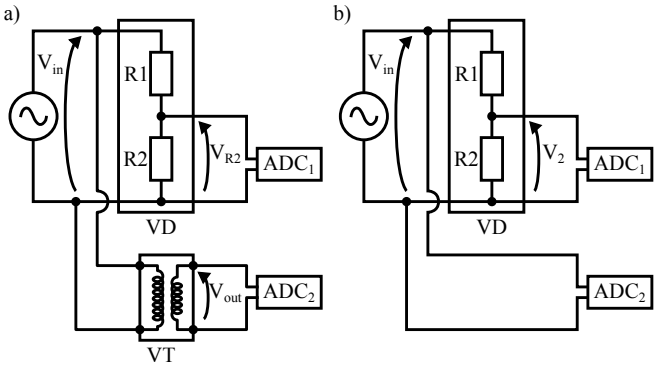

Fig. 6. Schematics of the two stages characterization of the voltage dividers. Characterization at nominal voltage (a) and frequency extension (b).

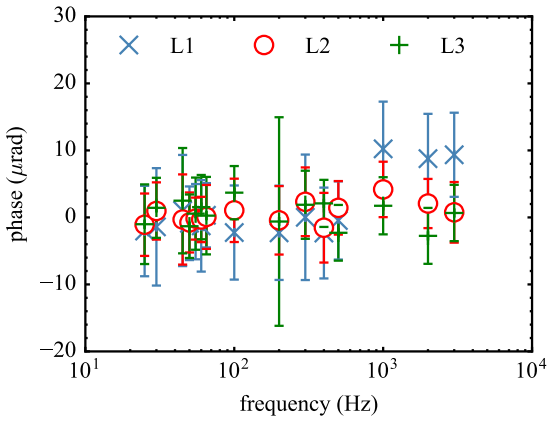

Fig. 7. Phase error characterization of the designed voltage dividers in the 25 Hz to 3 kHz range. The uncertainty bars indicate the experimental standard uncertainty in the single readings taken for determining the average.

where φ_{d1}, φ_{d2} represent the direct phase measurement made on samples acquired by ADC_1 and the direct phase measurement using samples acquired by ADC_2, respectively. Similarly, φ_{VD}, φ_{VT}, ε stand for the contribution of the voltage divider, the contribution of the voltage transformer and the error of the measurement system, respectively. As φ_{VT} is known, from this set of equations it is possible to directly determine φ_{VD} at 50 Hz and nominal applied voltage. The average value of φ_{VD} at 50 Hz and nominal voltage is 4 μrad with a experimental standard deviation of 10 μrad. In a second step, as shown in Fig. 6b, we apply the same technique for verifying the frequency dependence by removing the calibrated VT and connecting directly one ADC to the common voltage source which is now set to 5 Vrms. In particular, we vary the frequency of the voltage source from 25 Hz to 3 kHz and we compute the phase difference measured by the two ADCs as in the previous stage. In the 25 Hz to 3 kHz range, the VDs show an essentially flat characteristic with a maximum deviation of circa 10 μrad and an estimated standard uncertainty of less than 20 μrad (Fig. 7). Then, we can scale the phase response to the nominal voltage using the measurements obtained with the VT as a reference, assuming that the frequency dependence of the VDs is not voltage dependent. Even though the current paper reports the overall phase characterization of the voltage lines, the method can be similarly applied to the current path.

2) ADC phase error: In order to characterize the phase error (PE) of the ADCs in the PMU calibrator, we implement the method illustrated in Fig. 8. In a first moment, we acquire with the ADCs a VSL-PPS using a sampling frequency of 1 MS/s. The VSL-PPS (through the PXI chassis) triggers the acquisition of the ADCs as in a normal PMU calibration tests. Afterwards, we generate a sine waveform with a single DAC varying the frequency in the 50 Hz to 1 kHz range, and we applied the signal to the ADCs now working at th nominal sampling frequency of the calibrator (100 kS/s). In post-process, we calculate the trigger time (t_{ref}) analysing the acquired VSL-PPS signals and we estimate the zero-

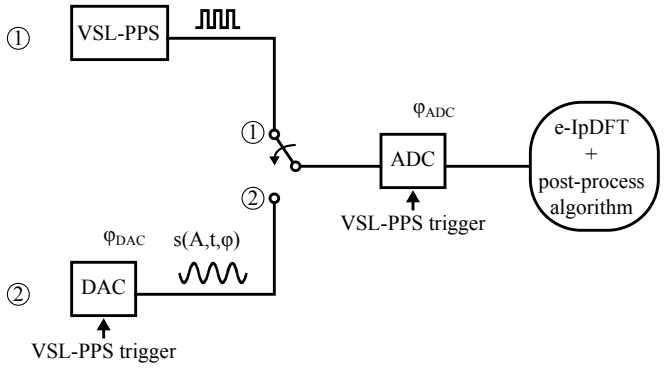

Fig. 8. Phase error characterization of the ADCs in the PMU calibrator.

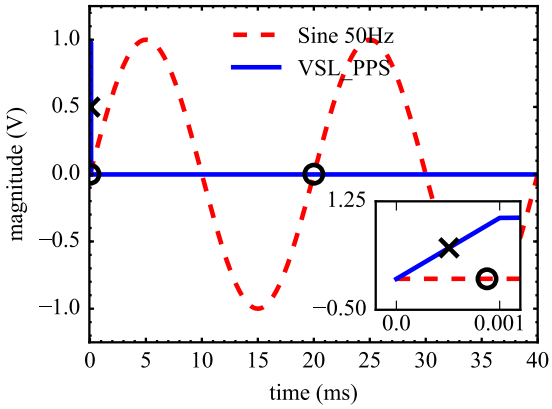

Fig. 9. Zero-crossing comparison between VSL(PPS) and s-f0.

crossing points of the sine waveforms. In particular, for the VSL-PPS we set the threshold to 50% the maximum value, and we calculate t_{ref} interpolating the nearest samples in the neighbourhood of the threshold (cross marker in 9). As we deal with a PPS, additive noise and signal offset do not signification influence the calculation of t_{ref}. In the other hand, we filter the sine waveform extracting the fundamental tone of the signal using the e-IpDFT algorithm on 1 s windows, and then reconstructing its fundamental component (s-f0) in the time domain. As with the VSL-PPS signal, we assess the time delay of the generation stage plus the one introduced by the ADCs ($t_{DAC+ADC}$) calculating the zero-crossing points of s-f0 (cross markers in 9). Even if, more complex models are feasible (e.g. cubic splines), around zero, where the sinusoidal waveform presents an almost-linear trend, a linear approximation is suitable. The difference between $t_{DAC+ADC}$ and t_{ref} gives the time delay of the generation stage which can be easily converted in phase domain (φ_{DAC}). As a consequence, the phase lag introduced by the ADCs comes as the difference between $\varphi_{DAC+ADC}$ and φ_{DAC}. In particulate, at 50 Hz, the phase lag of the ADCs is about 160 μrad (Fig. 10). The reproducibility of the measurements relies on the synchronization of the system, which is guarantee by the fact the PXI is lock to the 10 MHz of the UTC(VSL). The uncertainty on the ADCs phase is fully dominated by the limited sampling frequency used for the acquisition of VSL-PPS. In fact, the sampling frequency introduces an uncertainty equal to half of the time step (1 μs) which, in phase domain, corresponds to circa 157 μrad at 50 Hz. An higher sampling frequency will lead to a lower uncertainty on the ADCs phase estimation. This could be achieved acquiring the waveforms with a high-performance oscilloscope. Considering both the contributions of the ADCs and the VDs, a rough estimation of the total PE shows that the uncertainty is fully dominated by systematic effects in the ADCs delay measurements. As a consequence, further investigations on the systematic effects in the ADC phase delay determination need to be performed. This is part of our present research program. The target overall phase error is less than 200 μrad.

D. Frequency error and rate-of-change-of-frequency error

We assess the frequency error (FE) comparing the output of the PMU calibrator against a calibrated SRS SR620 reference frequency meter. The SR620 is locked to the 10 MHz of the UTC(VSL). We generate a continuous signal at nominal voltage which is scaled down by VDs and analysed by the SR620 in frequency mode with a gate time of 5 s. The SR620 has a resolution of 1 μHz and an uncertainty of 250 nHz [19]. As for the static tests of the IEEE Std, the maximum distortion caused by harmonics and Interharmonics is limited to 10%, we can apply the method for the whole set of static tests defined in the IEEE Std. In Fig. 11, we report the frequency deviation between the measured and the theoretical frequency. For the sake of simplicity, we limit the analysis in the 45 to 65 range for the static nominal test (Fig. 11a). The deviation between the ideal frequency (f_T) and the measurement one (f_M) is well within 1 μHz with a type A uncertainty of 0.5 μHz. Figure 11b shows the results when a harmonic component of rank k is added to the fundamental frequency of 50 Hz and 60 Hz (only the result on the first ten rank are shown). In

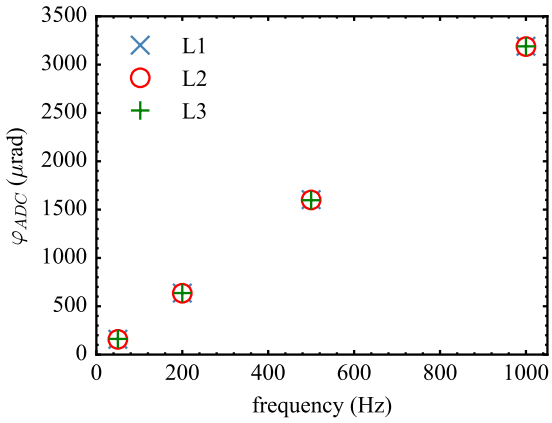

Fig. 10. Preliminary results of the phase error contribution of the ADCs voltage chain in the 50 Hz to 1000 Hz range.

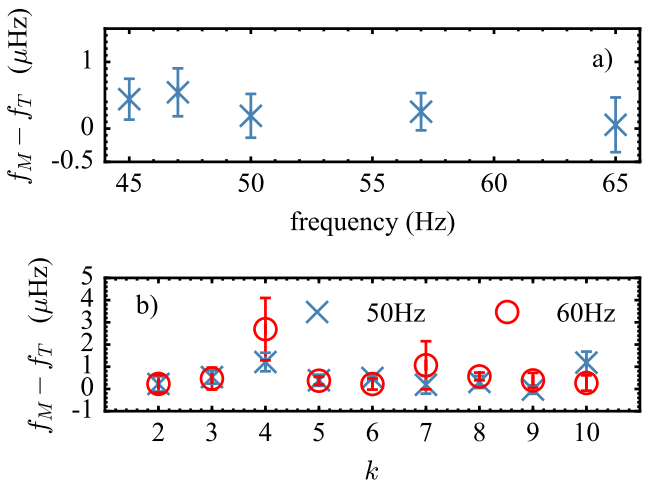

Fig. 11. Comparison between calibrator output (fM) and ideal frequency (fT) in case of static nominal (a) and with a single added harmonic distortion (b) of rank k.

this case, the maximum deviation of f_M is less than 3 μHz with a type A standard uncertainty of 1 μHz. The preliminary assessment of FE is around a few μHz both for static nominal and harmonic/out-of-band conditions. In static conditions, the RFE of the calibrator coincides with its ROCOF estimation. Therefore, we can compute the ROCOF as the difference between two consecutive frequency estimates, normalized by the reporting time (e.g. 20 ms). As a consequence, the RFE results much lower than the 200 mHz/s limit imposed by the IEEE Std.

IV. Conclusions

The scope of the paper is to describe the metrological characterization of the PMU calibrator presently under development at VSL laboratories. In particular, we present an extensive metrological characterization of the voltage path of the calibration as a function of frequency. First, we compare the output of the calibrator against a commercial voltmeter Fluke 5790B previously characterize again AC standard with an uncertainty of 25 ppm. In a first approximation, the magnitude error of the PMU calibrator results less than 50 ppm at nominal voltage. Second, we compare the PPS used as a trigger in the generation and acquisition operation of the calibrator against the VSL-PPS. We estimate a deviation to UTC(VSL) in the order of 54 ns with a timing error that can be consider negligible in the contest of PMU calibration. In the last part of the paper, we report the characterization of the relative phase error contribution of the voltage dividers, and the delay introduced by ADCs referred to UTC(VSL). This preliminary characterization show that the PE might be dominated by systematic effect on the ADCs delay characterization. The expect overall phase error is 200 μrad. In order to compare the proposed calibrator with the existing ones, we estimate the TVE in static nominal conditions around 0.02%. This figure is in line with the most advanced PMU calibrator developed by NIST and METAS. However, in order to confirm these preliminary results, further analysis needs to be performed. The future work concerns: (i) the analysis of the systematic effects on the ADCs delay measurements; (ii) a rigorous uncertainty budget to exactly estimate the minimum TVE both for voltage and current path; (iii) the extension of the system to dynamic tests of the IEEE Std; (iv) implementation of an automatic PMU characterization protocol.

References

[1] A. Gómez-Expósito, A. Abur, A. de la Villa Jaén and C. Gómez-Quiles, "A multilevel state estimation paradigm for smart grids," *Proc. 2011 IEEE*, vol. 99, no. 6, pp. 125.

[2] G. Sanchez-Ayala, J. R. Aguerc, D. Elizondo and M. Dino Lelic, "Current trends on applications of PMUs in distribution systems," *Proc. 2013 IEEE Power & Energy Society Conference on Innovative Smart Grid Technologies (ISGT 2013)*, pp.1-6.

[3] J. De La Ree, V. Centeno, J.S. Thorp, and A.G. Phadke, "Synchronized phasor measurement applications in power systems," *IEEE Trans. Smart Grid*, vol. 1, no. 1, pp. 2027, 2010.

[4] J. A. Jiang, J. Z. Yang, Y. H. Lin, C. W. Liu and J. C. Ma, "An adaptive PMU based fault detection/location technique for transmission lines. Part I: Theory and algorithms," *IEEE Trans. Power Delivery*, vol. 15, no. 2, pp. 486-493, Apr. 2000.

[5] F. Sossan, E. Namor, R. Cherkaoui and M. Paolone, "Achieving the Dispatchability of Distribution Feeders Through Prosumers Data Driven Forecasting and Model Predictive Control of Electrochemical Storage," *IEEE Trans. Sustain. Energy*, vol. 7, no. 4, pp. 17621777, Oct. 2016.

[6] *IEEE Standard for Synchrophasor Measurements for Power Systems*, IEEE Std. C37.118.1-2011, Dec. 2011.

[7] *IEEE Standard for Synchrophasors Measurement for Power Systems, Amendment 1: Modification of Selected Performance Requirements*, IEEE C37.118.1a-2014, Apr. 2014.

[8] Y. Tang and G. N. Stenbakken, "Calibration of phasor measurement unit at NIST," *IEEE Trans. Instrum. Meas.*, vol. 62, no. 6, pp. 1417-1422, June 2013.

[9] J-P. Braun and C. Mester, "Reference Grade Calibrator for the Testing of the Dynamic Behavior of Phasor Measurement Units," *Proc. 2012 IEEE Conference on Precision Electromagnetic Measurements (CPEM 2012)*, pp. 410-411.

[10] D. Georgakopoulos and S. Quigg, "Precision Measurement System for the Calibration of Phasor Measurement Units," *CPEM 2016 Conf. Digest*, August 2016.

[11] N.T.A. NGuyen, M. Popov, and G. Rietveld, "Phasor Measurement Unit Testing in Accordance with the IEEE C37.118-2011 Synchrophasor Standard", *IPSI BgD Trans. on Internet Research*, vol. 11, no. 2, pp. 1-10, 2015.

[12] G. Frigo et al., "Definition and Assessment of Reference Values for PMU Calibration in Static and Transient Conditions," *in Proc. IEEE AMPS 2016*, pp. 120-125, Sep. 2016.

[13] D. Colangelo et al, "Architecture and characterization of a calibrator for PMUs operating in power distribution systems," *in Proc. IEEE PowerTech 2015*, pp. 16, June 2015.

[14] National Instruments Corporation 2017 [Online]. Available: http://www.ni.com

[15] B. Voljč, M. Lindič, and R. Lapuh, "Direct Measurement of AC Current by Measuring the Voltage Drop on the Coaxial Current Shunt," *IEEE Trans. Instrum. Meas.*, vol. 58, no. 4, July, 2009.

[16] G.C. Bosco et al., "Phase Comparison of High-Current Shunts up to 100 kHz," *IEEE Trans. Instrum. Meas.*, vol. 60, no. 7, July, 2011.

[17] P. Romano and M. Paolone, Enhanced Interpolated-DFT for Synchrophasor Estimation in FPGAs: Theory, Implementation, and Validation of a PMU Prototype, *IEEE Trans. Instrum. Meas.*, vol. 24, no. 63, pp. 2824-2836, Dec. 2014.

[18] B. Trinchera, D. Serazio, and U. Pogliano, Asynchronous Phase Comparator for Characterization of Devices and PMU Calibrator, *CPEM 2016 Conf. Digest*, August 2016.

[19] SRS 2016 [Online]. Available: http://www.thinksrs.com