A Digital Five-Terminal Impedance Bridge

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***Abstract*— This paper describes a five-terminal (four terminal with shield) digital impedance bridge aided by digital adaptive phase regulation. It allows the comparison of ac resistances and capacitances with outstanding accuracy and with measurement uncertainties bearing only some $10^{-6}\,\Omega/\Omega$, as corroborated by extensive experimental investigations.**

***Index Terms*— Adaptive signal processing, digital signal processing, electrical resistance measurements, electronic circuits, impedance, precision measurements, uncertainty.**

I. Introduction

PIONEER work on digital impedance bridges was done at the Physikalisch-Technische Bundesanstalt, the German national metrology institute in the 1980s by using digital double-sinewave generators [1] feeding an arm of two impedances to be compared, as illustrated schematically in Fig. 1. The bridge balance was attained by controlling the amplitude and phase shift of digitally synthesized signals. Phase shifts were attained by shifting addresses of data stored in random access memories (RAMs), whose output was directed to commercial digital-to-analog converters (DACs). Further work [2], [3] followed, still relying on the use of inductive voltage dividers to measure voltage ratios. With advances in analog-to-digital converters (ADCs), the measurement of voltage ratios was later determined by sampling digital voltmeters [4]–[6]. In [4], a two-terminal impedance bridge is described, which uses a 16-bit sampling voltmeter (phase locked to the signals generators of the bridge) to determine ac voltage ratios with a sine-fit least squares algorithm applied on sampled data, to extract amplitude and phase of the fundamental signal components.

Motivated by recent advances in time-keeping and frequency synthesis devices like direct-digital-synthesizers (DDSs), we constructed a digital impedance bridge whose balance is aided by frequency control. Our system was devised to be used in daily routine calibrations (in the resistance range of 10 Ω to 100 kΩ and capacitances of 1 nF to 1 μF). It uses the same concepts of ratiometric voltage determinations with a sampling digital voltmeter, as described in [4]–[6]. It differs though from other developments by its adaptive digital regulation of phase which is done via adaptive digital frequency control of DDSs to attain bridge balance. Phase resolution is thus not limited by the number of steps of a step approximated synthesized sine waveform stored in a RAM but by the phenomenal resolution of 48 bit of modern DDSs for frequency adjustment. Voltage ratios are measured by synchronously sampling [4] the signals with a highly linear and high-resolution 28-bit sampling voltmeter as in [5] and [6], which delivers the 10 MHz time base used for signal synthesis. This automated and versatile digital five-terminal (four-terminal plus shield) impedance bridge is an alternative to the complicated traditional bridges [7]–[9], which are indeed very accurate and stable, but are cumbersome to operate and too time consuming for daily calibration work. This paper is an extended version of [10].

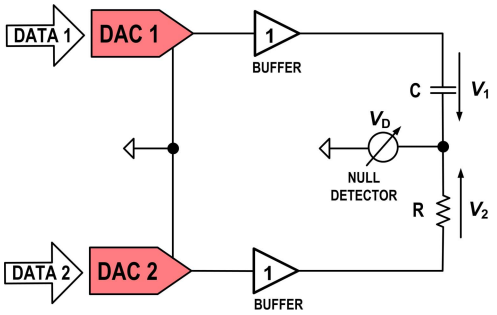

Fig. 1. Block diagram of a double-sinewave DAC based digital impedance bridge. The DAC signals V_1 and V_2 after the unitary gain buffers are amplitude- and phase-adjusted (by shifting either DATA 1 or DATA 2 in a RAM memory) to attain bridge balance (when the null detector indicates a 0 voltage V_D with respect to the ground). Voltage ratio V_1/V_2 is equal to -1 times the impedance ratio so that either a capacitance C or a resistance R can be determined if one of the impedances is previously known.

II. System Description and Implementation

The system evolved from a first approach [11] and culminated with its complete diagram as shown in Fig. 2, exemplified for the calibration of a capacitance C_X against a standard resistor R_P. Electrostatic shielding and coaxial cabling preclude coupling effects inside the bridge.

The definition of a four-terminal pair impedance standard [9] requires, as the name suggests, four inputs for C_X and R_P. In the case of Fig. 2, though, the bridge is not strictly coaxial, and the currents at the low terminals I_{XL} and I_{PL} do not flow back through the case of the standards as stated in [9]. (It is thus of five terminals.) This, however, does not invalidate the bridge. The unity-gain field effect transistor (FET) buffer amplifiers A5 and A6 ensure that the potentials $V_{XL} = V_{XS}$ and $V_{PL} = V_{PS}$, approaching the definition of four-terminal pair impedances.

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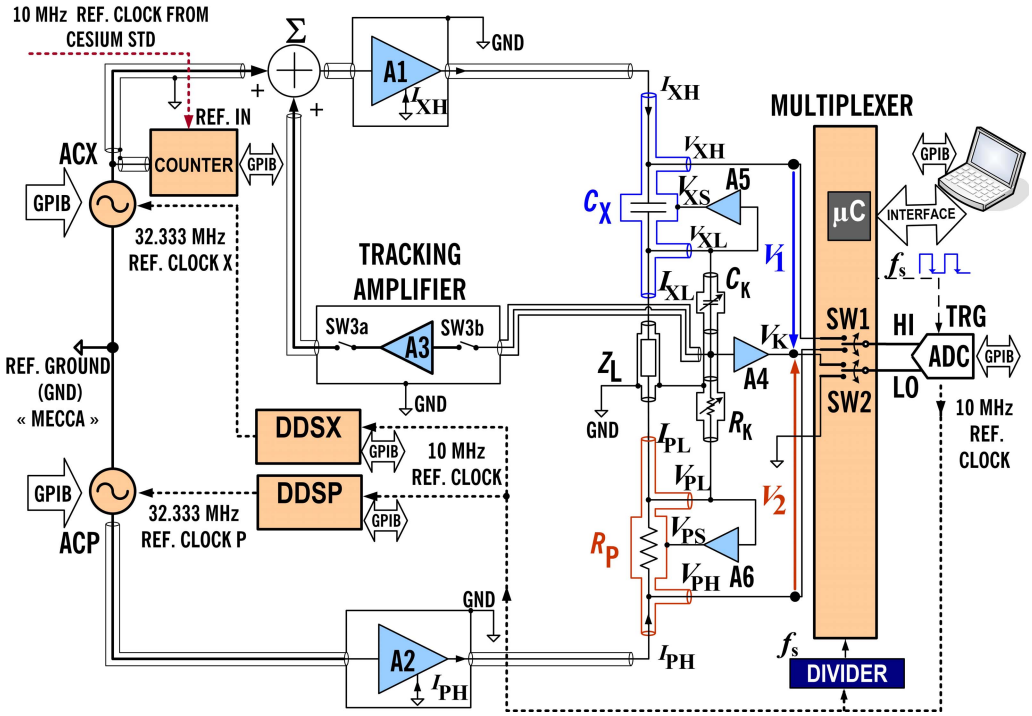

Fig. 2. Complete diagram of the digital ac impedance bridge.

The low-noise unity-gain buffer amplifiers A1 and A2, respectively, (of typically 5 nV/Hz$^{1/2}$ and with output impedance smaller than 0.01 Ω at 1592 Hz) supply the main arm $C_X R_P$. A coaxial cable of some centimeters in length and of impedance Z_L provides the electrical connection of both standards to be compared. In equilibrium, V_{XH} is nearly 90° out of phase with respect to V_{PH}, and the sum of I_{XL} and I_{PL} tends to 0. Although Z_L is small, it is not negligible, so the voltages V_{XL} and V_{PL} do not vanish, remaining within some tens to hundreds of microvolts, depending on the quality of amplitude and phase adjustments of ACX and ACP sources, which are high-grade audio sine wave generators with high amplitude stability and ultralow harmonic distortion (below −110 dBc), as detailed in Section III.

C_K and R_K build up a Kelvin arm to compensate for the voltage difference between V_{XL} and V_{PL} due to Z_L. This is best attained when the time constant $R_K C_K$ is made equal to $R_P C_X$, resulting in a feeble voltage signal V_K at the junction joining R_K and C_K. A unity-gain FET buffer amplifier A4 (Kelvin amplifier) precludes impedance loading of the connection between R_K and C_K. Nearly, perfect compensation due to Z_L is attained by sampling the differential voltages $V_1 = V_{XH} - V_K$ and $V_2 = V_{PH} - V_K$.

The multiplexer is interfaced to a PC and controls the analog parts of the bridge via optocouplers. Direct sampling is done with switch SW1 multiplexing synchronously between V_{XH} and V_{PH} (with respect to a Mecca ground GND) over M integer positive periods and triggering the ADC to acquire N samples per period with SW2 switched to GND. The connections to the multiplex are also shielded (not shown in Fig. 2 for the sake of simplicity and clarity). Relays representing SW1 and SW2 to the ADC are of very low capacitance between contacts and shielded to reduce crosstalk and stray coupling. Coaxial cables with shield tied to ground lead the signals to the ADC. The differential sampling of voltages V_1 and V_2 with respect to V_K is done via switch SW2 with SW1 multiplexing the ADC's HI (high) terminal between signals V_{XH} and V_{PH}. The direct and differential sampling serves different purposes. The direct sampling is used to phase-align the ac sources ACX and ACP by software to balance the bridge ($V_K \approx 0$). The differential sampled data of V_1 and V_2 are fast Fourier transformed (FFT) and used to calculate a complex ratio $(A + jB) =$ {FFT of the data vector of V_1 samples}/{FFT of the data vector of V_2 samples} at the angular frequency $\omega = 2\pi f \approx 1/(C_X R)$, for $j = (-1)^{1/2}$ and $R_P = R(1 + j\omega\tau)$. The constant τ stands for the time-constant of R_P and R for its dc resistance. The equations for computing C_X and its "tan δ" or dissipation factor D_X or an unknown resistor R_X and its time constant τ_X are stated in [5] and [6], which can easily be derived by inspection.

A preliminary balance is done by adjusting ACX in magnitude and phase (aided by a digital phase regulator) to attain equilibrium ($V_K \approx 0$) with calculated values of phase and amplitude of ACX starting with nominal values of the elements for a given amplitude of ACP as a first guess. Subsequent balances can be made by iteration with the algorithm downhill simplex [12]. However, if the FET tracking amplifier A3 (see Fig. 1) is engaged, soon after the first phase alignment of the signals takes place by repeated calculation as in [13], the balancing algorithm is disabled (i.e., no further time-consuming iterations occur), and ratio determinations of

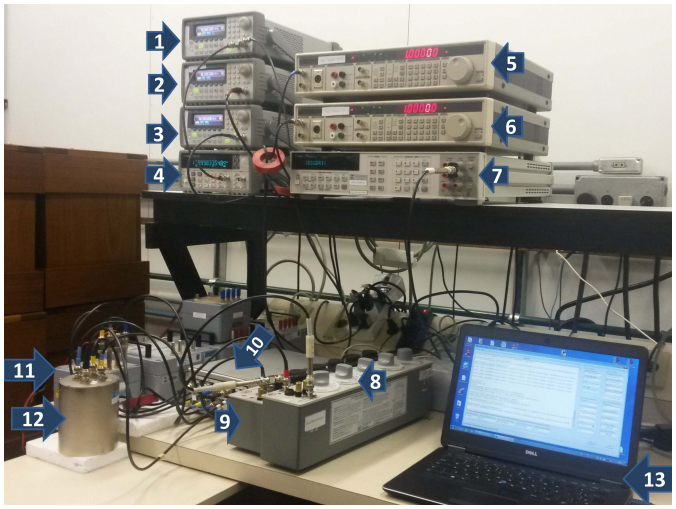

Fig. 3. Components of the bridge: (1) DDS based generator of the sampling frequency f_S from the 10 MHz of the sampling voltmeter. (2) DDS based generator for phase locking ACX with a 32.333 MHz reference clock. (3) DDS based generator for phase locking ACP with 32.333 MHz. (4) Counter tied to a cesium 10 MHz time standard. (5) ACX source, a Stanford Research model DS360[1] audio generator. (6) ACP source, a second DS360[1] generator. (7) Keysight sampling voltmeter model 3458A.[1] (8) C_K capacitance decade. (9) R_K resistance decade. (10) Multiplexer containing all amplifiers, microcontroller, and relays. (11) Capacitance standard C_X. (12) AC resistance standard R_P. (13) Notebook for automating the measurements.

A and B take some seconds only, what considerably speeds up measurements (compared with the time of nearly 10 min if balance is done by the downhill simplex algorithm alone). The tracking amplifier, as the name suggests, promotes "voltage tracking in amplitude and phase" between the two ac sources to counteract voltage fluctuations of either ACX or ACP due to their inherent amplitude instability over time (see further details at item A below). Amplifier A3 has a high negative gain and is engaged through switch SW3 (i.e., SW3a and SW3b controlled by the PC via the multiplexer) closing a negative feedback loop. It allows high accuracy and precision to be attained, even when working with run-of-the-mill workbench synthesizers of poor accuracy and amplitude stability. This makes the system affordable to secondary calibration laboratories.

Further, the use of amplifiers A3 to A6 improves performance, since $V_{XS} = V_{XL}$ and $V_{PS} = V_{PL}$, what approaches to the definition of four-terminal pair standards [9]. Fig. 3 shows a photograph of the measurement system indicating the components of the bridge (its diagram is in Fig. 2).

A. Role of the Tracking Amplifier

The operation of the tracking amplifier was introduced in the former section and is further described here for ratio measurements showing how it considerably aids the stability of impedance determinations by counteracting natural voltage fluctuations of the sources ACX and ACP. Although it can be fully described by mathematical expressions, a more heuristic approach is employed. For that, assume a disturbance on the path ACX–A1 causes V_{HX} (see Fig. 2) to raise. The variation on V_{HX} causes the Kelvin potential to raise as well, what is sensed by A3. Since, A3 has a negative gain, it closes a negative feedback to A1, counteracting this disturbance. Similarly, when the output of A2 suffers a disturbance causing V_{PH} to fall momentarily (since it is out of phase), the Kelvin potential falls as well, and the output of A1 rises due to the negative feedback (of A3 and A1) causing a reaction opposite to that variation. This means that A3 aids voltage and thus ratio stabilization. If A3 were not present, the sources should have a high amplitude stability (smaller than parts in 10^7). Virtually, the tracking amplifier promotes amplitude stability of the commercial sources, improving their performance. A3 has integrative component and is tailored to remain stable for all impedances to be compared (10 Ω to 100 kΩ and 1 to 100 nF). Its gain of nearly 1000 V/V at 1592 Hz compensates for amplitude instabilities of the ac sources by this very same factor.

III. Synchronization and Phase Alignment

There were two high grade audio sinewave generators available in the laboratory, but these sources could not be originally synchronized by an external clock. In order to address this problem, the internal clocking circuitry of the digital signal processor responsible for signal synthesis operating with a master clock f_{MCLCK} of 32.333 MHz was modified in house, so that this frequency could be fed into them from external DDSs (DDSP and DDSX). These devices were then frequency locked to the 10 MHz time-base reference of the ADC. This made ACX and ACP also frequency locked to the ADC for the full synchronous operation of the bridge.

Because ACX and ACP truncate their signal output frequency f at the fifth digit, the output signal is not commensurate (i.e., not fully synchronous) with the desired ADC sampling frequency f_S of the multiplexer. Their 32.333 MHz reference clocks must then be adjusted via DDSP and DDSX to counteract this frequency truncation. This adjustment is done by a digital regulator in the control software of the bridge (see Section III-A), so that f_S becomes commensurate with Nf except by an infinitesimal ξ, where N stands for the number of samples per period of the bridge signal frequency f. Thereafter, f is measured by a counter, which uses the 10 MHz time base of a cesium atomic clock standard as shown in Fig. 2. The uncertainty in the determination of f is thus negligible as compared to other uncertainty components of the system. Alternatively, instead of measuring the signal output frequency f of ACX, the sampling frequency f_S can be measured by the counter, since f and f_S are made commensurate (within $\pm\xi$), what avoids any deleterious and undesired coupling between the analog and digital parts of the bridge.

In an alternative setup, the circuit can be locked-up directly with the 10 MHz of a cesium time-base standard instead of using the internal 10 MHz time base of the ADC. In this case the counter can be suppressed from the measurements, and the ADC operates in a "quasi-synchronous" mode, i.e., being triggered by an f_S derived from the cesium standard. Experiments have shown that this "quasi-synchronous" measurement mode also yielded high quality measurements as compared when the

[1]The identification of commercial instrumentation does not imply endorsement that these are the best for the purpose.

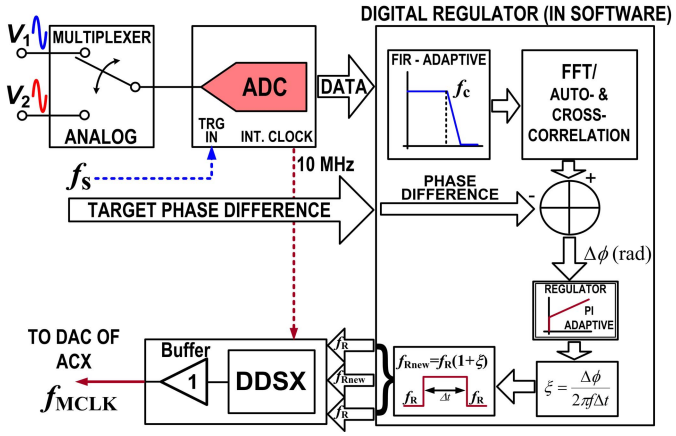

Fig. 4. Diagram of the digital phase-alignment regulator (right). It operates on data from the multiplexed ADC operating with a sampling rate f_S, whereby the sampled signals are synthesized by generators operating with a reference master clock f_{MCLK}. The figure shows the regulator acting on DDSX of source ACX (see text).

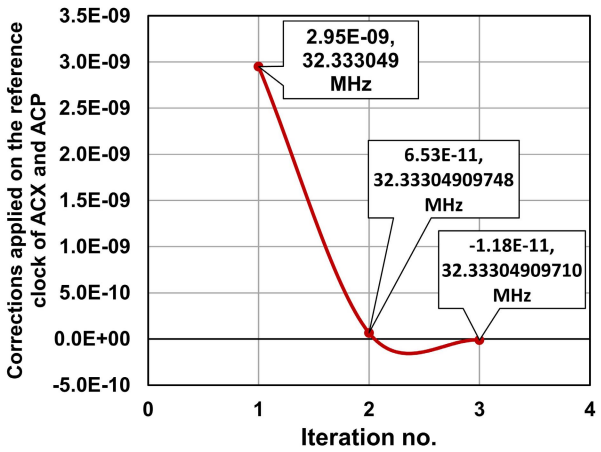

Fig. 5. Master (or reference) clock adjustments of ACX and ACP determined by the digital regulator. In the third iteration, the necessary correction ξ was smaller than the threshold (set by the user to 2×10^{-11}), leading the regulator to stop at a reference master clock f_{MCLK} of 32.333 049 097 10 MHz for both sources.

system operated full synchronously with the ADC's time-base reference.

A. Digital Phase-Alignment Regulator

The regulator is an algorithm (see Fig. 4) that operates on data from the ADC, which is multiplexed to allow sampling of V_1 and V_2 (either direct or differential). It is used to allow frequency synchronization of ACX and ACP with the internal 10 MHz clock of the ADC by adjusting their master clock f_{MCLK} (32.333 MHz), to compensate for frequency truncation errors and to set the phase angle between V_1 and V_2 to balance the bridge. Its principle is based on the fact that the absolute angular phase $2\pi ft$ of a sine waveform may be varied (with respect to a sine of nominal $\omega = 2\pi f$) by minute frequency variations Δf expressed by a fractional frequency correction $\xi = (\Delta f)/f$. The regulator is depicted on the right part of Fig. 4 and is composed of a finite response filter (FIR), an FFT or cross-correlator block, a proportional-integrative (PI) phase regulator, and an algorithm for timed DDS reprogramming.

The adjustment of ACX's and ACP's master clock f_{MCLK} (of 32.333… MHz) is the first procedure to be carried out before meaningful ratio measurements can be done. First, a set of data by direct sampling $V_1 = V_{XH}$ and $V_2 = V_{PH}$ is obtained from which the absolute phase of V_1 and V_2 is computed by an FFT or cross correlation. In a second repetition of the sampling process of V_1 and V_2, the absolute phases are computed again and a mean of phase differences is used to calculate a fractional frequency correction ξ to be applied on the DDS's reference frequency $f_R = f_{MCLK}$ to produce constant absolute phases of V_1 and V_2 as time elapses. The digital PI regulator starts working as a unitary proportional regulator with zero integrative constant (i.e., it feeds a missing phase to reduce the original phase variation with unitary gain). When the variation of absolute phases of V_1 and V_2 over time becomes, for instance, 1/100th times smaller than the first variation (after the second or third sampling repetition of f_R adjustment that yields a new f_{MCLK}), the proportional coefficient is reduced and the integrative coefficient slowly rises up to 0.3 on each sampling repetition to aid convergence (i.e., it becomes a PI regulator). The regulator remains always stable for proportional and integrative coefficients smaller than 1. Furthermore, it is well known from control theory that an integrative regulator reduces systematic deviations to 0 with time. In this sense, the variation of the reference frequency f_R (32.333 049 097 10 MHz as shown in Fig. 5) for an f_{MCLK} adjustment is cumulative since f_{MCLK} is finely adjusted to compensate for ACX's and ACP's frequency truncation. In the case that the phase difference (with the target phase difference nominally set to 0) does not converge to 0 (i.e., within a threshold defined by the user, e.g., of some parts in 10^{-11}) for a predefined number of iterations, a reset of the integrator takes place and the regulator starts over again with unitary gain. A possible cause of nonconvergence might be, for example, electromagnetic interference of nearby circuits (i.e., heavy-loading switching) that could wrack havoc the sampling process with corrupted samples. Generally, the adjustment of f_{MCLK} for ACX and ACP is a straightforward process as exemplified in Fig. 5, indicating that the final f_{MCLK} allows the ac sources to synthesize an output signal with fundamental f, such that Nf becomes commensurate with f_S within a ξ of -1.18×10^{-11} parts in three iterations only. The slight "lack of synchronization" of such a magnitude barely jeopardizes ratio measurements, since the phase shift resulting from such an infinitesimal ξ is small. For example, assuming the total multiplexed sampling time between records of V_1 and V_2 is $\Delta t = 1\ s$ for $\omega = 10^4$ rad/s and $\xi = 1.18 \times 10^{-11}$ Hz/Hz, the resultant absolute phase shift $\Delta\varphi$ between V_1 and V_2 amounts to $\Delta\varphi = \xi\omega\Delta t = 0.118$ μrad. This is far below effects of amplitude noise floor levels. For the setting of phase angle between V_1 and V_2, the target phase difference is the parameter, which is computed first from the nominal values of the standards to be compared and latter from the balance

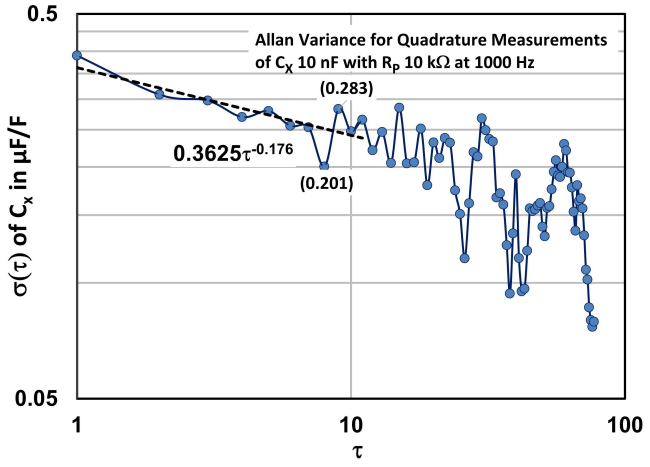

Fig. 6. Allan standard deviations of capacitance determinations (for a C_X of 10 nF nominal value) with a 10 kΩ standard resistor R_P at 1000 Hz versus the number of measurement averages τ. Averages of $\tau = 10$ measurements allow standard deviations of the order of 3×10^{-7} to be attained, as indicated by the dashed regression line represented by the exponential function.

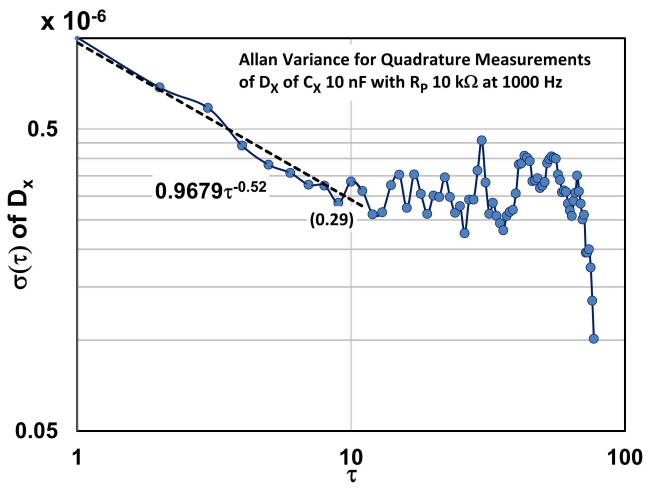

Fig. 7. Allan standard deviations of dissipation factor determinations for the same capacitor as in Fig. 6 at 1000 Hz. The regression line represented by the function indicates that the measurement process is dominated by white noise up to a τ close to 10.

algorithm (downhill simplex). After a sampling process, the signals are filtered by the FIR filter, FFT (or cross-correlated if desired) to find the actual phase. The measured phase is compared with the "target phase" (necessary to balance the bridge) and the phase difference passes through a PI regulator (first with unitary proportional gain). Finally, a fractional frequency correction is computed. Defining a reprogramming time window lasting a $\Delta t = 1$ s, DDSX is programmed to vary f_{MCLK} by $(1+\xi)$ lasting also Δt in time, what makes the phase of source ACX to advance or recede by the required phase difference $\Delta\varphi = \xi\omega\Delta t$. During the reprogramming sequence of time-length Δt, obviously no data acquisition (or sampling) occurs. The procedure of sampling, calculation and adjustment is repeated until $\Delta\varphi$ is smaller than a predefined threshold (e.g., 1µrad). It is worth mentioning that the better phase alignment of ACX is made, the lower is the output signal of the tracking amplifier (if engaged by the user) needed to effectively reduce the Kelvin voltage V_k (see Fig. 2), as the circuit path built up by ACX, A1, and A3 represents a feed-forward composite amplifier of very high (virtual) gain as seen from the Kelvin point connection of $R_K C_K$. In fact, amplifiers A1 and A3 are able to balance the bridge without the source ACX (i.e., with ACX set to 0), since the necessary voltage would be maintained by A3 alone. However, with a well-adjusted ACX, the output voltage of A3 amounts to some millivolts only, what makes the reduction of V_k more effective by many orders of magnitude.

IV. Experimental Investigations

Extensive investigations with the bridge corroborate its high grade performance. Fig. 6 shows Allan standard deviations for the calibration of a 10 nF standard capacitor C_x with a 10 kΩ standard resistor R_P. Nearly perfect agreement (within parts in 10^7) between the digital system and the four-terminal coaxial pair bridge was attained [14]. The Allan deviation of dissipation factor measurements of the same capacitor is shown in Fig. 7. A departure of the mean of only 0.8×10^{-6} when compared with a commercial capacitance bridge (Andeen Hagerling AH2700) was obtained. Fig. 8 shows Allan standard deviations for resistance calibrations in quadrature (after thermal stabilization) with a known standard

TABLE I
Uncertainty Contributions for Unitary Ratio Measurements

For Quadrature Measurements at 1592 Hz		Uncertainty u_A (x 10^{-6})	Uncertainty u_B (x 10^{-6})
Noise of ac sources	(Type B)	1.4	1.4
DVM intrinsic noise	(Type B)	0.04	0.04
DVM sampling noise	(Type B)	0.08	0.08
DVM quantization noise	(Type B)	0.082	0.082
Jitter of sampling process	(Type B)	0.31	0.31
Repeatability	(Type A)	0.3	0.3
TOTAL CONTRIBUTION:		1.5	1.5

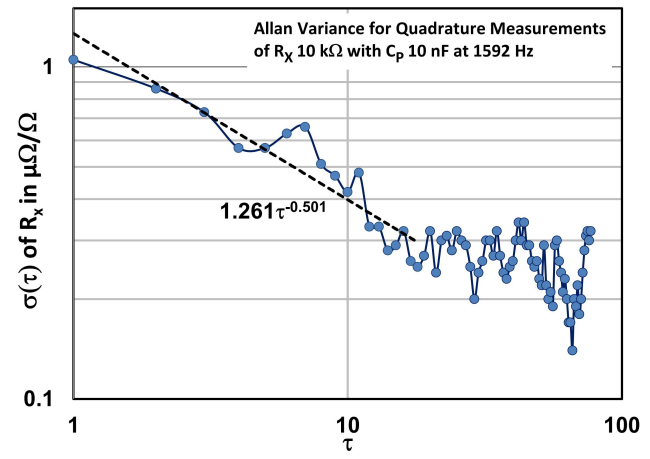

Fig. 8. Allan standard deviations for resistance determinations (for a R_X of 10 kΩ) with a known 10 nF standard capacitor C_P. Standard deviations of the order of 4×10^{-7} are attainable when averaging ten single measurements and still in the white noise regime.

TABLE II
QUADRATURE MEASUREMENTS OF A CAPACITANCE C_X WITH A STANDARD RESISTOR R_P

Reference values:	Capacitance	C_X = 9.999756 nF					u_{CX} = 0.25 μF/F		
	Dissipation factor	D_X = 107 x 10^{-6}					u_{DX} = 10^{-5}		
	Standard Resistor	R_P = 9.9999038 kΩ					u_{RX} = 0.2 μΩ/Ω		
	Time-constant	τ_P = 3 ns					$u_{\tau P}$ = 0.5 ns		
	Calculated Ref. Ratio	A = 77 x 10^{-6}					B = 0.999751		
C_X(nF)	u_{CX}(μF/F)	D_X	u_{DX}	A	u_A	B	u_B	δC_X(μF/F)	δD_X
9.999756	1.5	96e-6	1.6e-6	126e-6	1.5e-6	0.99975095	1.5e-6	0.038	-11e-5

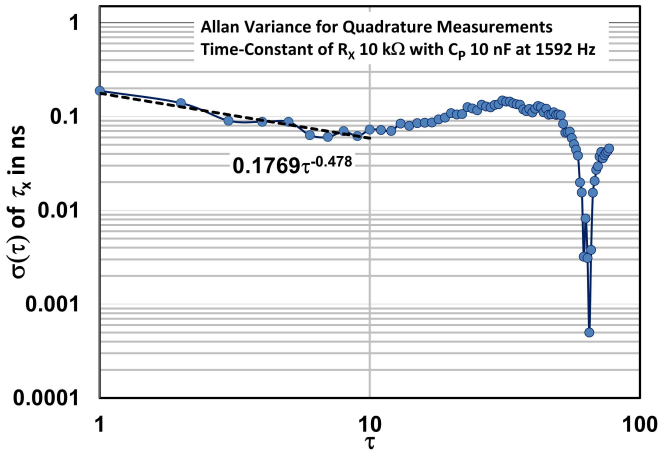

Fig. 9. Allan standard deviations in nanosecond of resistor time-constant τ_X determinations from quadrature measurements with a standard capacitor at 1592 Hz. In white-noise regime, standard deviations of around 0.1 ns are attainable when averaging ten measurements.

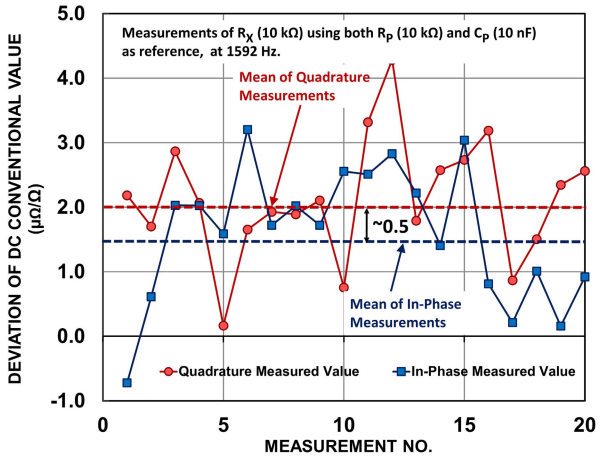

Fig. 10. Twenty comparisons of resistance determinations (in-phase measurements using a standard resistor, represented by squares) with those obtained from quadrature determinations (using a standard capacitor as the reference, represented by circles). The agreement between the mean values of both sets of measurements is within 0.5 × 10^{-6}.

capacitor. The agreement was 1.5 ×10^{-6} parts of the mean and this deviation is explained by a small heating effect in the resistor when operating the bridge with 7 V. The Allan deviations of time-constant determinations (after thermal stabilization) are shown in Fig. 9. Time constant determinations are in agreement with time-constant determinations of the same resistor (of 3 ns ± 0.3 ns) done at the Laboratoire National de Métrologie et d′ Essais (LNE), in France, and are within LNE's uncertainty limits.

The bridge also shows high performance for different quadrature configurations, as the calibration of a 100 nF standard capacitor C_X with a 1 kΩ standard resistor R_P, where the agreement between the digital and four-terminal coaxial pair bridge was smaller than 2 ×10^{-6} parts at 1592 Hz. Even when comparing a C_X of 1 nF with a standard resistor R_P of 10 kΩ at 1592 Hz, where the DVM voltage ratio is 10, the agreement between the digital with the coaxial bridge were within its expected uncertainty (less than 6 × 10^{-6} parts).

The comparison of resistors (so-called in-phase comparisons) was also extensively investigated [15] and can be summarized in Fig. 10, which indicates very good agreement (of 0.5 × 10^{-6} in the mean) compared with resistance determinations using a capacitor as reference. Since the standard resistors are not fully independent of frequency, their values differ a little bit from the dc (direct-current value represented on the zero line) values as shown in Fig. 10.

Table I summarizes the contributions of measurement uncertainties to the measurement of unitary voltage ratios [16]–[19] in quadrature by digital sampling the 2048 samples and by averaging 10 measurements as allowed by the Allan standard deviations in Figs. 6–9, for a coverage factor $k = 1$. Contributions due to DVM's sampling noise [16] are also included. The first column indicates the contributions of uncertainty. The second and third columns indicate the attainable uncertainty for the real and imaginary parts of voltage ratio (A and B), respectively, using the calculation procedure of [18], which is compatible with [19]. For a DVM voltage ratio other than one, the DVM's nonlinearity must obviously be taken into account in voltage ratio measurements. The DVM's nonlinearity is dependent on the DVM's aperture time and can easily be compensated numerically after calibrating the DVM by measuring voltage ratios with the help of a high-grade inductive voltage divider. The 3458A DVM[1] [20] used for ratio measurements yielded a maximum nonlinearity of 2 μV/V in its 10 V range. The results hitherto obtained with the digital bridge (with contributions as detailed in Table I) will be used in a deeper numerical modeling of measurement uncertainties based on Monte Carlo simulations [19].

Table II presents calibration results using a capacitor and a resistor with uncertainty figures for quadrature measurements. The first line shows the nominal values obtained from calibration certificates of the standards with their corresponding uncertainties to the right. The last line displays the measured values followed by their calculated measurement uncertainties. The uncertainties of capacitance u_{CX}, of dissipation factor u_{DX}

and of ratio A and B are valid for a coverage factor $k = 1$. The last two quantities δC_X (μF/F) and δD_X indicate measured deviations with respect to the reference values (as stated in the first line).

The good agreement of data is indicative of the quality of the bridge, its circuitry and balancing procedures. In addition, the results demonstrate low coupling effects (crosstalk and stray elements as capacitances) within circuits, whose effects normally pop up as systematic deviations of phase and amplitude.

V. Conclusion and Outlook

The present design of the digital impedance bridge is the result of improvement efforts from its first concept [11], which used common workbench synthesizers. After modifications in the synchronization circuitry of commercial audio sinewave generators of low harmonic distortion and electrostatic shielding of many elements of the bridge, voltage ratio measurements improved substantially (by a factor of nearly ten times as compared when using workbench synthesizers). The system can now be used in daily ac resistance and capacitance measurements and is able to deliver high-quality calibrations with uncertainties comparable with the DVM's inherent nonlinearity. Nonetheless, the principle upon which it is based can be further refined. Presently, the concept of a current comparator (CC) based impedance bridge that allows true four-terminal pair impedance measurements is under investigation [21]. With this design, DVM nonlinearities for ratios other than unitary will not influence measurements, since the digitizer will operate in its full range at all times or work as a detector by measuring feeble signals, which does not substantially contribute to final measurement uncertainties. Preliminary investigations with the CC based design indicate that measurement uncertainties may be lowered by a factor of 10 or more.

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