

# Digital Phase Standard of High Accuracy Up To the Megahertz Range

Waldemar G. Kürten Ihlenfeld

**Abstract**—This paper describes a system for generating and measuring extremely accurate phase angles that combines the digital synchronous signal generation with the synchronous subsampling technique, aided by digital phase regulation. The system can be set up with commercially available instrumentation. Experimental evidences suggest that the phase between two generated sine signals can be resolved to a few microradians up to the megahertz range.

**Index Terms**—Adaptive signal processing, digital signal processing, measurement standards, measurement techniques, phase estimation, signal analysis, uncertainty.

## I. INTRODUCTION

PHASE measurements find application in many areas of science and technology, for instance, in the characterization of sensors and transducers [1], in the measurement of the frequency stability of time-standards, ac bridges [2], and in the measurement of ac power and energy, to cite a few. This paper is the extended version of [3].

Over the last decades, a myriad of publications came out suggesting phase standard topologies, either by phase shifting two signals generated by digital-to-analog converters (DACs) [4] or by transforming sine waveforms into square waves and by measuring the difference of their starting points [5], [6]. Meanwhile, many algorithms for extracting the phase information from two sine waves arose as [7] and [8], and to estimate phase errors as in [9]. An interesting approach to tackle phase measurement problems under harsh noisy conditions using filtering is described in [10]. For metrology laboratories, an accurate phase measurement setup using coherent digital signal generation and sampling [11] combined with the heterodyne phase detection was reported in [12].

The system proposed here employs the coherent signal generation and sampling from a single time-base reference [11] (known as locked-in signal synthesis and signal detection), and is an extension of [13], [14] combined with subsampling [15]–[20], to widen its phase measurement frequency range. The applicability of an integrating digital voltmeter (DVM), usually used for low-frequency calibrations

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The author is with the Brazilian National Institute of Metrology, Quality and Technology, Duque de Caxias RJ-25250-020, Brazil (e-mail: wkgihlenfeld@gmail.com).

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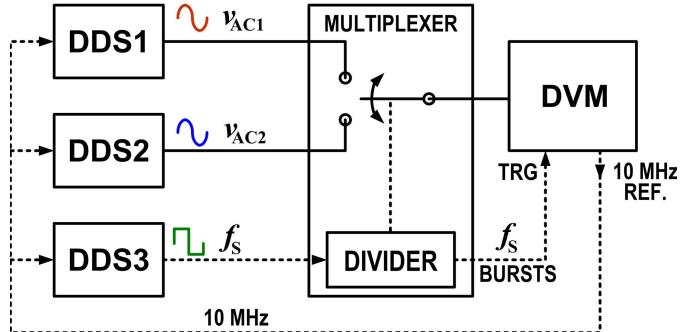


Fig. 1. Schematics of the phase standard employing DDS-based signal sources for sine synthesis and for triggering (see text).

(normally up to 1 kHz), can be expanded in its frequency range, allowing phase detection of a few microradians from low frequencies (of a few hertz) up to the megahertz range.

## II. DESCRIPTION OF METHOD AND HARDWARE

The concept of a phase is interesting, because the time  $t$ -dependent phase  $\phi$  of a sine waveform of frequency  $f$  and expressed as  $\phi = 2\pi ft$  is dimensionless, i.e., it is not dependent on any physical unit. Therefore, in theory, if two sine waveforms of frequency  $f$  are generated from a common frequency reference and sampled at equal time-spaced intervals at a rate  $f_S = Nf$  (for  $N$ , an integer greater than two) derived from the very same frequency reference, such a phase reference system is, in principle, “inherently error-free.” In the practice however, although we seek to get closer to the ideal case, we are forced to rely on a voltage or current signal, and limitations arise thus from signal noise and distortion, shortcomings in DACs, and analog-to-digital converters (ADCs), such as glitches or spikes and code errors, which introduce wideband spurs and distortion, nonlinearities, delays, and timing jittering among others.

In spite of the imperfections of direct-digital-synthesizers (DDSs) like unwanted spurs and modulation on amplitude and phase [21], [22], they were used as sine and square waveform generators in the system shown in Fig. 1 and were frequency locked to the 10-MHz reference of a sampling DVM [23]. The 48-bit DDSs [24] were properly filtered, and displayed harmonic distortion and phase noise smaller than  $-60$  dBc. Some commercial workbench synthesizers can also be used. The multiplexer selects alternately  $M$  periods of the sine signals  $v_{AC1}$  and  $v_{AC2}$  of frequency  $f_n$ , which are sampled by the DVM at a rate  $f_S = Nf_o$ , where  $f_o$  is the alias frequency onto which the signal of frequency  $f_n$  will

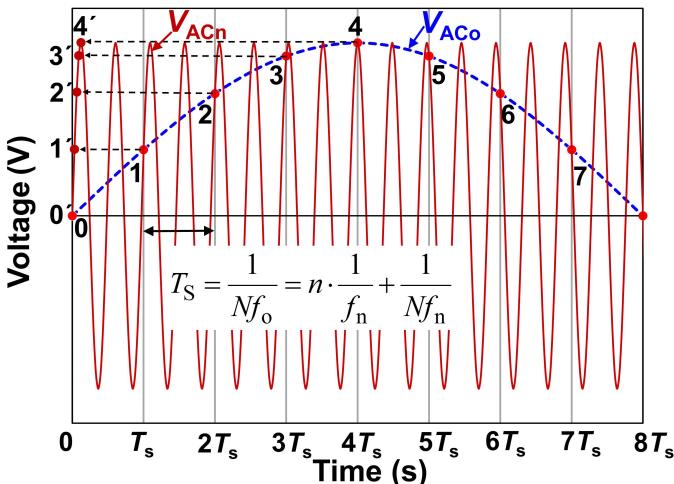


Fig. 2. Illustration of a signal  $V_{ACn}$  of frequency  $f_n$  sampled at a lower rate according to (1) for  $n = 2$  and  $N = 16$ . Only half a period of the aliased signal  $V_{ACo}$  of frequency  $f_o$  is shown for the sake of clarity. Note that  $T_s$ , i.e., the time between two samples of  $V_{ACo}$ , encompasses  $(2 + 1/16)$  periods of  $V_{ACn}$ . In addition, the set of digital samples  $\{0, 1, 2, 3, 4, \dots\}$  corresponds to the set  $\{0', 1', 2', 3', 4', \dots\}$  as if  $V_{ACn}$  values were sampled at a rate  $Nf_o (nN + 1)$ . Furthermore, the phase of  $V_{ACn}$  and of its alias  $V_{ACo}$  are numerically equal.

be folded back, as described in [3].  $N$  stands for the number of samples per period  $T_o = 1/f_o$  of the alias sine waveform of frequency  $f_o$ . The condition of the aliasing of  $f_n$  onto  $f_o$  is given when the sampling time  $T_s = 1/f_s$  encompasses  $(n + 1/N)$  periods of the  $f_n$  signal for  $n$  a positive integer equal to or greater than zero, that is

$$T_s = \frac{n}{f_n} + \frac{1}{Nf_n} = \frac{1}{Nf_o} \quad (1)$$

what yields the following relation between  $f_n$  and  $f_o$ :

$$f_n = f_o(nN + 1). \quad (2)$$

Therefore, over the period  $T_o$ , a total of  $N$  samples of the signals  $v_{AC1}$  and  $v_{AC2}$  of frequency  $f_n$  will also be harvested, as if they were sampled at a higher rate  $f'_s = Nf_n$ . This subsampling process [15]–[20] allows a sensible extension of phase measurements toward higher frequencies to be attained. Any harmonics of the  $f_n$  signals  $v_{AC1}$  and  $v_{AC2}$  “fold back” at  $2f_o$ ,  $3f_o$ , and so on. The advantage of subsampling becomes thus apparent, because the signals are sampled at a much lower rate, what allows extending the frequency range of a slow sampling digitizer at the expense of an increased sampling time. Although information on the  $f_n$  signal frequency is lost, we know it beforehand. Fig. 2 shows the aliasing process according to (1).

Fig. 3 shows the analogy of a 48-bit DDS with a programmable spur gear, which generates a sine waveform of higher frequency  $f_n$  as it rotates. The 48-bit corresponds to 281 trillion spurs of a spur gear mechanically attached to a ratchet that drives the gear’s rotation. In the case of Fig. 3, for the ratchet driving each spur, one by one, at a rate of 120 MHz, the resulting ac signal is of  $120\,000\,000/2^{48}$  Hz, or  $\sim 0.426 \mu\text{Hz}$ . The DDS’ output frequency  $f_n$  is programmed by the number called word  $w$  that stands for the number stored

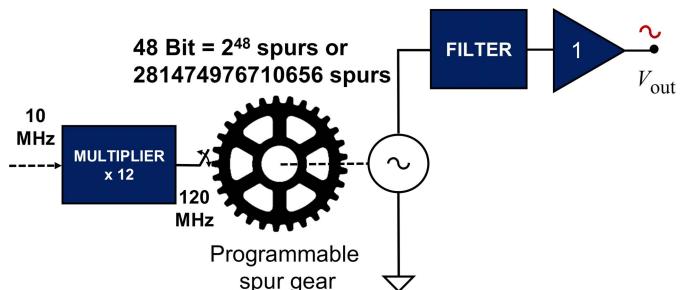


Fig. 3. Analogy of a 48-bit DDS with a programmable spur gear, which generates one period of a sine waveform while it rotates one turn as it is mechanically coupled with an ac voltage generator (whose output is further filtered to reduce jitter and noise, and buffered to feed a load). See text.

in the DDS’ phase accumulator for a given number of bits depth  $b$  and a master clock  $f_{MCLK}$  as

$$f_n = \frac{w f_{MCLK}}{2^b}. \quad (3)$$

In the mechanical domain (Fig. 3), the word  $w$  stands for the number of programmable steps of the spur gear to be jumped by each ratchet oscillation.

The master clock is the internal working frequency of the DDS that results from the input clock frequency  $f_{CLK}$  times the DDS’ internal multiplier constant  $m$ . For the case in Fig. 3,  $f_{CLK}$  is 10 MHz and  $m = 12$ , resulting in an internal master clock  $f_{MCLK}$  of 120 MHz (as used in the experiments described later). Because  $w$  assumes only integer values, truncation of the output frequency always appears and must be avoided in the phase standard as much as possible. However, it is possible to reduce its deleterious effects to a wide extend such as to a few parts in  $10^{-15}$  making phase offset errors barely noticeable, as is shown in Section III, what allows us to consider the system to work essentially coherent with the DVM time-base 10-MHz clock. To quantify the truncation error, the fractional error  $\xi$  is used and defined as follows:

$$\xi = \frac{f_n - f'_n}{f'_n} \quad (4)$$

where  $f'_n$  stands for the desired DDS output frequency.

Other effects of concern are spectral leakage and aliasing of high frequency signal components. Leakage effects, known as the spreading of spectral components due to the lack of synchronization of  $f_s$ , are indeed present. However, due to the small magnitude of  $\xi$ , leakage-induced errors on phase and spectral amplitudes are barely noticeable and are negligible as compared with noise effects. Likewise, aliasing due to the presence of spurious signals of higher frequency is a source of phase inaccuracy. Provided that such spurious are mitigated by band limiting the signal and that the folded-back components due to subsampling do not fall onto the alias component of interest at  $f_o$ , their effects are thoroughly negligible, as is shown in Section III.

Methods and procedures for doing accurate phase measurements are further discussed in Section III, where phase measurements were investigated using 48-bit DDSs for signal

TABLE I  
DDS SETTINGS FOR SIGNAL FREQUENCY SYNTHESIS

$n$	Desired $f_n$ ' (Hz)	DDS word $w$ to generate $f_n$ '	Resulting
0	96	225179981	-1.636e-09
1	1632	3828059683	-6.921e-11
2	3168	7430939385	-2.171e-11
3	4704	11033819087	-5.231e-12
7	10848	25445337895	+1.402e-11
13	20064	47062616106	-4.607e-13
65	99936	234412360605	+1.560e-12
651	1000032	2345699865916	+3.289e-14
3256	5001312	11731201489356	-3.112e-15
6511	10000992	23458574919029	+8.181e-15
For	$f_s = 1536$ Hz	3602879702	+2.876e-11

generation and cascaded ones for the synthesis of the sampling frequency  $f_s$ .

### III. EXPERIMENTAL INVESTIGATIONS

Table I exemplifies some of the  $f_n$  frequencies that can be synthesized according to (1) using an alias base frequency  $f_0$  equal to 96 Hz. The value of 96 Hz was chosen, because a window with a radix-of-two number of samples (e.g., 1024) acquired at a rate of 1536 Hz (i.e.,  $N = 16$  samples per period of 96 Hz) encompasses 40 integer periods of the power line network frequency of nominal 60 Hz. Hence, any harmonic of the power line are thus expected not to sensibly interfere with the measurements through leakage effects. This care is necessary, since all measurements and data processing are done in the frequency domain with the fast Fourier transform (FFT). Note that for  $f_n$  equal to 1.000032 MHz, the fractional error  $\xi$  is indeed small (+3.3e-14). However, the synthesis of a sampling frequency of 1536 Hz, as desired to detect its alias at  $f_0$ , has an  $\xi$  of +2.876e-11 and cannot be compensated (i.e., to attain  $\xi$  equal to zero) appropriately with one single 48-bit DDS. The small  $\xi$  represents a lack of synchronization and causes phase zero offset errors when sampling two channels via multiplexing with a single ADC. Since the channels are multiplexed, a finite time interval is necessary to acquire the samples. Therefore, if the sets of samples of  $v_{AC1}$  and  $v_{AC2}$  of Fig. 1 are separated (in time) by an acquisition time  $\Delta t$  of 1 s, the resulting phase offset becomes  $\Delta\phi = \xi\omega\Delta t$  or 181  $\mu$ rad. This undesired and “erroneous” offset pops up due to sampling the signals noncoherently, i.e., with  $f_s$  not truly commensurate with  $f_n$ . In fact, the signals are either advancing or receding with respect to  $f_s$ . One could assume that the use of two ADCs operating synchronously could circumvent this problem. This is in part true at low frequencies (some kilohertz) but not at higher frequencies, when timing-delay mismatches of the ADCs become more noticeable. The use of a single ADC or DVM (as a Keysight 3458A DVM [23]) solves the problem of internal delays in the trigger circuitry and nonlinearities when doing FFT-ratio or difference of FFT-phases [11], especially for signals of equal magnitude. Since the DVM trigger is locked to the internal DVM clock,

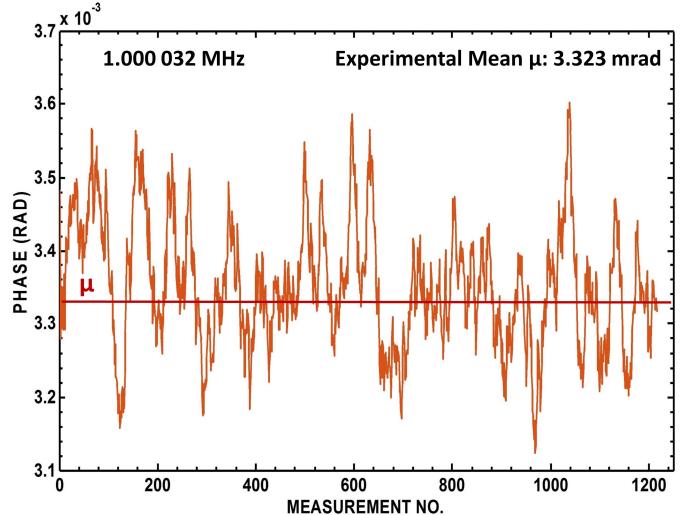


Fig. 4. Zero phase determinations with the multiplexer inputs with a single signal applied to them, i.e.,  $v_{AC2} = v_{AC1}$  and of equal amplitude of 10 V peak, showing the offset error due to the misalignment of the sampling frequency caused by uncorrected DDS truncation. A negative  $\xi$  means that the measured signal at terminal  $v_{AC2}$  is advancing in phase with respect to that at terminal  $v_{AC1}$ .

the use of the 10-MHz DVM’s time base for signal generation and triggering guarantees that the DVM’s trigger delay is kept constant for both sampled signals  $v_{AC1}$  and  $v_{AC2}$  what does not affect phase determinations.

Truncation errors when generating  $f_s$  are sensibly reduced when DDS3 of Fig. 1 is built by cascading three DDSs in series, one of 48-bit depth [24] to generate a nominal clock frequency of 20 MHz for the second DDS of 32-bit [25], which delivers a clock for the third one with 28-bit [26]. The second DDS was set to generate a nominal frequency of 1/10th the depth of bits of the third, i.e., 26.8435456 MHz. Therefore, the settable nominal resolution of the third DDS is 0.1 Hz. Like a Vernier of a caliper, such arrangement allows higher resolutions when setting  $f_s$  to be attained. Doing so, the corresponding words for the cascaded composite DDS3 are thus 46912496118443 for the first DDS [from (3) using  $f_n$  equal to 20 MHz and  $b$  equal 48], 960767920 for the second DDS (of 32-bit), and obviously 15360 for the third DDS (of 28-bit) to ultimately generate  $f_s$  of 1.536 kHz. The multiplier coefficient for the first two DDSs was also  $m = 12$  (yielding a master clock of 120 MHz for the first and second DDS of DDS3). The resultant  $\xi$  using the nominal values of frequencies amounts to -5.263e-10, which is, in absolute terms, bigger than  $\xi = 2.876e-11$  of a single 48-bit DDS generating  $f_s$  of 1.536 kHz. In this specific example, truncation is compensated by programming the first DDS of the composite DDS3 to generate a 20-MHz clock times the correction term  $(1 + 5.263e-10)$ , i.e., 20 000 000.010526 Hz. The resulting  $f_s$  of the cascade combination is still truncated, but with a smaller  $\xi$  of only -1.63e-15, which is nearly  $2.876e-11/1.63e-15 \approx 18000$  times smaller than the former. The expected offset error would thus, under the same conditions, amount to  $10^{-8}$  rad, what is undetectable by the system, since other noise sources are present.

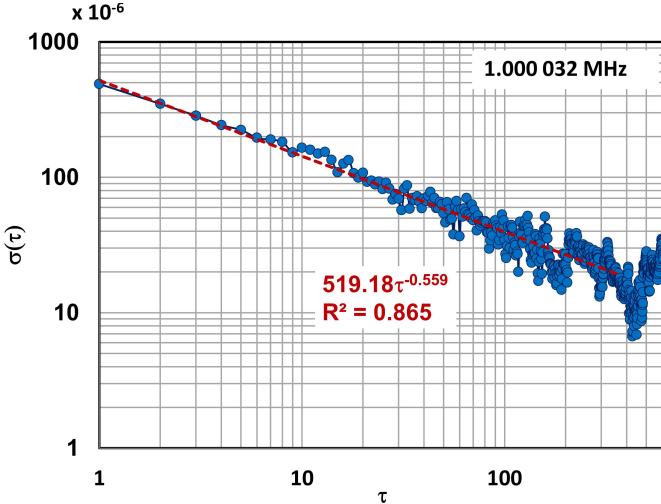


Fig. 5. Allan standard deviation for the data of Fig. 4. The plot shows that averaging of up to 200 or 300 sampling intervals  $\tau$ , the classical and the Allan standard deviations converge. The data follow an exponential on  $\tau$  indicating an essentially white noise dominated process with a correlation coefficient  $R^2$  as stated.

To demonstrate the effects described thus far, DDS1 and DDS2 were programmed to generate signals of 1.000032-MHz nominal frequency. DDS3 was programmed to generate 1.536 kHz without truncation corrections, i.e., the resultant fractional error  $\xi$  was  $-5.263 \times 10^{-10}$ . The expected theoretical offset error of the phase between  $v_{AC2}$  and  $v_{AC1}$  (for DDS1 and DDS2 starting simultaneously) is thus  $-\Delta\phi = -\xi\omega\Delta t$  or 3.307 mrad (with a minus signal because a phase difference of  $v_{AC2}$  with respect to the phase of  $v_{AC1}$  is being measured). The 1250 phase determinations with the system operating as stated are shown in Fig. 4 and have a mean value of 3.323 mrad. This mean is in agreement with the theoretical predicted value by +19  $\mu$ rad only.

The Allan standard deviations [27] for the data in Fig. 4 are shown in Fig. 5, indicating that the measurement process is influenced mainly by Gaussian (white) noise phenomena. Averages of 200 to 300 measurements points are thus supposed to deliver reliable standard deviations without systematic errors of nearly 20  $\mu$ rad at 1.000032 MHz.

There is, however, another way to infer on phase offsets due to DDSs' truncation errors with higher accuracy and precision. When we increase the observation time between phase determinations by a factor  $k$ , the phase difference will also be magnified by this factor for a constant  $\xi$  and  $\omega$ , enabling a better correction for DDS frequency truncation to be attained. Since the instrumentation is supposed to keep its precision, irrespective of measuring a quantity  $x$  or a magnified quantity  $y = kx$ , according to the law of variances, the variance of  $x$ , i.e.,  $s_x^2$  can be estimated from the variance of  $y$  denoted by  $s_y^2$  since  $s_x^2 = s_y^2/k^2$ . This procedure was employed to correct for the DDS truncation errors by applying a single signal on the two inputs of the multiplexer and waiting 30 s between two acquisitions with 1024 samples each. Two blocks of data were thus necessary for one phase determination. Each block was fast-Fourier-transformed, and the phase difference

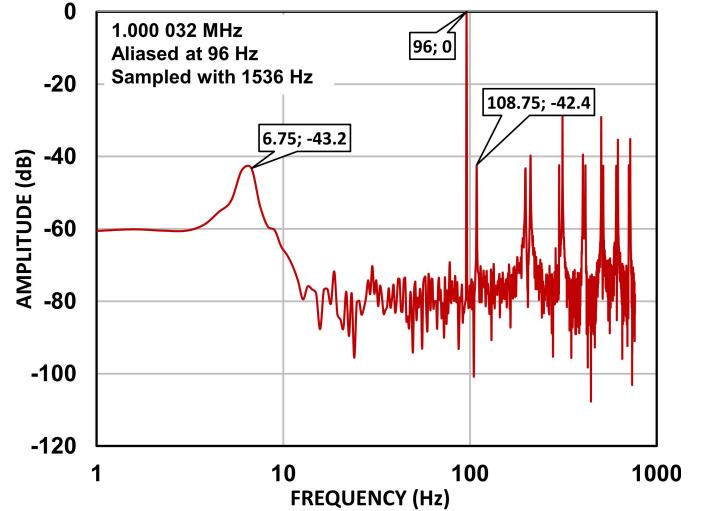


Fig. 6. Spectrum of a 1.000032-MHz signal aliased at 96 Hz. The closest component is located at 108.75 Hz with a magnitude of  $-42.4$  dB. No leakage is apparent at 96 Hz, as it is in other aliased components to the right. Close to the alias, the noise floor varies between  $-76$  and  $-85$  dB.

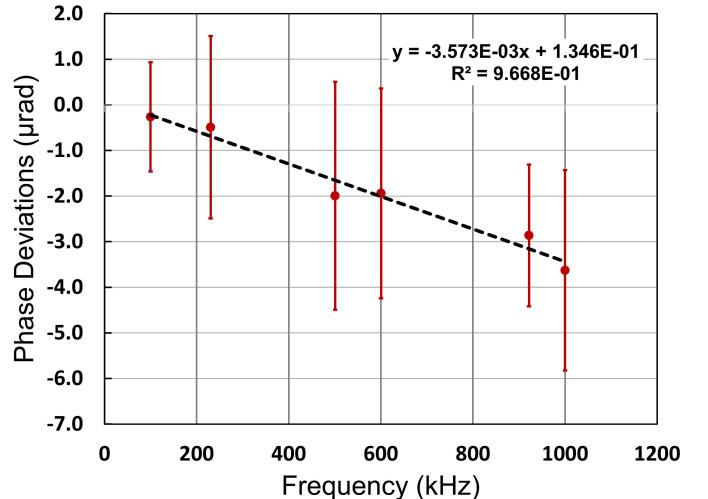


Fig. 7. Measured residual systematic deviations of the zero phase due to DDSs' truncation (see text). The  $f_n$  points are for  $f_0 = 96$  Hz,  $N = 16$ , and  $n$  equal to 65, 150, 326, 391, 600, and 651, respectively.

was calculated and divided by 30 to normalize it to the 1-s interval. The measurement process was repeated 25 times (after the truncation error was numerically compensated as previously described). Fig. 6 shows the spectrum of the aliased 1.000032 MHz signal.

The residual phase offsets at different frequencies starting at 99.936 kHz for different values of  $n$  in (2) are shown in Fig. 7, where the bars represent the standard deviations of measurement. At 1 MHz, the standard deviation is approximately 86  $\mu$ rad (using the equation for the dashed trend line in the inset of Fig. 5 with  $\tau = 25$ ), which divided by 30 yields a standard deviation of  $\sim 2.8$   $\mu$ rad, i.e., in fairly good agreement with that obtained and depicted in Fig. 7, although the ac signal was of smaller amplitude ( $\sim -7.5$  dB of 10 V full scale). Note that the determined phase offsets are small but not zero. Curiously, there is in Fig. 7 a clear linear tendency of the data

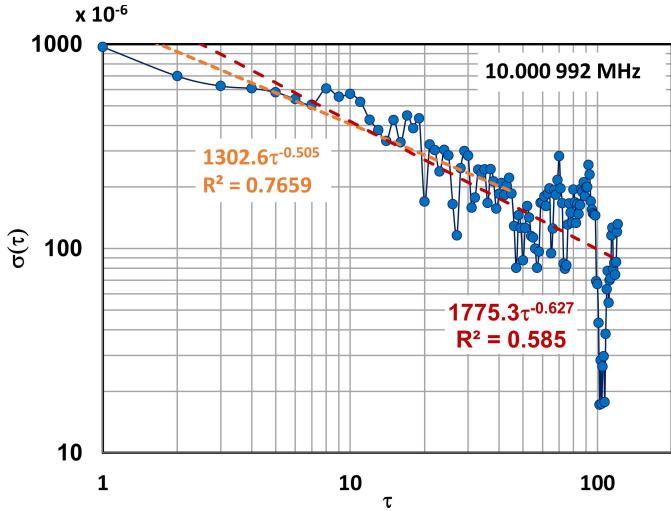


Fig. 8. Allan standard deviations of phase at 10 MHz (see text).

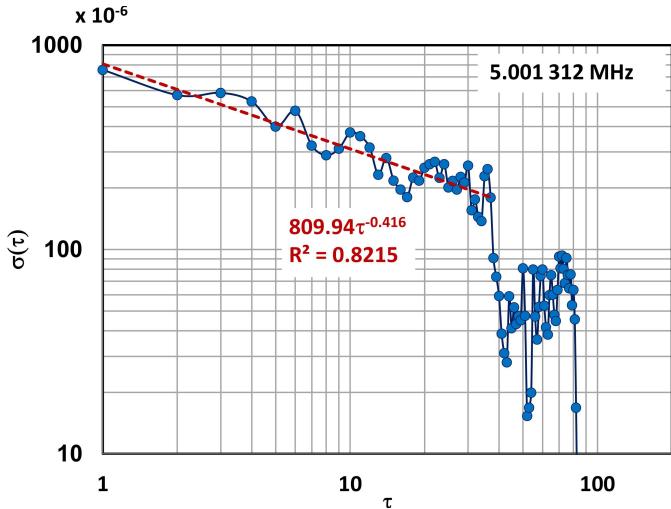


Fig. 9. Allan standard deviations of phase at 5 MHz (see text).

as  $f_n$  drops, as shown in the graphic by the dashed line. This behavior is attributed to rounding of the DDSs' programming words, which must be integer numbers. The compensation of residuals may be further accomplished by a finer trimming of DDS1 and DDS2 or even of  $f_s$  generated by DDS3. The later allows more degrees of freedom for a finer trimming due to the cascaded DDS arrangement. It seems, however, that a small offset for the zero phase adjustment of the system of the order of  $\sim 4 \mu\text{rad}$  at 1 MHz (what corresponds to a timing error of  $4 \mu\text{rad}/\omega$  or  $\sim 0.64 \text{ ps}$ ) suffices most demands in the practice. In any case, it can be compensated numerically if desired.

Investigations on zero phase offsets furnish thus a reliable insight on the capabilities of the method and phase standard. This shall be demonstrated for other frequencies starting with  $n = 6511$ , i.e., 10.000992 MHz. Fig. 8 shows the Allan phase standard deviation for 10 MHz under the same conditions as when measuring at 1 MHz. Essentially, white noise conditions can be ensured up to a  $\tau$  of 40 averaged measurements (according to the orange tendency line of Fig. 8) indicating that reliable phase measurements with standard deviations of  $\sim 200 \mu\text{rad}$  are feasible (as for 5 MHz in Fig. 9). The red tendency line for larger  $\tau$  of Fig. 8 should be avoided, since

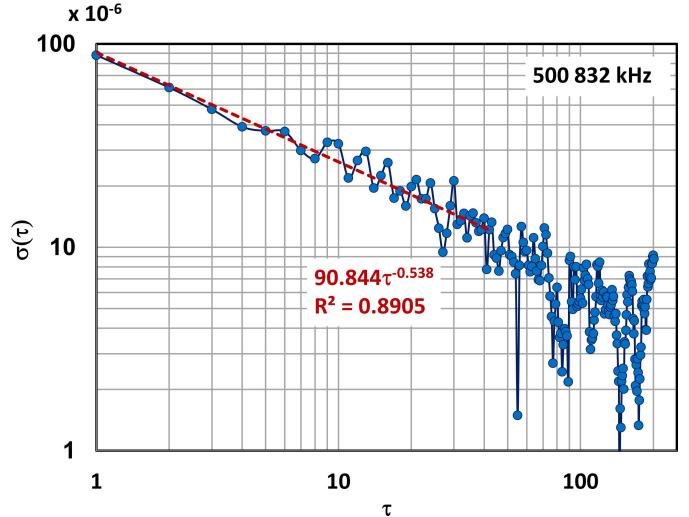


Fig. 10. Allan standard deviations of phase at 500 kHz (see text).

TABLE II  
HEURISTIC ATTAINABLE STANDARD DEVIATIONS  
FOR PHASE MEASUREMENTS

Frequency	Best attainable std. deviations*	Approx. no. of averages ( $\tau$ ) and measurement time*
10 MHz – 5 MHz	$\sim 200 \mu\text{rad}$	30, 120 s
1 MHz – 700 kHz	$\sim 20 \mu\text{rad}$	100, 400 s
500 kHz – 200 kHz	$\sim 5 \mu\text{rad}$	20, 80 s
100 kHz – 70 kHz	$\sim 2 \mu\text{rad}$	40, 160 s
50 kHz – 10 kHz	$\sim 2 \mu\text{rad}$	30, 120 s
10 kHz – 1 kHz	$\sim 2 \mu\text{rad}$	30, 120 s
1 kHz – 100 Hz	$< 1 \mu\text{rad}$	50, 200 s
< 100 Hz	$< 0.1 \mu\text{rad}$	20, 40 s

\*conditions may vary with DVM's measurement range, aperture time, and the total no. of samples ( $MN$ ) chosen.

the plot indicates abruptly the presence of flicker noise as  $\tau$  increases beyond 40. Phase determinations can though be improved by averaging blocks of data with 40 measurements each. Fig. 10 indicates that at 500 kHz, the  $10 \mu\text{rad}$  marking may be attained by averaging 40–50 measurements (provided white noise conditions apply). The procedure is repeated for 99.936 kHz, where phase standard deviations of only some microradians are attainable for  $\tau$  near 30 measurements.

At this point, it is not necessary to become repetitive and to show Allan standard deviations of phase for all frequencies of Table I. The experimental findings for other frequencies are summarized in Table II and are valid for the same aforementioned conditions. There is also not an abrupt change in the attainable standard deviations as the reader might suppose. The table was set up for the discrete frequency values of Table I and should be viewed as a guide only. Obviously, such estimates can be reduced as the number of blocks of measurements grows (under white noise conditions). For frequencies below 1 kHz up to some MHz, the heuristic values were obtained from [13].

#### IV. DIGITAL PHASE ALIGNMENT BETWEEN CHANNELS

Once the signals are frequency synchronized by making  $f_n$  and  $f_s$  "commensurate" within a negligible  $\xi$ , any phase

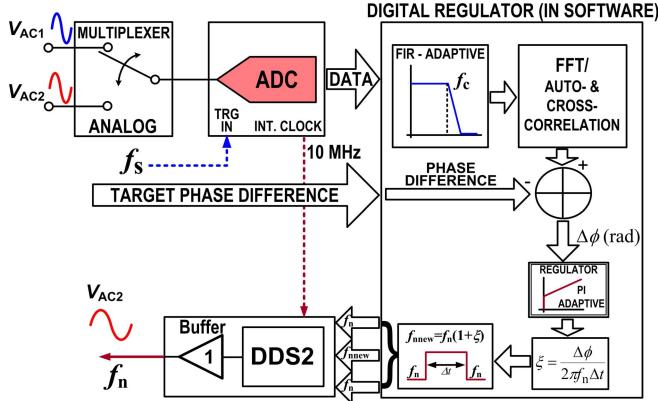


Fig. 11. Digital phase alignment regulator (see text).

angle between  $v_{AC1}$  and  $v_{AC2}$  can be digitally adjusted or “synthesized” with an accuracy far superior than that attainable by generators based on DACs, whose phase synthesis is based on shifting addresses of code stored in random-access-memories. The phase synthesis of the standard in Fig. 1 is done by a digital phase regulator [13] as explained next. Fig. 11 shows the schematics of the digital regulator, which is basically an algorithm (at the right part of Fig. 11) that operates on data of a multiplexed ADC. The data are filtered by an adaptive finite-impulse response (FIR) of maximum 13 stages to filter noise with a cutoff frequency  $f_c$  set to about ten times the fundamental frequency of the signals. As it acts on both signals, no phase difference between signals is produced by the FIR-filter. In sequence, the data are fast-Fourier transformed or cross correlated (if desired), where the phase between signals is computed and compared with the desired phase set by the user and stored in the input parameter “target phase difference.” It uses the same principle as outlined before, that phase shifts of sine waveforms can be produced by minute frequency variations with a fractional frequency error or correction coefficient  $\xi$ . The phase difference is led to a proportional-integrative (PI) regulator, which starts with unitary gain and integrative constant equal to zero. If the phase difference is not zero, a fractional error  $\xi$  is computed and the output frequency of DDS2 suffers a change to  $f_n$   $(1 + \xi)$  over a predefined time interval  $\Delta t$  (usually equal to 1 s) to make  $v_{AC2}$  to advance or recede in phase by the necessary phase difference to produce the desired phase difference between signals. The process repeats many times, and after a predefined number of repetitions set by the user (e.g., five), the PI regulator starts integrating the signal with its registers discharged, i.e., starting with small values because the proportional regulator already made the gross adjustment. This speeds up measurements considerably. In sequence, the knowledge of the number of averages for reliable phase measurements, as shown in the last section, becomes valuable. After some iterations to make the phase closer to the target phase, the number of averages is raised as demonstrated in Section III (provided white noise conditions hold), and the estimations of phase are used to force the PI regulator to adjust the phase within a threshold of some microradians, as defined

by the user. Therefore, any phase between 0 and  $2\pi$  can be set with negligible systematic deviations and with the lowest attainable standard deviations (if desired) as stated in Table II.

The regulator was experimentally verified with a programmable Josephson voltage standard [13] for the phase alignment of signals to be calibrated by differential measurements and in a digital impedance bridge [28], which demanded very accurate phases to be adjusted and determined, sometimes bearing within  $\pm 1 \mu\text{rad}$  or some nanoradians. Due to the phenomenal DDS’ resolution and adjustment sensitivity as shown in Section III, any phase can digitally be set by the digital regulator of the system by specifying a target phase (after a zero adjustment is made to purge almost totally the phase systematic errors by making  $f_s$ —within some parts of  $10^{-15}$  or smaller—commensurate with  $f_n$ ).

Accurate phase synthesis using a single multiplexed DVM (according to Figs. 1 and 11) requires that the impedance loading at the output of DDS1 and DDS2, delivering  $v_{AC1}$  and  $v_{AC2}$ , respectively, be matched. At higher frequencies (in the range of some kilohertzes and above), the loading due to the DVM’s input impedance and mismatches of the DDSs’ output impedance may cause systematic deviations on phase. In order to counteract such effects, the multiplexer has additional relay contacts that alternately places a dummy load with a value close to the DVM’s nominal impedance at the other DDS, whose output is not being sampled while the other is selected (not shown in Figs. 1 and 11 for the sake of simplicity). After  $f_n$  and  $f_s$  are made commensurate, a zero phase adjustment is thus also important to compensate for DDS loading effects. This compensation technique has proved to be valuable when measuring impedances with a digital impedance bridge [28]. A similar approach applies for compensating the load of a phase meter (as a device under test) whose inputs are placed at the DDSs’ outputs.

## V. MEASUREMENT UNCERTAINTIES

Theoretical investigations on Cramer–Rao lower bounds (CRLB) [29], on DDSs, and noise indicate best uncertainties of a few microradians up to the megahertz range to be attainable, provided that a large set of data samples are used. This depends on the signal frequency, as demonstrated in Table II. The signals  $v_{AC1}$  and  $v_{AC2}$  should have the same amplitude, otherwise nonlinearities of the DDSs and DVM may cause systematic deviations on phase. In this section, the attempt for evaluating measurement uncertainties is made for a block of repetitions  $\tau = 100$  of phase determinations at 1.000032 MHz.

The first component is the noise of the DDS synthesizers. Measurements indicated that the lowest attainable signal-to-noise ratio ( $SNR$ ) was greater than 80 dB [obtained from measurements as follows: FFT noise floor of  $-76$  dB plus FFT noise compression or processing gain of 27–31 dB due to fold back of aliased noise components, resulting in an  $SNR$  of 80 dB, i.e.,  $(-76 + 27 - 31)$  dB =  $-80$  dB of noise-to-signal ratio]. This is many times a better performance than the previously expected (of around 60 dB). The combination of two sources results in a total noise contribution of  $-74$  dB.

The second component is the  $SNR$  of the DVM used in the measurements. Specifications indicate an  $SNR$  greater

than 66 dB (for an input signal at 20 kHz). Measurements using audio sources indicated, however, an *SNR* estimate of about 70 dB. The contribution of a generator and DVM results thus in a combined *SNR* of 68 dB. Since the DVM bandwidth (of 12 MHz in the DSDC sampling mode) is much higher than the signals' frequency, the amplitude attenuation in the DVM's input circuitry is not pronounced.

Since the FFT on data is made, estimations of spectral components of the signal are indeed affected by noise, which are "compressed" depending on the total number of samples  $MN$  ( $M$  periods times  $N$  samples per period) employed in the record. FFT noise compression or FFT processing gain [30] on data is denoted by  $NC$  and expressed in dB as

$$NC = 10 \log_{10} \left( \frac{MN}{2} \right). \quad (5)$$

Subsampling, however, has some drawbacks. It increases noise in the first Nyquist zone (i.e., in the bandwidth from 0 to  $f_s/2$  Hz), because the signal's frequency components in the other Nyquist zones ( $f_s/2 - f_s, f_s - 3f_s/2, \dots$ ) fold all back onto the first Nyquist zone. Any spectra on odd Nyquist zones are folded back onto the first without inversion of that portion of the spectra, whereas spectra on even Nyquist zones are folded back with the inverted spectra with respect to their origin. This means that all noise components on every Nyquist zone combine altogether in the first one. It is assumed here, that all folded back noise components (on the first Nyquist zone) combine quadratically. Taken this assumption for granted, an  $f_n$  signal of 1.000032 MHz aliased at 96 Hz according to (1) and sampled at a rate  $f_s$  of 1.536 kHz (the Nyquist bandwidth of 768 Hz) is located in the 1303th Nyquist zone. Noise contributions all combined raise noise level by  $(1303)^{1/2} \sim 36$  or 31 dB in the first Nyquist zone.

In the light of such noise effects, uncertainty contributions due to ADC's quantization were neglected.

Finally, there is the contribution of sampling jitter  $SJ$ , which for a signal of magnitude equal to the ADC's full scale  $FS$  may be estimated (at the zero crossing of a sine) as

$$SJ = 2\pi f_n FS \delta \quad (6)$$

where  $\delta$  stands for a root-mean square timing fluctuation of the  $f_s$  sampling clock. A time jitter  $\delta$  of approximately 50 ps may be attainable by appropriate filtering of DDS3.

As a reference for our calculations, it is worth recalling the *CRLB* variance estimation for a polynomial phase signal affected by Gaussian noise [29]. It furnishes an estimation of the best attainable standard deviation (or uncertainty under white noise conditions) of the phase for a sine waveform sampled under Gaussian noise for a given number of samples  $MN$ . The *CRLB* is expressed as

$$CRLB = \frac{1}{2MN(SNR)^2}. \quad (7)$$

In the specific case,  $M$  is 64 periods sampled with  $N$  equal to 16 samples per period, totaling 1024 samples and *SNR* is 68 dB (due to the 80-dB contribution of the source and 70 dB from the sampler or DVM) what yields a *CRLB* of 7.74e-11 or a standard deviation of  $(CRLB)^{1/2} = 8.8 \mu\text{rad}$ .

TABLE III  
EVALUATION OF PHASE MEASUREMENT UNCERTAINTIES 1.000032 MHz

Contribution	Estimation	Value (V)	Squared Contrib.
<i>SNR</i> of source	-80 dB of FS	0.0001 FS	
Rise of noise alias <sup>1</sup>	$*(1303)^{1/2}=36$	0.0036 FS	
FFT $NC^2$	$*1/22.6$	0.00016 FS	
Reduction of rep <sup>3</sup>	$*1/10$	<b>1.60E-05 FS</b>	$=>(1.60E-5)^2FS^2$
ADC's <i>SNR</i>	-70 dB of FS	3.16E-4FS	
Rise of noise alias <sup>1</sup>	$*(1303)^{1/2}=36$	1.14E-2 FS	
FFT $NC^2$	$*1/22.6$	5.03E-4 FS	
Reduction of rep <sup>3</sup>	$*1/10$	<b>5.03E-5 FS</b>	$=>(5.03E-5)^2FS^2$
Clock Jitter	$2 f_i FS$	3.14E-4 FS	
Rise of noise alias <sup>1</sup>	$*(1303)^{1/2}=36$	0.0113 FS	
FFT $NC^2$	$*1/22.6$	0.0005 FS	
Reduction of rep <sup>3</sup>	$*1/10$	<b>5.00E-5 FS</b>	$=>(5.00E-5)^2FS^2$
Total quadratic sum of contributions		5.29E-9 FS <sup>2</sup>	
Total quadratic sum of contributions for two channels		$2^2 \cdot 5.29E-9 FS^2$	
Effective signal-to-noise ratio <i>SNRe</i> <sup>4</sup>		9726 or 79.7 dB	
<b>Uncertainty of phase <math>s_\phi</math> is <math>1/SNRe</math></b>		<b>103 <math>\mu\text{rad}</math></b>	

DVM's full-scale  $FS$ : 10 V.

Amplitude of sources  $V_{AC1}$  and  $V_{AC2}$  in volt: FS.

Total no. of samples  $MN$  in one record of  $V_{AC1}$  and  $V_{AC2}$ : 1024.

<sup>1</sup>Rise of noise due to fold-back of an integer no. of  $2^*f_n/(f_s)$  Nyquist zones.

<sup>2</sup>FFT  $NC$  stands for noise compression due to the fast-Fourier transform.

<sup>3</sup> $\tau$  stands for the number of measurement repetitions (rep.): 100.

<sup>4</sup> $SNRe$  is  $FS / (\text{Total quadratic sum of contributions for two channels})^{1/2}$ .

Because we use two blocks of sampled data affected by equal noise contributions, the number two in the denominator of (7) can be suppressed and the resulting estimation is  $(CRLB)^{1/2} = 12.4 \mu\text{rad}$ . Note that this estimation is much smaller than the attained Allan standard deviations, as shown in Fig. 5. This is because there are other contributions to the measurement uncertainty of phase  $s_\phi$  as previously outlined. Table III summarizes all contributions together showing how  $s_\phi$  is calculated step by step using the former expressions. The final estimated uncertainty is nearly two times that of the Allan standard deviation for  $\tau$  equal 100 (see Allan standard deviations plot of Fig. 5). The conservative noise contribution estimations and the assumption that the contributions of noise are quadratically folded back (as "rise of noise alias" in Table II) indeed overestimates uncertainties of phase. A rise of noise alias of 18 (or 25 dB) instead of 36 (or 31 dB) would result in an uncertainty figure of nearly 50  $\mu\text{rad}$ , i.e., in better agreement with Fig. 5. Further investigations are in course to understand such phenomena, including the effect of DDS' spectral spurs on phase determinations using subsampling.

## VI. CONCLUSIONS AND OUTLOOK

The feasibility of the present system was extensively corroborated by experimental investigations, and an attempt to access measurement uncertainties was made with real measurement data and instrument specifications. It was demonstrated that high-grade phase measurements can be done with subsampling in a wide range of frequencies up to the megahertz range using alias detection, i.e., using a much lower sampling frequency than that one required by the Nyquist theorem, which still holds. The high frequency signal is synchronously sampled, but more spaced in time only. This means, spending many periods between samples without leakage effects.

Due to the successive folding back of noise onto the first Nyquist bandwidth, noise reduction (or compression) can only be attained at the expense of using a large number of samples, provided Gaussian (white) noise conditions hold. Systematic errors may be reduced by attaining a sampling frequency commensurate with the signal frequency by an infinitesimal fractional frequency error. Despite efforts to purge residual systematic errors during zero phase adjustments of the system, a residual error always remains, because of remaining DDSs' truncation errors. Such residuals do not represent a drawback, since they are usually negligible and can be compensated numerically if desired.

Finally, after a zero phase adjustment of the system, any phase angle can be "synthesized" with the help of a digital phase regulator, which is able to set phases with dispersions (standard deviations) approaching the figures of Table II. Further improvement may be attained with externally triggered DACs for generating  $v_{AC1}$  and  $v_{AC2}$  with DDS1 and DDS2 delivering their sampling clock. This was successfully investigated with low-distortion audio sources [28].

The method may help tackling difficult phase measurements at higher frequencies, and find application in a new multifrequency impedance bridge under development, in the characterization of sensors and transducers at higher frequencies, in the measurement of ac power and energy at high frequencies (from power line frequency to the megahertz range, provided transducers are properly tailored), and in time-and frequency keeping tasks, to cite a few examples.

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**Waldemar G. Kürten Ihlenfeld** was born in União da Vitória, Brazil, in 1960. He received the B.E. degree in engineering from the Federal University of Paraná, Curitiba, Brazil, in 1983, and the M.E. degree in engineering, and the Ph.D. (*magna cum laude*) degree in electrical engineering from the Braunschweig University of Technology, Braunschweig, Germany, in 1994 and 1997, respectively.

From 1983 to 1999, he was with the Central Laboratory–LAC, a research institute of the Federal University of Paraná and the power utility company of Paraná, south of Brazil. From 1999 to 2013, he was with the Physikalisch-Technische Bundesanstalt, Braunschweig, where he was involved in the research and development of precision electronic circuits for ac power measurements, the mathematical modeling of sampling systems, digital signal processing, investigations on electro-thermal modeling of semiconductor devices, and hardware development. Since 2016, he has been with the Electrical Metrology Division, Brazilian National Institute of Metrology, Quality and Technology, Duque de Caxias, Brazil.