Investigation of a Microprocessor Chip Cooling System

ABSTRACT

As microprocessors advance, they become smaller and more powerful and require greater power dissipation which necessitates improved cooling systems. In order to create a more efficient cooling system, we studied how the resistance and heat transfer of a chip change with temperature, and how the resistance is affected when the chip is attached to a heat-sink in a wind tunnel with varying wind speed. We found that our experimental results were similar to out calculated theoretical results. From the experimental results, we were able to develop a heat transfer model which can predict the resistance of the chip to the ambient air as a function of air velocity and the maximum heat transfer to prevent chip failure.

INTRODUCTION

Well-modeled heat transfer models are required to prevent microprocessor failure. To find how a microchip's heat transfer and resistance vary with changes in temperature, we conducted experiments that simulate microprocessor heating. The purpose of this report is to find both theoretical and experimental values of the thermal coefficient of our chip, the time constant to reach steady state temperature, the chip-to-ambient resistance (and its components), and then to develop a heat transfer model to predict the resistance of a chip to ambient air as a function of air velocity and fin length. Lastly, using our data and knowledge of heat transfer, we would like to recommend different approaches to allow better cooling of the system.

NOMENCLATURE

(see Appendix A on p. 4)

METHODS

Experiment 1: Obtaining α with bare die sample

In the first experiment, we attempted to calculate the thermal coefficient of resistance of our microprocessor chip (shown in Appendix M, p. 9) by calibrating the electrical resistance of the sensor on the chip as a function of surface temperature. The chip was fixed to a hot plate using thermal grease and electrical resistance was measured using the '4-point probe method'. Surface temperature was measured using an Omega HHI2 thermocouple, placed on the resistor pattern by the researchers. Initial chip resistance was found after applying a voltage of VDC ~ 100 mV. The resistance was then measured at a temperature range of 30 °C to 120 °C, since we did not want to reach 150 °C, the estimated failure temperature of the chip. Because of the unsatisfactory results, we redesigned our test procedures.

Experiment 2: Obtaining α with ceramic packaging and $R_{chip\text{-}to\text{-}heat\ sink}$

Our improved test setup used an integrated circuit packaging which had mechanical support, electrical shielding, and permanent connection of leads for robustness. Appendix K on p. 9 shows a photo of the setup and equipment used. We repeated the procedure in Experiment 1with a smaller range of 22 °C and a smaller maximum temperature to avoid damaging the chip.

Experiment 3:

In Experiment 3, we applied voltages to the on-chip resistor pattern ranging from 5 to 25V in increments of 5V and determined the surface temperature of the chip by measuring its current draw. The heat-sink temperature was measured using our thermocouple. We collected data from three trials.

Experiment 4:

In the last experiment, we tested our chip with an Alpha Novatech S-1530 20W heat-sink (cut in quarters) in a model wind tunnel (Appendix J, p. 8). We measured different flow rates using an anemometer by varying the voltage, from 6V to 12V in increments of 2V, supplied to the fan and measured corresponding current. We then theoretically estimated the chip temperature, T_{chip} using results from Experiment 2 when

the chip was held at voltages of 9.71, 14.55 and 19.41V. We calibrated the air velocity V_∞ as a function of power input to the cooling fan.

RESULTS

Obtaining α: Experiments 1 and 2

From Experiment 1 we assumed a proportional fractional change in resistance to the temperature change by a coefficient, α, as shown in Eq. 1.

$$\frac{\Delta R}{R_0} = \alpha \Delta T \qquad \text{(Eq. 1)}$$

Using Eq. 1 our calculated α had large errors and inconsistencies between data sets, and was considered to be skewed. The results of Experiment 1 are shown in appendix C on p. 6.

From Experiment 2, with the ceramic wire-bonded chip packaging, our initial resistance value was 291.78 ± 0.02 Ω at 22 °C and α was 0.00283 ± 0.00035 1/°C. Using Eq. 2, where *i* represents each trial and α is the mean of all the α_i, we found α = 0.003437 ± 0.00085 1/°C. The plot of *R* vs. *T* is shown in Appendix D on p. 6.

$$R_i = R_0[1+ \alpha_i(T_i-T_0)], \qquad \text{(Eq. 2)}$$

Heat transfer and the resistance from the chip to the heat-sink was calculated using Eqs. 3 & 4.

$$Q_H = VI \qquad R_{chip\text{-}to\text{-}heat\ sink} = (T_{chip} - T_{heat\ sink})/Q_H \qquad \text{(Eqs. 3\&4)}$$

We found $R_{chip\text{-}to\text{-}heat\text{-}sink}$ was 9.986 ± 1.154 W/K. Heat transfer vs. Δ*T* is plotted in Appendix E on p. 7.

To determine the time constant for the chip to reach steady state temperature we used Eq. 5.

$$\tau = R_{chip\text{-}to\text{-}heat\ sink}\ C_{packaging,} \qquad \text{(Eq. 5)}$$

where $C_{packaging}$ is the capacitance of the ceramic (Appendix B, p. 5). Experimentally, the time constant was 4.62 ± 0.53 s, which was calculated using the experimental resistance value and the theoretical capacitance. This is close to the theoretical value of τ = 3.95 s.

Resistance: Theoretical Calculation: Experiments 3 and 4

Our theoretical calculation for the chip-to-ambient resistance was modeled as a sum of the resistance from the conduction in the chip (silicon) the contact resistance from the silicon to the aluminum, the resistance from the conduction in the base of the aluminum heat-sink, and the equivalent resistance of the convection from both the base top surface and the fins of the heat-sink. For the contact resistance, we used the top surface area of the chip, which was less than the heat-sink base area, and a contact resistance given in Appendix F on p. 7. For modeling the resistance of the heat-sink, we approximated the fins as cylinders because we were unable to find square geometry constants at the tested Reynolds numbers for use in calculating Nusselt number *Nu* using the Hilpert correlation [3]. Also, because our chip had fewer than 20 fins, we multiplied *Nu* by a correction factor *C*, as shown in Eq. 6. The electrical circuit diagram of the system can be seen in Appendix H on p. X (all physical constants and coefficients used are given in Appendix A on p. X). Reynolds number Re_D was calculated using Eq. 7 below.

$$< Nu >_W = C < Nu >_D = Ca_1 Re_D^{a_2} Pr^{1/3}, \qquad Re_D = \frac{u_{f,\infty} D}{v_f}, \qquad \text{(Eqs. 6 \& 7)}$$

where $u_{f,\infty}$ is the maximum velocity between the fin cylinders. From Eq. 5 we were able to find conduction coefficients, the heat-sink total efficiency, and ultimately the heat-sink resistance. The resistance values are summarized in Appendix F on p. 7.

Resistance: Experimental Results: Experiments 3 and 4

Using our data from Experiment 4, we used the divided ΔT by Q_H to solve for $R_{chip\text{-}to\text{-}ambient}$. In Fig. 1 we plot the $R_{chip\text{-}to\text{-}ambient}$ vs. air velocity for both our theoretical calculations and measurements from Experiment 4 at chip voltages of 9.71, 14.55 and 19.41V. The experimental data follows the same trend as the theoretical data as well as the manufacturer's data for the resistance of the heat-sink alone [2]. For the range of tested velocities, the percent error of our experimental versus theoretical resistances never exceeded 12.5%. In our plot, uncertainty is due to error in measurements of current and voltage and to resolution and precision error in the anemometer readings.

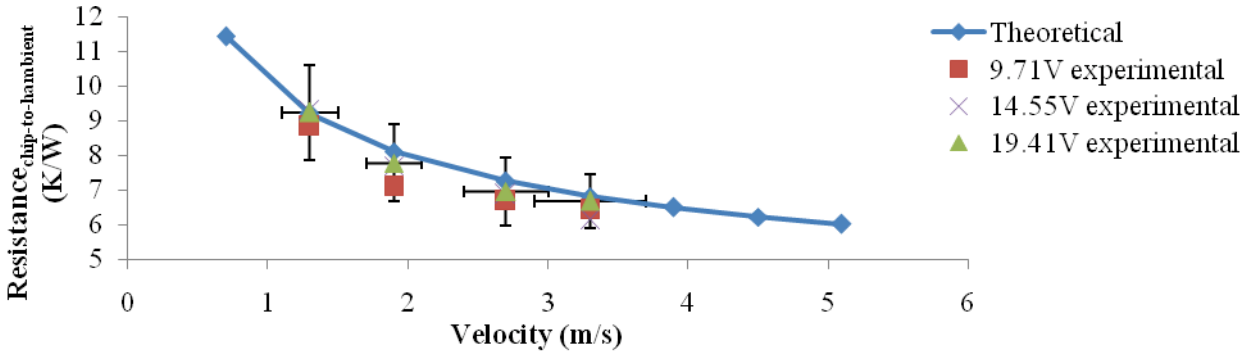


Fig. 1: Theoretical and experimental resistances vs. velocity for three voltages. Resistance does not appear to vary significantly with voltage.

Assuming fatal failure occurs at a chip temperature T_{chip} = 150 °C, we calculated maximum allowable chip heat exchange for our tested velocities using Eq. 6. The results are shown in Table 1. As expected, maximum allowable chip power Q_{Hmax} increases with increasing air velocity.

$$Q_{Hmax} = (A_b + A_f n_f) < Nu >_w \frac{k_f}{w}(T_{chip} - T_{air}) \qquad \text{(Eq. 6)}$$

V_∞ (m/s)	Q_{Hmax}
1.3	16.66
1.9	19.42
2.7	22.30
3.3	24.11

Table 2: Maximum chip heat transfer for tested air speeds.

DISCUSSION

The alpha obtained from experiment 2 was more accurate than from experiment 1 because we used a proper 4-point probe setup. This decreased the parasitic resistance, therefore lowering the initial and measured resistance. More importantly, we obtained the data without damaging the chip. In experiment 1, we scratched the surface of the resistor of the chip we were measuring, sometimes so severely that the resistance would increase dramatically between different attempts at the same temperature. The large temperature range also contributed the larger discrepancies from the linear model we were attempting to

validate. We found the best alpha value for the second experiment using the normalized slope of R vs. T as it produced the smallest error.

The theoretical time constant, $\tau = 3.95$ s, was smaller than the experimental value, 4.62 ± 0.53 s, possibly because the ceramic volume used to calculate ceramic resistance was estimated as that beneath the chip. The experimental resistance was also higher than the theoretical one which could contribute to the larger experimental time constant. They were within 17% of each other, which was considered satisfactory. Our theoretical results imply a required time of ~ 20 s to reach 99% of steady state. We may not have waited this long during the experiment, which may have added error to our results.

We were able to develop a heat transfer model which could predict $R_{chip\text{-}to\text{-}ambient}$ for a given air velocity with increasing accuracy as the velocity is increased. Our experimental and theoretical calculations for $R_{chip\text{-}to\text{-}ambient}$ vs. V_∞ are closely related quantitatively and in trend, showing the validity of our model. They also agree with the trend given by the manufacturer: as the air velocity is increased, so does the maximum allowable chip power. This is valid as increased velocities would increase heat dissipation from the heat sink. Also, it was not surprising that the experimental resistances were slightly higher than the theoretical calculations which could be manufacturing inconsistencies. It appears that the resistance of the total system was not dependent on the chip voltage, which makes sense physically.

CONCLUSIONS & RECOMMENDATIONS

The results of our experimental and theoretical calculations for the S1530 20W heat-sink have close agreement and we have calculated maximum heat transfers to prevent failure versus velocity (Table 2 on p. 4). For increased chip cooling, resistance can be lowered by increasing the fin length and/or spacing, increasing the profile area, or use of a higher conductivity fin material, such as copper or graphite [4]. Our studies show that there is a threshold length of 120 mm beyond which increasing fin length does not help (see Appendix L on p. 10). Enhanced convection from a faster or nearer fan or liquid cooling can also help. Other options include refrigeration/solid-state refrigeration if packaging space is not a limiting factor.

APPENDICES

Appendix A

Symbol	Definition
a	Geometry coefficient in Nusselt calculation

A	Area
C	Correction factor in Nusselt calculation
D	Diameter of cylinder (width of fin)
Q	Heat transfer
k	Conductivity
R	Resistance
u	Velocity
m	Ratio of solid-conduction to surface-convection
N_f	Number of fins
Nu	Nusselt number
Pr	Prandtl number
Re	Reynolds number
α	Thermal coefficient of resistance
η	Efficiency
τ	Time constant
υ	Kinematic viscosity

Table 1. List of symbols used

Appendix B

Constant, Coefficient	Value
k_{Al} *(aluminum)*	180 W/mK [3]
k_{Si} *(silicon)*	148 W/mK [3]
k_{air} *(air)*	26.3×10^{-3} W/mK [3]
$k_{ceramic}$ *(ceramic)*	18 W/mK [3]
a_1	0.683 [1]
a_2	0.466 [1]
C	0.99 [3]
N_f	16
Pr (22 ºC)	0.715 [3]
$R''_{Al\text{-}Si}$	0.9×10^{-4} m^{2}K/W [3]
υ_{air} (22 ºC)	1.5295×10^{-5} m^2/s

Table 2. List of constants/coefficients used

Appendix C

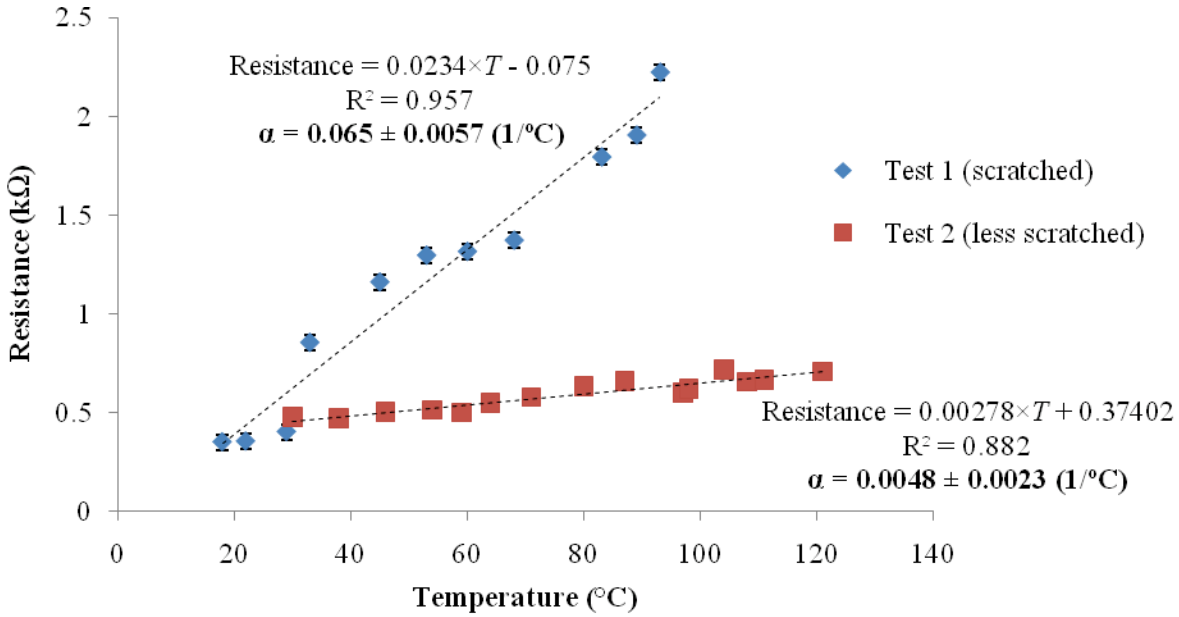


Fig. 3: Experiment 1: Thermal coefficient of resistance using bare die sample. Notice large discrepancy between slopes of two tests.

Appendix D

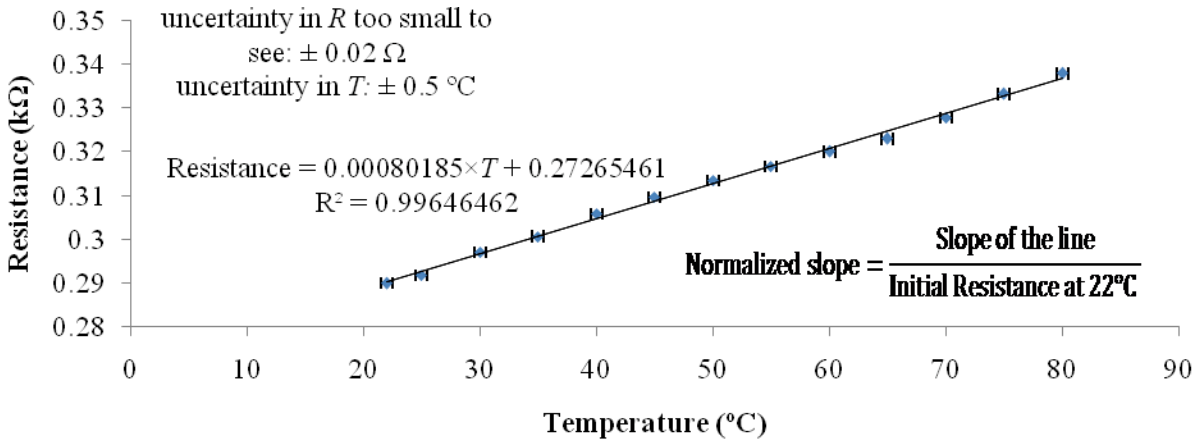


Fig. 4: Experiment 2: Resistance vs. temperature for the on-chip resistor pattern (using ceramic packaging sample).

Appendix E

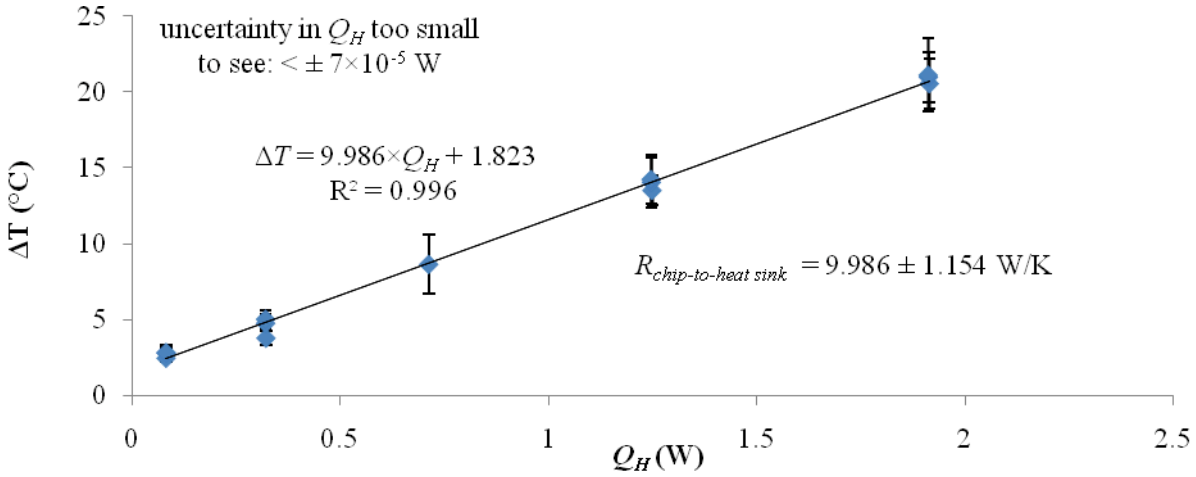


Fig. 5: ΔT vs. Q_H for the ceramic packaging

Appendix F

Resistance, ceramic (Experiment 2)	0.1234 K/W
Resistance, Al heat-sink base (conduction)	0.058 ± 0.013 K/W
Capacitance, packaging, ceramic	0.463 J/K
Resistance, Si chip (conduction)	0.048 ± 0.002 K/W
Resistance, Si-to-Al (contact)	1.406 ± 0.547 K/W

Table 3: Theoretical conduction/contact resistances and other values

Appendix G

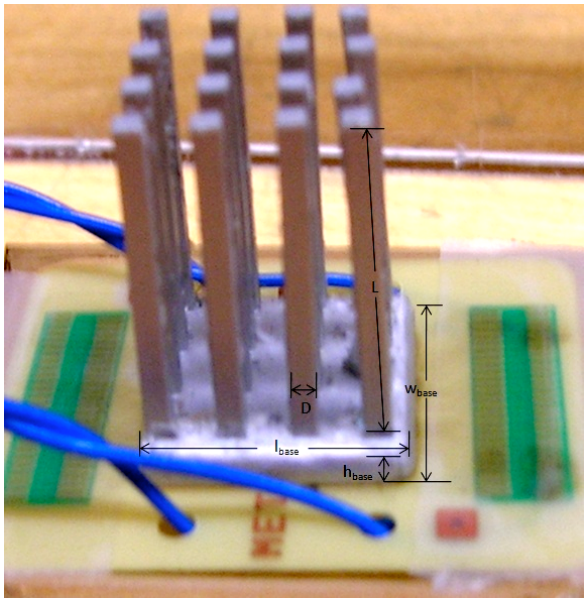


Fig. 6: The heat-sink dimensions

Appendix H

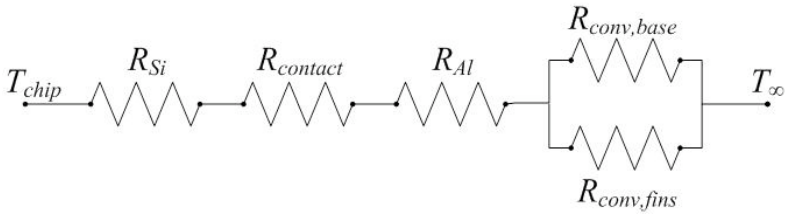


Fig. 7: The equivalent resistances of the model

Appendix I

$m = (\frac{P_{ku} < Nu >_w k_f}{A_k k_s D})^{\frac{1}{2}}$ **ratio of solid-conduction to surface-convection resistance**

$P_{ku,f} = \pi D$ **surface-convection perimeter for each fin**

$L_c = L + \frac{D}{4}$ **corrected length for circular fin**

$n_f = \frac{\tanh(mL_c)}{mL_c}$ **fin efficiency**

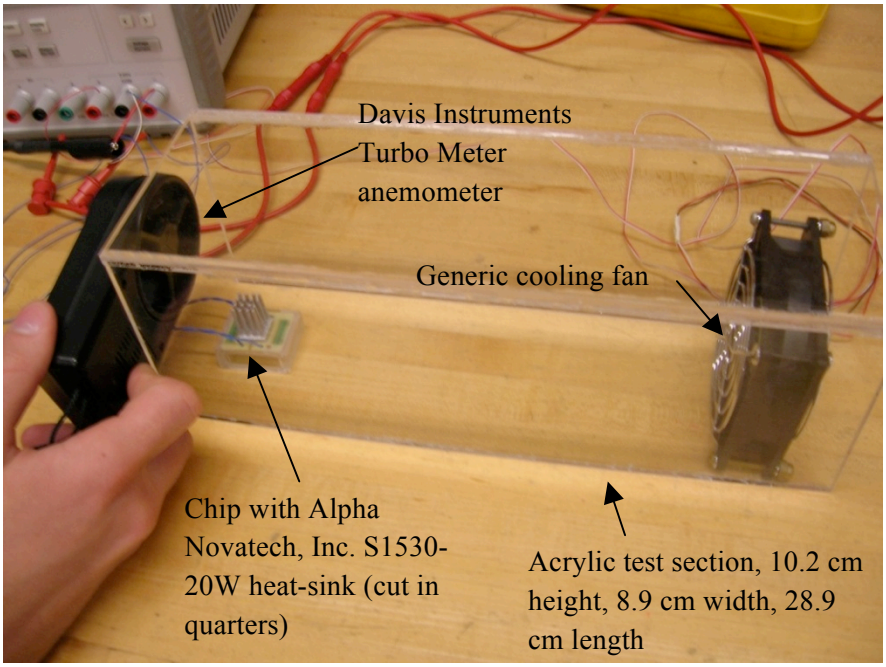
$\frac{1}{R_\sum} = \frac{1}{R_{ku,b}} + \frac{1}{R_{ku,f}}$ **resistances in parallel**

$R_{ku,b}^{-1} = A_b < Nu >_w \frac{k_f}{D}$ $R_{ku,b=}$ **= base-surface resistance,** $A_b = A_{base} - N_f A_k$

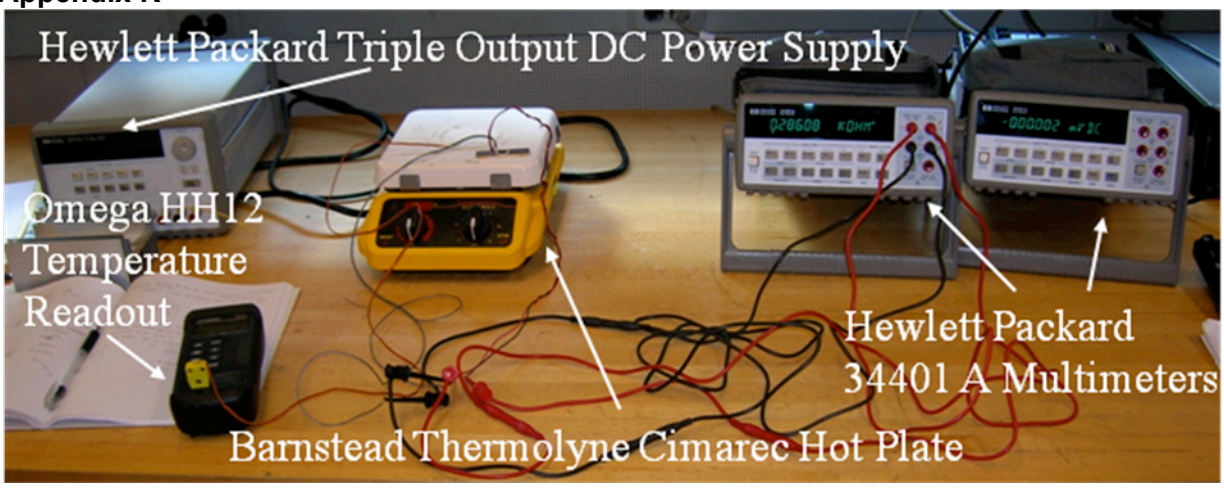
$R_{ku,f}^{-1} = A_f n_f < Nu >_w \frac{k_f}{D}$ $R_{ku,f}$ **= fin-surface resistance,** $A_f = N_f P_{ku,f} L_c$

$Q_{Hmax} = (A_b + A_f n_f) < Nu >_w \frac{k_f}{w} (T_{chip} - T_{air})$ **maximum allowable chip power**

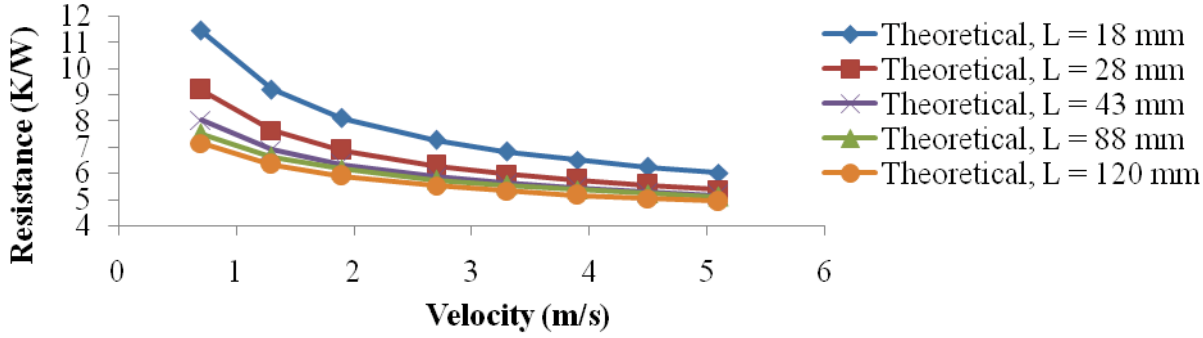
Appendix J



Appendix K

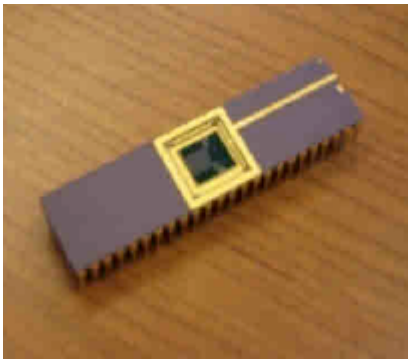


Appendix L



Theoretical Chip-to-ambient resistances with increasing fin length.

Appendix M



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[2] "S Series Omnidirectional Heat Sinks," Alpha Novatech, Inc., https://www.micforg.co.jp/dxf/S.pdf, Mar. 10, 2008, p. 4.

[3] Incropera, F. P., DeWitt, D. P., Bergman, T. L. and Levine A. S., *Fundamentals of Heat and Mass Transfer*, John Wiley: Hoboken, New Jersey, 2007, p.112, 426, 439.

[4] Mahajan, R., Chiu, C., and Chrysler, G., "Cooling a Microprocessor Chip," *Proceedings of the IEEE*, Vol. 94, No. 88, Aug. 2006, pp. X-X.