

60GHz TRANSMITTERS

by

Michael J Boers

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Department of Electronic Engineering
Faculty of Science
Macquarie University
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Abstract

Wireless systems offer the freedom to move around a home, an office or outside while maintaining connectivity to a network. They have revolutionised the way we work and play. Inside the home and office, wireless LAN systems provide internet access, enable video streaming and backup to the cloud. The push for faster wireless systems is driven by the desire for high quality media streaming, quicker wireless sync and back-up as well as a perennial need for the latest and greatest gadget and is enabled by high speed interfaces (PCIe gen II) and fast storage devices (solid-state drives (SSDs)). The recently ratified 802.11ad standard supports throughputs of up to 6.7 Gbps on 2 GHz wide channels providing a path to high speed, standardised wireless systems for consumer applications.

At the time the majority of the work in this thesis was done (2006-2010), there were no consumer wireless systems faster than a few hundred Mbps. This work in this thesis aims to develop key components for a 60 GHz transmitter (TX) as well as an architecture amenable to integration in a consumer device than can operate at a rate greater than 1 Gbps.

The introduction and following two chapters provide the motivation, application and background of 60 GHz links as well as an introduction to Silicon technology and a system level analysis of transmitters and phased array systems.

A key component in 60 GHz wireless systems is the power amplifier (PA). The PA uses a significant amount of power (especially in a phased array) and is responsible for driving the antennas. Three power amplifiers are described in Chapter 4.

Chapter 5 outlines two different architectures for 60 GHz systems, including implementation details and measurement results.

Finally a conclusion and suggestion for future work is outlined in Chapter 6.

Certificate of Originality

I certify that the work in this thesis entitled “60GHz Integrated Transmitter Design on Silicon” has not previously been submitted for a degree nor has it been submitted as part of requirements for a degree to any other university or institution other than Macquarie University.

I also certify that the thesis is an original piece of research and it has been written by me. Any help and assistance that I have received in my research work and the preparation of the thesis itself have been appropriately acknowledged.

In addition, I certify that all information sources and literature used are indicated in the thesis.



Michael J Boers

February 2014

Dedication

Dedication here.

Acknowledgements

Add Your Acknowledgements here!

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1

Introduction

“A device called a transistor, which has several applications in radio where a vacuum tube ordinarily is employed, was demonstrated for the first time yesterday at Bell Telephone Laboratories...”

– New York Times, 1948

1.1 Motivation

Since the demonstration of the first transistor in 1948, integrated circuits (ICs) have ridden a wave of development and innovation unparalleled in our history. They power

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the devices we use for entertainment, control our modes of operation, helped put man on the moon and enable us to talk with relatives on the other side of the world.

Of all the IC technologies it is Silicon, primarily complementary metaloxidesemiconductors (CMOS) with its generation-to-generation scaling (as observed by Moore) which provides the platform for smaller, higher performance and lower cost circuits that enable these devices to get faster, smaller and cheaper each year. With these generational improvements comes a desire to push the boundaries and explore new applications at higher frequencies.

Until the 130nm CMOS and 180nm Silicon Germanium (SiGe) nodes, Silicon technology was limited to applications well below 60 GHz due to slow (relatively speaking) transistor speed. As each generation progresses past these nodes, millimetre wave circuits that were once the domain of military applications [19] and point-to-point links [20] and typically implemented using type III-V semiconductors such as Gallium Arsenide (GaAs) and Indium Phosphide (InP), are now able to be implemented in Silicon. Silicon implementations enable applications in mass-markets such as the personal computer (PC) and cellphones due to the extremely low cost.

Technology	F_t (GHz)	F_{max} (GHz)	NF_{min}
Jazz SiGe 0.25um	75		
Jazz SiGe 0.18um	150		
Jazz SiGe 0.13um	200		
ST SiGe 0.13um	220	290	1.2
ST CMOS 65nm LP	175	325	1.2

Table 1.1: Overview of Silicon processes [15, 16].

The opening of 7 GHz contiguous bandwidth at 60 GHz and the performance of advanced CMOS [21] and SiGe [22] nodes paves a clear path to 60 GHz adoption for several applications.

This motivation for this thesis is the Silicon implementation of Gbps communication systems for both consumer wireless local area network (LAN) and low cost point-to-point links at 60 GHz. This thesis focuses on millimetre wave transmitters at the system and circuit level.

1.2 Applications

Many of the devices we use today employ wireless technology. With each generation of new devices there is a desire for higher throughput to reduce download time, increase performance and provide bandwidth for new applications. Wireless LAN (WLAN) was first implemented in the early 2000's. At inception it supported a few Mbps (11g) and has scaled to nearly 1 Gbps (11ac) today. The performance of WLANs will continue to improve but due to the low bandwidth per channel, high spectral efficiencies and MIMO systems will be required for speeds greater than 1 Gbps.

A 60 GHz system provides higher throughput at a much lower spectral efficiency than existing wireless systems. The 802.11ad specification provides for data rates up to 6.7 Gbps on 2 GHz wide channels [13]. There are several applications which can benefit from this high data rate, they are outlined below.

Wireless docking

60 GHz technology can enable wireless docking by providing a high bandwidth connection for video, connectivity and storage. Figure 1.2 shows a desktop environment with a 60 GHz link. In this distributed mode, there is no central hub. In other im-

1. INTRODUCTION

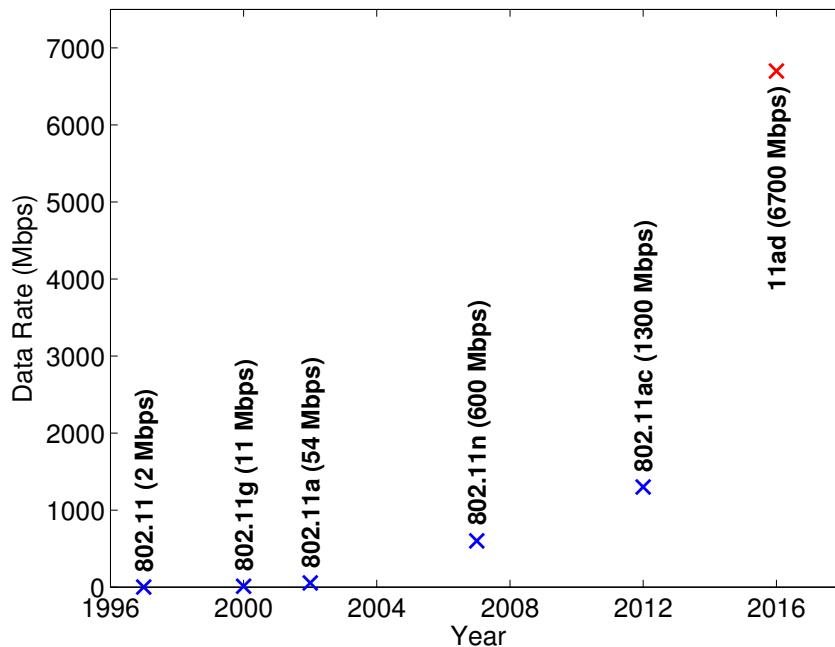


Figure 1.1: The 802.11 wireless evolution 11g to 11ad. The y-axis shows the highest PHY rate specified in the standard.

plementations a central hub can be used with connectors to attach to the local area network, universal serial bus (USB) and other devices.



Figure 1.2: 60 GHz for wireless docking [1].

Multimedia streaming

Due to the high data rate, 60 GHz can be used for uncompressed or lightly compressed high definition (HD) video streaming applications. Future mobile phones will enable full HD capture and a 60 GHz link would enable high speed dump of the video to a television or live streaming. Video streaming also enables applications where a different screen to the device screen can be used. For example in an airplane, video could be streamed to a monitor in the back of the seat.

Format	Raw	Lossless compression
24bit 1080i 30fps	1.49Gbps	0.5Gbps
24bit 1080p 60fps	2.98Gbps	1.5Gbps

Table 1.2: Data rate for video.



Figure 1.3: 60 GHz for wireless video streaming [2].

Point-to-point links

Point-to-point links are increasingly being used for wireless backhaul, and small-cell cellular applications. They can be installed alongside, or as a back-up for fibre links.

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Uses are envisaged in stadiums or other events like the Olympics where additional capacity is required over a short time period.

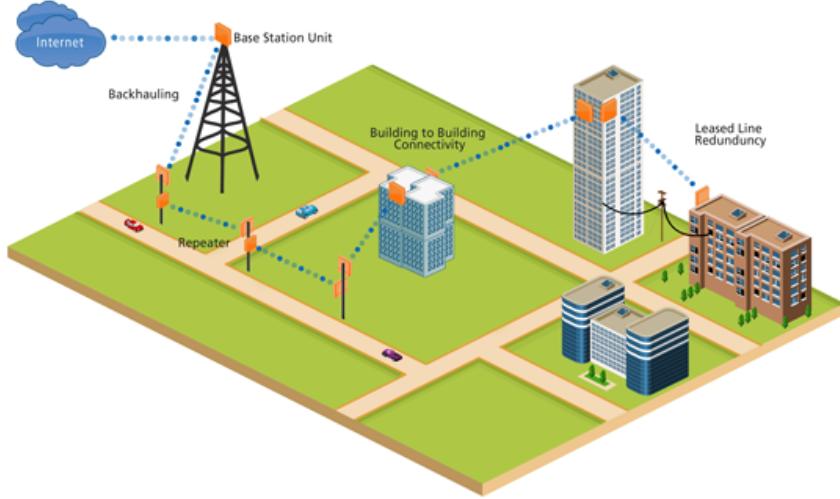


Figure 1.4: 60 GHz for wireless backhaul [3].

1.3 Communication at 60 GHz

Up to 7 GHz contiguous bandwidth is available worldwide for license free communication at 60 GHz as shown in Figure 1.5. The capacity of a channel is a product of the bandwidth and the signal to noise ratio (SNR) [23] and is shown in the following equation. Increasing the bandwidth enables high capacity at reasonable SNR levels.

$$C = BW \times \log_2(1 + SNR) b/s \quad (1.1)$$

The reason for the large allocation of bandwidth at 60 GHz is that it lies in one of the oxygen absorption bands. The attenuation due to oxygen is 15 dB/km which is not a problem for in room (or even up to few hundred meters) operation but restricts the use

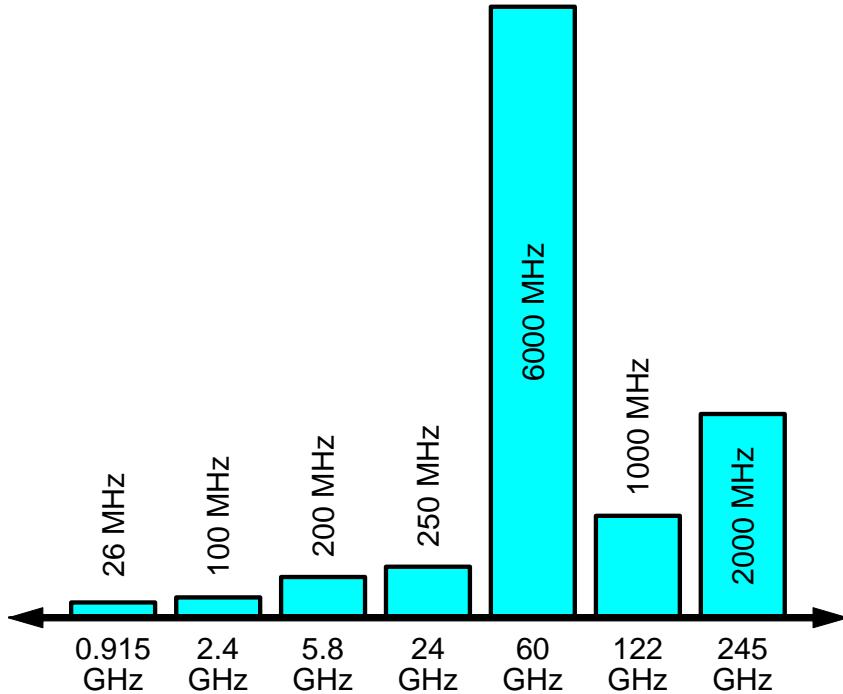


Figure 1.5: Unlicensed channel bandwidths.

beyond that. Rain also has an effect on performance of 60 GHz point-to-point links. The free space path loss, and effects of Oxygen and rain are shown in Figure 1.6 and Table 1.3.

In addition 60 GHz is highly attenuated by common building materials (see Table ??). For indoor use, this limits its application to in-room wireless.

Rate (mm/h)	60 GHz Loss (dB/km)
0.25	0.2
1.25	0.8
5	3
25	10
50	20
100	30
150	40

Table 1.3: Additional loss due to rainfall at 60 GHz [17].

1. INTRODUCTION

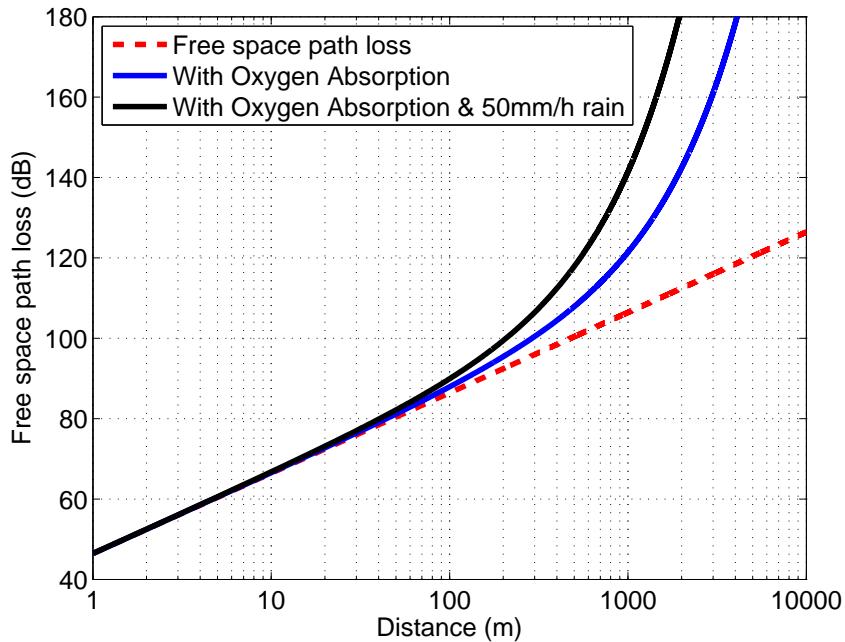


Figure 1.6: Free space path loss at 60 GHz. The loss including Oxygen absorption and rain are also shown.

Material	Thickness (mm)	Loss (dB)
Drywall	25	6.0 +/- 3.4
Whiteboard	19	9.6 +/- 1.3
Clear glass	3	3.6 +/- 2.2
Mesh glass	3	10.2 +/- 2.1
Human	100	30 +/- 10

Table 1.4: 60 GHz propagation loss through objects [18, 14].

1.4 Objective

There are several challenges that need to be overcome to enable millimetre wave Silicon transceivers, this thesis focuses on two of these:

- 1) The design of high efficiency PAs. PAs are key components inside radio transmitters and are responsible for the amplification of the RF signal and efficient transmission of RF energy to the antenna for radiation. High performance PAs lead to better battery life or enable higher performance systems for the same battery life and help to reduce the thermal heating in devices. The implementation of efficient millimetre wave PAs is challenging due to the transistor performance, low power supply, reliability concerns and modelling challenges.
- 2) The development of new architectures for 60 GHz systems which allow simple integration into consumer devices such as laptops. Conventional architectures used for wireless systems suffer from too much loss when used at 60 GHz, new designs need to be investigated which enable the efficiency integration of transmitters and receivers in devices.

1.5 The GLIMMR Project

The GLIMMR (Gigabit low-cost integrated millimetre wave radio) project was a collaborative research effort started in 2005. It consisted of researchers from the University of South Australia, Adelaide University, Macquarie University and was led by NHEW R&D Pty Ltd (Neil Weste) in a linkage grant with the Australian Research Council

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(ARC).

The objective of the project was to design low-cost silicon ICs and implement a system capable of >1 Gpbs at 60 GHz. The project was supported by Cadence Design Systems, Jazz Semiconductor, Peregrine Semiconductor, Intel Corporation, and AWR.

The work in this thesis was carried out as part of the GLIMMR project and focused on the development of the radio hardware and system architecture. Three SiGe tapeouts were undertaken, called GLIMMR test-chip 1,2 and 3 (GTC1, GTC2, GTC3).

1.5.1 GLIMMR test-chip 1 - GTC1

GTC1 contained several transistor characterisation structures as well as some small circuit designs. The goal was to characterise the process and validate the models. GTC1 was taped out in 2006.

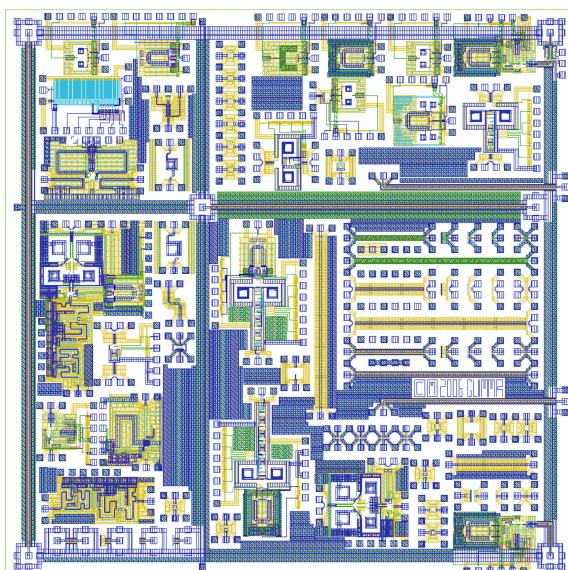


Figure 1.7: GLIMMR test-chip 1 (GTC1).

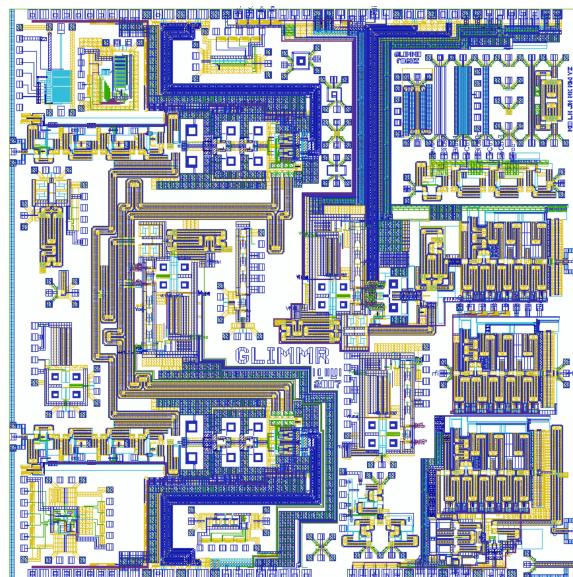


Figure 1.8: GLIMMR test-chip 2 (GTC2).

1.5.2 GLIMMR test-chip 2 - GTC2

GTC2 contained several circuits including the transmission line power amplifier in Chapter 4 and the single chip transmitter design in Chapter 5. GTC2 was taped out in 2007.

1.5.3 GLIMMR test-chip 3 - GTC3

GTC3 contained several circuits for a split-IF architecture including the transformer based power amplifier and the split-IF transmitter presented in Chapter 5. GTC3 was taped out in 2008.

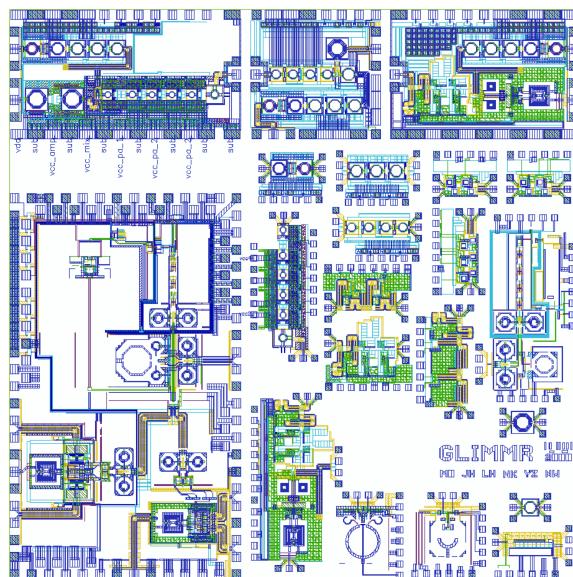


Figure 1.9: GLIMMR test-chip 3 (GTC3).

1.6 Contributions

The work in this thesis was done over 8 years from 2006-2013, originally as a full-time student at Macquarie University with the GLIMMR project and finally as an employee with Broadcom Corporation. There is a time lag between some of the results presented in this thesis and when they were originally designed.

This thesis develops theory and design techniques used to implement Silicon power amplifiers at millimetre-wave frequencies. Several topologies are implemented including transmission line based and transformer based designs. A design methodology is presented which results in the first-time-right design of 4 power amplifiers. A CMOS power amplifier is presented which is extremely small and achieved the highest efficiency at time of publication.

In addition, architectures for millimetre-wave systems are studied. Both a conventional and novel split-IF architecture are outlined. The split-IF architecture enables simple integration of 60 GHz in a laptop or for point to point links.

Awards arising from this thesis:

Winner 2008 high efficiency power amplifier design competition. Published in:

M. Boers, A. Parker, and N. Weste, "A gan HEMT amplifier with 6W output power and >85% power-added efficiency [student designs]," *Microwave Magazine, IEEE*

Publications arising from this thesis:

M. Boers, A. Parker, and N. Weste, "A gan hemt amplifier with 6W output power and >85% power-added efficiency [student designs]," *Microwave Magazine, IEEE*, vol. 9, no. 2, pp. 106110, 2008.

M. Boers, A. Parker, and N. Weste, "A 60 GHz transmitter in 0.18 um silicon germanium," in *Wireless Broadband and Ultra Wideband Communications, 2007. AusWireless 2007. The 2nd International Conference on*, pp. 3636.

M. Boers, "A 60 GHz transformer coupled amplifier in 65nm digital cmos," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE*, pp. 343346.

Additional publications with contributions from the author:

M. Boers, et. al. "A 60 GHz TX/RX 802.11ad transceiver with single coaxial cable and polarization diversity," in *ISSCC 2014*. [24].

V. Bhagavatula, M. Boers, and J. Rudell, "A transformer-feedback based wideband if amplifier and mixer for a heterodyne 60 GHz receiver in 40nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*, pp. 167170, 2012. [25]

J. A. Howarth, A. P. Lauterbach, M. J. Boers, L. M. Davis, A. Parker, J. Harrison, J. Rathmell, M. Batty, W. Cowley, C. Burnet, L. Hall, D. Abbott, and N. Weste, "60 GHz radios: Enabling next-generation wireless applications," in *TENCON 2005 IEEE Region 10*, pp. 16.

1.7 Organisation

Chapter 2 reviews Silicon technology for millimetre-wave applications. Both CMOS and SiGe are investigated and key parameters, process information and performance are outlined. Passive devices are reviewed as well as an overview of packaging technologies for millimetre-wave circuits.

Transmitters and phased arrays are introduced in Chapter 3. The fundamentals of radio transmitters are reviewed. Two transmitter architectures are analysed as well as several impairments. Phased arrays are important at 60 GHz due to the high free space path loss. Their application to 60 GHz systems is reviewed along with several key concepts.

Chapter 4 looks at the implementation of power amplifiers. Some theory is covered as well as four different designs.

Finally, two transmitter architectures are shown in Chapter 5. The first is a single chip transmitter with single output and the second is a split-IF transceiver which could be implemented with a single coaxial cable.

2

Silicon Technology

2.1 Overview

Historically high frequency RF systems have been implemented as hybrids, using type III-V compound semiconductors like Gallium Arsenide. Over the last decade research into Silicon based technologies for millimetre-wave communication [26, 27, 28, 29] and vehicular RADAR [30, 31, 32, 33, 34] has been done. SiGe and CMOS technology have both reached nodes which provide high performance at millimetre wave frequencies and enable the integration of full transceivers. While transceiver designs have been presented, several challenges remain, including high power consumption due to low PA efficiency and architectural considerations to enable 60 GHz implementation

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into consumer devices such as laptops.

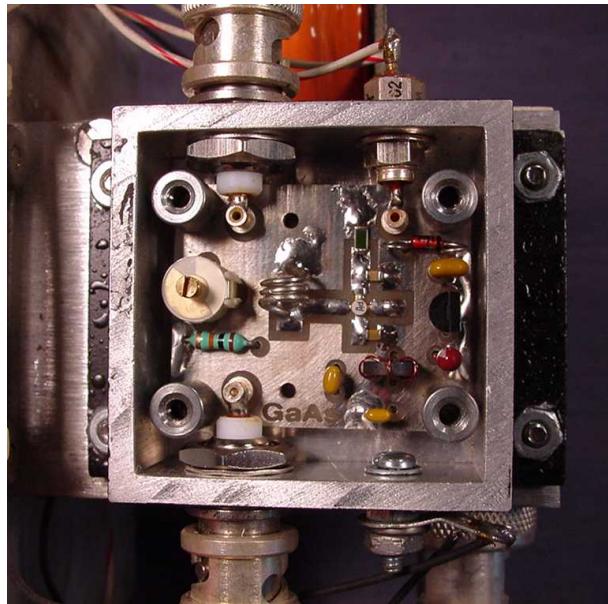


Figure 2.1: A GaAs hybrid.

This chapter looks at the use of Silicon technology for millimetre wave applications. Both CMOS and SiGe will be explored along with passive devices and packaging methods.

Why Silicon?

Silicon is the second most abundant element in the earths crust (27.7%) after oxygen (46%) and is the most common metalloid [35]. It is found in the environment combined with oxygen, predominantly silica (quartz) and other silicates (clay, feldspar, granite, asbestos) these silicon bearing compounds make up over 75% of the earths crust [36]. The abundance of silicon along with a host of favourable properties including high stability, excellent mechanical and thermal performance, its ability to form a high quality native oxide with a near ideal oxide/silicon interface, being able to grow exceptionally large, defect free single crystal wafers and the remarkable ease

at which low resistivity ohmic contacts (10-20 ohms / μm^2) can be manufactured [37] have contributed to its dominance as a semiconductor over the last 50 years.

CMOS field-effect transistor (FET) technology and SiGe heterojunction bipolar transistor (HBT) technology are two processes which use a Silicon wafer as a substrate. In order to reach mass market with a reasonable cost, transceivers must be implemented in Silicon. The remainder of this section looks at CMOS and SiGe in detail and outlines key performance trends related to millimetre-wave.

2.2 Choosing A Technology

CMOS and SiGe are both contenders for low-cost millimetre wave transceivers. This chapter reviews the cost, performance, reliability and other integration concerns for both technologies.

Of the silicon based semiconductor processes, CMOS is by far the most popular making up 95% of globally produced integrated circuits [38]. The popularity of CMOS stems from the ease at which it can be manufactured, the high level of integration it achieves and the generation-to-generation scaling trend which has to date, followed Moores law.

CMOS is a cost efficient process that was originally developed for digital systems, if an RF designer had a choice based purely on performance, CMOS FETs would most likely not be used. It is only when the economics are looked at that it becomes much more attractive, the key now is designing a system using a lower performing RF process which meets the application requirements.

2. SILICON TECHNOLOGY

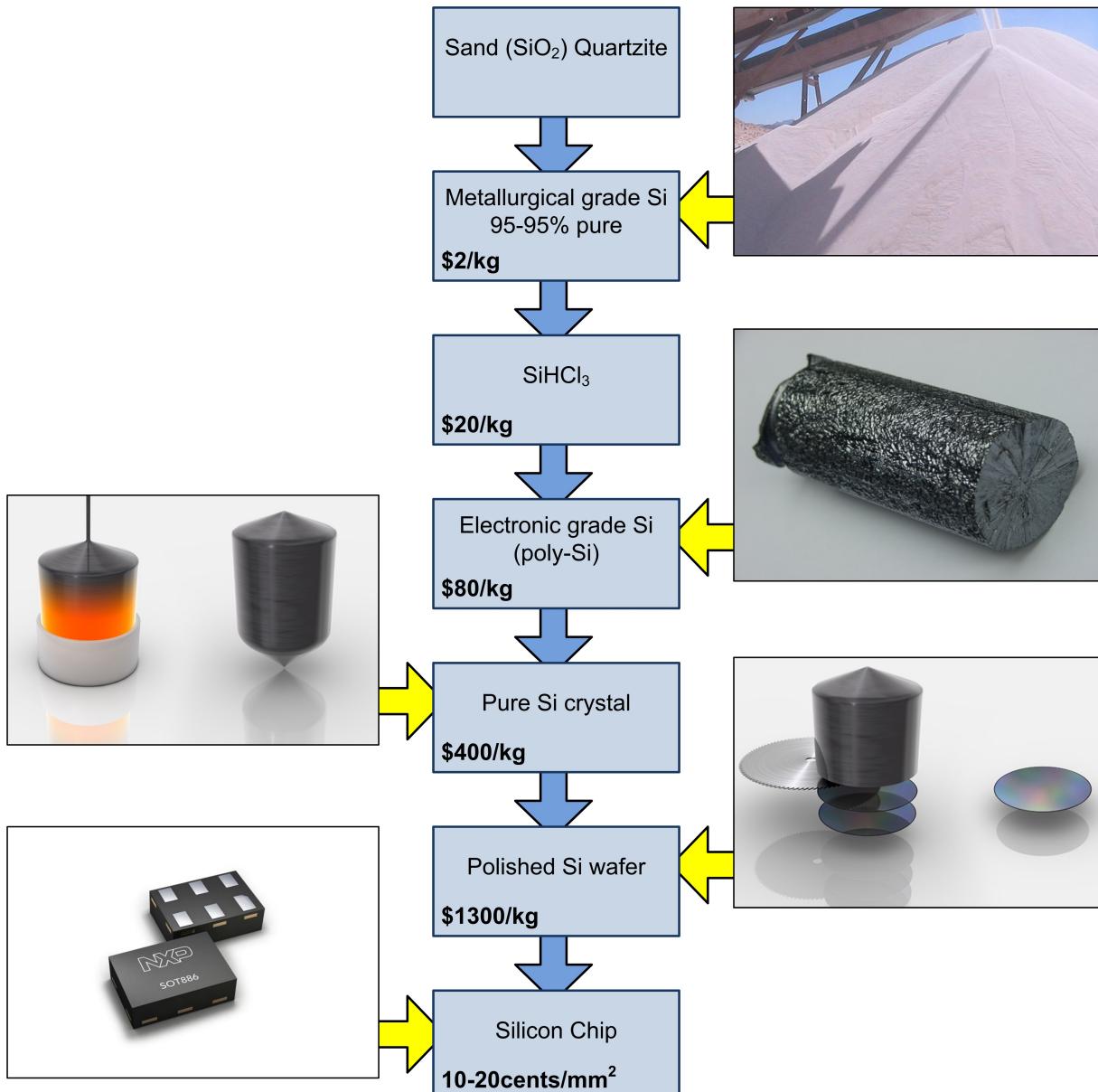


Figure 2.2: An overview of the process from sand to Silicon wafer. The low cost of the source materials and processing has enabled the mass-market adoption of Silicon technology. [4, 5, 6, 7, 8, 9]

2.2. CHOOSING A TECHNOLOGY

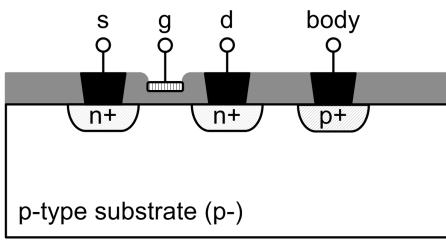
CMOS is implemented on a silicon substrate and FETs are used as the active devices. Increased performance in FETs (higher f_t , f_{max} and lower NF_{min}) occurs primarily due to the lateral scaling of the devices each generation. With better lithography smaller gate lengths can be implemented which reduces the gate transit time (electrons have less distance to travel), in addition, reduced dimensions reduce the parasitic capacitances in the intrinsic device.

FETs are majority carrier devices where drift current (the result of an applied electric field) between the drain and source is dependent on the voltage at the gate terminal. Interestingly, as a result of constant-field scaling NMOS devices have a peak f_t at 0.3mA/um, f_{max} at 0.2mA/um and NF_{min} at 0.15mA/um irrespective of the node [39].

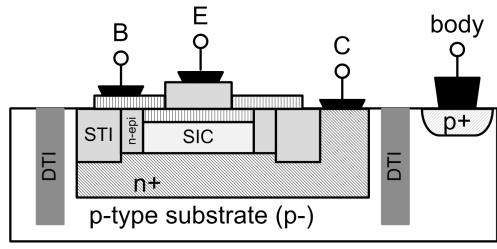
SiGe is a type-IV compound semiconductor. SiGe HBT technology is effectively a hetero-junction bipolar process implemented using a strained silicon-germanium epitaxy layer for the base of the transistor. The HBT NPN structure consists of a Si-N to SiGe-P junction emitter-base and a SiGe-P to Si-N base-collector junction [37]. The introduction of Germanium into the base of the HBT improves the performance of the device as it has a smaller band-gap than Silicon, improves the carrier transport parameters and can be graded to accelerate the carriers through the base [37].

SiGe offers several advantages over CMOS, it has lower 1/f noise, higher output resistance and higher voltage handling capacity than the equivalent (in speed) CMOS process [16] but it does not provide as high digital integration.

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CMOS NMOS device



SiGe NPN HBT device

Figure 2.3: Cross section of NMOS (left) and NPN HBT (right) [10].

2.2.1 Material Properties

There are several material properties which define performance limits for mm-wave devices [40, 10].

- Electron mobility (SiGe >Si)
- Hole mobility (SiGe >Si)
- Saturation velocity ($\text{Si} \approx \text{SiGe}$)
- Thermal conductivity ($\text{Si} > \text{SiGe}$)¹

2.2.2 Cost

The cost of manufacturing an integrated circuit can be broken down into the fixed costs (e.g. mask cost), and the per unit cost of the materials and manufacturing process to make the wafer.

¹this is not really a concern given the tiny amount of Germanium used in SiGe devices

At large volumes the cost of manufacturing Silicon is extremely cheap and can be anywhere from 50c to 5c per mm^2 . The mask cost depends on the technology (minimum feature size) as well as the number of masks that are required.

Table 2.1 shows a rough price for SiGe and CMOS.

Technology	Cost of Mask Set (\$)	Cost ($/mm^2$)
SiGe 180nm	100,000	30
SiGe 130nm	200,000	30
CMOS 65nm	400,000	15
CMOS 40nm	600,000	15

Table 2.1: Example pricing for SiGe and CMOS technologies.

2.2.3 Performance

If we compare CMOS and SiGe technologies that have a similar f_t , we can observe that they match in speed at approximately 2 generations apart, 0.18um SiGe is equivalent to 90nm GP CMOS and 0.13um SiGe is equivalent to 65nm GP CMOS.

The device f_t and f_{max} are both useful measures of a device performance. [10, 41]. f_t is the frequency at which the current gain ($H21$) of the device is equal to one. f_{max} is the frequency at which the maximum available gain (assumes ideal input and output match) (G_{max}) is equal to one.

For millimetre wave designs, f_{max} is usually a better measure as it takes into account additional parasitic elements which impact the performance of the device.

CMOS

A FET with parasitics is shown in Figure 2.4. The intrinsic device sets the maximum speed and performance characteristics and the parasitics of the device reduce this. Some of the parasitics have more of an impact on performance than others. The equations below show that for high f_{max} the gate resistance R_g and gate-to-source C_{gs} capacitance need to be reduced as well as R_d and R_s .

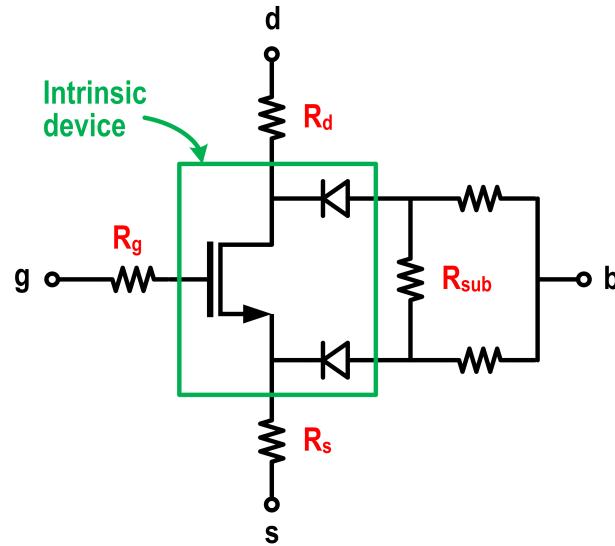


Figure 2.4: CMOS extrinsic device [11].

$$f_T = \frac{gm}{2\pi[C_{gs} + C_{gd}(1 + gmR_s)]} \quad (2.1)$$

$$f_{max} = \frac{f_T}{2\sqrt{g_{ds}(R_g + R_s) + 2\pi f_T R_g C_{gd}}} \quad (2.2)$$

SiGe

The f_{max} of a SiGe device is also affected by parasitics however they usually have less of an impact due to the much higher current density per area of transistor for HBTs resulting in less fingers and smaller metal to metal parasitics in the layout of a device. The backend in SiGe processes also has higher lateral and vertical spacing resulting in less parasitics. Care still needs to be taken to reduce the base resistance R_b as well as the base to collector capacitance C_{bc} .

$$f_T = \frac{1}{2\pi \left[\frac{nKT}{qI_c} (C_{be} + C_{bc}) + (R_E + R_C) C_{be} + \tau_b + \tau_c \right]} \quad (2.3)$$

$$f_{max} \approx \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} \quad (2.4)$$

Summary

Both SiGe and CMOS achieve high f_t and f_{max} . SiGe is less affected by layout parasitics than CMOS due to the higher current density per transistor and the larger spacing between metals. The table below shows the speed for some advanced SiGe and CMOS nodes.

Technology	F_t (GHz)	F_{max} (GHz)	NF_{min}
Jazz SiGe 0.25um	75		
Jazz SiGe 0.18um	150		
Jazz SiGe 0.13um	200		
ST SiGe 0.13um	220	290	
ST CMOS 65nm LP	175	325	

Table 2.2: Overview of Silicon processes [15, 16].

2.2.4 Noise

Noise in active devices can be separated into broadband noise such as thermal noise and shot noise and low frequency noise such as $1/f$ (or flicker) noise.

The thermal noise generated in a resistor is given by [42]:

$$\overline{e_n^2} = 4kT R \Delta f \quad (2.5)$$

Gate resistance in FETs and base resistance in HBTs both generate thermal noise.

Shot noise occurs when a current flows across a potential barrier such as the band-gap present at the PN-junction interface. It is the randomness of carrier transitions across the interface which generates this noise. Like thermal noise, shot noise is white in nature [42].

The shot noise can be described by [42]:

$$\overline{i_n^2} = 2qI_{DC}\Delta f \quad (2.6)$$

In HBT's both base and collector junctions contribute to shot noise. As the base current is multiplied by the transistor gain, it dominates. In FETs, only the leakage across the gate junction generates shot noise but this is at a very low level due to the small current.

Flicker noise has a $1/f$ power density spectrum and the exact physical origins are not completely understood [10]. $1/f$ noise is higher in CMOS devices and while being low frequency in nature is up-converted around the fundamental frequency in VCOs.

NF_{min} is a useful figure of merit (FOM) which can be used to compare the noise of two technologies.

CMOS

The NF_{min} for a CMOS device is given by the following [11]:

$$NF_{min} = 1 + 2 \frac{f}{f_t} \sqrt{\frac{\overline{i_{dn}^2}}{4kT} \left(R_g + R_s + \frac{\overline{i_{dn}^2}}{4kT g_m^2} \right)} \quad (2.7)$$

SiGe

$$NF_{min} = 1 + \frac{n_F}{\beta} + \frac{f}{f_t} \sqrt{\frac{2I_C}{V_T} (r_E + R_b) \left(1 + \frac{f_t^2}{\beta f^2} + \frac{n_F^2 f_t^2}{\beta f^2} \right)} \quad (2.8)$$

2.2.5 Reliability

The mechanisms for device degradation and breakdown are different in CMOS and SiGe due to the different structure of the active devices.

CMOS - Time Dependent Dielectric Breakdown

Time dependent dielectric breakdown (TDDB) is the breakdown of the insulating gate oxide in the CMOS device leading to a conduction path between the gate and the device substrate. Without this insulating layer the device no longer operates as a FET where current flow is dependent on the electric field [43].

Even though the gate dielectric is a good insulator, a small current still flows. The mechanism for this current flow is often attributed to Fowler-Nordheim tunnelling [44]. TDDB can be characterised by the total charge required to breakdown Q_{BD} which can be defined as [44]:

$$Q_{BD} = \int_0^{T_{BD}} I(t) dt \quad (2.9)$$

Foundries provide safe operating levels which will reduce the impact of TDDB, by following these rules the impact of TDDB can be mitigated.

CMOS - Hot Carrier Injection

Hot carrier injection (HCI) is the injection of a carrier (electron or hole) from the channel to the gate dielectric. HCI occurs in short channel devices under high electric fields (i.e. high V_{DS}). HCI affects the performance of the device, in particular it increases the threshold voltage which over time will reach a level that will not allow current to flow in the channel rendering the device un-fit for operation. HCI is not a sudden breakdown process, rather a degradation in the performance of the transistor over time.

HCI is the biggest concern for minimum feature size CMOS devices in mm-wave circuits.

CMOS - Negative-bias Temperature Instability

Negative-bias temperature instability (NBTI) is mainly a concern for PMOS devices, it results in a increase in the threshold voltage of the device over time.

SiGe - Avalanche Breakdown

Avalanche breakdown is the primary concern for reliability in SiGe devices. This breakdown occurs at high BC voltages where the electric field in the junction exceeds the breakdown field of the device [10]. This type of breakdown is characterized by a sudden increase in collector current.

Operating below the BV_{ceo} of the device will ensure Avalanche Breakdown does not occur.

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Summary

SiGe devices can handle much larger voltage swings than CMOS devices and do not degrade slowly over time as is the case with HCI effects in CMOS transistors. For high power applications that operate constantly across a long period of time, higher efficiency can be achieved in a SiGe process.

2.2.6 Conclusion

There is no clear winner. For high volume applications CMOS will always be the economic choice. For low to medium volumes, SiGe is a contender, especially for demanding performance specs which would benefit from a larger signal swing such as VCO phase noise or transceiver linearity. All processes should be evaluated for each application.

2.3 Passive Devices

Passive devices are extremely important in RF circuit design. They can be used to couple adjoining stages, provide a load and path for DC current to flow, they are used in impedance matching circuits in order to maximise the power transfer between circuits.

2.3.1 Capacitors

Capacitors are used to AC couple a signal, effectively blocking DC at the expense of a reduction in bandwidth. They can be used as resonant elements, tuning a circuit's impedance or resonating with an inductor in the tank of a VCO. They can also be used to decouple a local power supply from the rest of a system or provide a local reservoir of energy in an inductive power supply. There are several capacitor types depending on process availability; metal-insulator-metal (MIM), metal-to-metal (MTM) and MOS capacitors. MIM capacitors require one or more additional process step(s) in the fabrication process adding extra cost. MTM capacitors are implemented using only the metal that is available in the process.

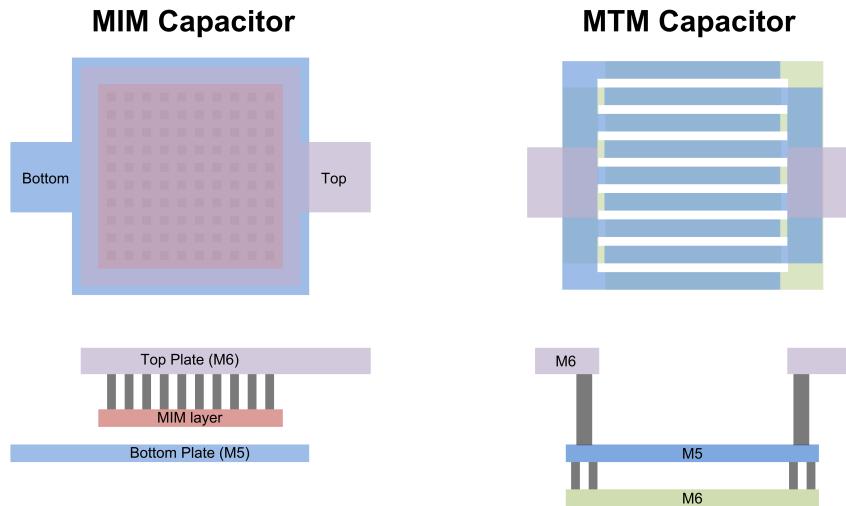


Figure 2.5: MIM and MTM capacitors in a Silicon technology.

MIM capacitors

MIM capacitors are implemented as parallel plate capacitors and typically use one of the standard metal layers in the process as one of the parallel plates [45, 46]. An

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insulator is deposited between this plate and an additional plate that is spaced above or below but much closer than the next standard metal layer.

MIM capacitors provide a high Q. The insulator is designed to have a low loss tangent and high dielectric constant in order to increase the capacitance per square. Capacitance values on the order of 1-2 fF/ μm^2 are easily achieved. Capacitance to the substrate is usually an order of magnitude less than that of equivalent MTM capacitors. Due to their layout, mainly square or rectangular, MIM capacitors exhibit low lead inductance and perform well into millimetre-wave frequencies.

Using MIM capacitors requires an additional mask and processing steps which increases the cost of the process. Most CMOS processes do not use MIM capacitors for this reason and high capacitances are available at advanced nodes due to the low metal to metal spacing.

MTM capacitors (inter-digital / finger / comb)

MTM capacitors are created with the standard metal available in the Silicon process. They are typically used in sub 100nm CMOS processes where minimum geometry sizes allow the implementation of MIM comparable capacitors without the need for any additional process steps [47]. As MTM capacitors rely on the capacitance between metal, (sidewall, plate-to-plate or both), the capacitance is limited by the minimum space allowed by DRC rules as well as the dielectric constant. In 65nm, 40nm and below, low-k dielectric constant materials (2.9) are used in the lower metal stack in order to reduce coupling between traces. While this has the desired effect of reducing capacitance between routing, it also reduces the achievable capacitance.

MOS capacitors

In both CMOS and SiGe processes, MOS capacitors are available. MOS capacitors use the capacitance between the gate and semi-conducting substrate. By biasing the device in different regions, the capacitance can be varied. MOS caps are useful as varactors in VCOs, or as decoupling capacitors combined with metal caps to increase the capacitance density per unit.

2.3.2 Inductors

Inductors can be created from the metal layers in Silicon processes. They have been studied from 30-100GHz in [48]. They can be used as part of matching networks, to tune out parasitic capacitances in RF switches and to supply bias currents. Inductors can be implemented at short sections of transmission line, as a line inductor or as single / multiple turn structure. Modelling is important in order to capture the self-resonant frequency.

In single-ended designs, correct modelling of the ground return path is extremely important as it can impact the tuning and stability of the devices.

For the transformers and inductors used in the designs in this thesis, a ground solid ground loop is simulated as part of the passive device structure. This has two benefits. Firstly, the ground return path is clearly modelled by being included in the EM simulation, secondly, circuitry outside of this area does not have a large impact on the performance of the passive device ².

²but we still need to be careful about coupling to nearby magnetic devices

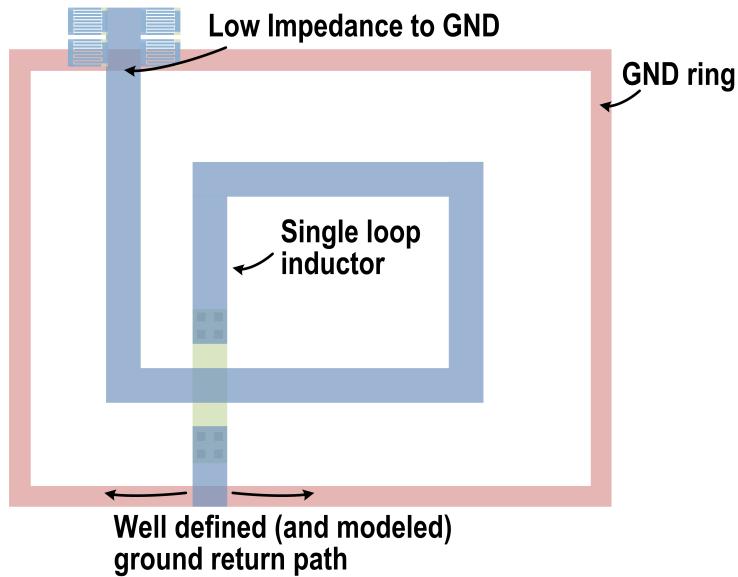


Figure 2.6: Inductor overview.

2.3.3 Transformers

Transformers are useful passive components for RF design. They have more degrees of freedom than inductor or capacitors and provide an extremely compact way to provide inter-stage coupling and matching between two stages of a differential circuit. They can also be used to couple stages in a mixer providing DC separation between the switching and gm stages. Transformers are used extensively in the power amplifier designs in Chapter 4.

Due to the magnetic coupling between coils, a transformer forms a higher order network than two separate inductors, this can be seen by the T model equivalent for the transformer shown in Figure 2.7.

G_{max} is a useful figure of merit for a transformer - it shows the minimum loss possible due to losses in the transformer itself (resistive loss in the metal, loss due to coupling

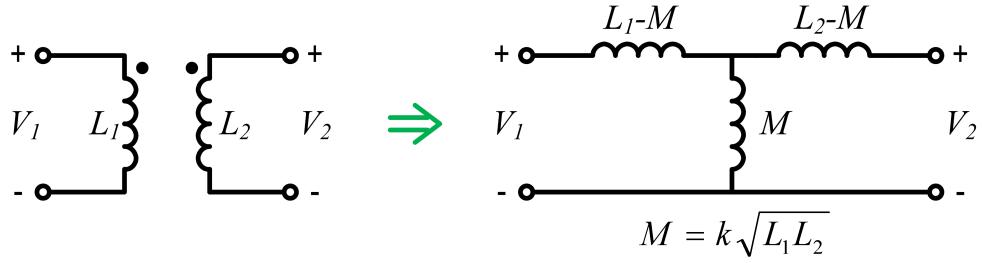


Figure 2.7: T model for a transformer [12].

into the substrate). The G_{max} can be described as a function of the coil Q and coupling factor k [12].

$$G_{max}(Q, k) = 1 + \frac{2}{Q^2 k^2} - 2 \sqrt{\frac{1}{Q^4 k^4} + \frac{1}{Q^2 k^2}} \quad (2.10)$$

2.3.4 Transmission lines

Transmission lines are required at frequencies where the routing distance is in the order of a fraction of a wavelength ($\lambda/15$), this applies for 60 GHz on chip where the wavelength in free space is 5mm and routing on chip can be multiple millimetres.

Transmission lines for the GLIMMR project were simulated in HFSS by Leonard Hall and implemented in Cadence by James Howarth. A library of single ended and differential lines was created with several characteristic impedances from 30ohms to 90ohms.

While transmission lines can be used for matching in millimetre wave circuits, they are much larger than inductors and transformers and result in an area penalty compared to other approaches (as shown in Chapter 4).

2.3.5 BEOL comparison

There are several BEOL characteristics which can impact the performance of passive devices. These are shown in

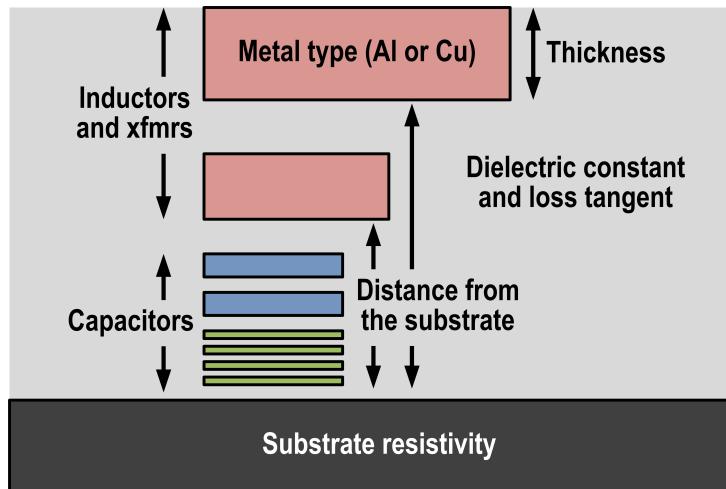


Figure 2.8: The left shows the metals used for different passive devices. The right highlights some of the main BEOL parameters which impact performance.

BEOL figure of merit

Several FOMs can be used to compare the BEOL for a process. Transmission line loss in dB/mm depends on the metal, spacing, loss tangent and dielectric constant of the process. It is also implementation dependent - in some processes microstrip lines may perform better than CPW lines for example.

Transformer G_{max} is measure of the loss through a transformer. This is mainly dependent on the geometry, metal type and loss of the substrate.

Processes with thick copper metals and higher spacing between the top layer metals and the Silicon substrate give better performance.

2.4 Packaging At 60 GHz

Packaging is an important step for millimetre-wave circuits, the key consideration is reducing the loss from the PA output (or LNA input) to the antennas, as well as providing a stable substrate for the device, low warp, temperature, moisture...

Wirebond and bumped die are two different methods which can be used.

2.4.1 Wirebond Package

In a wirebond package, pads are placed around the edge of the chip and the connection to package, board or module is done using fine pieces of wire, typically Gold or Aluminium. A wirebond transition is shown in Figure

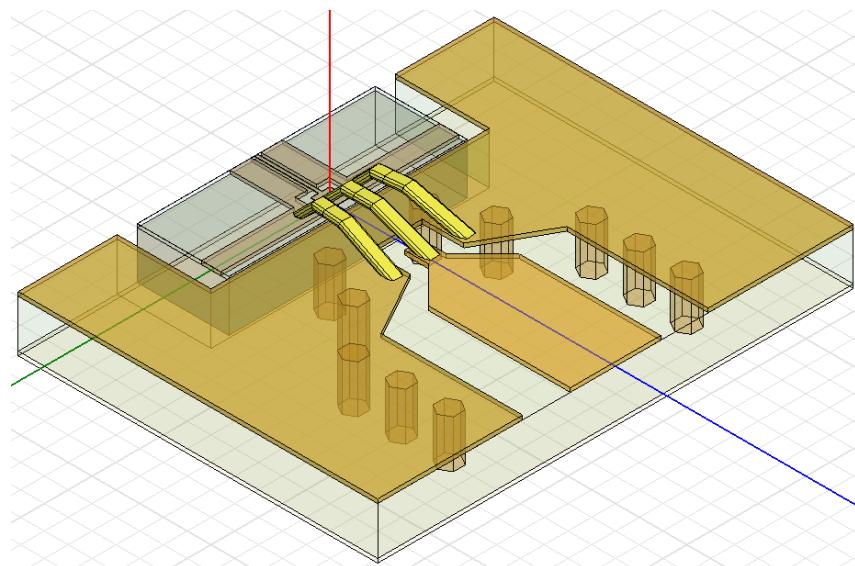


Figure 2.9: High frequency bond-wire transition.

2.4.2 Bumped Die

In a bumped die, solder balls (as small as 75um in diameter) are used to connect a die to package, module or board. This is shown in the following Figure 2.10.

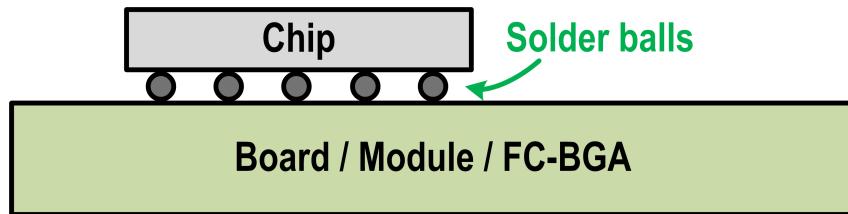


Figure 2.10: Solder balls from chip to board, module or FC-BGA package.

3

Transmitters and Phased Arrays

“... in the microwave area, structures included in the definition of integrated electronics will become increasingly important. The successful realization of such items as phased-array antennas, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar.”

– Gordon Moore, 1965

3.1 Introduction

Radio frequency (RF) systems are responsible for the conversion between a baseband signal and a signal modulated around a carrier. There are many different types of RF systems, this thesis is focused on efficient transmitters for 802.11ad applications.

Phased array systems use multiple antennas to achieve higher performance over a single antenna system. At millimetre-wave frequencies phased arrays provide an efficient way to help close the link budget, unlike lower frequencies they are easily implementable due to the small wavelength and provide several benefits.

This chapter starts with a comparison of 5GHz and 60 GHz communication links and reviews the fundamentals of transmitters and phased arrays for millimetre-wave applications.

3.2 A comparison of 60 GHz and 5GHz systems

Wireless LAN links at 2.4 and 5GHz are probably one of the most pervasive communication technologies available today, they are used in the home, office and to connect the internet of things. There are several key differences between operation at 60 GHz and 5GHz and these are outlined below:

1. The channel capacity of a 60 GHz system is higher due to a wider available bandwidth. At 5GHz, up to 160MHz channels are used versus 2 GHz at 60 GHz [13, 49]. In terms of capacity, this results in an $2000/160 = 12.5$ improvement in

3.2. A COMPARISON OF 60 GHZ AND 5GHZ SYSTEMS

speed (bits/Hz) for the same SNR. Alternatively, the same speed can be achieved with reduced SNR at 60 GHz.

2. At 60 GHz, the free space path loss for an AWGN channel is higher by $20 \times \log_{10}(\frac{60}{5}) = 21.5 \text{ dB}$ resulting in a $12\times$ reduction in range.¹
3. Due to a smaller wavelength (5mm at 60 GHz vs. 60mm at 5GHz), more antennas can fit in a given area.

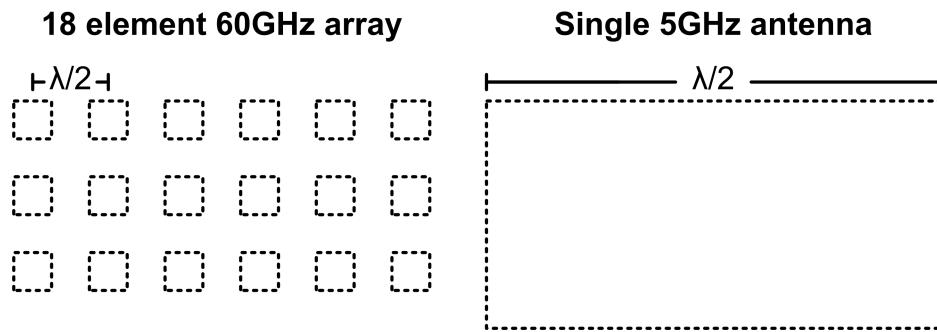


Figure 3.1: Simple comparison of size between 60 GHz and 5GHz antennas

To achieve the increased capacity offered by the wide bandwidth of a 60 GHz implementation some of the losses associated with reduced wavelength need to be overcome, this is possible by using multiple elements in a phased array. Figure 3.1 shows 18 elements at 60 GHz in the same area as a simple 5GHz antenna.

In addition to increasing the 60 GHz link budget, high gain antennas provide:

- The ability to steer away from sources of interference
- More efficient use of the spatial channel (multiple links can operate on the same channel at the same time).

¹The loss is even higher due to oxygen absorption of 60 GHz of 15dB/km but this of little consequence for short-range links. [50]

3. TRANSMITTERS AND PHASED ARRAYS

The remainder of this chapter gives an overview of transmitters and phased arrays and quantifies some of the concepts introduced here. It is not exhaustive, for more details the reader is referred to [51, 52].

3.3 Transmitter Fundamentals

3.3.1 Architectures

Radio transmitters are responsible for the up-conversion of a baseband signal to RF. For amplitude and phase modulated systems two architectures are commonly used: direct conversion and super heterodyne.

Direct Conversion Transmitter

A direct conversion transmitter is shown in Figure 3.2. In direct conversion transmitters the baseband signal is directly up-converted around the LO frequency using a single mixing stage. The direct conversion architecture is relatively simple and takes up less area than an equivalent super-heterodyne implementation. One challenge is the generation of the quadrature LO directly at the RF carrier, this is especially difficult for 802.11ad systems due to the high channel frequencies (58-63GHz).

LO pulling is a common concern in high power, low frequency direct conversion transmitters. LO pulling occurs when the power amplifier couples into a fundamental frequency VCO or the LO generation circuit (through the circuit itself or the power supply) and modulates the transmitted signal with the transmitted waveform. This results

in a degradation of output EVM due to corruption of the LO signal. The concern of LO pulling at 60 GHz is reduced since the output power is low and losses in the coupling paths are high at 60 GHz.

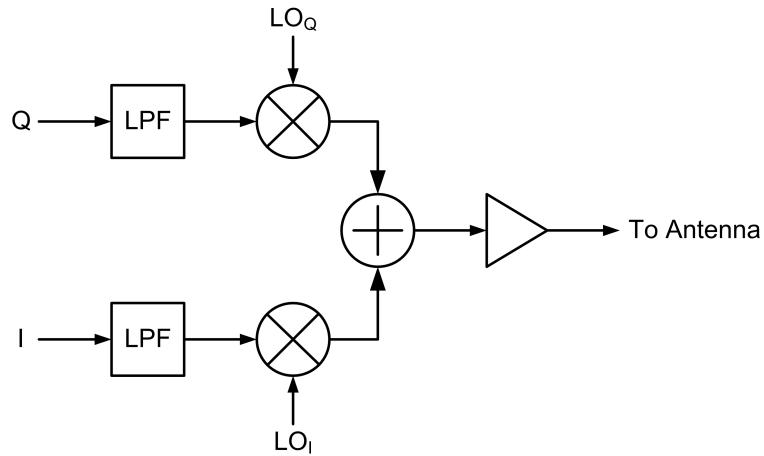


Figure 3.2: Direct-conversion transmitter.



Figure 3.3: Up-conversion in a direct conversion transmitter. The complex (I/Q) signal at baseband (BB) is up-converted directly to RF using an LO at the centre of the RF channel.

Super Heterodyne Transmitter

Figure 3.4 shows a simple super heterodyne transmitter. In this architecture the baseband signal is first up-converted to an IF frequency then a second stage of mixing up-converts the IF to RF. The first mixer uses quadrature conversion to reject the image. An image is present after the second up conversion stage however this is usually

3. TRANSMITTERS AND PHASED ARRAYS

far enough away from the RF that a simple filter (or the inherent filtering in the TX) attenuates it to a desired level.

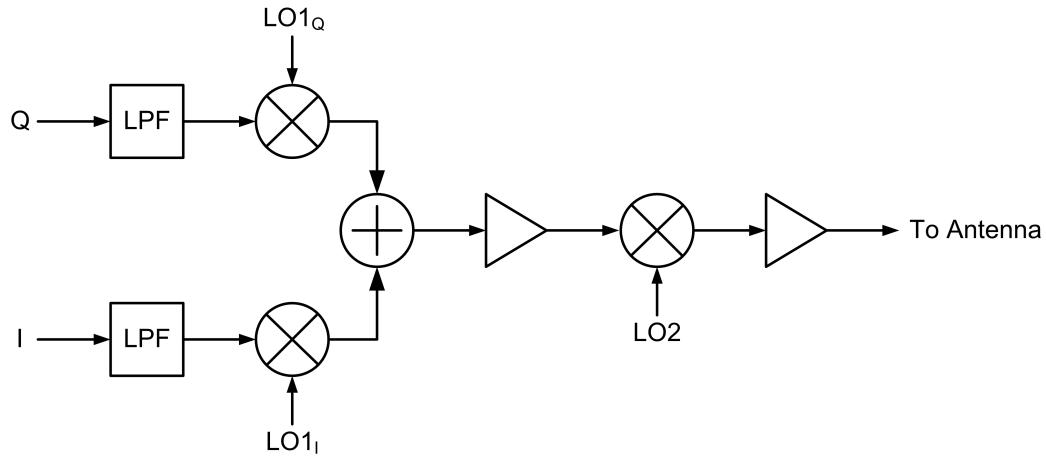


Figure 3.4: Super-heterodyne transmitter.

Super heterodyne transmitters reduce the frequency required for quadrature LO and enables gain to be spread between more stages (this is more beneficial for the RX than TX). In a spilt chip architecture, super heterodyne enables the front-end to be implemented on a separate chip that the IF radio.

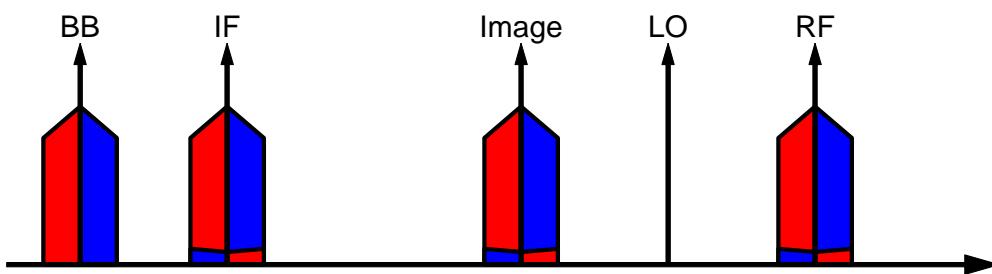


Figure 3.5: Up-conversion in a super-heterodyne transmitter. The complex (I/Q) signal at baseband (BB) is first up-converted to an intermediate frequency (IF) and then converted to RF using an offset LO.

There are different types of super-heterodyne systems based on the way the LO is generated.

Sliding IF

In a sliding IF architecture, LO1 (quadrature LO) and LO2 (IF to RF mixer LO) are related to each other and can be generated from the same PLL. An example of a sliding-IF is the architecture used in GTC2 (see the next chapter). In this architecture a 12 GHz LO1 and 48GHz LO2 is used. When the RF channel changes, both of the LO's move together.

Fixed IF (Fixed LO1)

In a fixed IF architecture, LO1 is fixed and LO2 changes to move between channels. This places the lowest requirement on bandwidth for the IF path, it enables a fixed IF band-pass filter to be used for DAC image rejection in a Nyquist DAC system rather than baseband filters. It comes at the expense of VCO tuning requirement for the LO2 PLL.

Sliding IF (Fixed LO2)

In a sliding IF (fixed LO2) system, the IF to RF conversion LO (LO2) is fixed and LO1 (and the IF frequency) move to switch between channels. This architecture reduces the burden on the PLL used to generate the higher LO resulting in better phase noise performance although it is rarely used as there is a large bandwidth requirement on the IF signal path. It needs to shift by the full RF channel spacing. At 60 GHz, this corresponds to a 6GHz shift or 8GHz bandwidth requirement.

3.3.2 Error Vector Magnitude

The error vector magnitude (EVM) is a good measure of performance for a digitally modulated system [42]. In an ideal system transmitted and received constellation points would be the same. In a real system, noise, linearity and other imperfections move these constellation points. EVM is a measure of how far the constellation points are shifted from the ideal location.

$$EVM(dB) = 10 \times \log_{10} \left(\frac{P_{error}}{P_{reference}} \right) \quad (3.1)$$

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{reference}}} \times 100\% \quad (3.2)$$

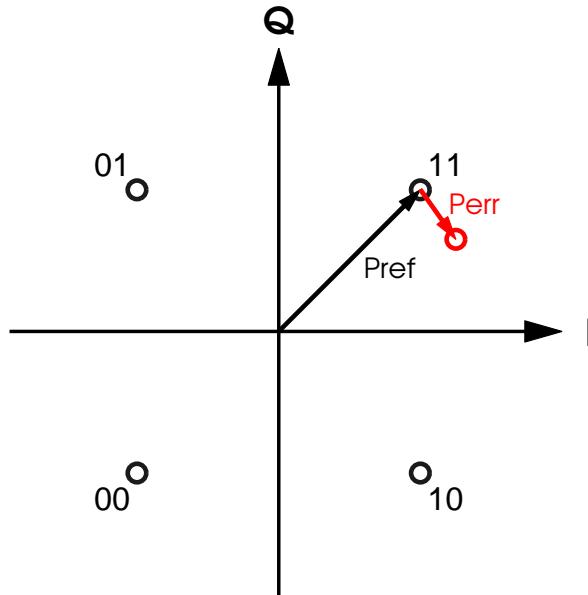


Figure 3.6: QPSK constellation with error vector shown in red.

Transmit EVM is the EVM measured at the output of the transmitter after up-conversion

3.3. TRANSMITTER FUNDAMENTALS

and amplification. Standards such as 802.11 [13, 49] specify the EVM requirement for the transmitter. EVM requirements for each single carrier MCS in 802.11ad are shown in Table 3.1. While there are several contributors to EVM in a transmitter, to get the highest efficiency, the PA should dominate.

MCS Index	Modulation	Coding rate	EVM value (dB)
1	$\theta/2$ -BPSK	1/2 with repetition	-6
2	$\theta/2$ -BPSK	1/2	-7
3	$\theta/2$ -BPSK	5/8	-9
4	$\theta/2$ -BPSK	3/4	-10
5	$\theta/2$ -BPSK	13/16	-12
6	$\theta/2$ -QPSK	1/2	-11
7	$\theta/2$ -QPSK	5/8	-12
8	$\theta/2$ -QPSK	3/4	-13
9	$\theta/2$ -QPSK	13/16	-15
10	$\theta/2$ -16QAM	1/2	-19
11	$\theta/2$ -16QAM	5/8	-20
12	$\theta/2$ -16QAM	3/4	-21

Table 3.1: Single carrier EVM requirements for 802.11ad [13].

The worst-case (often pessimistic) transmit chain EVM can be approximated as the RMS sum of individual contributors, where it is assumed that each contributor is uncorrelated and adds as squares.

$$EVM_{tx} = \sqrt{EVM_a^2 + EVM_b^2 + \dots} \quad (3.3)$$

$$EVM\% = 10^{EVM_{dB}/10} \quad (3.4)$$

In 802.11ad EVM is calculated for SC transmitters using the following:

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$$EVM = 10 \log_{10} \left(\sqrt{\left(\frac{1}{N_S P_{avg}} \sum_{i=1}^{N_S} [(I_i - I_i^*)^2 + (Q_i - Q_i^*)^2] \right)} \right) \quad (3.5)$$

3.3.3 Impairments

I/Q Phase and Amplitude Imbalance

I/Q phase and amplitude imbalance in the baseband and LO paths affect the suppression of the side-carrier (image). In a quadrature up-convertor the image is mirrored around the LO and falls on top of the wanted signal. There are two types of imbalance, fixed and frequency selective. Frequency selective phase imbalance is difficult to correct in a wideband system (requires frequency domain equalisation) so it should be minimised. Fixed phase and amplitude mismatch are easily correctable in the digital baseband of the transmitter.

Phase and amplitude imbalances in the I/Q paths can be modelled using the following [53].

$$y_{phase} = \exp \left[j \times \left(-0.5 \times \pi \times \frac{I_P}{180} \right) \right] x_r + \exp \left[j \times \left(\frac{\pi}{2} + 0.5 \times \pi \times \frac{I_P}{180} \right) \right] x_i \quad (3.6)$$

$$y_{amplitude} = 10^{(0.5 \times \frac{I_A}{20})} \times x_r + j \left[10^{(0.5 \times \frac{I_A}{20})} \right] \times x_i \quad (3.7)$$

where:

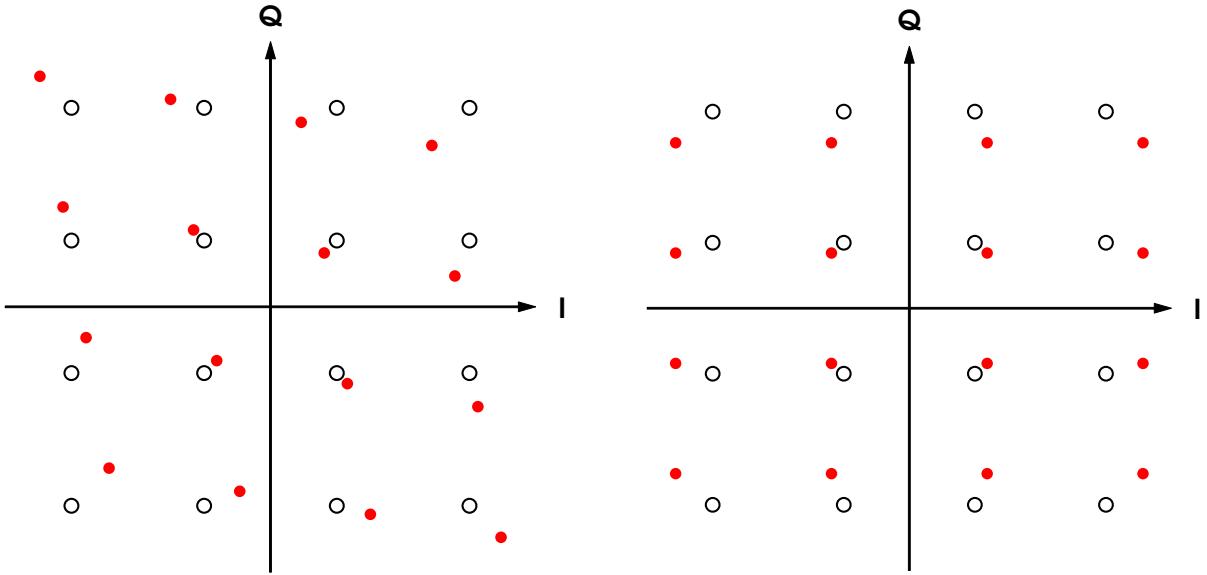


Figure 3.7: 16-QAM constellation with 20 degrees phase imbalance in I/Q paths.

Figure 3.8: 16-QAM constellation with 3dB amplitude imbalance in I/Q paths.

$$I_P, I_A = \text{Phase imbalance (degrees), amplitude imbalance (dB)} \quad (3.8)$$

$$x_r, x_i = \text{real part of } x, \text{imaginary part of } x \quad (3.9)$$

Phase imbalance is usually generated in the LO path from mismatch or variation in a polyphase filter, hybrid or quadrature divider. Amplitude variations in a hard switching LO do not have as large an impact as variations in gain in the analog baseband or DAC output amplitude mismatch. Sideband suppression (SBS) is a function of these phase and amplitude imbalances and is given by the following formula. Figure 3.9 shows the amplitude versus phase imbalance curves for different sideband suppression targets.

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$$SBS(dBc) = 10 \times \log_{10} \left(\frac{G^2 - 2G\cos\phi + 1}{G^2 + 2G\cos\phi + 1} \right) \quad (3.10)$$

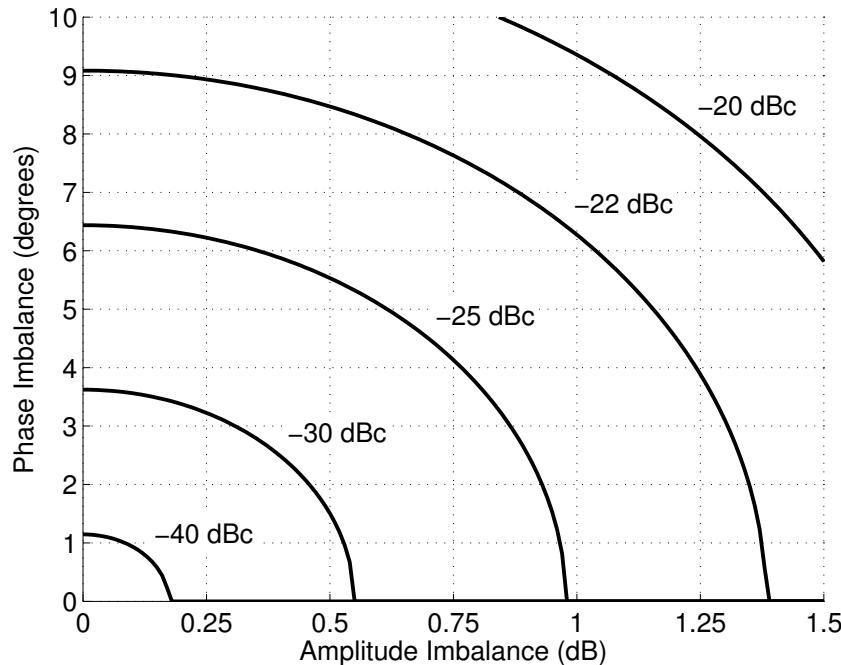


Figure 3.9: Amplitude (dB) and phase (degree) imbalance curves for different sideband suppression (dBc) levels.

The EVM contribution from IQ mismatch is equal to the sideband suppression [54].

$$EVM_{IQmm}(dB) = SBS(dBc) \quad (3.11)$$

$$EVM_{IQmm}(\%) = 10^{\frac{SBS(dBc)}{10}} \quad (3.12)$$

DC Offset

DC offset between the I and Q paths shifts the constellation directly in the I or Q direction by the amount of the offset. DC offset is one of the primary contributors to local oscillator feedthrough (LOFT).

The 802.11ad standard requires less than -23dBc LOFT. The amplitude of the baseband signal directly impacts the DC offset requirements. Since LOFT is the ratio of average signal swing to DC offset, higher swing increases the tolerance to DC offset at the expense of transmitter power for increased linearity [55].

The following formula shows the maximum DC offset V_{max_DC} for a desired LOFT $LOFT(dBc)$ and baseband amplitude V_{rms} .

$$V_{max_DC} = \frac{V_{rms}}{20\log_{10}\left(\frac{LOFT(dBc)}{10}\right)} \quad (3.13)$$

To achieve better than -30dBc LOFT with a baseband signal swing of 600mV, the allowable baseband offset is

$$\frac{0.6/2\sqrt{2}}{20\log_{10}\left(\frac{30}{10}\right)} = 22.2mV \quad (3.14)$$

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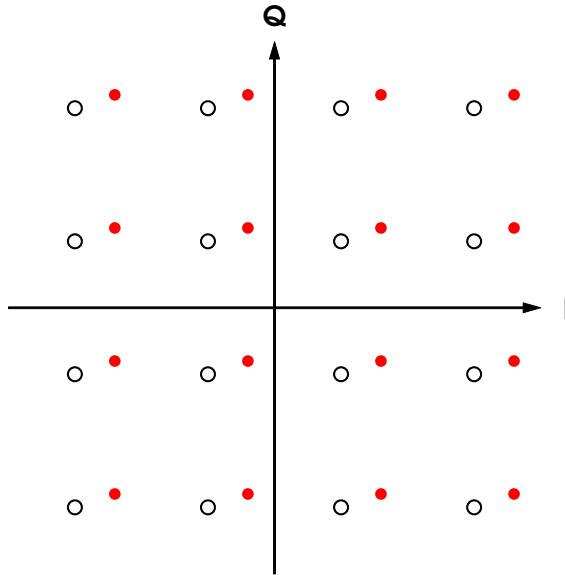


Figure 3.10: DC offset translates the I/Q constellation.

Noise

There are several noise sources in the transmitter. Quantisation noise in the DAC bounds the maximum SNR achievable but is usually not the limiting factor for wide-band systems², the transmit chain noise figure and LO noise floor contribute to the SNR for millimetre wave transmitters. In the absence of linearity, phase noise primarily from the VCO but with contributions from the LO generation circuits is the dominant source of EVM degradation in Silicon 60 GHz transmitters.

Phase noise is the close in fluctuations in frequency from the VCO. Within the loop bandwidth of the PLL the phase noise is reduced to a frequency scaled version of the crystal, outside the loop bandwidth the VCO sets the phase noise and further out the LO generation (multiplier, divider and buffer circuits) and TX chain noise figure set the noise floor.

²DAC dynamic range is typically increased to account for back-off to accommodate high PAR and also out of band noise floor.

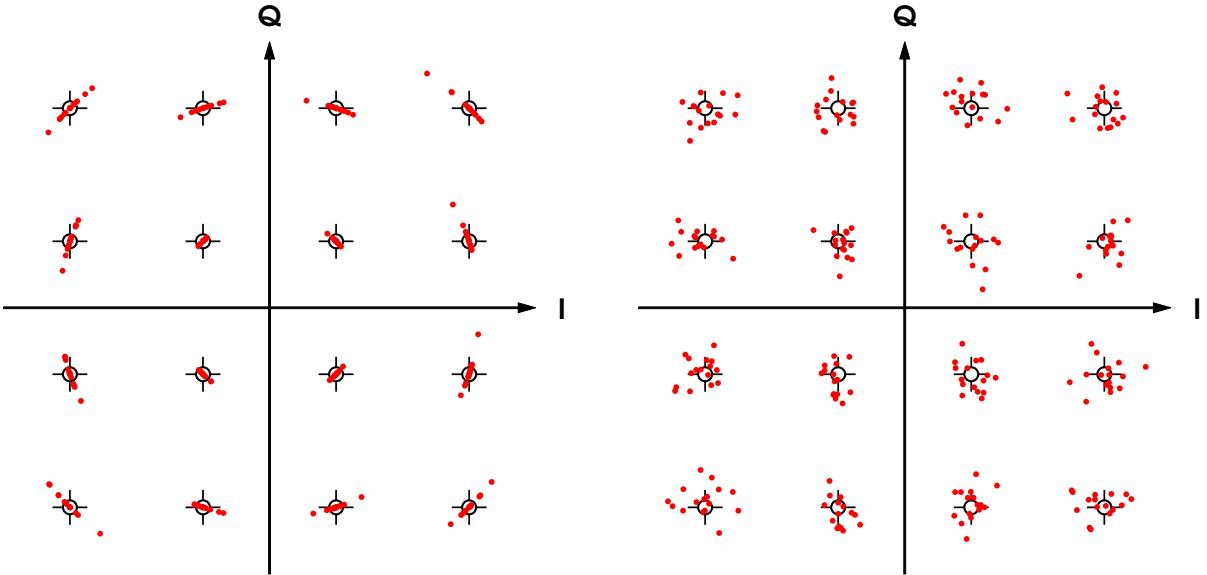


Figure 3.11: 16-QAM constellation with phase noise.

Figure 3.12: 16-QAM constellation with 10dB TX SNR.

Non-linearity

Non-linearity can occur at any point in the transmit chain but to get the highest efficiency it should be dominated by the PA. Memory-less non-linearity can be defined using two characteristics: amplitude to amplitude conversion (AM-to-AM) and amplitude to phase conversion (AM-to-PM).

AM-to-AM conversion is the compression in power as the output signal is increased. AM-to-AM conversion in a linear amplifier is usually quantified by the 1dB compression point as shown in Figure 3.13.

AM-to-PM conversion is the modulation of output phase based on the size of the input signal. AM-to-PM conversion is shown in versus input power in Figure 3.14.

AM-to-AM and AM-to-PM are

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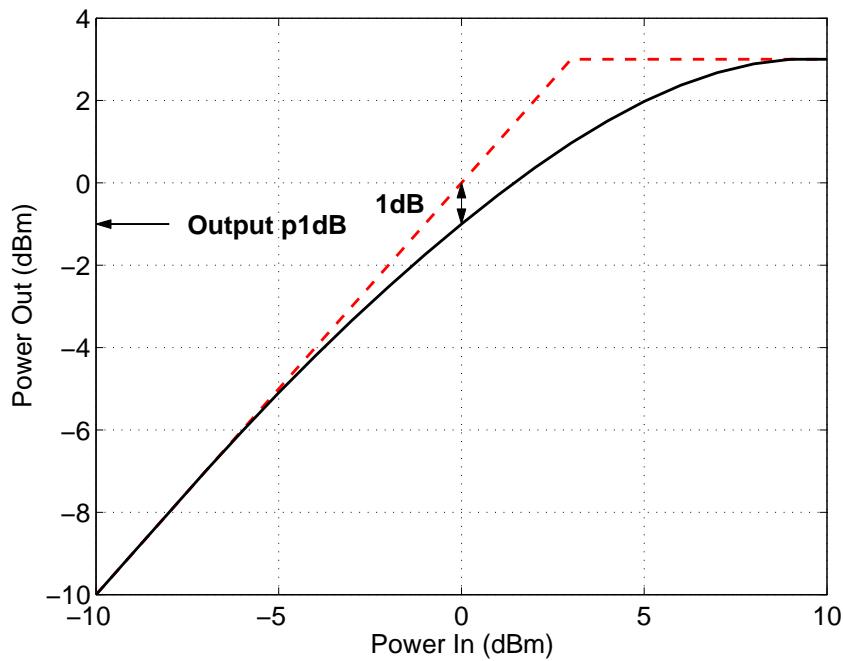


Figure 3.13: Output 1dB compression point definition.

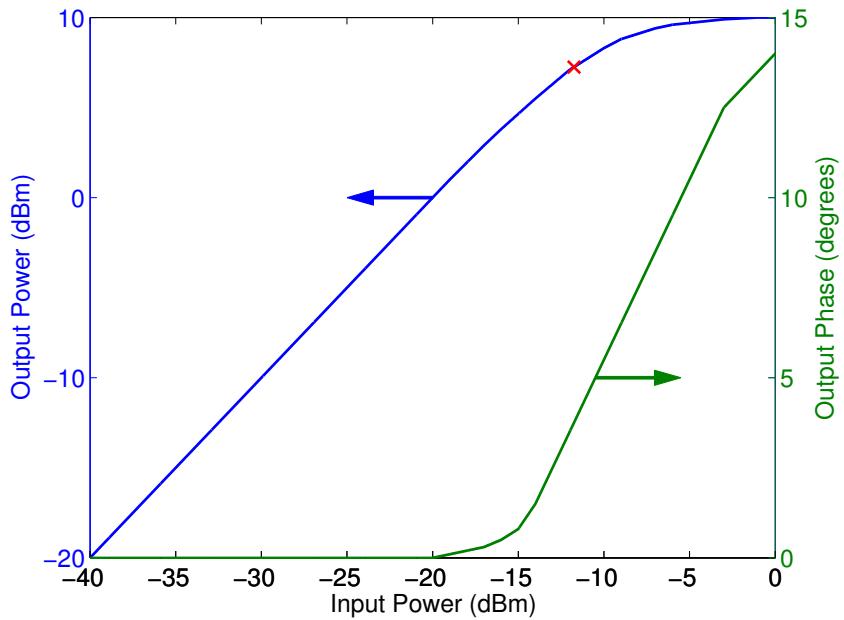


Figure 3.14: Example plot of am-am and am-pm characteristics for a transmitter.

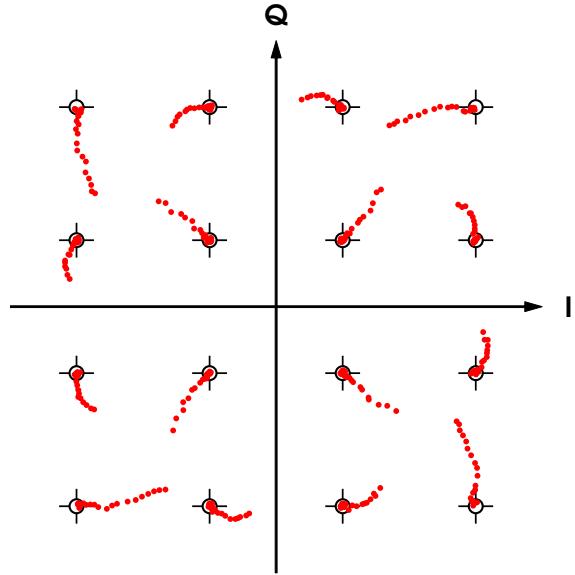


Figure 3.15: 16-QAM constellation pushed into hard compression. A noise floor of -40dB is added to the transmitter. The PA is pushed to saturation. The power of each constellation is normalized.

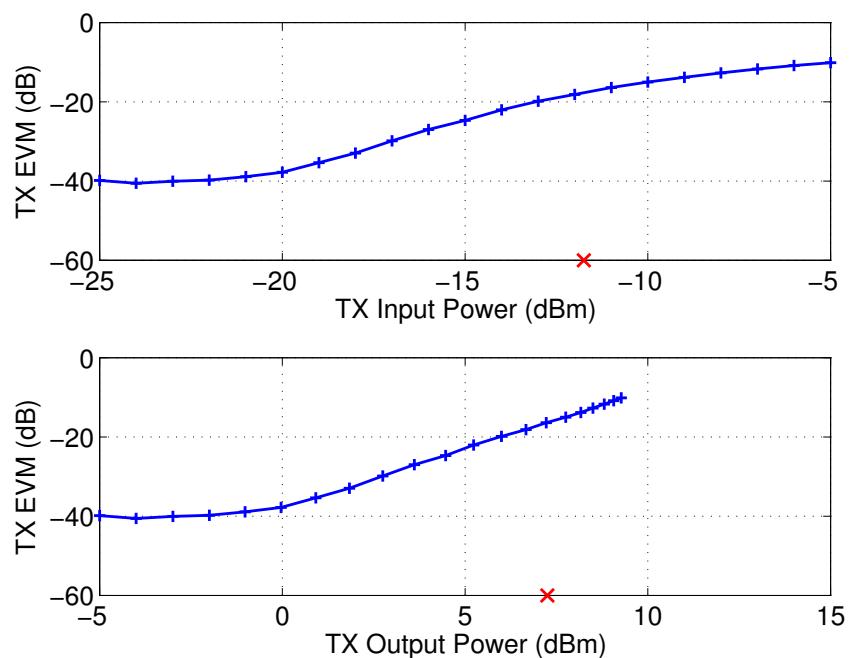


Figure 3.16: Plots showing TX EVM versus input and output power. A noise floor of -40dB is added to the transmitter.

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Intermodulation distortion

Spectral re-growth refers to the out-of-band frequency components generated in the transmitter. Spectral regrowth can be generated by non-linearity in the transmit chain, insufficient analog filtering of a Nyquist sampled DAC, insufficient digital filtering in an oversampled DAC or noise from the transmit chain on PLL but it should be dominated by the PA [55]. In a system where the PA dominates transmit power, allowing the spectral regrowth to be PA dominated enables the transmitter to perform at peak efficiency.

Spectral regrowth is limited by the transmit spectral mask as defined in the relevant standard. The 802.11ad spectral mask is shown in Figure 3.17.

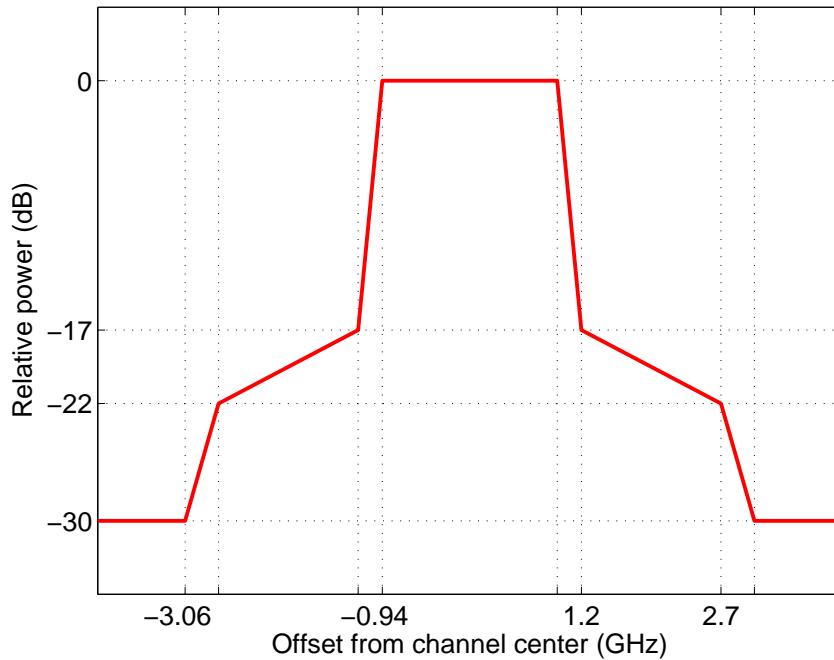


Figure 3.17: 802.11ad spectral mask [13].

Spectral regrowth occurs when frequency components from the signal or its harmonics inter-modulate with each other to produce out of band components.

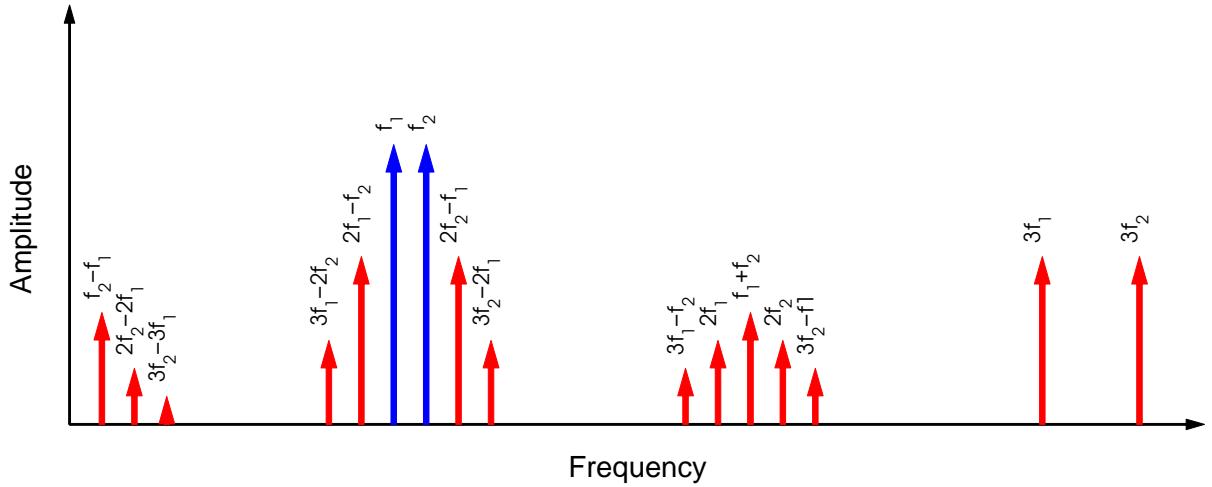


Figure 3.18: Two input frequencies f_1 and f_2 inter-modulate to create many output components.

All Impairments

None of the TX impairments operate alone, they combine to distort the transmitted signal. Some are easy to correct with calibration in the digital baseband (I/Q phase and amplitude imbalance), in the analog domain (DC offset) and some are not easily reduced in a wide-band system (PA non-linearity). Figure 3.19 shows the combination of several impairments.

3. TRANSMITTERS AND PHASED ARRAYS

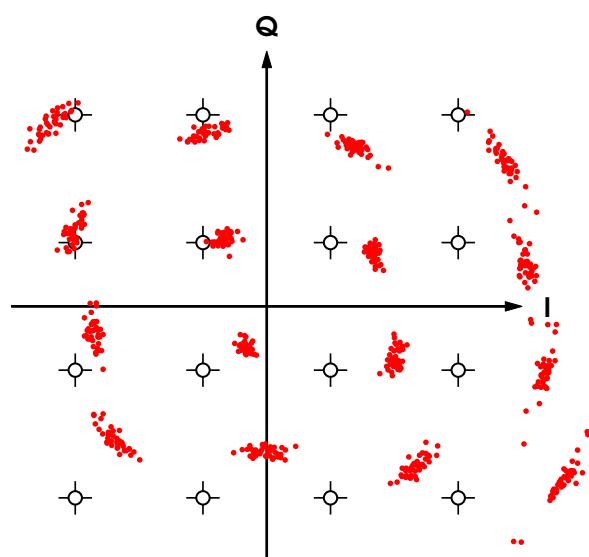


Figure 3.19: Combination of TX impairments.

3.4 Phased Arrays

Phased array systems have been used for RADAR [56, 57, 58], communication links [59, 60, 61] and satellite systems [62]. They offer several advantages over conventional single antenna systems and are especially attractive at millimetre-wave due to the small wavelength. This chapter looks at why phased arrays are uniquely suited for millimetre-wave transceivers, the benefits, some fundamentals, system level considerations and challenges.

Phased arrays are made up of 2 or more antennas which can be excited with specific phases to form a focused beam. Many applications can benefit from the focused transmission and reception of energy rather than using a broad beam. In an active phased array, changing the relative phases at each antenna enables the beam to be steered. The following properties control the performance of an array [63, 64]:

1. The position of each element
2. The excitation amplitude of each element
3. The excitation phase of each element
4. The antenna pattern (or unit pattern) of the elements

Phased arrays are required at millimetre-wave frequencies due to the higher free space path loss. It is important to note however, that they are easily implementable at these frequencies due to the small wavelength that enables many antennas to be placed in a small area. For example, in the same area that a 5GHz antenna occupies, 20 or more 60 GHz elements can be placed.

3.4.1 Array Pattern

The array pattern of a phased array is the summation of individual elements in the far field. In the case where identical elements are used, it can be defined as the product of the unit element pattern and the array factor [51]. If $\mathbf{d}_0, \mathbf{d}_1, \mathbf{d}_2, \dots$ denotes the position of elements with relative feed coefficients a_0, a_1, a_2, \dots then the array factor can be given as [65]:

$$A(\mathbf{k}) = a_0 e^{j\mathbf{k} \cdot \mathbf{d}_0} + a_1 e^{j\mathbf{k} \cdot \mathbf{d}_1} + a_2 e^{j\mathbf{k} \cdot \mathbf{d}_2} + \dots \quad (3.15)$$

The array factor for a linear array of elements is shown in Figures 3.20 to 3.23. In the 1 element case, there is no array, the array factor is a unit circle. For 2 elements the beam-width is reduced to 46.1° and 11.2° for 8 elements.

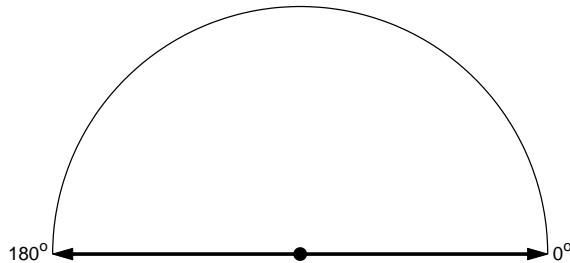


Figure 3.20: 1 element array factor

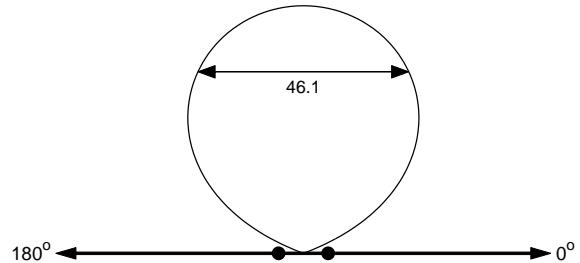


Figure 3.21: 2 element linear array factor, $\frac{\lambda}{2}$

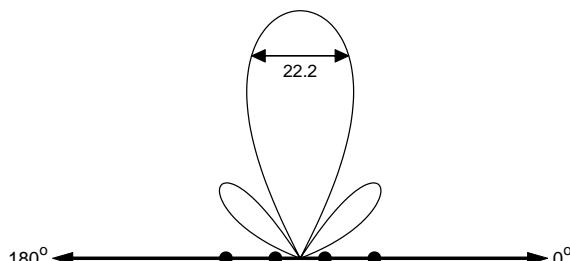


Figure 3.22: 4 element linear array factor, $\frac{\lambda}{2}$

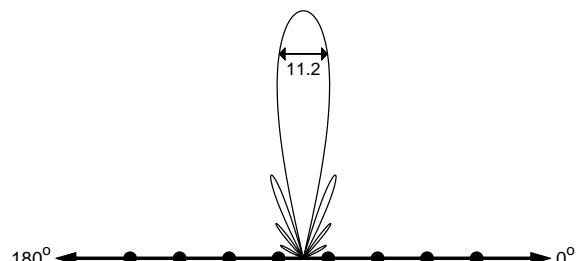


Figure 3.23: 8 element linear array factor, $\frac{\lambda}{2}$

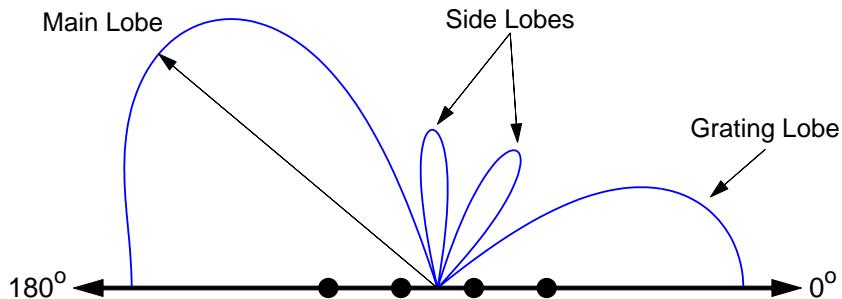


Figure 3.24: 4 element array, $\frac{\lambda}{2}$ spacing, with annotations

3.4.2 Array Gain

The array gain for a phased array is the increase in gain beyond a single element due to the array factor. Ideally, every doubling of antennas increases the array gain by 2x. In decibels this can be expressed as an increase of $10 \times \log_{10}(n)$ where n is the number of elements in the array.

3.4.3 Array Steering

Increasing the number of antennas for more gain is useful only if they beam can be steered. In an active phased array, steering is achieved by adjusting the relative phase at each antenna. Side-lobe levels can be changed by adjusting the excitation amplitude as well as the phase but this is rarely done in communication systems since reducing side-lobes usually also results in decreased power in the main lobe and maximising the link margin is more important than minimising energy elsewhere.

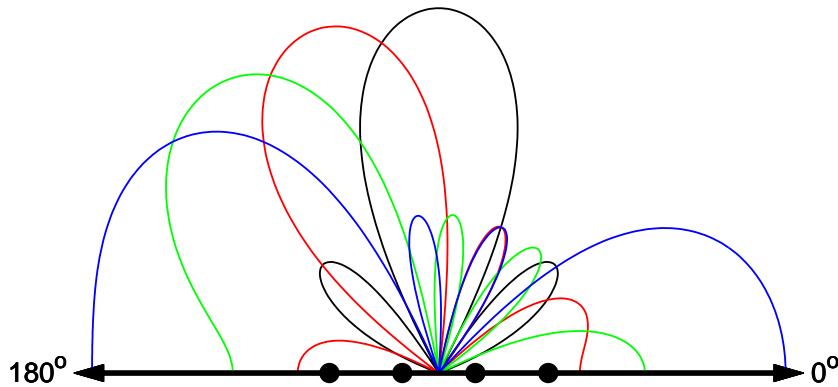


Figure 3.25: 4 element array, $\frac{\lambda}{2}$ spacing, steering from 90 to 150

3.4.4 Increase in Transmit EIRP

In a phased array transmitter, energy is radiated from multiple antennas and combined in space. Phased array transmitters not only benefit from the increase in antenna gain but also benefit from the spatial power combining of multiple power amplifiers. The increase in EIRP beyond a single transmit chain is:

$$10 \times \log_{10}(n) + 10 \times \log_{10}(n) = 20 \times \log_{10}(n) \quad (3.16)$$

Figure 3.26 shows the increase in TX EIRP relative to a single antenna with increasing number of front-ends.

3.4.5 RX SNR Improvement

Compared to a single antenna receiver, multiple antennas improve the received signal SNR by:

$$10 \times \log_{10}(n) \quad (3.17)$$

The SNR improvement is shown in the Figure 3.26

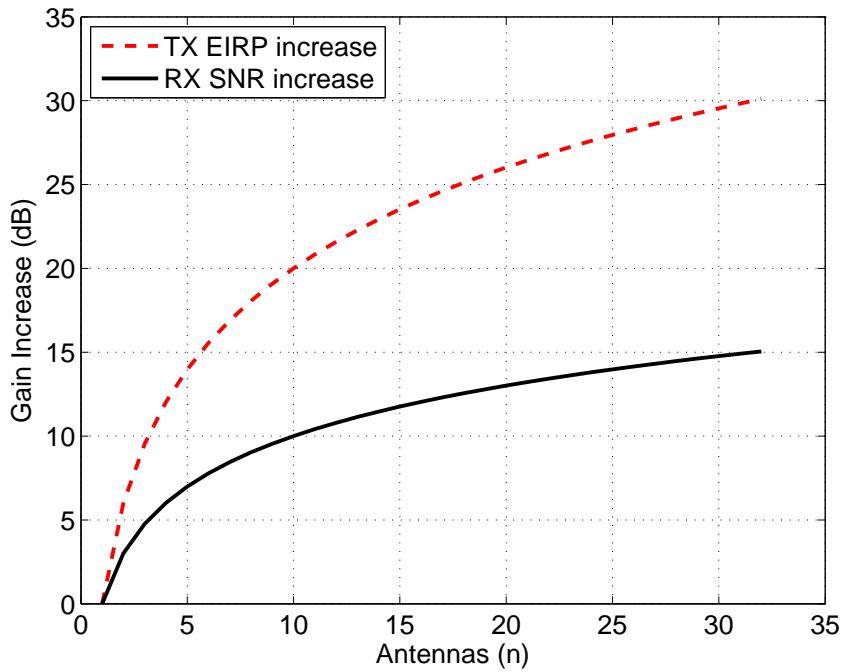
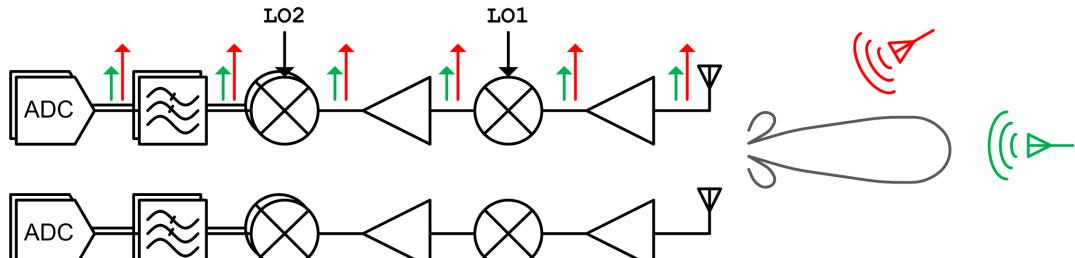


Figure 3.26: TX EIRP and RX SNR increase vs. Antennas

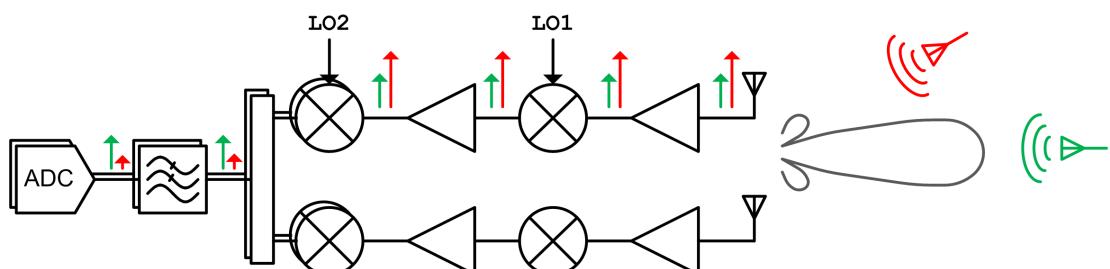
3.4.6 Phased Array Architectures

Figure 3.27 shows four different architectures for phased arrays. Digital phase combining is used in MIMO systems but is not ideal for a phased array as each chain needs to be duplicated for each antenna. Phase shifting in the LO path reduces imperfections in the RF path and is simpler in a super-heterodyne architecture when done at the second LO. Phase shifting in the RF path results in the lowest power and area.

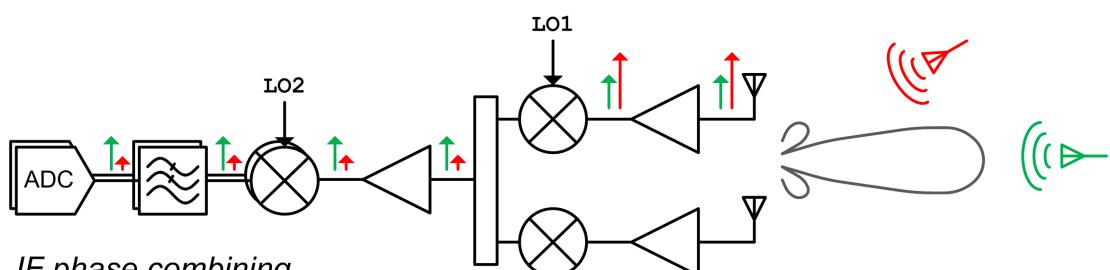
3. TRANSMITTERS AND PHASED ARRAYS



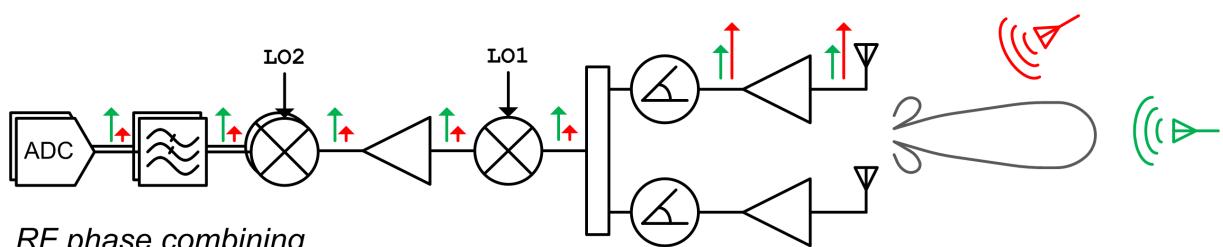
Digital phase combining



Baseband phase combining



IF phase combining



RF phase combining

Figure 3.27: Phased Array Architectures

3.4.7 Link Budget

A link budget for a 16TX, 16RX 60 GHz phased array system is shown below. The noise at the receiver input can be defined as:

$$N_{tot} = kT_0B \quad (3.18)$$

where:

$$k = 1.38e^{-23} \text{ Joule}/\text{°C} \text{ (Boltzmann's constant)}, \quad (3.19a)$$

$$T_0 = 270 \text{ °K} \text{ (Receiver temperature)}, \quad (3.19b)$$

$$B = 1.86 \text{ GHz} \text{ (Receiver bandwidth)} \quad (3.19c)$$

For a representative 60 GHz 802.11ad single carrier system, the total noise at the receiver input is:

$$N_{tot} = 1.38e^{-23} \times 270 \times 1.86e^9 \quad (3.20)$$

$$= -81.3 \text{ dBm} \quad (3.21)$$

Given a system noise figure of 10dB and 10dB SNR margin for QPSK demodulation, the receiver sensitivity is:

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$$S_{min} = N_{tot} + NF + SNR \quad (3.22)$$

$$= -61.3 dBm \quad (3.23)$$

The system sensitivity can be defined as the receiver sensitivity with antenna / system gain added. In the case of a 16 element system with 3dBi unit elements (average routing loss is included) the additional system gain is:

$$G_{rx} = 10 \times \log_{10}(n) + G_{ant} \quad (3.24)$$

$$= 15 dB \quad (3.25)$$

$$RX_{sens} = S_{min} - G_{rx} \quad (3.26)$$

$$= -76.3 dBm \quad (3.27)$$

$$(3.28)$$

At the transmitter, given 16 antennas with 0dBm output power each, the transmit EIRP can be given as:

$$TX_{eirp} = P + 20 \times \log_{10}(n) + G_{ant} \quad (3.29)$$

$$= 27 dBm \quad (3.30)$$

The link margin is the difference in TX_{eirp} and RX_{sens} :

$$LM = TX_{eirp} - RX_{sens} \quad (3.31)$$

$$= 103.4dB \quad (3.32)$$

In an AWGN channel, the range can be calculated from the free space path loss:

$$FSPL = \left(\frac{4\pi d}{\lambda} \right)^2 \quad (3.33)$$

$$d = \frac{\lambda \sqrt{FSPL}}{4/\pi} = 58.8m \quad (3.34)$$

The resulting distance of 58.8m indicates the best case possible and different channel types, reflection loss and margin for AGC and other system factors will reduce this. Figure 3.28 shows the difference in link distance for different number of antennas in the array. In this plot both TX and RX antennas = n .

3.4.8 Blocked Links

The propagation of millimetre wave signals is significantly different to lower frequency signals. Unlike 2.4GHz and 5GHz which are composed of multiple waves coming from a primary and multiple secondary sources, 60 GHz can be viewed more like a quasi-optical signal. This is due to the small wavelength which results in reduced diffraction

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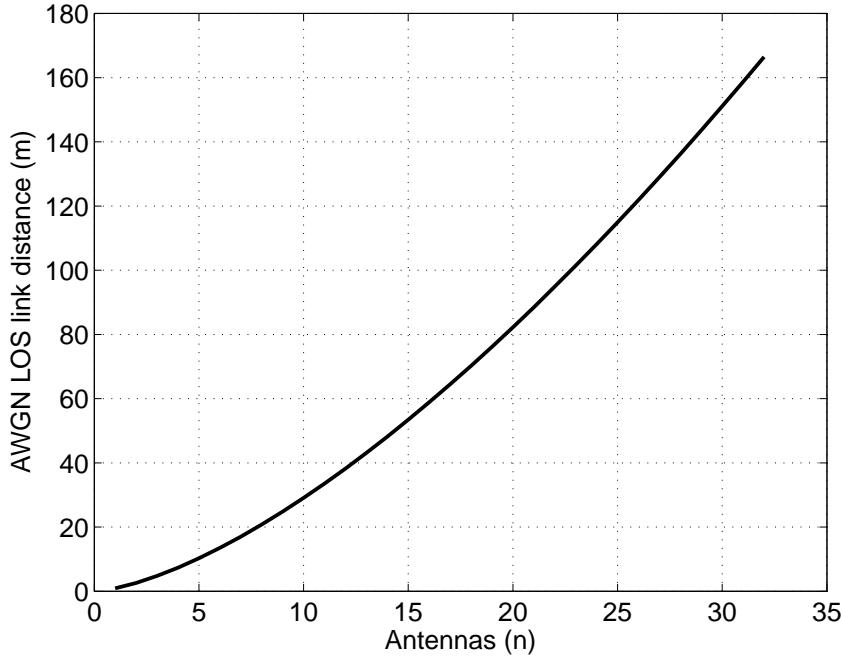


Figure 3.28: LOS link distance in an AWGN channel for increasing antennas

effects and sharp shadowing losses [66].

The modelling of 60 GHz links is typically done with ray tracing software which calculates the potential spatial paths between a transmitter and receiver and the losses due to reflection.

For millimetre wave links >10m, high gain, steerable antennas are used to close the link budget. The losses due to blockage by humans can be on the order of 20-30dB [14], in this case, steering around the blocked link by using a reflected path often results in better link performance. Reflection losses in typical office environments are on the order of 10dB [14].

Figures 3.29 and show a LOS link using a reflected path after being blocked by a human.

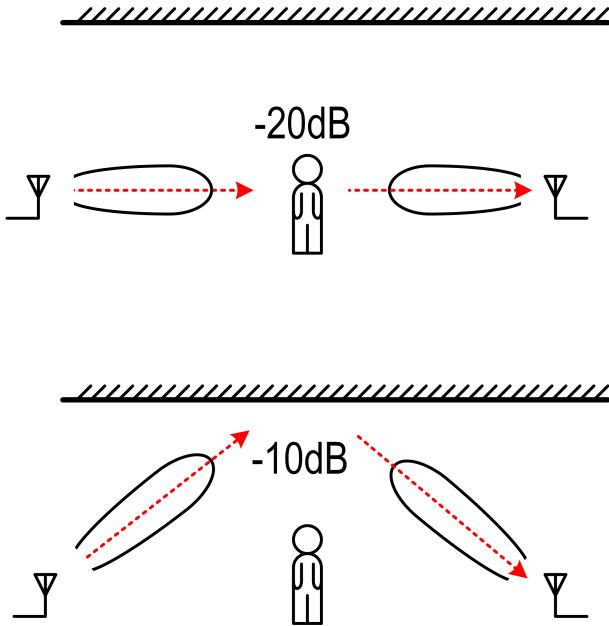


Figure 3.29: A blocked LOS link is shown at the top. In this link, the blocker has 20dB loss. In a beam-formed system, it is better to steer around the blocker and use a reflected path. The loss of due to reflection varies based on the material but 10dB has been found to be a reasonable approximation [14].

3.4.9 Optimal Number of TX Antennas

In a real phased array system constraints such as maximum power dissipation and routing losses impact the optimal number of antennas. The EIRP of n antennas can be defined as:

$$EIRP(n) = 20 \times \log_{10}(n) + P_{out} \quad (3.35)$$

A simple transmitter is shown in Figure 3.30. In a system constrained by a power limit, and assuming several overheads which cannot be reduced, the EIRP for the transmitter can be given by:

3. TRANSMITTERS AND PHASED ARRAYS

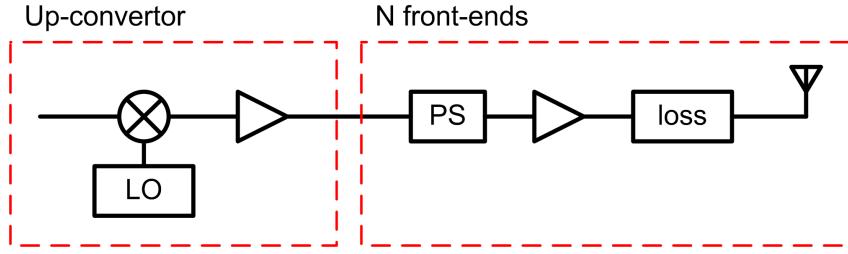


Figure 3.30: Simple transmitter block diagram

todo: fix this equation

$$Pdc_{avail} = Pdc_{max} - Pdc_{core} - n \times Pdc_{fixed} \quad (3.36)$$

$$Pdc_{pa} = \frac{Pdc_{avail}}{n} \quad (3.37)$$

$$Prf_{out} = 10 \times \log_{10}(Pdc_{pa} \times PA_{eff}) \quad (3.38)$$

$$EIRPconstrained(n) = 20 \times \log_{10}(n) + Prf_{out} - n \times 1.5 \times loss \quad (3.39)$$

$$(3.40)$$

where,

$$loss = \text{Routing to antenna loss in dB/mm} \quad (3.41)$$

Figure 3.31 shows this analysis for 600mW total power, a fixed overhead of XXmW per front-end and routing loss of 0.3dB/mm. It can be seen that around 8 antennas is optimal. Different system parameters will result in different optimum.

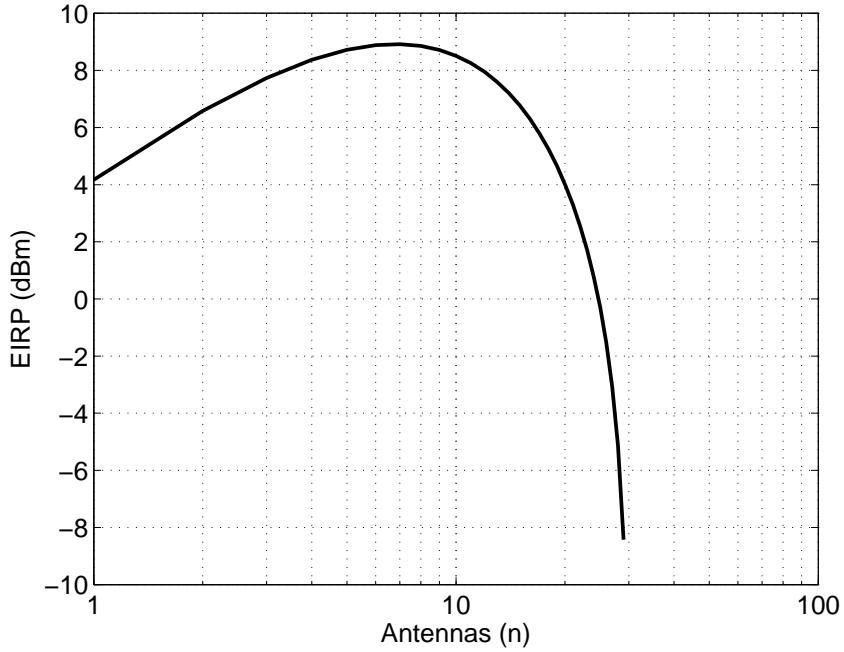


Figure 3.31: Total EIRP vs. number of TX antennas for a fixed power budget

3.4.10 TX/RX Switch

In most WLAN and BT systems a single antenna is used with a TX/RX switch. At 60 GHz the switch loss can be in the range of 1-2dB depending on technology and implementation [67]. Depending on the area available for the antenna array and the performance requirements of the system a choice can be made between separate TX and RX arrays or a single array with TX/RX switches. In almost all cases, a single array using shared TX/RX antennas which achieves the maximum aperture area with lowest routing losses is the most optimal.

3. TRANSMITTERS AND PHASED ARRAYS

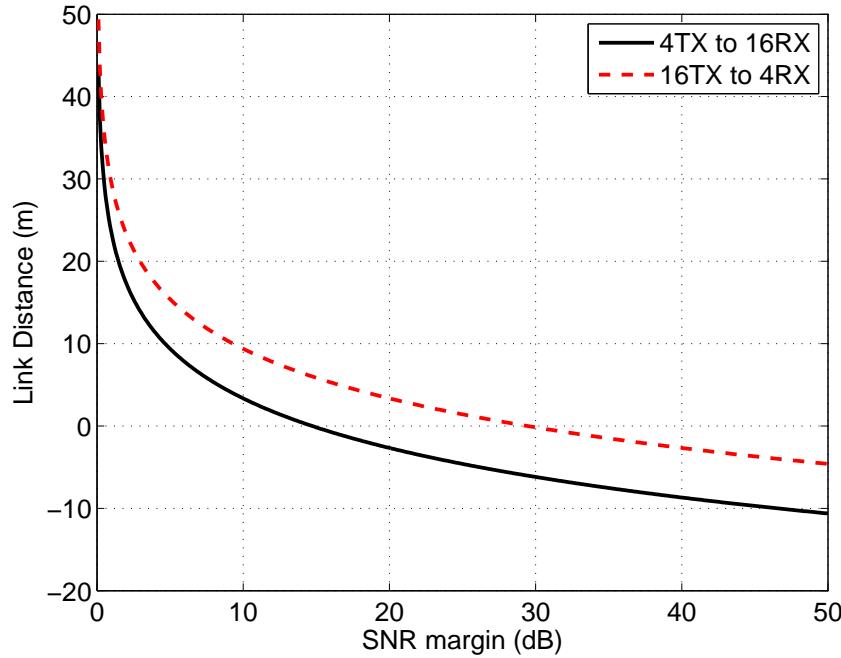


Figure 3.32: Link SNR margin vs. distance for an asymmetric link setup

3.4.11 Asymmetric Links

In the 60 GHz eco-system handheld devices will communicate with powered (always plugged in) devices such as routers, televisions, monitors and docks. In such an environment it is important to try and limit the power use by battery operated devices and push as much of the burden on the plugged in device. The limiting case is battery to battery communication such as cellphone to cellphone. If cellphone to cellphone (or tablet to cellphone) communication can be limited to LOS with the assumption that the user will help with orientation then an efficient system can be implemented.

In an ecosystem where different devices have different numbers of antennas, and assuming the power amplifiers on both sides of the link are the same, the forward and reverse links have different margin. For example, in the case where a cellphone has 4 antennas and a television has 16 antennas the following graph shows SNR margin

versus distance for 4TX to 16RX and 16TX to 4RX. In the first case the AWGN LOS distance is 15m and 30m in the second.

4

High Efficiency Power Amplifiers

4.1 Introduction

Power amplifiers are a core component in RF transmitters. They are responsible for the efficient delivery of RF power to a load [42]. The power of a transmitter is often dominated by the PA. By increasing the efficiency of the PA the transmitter efficiency and system power can be improved.

In high power, low frequency systems like cellular base stations, the limiting factor is often thermal and cooling effects. Increasing the efficiency by even a few percent helps increase the radiated power substantially. In millimetre-wave transmitters the power amplifiers operate at much lower power but with several in parallel. For consumer

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devices which operate from a battery, a peak power limit is imposed by the system architect. In this case, increasing efficiency either allows increased output power (higher performance) or, if this is not required, result in an improvement in battery life.

The importance of efficiency is shown in Figure 4.1, for a required output power the normalised power consumption versus efficiency is shown. It can be seen that at very low efficiencies which are characteristic of millimetre-wave power amplifiers, increasing efficiency only slightly makes a huge difference in system power consumption.

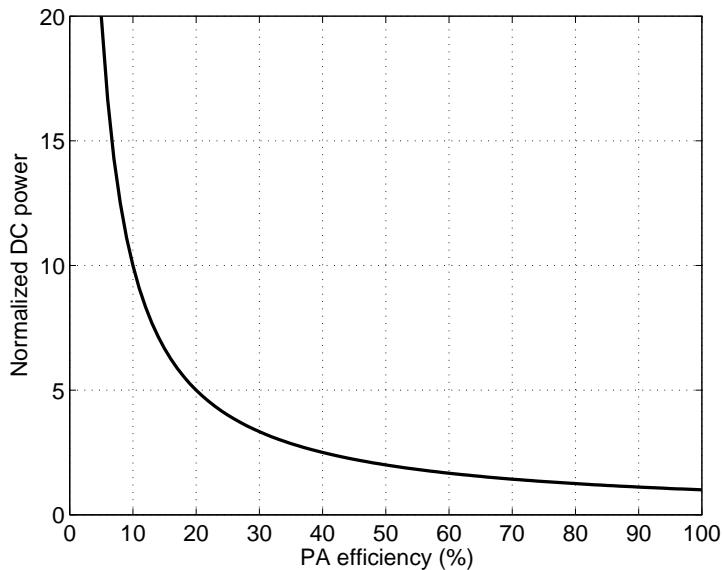


Figure 4.1: Normalised DC power of a PA versus the efficiency.

This chapter presents some fundamentals of high frequency power amplifier design and a methodology which results in the first time right design of four power amplifiers.

The first PA is a low frequency, high efficiency design undertaken for the 2007 IMS student high efficiency power amplifier competition, an annual event held at the IMS-RFIC conference. This power amplifier won the competition with a measured efficiency of 88% [68]. While not a millimetre-wave power amplifier, many of the same modelling, simulation and design techniques apply on a board level hybrid as they do

on a chip level integrated circuit.

The second power amplifier is a transmission line based design in Jazz 0.18um Silicon Germanium. This power amplifier has a wide bandwidth with only 2.5dB variation from 57-64GHz. It achieves a peak gain of 30dB and has a p1dB of 8-9dBm. It suffers from a large area due to the transmission lines.

Two transformer based power amplifiers for 60GHz applications are shown in the last section of this chapter. They show that transformer based designs can achieve high performance while taking much less area than their transmission line based counterparts. The first, a four stage transformer coupled power amplifier designed in SiGe achieves a the same performance as the transmission line design with a reduction in area of 4x. The second, also a four stage design but in CMOS, achieves the same area saving and achieves a state of art efficiency of 7.7% at 1dB compression [69].

4.2 Fundamentals

A simple transmitter with the integrated PA highlighted in blue is shown in Figure 4.2.

The PA is placed after the last up-conversion stage and connected to the output of the chip where it interfaces to the antenna. Power amplifier designs need to take performance, efficiency, reliability (from ESD, device stress and antenna mismatch) into consideration. This section reviews some system requirements, topologies and optimization points for power amplifiers.

4. HIGH EFFICIENCY POWER AMPLIFIERS

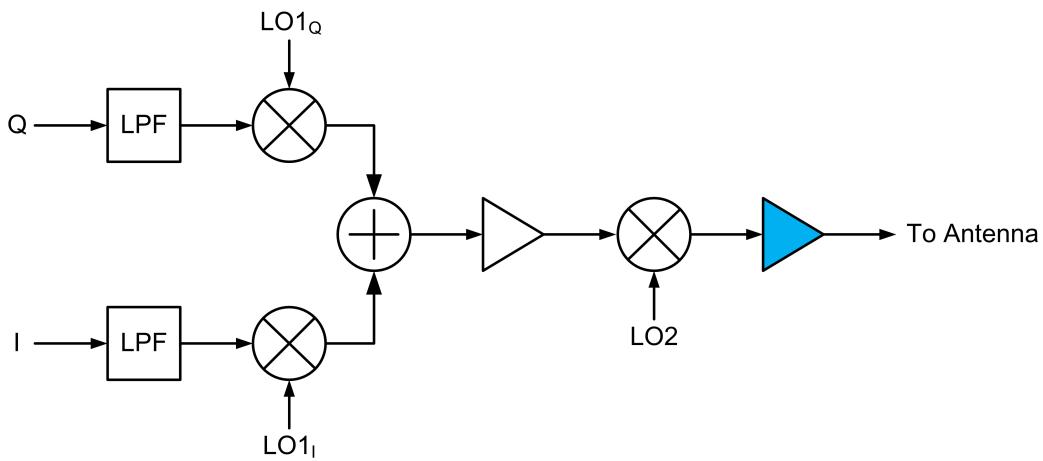


Figure 4.2: Block diagram of a transmitter with the PA highlighted in blue.

4.2.1 Key Parameters

Several key parameters for power amplifiers are outlined below.

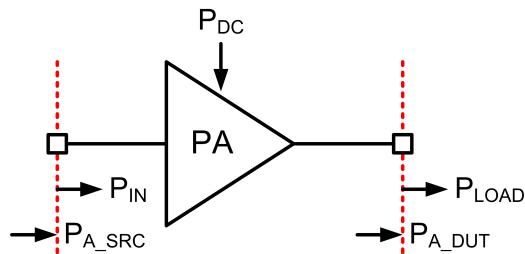


Figure 4.3: PA with annotated power definitions.

Power added efficiency (PAE) is a measure of efficiency which takes into account the gain of the device.

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (4.1)$$

Transducer gain (G_T) is the power delivered to the load divided by the power available from the source.

$$G_T = \frac{P_{LOAD}}{P_{A_SRC}} \quad (4.2)$$

Power gain (G_P) is the power delivered to the load divided by the power available into the amplifier. It only takes into account output match.

$$G_P = \frac{P_{LOAD}}{P_{IN}} \quad (4.3)$$

Available gain (G_A) is the power available from the amplifier divided by the power available from the source. It only takes into account input match.

$$G_A = \frac{P_{A_DUT}}{P_{A_SRC}} \quad (4.4)$$

4.2.2 PA Efficiency

The maximum theoretical efficiency for a class-A power amplifier with an inductive tank is 50%, for a simple amplifier with 1V Vcc, 10mA quiescent bias current and 100ohm load, this is shown in the following equations.

$$\begin{aligned} P_{DC} &= V * I_Q \\ &= 10mW \\ P_{AC} &= \frac{V_{rms}^2}{R_L} \\ &= 5mW \end{aligned}$$

In real implementations, the theoretical efficiency is reduced by losses in the inductive

4. HIGH EFFICIENCY POWER AMPLIFIERS

tank, losses in the output matching network and limits on the voltage swing due to transistor turn-on voltage or reliability concerns.

Figure 4.5 shows a simple circuit for a linear PA and reduction in maximum efficiency due to losses in the output matching network (b), resistance in the tank inductor (c) or limits on the voltage swing (d) class-A results are shown in blue.

By biasing instead in a class-B mode, the linear PA topology can achieve better efficiency, the red dotted lines in Figure 4.5 show this.

The combined efficiency with 6 Ohms resistive losses (in tank, ground and device), 2dB loss in the output matching network, 0.2 Volt minimum swing and 6dB last stage gain is 12% for class-A and 20% for class-B. This is just the last stage efficiency, adding additional stages which is typically required at 60 GHz results in even lower efficiencies.

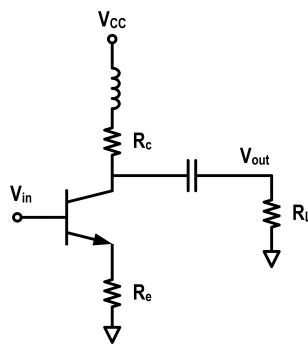


Figure 4.4: Example linear PA schematic.

Waveform engineering techniques [70] that involve increasing efficiency by terminating specific harmonics of the amplifier with certain impedances to achieve class D, F, E (or their inverse) require the core transistor to have gain at these harmonics. For 60 GHz designs, the second harmonic is 120 GHz, third 180 GHz and fourth 240 GHz. With limited f_{max} the useful harmonics are really only the first and possibly second in

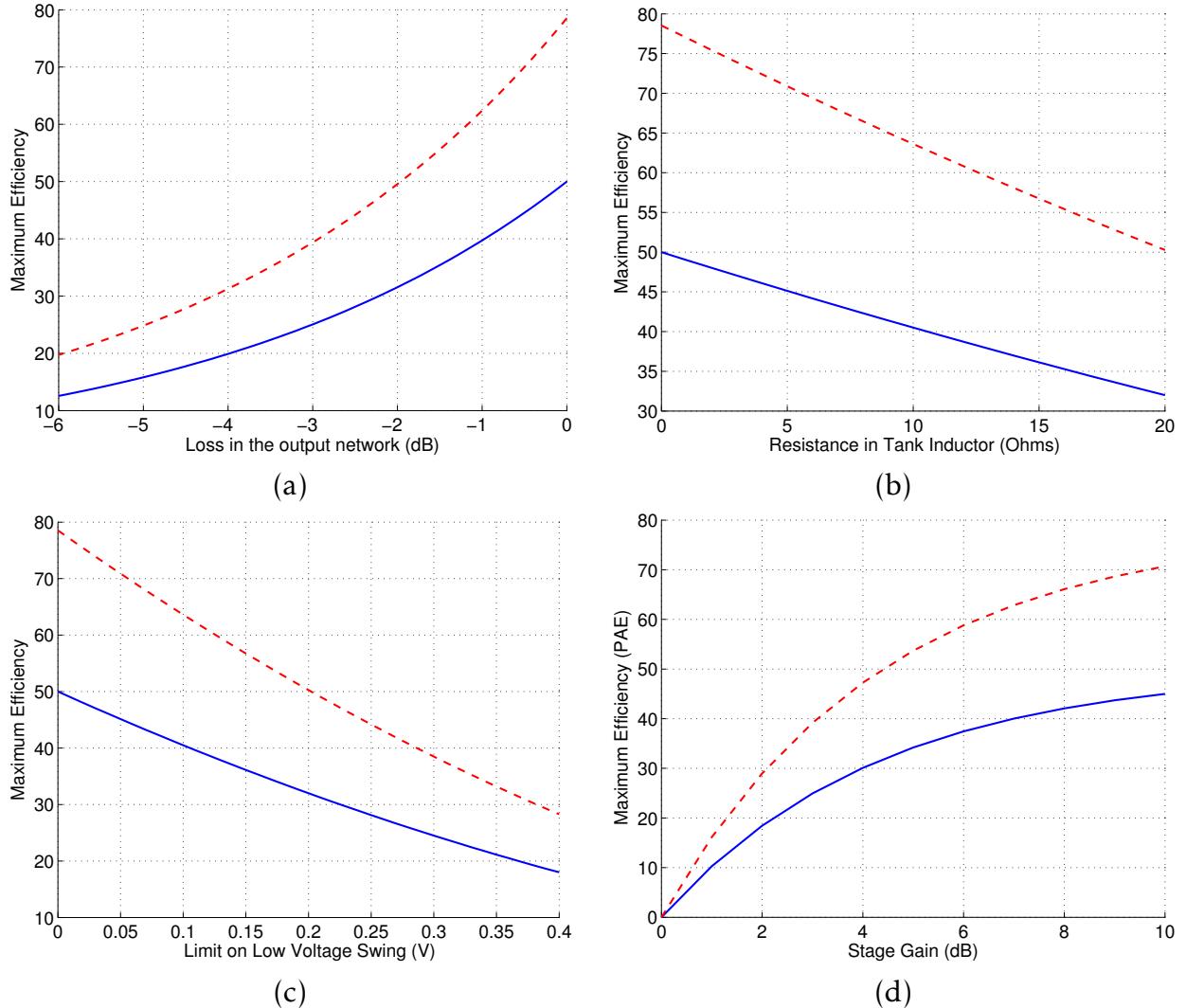


Figure 4.5: (a) frontend option with separate TX and RX antennas (b) frontend option with shared antenna using SPDT switch (c) frontend option with shared antenna using DPDT switch

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0.18um SiGe and maybe the third in 65nm CMOS.

The type of modulation used dictates how much distortion can be introduced by the PA. For 11ad systems with QPSK, 16-QAM and 64-QAM modulations, the contribution from the PA can be up to 1-2%. This level of EVM usually requires a linear PA with some back-off from the saturated output power level, Figure 3.16 in Chapter 3 shows this.

With the exception of the 1GHz board level PA, the PAs in this chapter are linear designs which meet the distortion requirements for 11ad systems.

4.2.3 PA Optimisation for 60GHz Systems

In multi-element phased array systems the output power from several power amplifiers is combined in free-space. This spatial power combining offers a benefit as the power from each PA can be reduced. On the other hand, in technologies like CMOS where a low voltage supply limits the reasonable output power - required system EIRP can be achieved by increasing the number of transmit chains and power amplifiers.

Given a target EIRP, multiple power amplifiers can be used in parallel to reduce overall DC power consumption. This is shown in the following figure.

4.3 Design Methodology

A structured approach to design and modelling enables the first pass correct design of RF circuits including PAs. This chapter explores both 1GHz and 60GHz power ampli-

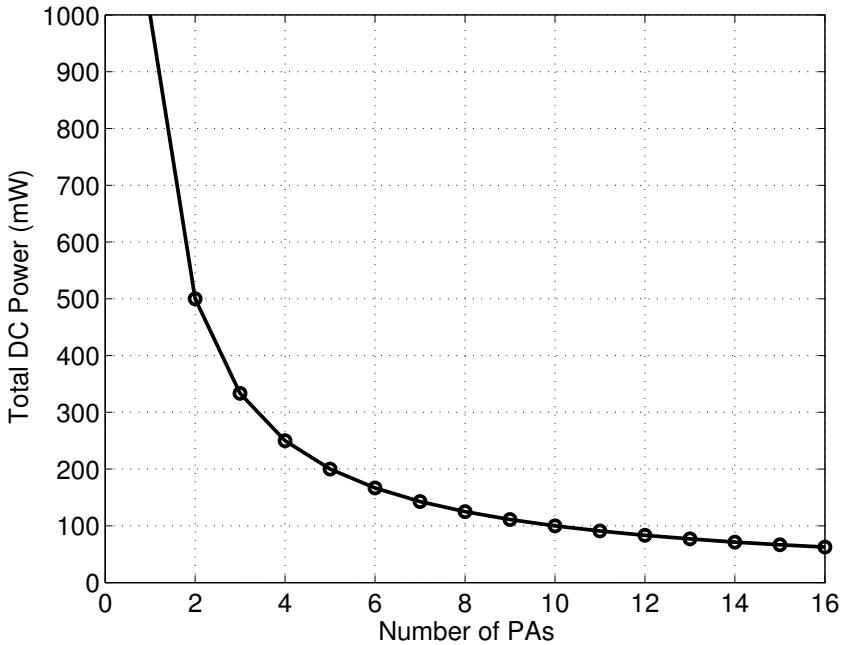


Figure 4.6: Total power to achieve a 20dBm EIRP assuming 10% PA efficiency.

fiers and both use the same design methodology. It consists of: 1) good device models 2) simple RLC extraction for small interconnect much smaller than a wavelength 3) EM modelling of custom passive devices.

This design methodology was used for the power amplifiers in this section as well as the other circuits in the next chapter.

4.3.1 Device modelling and optimisation

Device models are often provided by the manufacturer or foundry but need to be validated especially if modifying the base layout. For all the designs in this thesis, test devices were taped out with calibration structures in order to check the models. Standard calibration and de-embedding methods were used. For board level designs, calibration is done to the SMA cables then on board de-embedding structures are used

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to move the reference plane to the device under test. The short, open, load, through (thru) (SOLT), layouts are shown in Figure 4.7.

Probes are used to measure on-chip devices. In this case, the probes are calibrated to the end of the probe tips using a calibration standard such as CS-5 from Cascade Microtech. On-chip SOLT structures shown in Figure 4.8 are used to move the reference place to the device.

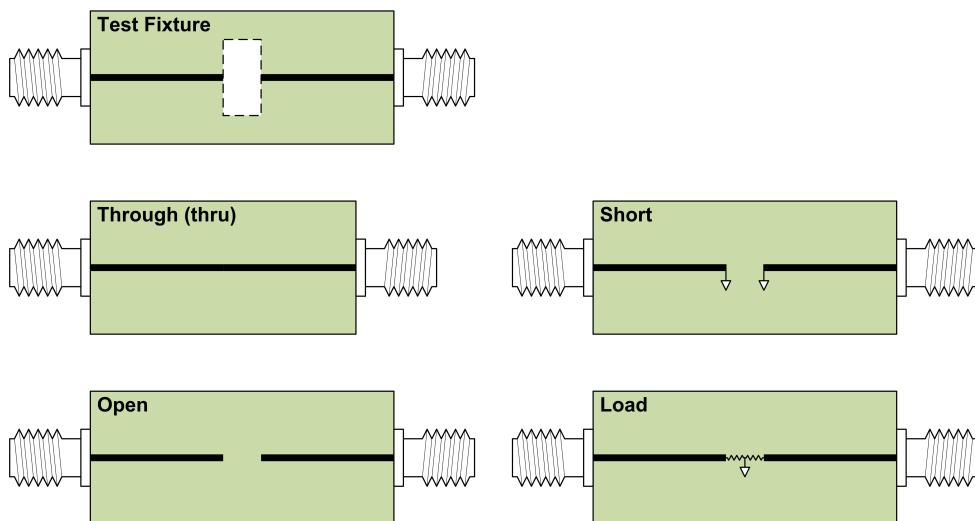


Figure 4.7: Test fixture and SOLT structures for board level design.

Transmission lines are also included in the de-embedding structures. Open short and TRL methods are both used for de-embedding and more details can be found in [71].

Once the devices are validated, they can be optimised for operation in the design.

CMOS Device Optimisation

The length, width and number of fingers need to be optimised as well as the device layout. The smallest length offered by the technology is used to reduce transit time.

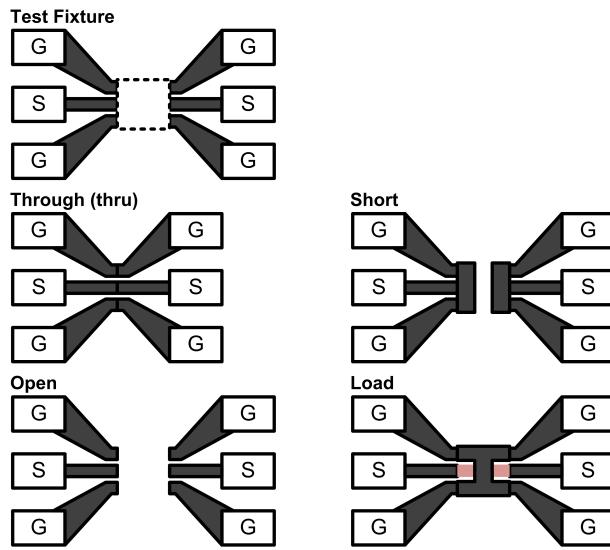


Figure 4.8: Test fixture and SOLT structures for chip level design.

The total width is the device width multiplied by the number of fingers.

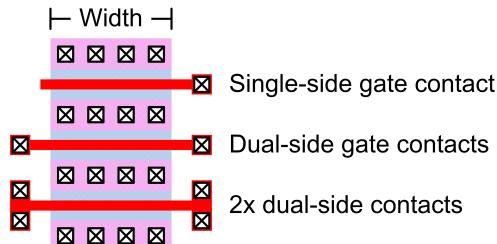


Figure 4.9: Gate contact options.

For 65nm LP technology a width of 1.0-1.5um is used to maximise performance.

The f_t , f_{max} of the transistor versus bias is shown in Figure 4.10.

The number of fingers are chosen based on the required output power of the stage.

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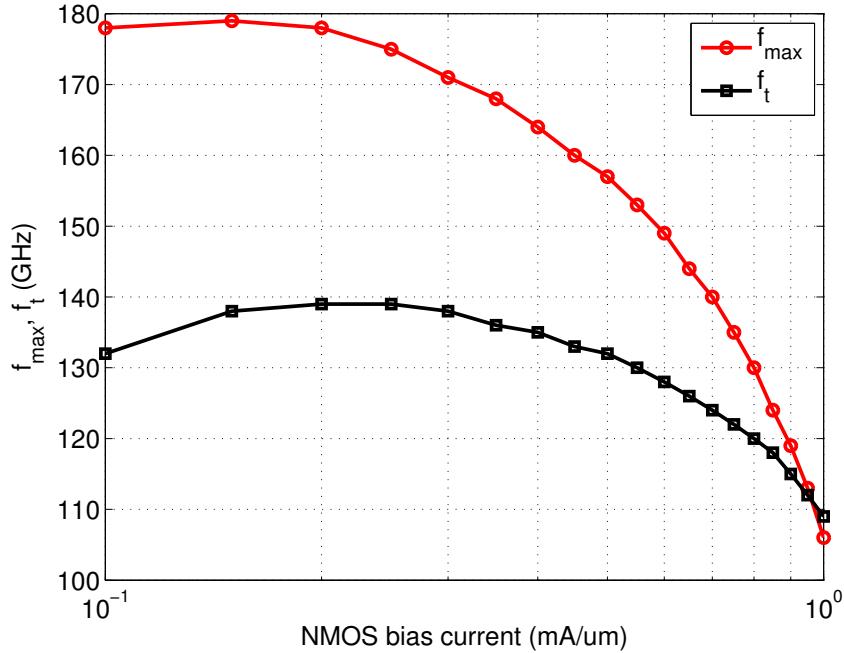


Figure 4.10: CMOS device f_t and f_{max} versus bias current.

SiGe Device Optimisation

The best topology for SiGe devices when trying to maximise speed is three base and two emitter fingers. This configuration minimises the transit time of electrons between the emitter and collector while maintaining a large emitter area [72].

The optimisation of SiGe devices is simpler than CMOS as it is usually done by the foundry and the only degree of freedom is device layout and emitter area.

4.3.2 RLC extraction

For integrated designs, the core device up to the contact or first-layer metal is usually modelled by the foundry. The parasitic elements from interconnect and escape to

the higher metal layers are not captured. Parasitic extraction is used to model these connections. It is important that a well defined reference plane is used to make sure interconnect is not double counted. Figure 4.11 shows a transistor in a test fixture with the reference plane defined in red.

All parasitics within the red boundary are extracted with parasitic extraction. Outside of this, EM modelling is used.

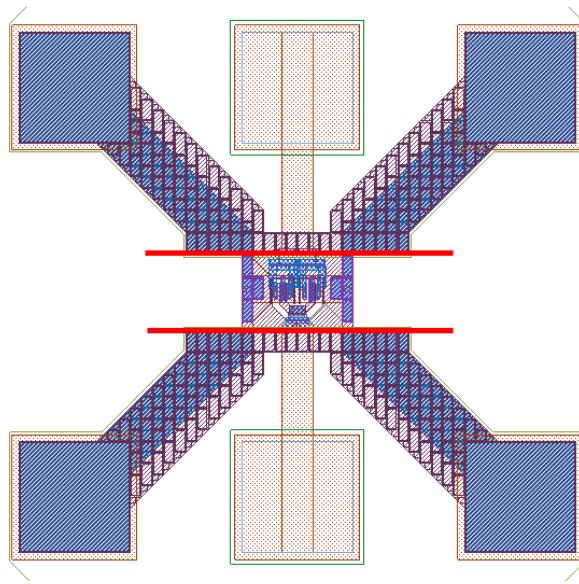


Figure 4.11: Transistor shown in test structure with reference plane defined in red.

4.3.3 Electromagnetic (EM) modelling

Proper modelling of EM devices reduces the chance of frequency mismatch, in-stability and several other problems in power amplifier design. A 2.5D or 3D simulator can be used. For the designs in this thesis HFSS was used.

As shown in Chapter 2 Figure 2.6 a clear ground return path and boundary can help with the device design. The well defined structure provides two benefits. Firstly, for

4. HIGH EFFICIENCY POWER AMPLIFIERS

single-ended designs where this path forms part of the structure, it needs to be modelled. For differential designs, it helps reduce the impact of surrounding ground loops.

4.4 A GaN HEMT amplifier with 6 Watts output power and >85% PAE

While not a millimetre-wave design, this was an interesting project investigating high efficiency power amplifiers. Many of the techniques including modelling, EM simulation and design at a board and component level translate to millimetre-wave at the chip and transistor level.

The 2007 IEEE MTT-S student power amplifier competition requires students to design and fabricate a highly efficient power amplifier. Recently published results show power amplifiers in the low GHz range with efficiencies greater than 80% [73, 74]. This chapter presents the winning power amplifier implemented with a GaN HEMT transistor and having power added efficiency greater than 85%. It will be shown that CAD simulation tools, accurate device models and sensible design rules can produce first-pass power amplifier design success. An overview of design, fabrication and testing processes is presented here together with measured results. The design was published in Microwave Magazine [68].

4.4.1 Design

The transistor chosen for this design was a 10W RF Power GaN HEMT from Cree (CGH40010). The transistor used is available in a screw-down package and is not internally matched. It comes with an accurate non-linear model which is critical for the design of high-efficiency power amplifiers. AWRs Microwave Office software was used for the design of the amplifier. It is an integrated environment that allows the design

4. HIGH EFFICIENCY POWER AMPLIFIERS

and simulation of PCB or IC RF circuits as well as providing seamless connection to EM simulators such as Sonnet. The design and modelling strategies employed are similar to that presented in [75], but were adapted to deal with a non-linear amplifier rather than Class-A. Instead of using multi-match software to synthesise the input and output matching networks, an input and load termination optimisation method was used to obtain the maximum power-added-efficiency and matching networks were designed around these components. At the heart of any efficient amplifier is a switch. The switching action results in output currents or voltages that resemble a square wave. While the PAE calculation is concerned with power at the fundamental (and hence harmonics should be minimised), these harmonics need to be present otherwise the current and voltage waves cannot exist in any other form than a pure sinusoid. Due to this, impedances at all harmonics up to the fifth were included in the input and output matching tuners. The amplifier was designed without a specific class. The main concern was what harmonic impedances could be provided at the input and output of the amplifier in order to obtain maximum efficiency. To model the effect of different terminations at the input and output of the transistor, an optimisation routine was setup where the impedance (magnitude and phase) presented to the input and output for 5 harmonics was a parameter as well as the bias and drain voltage. Loose convergence tolerances were set in the Harmonic Balance simulator and the goals of the optimisation were set to greater than 85% PAE with greater than 6 Watts output power at 1.2GHz. The efficiency generated by this method was 88% at 1.2GHz with an output power just above 6 Watts. The next step is to take the ideal components (impedance tuners) at the input and output of the transistor and turn them into real matching networks made up of transmission lines and capacitors. The transistors are bilateral in this configuration so a change of output impedance affects the input impedance and vice versa. One of the advantages of using this method allows the input match to

4.4. A GAN HEMT AMPLIFIER WITH 6 WATTS OUTPUT POWER AND >85% PAE

be designed with the output matched in a condition that achieves high efficiency (i.e. with the lossless matching network). This reduces the amount of time re-optimising the input match as the output match is changed. As time was limited, a trial and error approach was used to transform the ideal impedance tuners into real matching networks. In the future, an automated method that takes the parameters from the source and load tuners and creates the matching networks could be employed. The resulting input matching networks are shown in Figure 4.12.

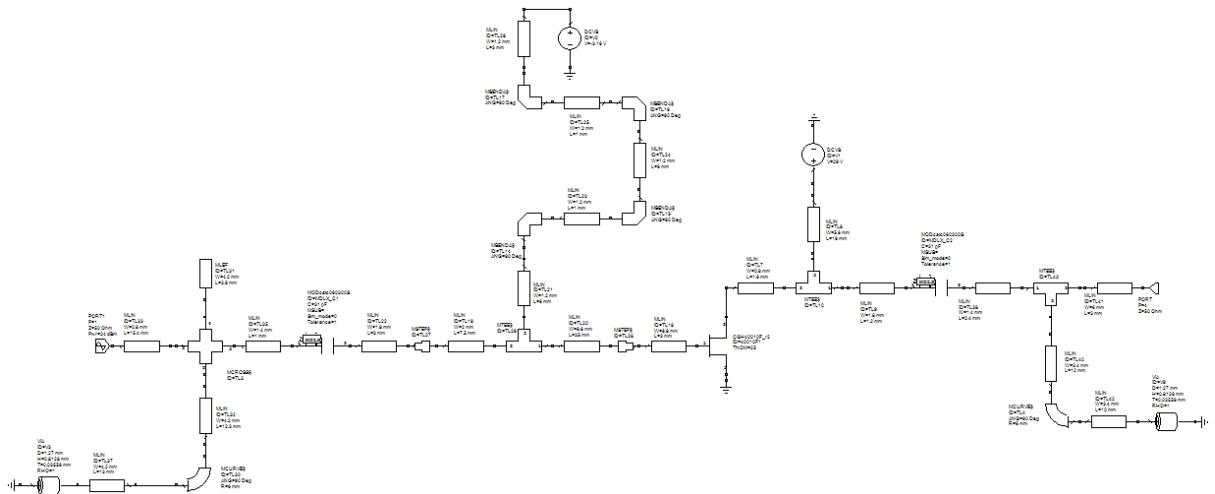


Figure 4.12: Schematic for 1GHz PA including transmission lines.

As there are some significant steps in the matching networks, Sonnet was used to analyse them. Some of the reasons that this is needed are outlined in [76, 75]. This was done in four parts. Two EM networks were created for the input and two for the output. In order to have the ability to tune out any changes to the efficiency resulting from the enhanced modelling of the matching networks, the lines were shortened by approximately 5mm at each port and transmission line component was used. This allowed Sonnet to take care of any step and coupling effects and the variable transmission lines in the schematic are used to tune out any differences. Only one EM simulation was needed for each network taking a few minutes to simulate and providing a more accu-

4. HIGH EFFICIENCY POWER AMPLIFIERS

rate model.

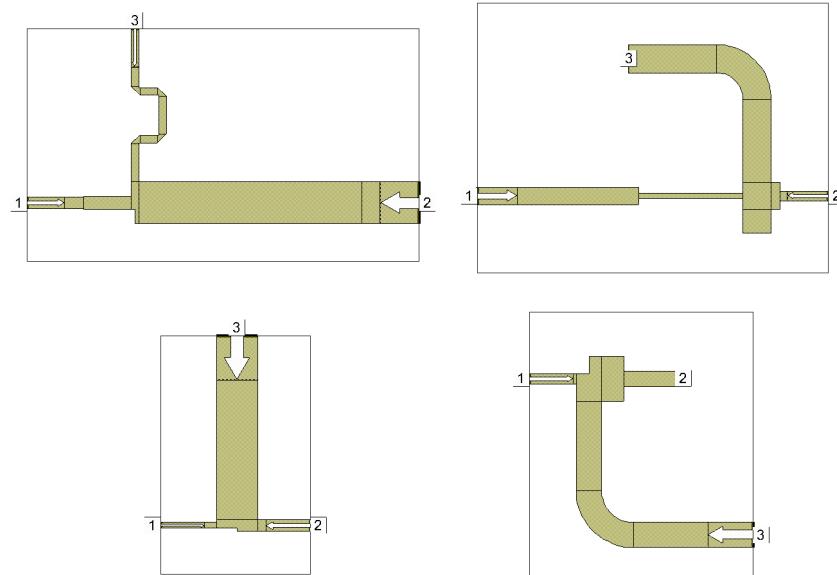


Figure 4.13: Matching networks modelled in Sonnet.

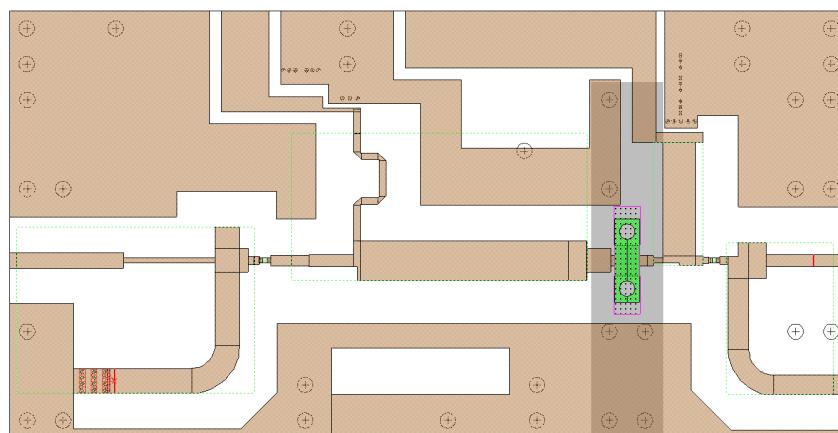


Figure 4.14: Final layout for the amplifier.

4.4.2 Results

The efficiency and output power levels were extremely close to specification especially across the frequency desired for this design. A slight error in the calibration shows the

4.4. A GAN HEMT AMPLIFIER WITH 6 WATTS OUTPUT POWER AND >85% PAE

measured PAE to be slightly higher than that measured at the competition. The simulated output current and voltage waves are shown in the figure below. It appears, due to the voltage peaking that this amplifier is operating in a quasi-F-1 mode. It is likely that there is a portion of class-E operation as well due to the output capacitance within the device and the capacitance added by the packaging. As Steve Cripps mentions in the introduction to his latest book [5] it is difficult to determine the class unless the output current and voltage waves can be directly measured. To compound this, these simulation results are not the intrinsic transistor current and voltage waveforms as they are measured outside the package.

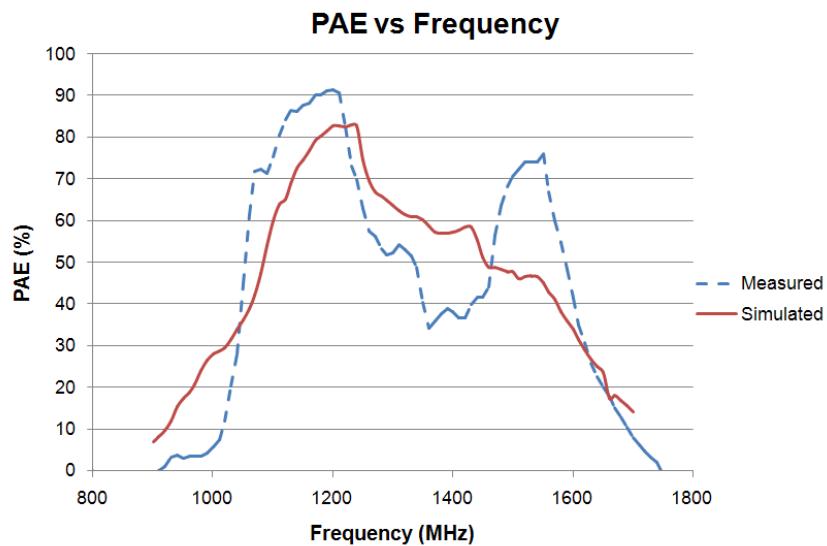


Figure 4.15: PAE vs. Frequency

4.4.3 Discussion

The amplifier is shown in Figure 4.18, it achieves an efficiency of 85%, gain of xx dB.

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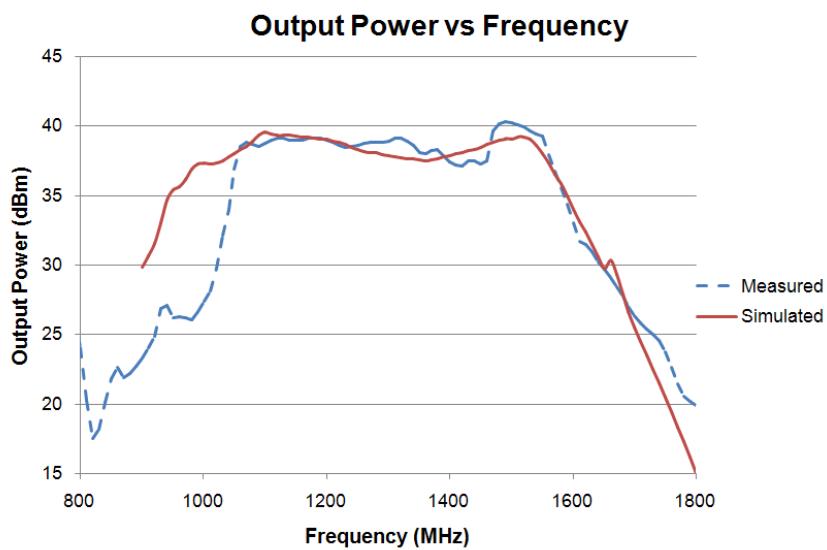


Figure 4.16: Ouptut power vs. frequency.

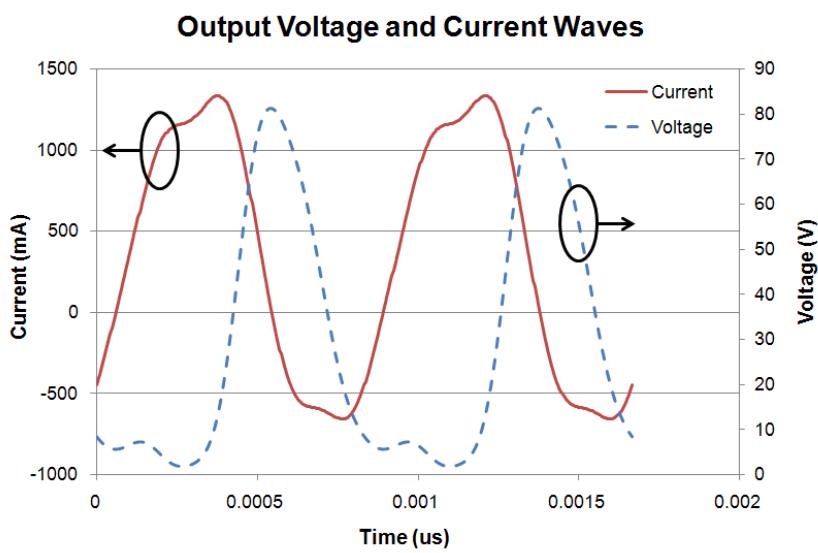


Figure 4.17: Output voltage and current waves.

4.4. A GAN HEMT AMPLIFIER WITH 6 WATTS OUTPUT POWER AND >85% PAE

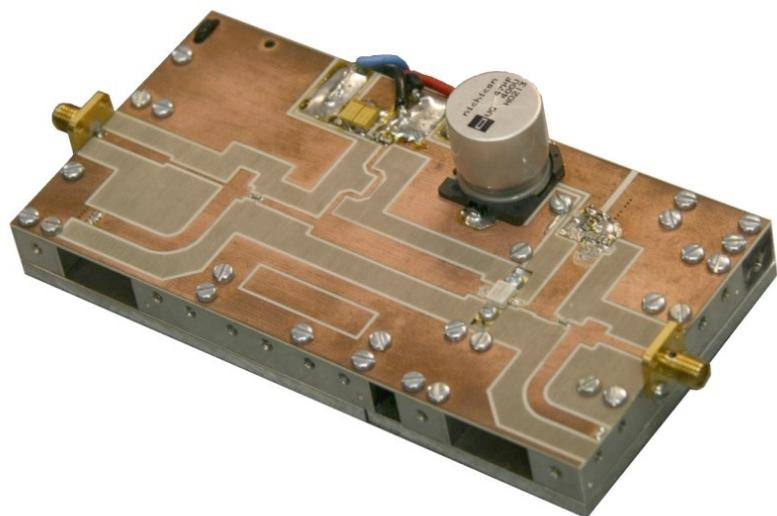


Figure 4.18: Photo of the finished amplifier.

4. HIGH EFFICIENCY POWER AMPLIFIERS

4.5 A 60GHz Transmission Line Power amplifier

This section outlines the design of a power amplifier in 0.18um SiGe using transmission lines.

The power amplifier consists of 5 stages. A cascode input stage provides 8dB of gain. The final 4 stages are common-emitter amplifiers biased in Class A. Inter-stage matching is carried out using transmission lines and capacitors. The large-signal power gain for the power amplifier is 30dB, it has a 3dB bandwidth of 11.5GHz, centered at 58GHz. Each bias stage consists of a quarter wavelength transmission line connected to a current source, fed using a 4-bit current-mode DAC. The nominal DAC value is set for maximum gain and can be programmed to output current down to zero allowing the PA to be switched off if needed. The bias networks are cascaded and loadable via a serial control port.

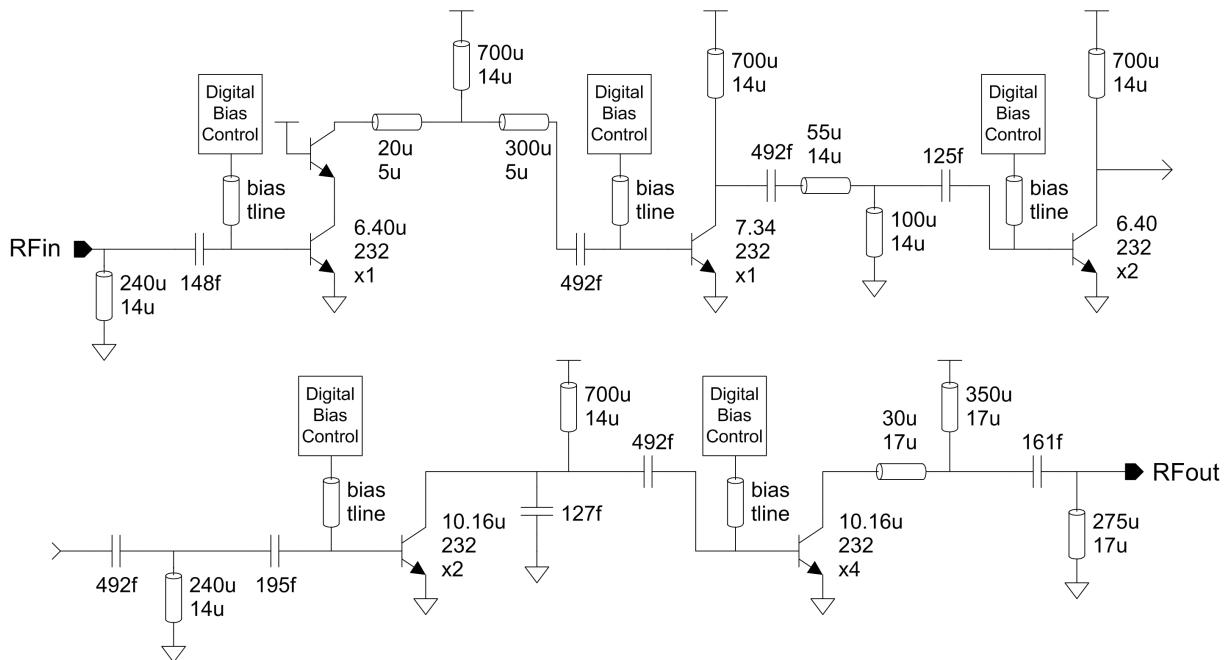


Figure 4.19: Block diagram of the SiGe PA.

The characteristic impedance for the bias lines was chosen to minimise RF loss and provide maximum isolation. Capacitors are used at the end of the bias lines for RF grounding. The transistors in the power amplifier have three base and two emitter fingers. This configuration minimises the transit time of electrons between the emitter and collector while maintaining a large emitter area [72]. Using maximum (10.16m) sized fingers (for this process) in the output stages means that the parasitics in the feed structure can be kept to a minimum (fewer transistors are needed for the same effective emitter length)

Mismatch in a power amplifier contributes to low efficiency, a worsened VSWR, higher die temperature for the same output power and is the cause of many other undesirable effects. It is not valid to match a power amplifier using small signal S-parameters as the input and output characteristics of a HBT change under large-signal conditions. Matching must be done under large signal conditions using a Periodic Steady State (PSS) or Harmonic Balance (HB) simulator.

The problem with PSS and HB simulations is that they are time consuming when compared to an S-parameter analysis. A method was developed to counter this, it allows matching networks to be evaluated and optimised quickly; it is described in the following paragraphs.

For each stage of the design a frequency-domain large signal model of the transistors input impedance with matched output, and output impedance with matched input was created (as the transistors are bilateral in this configuration, mismatch on the output changes the input impedance and vice versa).

The approach is shown in Figure 3. Transistor 1 is to be matched to transistor 2. Circuit

4. HIGH EFFICIENCY POWER AMPLIFIERS

3 is used to model the output impedance of transistor 1. It is generated using an optimisation routine, programmed in visual basic, (within Analog Office) that minimises the mean square error between the real and imaginary components of the large-signal impedance looking into Z_{out} for circuit 1 (Ar) and circuit 2 (Am). The same method is used to model the input of transistor 2 with circuit 4.

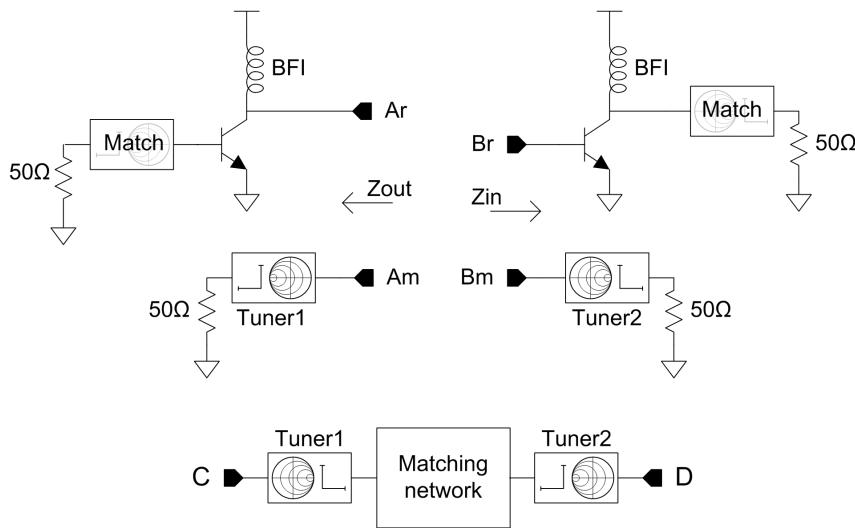


Figure 4.20: Matching high power devices.

By creating these impedance models we can determine the absolute effect of the matching network. To get the best performance out of the power amplifier it is now a process of minimising the loss of the network with a simple simulation instead of undertaking a large-signal analysis of the whole amplifier.

On a stage-by-stage basis we can optimise the inter-stage match and see how it contributes to the overall frequency response of the power amplifier. The matching networks were optimised using a gradient descent method for low loss (maximum gain). Other factors which were considered were tolerance to manufacturing parameters and low frequency stability. The output stage was optimised for maximum power transfer using the load-pull wizard in AWRs Analog Office.

All the transmission lines in the power amplifier are shielded micro-strip type with fixed shield and adjustable width, except for the output stage which employs micro-strip lines. Micro-strip lines are used in the output stage as they provide a lower DC resistance for the same characteristic impedance (a 50ohm micro-strip is 17um wide as opposed to 14um for the shielded type). Attention was focused on the design of each transistors feed network. The two critical aims are reducing resistance in series with the base and reducing the base-to-collector capacitance. The resistance in series with the collector while not as critical, must be made as small as possible as it reduces the voltage available to the transistor. A distributed R+C+CC circuit for each transistor was extracted using Calibre (Mentor Graphics) within the Cadence layout environment.

The power amplifier occupies an area of $0.870 \times 0.930 \text{ mm}^2$.

4.5.1 Layout

4.5.2 Measurements

A summary of the power amplifier performance is shown in Table 4.1 and measurements results follow.

Paramater	Units	Measurement
Gain	dB	25-30
S22	dB	25-30
S11	dB	25-30
Psat	dBm	12-13
p1dB	dBm	8-9
Power	mW	385

Table 4.1: Measured results of GTC2 PA.

4. HIGH EFFICIENCY POWER AMPLIFIERS

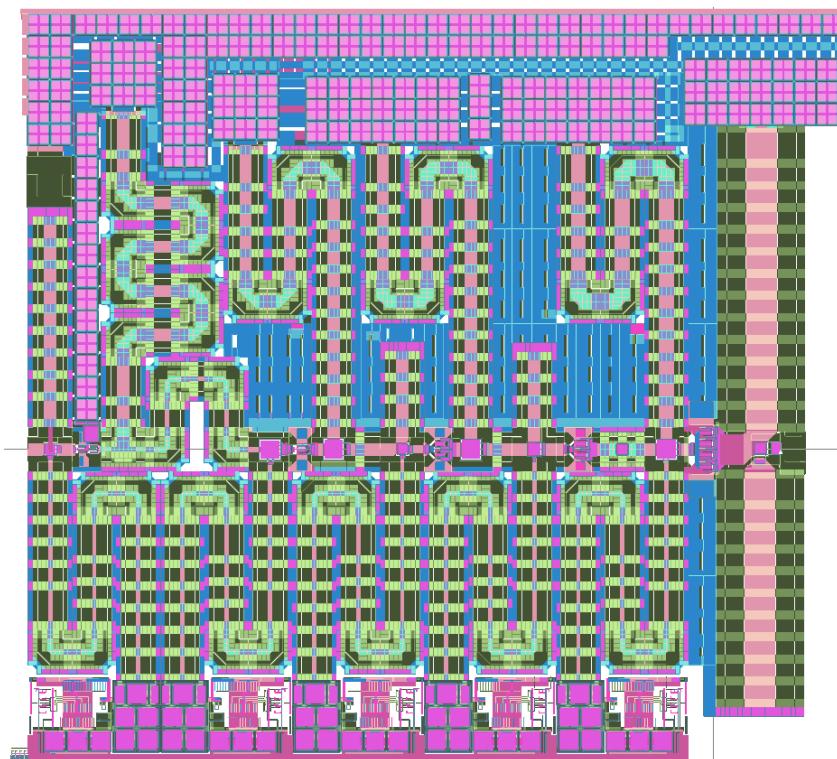


Figure 4.21: Layout of the power amplifier.

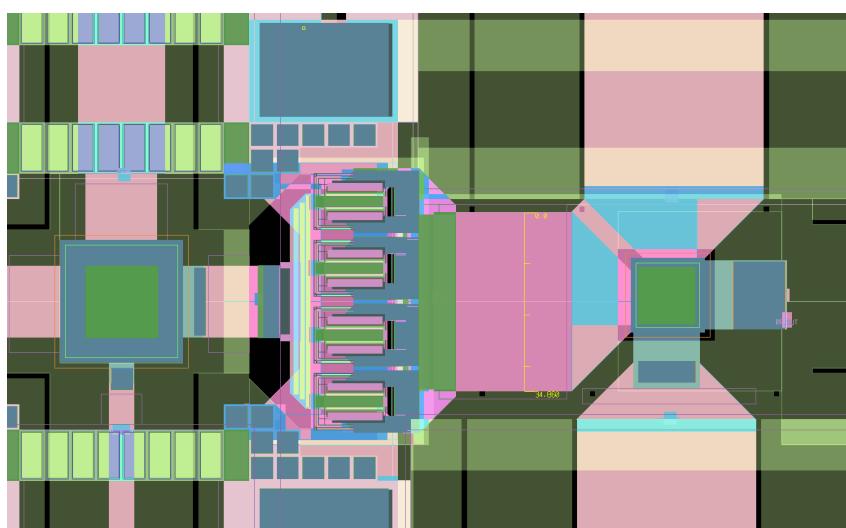


Figure 4.22: Layout of the output stage transistors.

4.5. A 60GHZ TRANSMISSION LINE POWER AMPLIFIER

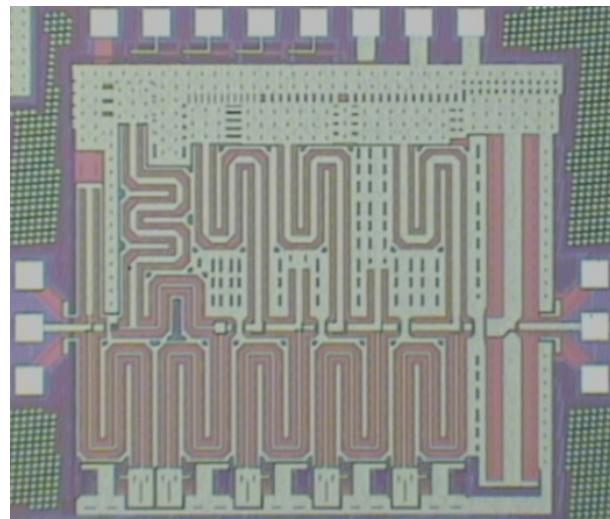


Figure 4.23: Die photo of the implemented power amplifier.

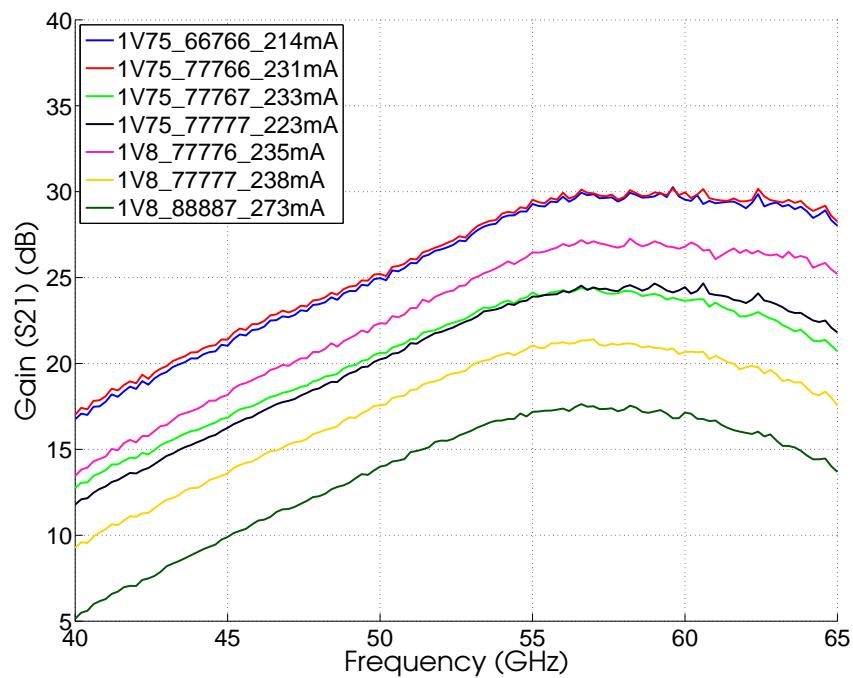


Figure 4.24: GCT2 PA gain plot.

4. HIGH EFFICIENCY POWER AMPLIFIERS

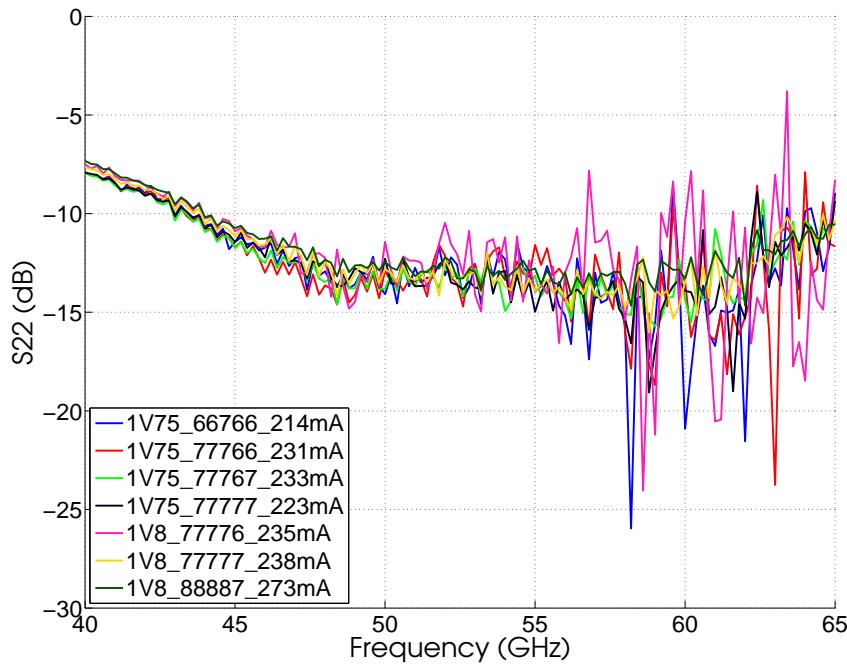


Figure 4.25: GTC2 PA S22 plot.

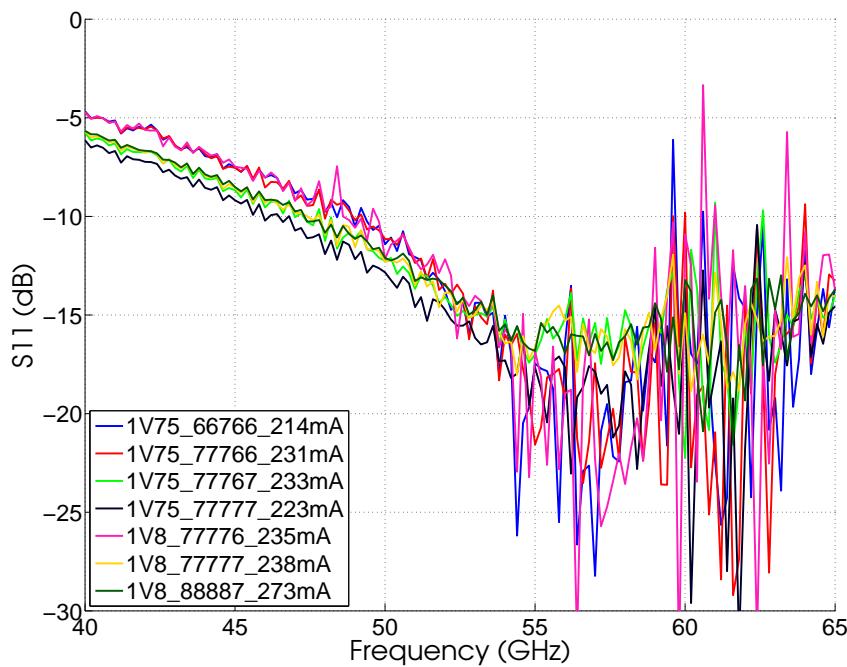


Figure 4.26: GTC2 PA S11 plot.

4.5.3 Discussion

A die micrograph of the PA is shown in Figure 4.23. The PA achieves 25-30dB of gain, output saturation of 12-13dBm a 1dB compression point of 8-9dBm. The PAE at 1dB compression is only 2.1%, at Psat the PAE is 5.2%.

The area for this PA is large, if it was to be integrated in a phased array nearly 1mm^2 would be needed for each PA. In the following two sections, two transformer based designs are shown which achieve higher efficiency and utilize much smaller area.

4.6 A 4-stage transformer based power amplifier in 0.18um SiGe

In the next generation of GLIMMR chips, there was a goal to reduce size and increase efficiency. The power amplifier outlined in this section was used in GTC3 and achieves better performance than the transmission line design, takes up one quarter of the area and uses transformers for inter-stage coupling. A comparison of the two PAs is shown in Figure.

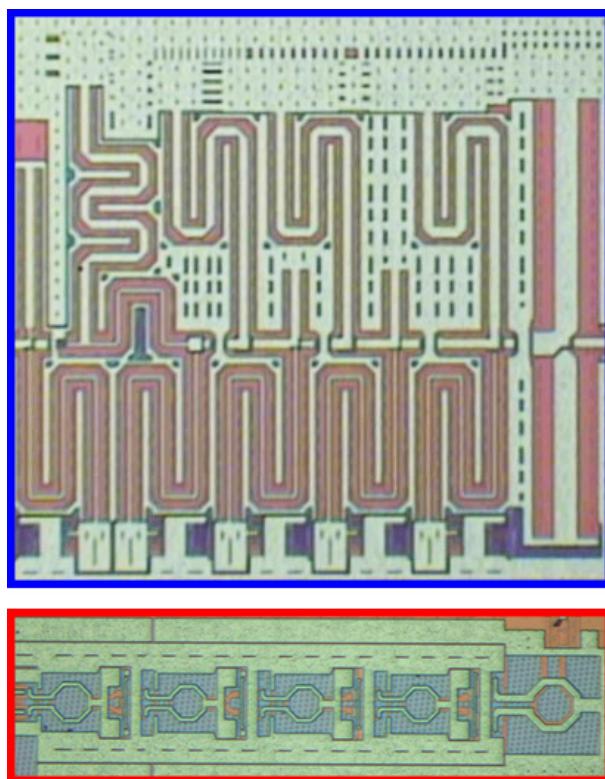


Figure 4.27: Comparison of GTC2 (blue outline) and GTC3 (red outline) power amplifiers/

The power amplifier is a four stage design. The differential architecture is used to improve output power. Bias is provided to transistors through resistors. At the output a balun is used for matching and to convert the differential single into a single-ended

4.6. A 4-STAGE TRANSFORMER BASED POWER AMPLIFIER IN 0.18UM SIGE

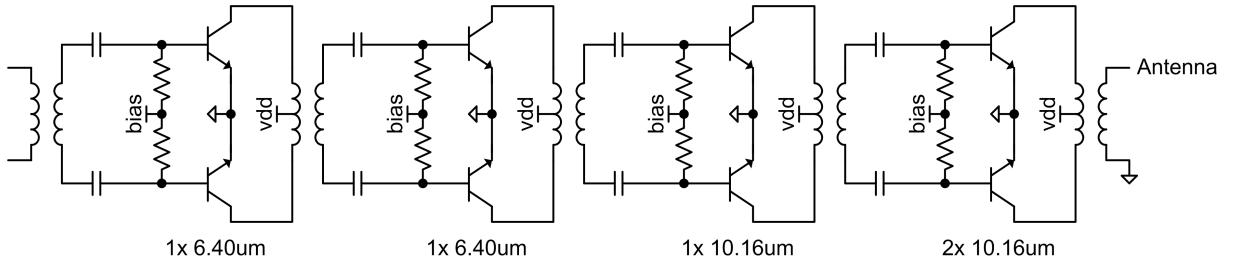


Figure 4.28: Schematic of Power Amplifier

signal.

Interstage matching is provided with single loop transformers and series capacitors. The inclusion of the capacitor in the matching network adds another degree of freedom and the capacitors in this process are high-Q MIM capacitors.

The size of the transistors is scaled in order to improve efficiency, the first two stages use 1x6.40um devices, the third stage uses 1x10.16um devices and the output stage has 2x10.16um devices.

4.6.1 Measurements

A standalone test structure shown in Figure 4.29 is used to test the power amplifier. The test-structure is matched to 50Ω at the output. The input is matched to the output of the IF amplifier. To enable simple testing a single-ended to differential balun is used.

The output of the PA is well matched, it achieves better than -10dB across the 802.11ad band (57-64GHz). The gain of the PA is better than 25dB across the same band. S22 and S21 measurements can be seen in Figures 4.31 and 4.30.

4. HIGH EFFICIENCY POWER AMPLIFIERS

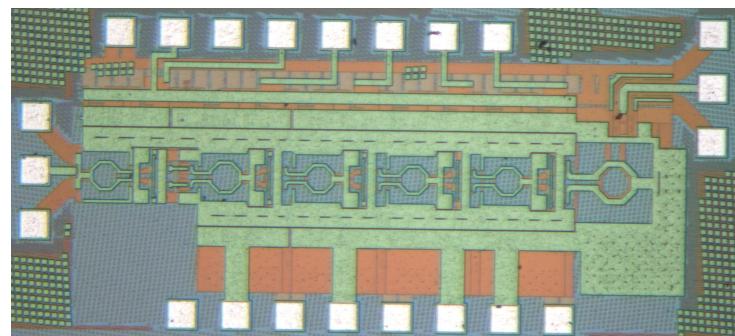


Figure 4.29: Standalone PA for Testing

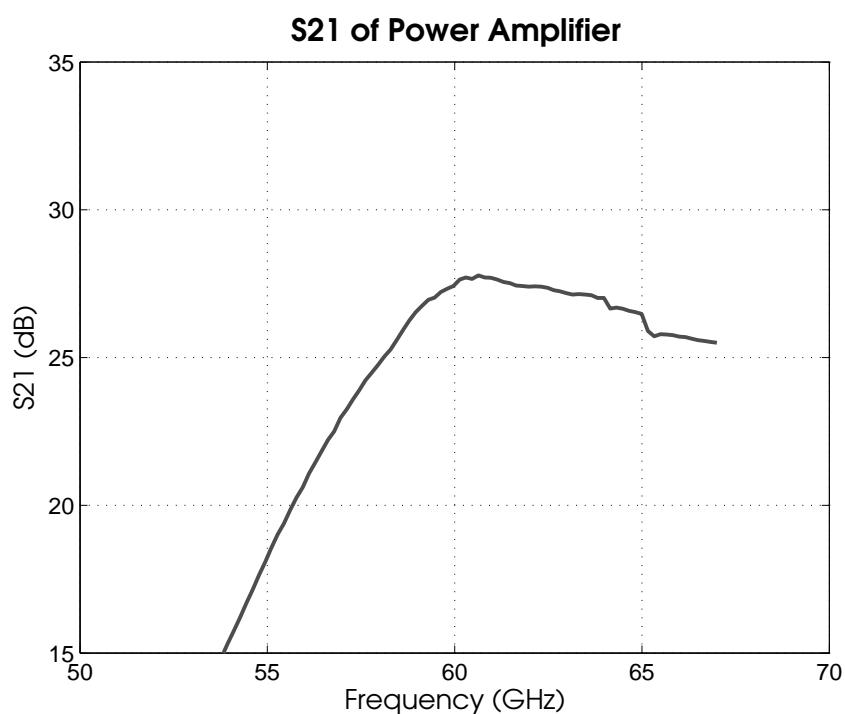


Figure 4.30: Gain of Power Amplifier

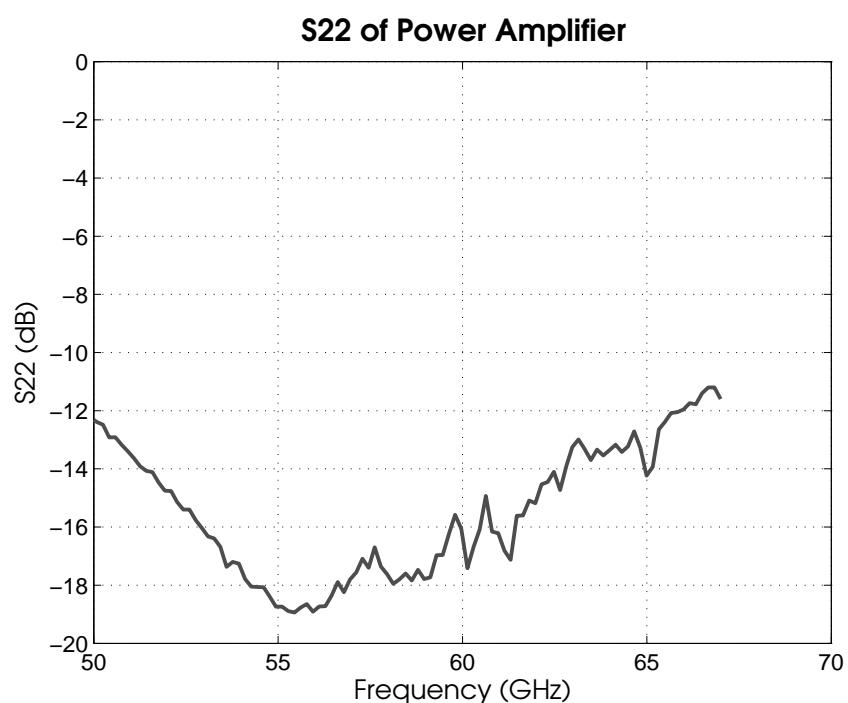


Figure 4.31: S_{22} of Power Amplifier

4.7 A high efficiency 3-stage transformer coupled power amplifier in 65nm digital CMOS

4.7.1 Introduction

Over the last decade interest in the 7GHz of unlicensed spectrum centered at 60GHz has grown extremely rapidly. The proliferation of wireless enabled devices, a continual trend towards higher data rates and the congestion occurring in popular unlicensed bands (such as 2.4 and 5GHz) has fuelled this interest. Applications for 60GHz systems include uncompressed video streaming, wireless personal area networks as well as low energy per bit communication links. The power amplifier is a critical component in any communication system and typically consumes a large percentage of transmitter power. In millimetre-wave systems, a phased array can be employed to spatially combine the power from multiple antennas and increase the antenna gain. In such a system, achieving high gain and efficiency in the amplifier is crucial as it may be implemented 16 or more times depending on the number of antennas the solution requires. Published 60GHz amplifiers typically fall into three different categories; transmission line based [77, 78, 79], lumped element based [80, 81] and transformer based [82, 83]. Transmission line amplifiers use typical MMIC design strategies and benefit from a well defined current return path. This aids accuracy; the tradeoff is the large area which these designs generally require. Lumped element and transformer based designs facilitate smaller layouts with the requirement of better modelling and design methodology to get close agreement between simulated and measured performance. In the case of differential designs, transformers are preferred as they allow a

much simpler layout. With a large number of antennas in a phased array, the output 1dB compression point for each individual amplifier can be relaxed. In this type of system, the most important parameters to consider are power added efficiency (PAE) and the gain provided by each stage. High PAE is desired in order to decrease the system power consumption. Gain is required to amplify the low power output from the up-conversion mixer. Having a high gain per stage reduces the number of stages needed in the amplifier. This chapter outlines a high efficiency 3-stage transformer coupled amplifiers fabricated in digital CMOS.

4.7.2 Methodology and implementation

The most important aspect of millimetre-wave design is a structured design flow and a methodology that enables repeatable, first-pass correct design success. At the heart of the design flow is accurate transistor and passive models along with an accurate parasitic extraction engine. The amplifier presented in this paper was designed using the BSIM4 transistor model with RF enhancements based on [84]. Passive devices were simulated in HFSS and mapped to a custom wide-band equivalent circuit model using Microwave Office and Matlab. Post-layout parasitic extraction was done to capture interconnect and via parasitics. As the interconnect is very small compared to the wavelength at 60GHz this lumped approach can be used.

4.7.3 Amplifier topology

A differential transformer based topology was chosen for a number of reasons. Compared to the transmission line approach, it saves a lot of area. Compared to the lumped

4. HIGH EFFICIENCY POWER AMPLIFIERS

element approach, it makes for a much easier and compact layout. The schematic is shown in Fig 1. In general differential circuits are preferred over single-ended circuits as they possess greater immunity to common mode noise and have a well defined virtual ground which simplifies modeling. In a power amplifier a differential topology splits the output between two transistors. If a single-ended output is desired, this power can efficiently be combined using a BALUN like in this design.

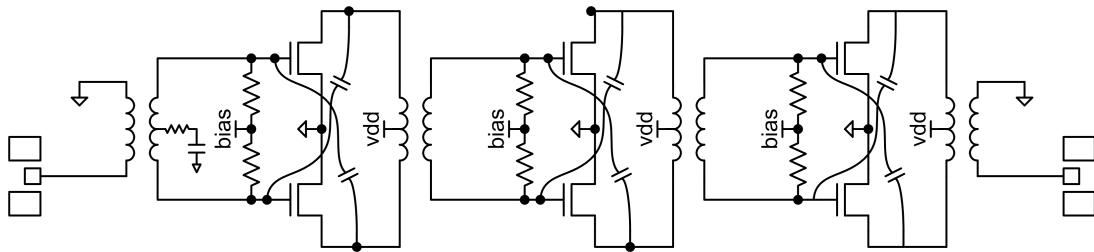


Figure 4.32: Block diagram of the transformer-coupled CMOS PA.

4.7.4 Transistor size and layout

Sizing the transistors for a millimetre-wave amplifier is a tradeoff between power handling capability and fmax. Below a certain width, the layout parasitics associated with the routing dominate; at larger widths the gate resistance is dominant. Simulation including the parasitic components leads to an optimal gate width of 1um. Transistors are placed using custom P-Cells which include routing up to the highest metal. The P-Cell is designed to reduce the gate resistance and inductance, reduce CGD and resistance between the channel and tie-downs. A 20x1um finger NMOS placed in an island surrounded by substrate contacts has been used as the unit cell in this amplifier. Transistors are sized 2 x 20 x 1um, 3 x 20 x 1um, 4 x 20 x 1um for the first, second and final stages.

4.7.5 Transformer design

Transformers are used throughout the amplifier. At the input and output they provide a single-ended to differential transformation. At the input stage the secondary turns (connected to the transistor gates) centre-tap is decoupled to ground through an RC filter to reduce the possibility of common-mode oscillation. Between the stages, the transformers are used as matching networks, to provide VDD to the drains and couple the signal from the output of the previous stage to the input of the next. The transformers are modelled using HFSS. Parameterised multi-port s-parameters are extracted for several loop widths, radius and overlaps. These s-parameters are input into a custom software module that creates equivalent circuit models for Cadence, ADS and AWR MWO. No substrate shielding techniques are used however a multi-metal ground ring is implemented around each transformer. This ground ring ensures that any metal outside the transformer perimeter does not affect the performance; it also allows ground to be distributed through the circuit with low impedance. The Gmax for the transformer is extremely low, -0.5dB at 60GHz. The transformers are implemented using the top 2 copper layers (0.9um thick).

4.7.6 Neutralization

Common-source amplifiers at millimetre-wave frequencies often suffer from gain degradation due to drain-gate capacitive feedback. This capacitance across a voltage gain node is magnified by the gain of the stage. In addition, this capacitance can de-stabilize the amplifier. At lower frequencies a cascode topology is often employed to reduce the effect of the miller capacitance. At millimetre-wave frequencies, the capacitance asso-

4. HIGH EFFICIENCY POWER AMPLIFIERS

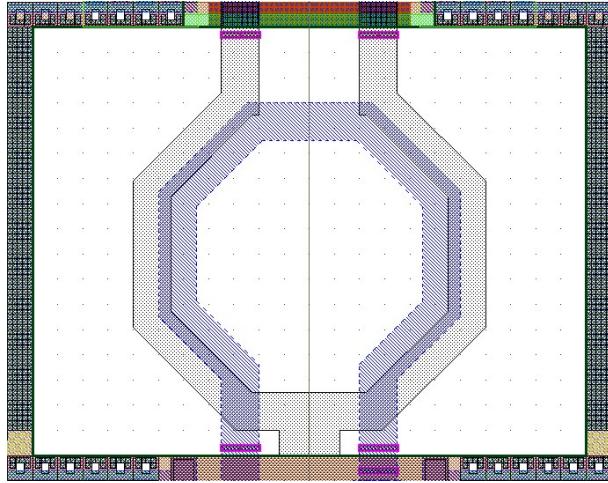


Figure 4.33: Transformer design.

ciated with the drain and source nodes often creates a pole which needs to be removed with a series inductance. This inductance adds area and in a amplifier with limited headroom the cascode topology is not practical. Neutralization is a technique that aims to negate or reduce the effects of the drain-gate capacitance. It has been demonstrated recently at 60GHz in [82]. It is easily achievable in a differential amplifier as out of degree phase signals are available. The neutralization is accomplished by feeding back some of the output of the positive stage to the input of the negative stage and vice versa. The feedback is implemented using a metal plate capacitor and varies depending on the stage from 15-30fF. The neutralization is only useful across a narrow frequency range. To ensure stability at low frequencies where the transistors have a large amount of gain, high pass elements such as transformers or series capacitors need to be used. At high frequencies the quickly rolling off frequency response of the amplifier aids stability. Compared to other stabilization techniques such as series RC networks the neutralization technique does not degrade the performance of the amplifier.

4.7. A HIGH EFFICIENCY 3-STAGE TRANSFORMER COUPLED POWER AMPLIFIER IN 65NM DIGITAL CMOS

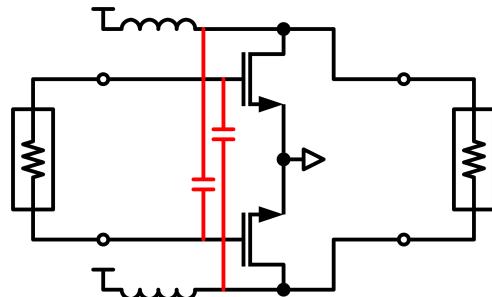


Figure 4.34: Differential devices with neutralization capacitors shown in red.

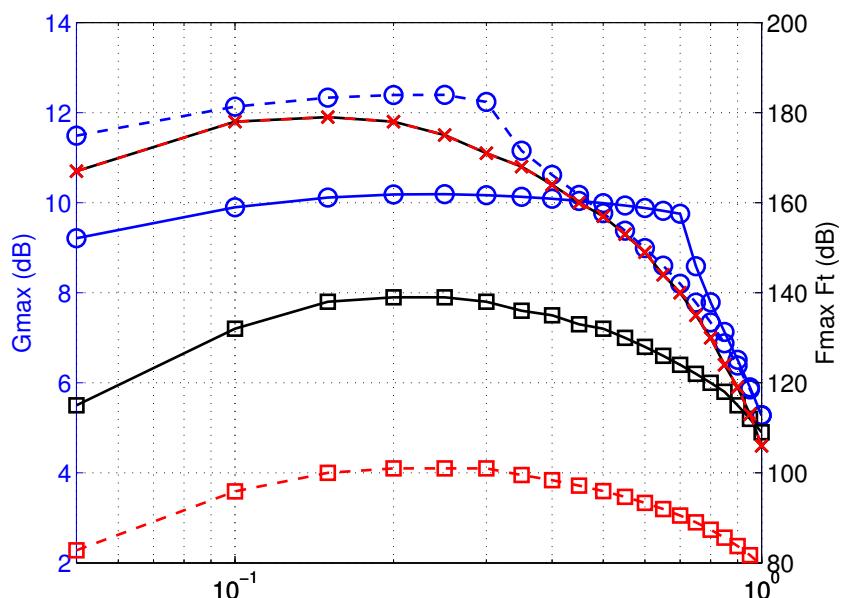


Figure 4.35: The G_{max} of a differential transistor is 2.5dB higher than without.

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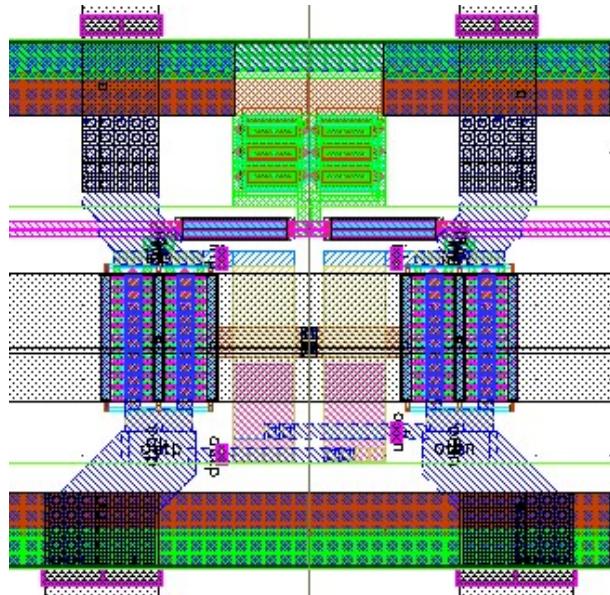


Figure 4.36: Transistor layout showing neutralization capacitors.

4.7.7 Layout

The core of the amplifier (not including input balun which is only for testing) takes an area of 350um x 150um. The compact layout is due to the use of transformers through-out the design. Apart from the reduced cost, the small size also keeps routing between the transistors to a minimum improving performance and reducing the need for additional modelling steps.

4.7.8 Measurement Results

The amplifier presented in this paper achieves a peak efficiency of 18% and a saturated output power of 10.5dBm (both limited by measurement). The gain is greater than 30dB from 61 to 65 GHz demonstrating the highest achieved gain per stage for any CMOS amplifier. The PAE at 1dB compression and 61GHz is 7.7% Figure 5 shows

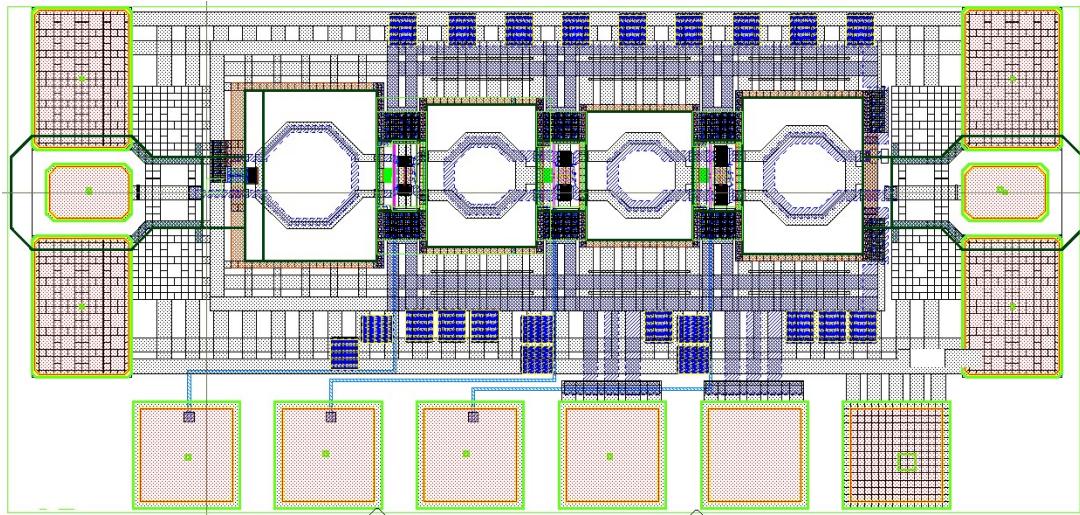


Figure 4.37: Layout.

the s_{21} and s_{22} of the amplifier across frequency for different temperature settings. The gates are biased with a constant voltage across temperature. With a temperature dependent bias network, the gain will be more constant across temperature. Figure 6 shows the output 1dB compression point of the amplifier across frequency and temperature.

4.7.9 Comparison

Table 4.2 below compares the amplifier presented in this chapter to other state of the art amplifiers published at the same time. It achieves the highest efficiency at p1dB.

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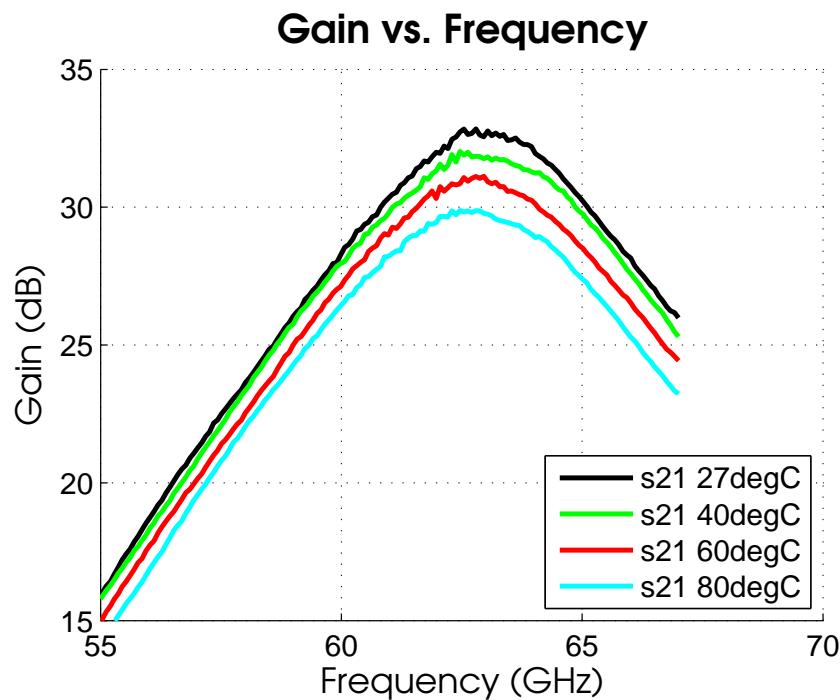


Figure 4.38: Gain (S_{21}) vs. frequency.

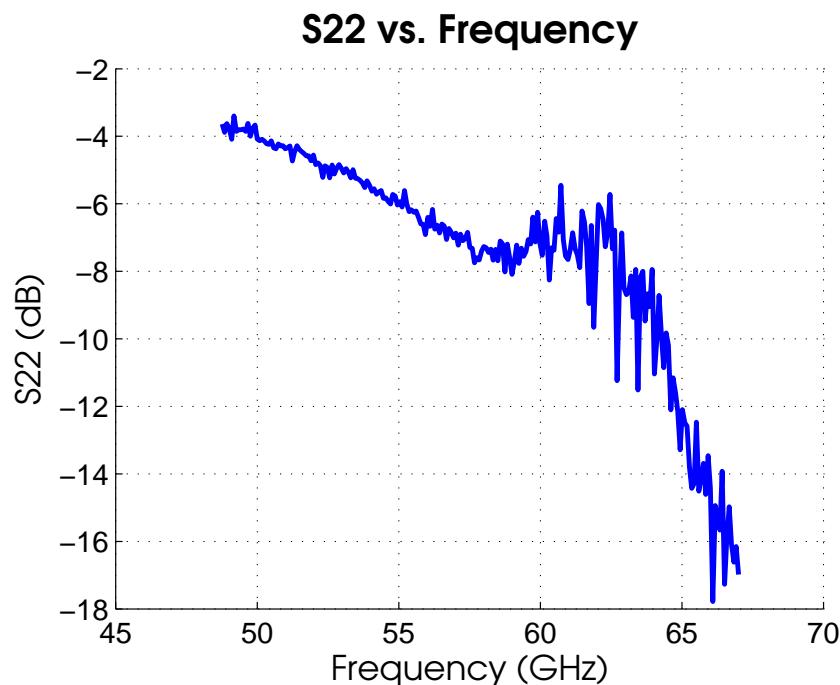


Figure 4.39: S_{22} vs. frequency.

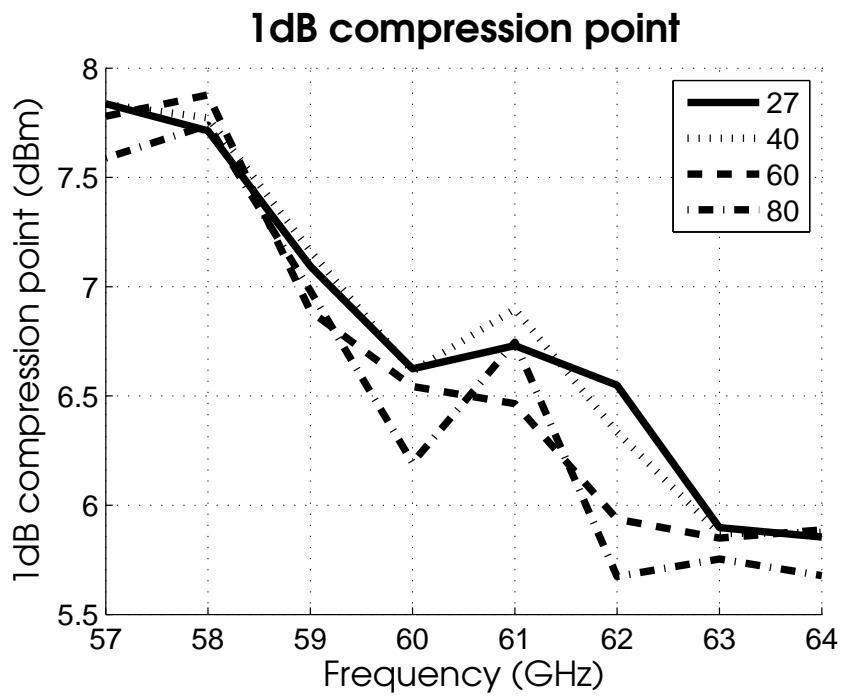


Figure 4.40: Output 1dB compression point.

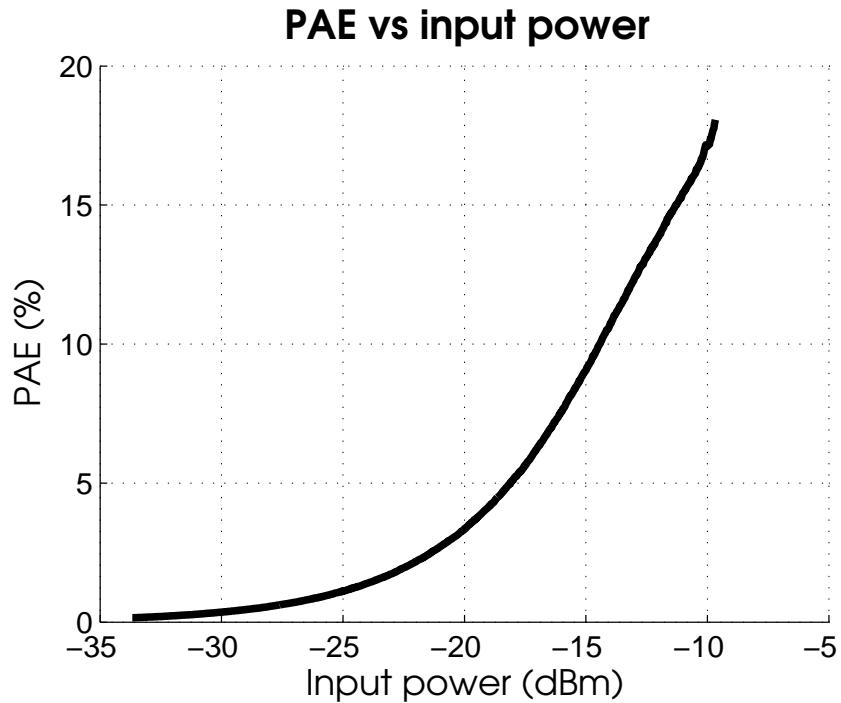


Figure 4.41: PAE vs. input power.

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Ref	Year	Process	Stages	Topology	Pg	p1dB	Psat	Vdd	Pdc	PAE
[81]	2006	90nm	3	L/C	5.2	6.4	9.3	1.5	39.75	6.05
[83]	2008	90nm	2	xfmr	7.7	9.0	12.3	1	88	7.09
[78]	2008	90nm	4	tline	8.3	8.2	10.6	1.2	220	2.7
[79]	2008	90nm	3	tline	14.3	10.0	11.0	1.0	150	6.35
[77]	2008	90nm	3	tline	17	5.1	8.4	1.5	54	5.8
[82]	2009	65nm	3	xfmr	15.8	2.5	11.5	1	43.5	4.0
[80]	2009	45nm	3	L/C	19	7.9	1.2		6.4	
[69]	2010	65nm	3	xfmr	30	6.8	10.6	1	65	7.7

Table 4.2: Comparison of CMOS power amplifiers, this work is shown in red.

5

Architectures for Mm-wave Systems

5.1 Introduction

This chapter outlines two transmitters designed for the GLIMMR project.

The first transmitter (GTC2-Tx) is a single-chip super-heterodyne transmitter. This architecture is good for a simple implementation inside a mobile phone or small handheld device. It has only one transmit and one receive port and is not capable of beam-forming and is suited for close (within 1-2m) applications such as docking or desktop bus. This architecture is shown in Figure 5.1. The RF chip is shown on the bottom right, it takes an analog I/Q signal as input and generates a 60 GHz output to drive an antenna. The author was responsible for the transmitter design and the TX module

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

design (excluding the antennas).

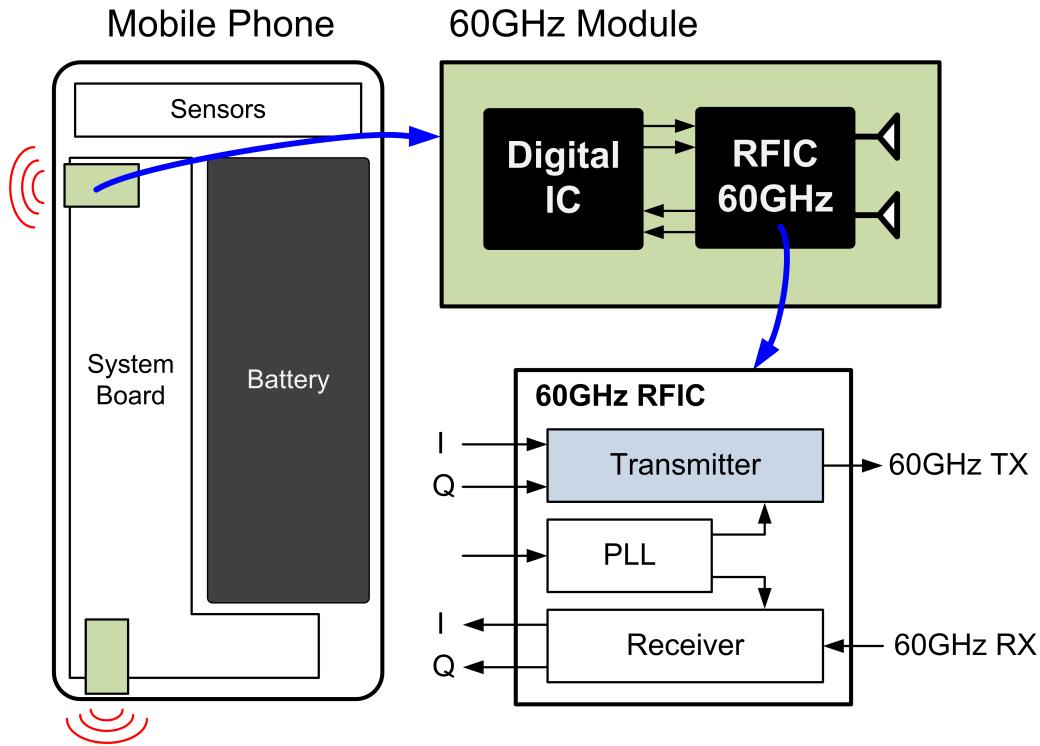


Figure 5.1: A single chip implementation for 60 GHz and application to mobile phones.

The second transmitter (GTC3-Tx) is a novel split-IF architecture which is split at a 9GHz IF frequency and enables the baseband chip to be placed away from the RF front-end chip. The RF front-end is built in a modular fashion to enable several to be integrated into a phased array. The architecture enables extremely high element count phased arrays due to the distributed nature. The author was responsible for the transmitter and the high level architecture was a joint invention with Leonard Hall. This architecture is well suited for implementation inside a laptop or high powered router. and is shown in Figure 5.2.

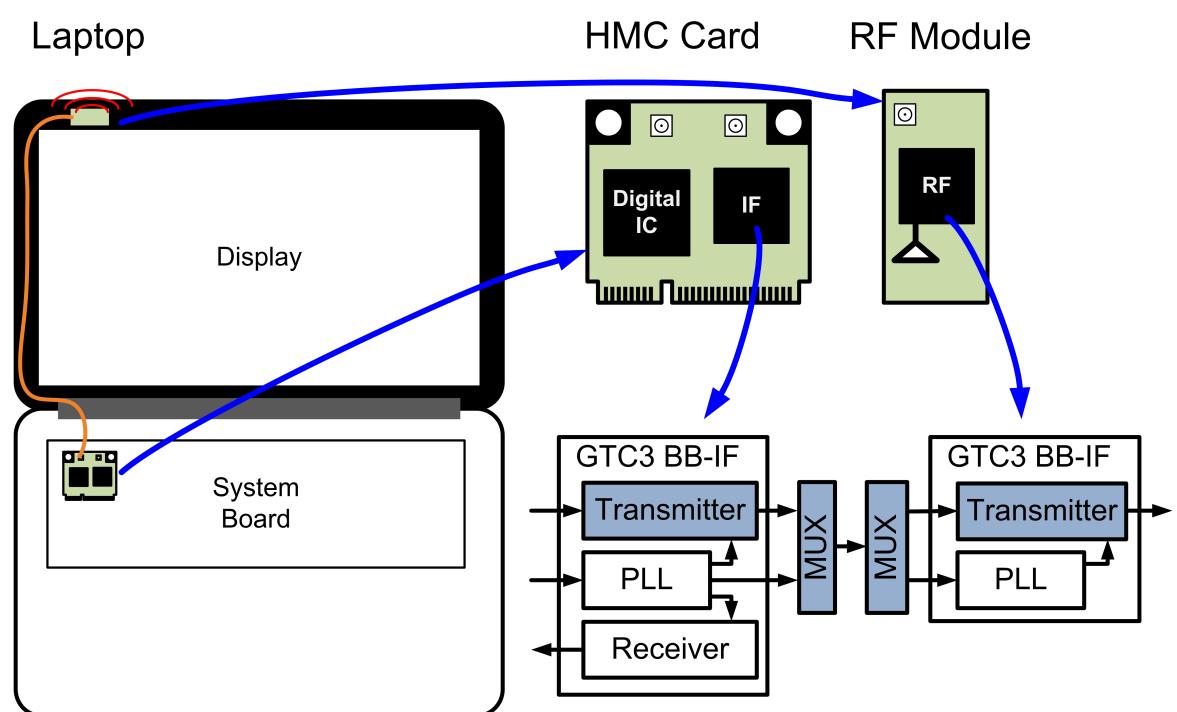


Figure 5.2: A two chip implementation for 60 GHz and application in laptops.

5.2 GTC2-Tx: A 60 GHz +12dBm single-chip transmitter

5.2.1 Introduction

This chapter presents a simple super-heterodyne 60 GHz transmitter designed for the GLIMMR project (GTC2). The transmitter is implemented using Jazz Semiconductors SBC18hx1 SiGe process [85]. This process has 6 metallization layers, MIM capacitors and planar inductors. An overview of the transmitter design strategy and simulation results is given in [29] and outlined below.

A high level block diagram of the 60 GHz GLIMMR transceiver is shown in Figure 5.3 with the authors contributions highlighted in blue.

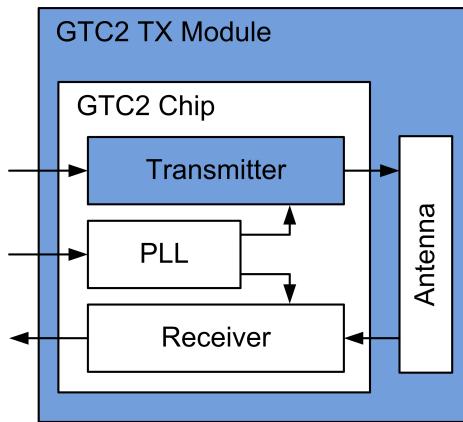


Figure 5.3: Simple diagram of GTC2 showing the areas covered in this section.

Link Calculation

This system is designed for short-range 1-to-1 operation or medium range 1-to-N operation.

5.2. GTC2-TX: A 60 GHZ +12DBM SINGLE-CHIP TRANSMITTER

Assuming a goal of 1 Gpbs, transmit power of 9dBm (at p1dB point), losses to antenna of 2dB and 5dBi antenna gain the EIRP is 12dBm.

For a 1-to-1 implementation, 2Gbps can be achieved at just over 2 meters in an AWGN channel.

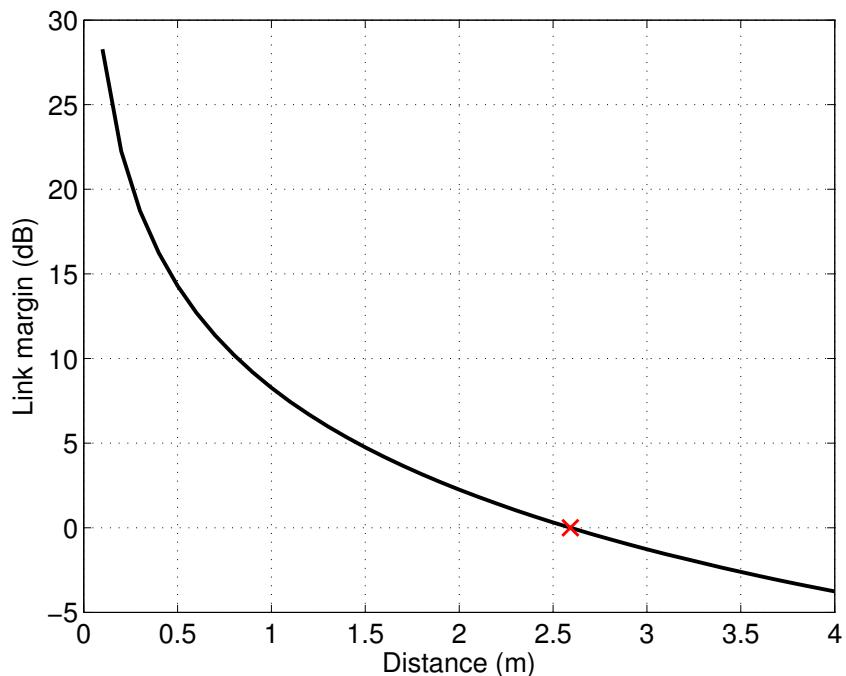


Figure 5.4: AWGN link margin in dB versus distance for 1x1 QPSK 2Gbps link. TX EIRP 12dBm, antenna gain 3dBi each side, RX NF of 10dB, SNR requirement of 10dB.

Specifications

The transmitter specifications are shown in Table 5.1.

Specification	Units	Value
Psat	dBm	>12
P1dB	dBm	>10
Max Gain Variation (2 GHz channel)	dB	2

Table 5.1: System requirements for GTC2 Tx

5.2.2 Architecture

A super-heterodyne architecture is used for the transmitter, this offers some advantages over a direct-conversion system. For one, the generation and distribution of the LO signal is simplified. In this system, a 24GHz VCO is phase locked to an external 180MHz reference. The IQ mixer operates with an LO of 12 GHz which is obtained via a 24-12 GHz quadrature divider. The 48GHz LO for the second mixer is generated by a frequency doubler. The moving IF architecture simplifies the design of the frequency synthesizer and the high IF frequency reduces the need for image filtering as it is well out of the bandwidth of the transmitter (48GHz). A block diagram of the transmitter is shown in Figure 5.5.

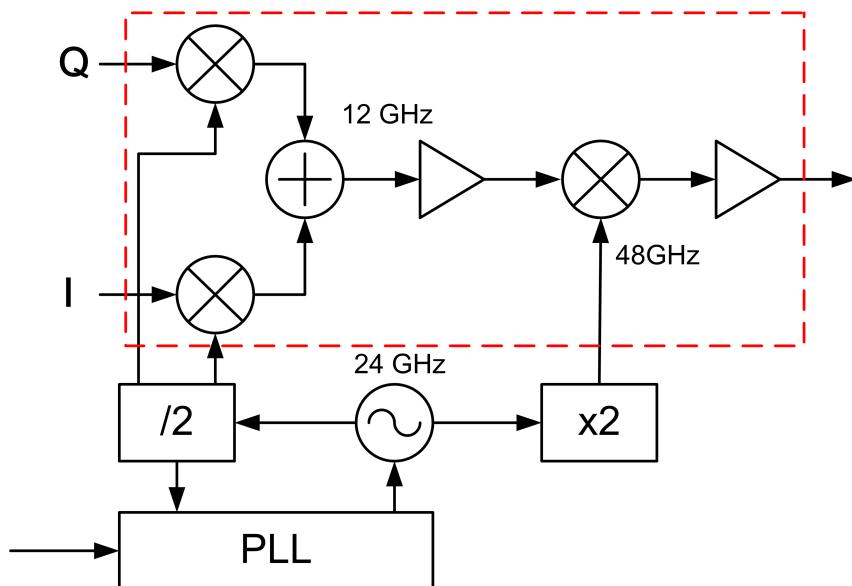


Figure 5.5: GTC2 block diagram.

5.2.3 Circuit design

5.2.3.1 Power amplifier

The power amplifier design is covered in more detail in section xx. It consists of 5 stages. A cascode input stage provides 8dB of gain. The final 4 stages are common-emitter amplifiers biased in Class A. Inter-stage matching is carried out using transmission lines and capacitors. The large-signal power gain for the power amplifier is 30dB, it has a 3dB bandwidth of 11.5GHz, centred at 58GHz. Each bias stage consists of a quarter wavelength transmission line connected to a current source, fed using a 4-bit current-mode DAC. The nominal DAC value is set for maximum gain and can be programmed to output current down to zero allowing the PA to be switched off if needed. The bias networks are cascaded and loadable via a serial control port.

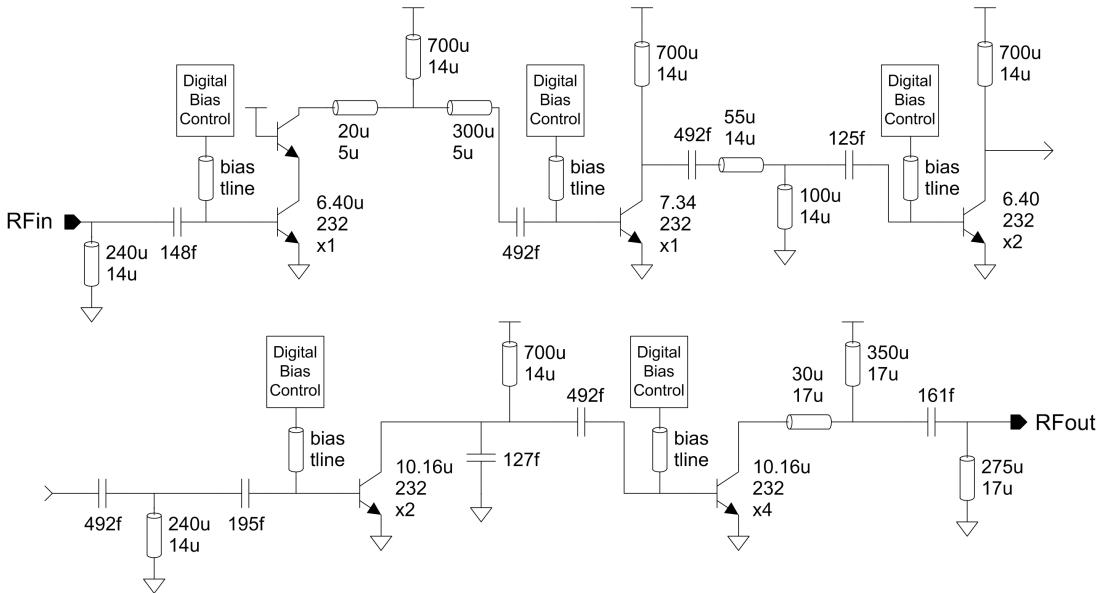


Figure 5.6: Block diagram of the SiGe PA

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5.2.3.2 Baseband to IF Mixer

The first up-conversion stage employs an image-reject Gilbert cell mixer. To achieve infinite image-rejection the phase of the baseband (BB) I and Q signals must be perfectly quadrature and equal in amplitude. The LO must also have a 90 phase shift. Due to the tolerance and mismatch inherent in the manufacturing process this is not achievable. To maintain 25dB of image-rejection the phase error must be less than 5 and the amplitude error must be less than 5% [86]. The switching transistors are bi-ased for maximum ft. This results in a current density of approximately 1mA/micron of emitter length. At this current density the transconductance stage would be twice the size of the switches in order to have the same ft. However, they are sized 4x larger, this gives a lower noise figure and reduced gain which is optimal for the maximum 2 GHz input frequency. With sufficient LO drive the switching transistors act as ideal switches and do not contribute to the non-linearity of the circuit [87], the transconductance stage is the main non-linear element. To increase the linearity and reduce the gain, emitter degeneration resistors are used. The transconductance stage is dc coupled to the input transmission lines. This allows the use of high value (1uF) off-chip capacitors for the BB signal which are not achievable on-chip. The input match is obtained using 100 ohm resistors between the differential signal paths. Inductors are used at the output. This keeps the voltage across transistors at an effective level, allows the output to be tuned to the 12 GHz IF frequency and matched to the following stage. As this design employs a moving IF, the low Q of the on-chip inductors is not a problem and allows a broadband match to be achieved. The inductors were chosen to resonate well away from their self resonant frequency (i.e. approximately 1/3 fsrf).

5.2. GTC2-TX: A 60 GHZ +12DBM SINGLE-CHIP TRANSMITTER

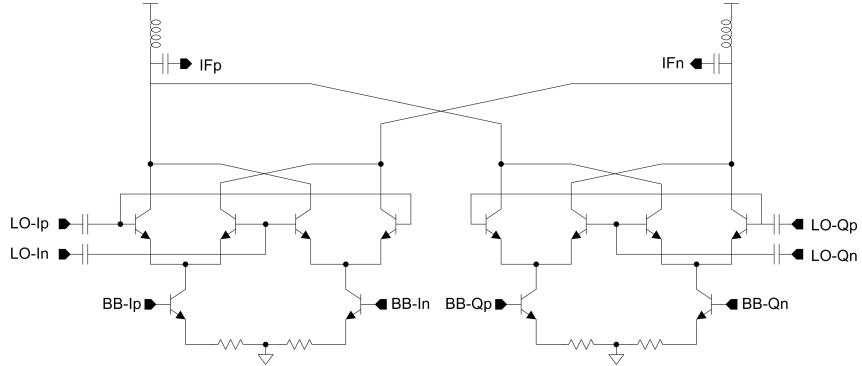


Figure 5.7: Block diagram of SiGe mixer

5.2.3.3 RF Mixer

The second up-conversion mixer is a Gilbert Cell with tuned input and output. The input is matched to the complex conjugate of the output of the previous mixer. The output is tuned to 50 ohms using a transmission line and capacitor as the passive balun that follows this mixer was designed with 50 ohm single-ended ports. The image for this mixer is centred around 36 GHz. The tuned output stage attenuates this signal. In the future a notch filter at 36 GHz will be employed to reduce this image further.

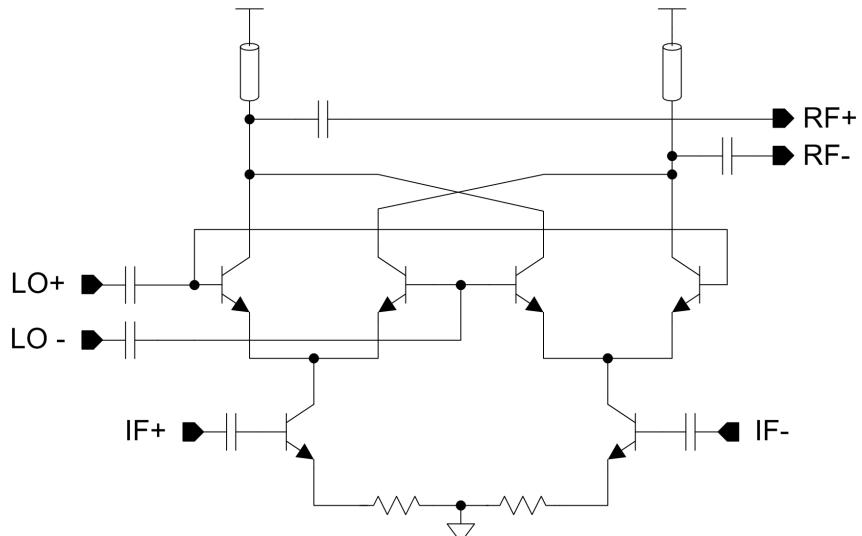


Figure 5.8: Block diagram of SiGe mixer

5.2.4 Layout

The layout of the transmitter is shown in Figure 5.9. The pins are taken to one edge as the design was located on a multi-project wafer (MPW) and was not able to be sub-diced.

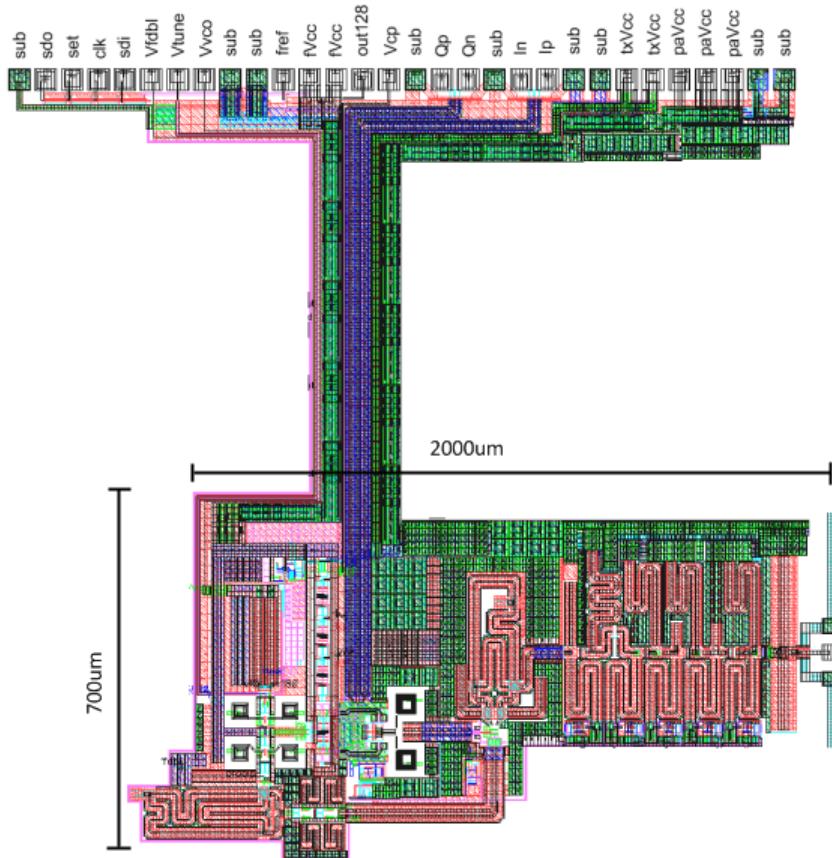


Figure 5.9: Layout of GTC2 transmitters

5.2.5 Development Boards

Boards designed to test the transmitter are shown below. A bond-wire antenna (Weste and Hall) [88] was used at the output of the transmitter. The test setup consists of a

5.2. GTC2-TX: A 60 GHZ +12DBM SINGLE-CHIP TRANSMITTER

master board which contains control logic (small micro-processor), voltage regulation, power supply conditioning and some baseband attenuation. The daughter boards we implemented on Rogers 4003 substrate and contain the chip, some decoupling capacitors and the bond-wire antennas. The chip is mounted in a cavity and bondwires are used to connect to the PCB.

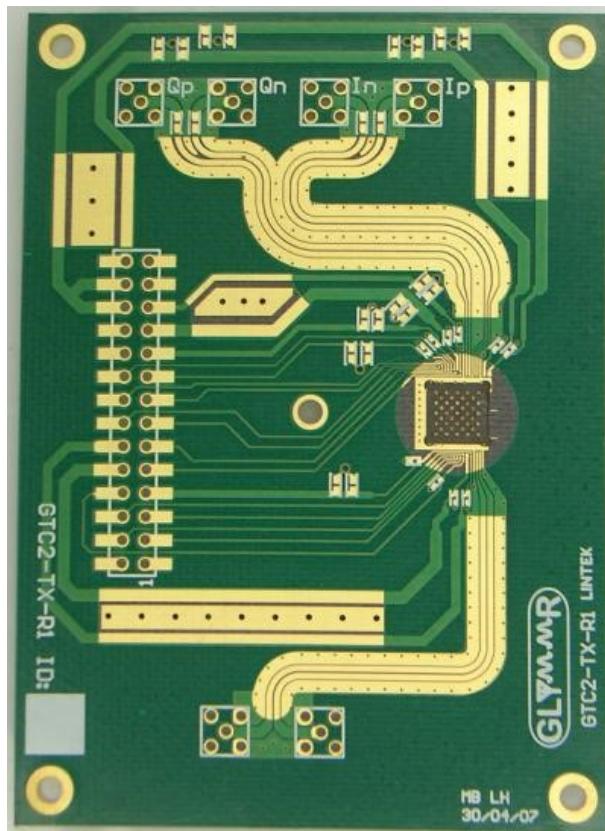


Figure 5.10: RF daughter board for TX testing.

5.2.6 Wire-bonding

This chip uses wirebonding to connect to the chip. Wire-bonding is feasible at 60 GHz however WLCSP packaging is preferred if available.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

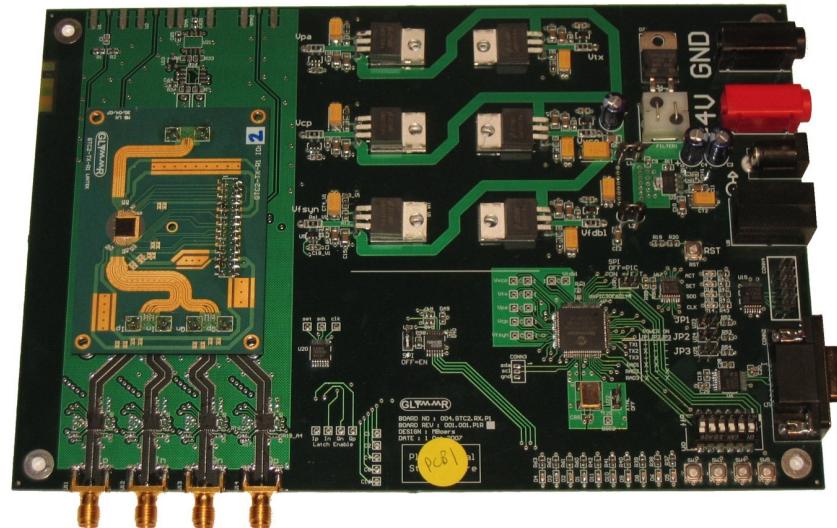


Figure 5.11: Development boards designed for testing the transmitter

5.2.7 Measurement Results

The transmitters measured performance matched the simulated results closely. The output was tuned to the 60 GHz band (57-64GHz) and provided close to 30dB gain across this range.

5.2.8 Outcomes

The architecture presented here would be amenable to integration in a single chip 60 GHz system.

Difficulties associated with integration of this architecture Requirement for more antennas Bondwire vs. patch antennas

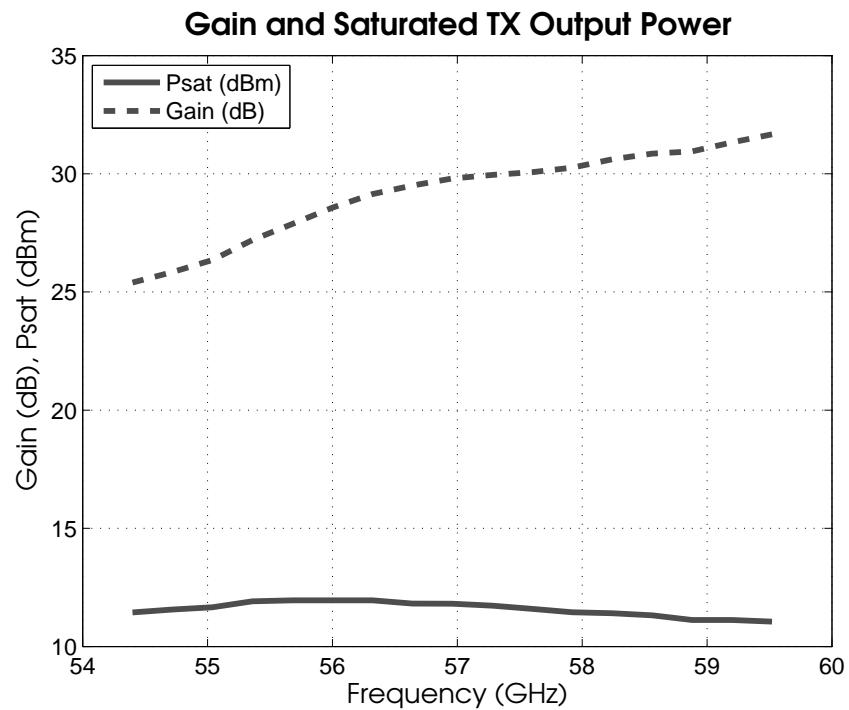


Figure 5.12: Gain and Saturated Output Power

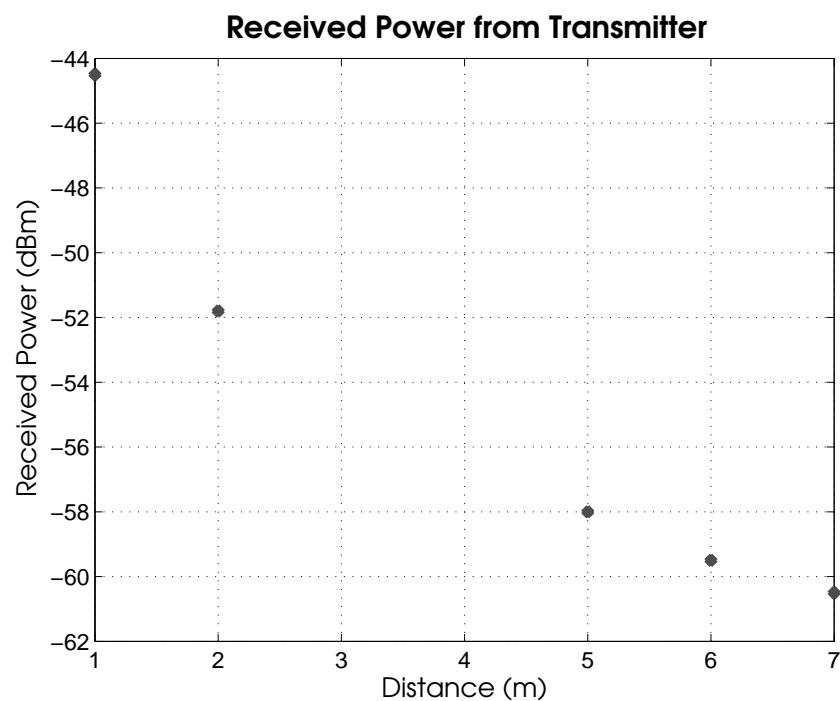


Figure 5.13: Received power from the transmitter

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

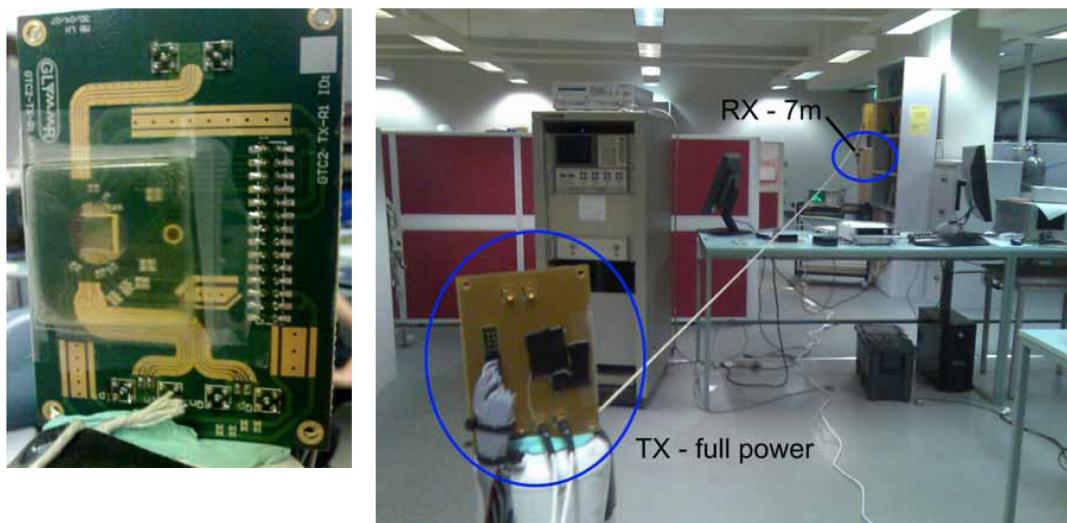


Figure 5.14: Photo showing TX to Spectrum Analyzer link experiment

5.3 GTC3-Tx: A Split-IF 60 GHz TX

This section presents the authors work on GLIMMR test-chip 3 (GTC3). In particular the transmitter and overall architecture will be shown. A block diagram of the system with the authors contributions highlighted in blue is shown in Figure 5.15.

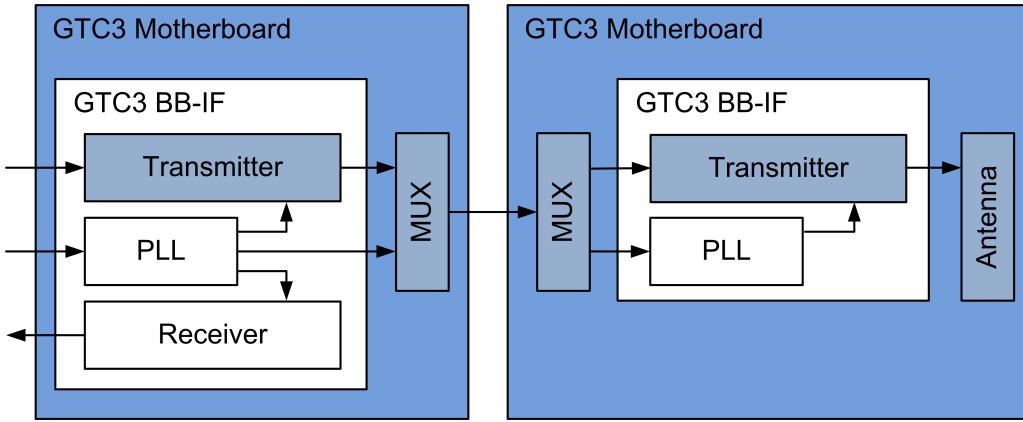


Figure 5.15: Simple diagram of GTC3 showing the areas covered in this section.

5.3.1 Introduction

The continual performance improvement, feature addition and size reduction makes the integration of millimetre wave transceivers in consumer devices challenging. Architectures used for WLAN and Bluetooth where the RF signal is routed over a coaxial cable to the antenna are problematic at 60 GHz due to high losses. Mounting the whole transceiver at the site where the antenna is located also poses difficulties due to large area of the module, high power dissipation and digital interference with LCD screens.

Figure 5.16 shows three architectures commonly used for wireless communication systems. In a laptop or television, the antennas can be up to 15cm away from the digital source.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

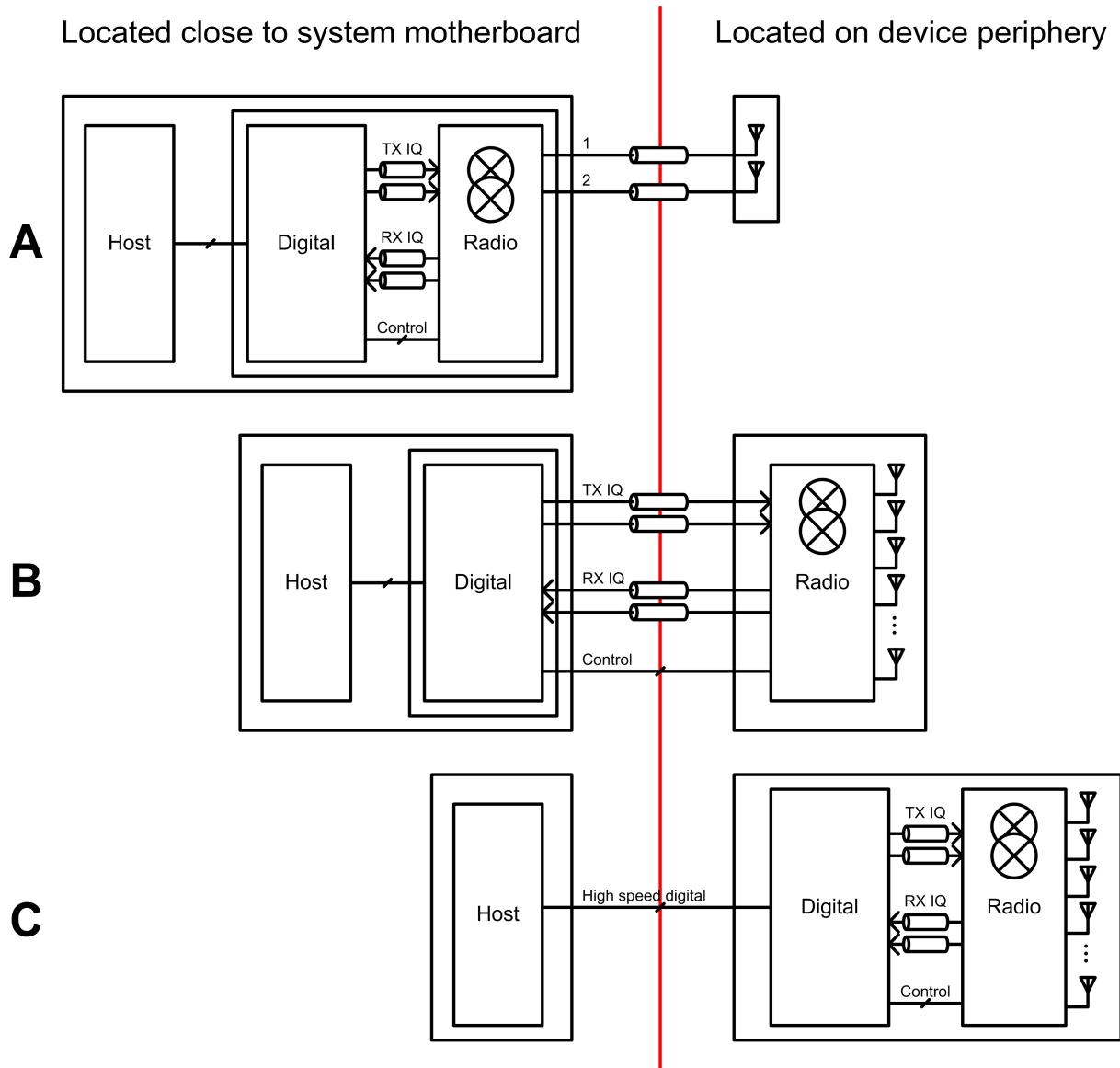


Figure 5.16: Typical architectures for wireless communication systems

5.3.1.1 RF Interface

Figure 5.16 (A) shows a typical setup for WLAN or Bluetooth where a passive antenna is separated from the radio and host platform via a long coaxial cable. This works well at lower frequencies for the following reasons. Only a few 2-4 antennas are required and the losses over the coaxial cable are low. At 60 GHz, the losses would be too high (several dB per cm).

5.3.1.2 Analog I/Q Interface

Figure 5.16 (B) shows a front-end module and antennas separated from the digital core at the analog I/Q interface. This architecture is challenging to implement due to the large number of lines required between the two chips and the power penalty of the I/Q link. It also enforces a dual chip architecture which is not competitive for WLAN or Bluetooth.

5.3.1.3 Digital Interface

Figure 5.16 (C) shows the entire radio including digital baseband at the front-end. The radio is connected to the host using digital link (PCI-e) or other.

An alternative architecture is proposed for 60 GHz systems. In this architecture the radio is split at the IF port and a single coaxial cable is used to route all the signals required.

Figure 5.17 shows a high level system diagram. The digital and radio up to an inter-

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

mediate frequency (IF) is close to the host processor. A second module which contains IF to RF conversion and the antennas is placed close to the device periphery.

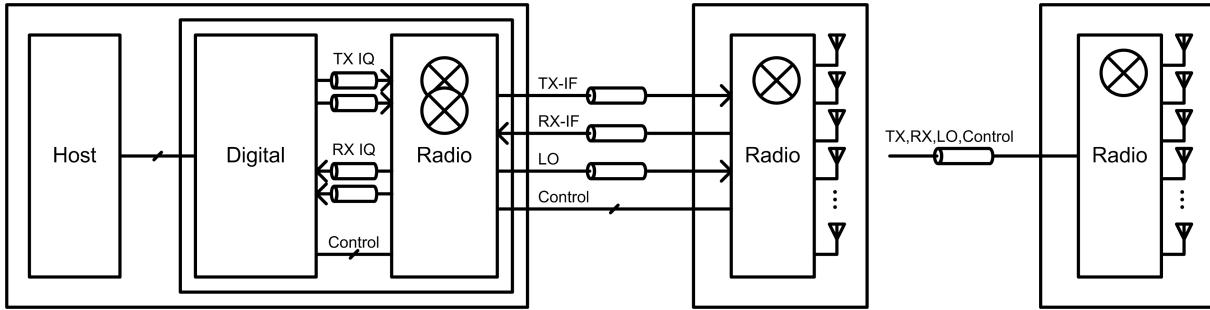


Figure 5.17: Proposed Split-IF Architecture - Taped out in January 2009.

This architecture can be implemented with multiple connections for power, IF, LO and control or the signals can be multiplexed onto a single coaxial cable.

5.3.2 System Design

Link Calculation

The target for this system is a single baseband chip with a scalable number of front-end chips. Assuming transmit and receive modules have specifications as outlined in Table 5.2, Figure 5.18 shows the distance for a 1 Gpbs link versus number of antennas. Four antennas provides a reasonable link for in-room operation.

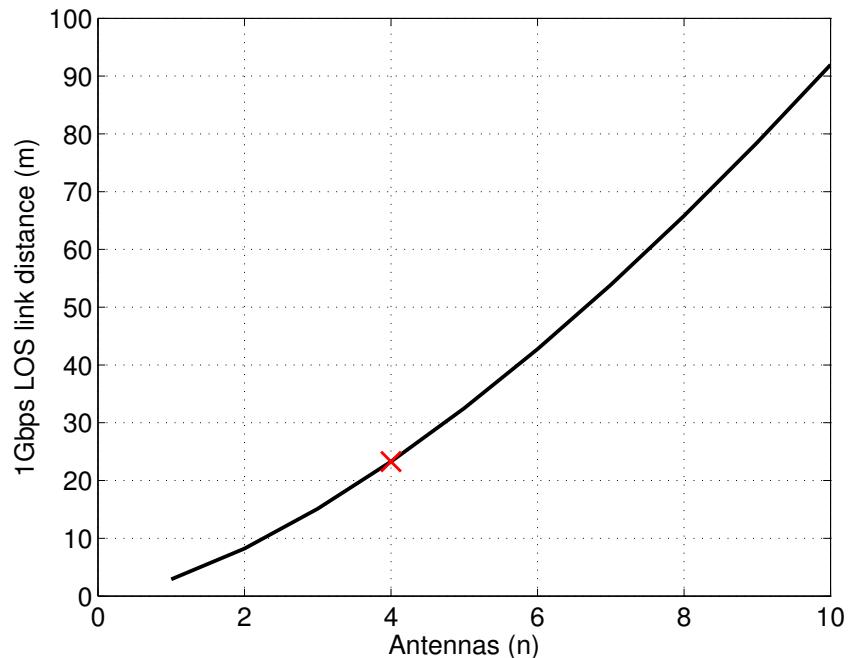


Figure 5.18: Link distance versus number of antennas for a 1 Gpbs (BPSK) 60 GHz link.

TX Specification	Units	Value
P _{sat}	dBm	>12
P _{1dB}	dBm	>10
Max Gain Variation (2 GHz channel)	dB	2

RX Specification	Units	Value
NF	dB	<10

Table 5.2: System requirements for GTC2 Tx

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

Specifications

Power over coax

The transfer of DC power over a coaxial cable to power an RF amplifier (LNA or PA) is a common technique used to improve the performance of systems at low frequencies (up to 5GHz) where the antenna would have to route several meters. It is used in remote HAM antenna installs, [89], has applications in wireless-LAN installations [90] where the antennas and amplifiers are placed on a mast and has also been used in low noise GPS receivers [91]. Most of these applications use off the shelf connectorised cables and bias tees to inject the DC signal. Bias tees are three port devices. One port is inductor coupled and contains only the DC signal (the inductor provides a high impedance to the RF), an RF port which is capacitor coupled and a DC+RF port.

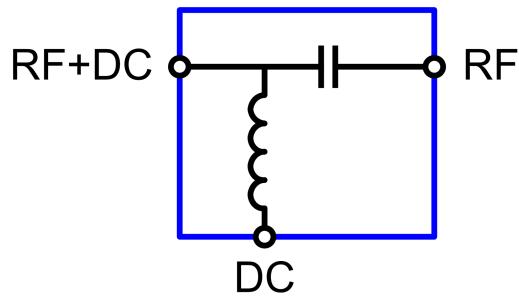


Figure 5.19: A bias tee.

One of the primary considerations when supplying DC over coax is the power lost in the bias tee and cable due to resistive losses. A power budget for the coaxial link is shown below.

The resistance of the DC link is:

$$R_{tot} = 2 \times R_{bias_tee} + 2 \times R_{connector} + R_{coax/m} \times L \quad (5.1)$$

If we include a switching regulator with efficiency = S_{eff}

$$P_{sw} = P_{out}/S_{eff} \quad (5.2)$$

$$V_{sw} = V_{in} - R_{tot} \times I_{sw} \quad (5.3)$$

$$V_{sw} = V_{in} - R_{tot} \times \left(\frac{P_{out}/S_{eff}}{V_{sw}} \right) \quad (5.4)$$

$$V_{sw}^2 - V_{sw} V_{in} + R_{tot} P_{out}/S_{eff} = 0 \quad (5.5)$$

Solving for V_{sw} we get

$$V_{sw} = V_{in}/2 + \frac{(V_{in}^2 - 4R_{tot}P_{out}/S_{eff})^2}{2} \quad (5.6)$$

and

$$P_{loss} = \frac{(V_{in} - V_{sw})^2}{R_{tot}} \quad (5.7)$$

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

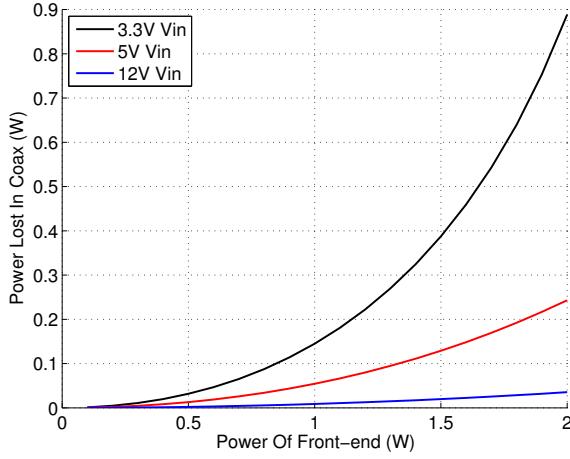


Figure 5.20: Power lost over the coax cable, assumes fixed 1Ω R_{tot}

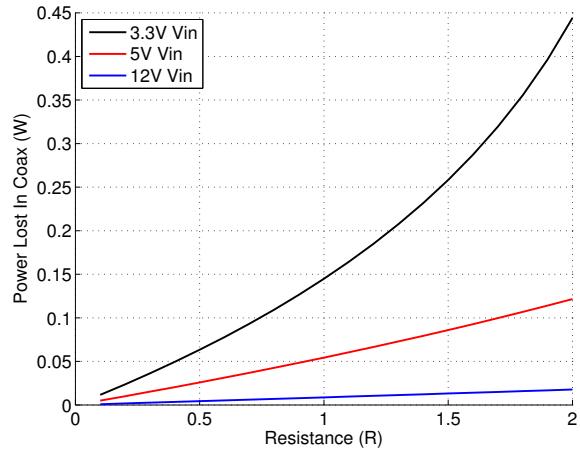


Figure 5.21: Power lost over the coax cable, assumes fixed 1W front-end power

These results show the importance of reducing the resistance of the coaxial cable and other resistive losses in the path. Also, if a higher voltage can be used (5V or 12V), it is recommended.

IF over coax

Transmitting an intermediate frequency over coaxial cable is proposed in [91] for a remote GPS installation in order to reduce the losses of routing the RF signal. This architecture is also used in satellite ground stations and cellular base-stations.

The primary goal of transmitting an IF frequency over coaxial cable is to reduce the losses associated with a higher signal level. At 60 GHz the losses over standard coaxial cable used in laptops for 5.8GHz systems would be too high (on the order of 20-30dB/m).

At 9GHz the losses are much lower and importantly, the losses do not degrade the receiver sensitivity or output power as they are at an intermediate node.

LO over coax

There are two options for sending an LO frequency over the coaxial cable. The first is to send a lower frequency signal (MHz range) and use that to lock a PLL on the front-end as shown in [24].

The second option is to send a harmonic component of the final LO and use frequency multiplication at the front-end. This is the option we use in this work. The frequency plan is shown next.

Frequency Plan

There are several considerations for the frequency plan in a multiplexed system.

The frequency scheme chosen is VCO/2 for LO1, VCOx3 for LO2 resulting in a VCO range from 16-19GHz.

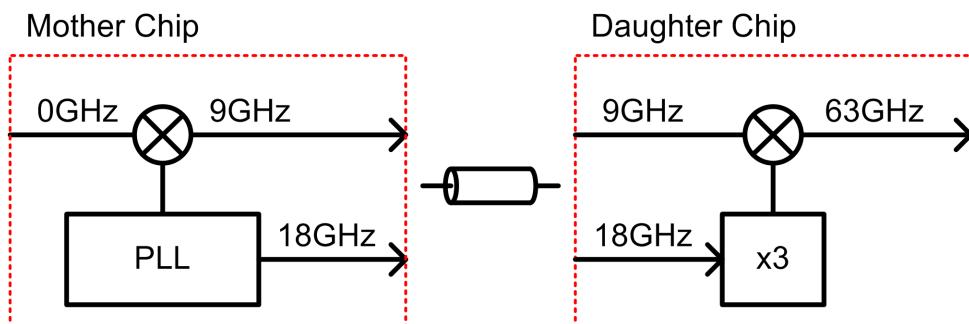


Figure 5.22: Frequency Plan for Split-IF Architecture

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

Channel	Frequency	IF Frequency	VCO Frequency	LO Frequency
1	58.32	8.33	16.66	49.99
2	60.48	8.64	17.28	51.84
3	62.64	8.95	17.90	53.59
4	64.8	9.26	18.51	55.54

Table 5.3: Split-IF Radio Frequency Plan

Control over coax

We did not implement the circuitry for control over coax on the chip - we envisaged a simple ASK or OOK system running at low GHz frequencies. This should operate in the linear region to reduce any harmonic and intermodulation content outside of the band. It should also be designed to be away from standard communication bands such as cellular, Bluetooth and Wireless LAN.

Block Diagram

The TX block diagram is shown in Figure 5.23. The two chips taped out are shown in blue highlight (some features removed for clarity). The left chip contains baseband to IF up-conversion as well as a PLL. The right chip contains IF to RF up-conversion mixer, a PA, a tripler and a phase shifter in the 18GHz LO path.

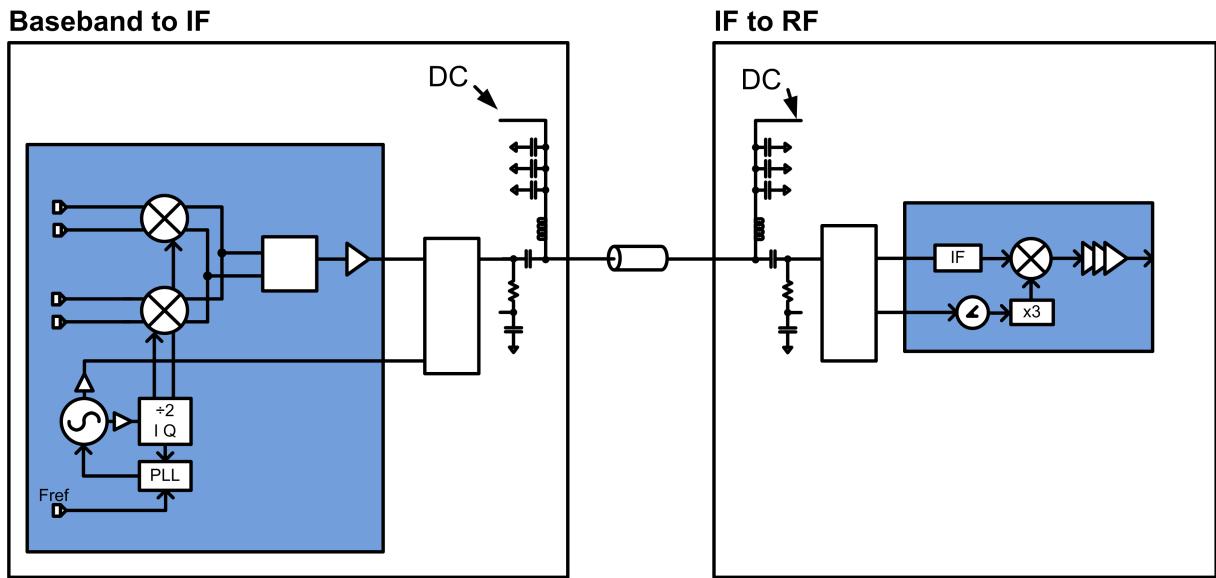


Figure 5.23: TX block diagram for Split-IF architecture

5.3.3 Circuit Design - Mother Chip

Baseband to IF mixer

5.3.4 Circuit Design - TX Daughter

IF to RF mixer

The IF to RF mixer shown in Figure 5.25 is a simple Gilbert cell which is matched to the output of the IF amplifier and the input of the power amplifier. Rather than matching to a 50ohm impedance, the conjugate matching networks save area.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

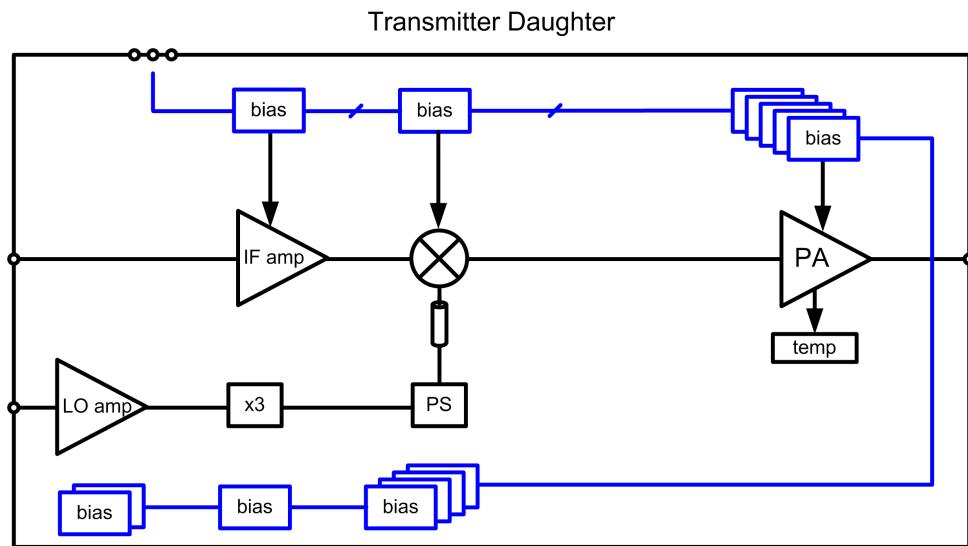


Figure 5.24: TX Daughter Chip Block Diagram

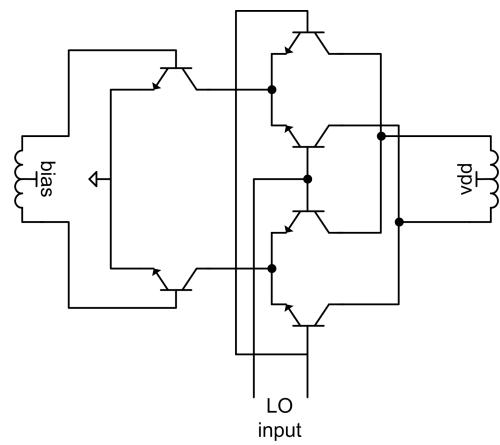


Figure 5.25: Schematic of IF to RF mixer

Power Amplifier

The PA is discussed in detail in the previous chapter. The schematic is shown in Figure 5.26. It is a four stage transformer coupled design which achieves 25-30dB gain and has a wide band-width.

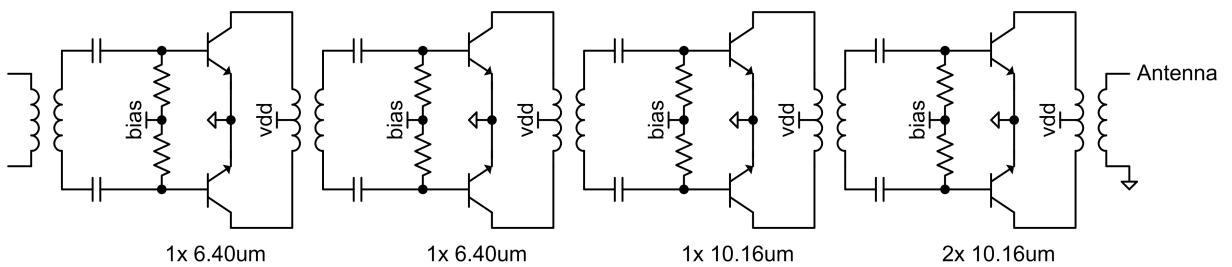


Figure 5.26: Schematic of Power Amplifier

5.3.5 Layout

5.3.6 Module Design

The front-end module for GTC3-Tx is shown in the figure below. It consists of an IF and LO input and a connector for 60 GHz output. The module is designed for wire-bond connection and has a routed out area for the die to sit in that reduces the 60 GHz losses.

The wire-bond connections are optimised for low loss. A zoomed in photo of the module is shown in Figure 5.30.

The wire-bond connection was simulated and optimised in HFSS. The simulated loss with protective goop is between 0.8 and 1.2dB across the 60 GHz band. This also includes some transmission line routing on the PCB and chip.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

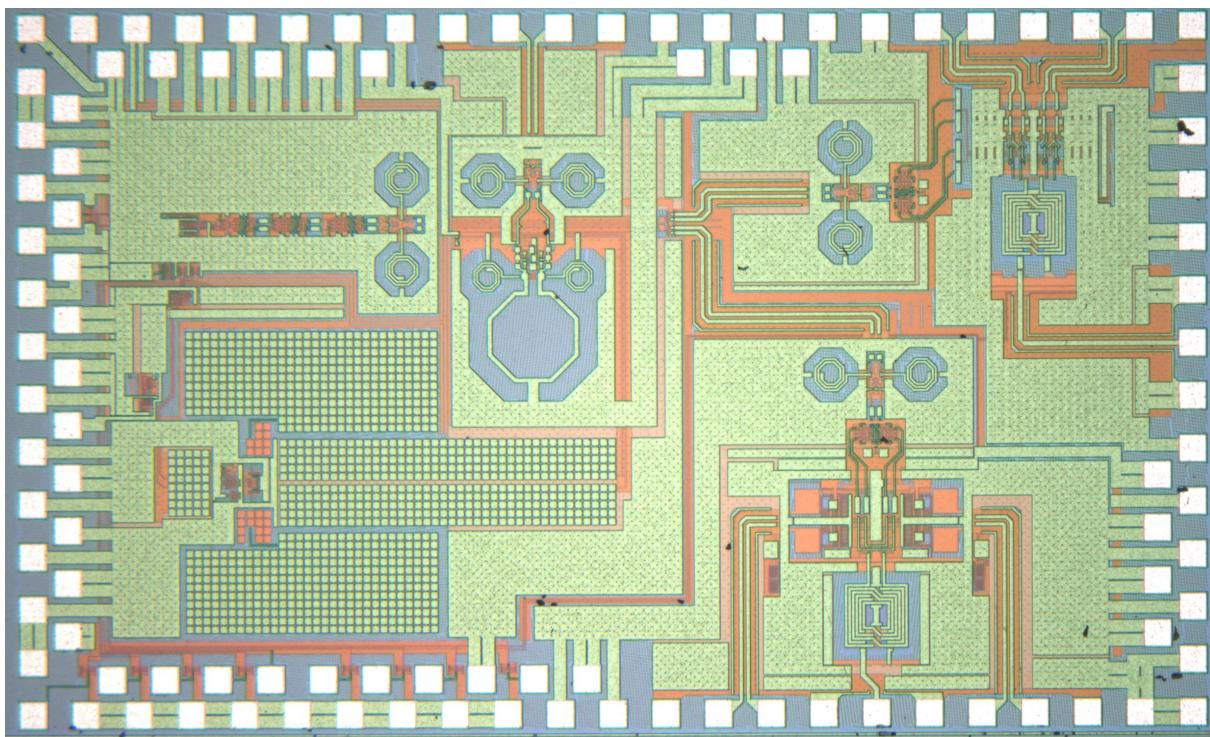


Figure 5.27: *Chip micro-graph for Baseband to IF Chip*

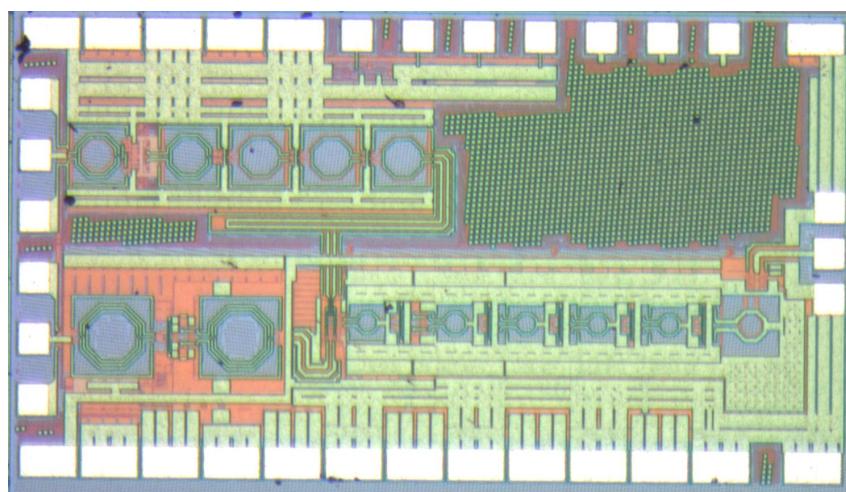


Figure 5.28: *Chip micro-graph for IF to RF chip*

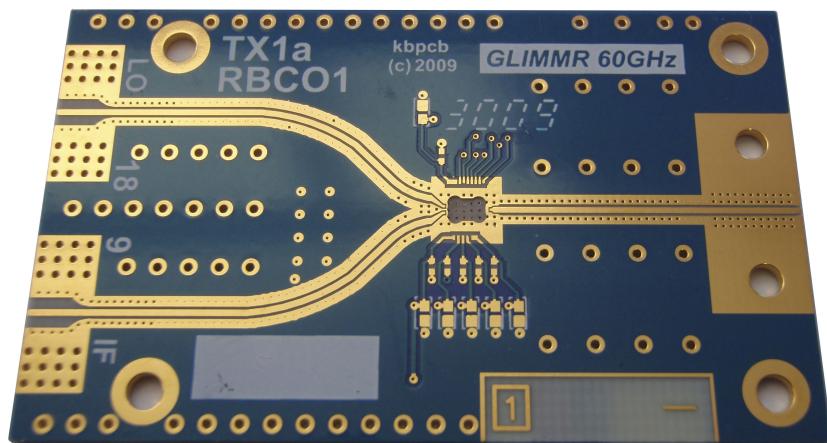


Figure 5.29: Photo of GTC3 module.

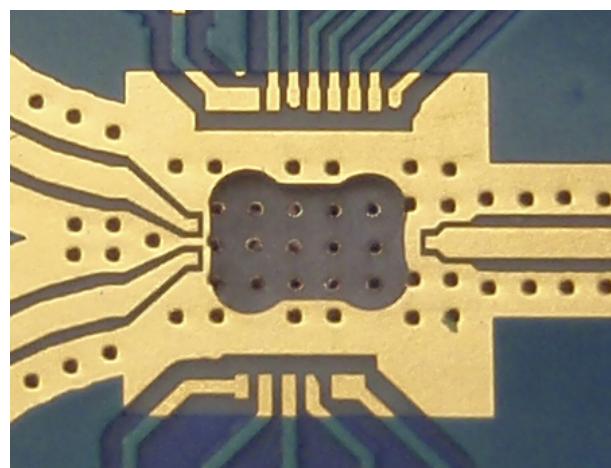


Figure 5.30: Photo of GTC3 module.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

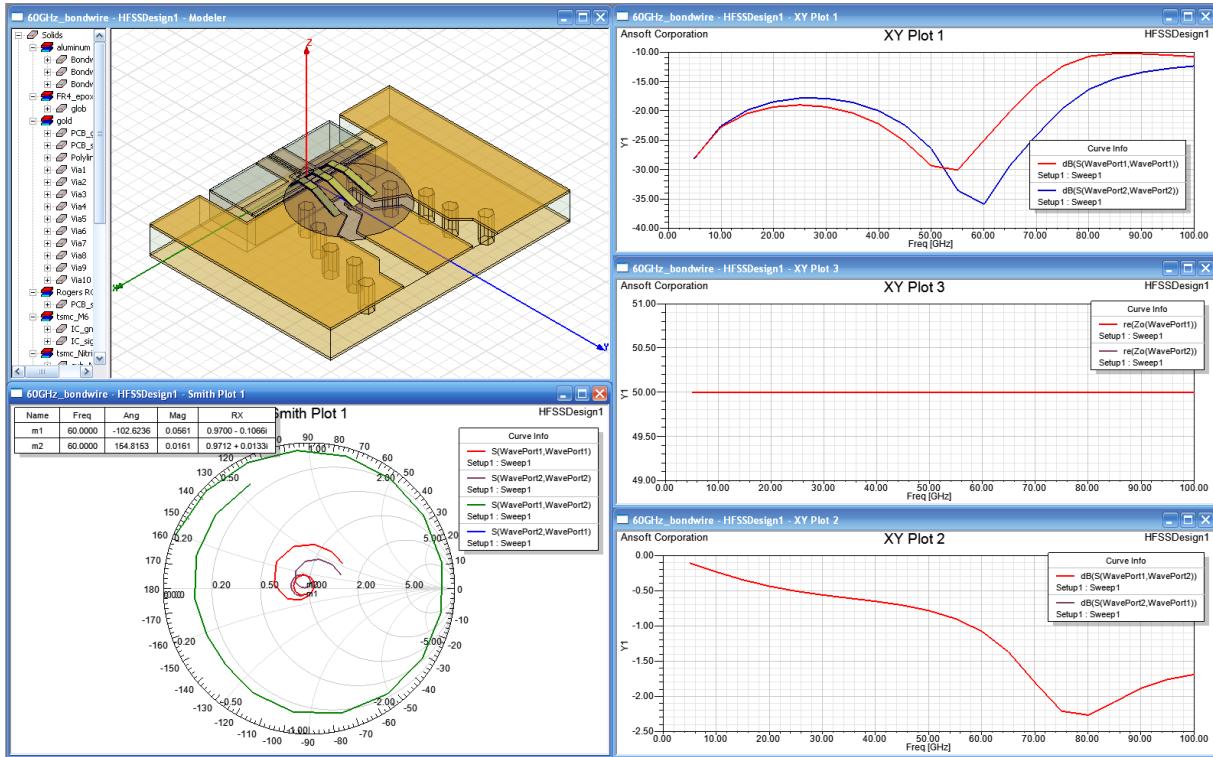


Figure 5.31: Photo of GTC3 module.

5.3.7 4 Element Linear Phased Array

A four-element phased array was designed in HFSS. The elements are proximity coupled patch antennas which reduce the requirement for fine resolution (and tight tolerance) vias.

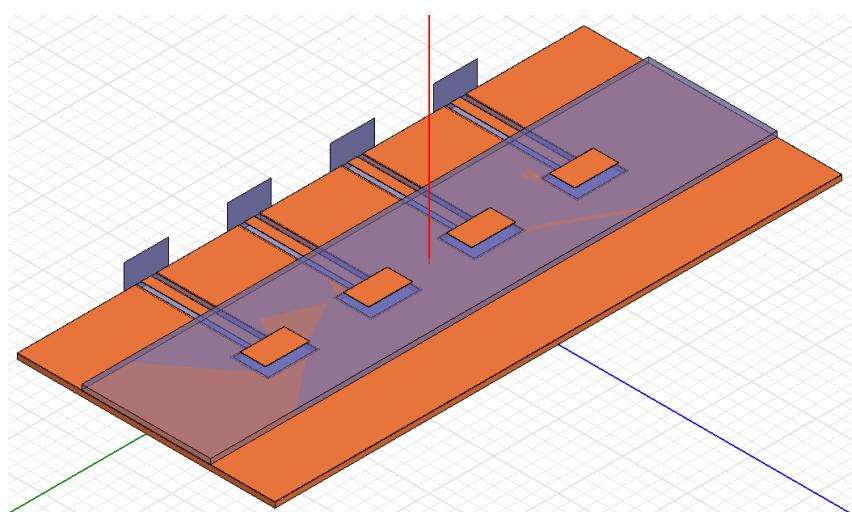


Figure 5.32: Photo of GTC3 module.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

5.3.8 Measurement Results

The test and measurement setup is shown in Figure 5.33. Agilent E82x7D sources are used for the 9 GHz IF signal and 18 GHz LO signal. A Rohde and Schwarz NRP-Z57 60 GHz power meter is used to measure the cable loss and calibrate the spectrum analyzer. A Rhode and Schwarz FSU 67 GHz spectrum analyzer is used to measure different frequency components.

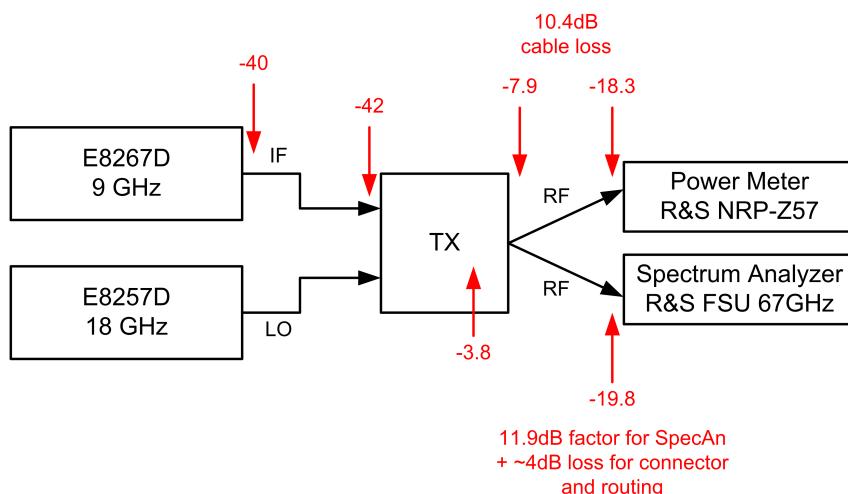


Figure 5.33: Test and calibration setup for GTC3 measurements.

The current for different sub-blocks at several bias points is measured in Figure 5.4. It shows the digital controller is working and the block settings can be updated. The last stage of the PA consumes the largest amount of current.

Bias	IF	Mix	PA1	PA2	PA3	PA4	PA5	PSa	PSb	PSc	PSd	LO	x3	48G	48G
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	10	6	16	16	15	24	47	0	4	0	4	10	6	6	6
15	19	9	30	31	30	45	85	0	4	0	4	19	12	12	12
24	26	12			40	62	112	0	6	0	6	27	18	17	17
31	34	14	55	53	53	77	131	0	6	0	6	35	21	22	22

Table 5.4: GTC3 Tx current consumption in mA from 1.8V.

The gain of the transmitter from 9GHz IF input to 60GHz RF output is shown for each 802.11ad channel in Figures 5.34 and 5.35. It can be seen that the transmitter is slightly high tuned. The gain flatness for channels 2,3 and 4 is less than 5 dB which is easily correctable with DAC pre-distortion. Channel 1 flatness is slightly worse and could be corrected with a metal spin.

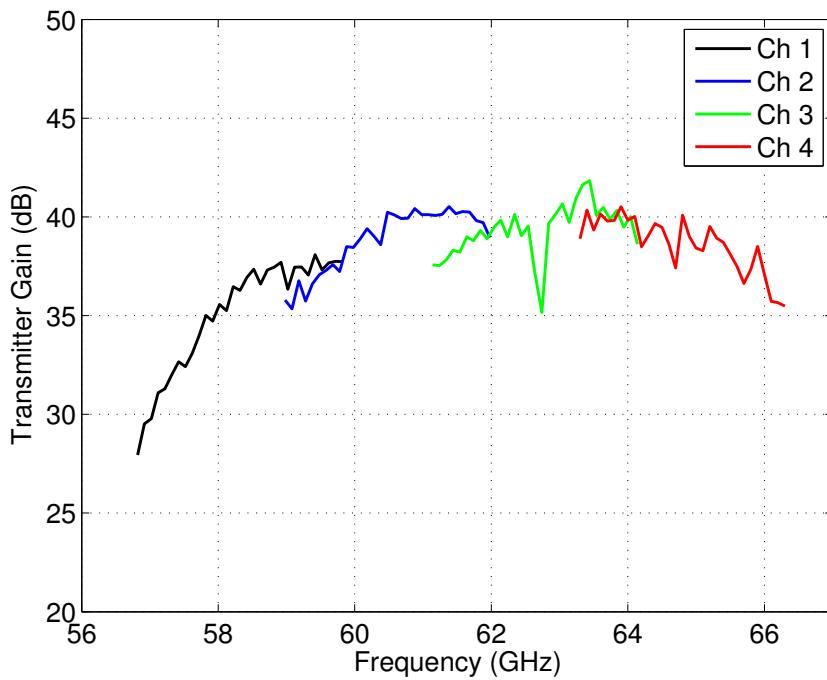


Figure 5.34: TX gain for each 802.11ad channel.

The output 1dB compression point of the TX is an important specification. The Op1dB point is shown measured across each channel in Figures 5.36 and 5.37. This measurement is taken with the spectrum analyzer and calibrated with the power meter. It shows that the output 1dB compression point varies from 4 to 10 dBm calibrated to the output of the chip. The compression point is dependent on the output match and falls off at the edges of channel 1 and 4. There is also a consistent notch in the measurements at 62.8 GHz which most likely comes from the bond-wire and transmission line interface to the 60GHz coaxial connector.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

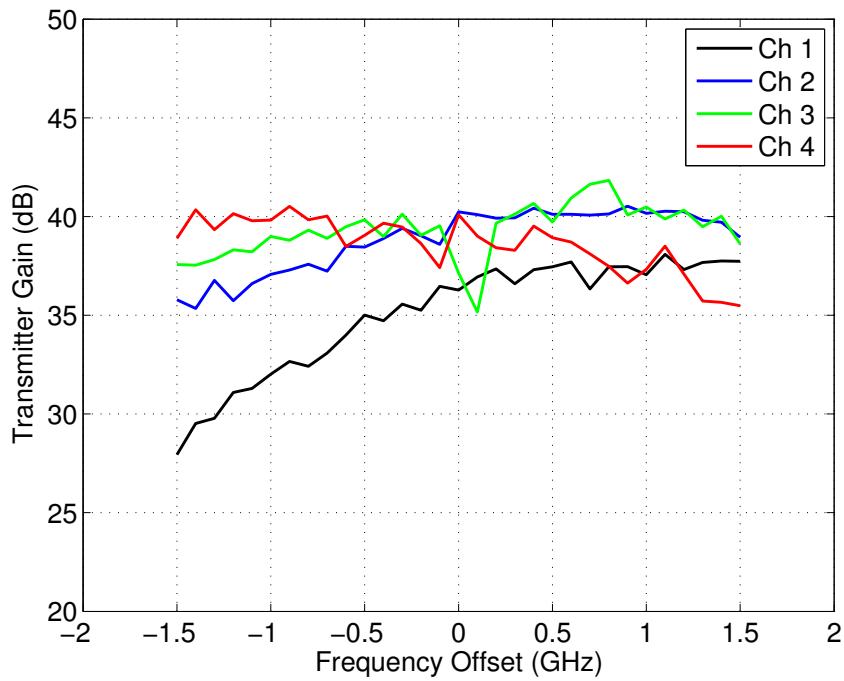


Figure 5.35: Relative TX gains for each 802.11ad channel.

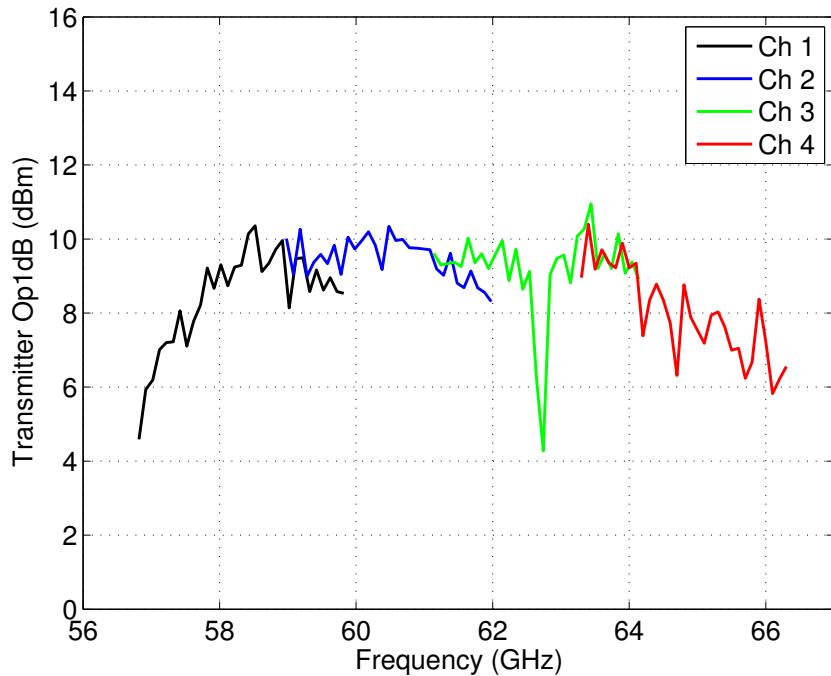


Figure 5.36: TX output 1dB compression point for each 802.11ad channel.

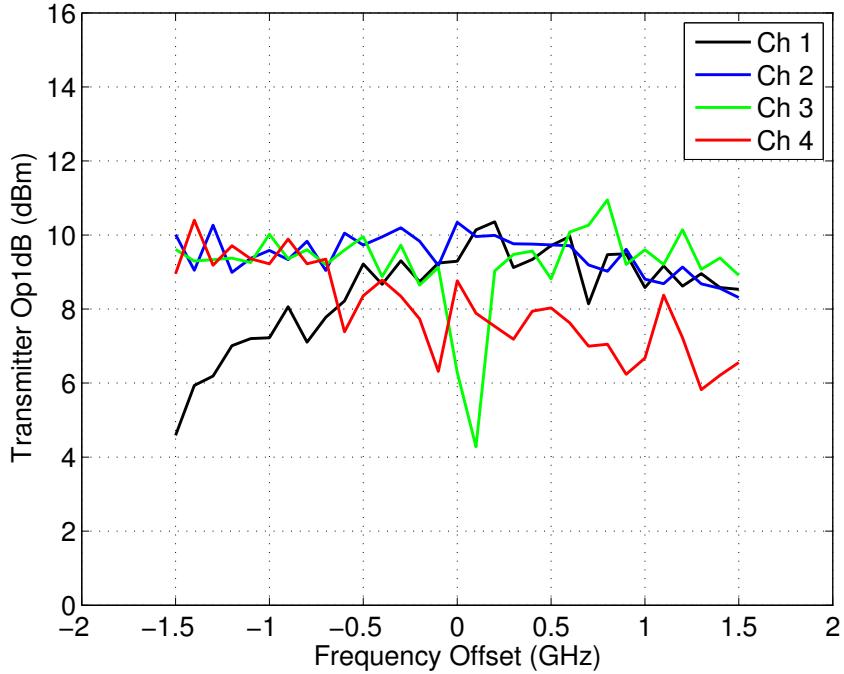


Figure 5.37: Relative TX output 1dB compression point for each 802.11ad channel.

A spectrum plot for each channel is shown in Figure 5.38 it shows the lower image, LO feedthrough and the upper image.

Figure 5.39 shows the gain versus IFamp and mixer bias settings. Figure 5.40 shows the transmitter output 1dB compression point versus the IFamp and mixer bias settings.

A plot of the transmitter gain with fixed IF frequency is shown in Figure 5.41. It shows the frequency response of the PA and output matching network. It shows a flat response from 58 to 67 GHz with a steep roll-off beyond that.

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

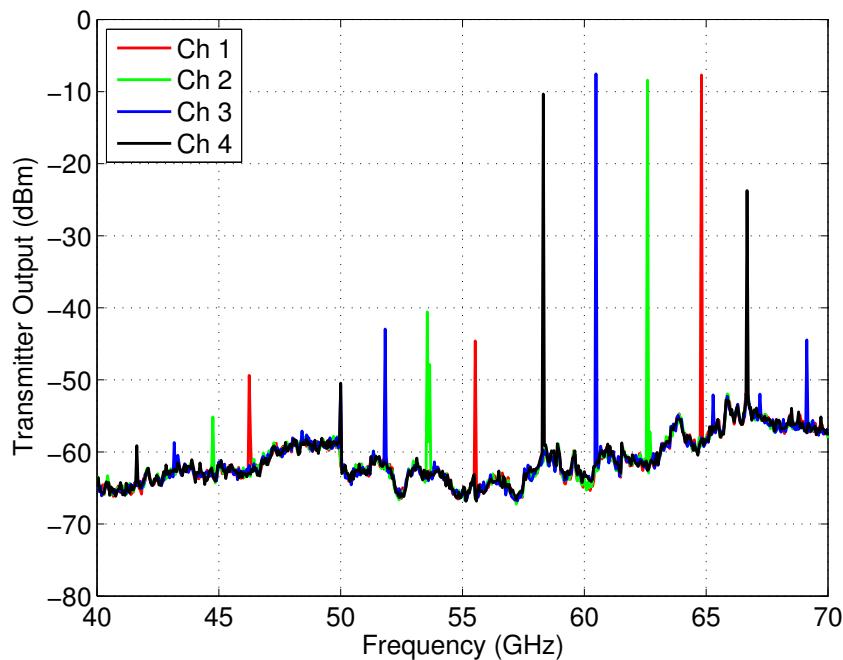


Figure 5.38: Output spectrum for each channel showing lower image, LO signal and upper image.

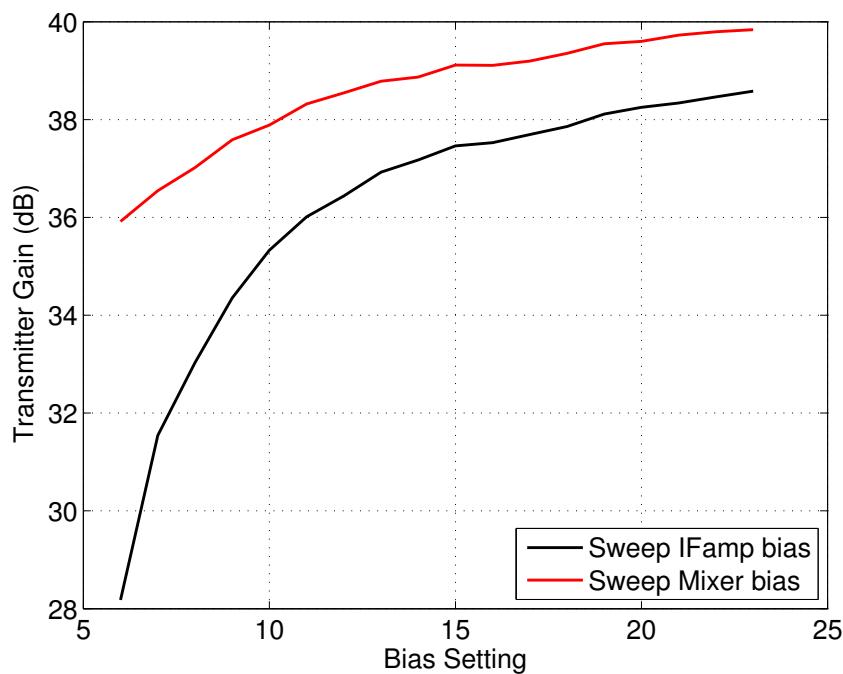


Figure 5.39: Gain versus IFamp and mixer bias settings.

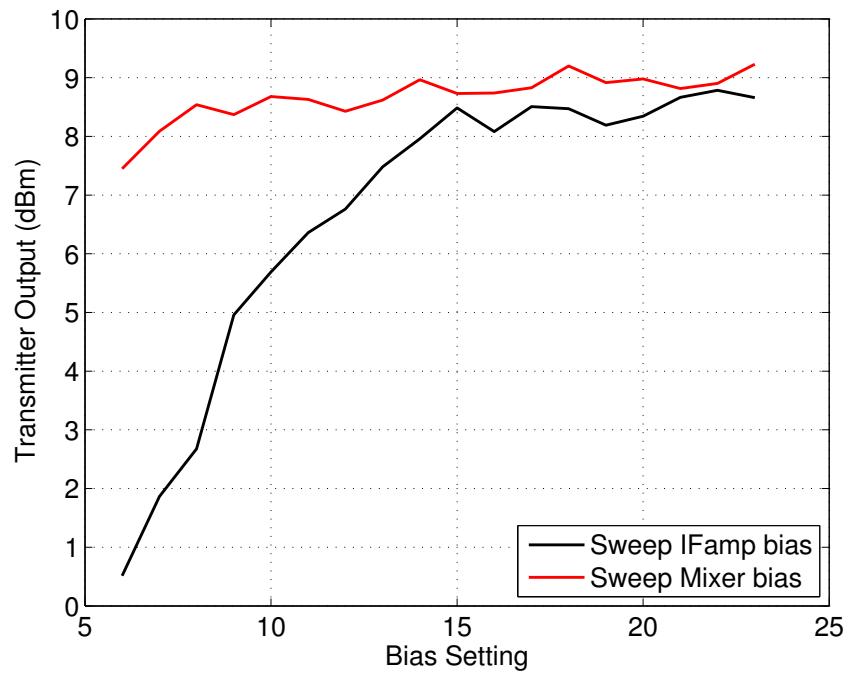


Figure 5.40: Op1dB compression point versus IFamp and mixer bias settings.

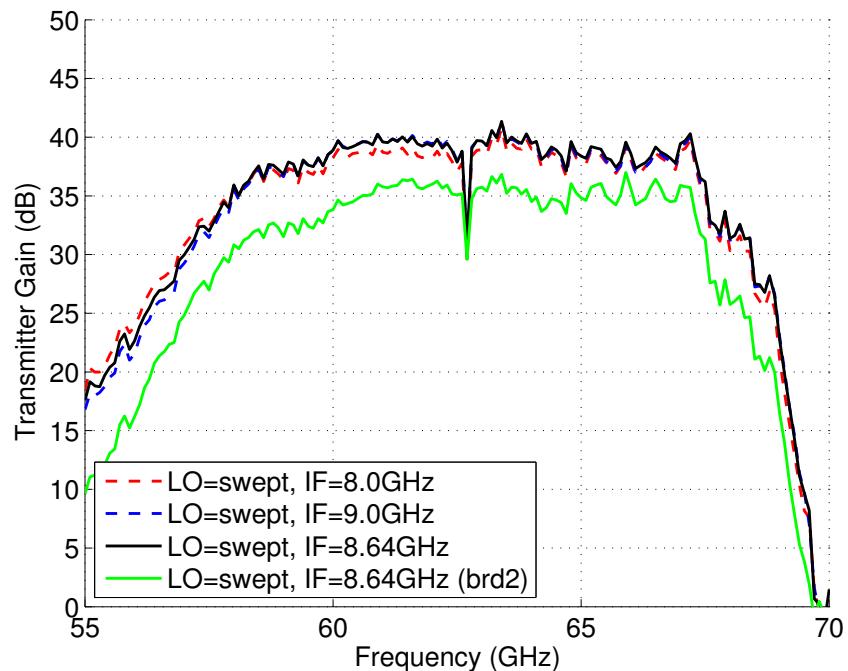


Figure 5.41: Gain and Saturated Output Power

5. ARCHITECTURES FOR MM-WAVE SYSTEMS

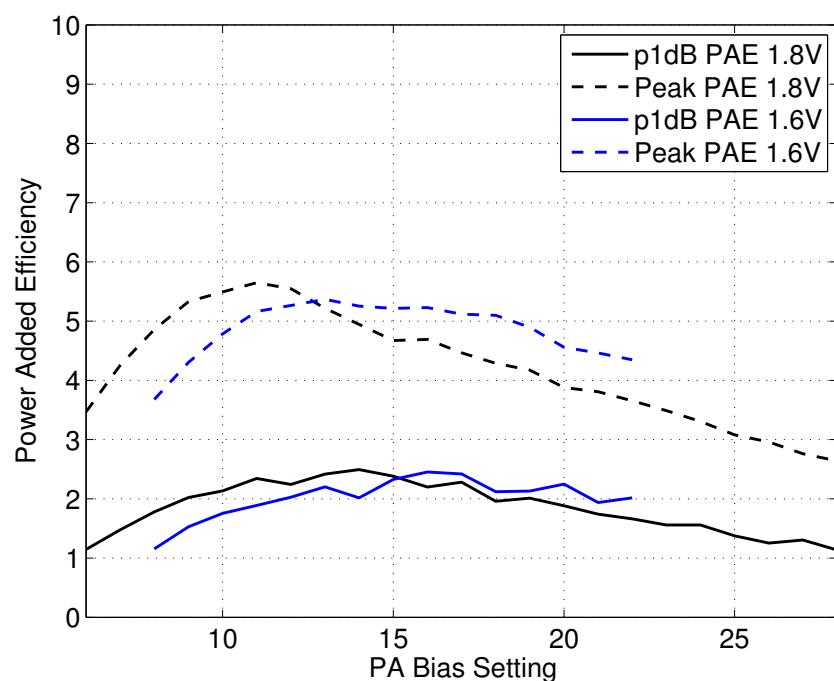


Figure 5.42: Gain and Saturated Output Power

6

Conclusions

This research has investigated circuits and architectures for 60 GHz transmitters and proposes a system architecture for high speed applications that is amenable to integration in large consumer electronic devices.

6.1 Contributions

6.1.1 Power Amplifier Design

The power amplifier is a key block in the radio transmitter. A design flow is outlined in Chapter 4 which scales from low frequency to 60 GHz and enabled the first time

right design of four power amplifiers. A high efficiency power amplifier at 1 GHz was designed for the IMS student power amplifier competition and won first place, it achieved greater than 88% efficiency. A transmission line based 60 GHz PA was demonstrated in 0.18um SiGe that achieves 30dB gain and 3dB bandwidth of 11.5GHz. Two transformer coupled power amplifiers were designed for 60GHz. The first, a SiGe 5 stage design achieves a wide bandwidth, high gain but a peak efficiency of only 5%. A second design in 65nm CMOS achieves a high gain and efficiency and shows the advantage of neutralization.

6.1.2 Transmitter System Design

Chapter 3 outlines some of the key differences between 60 GHz and 5 GHz systems. Millimeter wave transmitter fundamentals are outlined as well as several impairments. The requirement for phased array systems is demonstrated and fundamentals are reviewed. A link budget for 60 GHz system is built and transmitter specifications derived. Given a system power budget a technique

6.1.3 Split-IF Architecture for 60GHz Systems

6.2 Opportunities for Further Work

6.3 Summary

A

Acronyms

SSD Solid-State Drive

TX Transmitter

PA Power Amplifier

IC Integrated Circuit

CMOS Complementary metaloxidesemiconductor

SiGe Silicon Germanium

GaAs Gallium Arsenide

InP Indium Phosphide

APPENDIX

PC Personal Computer

LAN Local Area Network

WLAN Wireless LAN

USB Universal Serial Bus

HD High Definition

FET Field Effect Transistor

HBT Heterojunction Bipolar Transistor

B

Programming Code

B.1 Arduino Code

```
const int reg_width = 5;
const int reg_number = 15;
int data_in[reg_number] = {14,14,14,14,14,14,14,14,14,14,14,14,14,14,14,14};
int data_out[reg_number];
int incomingByte = 0;

void setup() {
    pinMode(13, OUTPUT); // this is SCLK
    pinMode(12, INPUT); // this is MISO --- chip sdi
    pinMode(11, OUTPUT); // this is MOSI --- chip sdo
    pinMode(10, OUTPUT); // this is EN --- chip EN
    // init serial port
    Serial.begin(19200);

    digitalWrite(10, LOW);

    for (int i=reg_number-1; i>=0; i--) {
        data_out[i] = readWriteReg(0);
```

APPENDIX

```
//Serial.println(data_out[i]);
}
for (int i=reg_number-1; i>=0; i--) {
    data_out[i] = readWriteReg(0);
    //Serial.println(data_out[i]);
}
// clear out registers
digitalWrite(10, HIGH);
delay(8);
digitalWrite(10, LOW);
delay(8);
}

void loop() {
    // send data only when you receive data:
    if (Serial.available() > 3) {
        // looking for address, value pair 127,222
        int strt=0;
        int gadd=0;
        int addr=0;
        int data=0;
        int gdat=0;
        while (Serial.available() > 0) {
            incomingByte = Serial.read();
            if (incomingByte == 58) {
                strt=1;
            }
            else if (strt == 1 && gadd==0 && gdat==0) {
                addr=incomingByte;
                gadd=1;
            }
            else if (strt == 1 && gadd==1 && gdat==0) {
                data=incomingByte;
                gdat=1;
            }
            else if (incomingByte == 59 && strt == 1 && gadd==1 && gdat==1) {
                if (addr <= 14 && data <= 31) {
                    data_in[addr] = data;
                    for (int i=reg_number-1; i>=0; i--) {
                        data_out[i] = readWriteReg(data_in[i]);
                    }
                    delay(10);
                    digitalWrite(10, HIGH);
                    delay(8);
                    digitalWrite(10, LOW);
                    delay(8);
                }
            }
            else if (incomingByte == 60 && strt == 1 && gadd==1 && gdat==1) {
                if (addr <= 14 && data <= 31) {
                    data_in[addr] = data;
```

```
        }
    }
    else if (incomingByte == 61 && strt == 1 && gadd==1 && gdat==1) {
        for (int i=reg_number-1; i>=0; i--) {
            data_out[i] = readWriteReg(data_in[i]);
        }
        delay(10);
        digitalWrite(10, HIGH);
        delay(8);
        digitalWrite(10, LOW);
        delay(8);
    }
}
}

unsigned int readWriteReg(int data) {
    int out = 0;
    int in = 0;
    for (int i=reg_width-1; i>=0; i--) {
        in = readWriteBit(bitRead(data, i));
        out = out + in*(pow(2,i));
    }
    return out;
}

unsigned int readWriteBit(int data) {
    int val = 0;
    // set data
    digitalWrite(11, data);
    delay(2);
    // raise clock
    digitalWrite(13, HIGH);
    delay(1);
    // read data
    val = digitalRead(12);
    delay(1);
    // set clock low
    digitalWrite(13, LOW);
    // return the read value
    return(val);
}
```

B.2 Python Code

```
import serial
from time import sleep

ser = serial.Serial(
    port='COM61',
    baudrate=19200
)
ser.open()

def ggWrite(addr,data):
    ser.write(':%c%c;' % (chr(addr),chr(data)))
    sleep(2)

def ggLoad(addr,data):
    ser.write(':%c%c%c' % (chr(addr),chr(data),chr(60)))
    sleep(0.5)

def ggTrig():
    ser.write(':%c%c%c' % (chr(0),chr(0),chr(61)))
    sleep(2)

def ggWritePA(bias1,bias2,bias3,bias4,bias5):
    ggLoad(2,bias1)
    ggLoad(3,bias2)
    ggLoad(4,bias3)
    ggLoad(5,bias4)
    ggLoad(6,bias5)
    ggTrig()

def ggWritePS(a,b,c,d):
    ggLoad(7,a)
    ggLoad(8,b)
    ggLoad(9,c)
    ggLoad(10,d)
    ggTrig()
```

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