



VRIJE
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Analog Electronics lab session

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Session 3 : Design of differential pairs and of an OTA

In this exercise you will learn ...

- Fundamentals about differential pairs
- How to “design on paper”
 - Differential pair with resistive load
 - OTA
- Learn to value $\frac{g_m}{I_D}$ - and $\frac{g_m}{g_{ds}}$ -plots !
 - with those plots one can identify design trade-offs!
- How to code in MATLAB the OTA-design

Session 3 : Design of differential pairs and of an OTA

- Solve exercise I a-d
 - ETA: 20 min

Session 3 : Design of differential pairs and of an OTA

Exercise I

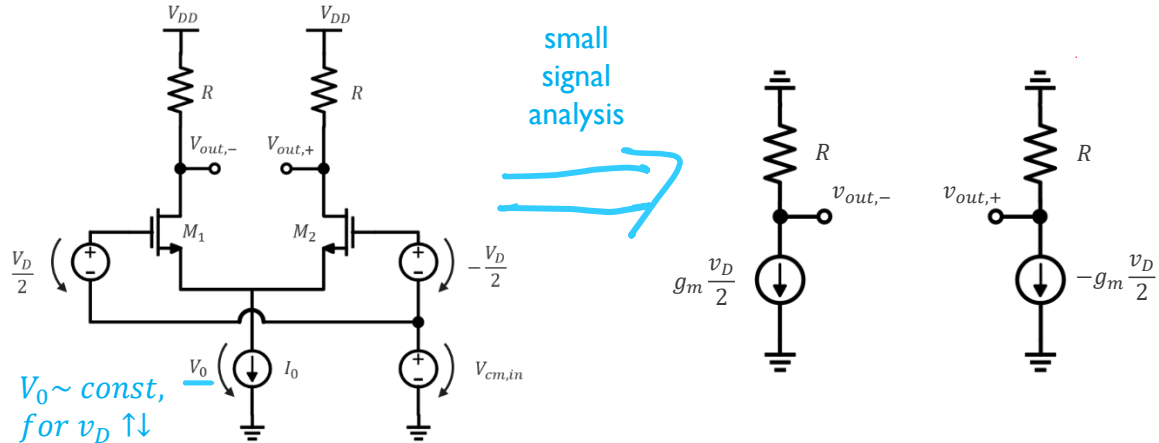
- a) Give the equation of the small signal voltage gain $\frac{v_{out,-}}{v_D}$, $\frac{v_{out,+}}{v_D}$ and the differential voltage gain, when $V_D = 0$?

a) Remark: $M_1 = M_2$

$$A_{V,-} = \frac{v_{out,-}}{v_D} = -\frac{g_m}{2} \cdot R$$

$$A_{V,+} = \frac{v_{out,+}}{v_D} = \frac{g_m}{2} \cdot R$$

$$A_{V,diff} = g_m \cdot R$$

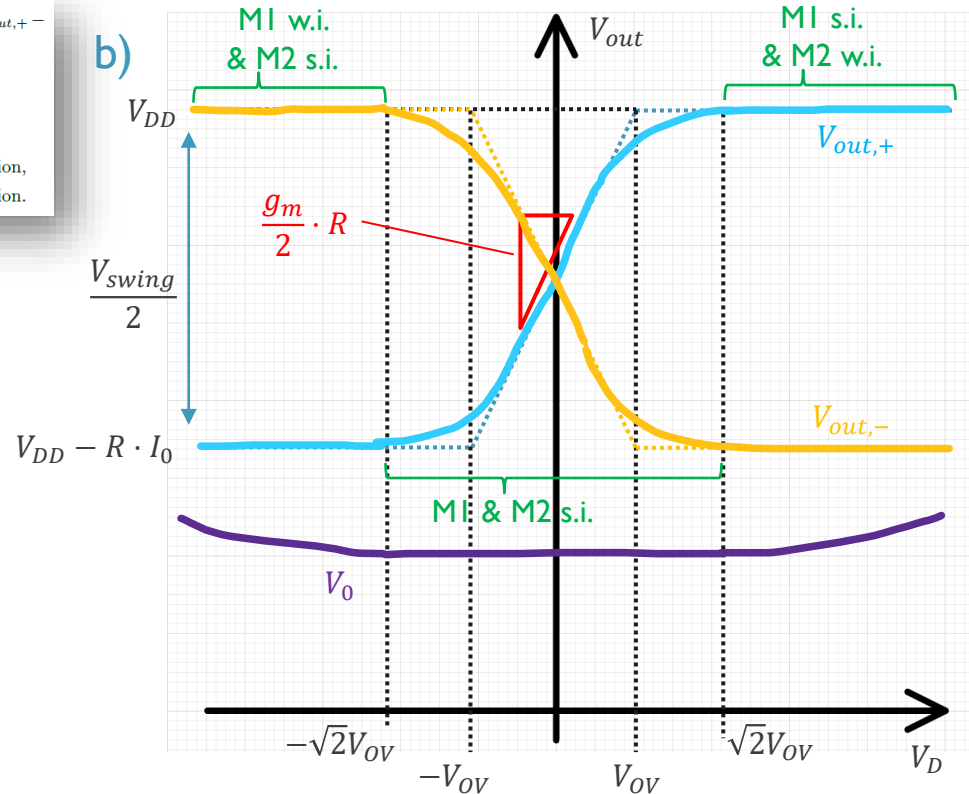
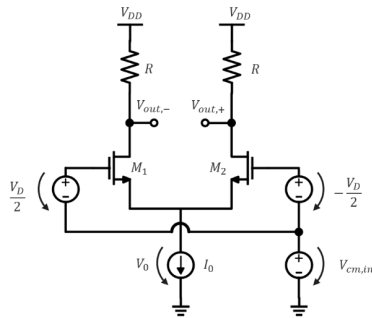


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Exercise I

b) Draw on Fig. 2 the voltages $V_{out,+}$, $V_{out,-}$ and V_0 and on Fig. 3 ($V_{out,+} - V_{out,-}$) qualitatively. Moreover, indicate on both figures:

- V_{OV} and $\sqrt{2}V_{OV}$,
- A_V ,
- range, where M_1 and M_2 are in strong inversion,
- range, where M_1 is in weak inversion, but M_2 in strong inversion,
- range, where M_1 is in strong inversion, but M_2 in weak inversion.

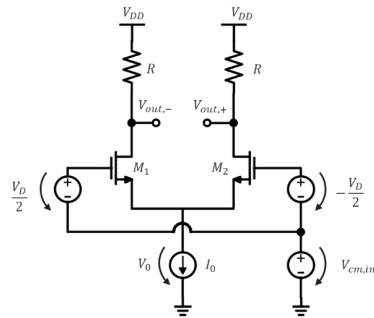


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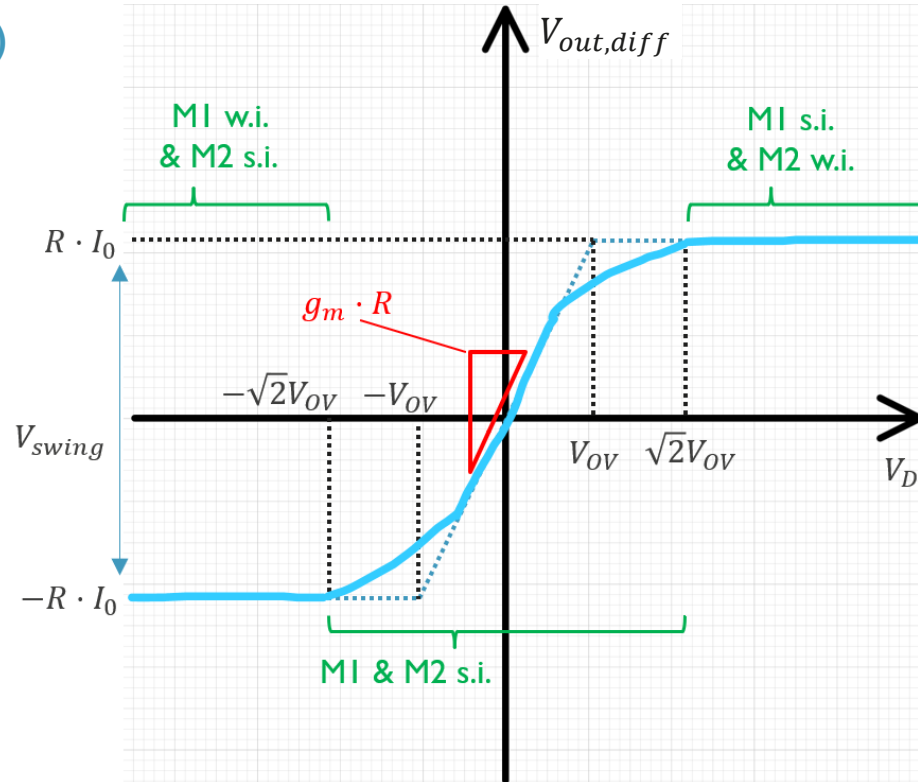
Exercise I

b) Draw on Fig. 2 the voltages $V_{out,+}$, $V_{out,-}$ and V_0 and on Fig. 3 ($V_{out,+} - V_{out,-}$) qualitatively. Moreover, indicate on both figures:

- (i) V_{OV} and $\sqrt{2}V_{OV}$,
- (ii) A_V ,
- (iii) range, where M_1 and M_2 are in strong inversion,
- (iv) range, where M_1 is in weak inversion, but M_2 in strong inversion,
- (v) range, where M_1 is in strong inversion, but M_2 in weak inversion.



b)



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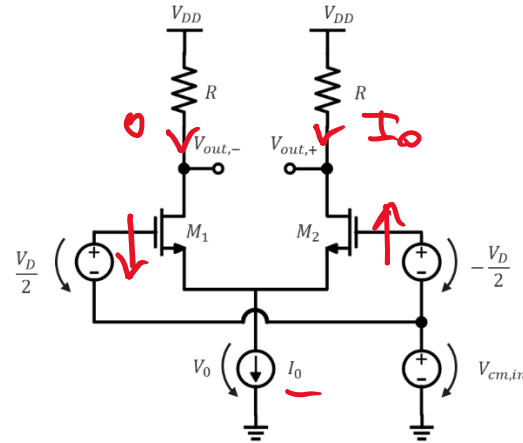
Exercise I

c) Give the amount of current, which is flowing through M_1 and M_2 , when

- (i) $V_D = 0$,
- (ii) $V_D < -\sqrt{2} \cdot V_{OV}$,
- (iii) $V_D > \sqrt{2} \cdot V_{OV}$.

c) $I_{D,M1}$ and $I_{D,M2}$ given as follows

- i. $V_D = 0V$: $I_{D,M1} = I_{D,M2} = 0.5 \cdot I_0$
- ii. $V_D > \sqrt{2} \cdot V_{OV}$: $I_{D,M1} = I_0$ and $I_{D,M2} = 0$
- iii. $V_D < -\sqrt{2} \cdot V_{OV}$: $I_{D,M1} = 0$ and $I_{D,M2} = I_0$



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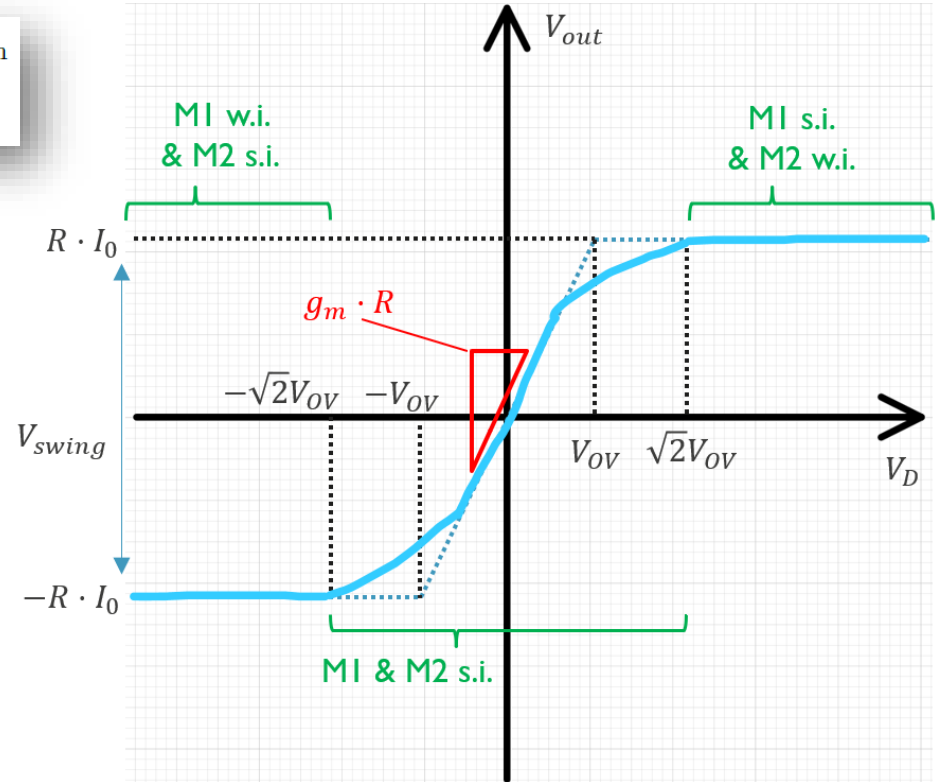
Exercise I

- d) Based on Fig. 3, derive an equation describing the relationship between V_{swing} , V_{OV} and A_V .

Remark: $V_{swing} = \max(V_{out,+} - V_{out,-}) - \min(V_{out,+} - V_{out,-})$

- d) option I: graphically

$$\Rightarrow A_{V,diff} = \frac{V_{swing}}{2 \cdot V_{OV}}$$



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Exercise I

d) Based on Fig. 3, derive an equation describing the relationship between V_{swing} , V_{OV} and A_V .

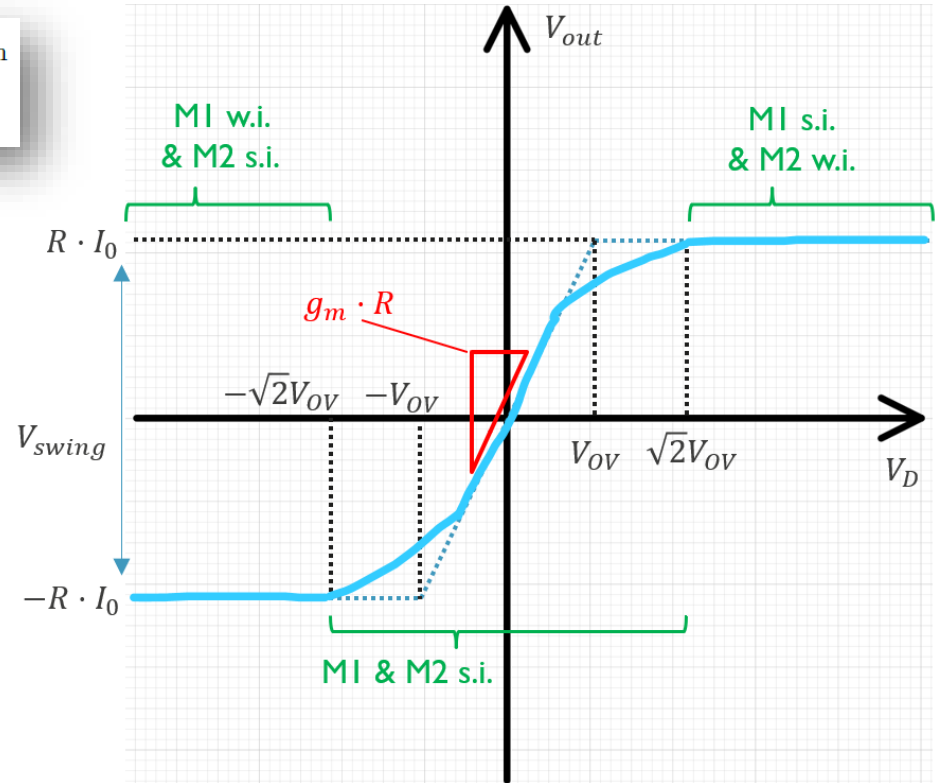
Remark: $V_{swing} = \max(V_{out,+} - V_{out,-}) - \min(V_{out,+} - V_{out,-})$

d) option 2: analytically

$$\frac{g_{m1,2}}{I_{D1,2}} = \frac{g_{m1,2} \cdot R}{(I_0/2) \cdot R} = \frac{2}{V_{OV}}$$

$$\Leftrightarrow 2 \cdot A_{V,diff} = \frac{I_0}{V_{OV}} \cdot 2 \cdot R = \frac{V_{swing}}{V_{OV}}$$

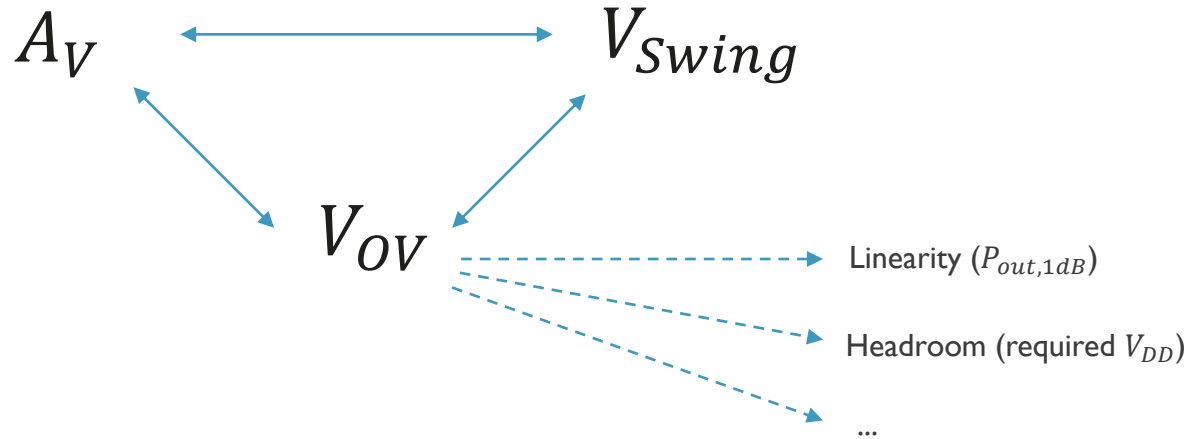
$$\Leftrightarrow A_{V,diff} = \frac{V_{swing}}{2 \cdot V_{OV}}$$



Session 3 : Design of differential pairs and of an OTA

Summary

- Waveforms of an ideal differential amplifier has been presented
- (in this exercise) Trade-off triangle of differential amplifiers has been identified
 - ... in reality, one has even an octagon (see literature [1-3])



➤ Now, the differential amplifier is going to be designed

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- Solve exercise I e-j
 - ETA: 30 min

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Exercise I

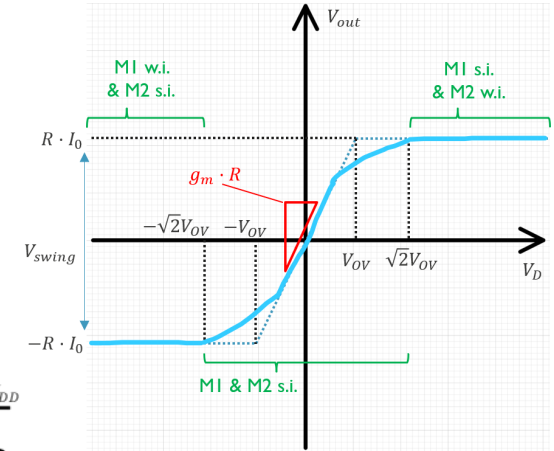
e) Give V_{swing} as a function of I_{bias} .

$$V_{GS3} = V_{GS4}$$

$$\Rightarrow \circ$$

$$\Rightarrow \frac{I_4}{I_3} = \frac{W_4}{W_3}$$

$$I_D = \frac{\mu C_{ox}}{2\alpha} \left(\frac{W}{L}\right) V_{OV}^2$$

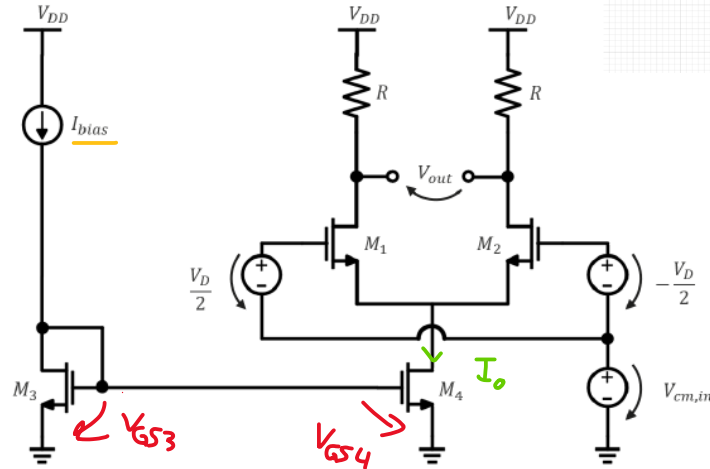


e) $V_{swing} = 2 \cdot R \cdot I_0$

current mirror equation (neglecting CLM):

$$\frac{I_0}{I_{bias}} = \frac{W_4}{W_3}$$

$$\Rightarrow V_{swing} = 2 \cdot R \cdot I_{bias} \cdot \left(\frac{W_4}{W_3}\right)$$

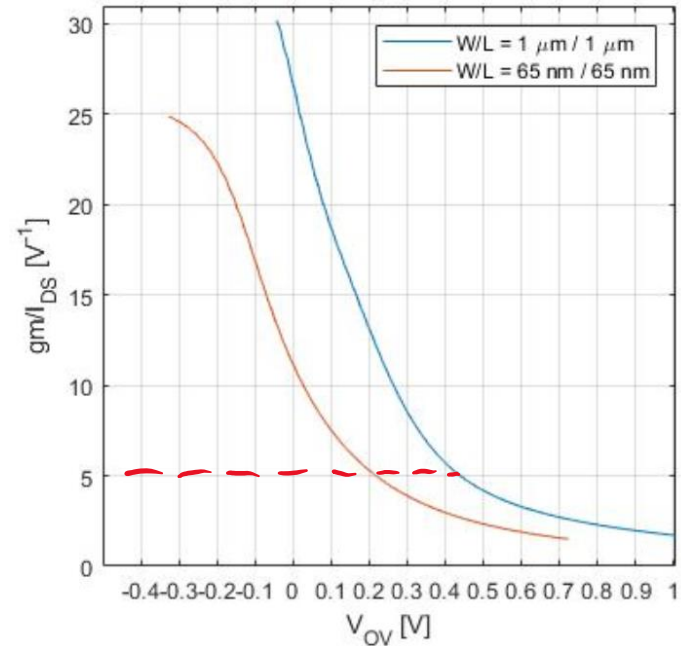


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Exercise I

f) Calculate, what $\frac{g_m}{I_D}$ is required to have exactly A_V and V_{swing} .

$$f) \quad \frac{g_{m_{1,2}}}{I_{D_{1,2}}} = \frac{g_{m_{1,2}}}{(I_0/2)} = \frac{g_{m_{1,2}} \cdot R}{(I_0 \cdot R/2)} = \frac{A_V}{\left(\frac{V_{swing}}{2}\right)/2} = \frac{A_V}{V_{swing}/4} = 4 \cdot \frac{A_V}{V_{swing}} = 5$$



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Exercise I

g) Calculate R and g_m such that this circuit passes exactly the V_{swing} , P_{diss} and A_V -specification.

g) First, calculate the max. allowed current

$$P_{diss} = V_{DD} \cdot (I_0 + I_{bias})$$

$$\Leftrightarrow I_0 = \frac{P_{diss} - V_{DD} \cdot I_{bias}}{V_{DD}} \approx 1mA$$

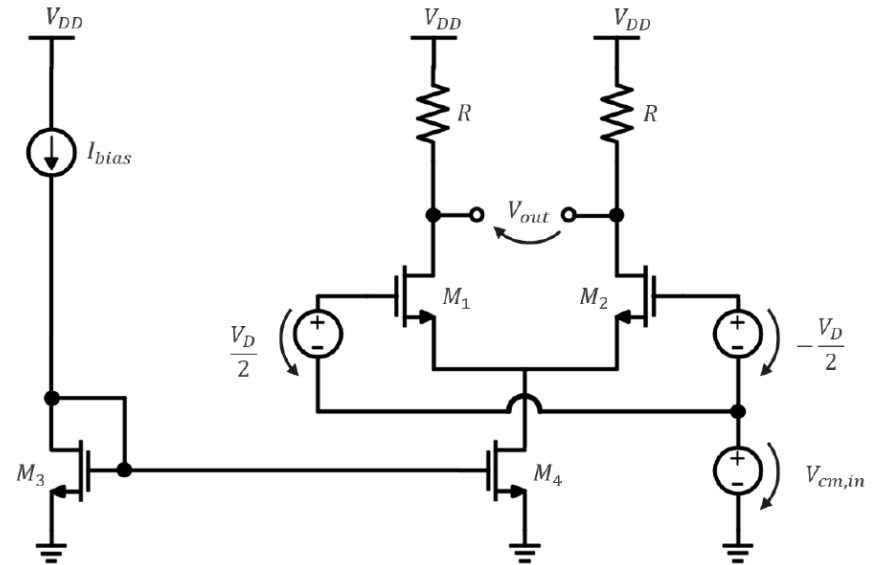
Then, calculate $g_{m_{1,2}}$

$$g_{m_{1,2}} = \left(\frac{I_0}{2}\right) \cdot 5 = 2.5mS$$

Now, calculate R

$$A_{V,diff} = g_{m_{1,2}} \cdot R$$

$$\Leftrightarrow R = \frac{A_{V,diff}}{g_{m_{1,2}}} = 400 \Omega$$



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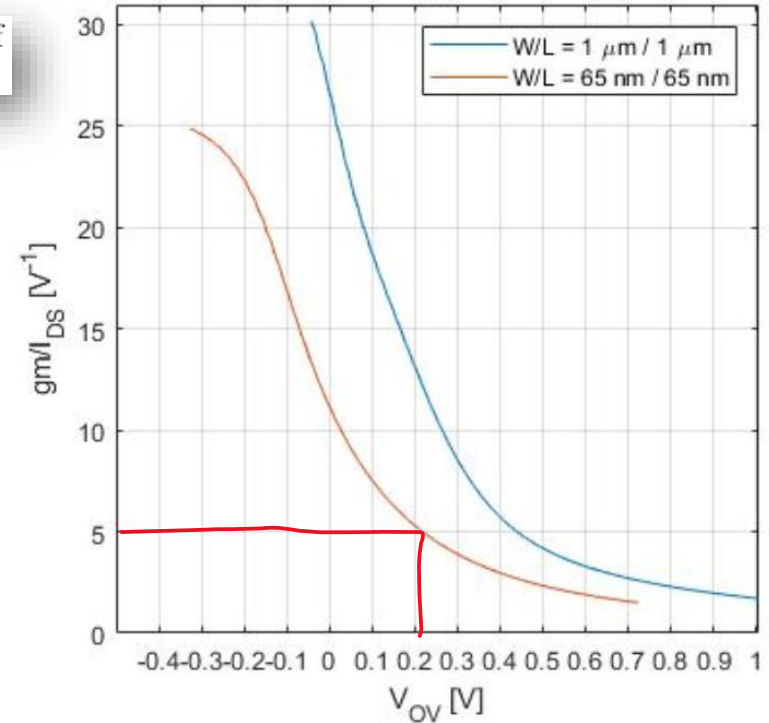
Exercise I

h) Calculate the required width W_1 and W_2 as well as L_1 and L_2 with aid of Fig. 5 and Fig. 6.

h) Reminder: $\frac{g_{m_{1,2}}}{I_{D_{1,2}}} = \underline{5}$

Set length to minimum, i.e. $L_{1,2} = 65\text{nm}$ ($f_T \sim \frac{1}{L^2}$)

Determine $V_{OV} \rightarrow 0.2\text{V}$



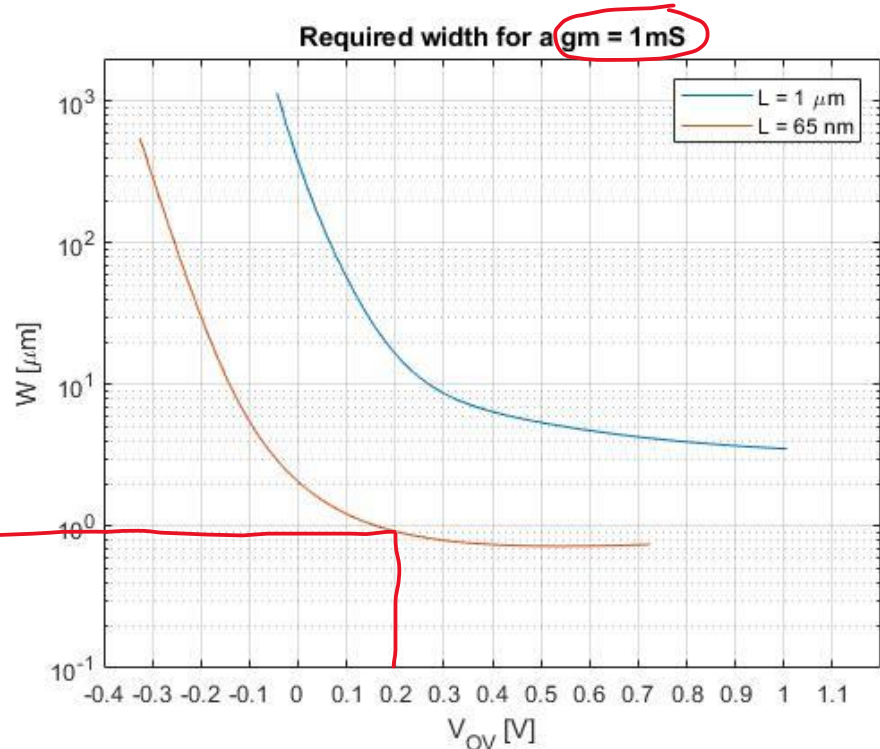
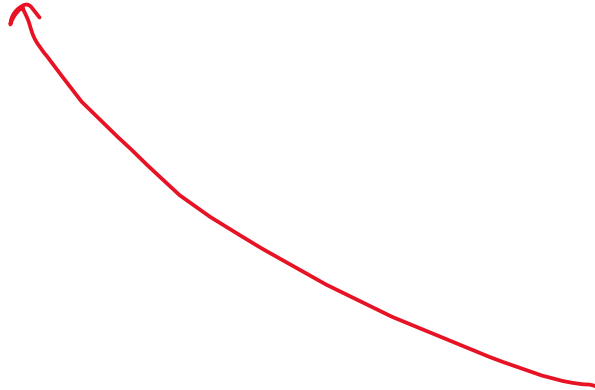
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Exercise I

h) Now determine the width $W_{1,2}$ at $V_{OV} = 0.2V$

from g): $g_m = 2.5mS = 2.5 \cdot \underline{1mS}$

$\Rightarrow 0.9\mu m \cdot \underline{2.5} = 2.25 \mu m$



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Exercise I

$V_{Dsat} \approx V_{OV}$ (very pessimistic assumption)

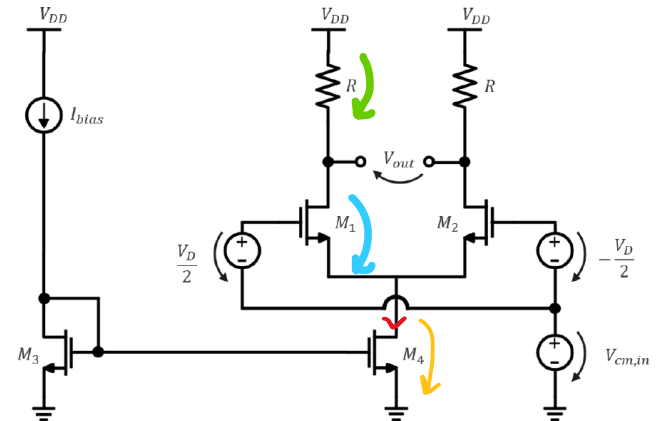
- i) Decide what length L_1 , L_2 and V_{OV} you would choose for M_3 and M_4 . Explain why? Then, calculate the width W_3 and W_4 with aid of Fig. 6.

- i) $L_{3,4} = 1\mu m$ to have negligible CLM (good current source)

Then, decide for a suitable value for $V_{OV_{3,4}} \rightarrow 0.3 V$

to ensure saturation for all M_x :

$$\underline{V_{OV,3,4}} + \underline{V_{OV,1,2}} + \underline{\frac{V_{swing}}{2}} \leq V_{DD}$$



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Exercise I

i) Calculate the width $W_{3,4}$

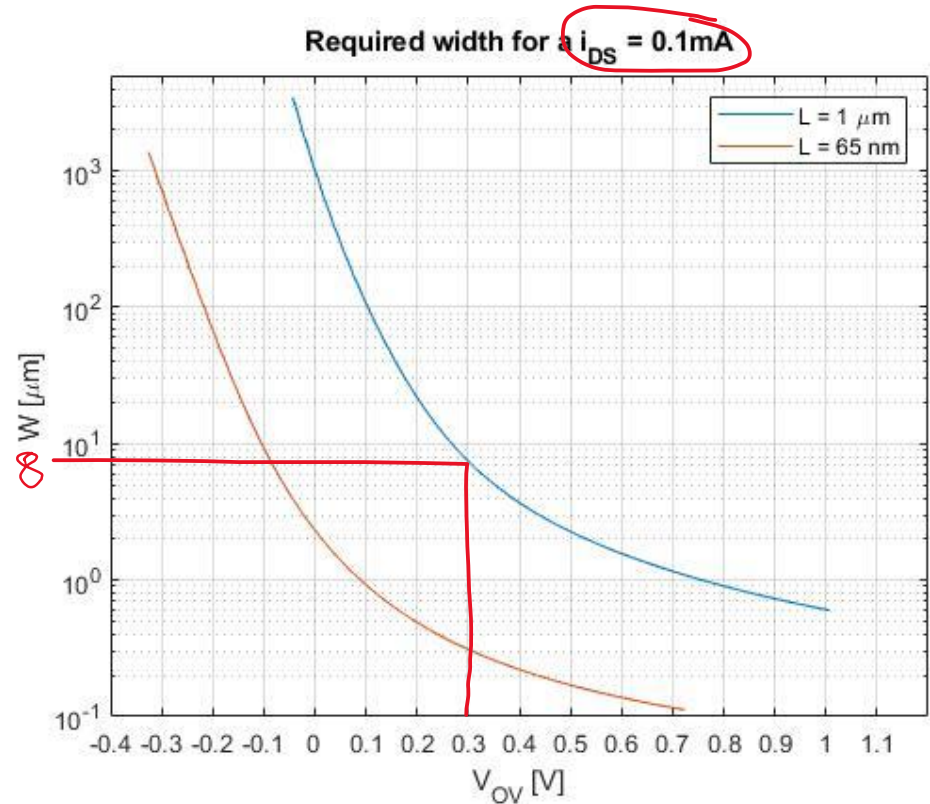
from g):

$$\begin{aligned} I_{DS,4} &= I_0 \\ &= 1mA = 10 \cdot 0.1mA \end{aligned}$$

$$\Rightarrow 8 \mu m \cdot 10 = 80 \mu m$$

Then, with current mirror equation
determine W_3

$$\frac{I_0}{I_{bias}} = \frac{W_4}{W_3} \Leftrightarrow W_3 = \frac{W_4}{(I_0/I_{bias})} = \frac{W_4}{10} = 8 \mu m$$



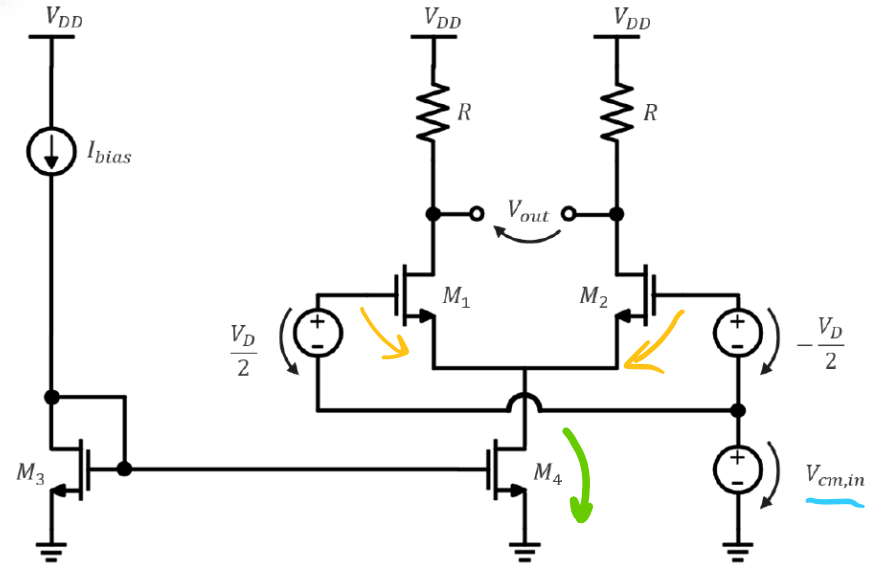
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Exercise I

- j) Calculate the minimum allowed input common mode voltage $V_{cm,min,in}$.
What happens, if one sets $V_{cm,in} < V_{cm,min,in}$?

j) $V_{cm,in,min}$ calculated as follows

$$\begin{aligned}\underline{V_{cm,in,min}} &= \underline{V_{Dsat4}} + \underline{V_{GS1,2}} \\ &= \underline{V_{Dsat4}} + \underline{V_{OV1,2}} + \underline{V_{th,n}} \\ &= \underline{0.3V} + 0.2V + 0.4V = 0.9V\end{aligned}$$



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Exercise I

j) What happens, if $V_{cm} < V_{cm,in,min}$?

→ drives M4 into triode ...

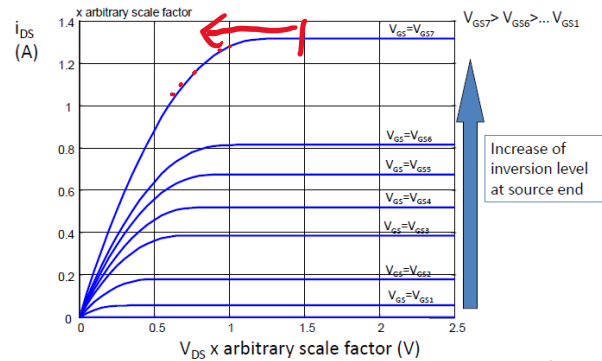
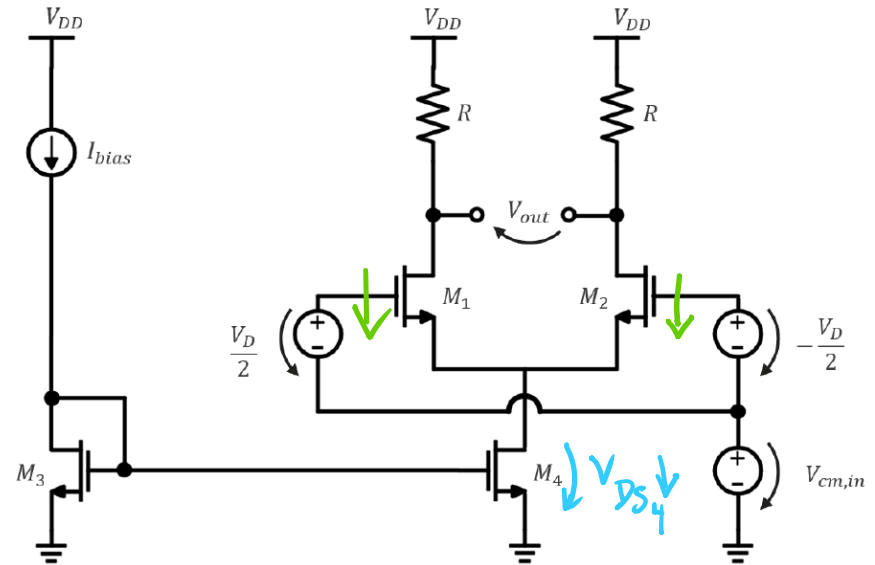


Figure 1.17: Drain current I_{DS} as a function of V_{DS} for different V_{GS} values. The flat behavior, starting at the onset of saturation, is an idealized representation, that will be refined below.



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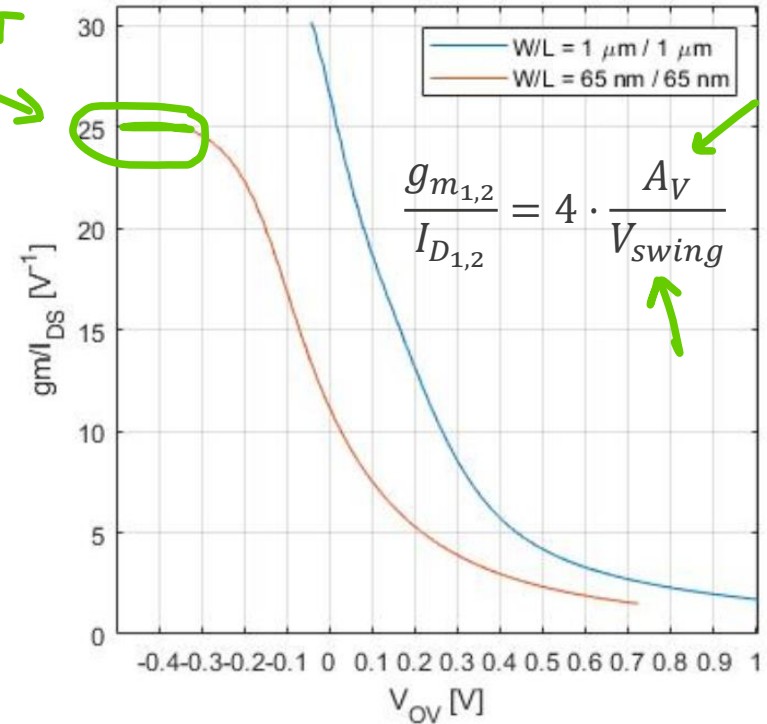
Summary

side note:

$$\frac{g_m}{I_D} = \frac{1}{n V_T}$$

$n = 1,5$

- Value the $\frac{g_m}{I_D}$ -plot !
 - With $\frac{g_m}{I_D}$ one can identify the entire trade-off in one plot !



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- Solve exercise 2 a-e
 - ETA: 25 min

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Exercise 2

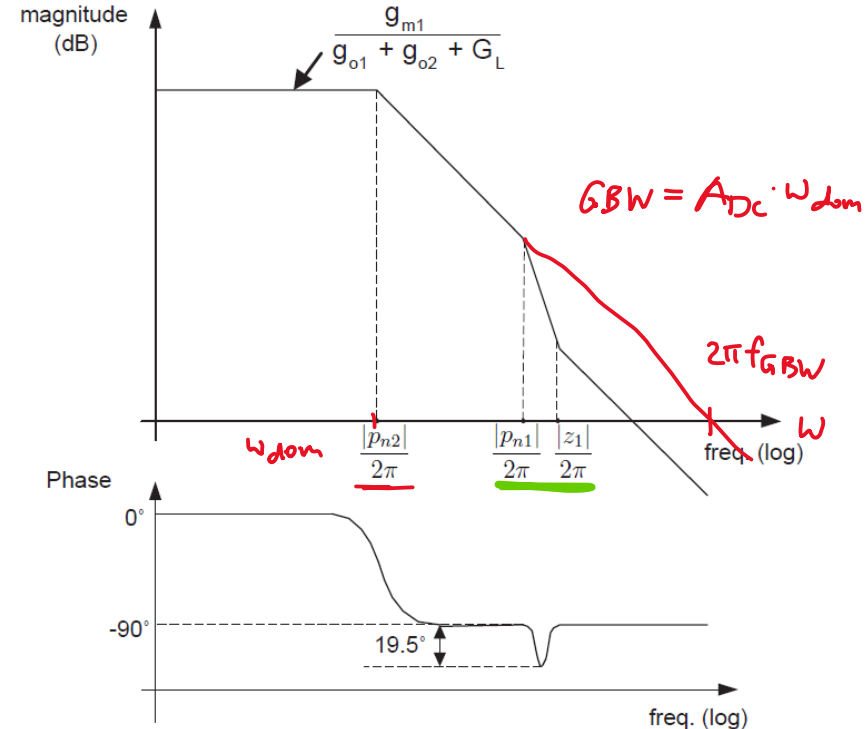
- a) Give the small signal voltage gain equation of this circuit including the capacitances and indicate
- dominant pole,
 - non-dominant pole,
 - zero.
- b) Assume the pole-zero-doublet to be far away from the dominant pole. Draw the bode- and phase plot and indicate location of the dominant pole and GBW.

a)

$$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m,1,2}}{g_{o2} + g_{o6}} \cdot \frac{1 + s \frac{C_{d1,5}}{2gm_5}}{1 + s \frac{C_{d1,5}}{gm_5}} \cdot \frac{1}{1 + s \frac{C_{d2,6}}{g_{o2} + g_{o6}}}$$

zero
non-dominant pole
dominant pole

b) see drawing



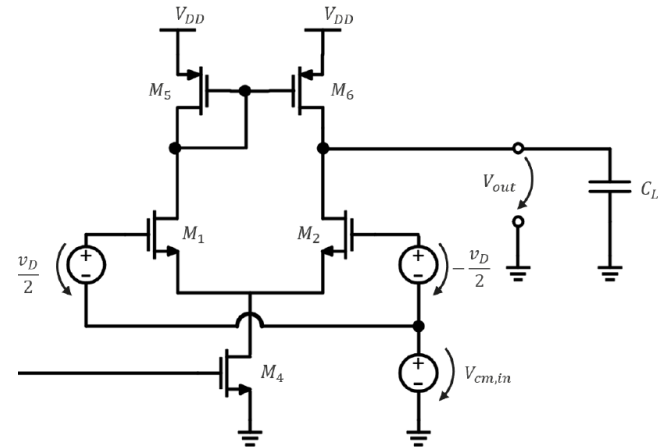
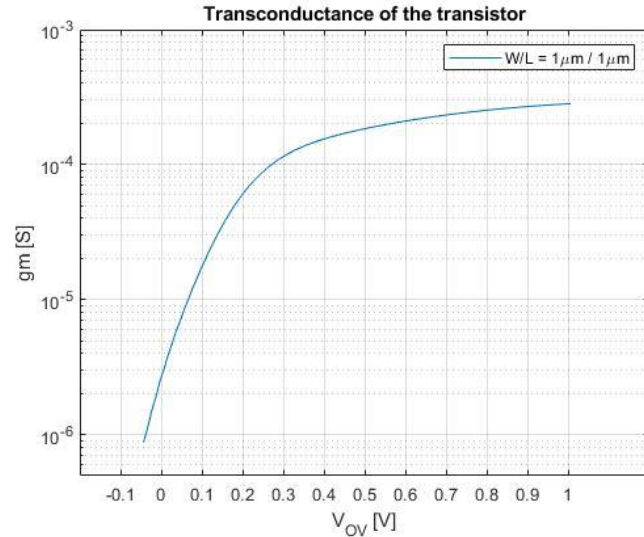
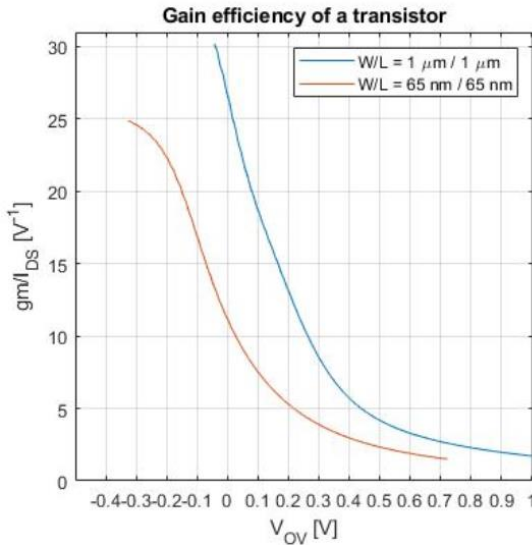
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Exercise 2

- c) What happens to the pole-zero-doublet, if one increases/decreases the V_{OV} of M_5 and M_6 assuming that the current flowing through M_4 is fixed as well as the lengths are fixed?

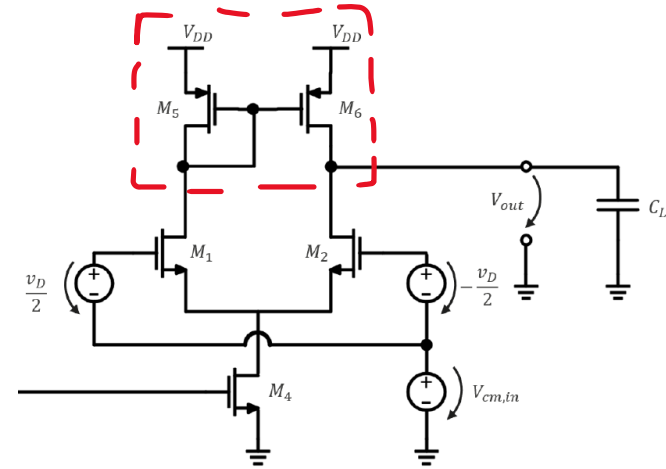
$$c) \quad p_{non-dom} \sim \frac{g_{m5}}{C_{gs5,6}}$$

$$V_{OV,5} \uparrow \Rightarrow g_{m5} ? \Rightarrow p_{non-dom} ?$$



Exercise 2

$$I_{DS} = \mu C'_{ox} \cdot \frac{W}{2L} \cdot V_{OV}^2$$

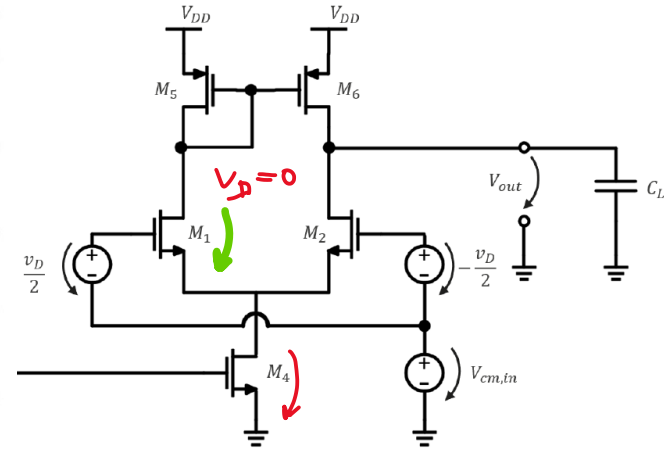
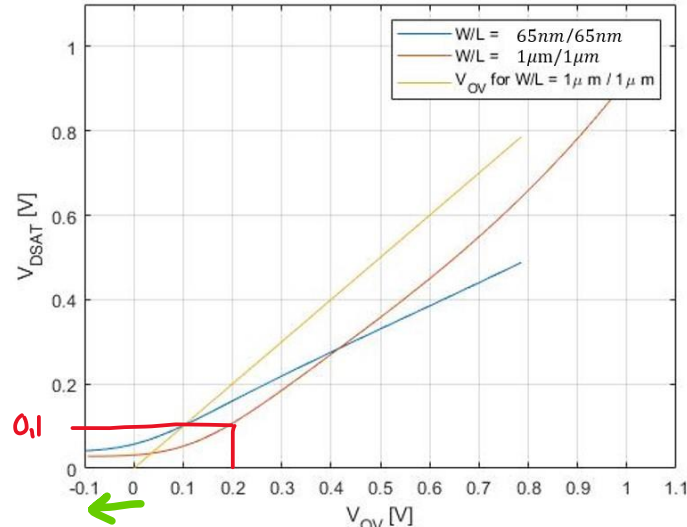


Exercise 2

- d) Assume $V_{OV,3,4} = 0.2V$, $V_{Dsat,5,6} = -0.25V$ and $V_{OV} < -0.1V$ for the remaining devices. With aid of Fig. 9, calculate the maximum/minimum possible output common mode voltage $V_{cm,max,out}$ and $V_{cm,min,out}$, where all transistors are still in saturation.

- d) Calculate $V_{out,cm,min}$
(for $V_{OV,4} = 0.2V$ and
remaining $V_{OV} < 0V$)

$$V_{out,cm,min} = \underline{V_{Dsat,4}} + \underline{V_{Dsat,1,2}}$$
$$= \underline{0.1V} + \underline{0.05V} = 0.15V$$

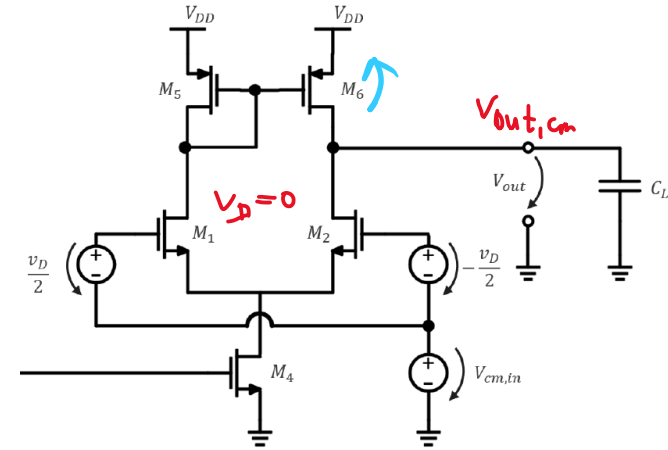
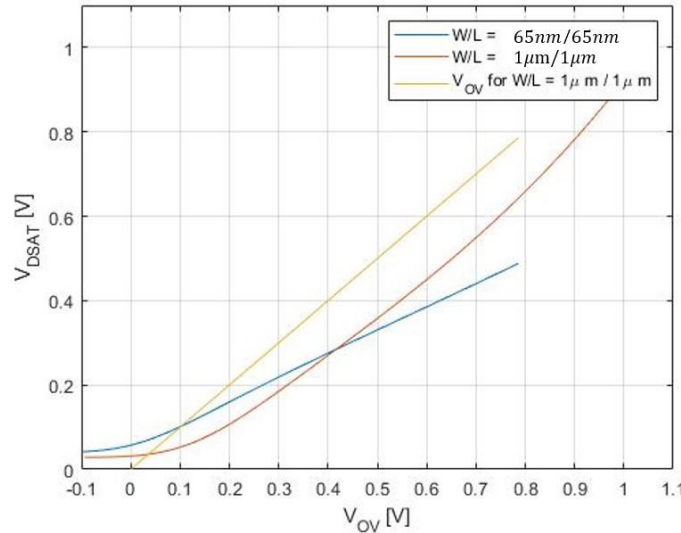


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Exercise 2

- d) Calculate $V_{out,cm,max}$ (for $V_{OV,4} = 0.2V$ and $V_{Dsat,5,6} = -0.25V$)

$$\begin{aligned}\underline{V_{out,cm,max}} &= V_{DD} + \underline{V_{Dsat,5,6}} \\ &= 1.1V - 0.25V = \underline{0.85V}\end{aligned}$$



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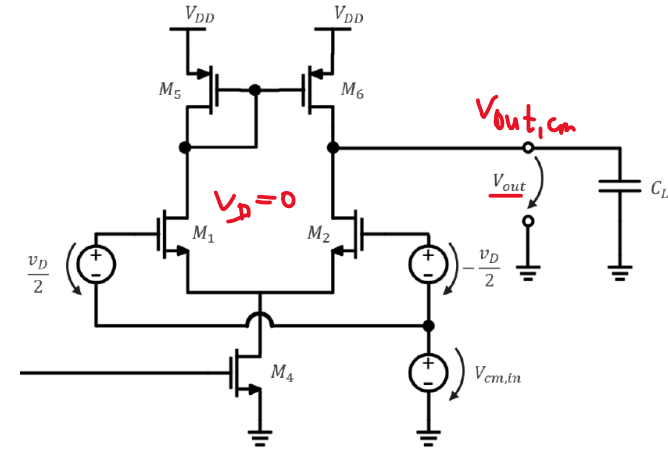
Exercise 2

- e) The designer decides to set the output common mode voltage for $v_D = 0$ to the midpoint between $V_{cm,max,out}$ and $V_{cm,min,out}$. Explain how and calculate for that the required V_{OV} .
Hint: Examine the PMOS pair for $v_D = 0$.

- e) $V_{out,cm}$ calculated as follows

$$\underline{V_{out,cm}} = \frac{V_{out,cm,max} + V_{out,cm,min}}{2} = 0.5V$$

How to setup $V_{out,cm}$ in OTA's ?

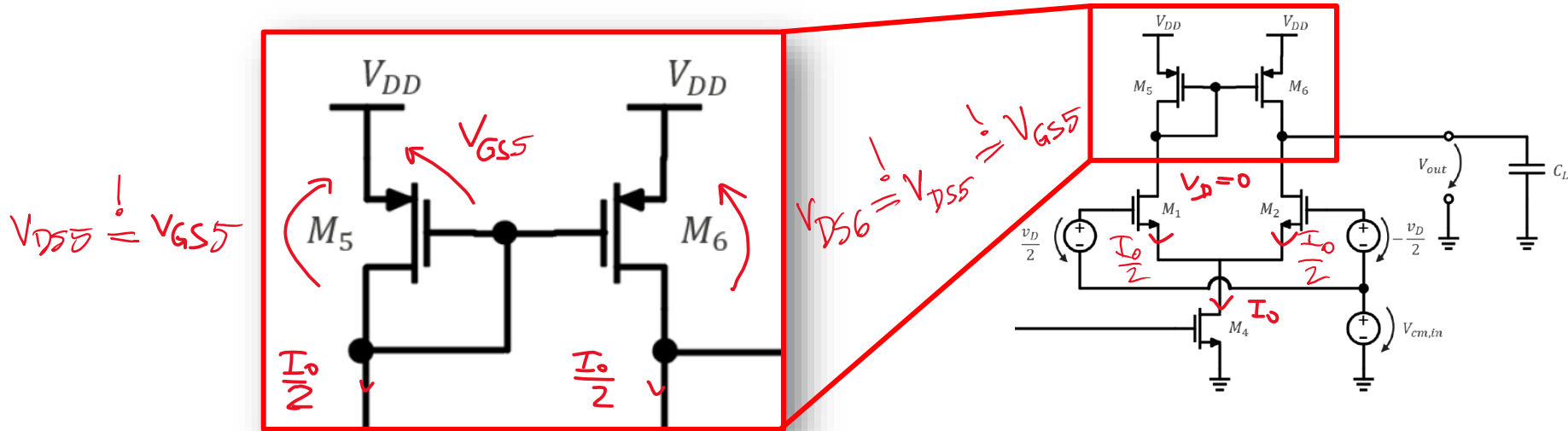


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Exercise 2

e)
$$V_{out,cm} = \frac{V_{out,cm,max} + V_{out,cm,min}}{2} = 0.5V$$

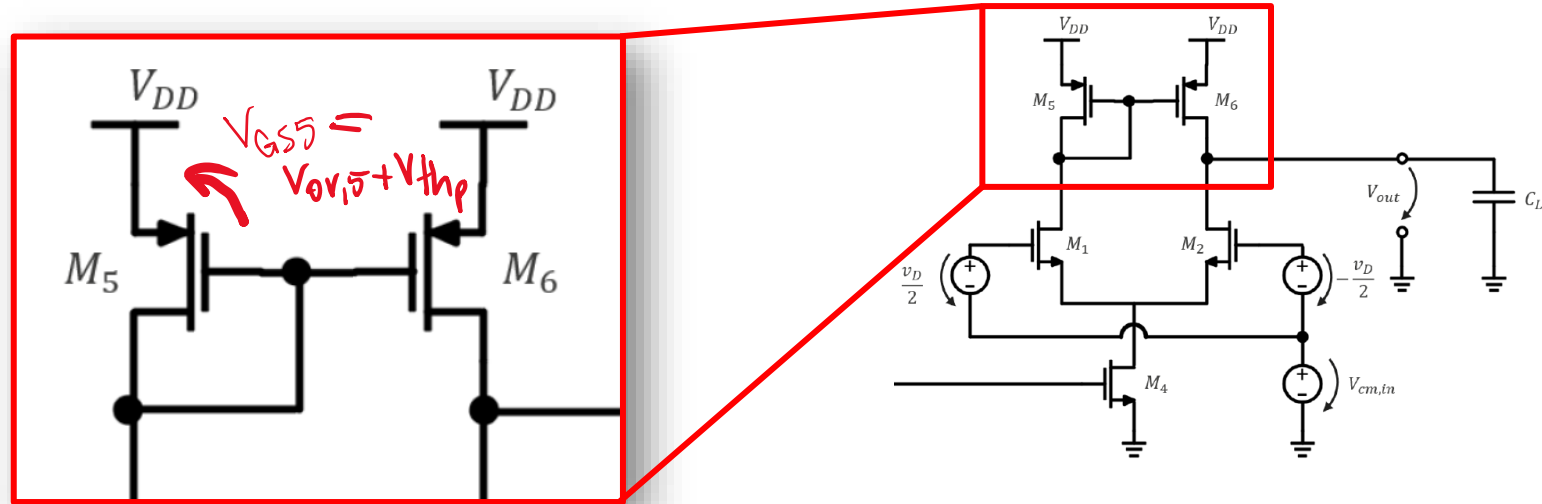
How to setup $V_{out,cm}$ in OTA's ?



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Exercise 2

e) Consequently, $|V_{OV,5}| = \underline{V_{DD}} - \underline{V_{out,cm}} - \underline{|V_{th,p}|} = \underline{\underline{0.38V}}$



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- Solve exercise 2 f-i
 - ETA: 20 min

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Exercise 2

f) Find and explain a suitable simplification of the equation from "a)" such that Fig. 8 becomes useful for designing the OTA. Then, calculate the required V_{OV} and $V_{in,cm,min}$ for M_1 and M_2 to achieve $A_V > 8$.

f) How to simplify $A_V(s=0)$?

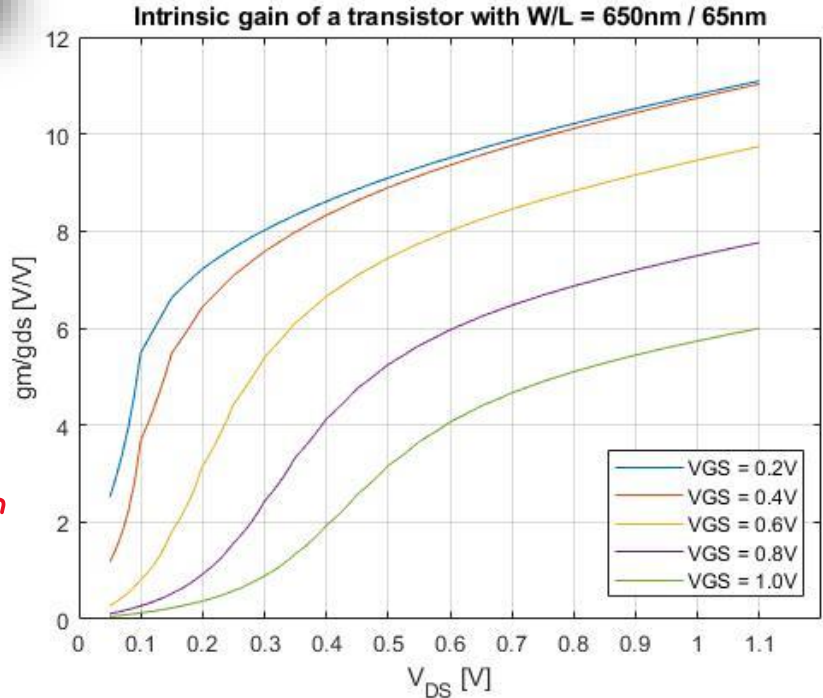
$$A_v(s) = \frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m,1,2}}{g_{02} + g_{06}} \cdot \frac{1 + s \frac{C_{d1,5}}{2g_{m5}}}{1 + s \frac{C_{d1,5}}{g_{m5}}} \cdot \frac{1}{1 + s \frac{C_{d2,6}}{g_{02} + g_{06}}}$$

zero
non-dominant pole
dominant pole

⇒ make $L_{5,6} = 1\mu m$ for negligible CLM

⇒ $g_{02} \gg g_{06}$

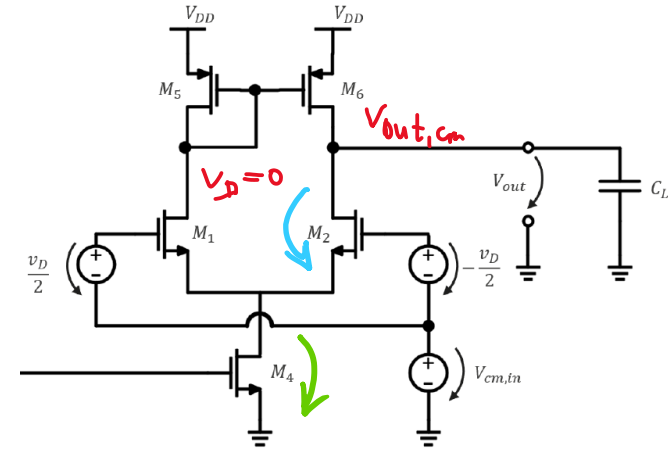
$$A_V(s=0) \approx \frac{g_{m,1,2}}{g_{02}}$$



Exercise 2

f) $V_{DS,2}$ calculated as follows

$$\underline{V_{DS,2}} = \underline{V_{out,cm}} - \underline{V_{Dsat,4}} = 0.5 - 0.1V = 0.4V$$



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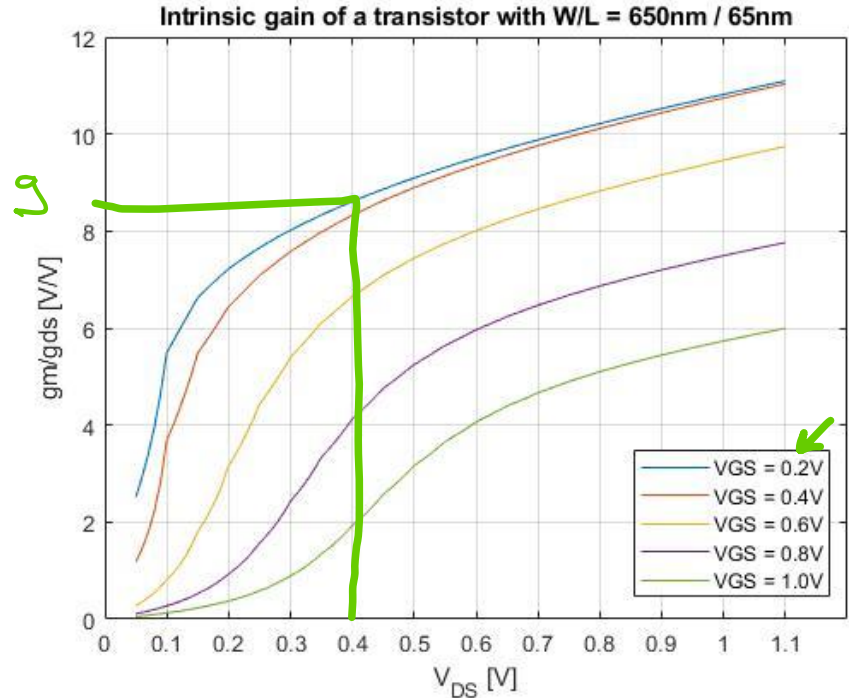
Exercise 2

f) Search $V_{OV,1,2}$ for $A_V(s = 0) > 8$

$$\rightarrow V_{GS,1,2} = 0.2V \rightarrow A_V \sim 9 \leftarrow$$

$$\rightarrow \underline{V_{OV,1,2}} = V_{GS,1,2} - V_{th,n} = -0.2V$$

$$\rightarrow V_{in,cm} = V_{GS,1,2} + V_{Dsat,4} = 0.3V$$



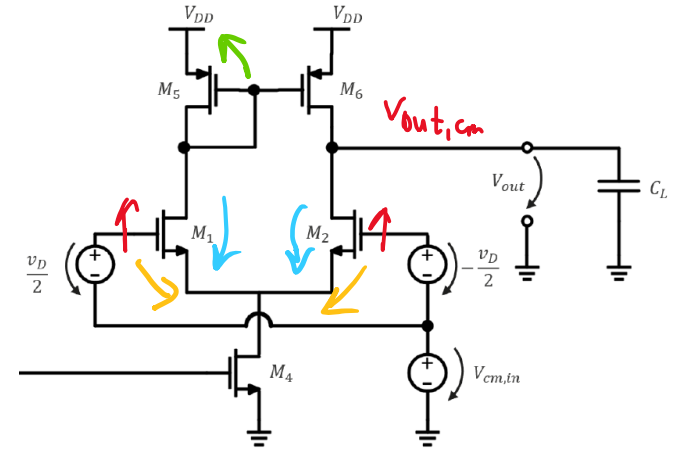
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Exercise 2

g) Calculate $V_{in,cm,max}$.

g) $V_{in,cm,max}$ calculated as follows:

$$\begin{aligned} V_{in,cm,max} &= \underbrace{V_{DD}}_{\text{red}} + \underbrace{V_{GS,5}}_{\text{green}} - \underbrace{V_{DSat,1,2}}_{\text{blue}} + \underbrace{V_{GS,1,2}}_{\text{yellow}} \\ &= V_{out,cm} - \underbrace{V_{DSat,1,2}}_{\text{blue}} + \underbrace{V_{GS,1,2}}_{\text{yellow}} \\ &= \underbrace{0.5V}_{\text{red}} - \underbrace{0.05V}_{\text{blue}} + \underbrace{0.2V}_{\text{yellow}} = \underbrace{0.65V}_{\text{yellow}} \end{aligned}$$



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Exercise 2

h) Assume a current of I_0 is flowing through M_4 . Given that all transistors are in saturation, determine what current I_{CL} flows through C_L , if

- (i) $V_D = 0$,
- (ii) $V_D < -X$: M_1 is in weak inversion and M_2 in strong inversion,
- (iii) $V_D > X$: M_1 is in strong inversion and M_2 in weak inversion.

Moreover, determine X .

h) Following current I_{CL} flows through C_L given that all transistors are in saturation

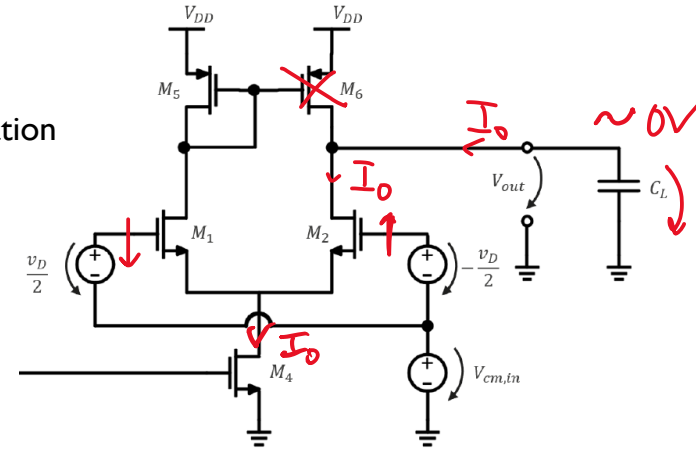
(i) $V_D = 0V : I_{CL} = 0A$

(ii) $V_D < -X : I_{CL} = -I_0$

(iii) $V_D > X : I_{CL} = I_0$

What is X ? $\sqrt{2} \cdot V_{OV}$?

$\rightarrow X = \sqrt{2} \cdot V_{Dsat,1,2} \sim 71 \text{ mV}$ (for $V_{OV,1,2} = -0.2V$)



Session 3 : Design of differential pairs and of an OTA

Exercise 2

i) Calculate the SR , the required I_0 and $g_{m,1,2}$ necessary to pass exactly the f_{GBW} -requirement with aid of Fig. 5. After that, calculate $g_{m,5,6}$.

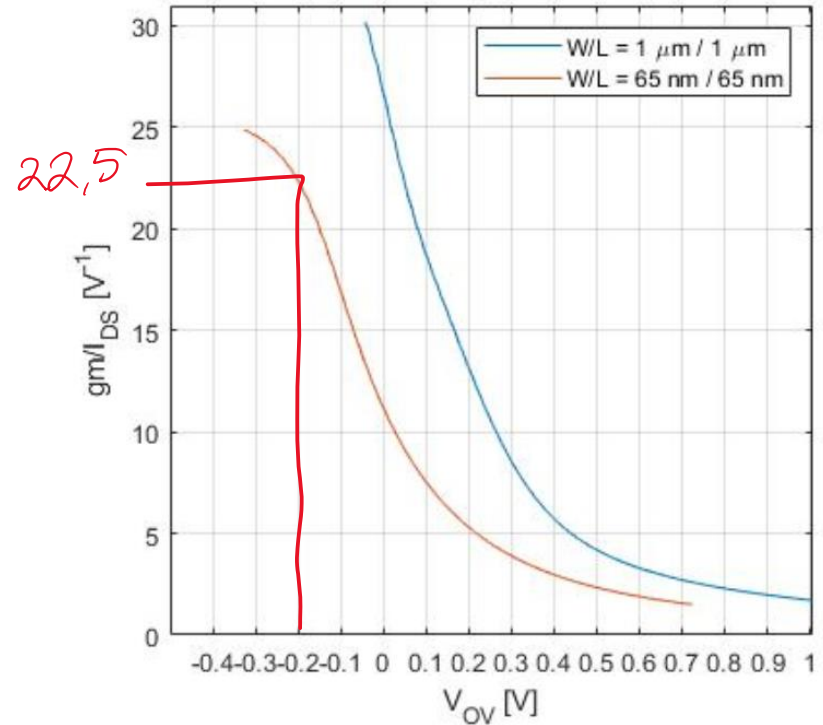
ii) Determine SR (Slew Rate) for given f_{GBW} -spec and $V_{OV,1,2}$

$$\frac{g_{m1,2}}{I_{D1,2}} = \frac{2\pi f_{GBW} \cdot C_L}{(I_0/2)} = 2 \cdot \frac{2\pi f_{GBW}}{SR}$$

$$SR = \frac{I_0}{C_L}$$

$$\rightarrow \frac{g_{m1,2}}{I_{D1,2}} = 22.5 \text{ for } V_{OV,1,2} = -0.2V$$

$$\rightarrow SR = 2 \cdot \frac{2\pi f_{GBW}}{22.5} = 400mV/ns$$



Session 3 : Design of differential pairs and of an OTA

Exercise 2

i) Calculate I_0 for M4

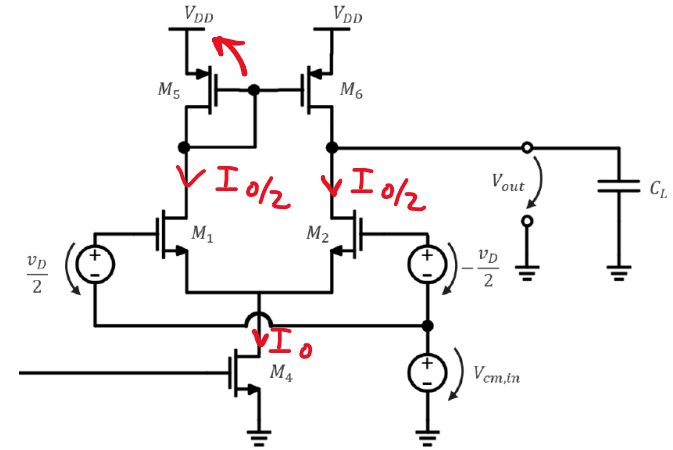
$$I_0 = SR \cdot C_L = 400\text{mV/ns} \cdot 500\text{fF} = 200\mu\text{A}$$

Determine $g_{m,1,2}$

$$g_{m,1,2} = 22.5 \cdot \left(\frac{I_0}{2}\right) = 2.25\text{mS}$$

Determine $g_{m,5,6}$

$$g_{m,5,6} = \frac{2 \cdot (I_0/2)}{V_{OV,5,6}} \approx 526\mu\text{S}$$

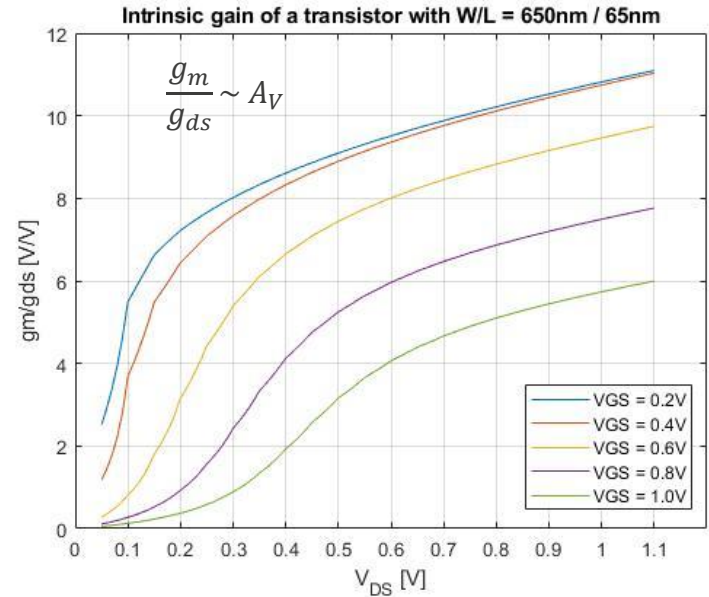
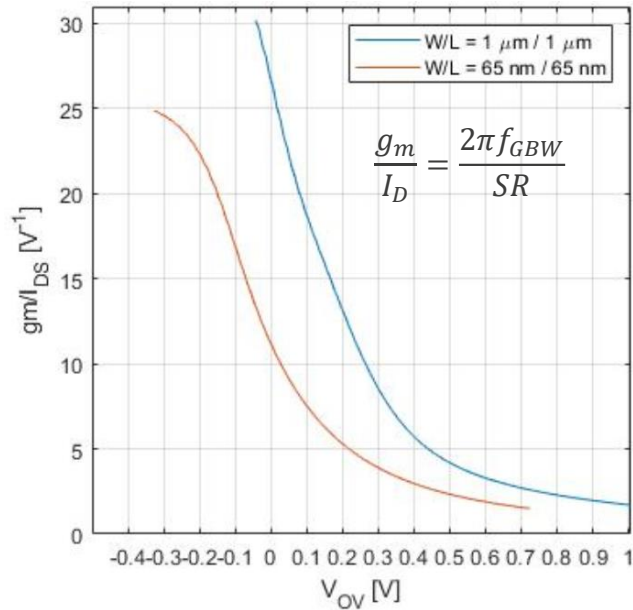


Session 3 : Design of differential pairs and of an OTA

Summary (I)

I. Value the $\frac{g_m}{I_D}$ - and $\frac{g_m}{g_{ds}}$ - plots!

- One can predict the feasibility of the given specifications for an OTA in one view



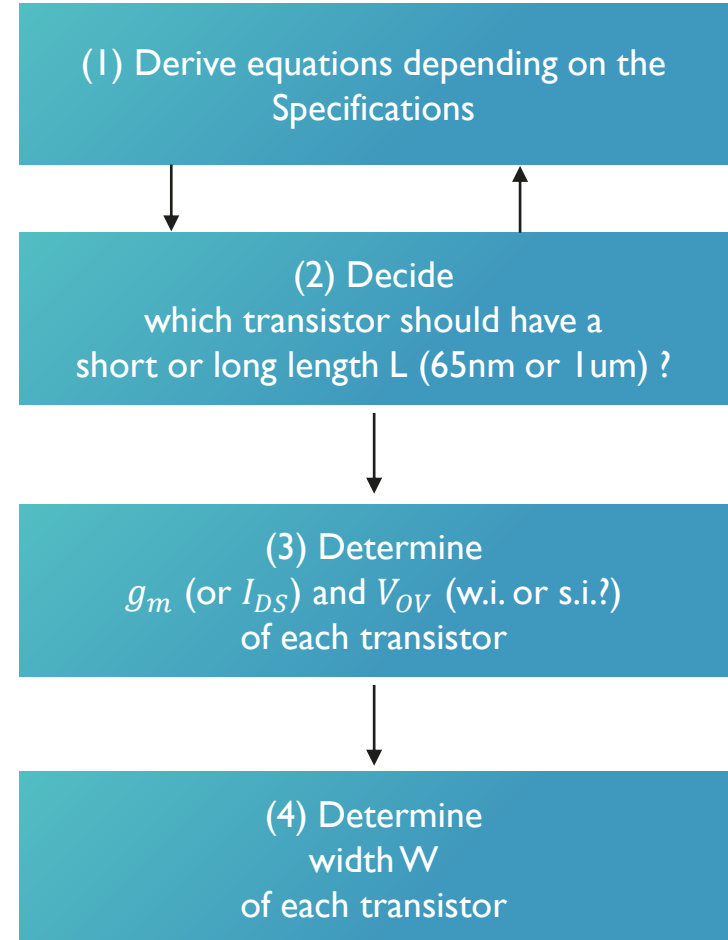
Session 3 : Design of differential pairs and of an OTA

Summary (2)

2. Design flow introduced

3. Learned how to “design on paper” with

- W -plot for fixed g_m or i_{ds}
- $\frac{g_m}{I_D}$ - and $\frac{g_m}{g_{ds}}$ -plots
- V_{dsat} -plot
- Those plots will help you to save time when designing for the final lab session!



Session 3 : Design of differential pairs and of an OTA

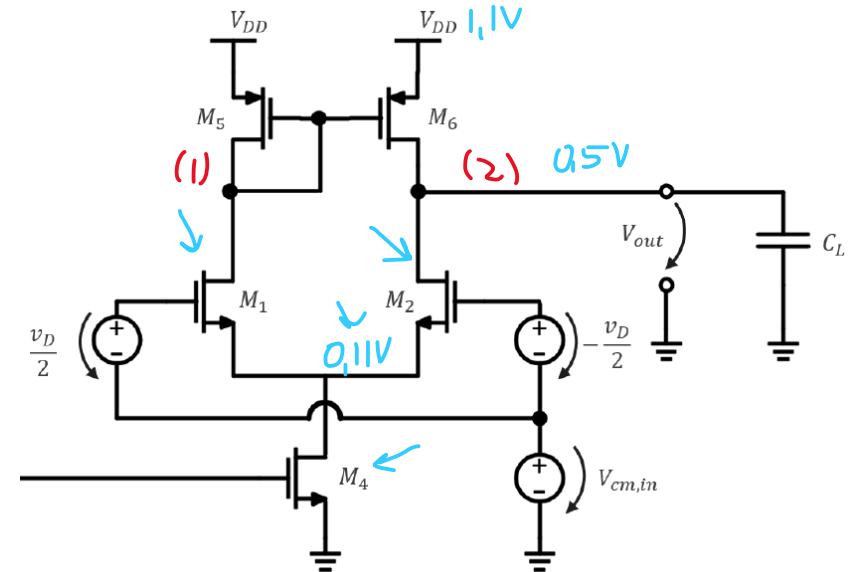
MATLAB session

■ Exercise 3

1. Type in the code accordingly to this presented OTA exercise
2. Solve following scientific questions?
 1. How can one move the pole-zero-doublet?
 - 2 options
 2. How can I increase the f_{GBW} ?
- ETA: 30 min

Hints:

1. Use the following command to copy transistors e.g. M1 and M2
 1. `M2 = cirElementCopy(M1, M2);`
2. Before coding, draw all voltage condition on the OTA-circuit
 - i.e. vgs, vgd, vds, ids (or gm) of each transistor !
 - This will help you to speed-up your coding
3. Code it smart !
 1. code it such that you can play around with the pole-zero doublet !



Session 3 : Design of differential pairs and of an OTA

... some helpful references

- [1]: “Analog Design Essentials”, Sansen, Willy M. C, 2006
- [2]: “Design of Analog CMOS Integrated Circuits”, Razavi, Behzad, 2016
- [3]: “Analysis and Design of Analog Integrated Circuits”, P. Gray, P. Hurst, S. Lewis and R. Meyer, John Wiley and Sons, 2009



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