ETRO ELECTRONICS & INFORMATICS

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Analog Electronics Exercises

session 2

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Exercise 1

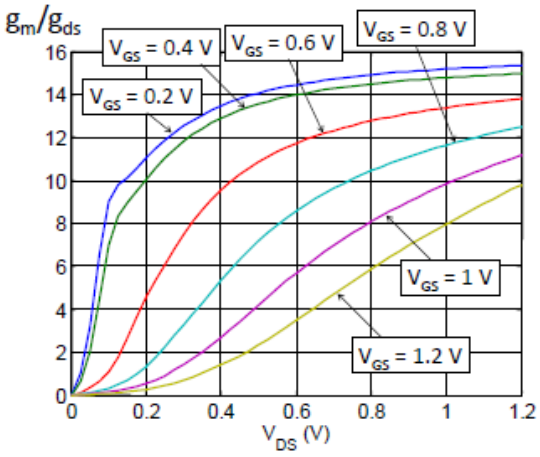


Figure 1: $g_m/g_{ds} \times V_{DS}$ curve taken from the class notes (Fig.1.32) showing the intrinsic gain as a function of V_{DS} for different V_{GS} values for a minimum-length transistor of a $90nm$ process with $V_{SB} = 0V$. Note that V_{th} is around $320mV$.

Assume that we utilize $90nm$ CMOS technology whose $g_m/g_{ds} \times V_{DS}$ curve for the minimum-length transistor is given above. Suppose that the size of the transistor is fixed.

a) What is the highest gain we can achieve with a single stage using this transistor technology?

b) What is the highest gain for the highest speed that we can attain with the $90nm$ process?

c) How can we increase the gain further beyond the technology limits?

Exercise 2

The following circuit is given. Assume that all transistors are in saturation mode, and neglect the g_{ds} of transistors. You can also neglect the extrinsic and intrinsic capacitors of transistors which are not given in the question. ($R_S = 500\Omega$, $R_1 = 5k\Omega$, $R_L = 500\Omega$, $g_{m1} = 2mA/V$, $g_{m2} = 20mA/V$, $C_L = 1.1pF$, $C_{gs1} = 20fF$, $C_{gd1} = 10fF$, $C_{gs2} = 30fF$, $C_{gd2} = 15fF$)

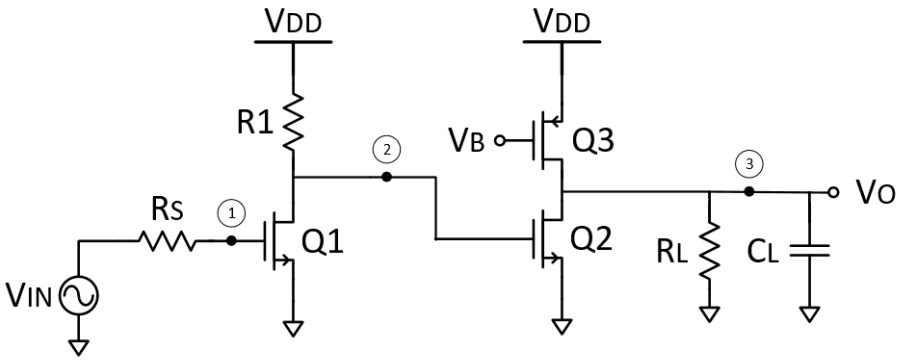


Figure 2: Two cascaded common source stages.

a) Calculate the DC gain of the circuit.

b) Find the values of existent poles in rad/s. You can neglect zeros since they are far away from w_T.

c) Calculate the phase margin.

Exercise 3

Add the capacitor C_c between the gate and drain of Q_2 to improve the phase margin of the circuit in Exercise 2 by Miller compensation.

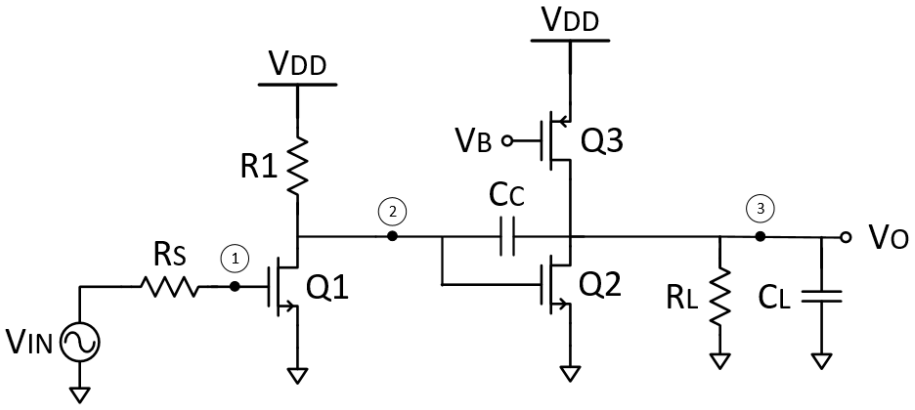


Figure 3: Two cascaded common source stages with Miller compensation.

a) Calculate the value of C_c which makes the amplifier to have a uniform $-20dB/decade$ gain rolloff with a unity gain frequency w_T of $2Grad/s$. It means that there will be only one pole whose frequency lower than w_T.

b) Calculate the resultant phase margin. Do not forget to take into account the right half-plane zero occurs in the second stage since it will get closer to w_T due to the Miller compensation.

Exercise 4

Add a resistance R in series with C_c to improve the phase margin we obtained in Exercise 3.

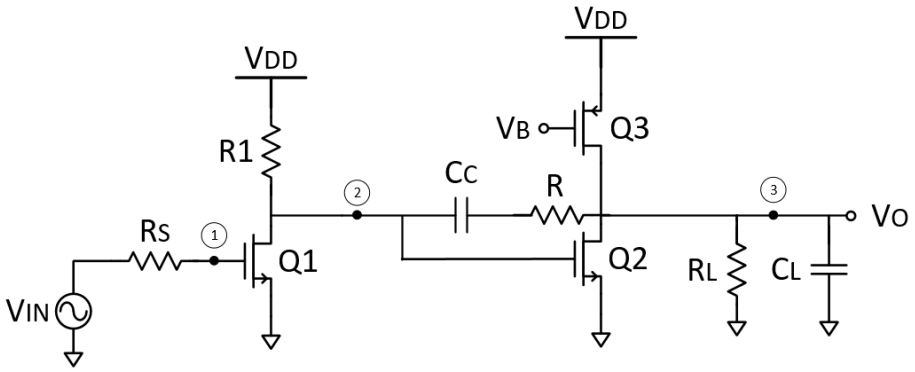
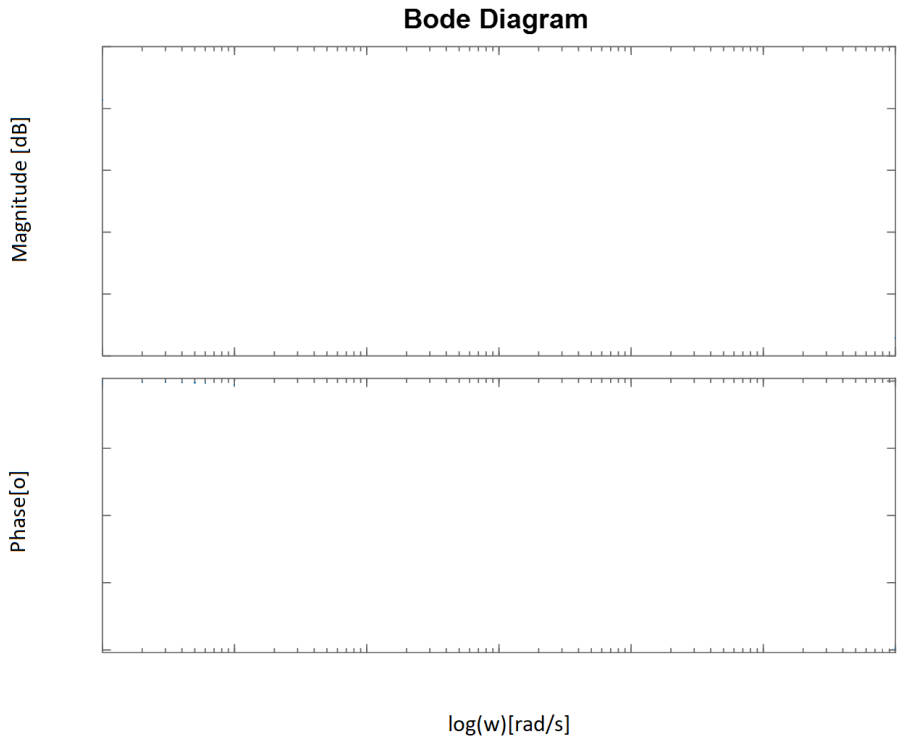
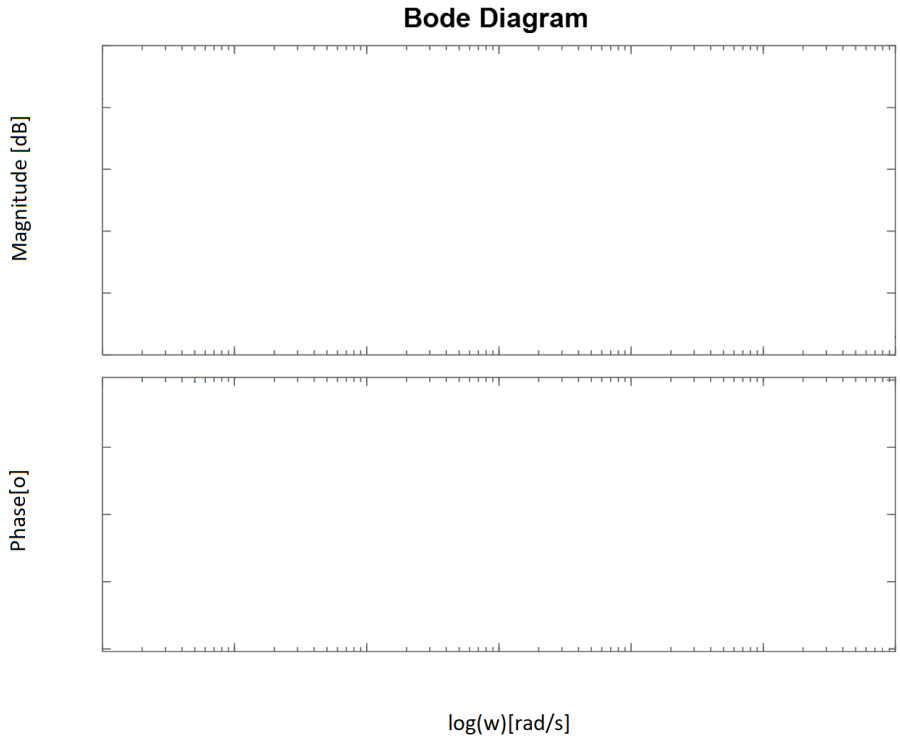


Figure 4: Two cascaded common source stages with added R in series with C_C.

a) What value of R is needed to remove the first non-dominant pole by shifting the zero to the same frequency as the pole?

b) Calculate the new phase margin obtained after adding R.


Bode Diagram
Magnitude [dB]
Phase[o]
log(w)[rad/s]


Bode Diagram
Magnitude [dB]
Phase[o]
log(w)[rad/s]