Analog Electronics Exercises

session 3

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Exercise 1

In Fig. 1 a differential pair with resistive load is given. Assume for simplicity that in this circuit the bulks of M_1 and M_2 are connected to their source connections thanks to triple-well-technology. Moreover, assume for $V_D = 0V$ that M1 and M2 are in strong inversion and assume $V_{Dsat} = V_{OV}$.

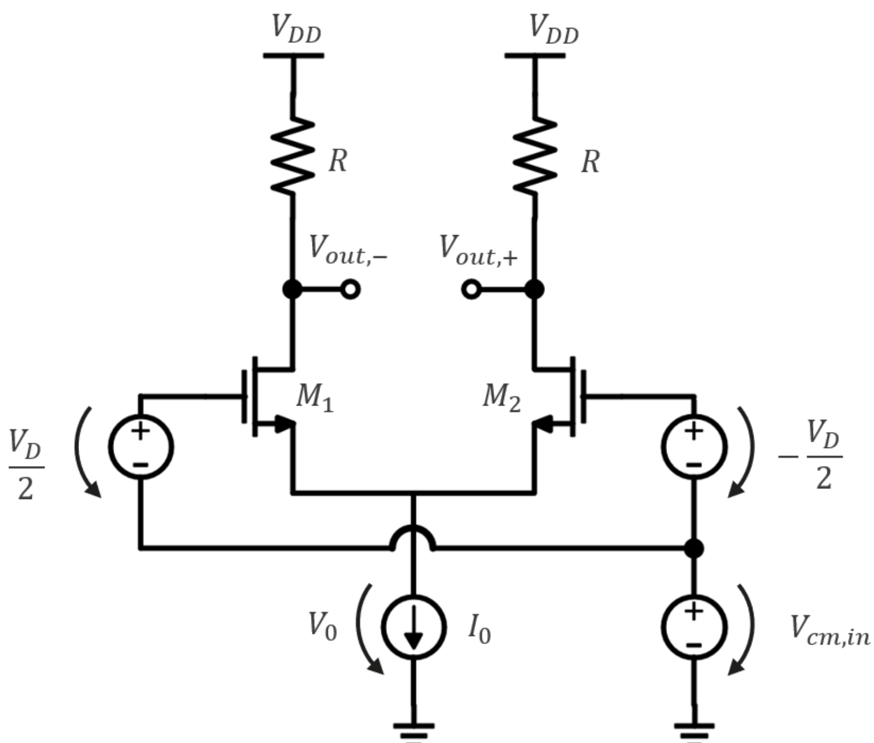


Figure 1: Differential amplifier with ideal current source

a) Give the equation of the small signal voltage gain $\frac{v_{out,-}}{v_D}$, $\frac{v_{out,+}}{v_D}$ and the differential voltage gain, when $V_D = 0$?

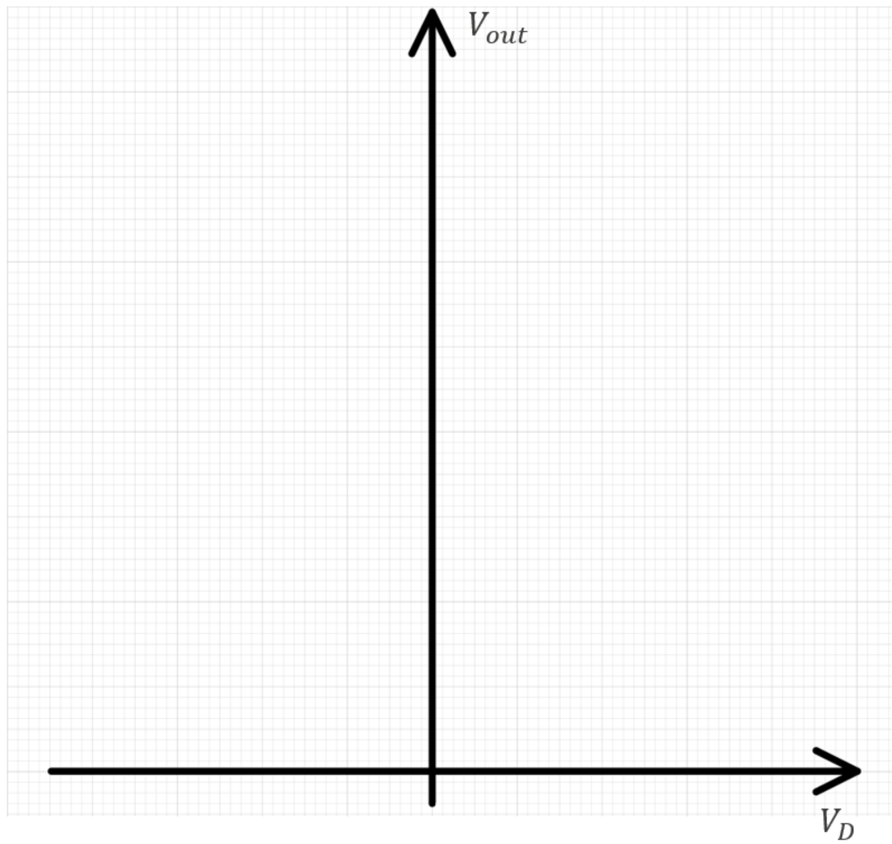


Figure 2: V_{out} as a function of v_D

b) Draw on Fig. 2 the voltages $V_{out,+}$, $V_{out,-}$ and V_0 and on Fig. 3 ($V_{out,+} - V_{out,-}$) qualitatively. Moreover, indicate on both figures:

(i) V_{OV} and $\sqrt{2}V_{OV}$,

(ii) A_V,

(iii) range, where M_1 and M_2 are in strong inversion,

(iv) range, where M_1 is in weak inversion, but M_2 in strong inversion,

(v) range, where M_1 is in strong inversion, but M_2 in weak inversion.

c) Give the amount of current, which is flowing through M_1 and M_2, when

(i) $V_D = 0$,

(ii) $V_D < -\sqrt{2} \cdot V_{OV}$,

(iii) $V_D > \sqrt{2} \cdot V_{OV}$.

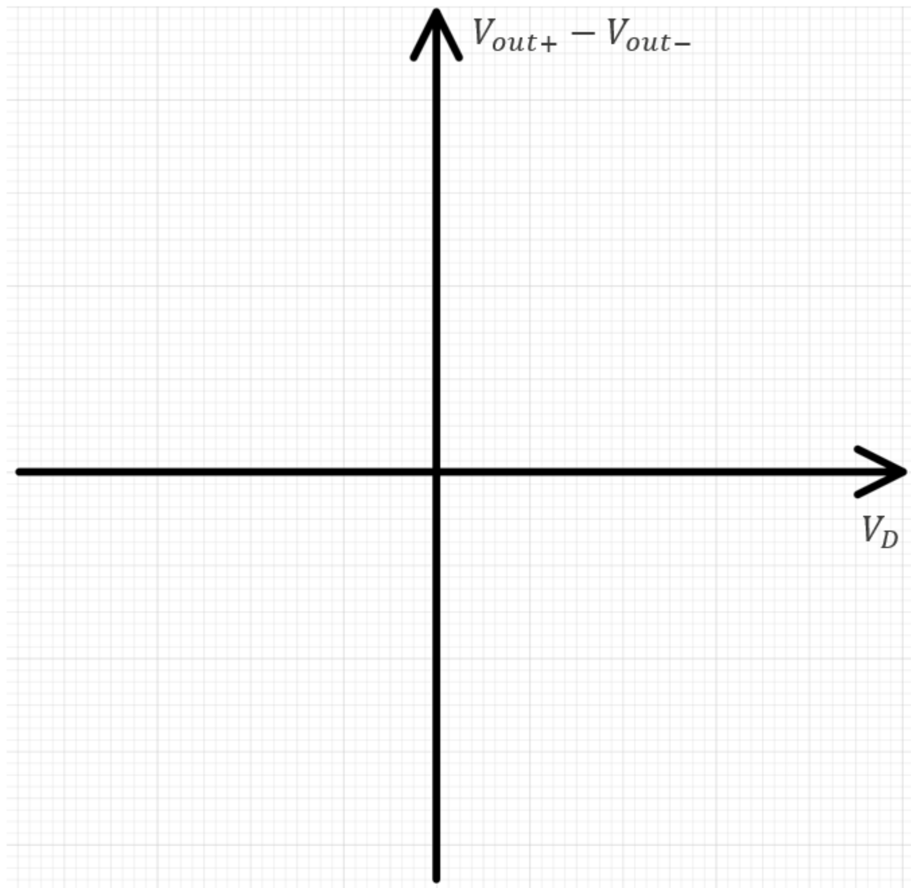


Figure 3: V_{out} as a function of v_D

d) Based on Fig. 3, derive an equation describing the relationship between V_{swing}, V_{OV} and A_V.
Remark: $V_{swing} = max(V_{out,+} - V_{out,-}) - min(V_{out,+} - V_{out,-})$

Now the considered circuit is extended with a current mirror (Fig. 3) and your employer mandates the following specifications:

- $P_{diss} = 1.2mW$;
- $V_{swing} = 0.8V_{pp}$;
- $A_V = 0dB$;
- $V_{DD} = 1.1V$;
- $V_{th,n} = 0.4V$;
- $I_{bias} = 100\mu A$.

Moreover, assume for simplicity that that $V_{Dsat} = V_{OV}$ in this exercise.

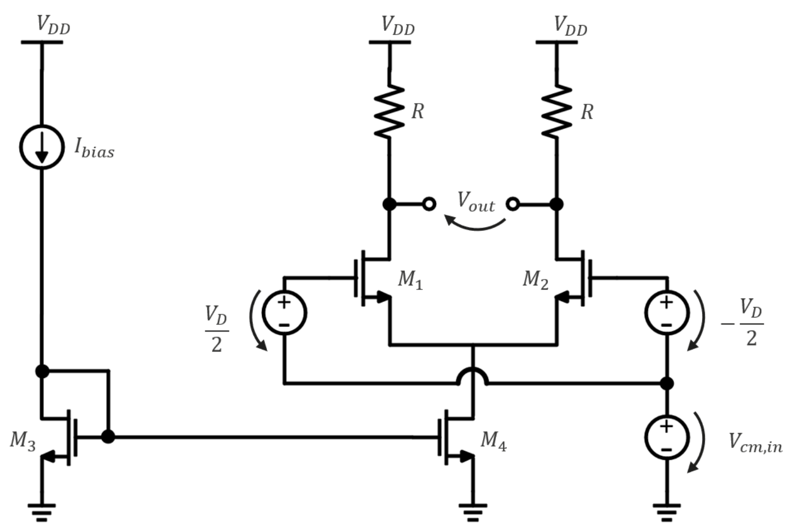


Figure 4: Differential amplifier with current mirror

e) Give V_{swing} as a function of I_{bias}.

f) Calculate, what $\frac{g_m}{I_D}$ is required to have exactly A_V and V_{swing}.

g) Calculate R and g_m such that this circuit passes exactly the V_{swing}-, P_{diss} and A_V-specification.

h) Calculate the required width W_1 and W_2 as well as L_1 and L_2 with aid of Fig. 5 and Fig. 6.

i) Decide what length L_1, L_2 and V_{OV} you would choose for M_3 and M_4. Explain why? Then, calculate the width W_3 and W_4 with aid of Fig. 6.

j) Calculate the minimum allowed input common mode voltage $V_{cm,min,in}$. What happens, if one sets $V_{cm,in} < V_{cm,min,in}$?

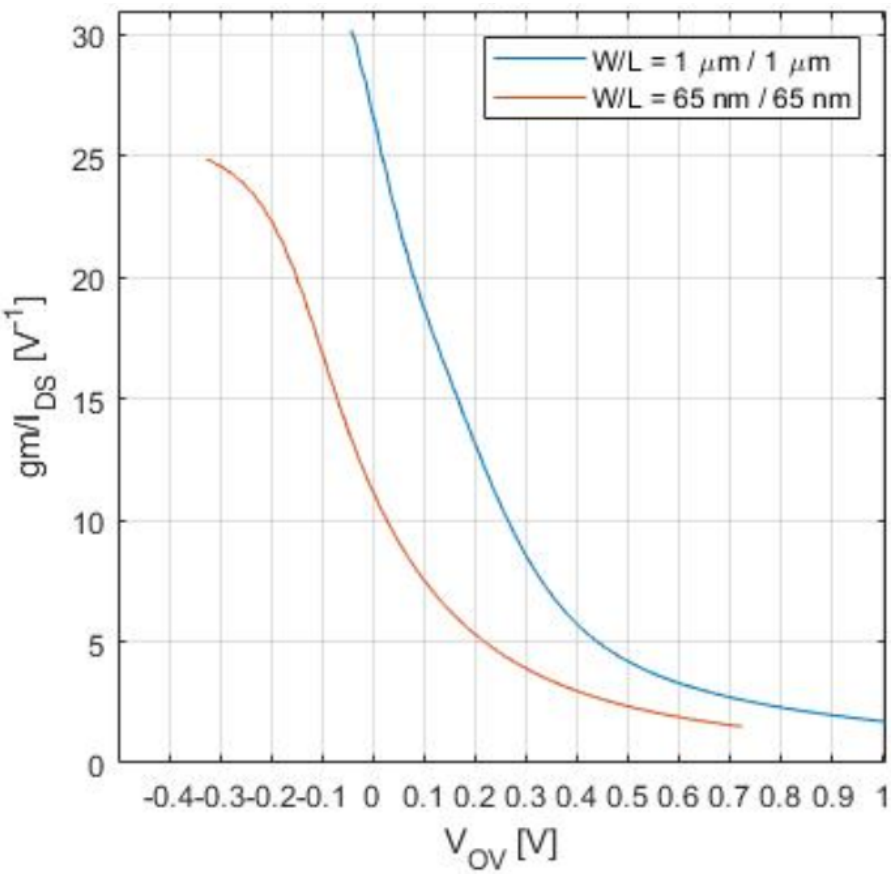
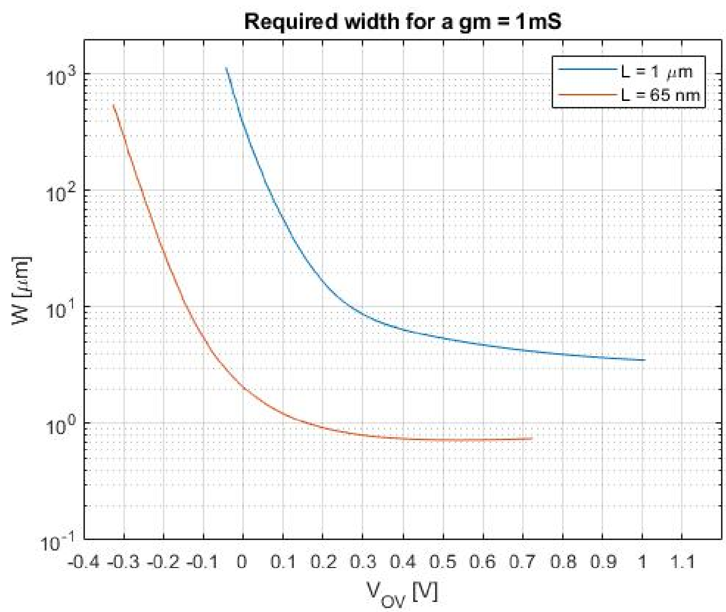
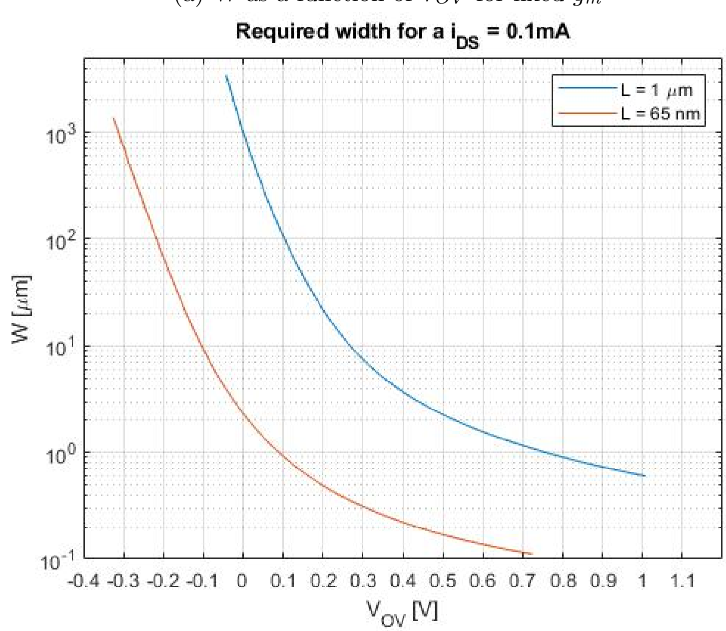


Figure 5: g_m/I_{DS} as a function of V_{OV}



(a) W as a function of V_{OV} for fixed g_m



(b) W as a function of V_{OV} for fixed i_{DS}

Figure 6: plots for calculating required width

Exercise 2

Now an OTA is considered (Fig. 7) and it is assumed again for simplicity that in this circuit the bulks of M_1 and M_2 are connected to their source connections thanks to triple-well-technology. Moreover, assume following specifications:

- $V_{DD} = 1.1V$
- $V_{th,n} = 0.4V$, $V_{th,p} = -0.22V$
- $f_{GBW} = 716MHz$
- $C_L = 500fF$

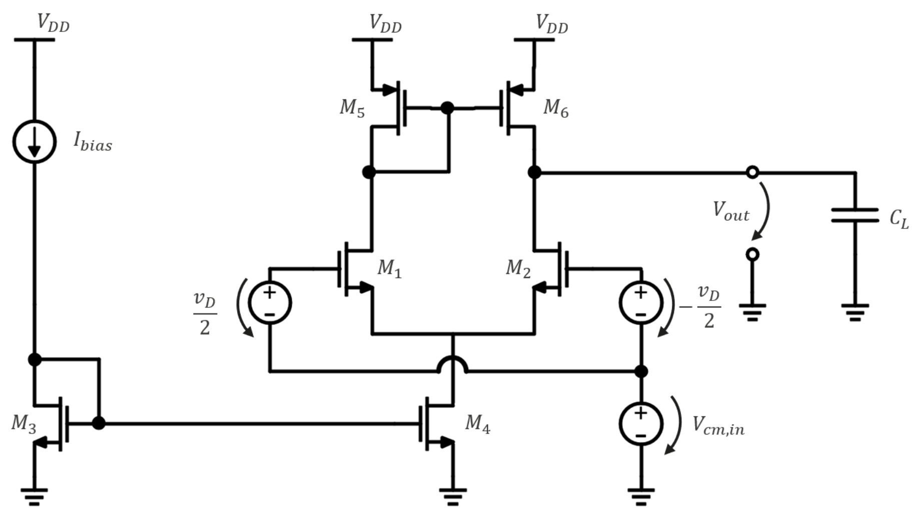


Figure 7: OTA

a) Give the small signal voltage gain equation of this circuit including the capacitances and indicate
   (i) dominant pole,
   (ii) non-dominant pole,
   (iii) zero.

b) Assume the pole-zero-doublet to be far away from the dominant pole. Draw the bode- and phase plot and indicate location of the dominant pole and GBW.

c) What happens to the pole-zero-doublet, if one increases/decreases the V_{OV} of M_5 and M_6 assuming that the current flowing through M4 is fixed as well as the lengths are fixed?

d) Assume $V_{OV,3,4} = 0.2V$, $V_{Dsat,5,6} = -0.25V$ and $V_{OV} < -0.1V$ for the remaining devices. With aid of Fig. 9, calculate the maximum/minimum possible output common mode voltage $V_{cm,max,out}$ and $V_{cm,min,out}$, where all transistors are still in saturation.

e) The designer decides to set the output common mode voltage for $v_D = 0$ to the midpoint between $V_{cm,max,out}$ and $V_{cm,min,out}$. Explain how and calculate for that the required V_{OV}.
Hint: Examine the PMOS pair for $v_D = 0$.

f) Find and explain a suitable simplification of the equation from "a)" such that Fig. 8 becomes useful for designing the OTA. Then, calculate the required V_{OV} and $V_{in,cm,min}$ for M_1 and M_2 to achieve $A_V > 8$.

g) Calculate $V_{in,cm,max}$.

h) Assume a current of I_0 is flowing through M4. Given that all transistors are in saturation, determine what current I_{CL} flows through C_L, if

   (i) $V_D = 0$,

   (ii) $V_D < -X$: M_1 is in weak inversion and M_2 in strong inversion,

   (iii) $V_D > X$: M_1 is in strong inversion and M_2 in weak inversion.

   Moreover, determine X.

i) Calculate the SR, the required I_0 and $g_{m,1,2}$ necessary to pass exactly the f_{GBW}-requirement with aid of Fig. 5. After that, calculate $g_{m,5,6}$.

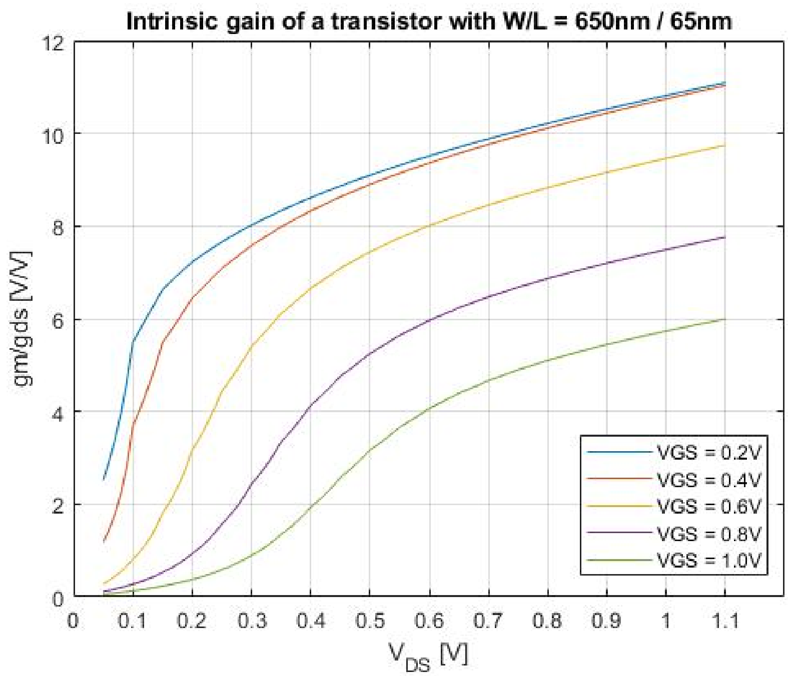


Figure 8: $\frac{g_m}{g_{ds}}$ as a function of V_{DS}

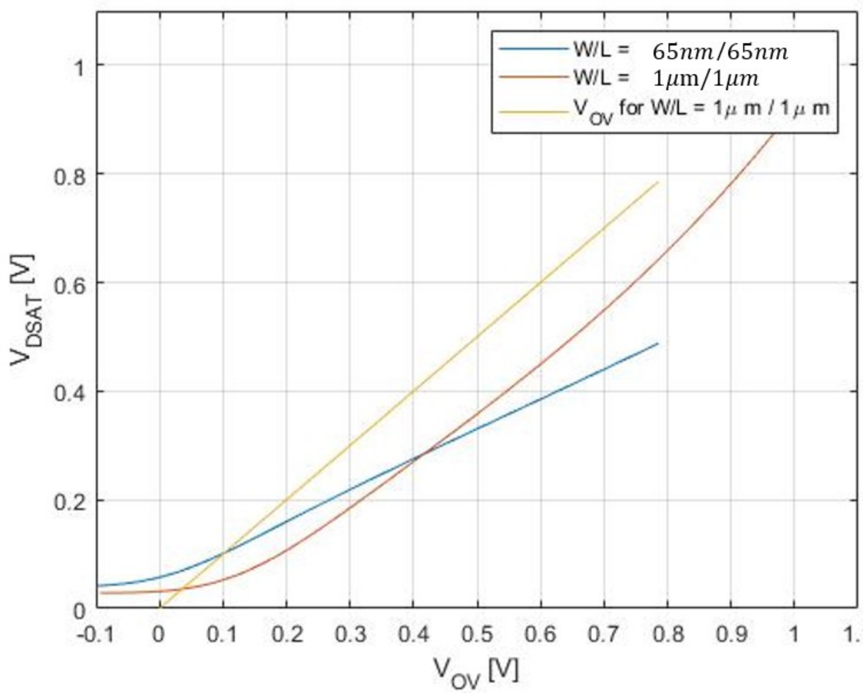


Figure 9: V_{Dsat} as a function of V_{OV}. Assume $V_{Dsat}(V_{OV} = -0.1V) \approx 50mV$ for $L = 1um$ and $L = 65nm$