CSCE 210: Computer Hardware Foundations

Test 2 Study Guide

Topics: Chapters 5-7 (Englander), HW 3-5, ICA 3-5, Lectures 9 - 17

Closed book, closed notes. You may use a calculator only for calculations. You may have a "cheat sheet", i.e., an index card 3"×5" filled up (on both sides) with anything you want. You need to turn in this card with the test.

Materials covered:

1. Chapters 5-7 (Englander) to the extent they were covered in class or assigned explicitly for reading.
2. All lecture material and discussion from Lectures 9– 17. See **BB > Course Documents** and **BB > Recordings**.
3. Homework Assignments (HWs) 3 – 5 and In-Class Activities (ICAs) 3 - 5. The solutions for Homework Assignments and In-Class Activities are posted in **BB > Assignments**.

Test format:

1. The test format will be similar to Test 1.
2. Multiple-choice questions on the mentioned material, similar to those in this study guide.
3. Short essay questions, similar to those in HWs and this study guide. Also, look at the Reading Review Questions and Exercises following each chapter.
4. Fill-in-the-blanks. Memorize the description of the keywords (those in bold) used in text.
5. Simple programs to write/analyze in the LMC assembly language like those in HW 4, ICA 4, and covered in class.
6. Working the machine cycle for the LMC instructions (LDA, STO, ADD, SUB, or branch) like in HW 5 and ICA 5.

I. MC, T/F, and fill in blanks questions.

1. What is the range of a 1-byte number stored in BCD format?
   A. 0-9
   B. 0-99
   C. 0-999
   D. 0-9999

2. What is the most common way to represent negative integers in binary form?
   A. As BCD
   B. Using 2's complement
   C. Using sign-and-magnitude
   D. None of the above

3. Changing every 0 to a 1 and every 1 to a 0 is also known as
   A. reversion.
   B. inversion.
   C. diversion.
   D. conversion.

4. Using sign-and-magnitude representation, the largest positive number that can be stored in 8 bits is
   A. 7
   B. 127
   C. 255
   D. 512

5. Using sign-and-magnitude representation, if the leftmost bit is 1 the number is
   A. positive.
   B. negative.
   C. an error.
   D. a character

6. Using sign-and-magnitude representation, storing the number -12 in 4 bits is
   A. 1100
   B. 0011
   C. 0100
   D. impossible.

7. In the 2's complement representation, a negative number begins with
   A. -1
   B. 0
   C. 1
   D. -0

8. What is the 8-bit 2's complement representation for $(-35)_{10}$?
   A. 11011101
   B. 01011101
   C. 11011100
   D. 11011111

9. If $(-9)_{10}$ is supposed to be stored in 1 byte (8 bits), it is represented in the computer in the following 2's complement form:
   A. 00001001
   B. 11110111
   C. 11110110
   D. 11111111

10. Shifting numbers left and increasing the exponent until leading zeros are eliminated is called
    A. conversion.
    B. factorization.
    C. normalization.
    D. excess notation.

11. In the LMC, where does the little man find the address of the next instruction to execute?
    A. in the mailboxes
    B. in the in-basket
    C. in the calculator
    D. in the instruction location counter
    E. in the out-basket

12. Which of the following arithmetic instructions in <u>not</u> in the LMC instruction set?
    A. SUB
    B. MUL
    C. ADD
    D. STO

13. How many instructions are in the instruction set of the LMC computer?
    A. about 50
    B. about 10
    C. about 100
    D. about 150

14. In the LMC instructions IN (901) and OUT (902), 01 and 02 represent the addresses of _____.
    A. input device and output device, respectively
    B. memory locations
    C. accumulators
    D. calculators

15. In the LMC instruction BRP 25, the branch to the instruction at address 25 is executed when the contents of the Accumulator is _____. (choose the most precise answer)
    A. <0
    B. >0
    C. ≥0
    D. =0
    E. ≤0

16. In the LMC computer, the Little Man acts as (the) _____.
    A. memory
    B. I/O interface
    C. ALU
    D. control unit
    E. program counter

17. A privileged instruction such as SVC 33 (request to increase storage) can be issued within the application program, but program control is always surrendered to _____ to execute the instruction.
    A. the user
    B. the application program
    C. the operating system
    D. the programmer

18. In the LMC, the LOAD instruction copies data from the
    A. in basket to a mailbox.
    B. calculator to a mailbox.
    C. in basket to the calculator.
    D. mailbox to the calculator.

19. In the LMC, the STORE instruction copies data from the
    A. in basket to a mailbox.
    B. mailbox to the calculator.
    C. calculator to a mailbox.
    D. in basket to the calculator.

20. In the LMC, the ADD instruction adds data from
    A. the in basket to a mailbox.
    B. a mailbox to the calculator.
    C. a mailbox to the in basket.
    D. one mailbox to another mailbox.

21. In the LMC, the INPUT instruction takes data from the
    A. in basket and places it in a mailbox.
    B. mailbox and places it in the in basket.
    C. mailbox and places it in the calculator.
    D. in basket and places it in the calculator.

22. In the LMC, the BRANCH UNCONDITIONALLY instruction changes the value in the
    A. mailbox.
    B. calculator.
    C. out basket.
    D. program counter (also called instruction location counter).

23. The _____ stores an address of the current/next instruction to execute.
    A. instruction register
    B. accumulator
    C. control Unit
    D. ALU
    E. program/instruction counter

24. The _____ executes an instruction and performs arithmetic and logic operations.
    A. instruction register
    B. accumulator
    C. control unit
    D. ALU
    E. program/instruction counter

25. The _____ holds the address of a memory location at which the instruction or data is stored.
    A. MAR
    B. MDR
    C. instruction counter
    D. accumulator

26. If the size of the MAR is 20 bits, it can address _____ unique memory locations.
    A. 262144
    B. 524288
    C. 1048576
    D. 2097152
    E. 4194304

27. A bus can carry _____.
    A. instructions
    B. data
    C. addresses
    D. control signals
    E. all the above

28. Access time to registers is _____.
    A. measured in milliseconds
    B. measured in microseconds
    C. measured in seconds
    D. almost instant

29. _____ buses are subject to radio-generated electrical interference which limits their speed and length.
    A. Serial
    B. Parallel
    C. Full-duplex
    D. Multi-point
    E. Simplex

30. The most common size of RAM in contemporary PC computers available on the market now is close to
    A. 16KB
    B. 1MB
    C. 64TB
    D. 8GB

31. Flags are _____ registers used to keep track of special conditions such as overflow.
    A. status
    B. general-purpose
    C. memory data
    D. memory address

32. The following sequence of steps in the instruction cycle:
    PC → MAR
    MDR → IR
    IR [address] → MAR
    A → MDR
    PC+1 → PC
    represents the _____ instruction.
    A. ADD
    B. SUB
    C. STO
    D. LDA
    E. BR

33. If the instruction's operation code is 5 bits long, how many unique instructions can it represent?
    A. 4
    B. 32
    C. 16
    D. 8
    E. 5

34. The ALU and CU together are known as the
    A. CPU.
    B. instruction set.
    C. program counter.
    D. Memory Management Unit.

35. The area inside of the CPU that holds data temporarily and performs calculations is called the
    A. accumulator.
    B. program counter.
    C. arithmetic logic unit.
    D. Memory Management Unit.

36. The 1-bit registers that are used to allow the computer to keep track of special conditions (like overflow or power failure) are often called
    A. flags.
    B. loops.
    C. the ALU.
    D. I/O counters.

37. The register that holds the address of the memory location that needs to be accessed is called the
    A. IR.
    B. MAR.
    C. MDR.
    D. MBR.

38. The register that holds the current instruction is called the
    A. IR.
    B. PC.
    C. LMC.
    D. MBR.

39. The register that will hold the data value that is being transferred between the CPU and a particular memory location is called the
    A. PC.
    B. ALU.
    C. MAR.
    D. MDR.

40. The mailboxes in the LMC model are the equivalent to a real computer's
    A. CPU.
    B. ports.
    C. memory.
    D. control unit.

41. If the memory address register is 8 bits wide, the number of possible memory addresses is
    A. 8
    B. 16
    C. 64
    D. 256

42. When the instruction being executed is to store data, the data will be transferred from another register in the CPU to the _____, and from there it will be transferred into memory.
    A. IR
    B. PC
    C. MAR
    D. MDR

43. A bus in which there is an individual line for each bit of data, address, and control is called a
    A. wide bus.
    B. serial bus.
    C. parallel bus.
    D. dedicated bus.

44. A bus that transfers data sequentially, one bit at a time using just a single line pair is called
    A. a serial bus.
    B. a single bus.
    C. a narrow bus.
    D. a sequential bus.

II. <u>Fill out the blanks with the most appropriate word(s)</u>

1. In an instruction STO 50, an implicit source is a(n) _____.

2. The first phase in the instruction (machine) cycle is called the _____ phase, and the second phase is called the _____ phase.

3. The _____ holds a data value that is being written to or read from the memory location currently addressed by the MAR.

4. A _____ is a set of parallel or serial wires, or optical conductors that can carry bits.

5. A bus line that is "one-way" is called a(n) _____ bus line.

6. A bus line that can carry data in both directions at the same time is called a(n) _____ bus line.

7. In an instruction *STO 80*, an *80* is a(n) _____ and *STO* is a(n) _____.

III. Make the following calculations. Do not use a calculator that provides direct conversion.

1. Calculate the largest positive integer that can be stored in 2 bytes assuming a) an unsigned integer and b) an integer using sign-and-magnitude format.

2. Two's complement
   a. Find the 2's complementary representation in 8-bits of the number -51.

   b. Find the 2's complementary representation in 16-bits of the number -331.

3. Show how decimal value 12.25 is represented in SEEMMMMM format. Use the floating point format SEEMMMMM, where S = 0 is "+" and 5 is "-"; EE is the exponent in excess-50, and MMMMM are five digits of mantissa.

4. Show how -0.00012325 is represented in SEEMMMMM format.

5. Convert 55698799 in SEEMMMMM to a decimal integer without exponents.

6. Show the packed decimal format of the following decimal values.

   a. $(18)_{10}$

   b. $(-18)_{10}$

   c. $(131)_{10}$

   d. $(-75)_{10}$

7. Convert the following decimal values to the 8-bit sign-and-magnitude representation.

   a. $(18)_{10}$

   b. $(-18)_{10}$

   c. $(119)_{10}$

   d. $(-75)_{10}$

8. Convert the following decimal values to the 8-bit binary floating-point representation. Use the format S EEE MMMM, where all digits are binary, S = 0 is positive and 1 is negative, EEE is the exponent in excess-3 notation, and MMMM are four digits of the mantissa.

   a. $(.40625)_{10}$

b. $(-12)_{10}$

9. Convert the following decimal values to the 32-bit binary floating-point representation. Use the format where the 1 bit is allocated to the sign, 8 bits to the exponent, and 23 bits to the mantissa. All digits are binary, S = 0 is positive and 1 is negative and the exponent is in excess-127 notation.

   a. $(15.625)_{10}$

   b. $(-46.25)_{10}$

IV. <u>Write the LMC program</u> that reads in two numbers (one at a time); places them in memory locations 50 and 51, respectively; calculates their positive difference; places this difference in memory location 52; and writes the result (i.e., the difference) out.

Memory Address	Instruction (Mnemonic)	Instruction (Code)
00		
01		
02		
03		
04		
05		
06		
07		
08		
09		
10		
11		
12		
13		
14		
15		

V. In the LMC program below, determine the contents of the Program Counter (PC) before and after each instruction is executed. Also determine the contents of the out-basket (OUT), Accumulator (A), and memory locations 60, 61, and 62 after each instruction is executed. Note that some instructions may not be executed. Also, note that memory locations 60, 61, and 62 have been initialized with 15, 15, and 10, respectively.

Memory Address	Instruction	PC	OUT	A	60	61	62
00	LDA 60	00 → 01					
01	ADD 62						
02	STO 61						
03	BRP 05						
04	BR 01						
05	OUT						
06	HLT						
…	…						
…	…						
60	15						
61	15						
62	10						

VI. Suppose that the following instruction and data is found at memory locations 05 and 75, respectively.

Memory Address	Instruction (Mnemonic)	Instruction (Code)
…	…	…
05	LDA 75	575
…	…	…
75	40	

Show the contents of the PC, the MAR, the MDR, the IR, and the Accumulator (A) as each step of the fetch-execute cycle is performed for instruction **LDA 75** residing at address 05. If the contents of the register is unknown, write the "?" in the space provided.

	PC	MAR	MDR	IR	A
PC → MAR					
MDR → IR					
IR [address] → MAR					
MDR → A					
PC+1 → PC					

VII. Short essay questions - These are examples of short essay questions. There will be only between 2 and 5 short essay questions on Test 2.

1. What factors determine the speed of the computer?

2. Why are buses used in the computer? What can they carry? What is the difference between a multipoint bus and a point-to-point bus? Explain the term *throughput* and *data width* of the bus.

3. What are registers? Where are they located? Why are they needed? Are they temporary or permanent memory?

4. How are the registers in the CPU different from main memory?

Answers

I. MC, T/F, and fill in blanks questions.

1. B	10. C	19. C	28. D	37. B
2. B	11. D	20. B	29. B	38. A
3. B	12. B	21. D	30. D	39. D
4. B	13. B	22. D	31. A	40. C
5. B	14. A	23. E	32. C	41. D
6. D	15. C	24. D	33. B	42. D
7. C	16. D	25. A	34. A	43. C
8. A	17. C	26. C	35. C	44. A
9. B	18. D	27. E	36. A	

II. Fill out the blanks with the most appropriate word(s)

1. accumulator
2. fetch, execute
3. memory data register (MDR)
4. bus
5. simplex
6. full duplex
7. operand (or address), operation code (opcode)

III. Make the following calculations. Do not use a calculator that provides direct conversion.

1. Calculate the largest positive integer that can be stored in 2 bytes assuming a) an unsigned integer and b) an integer using sign-and-magnitude format.

   a) In two bytes there are 16 bits, and as we know from Chapter 3 the largest positive integer if the two bytes represents only unsigned integers → $2^{16} - 1 = 65,536 - 1 = 65,535$

   b) In two bytes there are 16 bits, of those 15 are available for positive numbers (magnitude):
   $= 2^{15} - 1$
   $= 32768 - 1$
   $= 32,767$

2. Two's complement
   a. Find the 2's complementary representation in 8-bits of the number -51.

      Step 1: 51 in binary using 8-bits is 00110011
      Step 2: Flip (invert) the bits: 11001100
      Step 3: add 1: 11001101

   b. Find the 2's complementary representation in 16-bits of the number -331.

      Step 1: 331 in binary using 16-bits is 0000 0001 0100 1011
      Step 2: Flip the bits: 1111 1110 1011 0100
      Step 3: add 1: 1111 1110 1011 0101

3. Show how decimal value 12.25 is represented in SEEMMMMM format. Use the floating point format SEEMMMMM, where S = 0 is "+" and 5 is "-"; EE is the exponent in excess-50, and MMMMM are five digits of mantissa

   12.25 = .1225 x 10^2
   S=0
   EE=52
   MMMMM = 12250, where the added zero is added to make five digits
   Answer: 05212250

4. Show how -0.00012325 is represented in SEEMMMMM format.

   $-0.00012325 = -.12325 \times 10^{-3}$
   S=5
   EE=47
   MMMMM = 12325
   Answer: 54712325

5. Convert 55698799 in SEEMMMMM to a decimal integer without exponents.

   5 = S; sign is negative
   56 = EE; exponent is 6 (since it is in excess-50 format)
   98799 = MMMMM
   $-0.98799 \times 10^6 = -987990$

6. Show the packed decimal format of the following decimal values.

   a. $(18)_{10}$
      0001 1000 1100

   b. $(-18)_{10}$
      0001 1000 1101

   c. $(131)_{10}$
      0001 0011 0001 1100

   d. $(-75)_{10}$
      0111 0101 1101

7. Convert the following decimal values to the 8-bit sign-and-magnitude representation.

   a. $(18)_{10}$
      0001 0010

   b. $(-18)_{10}$
      1001 0010

   c. $(119)_{10}$
      0111 0111

   d. $(-75)_{10}$
      1100 1011

8. Convert the following decimal values to the 8-bit binary floating-point representation. Use the format S EEE MMMM, where all digits are binary, S = 0 is positive and 1 is negative, EEE is the exponent in excess-3 notation, and MMMM are four digits of the mantissa.

   a. $(.40625)_{10}$

	IP	R
.40625 * 2	0	.8125
.8125 * 2	1	.6250
.625 * 2	1	.250
.25 * 2	0	.50
.5 * 2	1	.00

$(.40625)_{10} = (.01101)_2$

$.01101 \times 2^0$
1.101×2^{-2}

S = 0 (positive)
EEE = 3 + (-2) = 1 = $(001)_2$
MMMM = 1010

SEEEMMMM = 0 001 1010

   b. $(-12)_{10}$

	IQ	R
12 / 2	6	0
6 / 2	3	0
3 / 2	1	1
1 / 2	0	1

$(-12)_{10} = (-1100)_2$

-1100×2^0
-1.100×2^3

S = 1 (negative)
EEE = 3 + 3 = 6 = $(110)_2$
MMMM = 1000

SEEEMMMM = 1 110 1000

9. Convert the following decimal values to the 32-bit binary floating-point representation. Use the format where the 1 bit is allocated to the sign, 8 bits to the exponent, and 23 bits to the mantissa. All digits are binary, S = 0 is positive and 1 is negative and the exponent is in excess-127 notation.

   a. $(15.625)_{10}$

$(15.625)_{10} = (1111.101)_2$

1111.101×2^0
1.111101×2^3

S = 0 (positive)
EEEEEEEE = 127 + 3 = 130 = $(1000\ 0010)_2$
23-bit Mantissa = 11110100000000000000000

Solution: 0 10000010 11110100000000000000000

b. $(-46.25)_{10}$

$(-46.25)_{10} = (-101110.01)_2$

-101110.01×2^0
-1.0111001×2^5

S = 1 (negative)
EEEEEEEE = 127 + 5 = 132 = $(1000\ 0100)_2$
23-bit Mantissa = 01110010000000000000000

Solution: 1 10000100 01110010000000000000000

IV. <u>Write the LMC program</u> that reads in two numbers (one at a time); places them in memory locations 50 and 51, respectively; calculates their positive difference; places this difference in memory locations 52; and writes the result (difference) out.

Memory Address	Instruction (Mnemonic)	Instruction (Code)
00	IN	901
01	STO 50	350
02	IN	901
03	STO 51	351
04	SUB 50	250
05	BRP 08	808
06	LDA 50	550
07	SUB 51	251
08	STO 52	352
09	OUT	902
10	HLT	000
11		
12		
13		
14		
15		

V. In the LMC program below, determine the contents of the Program Counter (PC) before and after each instruction is executed. Also determine the contents of the out-basket (OUT), Accumulator (A), and memory locations 60, 61, and 62 after each instruction is executed. Note that some instructions may not be executed. Also, note that memory locations 60, 61, and 62 have been initialized with 15, 15, and 10, respectively.

Memory Address	Instruction	PC	OUT	A	60	61	62
00	LDA 60	00 → 01	?	15	15	15	10
01	ADD 62	01 → 02	?	25	15	15	10
02	STO 61	02 → 03	?	25	15	25	10
03	BRP 05	03 → 05	?	25	15	25	10
04	BR 01	This instruction is not executed (since BRP is executed because A = 25 >=0)					
05	OUT	05 → 06	25	25	15	25	10
06	HLT	06 → 06	25	25	15	25	10
…	…						
…	…						
60	15						
61	15						
62	10						

VI. Suppose that the following instruction and data is found at memory locations 05 and 75, respectively.

	PC	MAR	MDR	IR	A
PC → MAR	05	05	LDA 75	?	?
MDR → IR	05	05	LDA 75	LDA 75	?
IR [address] → MAR	05	75	40	LDA 75	?
MDR → A	05	75	40	LDA 75	40
PC+1 → PC	06	75	40	LDA 75	40

VII. Short essay questions

The answers to the essay questions are in the textbook, lecture notes, or homework solutions posted on BB.