

Depletion Mode MOSFET

Test Conditions

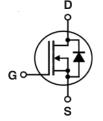
IXTA3N100D2 IXTP3N100D2

 $\mathbf{V}_{\mathsf{DSX}}$ 1000V **3A** D(on)

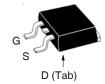
6Ω

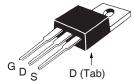
N-Channel

Symbol



Maximum Ratings





G = Gate = Drain D S = Source Tab = Drain

TO-220AB	(IXTP)
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Features

- · Normally ON Mode
- International Standard Packages
- Molding Epoxies Meet UL94 V-0 Flammability Classification

Advantages

- Easy to Mount
- · Space Savings
- High Power Density

Applications

- · Audio Amplifiers
- Start-Up Circuits
- Protection Circuits
- Ramp Generators
- Current Regulators
- Active Loads

<u>-,</u>	1001001111110110		90
V _{DSX}	$T_{_{\rm J}} = 25^{\circ}\text{C to } 150^{\circ}\text{C}$	1000	V
V _{GSX}	Continuous	±20	V
V _{GSM}	Transient	±30	V
$\overline{\mathbf{P}_{D}}$	T _C = 25°C	125	W
T,		- 55 +150	°C
T _{JM}		150	°C
T _{stg}		- 55 +150	°C
T _L	Maximum Lead Temperature for Soldering	300	°C
$T_{\mathtt{SOLD}}$	1.6 mm (0.062in.) from Case for 10s	260	°C
M _d	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in.
Weight	TO-263	2.5	g
	TO-220	3.0	g

SymbolTest ConditionsCharacter $(T_J = 25^{\circ}C, Unless Otherwise Specified)$ Min.			teristic Typ.	Values Max		
BV _{DSX}	$V_{GS} = -5V, I_{D} = 250\mu A$		1000			V
V _{GS(off)}	$V_{DS} = 25V, I_{D} = 250\mu A$		- 2.5		- 4.5	V
I _{gsx}	$V_{GS} = \pm 20V, V_{DS} = 0V$				±100	nA
DSX(off)	$V_{DS} = V_{DSX}, V_{GS} = -5V$	T _J = 125°C				μ Α μ Α
R _{DS(on)}	$V_{GS} = 0V, I_{D} = 1.5A, \text{ Note 1}$				6	Ω
I _{D(on)}	$V_{es} = 0V, V_{ps} = 50V, Note 1$		3			A



				teristic Values Typ. ∣ Max.		
(1) - 20 0,	Officed Officiwise Openica)		. , p.	mux.		
g_{fs}	$V_{DS} = 30V, I_{D} = 1.5A, \text{ Note 1}$	1.2	2.0	S		
C _{iss}			1020	pF		
C _{oss}	$V_{GS} = -10V, V_{DS} = 25V, f = 1MHz$		68	pF		
C _{rss}			17	pF		
t _{d(on)}	Resistive Switching Times		27	ns		
t, (· ·		67	ns		
t _{d(off)}	$V_{GS} = \pm 5V, V_{DS} = 500V, I_{D} = 1.5A$		34	ns		
t,	$R_{\rm g} = 3.3\Omega$ (External)		40	ns		
Q _{g(on)}			37.5	nC		
Q _{gs}	$V_{GS} = 5V, V_{DS} = 500V, I_{D} = 1.5A$		4.4	nC		
Q_{gd}			21.2	nC		
R _{thJC}				1.0 °C/W		
R _{thCS}	TO-220		0.50	°C/W		

Safe-Operating-Area Specification

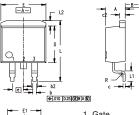
		Characteristic Values			
Symbol	Test Conditions	Min.	Тур.	Max.	
SOA	$V_{DS} = 800V, I_{D} = 94mA, T_{C} = 75^{\circ}C, Tp = 5s$	75		W	

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values			
$(T_J = 25^\circ)$	C, Unless Otherwise Specified)	Min.	Тур.	Max.	
V _{SD}	$I_F = 3A, V_{GS} = -10V, \text{ Note 1}$		0.8	1.3 V	
t _{rr}	$I_F = 3A$, -di/dt = 100A/ μ s		970	ns	
I _{RM}	$V_{\rm B} = 100 \text{V}, V_{\rm GS} = -10 \text{V}$		12.7	A	
\mathbf{Q}_{RM}) V _R = 100V, V _{GS} = -10V		6.16	μC	

Note 1. Pulse test, $t \le 300\mu s$, duty cycle, $d \le 2\%$.

TO-263 Outline

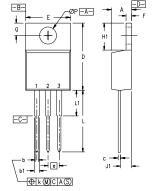




1.	Gate	
2.	Drain	
3.	Source	
4.	Drain	
	Bottom	
Si	de	

Dim.	Millimeter		Inch	nes
	Min.	Max.	Min.	Max.
Α	4.06	4.83	.160	.190
b	0.51	0.99	.020	.039
b2	1.14	1.40	.045	.055
С	0.40	0.74	.016	.029
c2	1.14	1.40	.045	.055
D	8.64	9.65	.340	.380
D1	8.00	8.89	.280	.320
E	9.65	10.41	.380	.405
E1	6.22	8.13	.270	.320
е	2.54	BSC	.100	BSC
L	14.61	15.88	.575	.625
L1	2.29	2.79	.090	.110
L2	1.02	1.40	.040	.055
L3	1.27	1.78	.050	.070
L4	0	0.13	0	.005

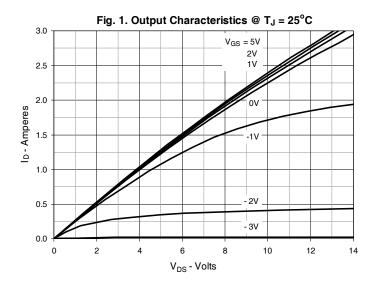
TO-220 Outline

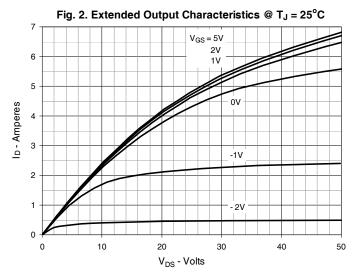


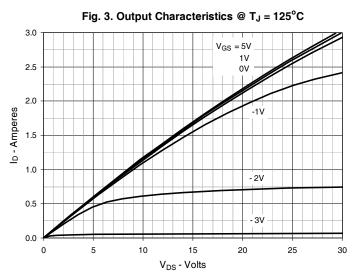
Pins: 1 - Gate 2 - Drain 3 - Source

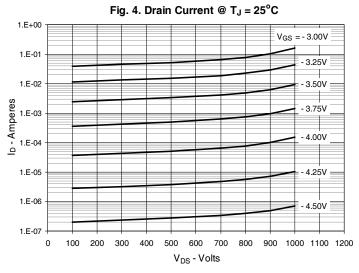
MY2	INCH	INCHES		METERS
2114	MIN	MAX	MIN MAX	
Α	.170	.190	4.32	4.83
b	.025	.040	0.64	1.02
b1	.045	.065	1.15	1.65
С	.014	.022	0.35	0.56
D	.580	.630	14.73	16.00
E	.390	.420	9.91	10.66
е	.100 BSC		2.54 BSC	
F	.045	.055	1.14	1.40
H1	.230	.270	5.85	6.85
J1	.090	.110	2.29	2.79
k	0	.015	0	0.38
L	.500	.550	12.70	13.97
L1	.110	.230	2.79	5.84
ØΡ	.139	.161	3.53	4.08
Q	.100	.125	2.54	3.18

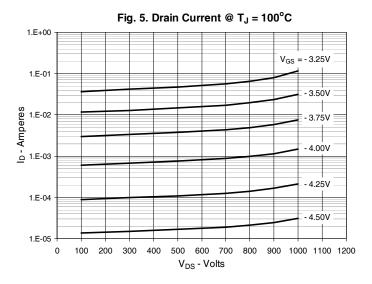












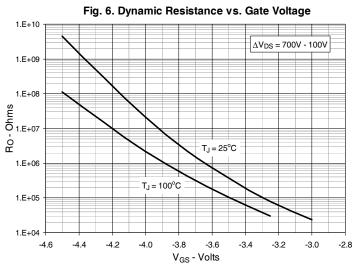




Fig. 7. Normalized R_{DS(on)} vs. Junction Temperature

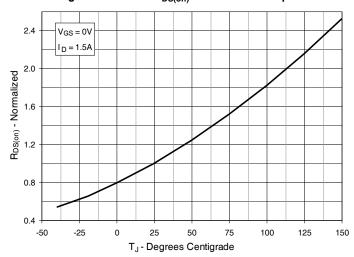


Fig. 8. $R_{DS(on)}$ Normalized to $I_D = 1.5A$ Value vs. Drain Current

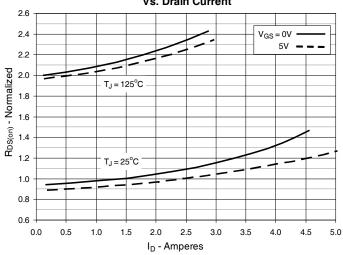


Fig. 9. Input Admittance

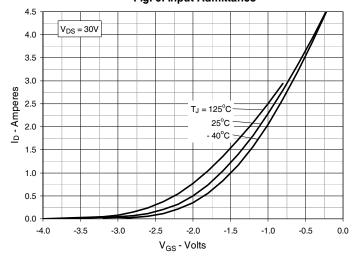


Fig. 10. Transconductance

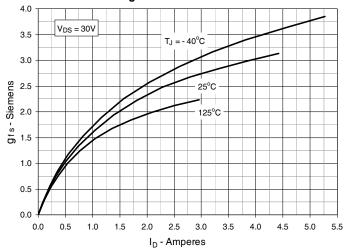


Fig. 11. Breakdown and Threshold Voltages

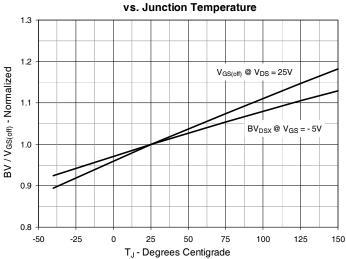
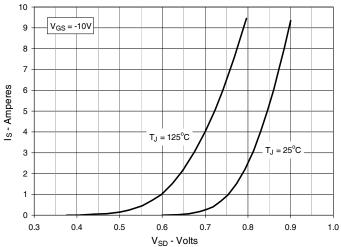
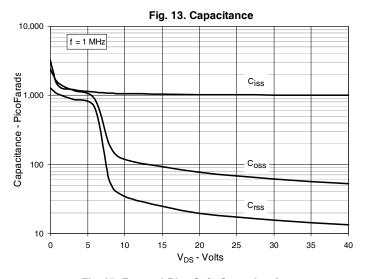


Fig. 12. Forward Voltage Drop of Intrinsic Diode



IXYS Reserves the Right to Change Limits, Test Conditions, $\$ and $\$ Dimensions.





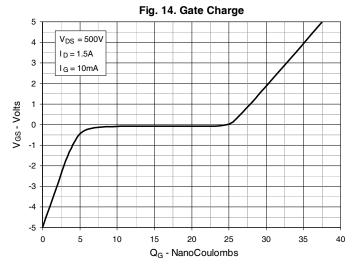


Fig. 15. Forward-Bias Safe Operating Area

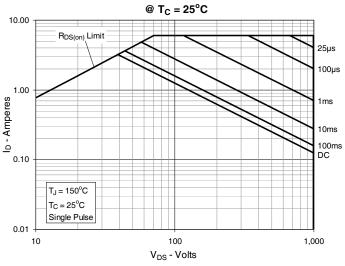


Fig. 16. Forward-Bias Safe Operating Area

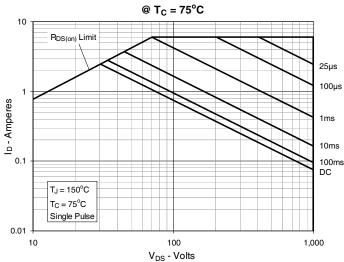


Fig. 17. Maximum Transient Thermal Impedance

