Weighing scale-reader

2.737 Mechatronics

Instructor: Prof. David L. Trumper

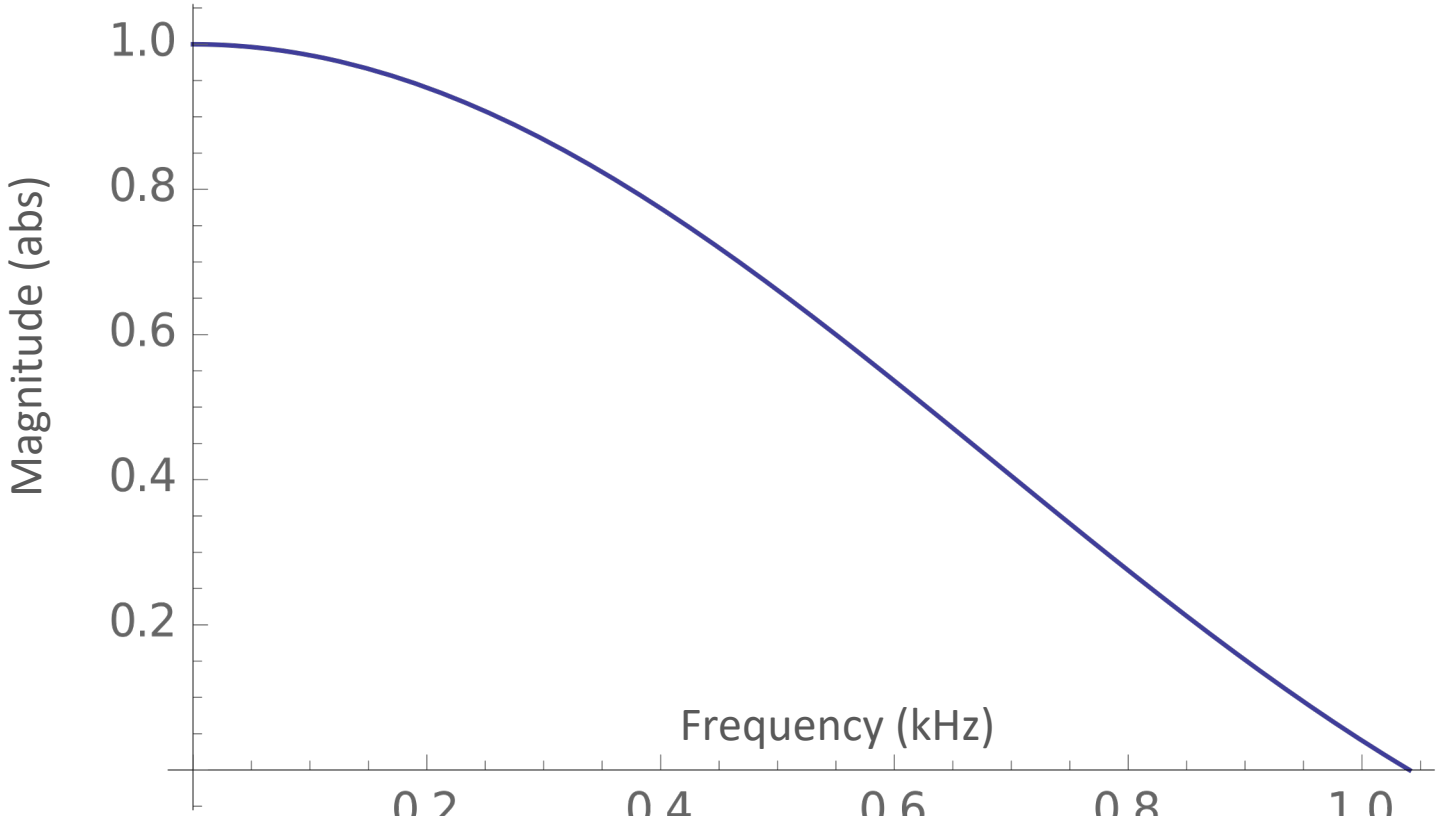
Key takeaway: Oversampling for noise reduction.

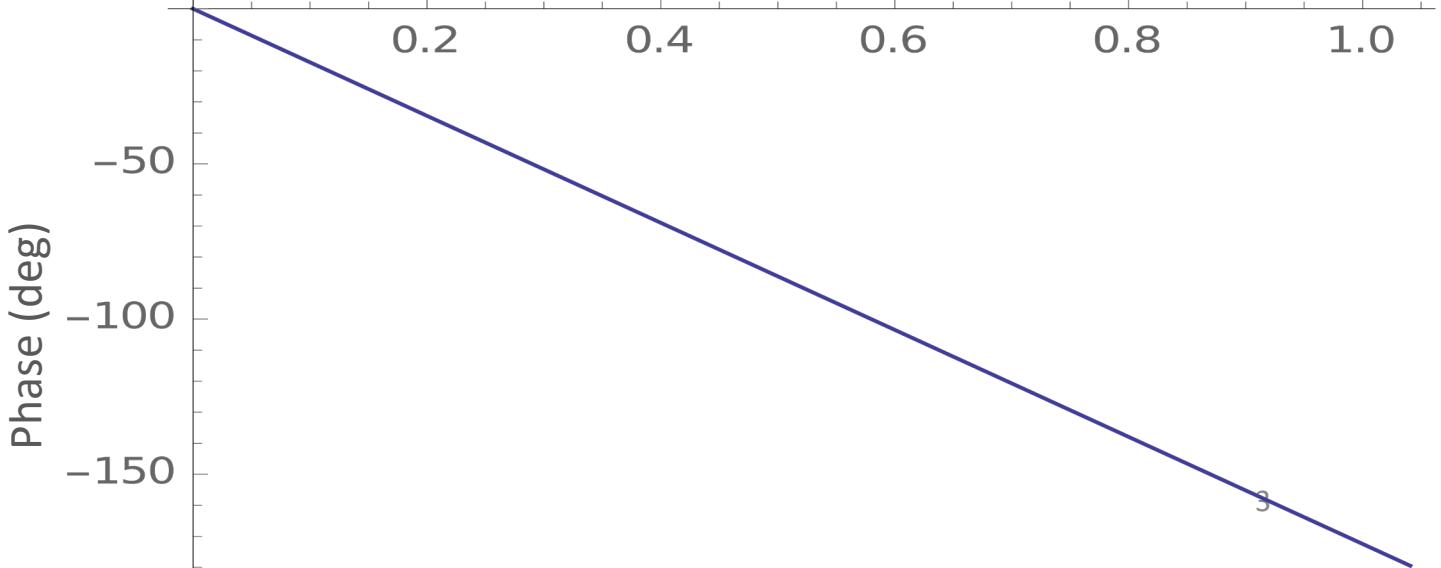
Code Overview

- Field Programmable Gate Array (FPGA)
  - Reads C/AI0 at 333 kHz as a 12-bit integer value, and
  - Oversampling Implemented: Takes a moving average with 320 previous values and converts the result into fixed point.
    - Effectively, the fidelity (tracking of AI without too much phase lag) of the output oversampled AI signal is at frequencies considerably below 333/320 = 1.041 kHz. The phase decreases linearly with frequency going to -180 degree at 333/320 = 1.041 kHz.
    - We are trading throughput (limiting how fast dynamics we can perceive from the AI signal) for lower noise and hence better resolution.
    - For more information, refer to - http://www.cypress.com/file/236481/download

- Real-Time (RT)
  - Reads the oversampled C/AI0 from the FPGA.
  - Has operations for filtering, converging voltage to load and implements the “tare” function.

Frequency response of Moving average filter

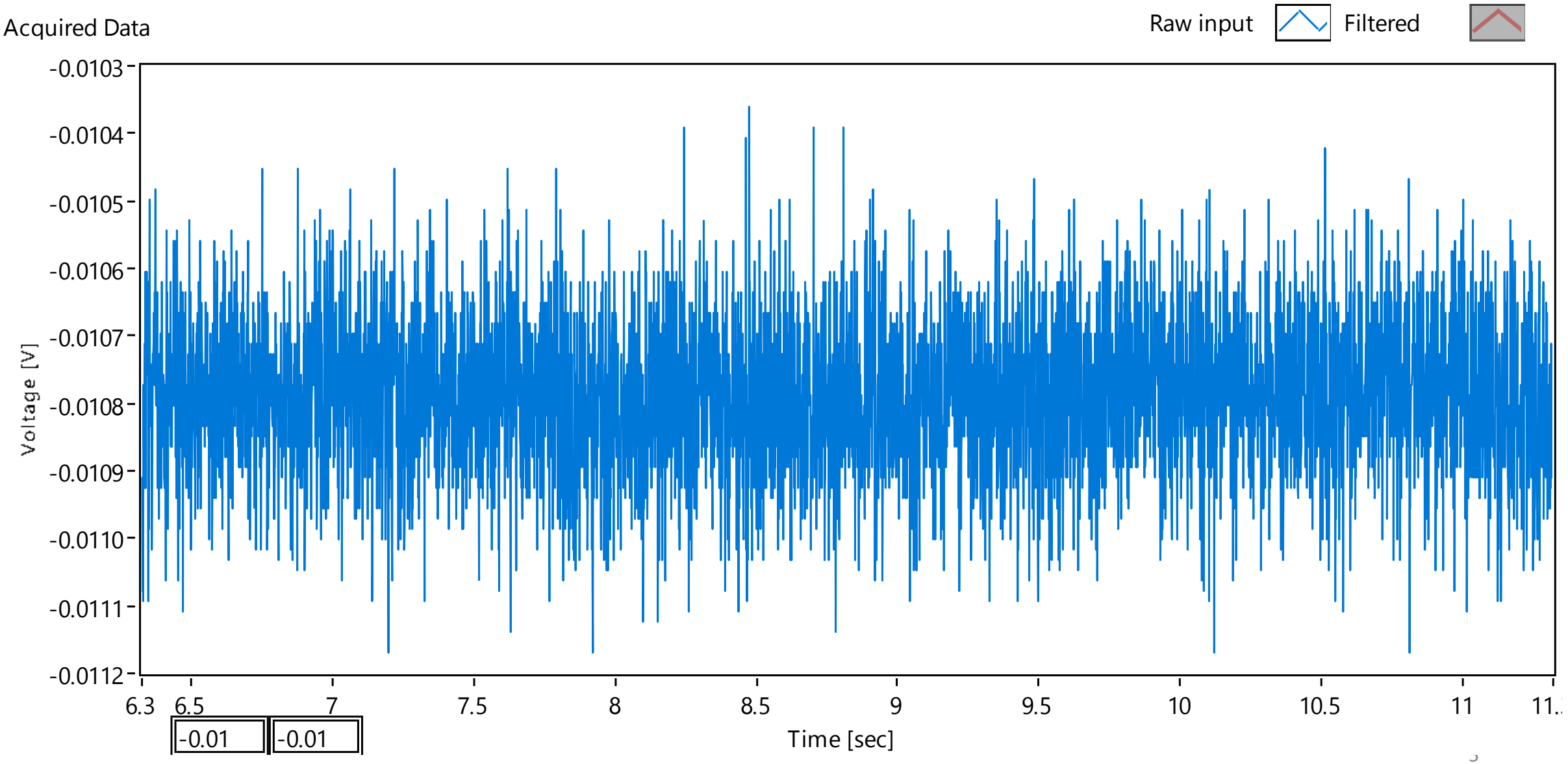




If you need better frequency response, then look at alternative FIR implementations - http://www.analog.com/media/en/technical-documentation/dsp-book/dsp_book_Ch15.pdf

Oversampling

Oversampling implemented (320:1)



Oversampling implemented (320:1)

Effective resolution increase:

$$w = \frac{\log(N_{avg})}{\log(4)}$$

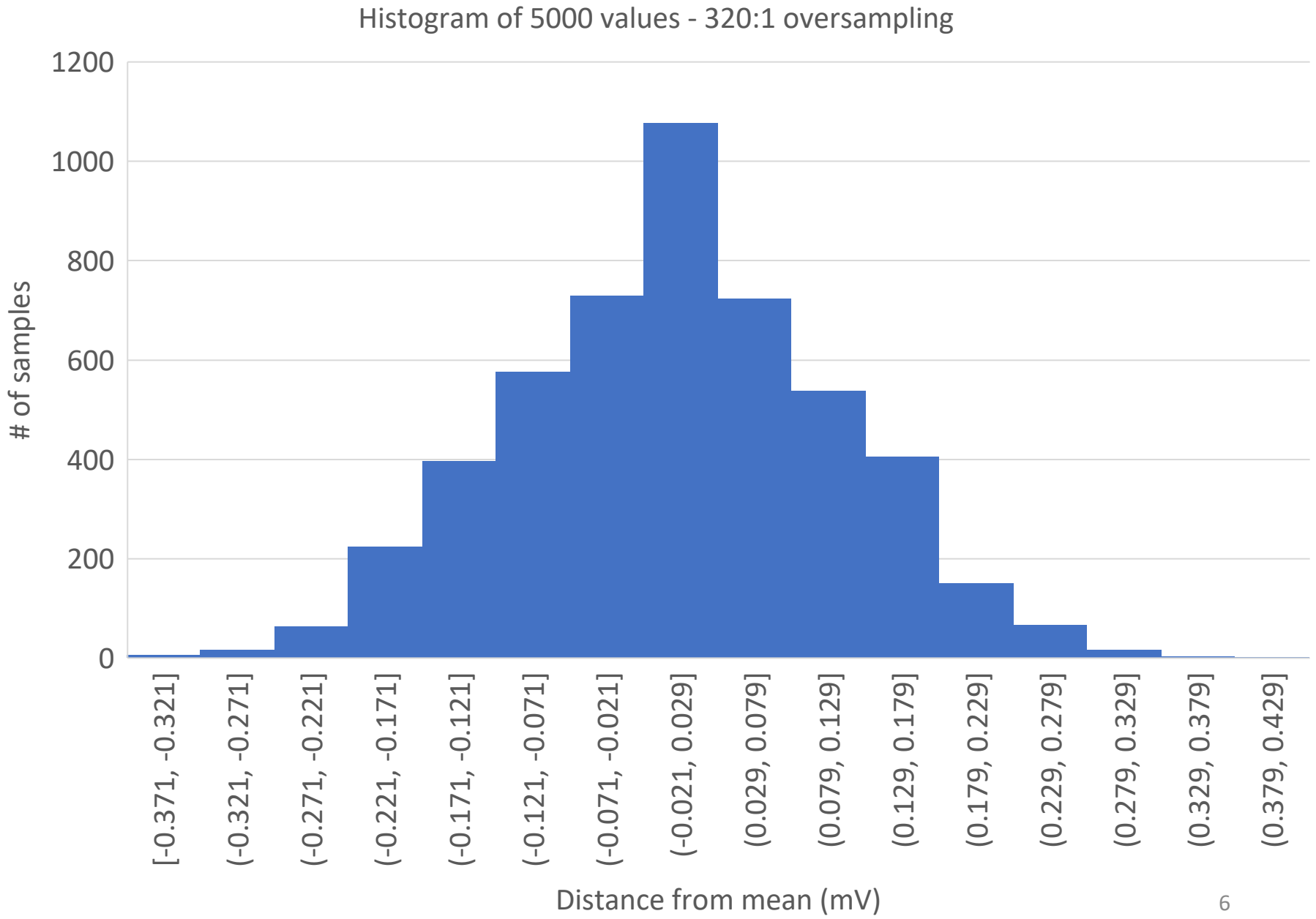
N_{avg} = 320 sample average,
w = 4.17

The system effectively should behave as a 16-bit ADC.

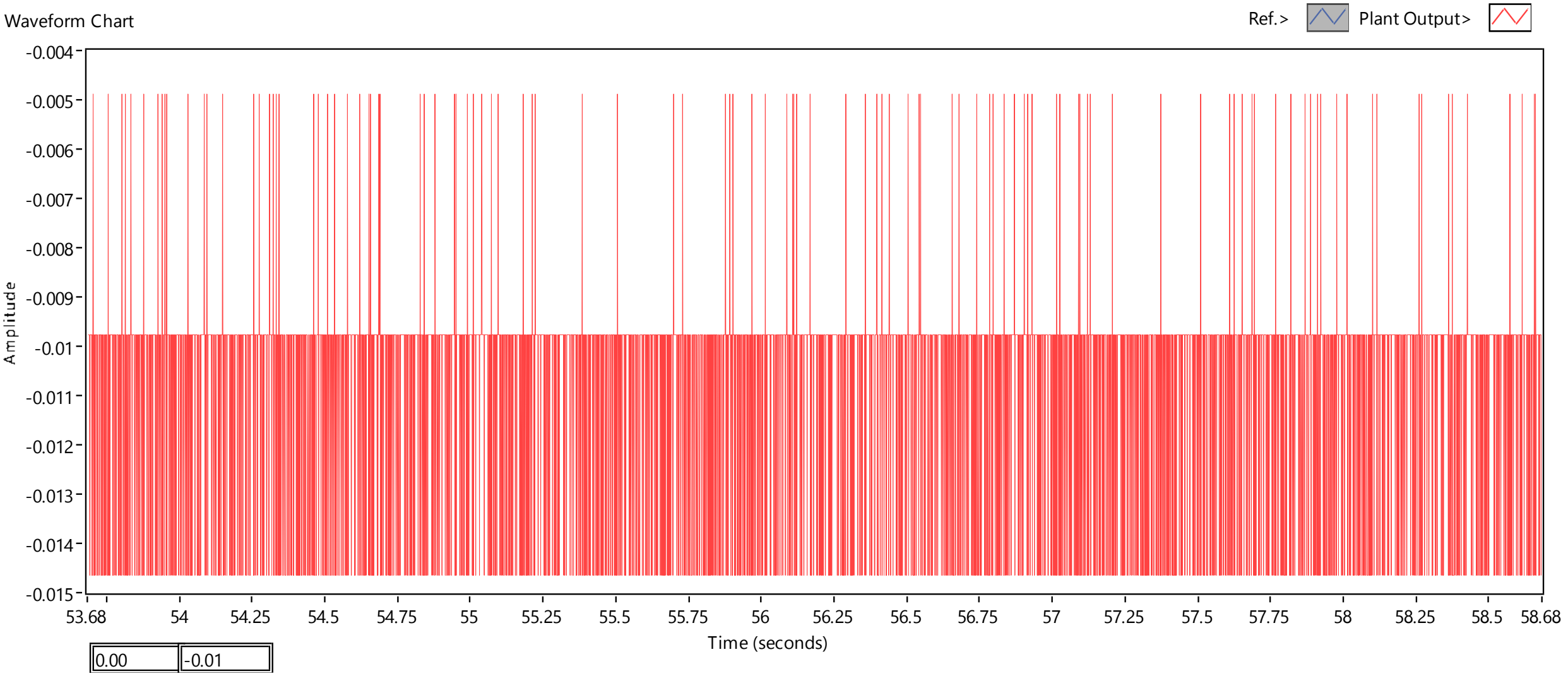
16-bit resolution:
20/2^16 = 0.305 mV

Measurement:
10 times better resolution and lower noise than original.

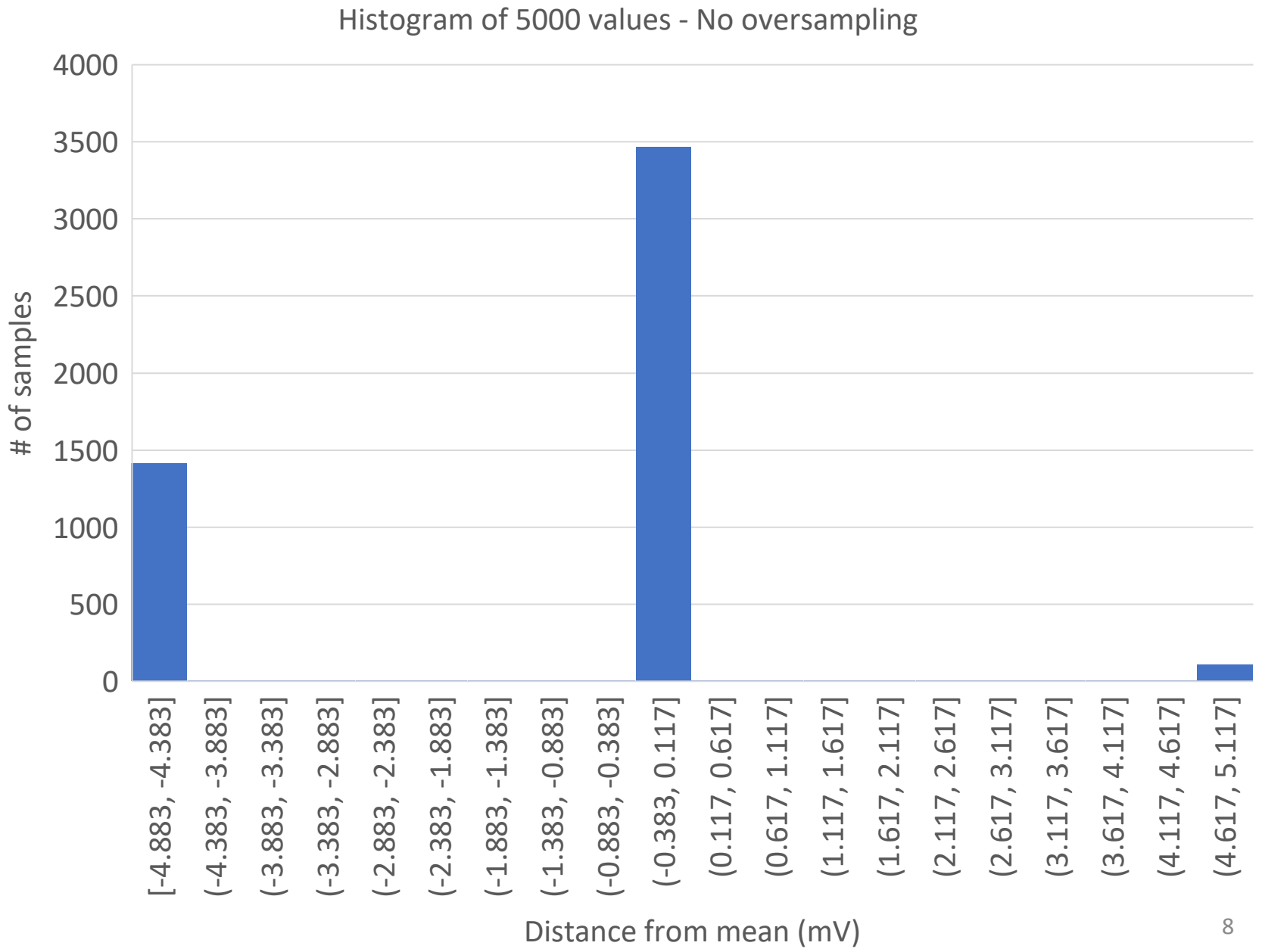
Total spread:
Max-Min = 0.778 mV



Original 12-bit Analog input



Original 12-bit Analog input

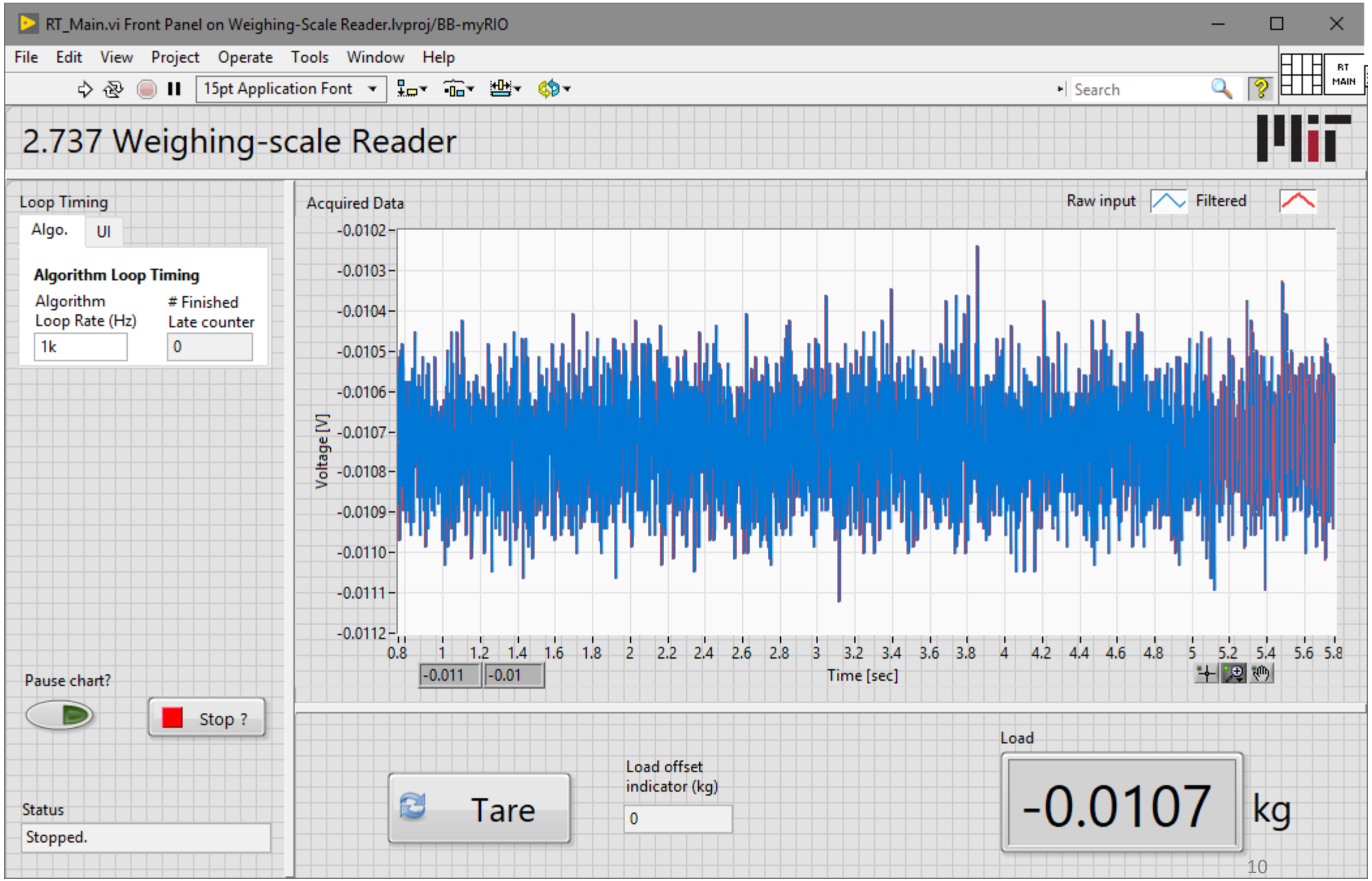


12-bit resolution:
20/2^12 = 4.883 mV

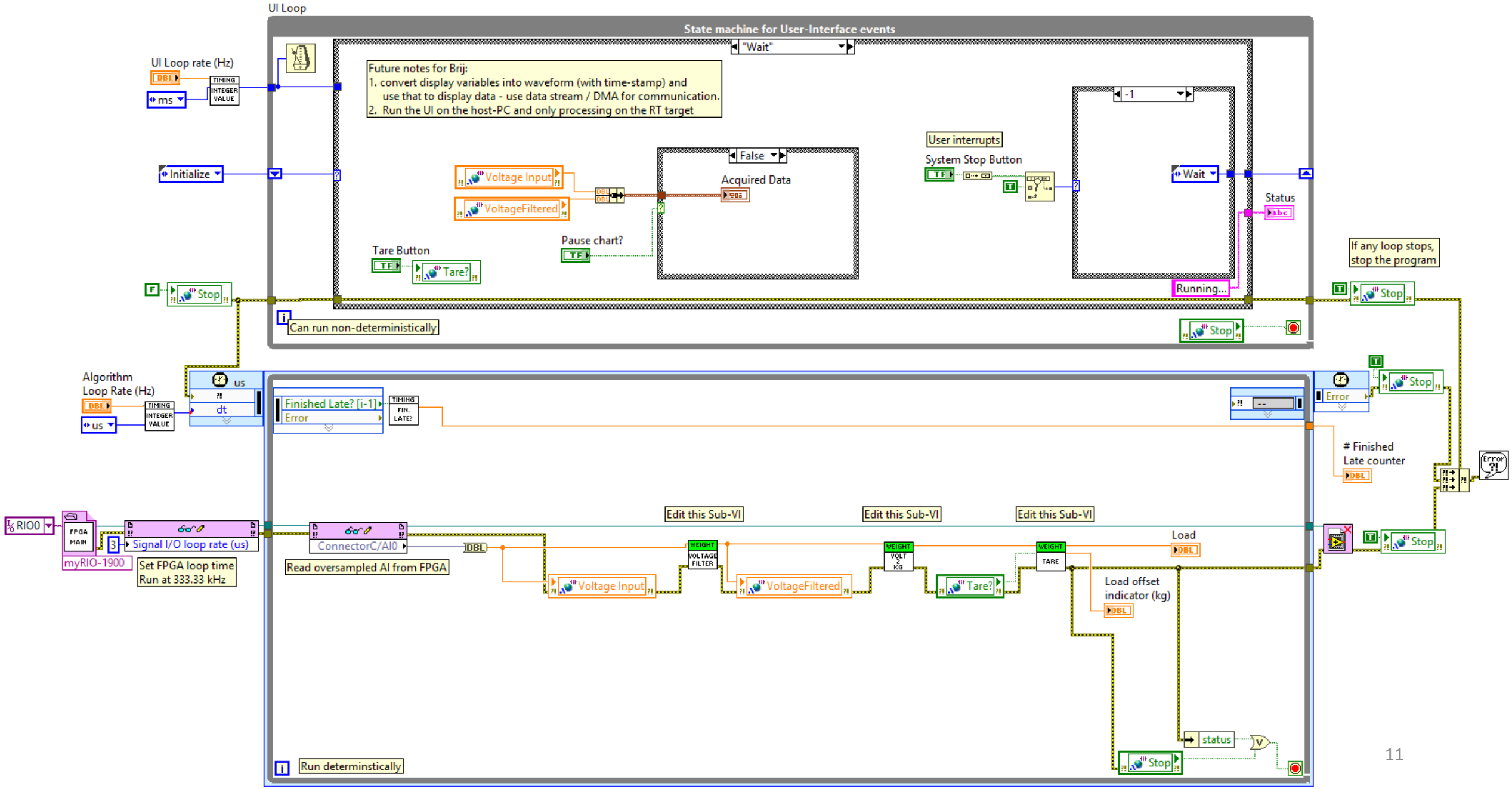
Total spread:
Max-Min = 9.776 mV

Code screenshots

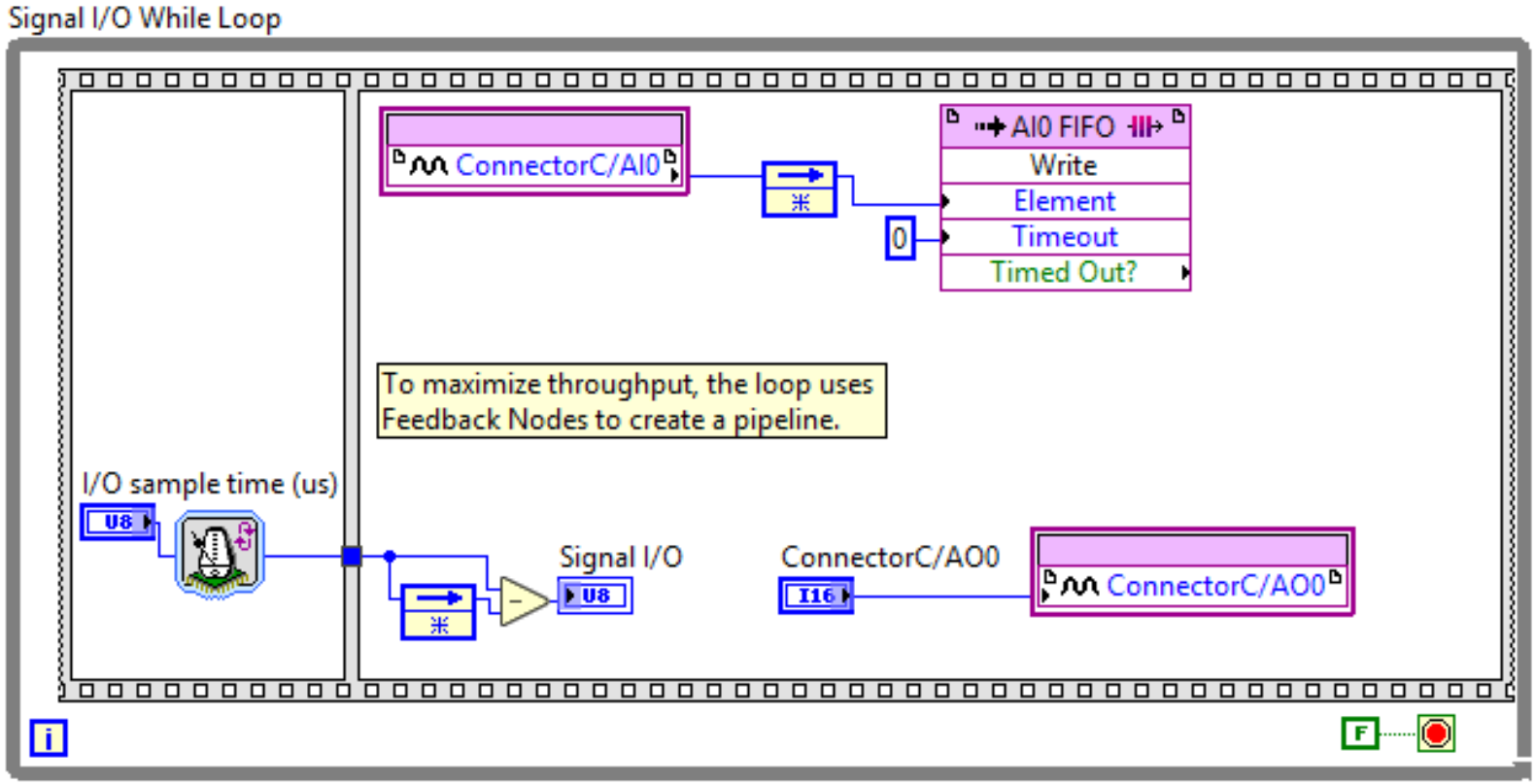
Front Panel

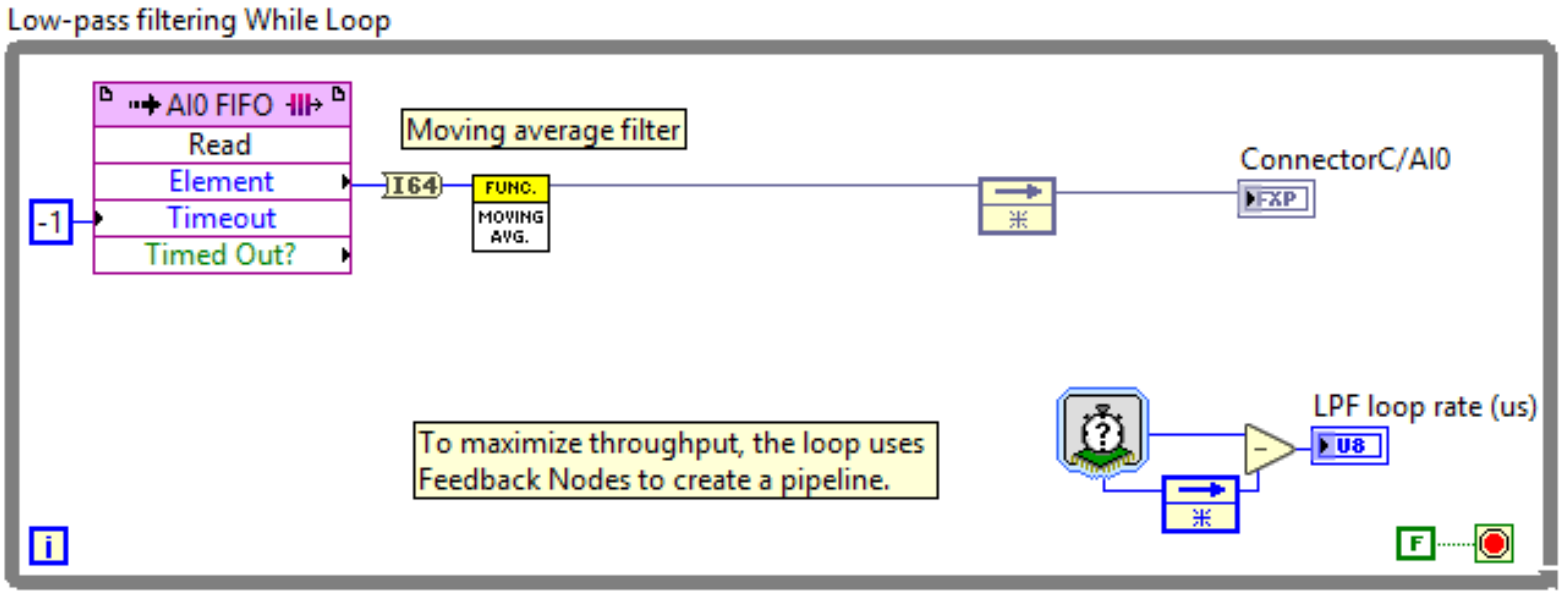

RT_Main.vi Front Panel on Weighing-Scale Reader.lvproj/BB-myRIO
File Edit View Project Operate Tools Window Help
15pt Application Font
Search
RT MAIN
2.737 Weighing-scale Reader
Loop Timing
Algo.
UI
Algorithm Loop Timing
Algorithm Loop Rate (Hz)
1k
Finished Late counter
0
Acquired Data
Raw input
Filtered
Voltage [V]
-0.0102
-0.0103
-0.0104
-0.0105
-0.0106
-0.0107
-0.0108
-0.0109
-0.0110
-0.0111
-0.0112
0.8 1 1.2 1.4 1.6 1.8 2 2.2 2.4 2.6 2.8 3 3.2 3.4 3.6 3.8 4 4.2 4.4 4.6 4.8 5 5.2 5.4 5.6 5.8
-0.011
-0.01
Time [sec]
Pause chart?
Stop ?
Status
Stopped.
Tare
Load offset indicator (kg)
0
Load
-0.0107
kg

Block diagram



FPGA Block-diagram

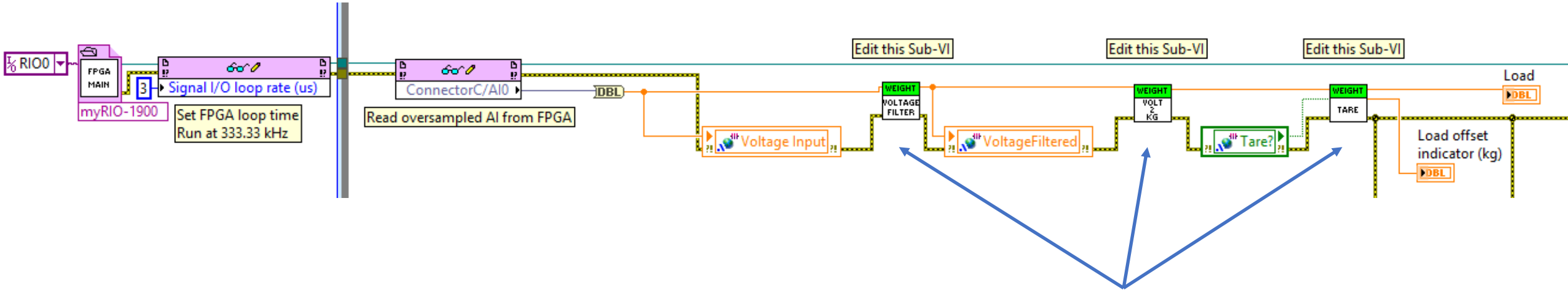




Tasks

Modify the 3 sub-VIs

- Implement any further filtering if you would like.
- Write to code to convert from voltage to weight measurement.
- Write code to implement tare functionality on pressing the tare button.



Double-click to open sub-VI and modify to implement your own code.

References

- https://forums.ni.com/t5/Example-Programs/Convert-Sine-Wave-Generator-Raw-Output-to-Fixed-Point/ta-p/3530621
- https://forums.ni.com/t5/LabVIEW/Moving-Average-Filter/td-p/2550513
- https://terpconnect.umd.edu/~toh/spectrum/Smoothing.html
- http://www.cypress.com/file/236481/download