Coral

Design of Power Supply Distribution Networks for EdgeTPU chips

The Problem

EdgeTPU chips are designed to accelerate a certain type of operations typically associated with neural networks. This means that their use is bursty in nature, their services being required only when those operations are needed and being completely idle -save from some inconsequential baseline power- for the rest of the time. On the other hand, those operations typically require a large amount of arithmetic logic units (ALUs) to be activated simultaneously, the exact number being model dependent. The last two statements result in a profile that shows very high peaks of current for very short intervals of time followed by periods of inactivity that are relatively long when compared to the peaks. The following picture shows the load transient on the 3.3V input of a Coral edgeTPU module for a power supply that was designed only considering the maximum expected current of the module itself (~2.5A_{MAX} for the 3.3V rail) and with no regards to transient behavior of the converter.

Voltage Transient Measured on a Poorly Optimized Voltage Converter

As can be seen from the plot, the input voltage rail (yellow trace, AC Coupling, 200mV/div) sees variations in excess of 400mV$_{PP}$ leading eventually to brownout of the module itself.

In this case the input voltage to the DC/DC converter is 12V, which -given the nature of switching buck converters- minimizes the disruption to the voltage rail. In the case where the DC/DC converter was powered at 5V -for example from a USB connector- the resulting transient in the output voltage rail can be considerably worse given the smaller voltage difference across the voltage regulator.

The repeated bursts of activity -in the case of the picture above a model for face recognition- promote extreme care in the design of DC/DC converters that power edgeTPU modules in order to avoid the wide variations on the input voltage rail as a consequence of sudden current draw. Part of EVT characterization of any product using an EdgeTPU must include a complete evaluation of the PDN in order to minimize the load transient experienced by the PDN as a consequence of the specific model being used. The last part of the sentence is meant to clarify that whatever optimization is performed is necessarily highly dependent on the model that will be run in the TPU, with different models generating widely different current profiles. The recommendations of this application note thus can only be generic. Final optimization is by necessity project specific.

The degrees of freedom available to the power supply designer are dependent on the design itself. This application note will outline a few possible areas that can help in designing a robust DC/DC converter but the

manufacturer of whatever part is used has already written extensively about all of these subjects in a level of detail that cannot be duplicated in this application note. This document is not meant to replace that information but to give a description of the problem of powering EdgeTPU devices and a broad overview of possible solutions. The careful designer will then look for more specific information through the manufacturer of the regulator used.

The DC/DC Converter's Loop Bandwidth

The Role of Loop Bandwidth

The speed with which the DC/DC regulator can follow and react to the voltage fluctuations that result from load transients is -by and large- dependent on the bandwidth of the DC/DC regulator's control loop. The control of the regulator loop becomes an important factor for the proper design of a power distribution network.

Some regulators expose the loop compensation network to the user so that a passive network that maximizes the loop bandwidth of the individual application can be synthesized: While more complicated, these converters allow full control of the loop characteristics. On the other side of the spectrum we have converters with an internal compensation network. These are simpler devices to design with but they have a more limited ability to optimize the loop characteristics.

It must also be stressed that in most devices the loop bandwidth is usually tuned to be a percentage of the switching frequency F_s, typically chosen to be between $F_s/8$ and $F_s/10$. Switching regulators with higher switching frequencies will then be preferable for applications like edgeTPUs because of their inherent superior ability to track output voltage variations.

Loop Control Techniques

There are a variety of control techniques used for loop compensation. The reader is referred to the wealth of information that is available through various controller manufacturers for a detailed study of the pros and cons of them. Among the many types, regulators that employ a Constant On Time (COT) loop policy are an excellent choice because of their speed. By doing away with the error amplifier and an internal clock, both of which contributed to delays to the feedback loop, the loop response time has been decreased. The drawback is that ripple in the output voltage is used by the control loop itself and so COT regulators show a somewhat higher voltage ripple, which typically must be in the range of 50 mV to 100 mV. In the case of the Google Coral module a certain amount of ripple in the input voltage can be very easily tolerated because of the internal DC/DC converter that generates all the voltage rails from the 3.3 Volt supply.

Compensation Network

The response of the DC/DC converter is dependent on the properties of the feedback loop of the regulator itself, expressed in terms of the location of poles and zeros of its transfer function. The location of the poles and zeros can be modified by the user in different ways.

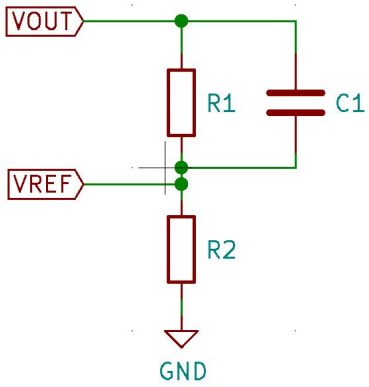
As previously stated the compensation network of any given converter can be internal, in which case little can be done to change it, or it can be external, in which case a pin or two are set aside to connect to an RC

network made of discrete components the topology of which falls into some very well studied patterns. The possible changes available to the designer will depend on which type of regulators we are working with.

Internal Compensation network

When the compensation network is internal to the device the only place in which the designer can act are the external feedback resistors that provide a snapshot of the output voltage to be compared with a reference voltage.

There are a number of ways in which capacitors can be connected to the feedback resistors[1]. In most cases a single feedforward capacitor placed across the top resistor will have a marked effect on the phase margin. With the addition of a zero at the appropriate frequency the control loop can respond faster to variations in the voltage rail.



The exact value of the capacitor is dependent on the regulator used and can vary between a few tens and a few hundreds of pF. Simulation tools -usually provided by the manufacturer- can be used to find a ballpark value, and trial and error can refine the choice.

External Compensation network

Converters that expose their compensation network allow the user to fine tune the bandwidth of the converter through appropriate choice of compensation network and the components of it. There are 3 different types of compensation networks that have been extensively studied and each regulator is designed of one of them and the datasheet provides the information necessary to determine its components.

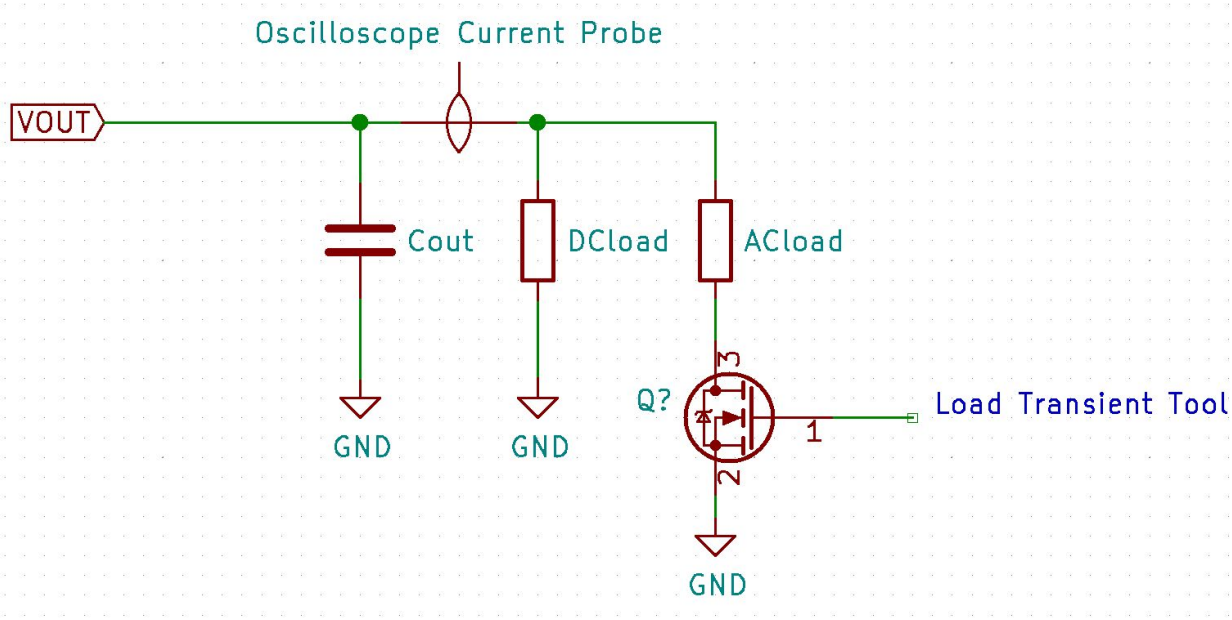
As always, the goal is to choose a configuration that maximizes the speed of the control loop.

Optimizing the Load Transient

Load transient can be measured through the use of a load transient generator tool. In their simplest incarnation these tools are composed of a MOSFET that opens and closes at a specific duty cycle the frequency and duty cycle of which can be set by the user in order to simulate actual conditions. When the MOSFET closes it shunts a resistor across the output of the DC/DC regulator thus providing a changing load to the converter.

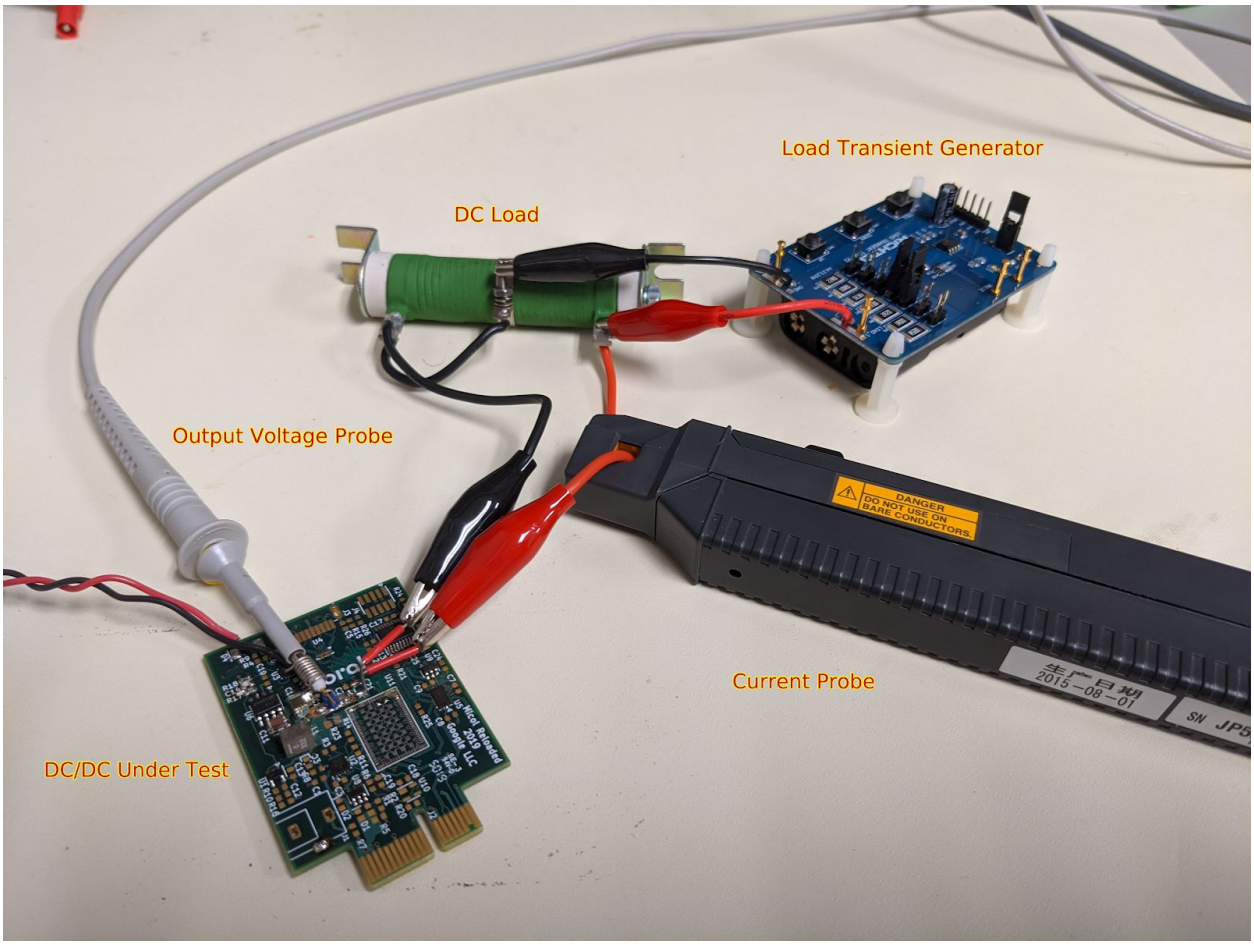
[1]For a exhaustive treatment of the various possibilities see https://www.ti.com/lit/pdf/slva289

Optionally, an additional resistor provides a static load. Both the load current -measured with a current probe- and the output voltage -AC coupled- are monitored by means of an oscilloscope.



The goal in this case is to emulate the static and dynamic currents that are generated by the TPU while running models.

A typical test setup looks like the following picture.

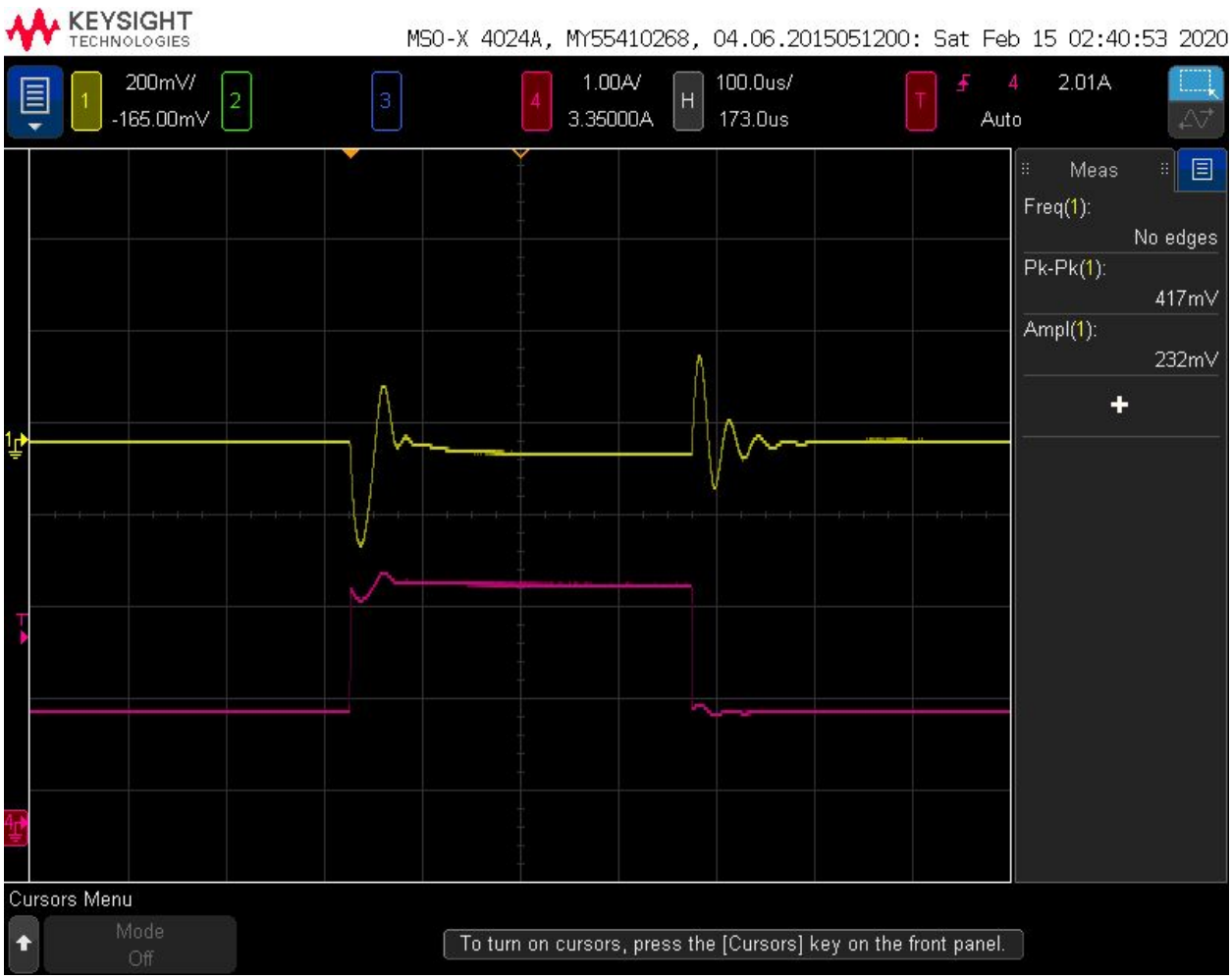


The DC load provides a constant load to the DC/DC regulator. In this case the DC loads emulates the steady state power consumption of the EdgeTPU and the variable resistor is tuned to provide about 200 mA of current.

The load transient generator is connected in parallel with the DC load and -for this device- the pulse width is tuned via the small switch buttons visible on the board.

Notice the way the output voltage probe is connected to the circuit. A wire wrapped around the tip of the probe minimized the loop between ground and tip, thus leading to a reduction of the external noise picked up by the probe. This consideration is important given the switched nature of the DC/DC converter.

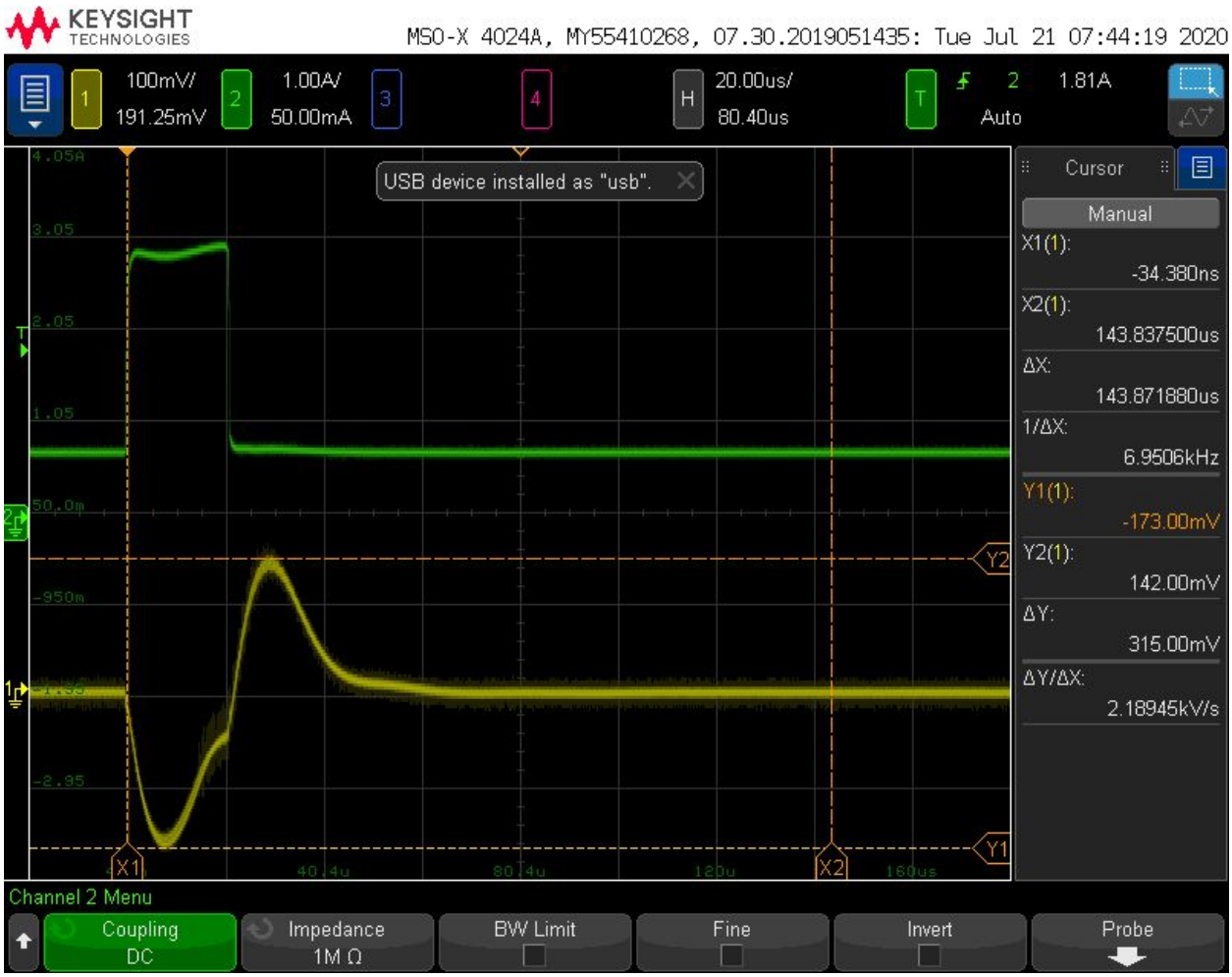
The resulting scope shot looks more or less like the one shown in the picture below where the yellow trace is the regulated voltage, while the magenta trace is the input current to the DC/DC converter. As it can be seen, the load has a static 1.3A current to which an additional 1.3A is added.



The effect on the output voltage is readily appreciated in the swings caused by the load transitions from 1.3 to 2.6A. At 200mV/div the swing on the 3.3V supply goes from roughly +/-210mV.

Notice also how the output voltage seems to oscillate for a few cycles before finally settling down. The role of DC/DC optimization is to work on the location of poles and zeros of the transfer function in order to minimize the voltage swing of the regulated voltage and reduce the oscillations that can result from unoptimized loops. The maximum voltage swing allowed must be within the allowable range of the edgeTPU.

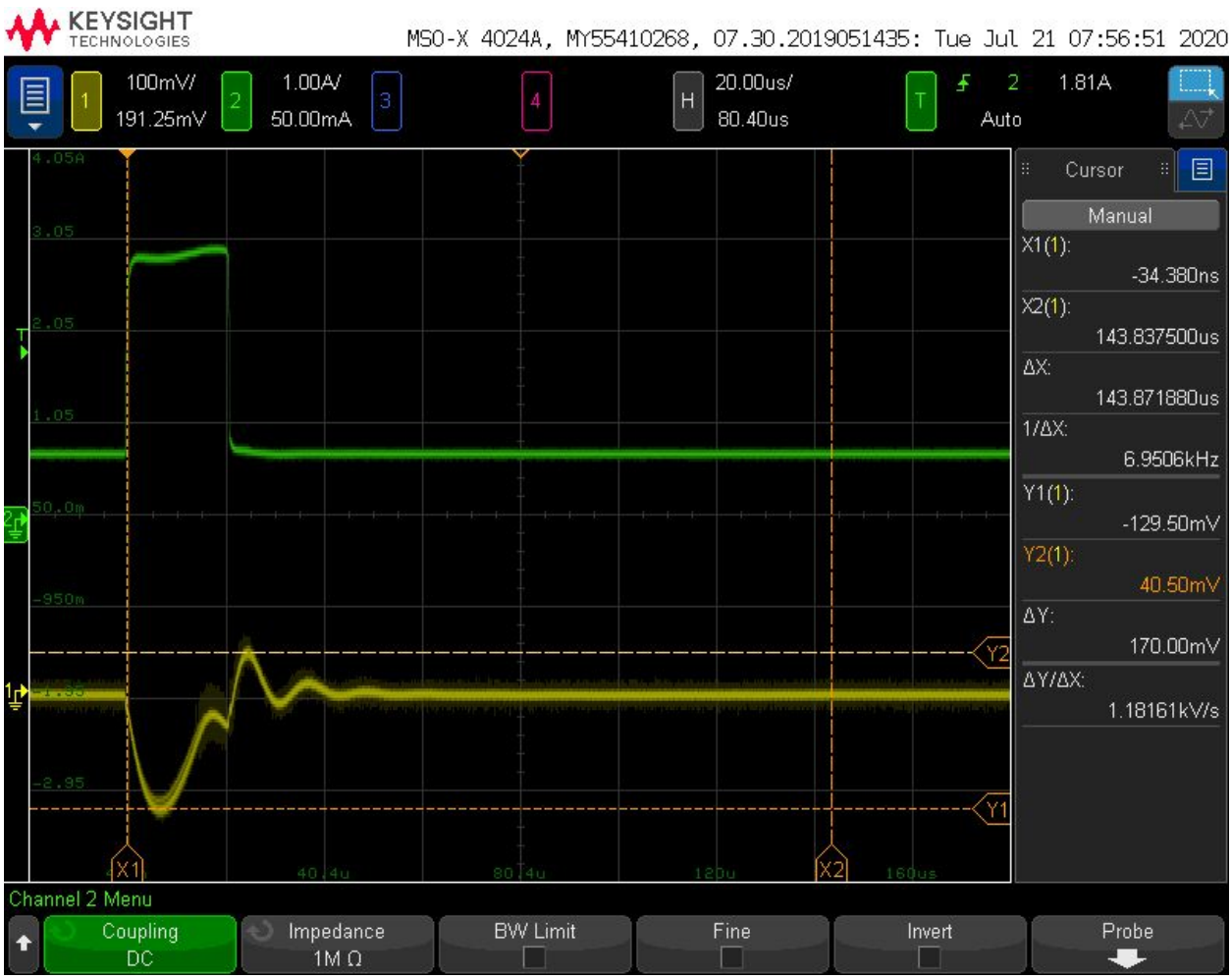
In the following picture the output current of the DC/DC converter is measured with a current pulse with features similar to those found in running ML models. In this case the DC/DC regulator has no feedforward capacitor and the output voltage (yellow trace) is measured in AC mode.



The output voltage ripple is 315 mV, almost 10% of the 3.3 V output voltage of this regulator

The following picture shows the same test run when a 470 pF feedforward capacitor is used in the DC/DC regulator. The effect of the feedforward capacitor can be readily appreciated in the lower ripple on the DC rail, now reduced to 170 mV. This represents about 5% noise on a 3.3V rail. Further improvement can be obtained with a trial and error approach to finding a more optimized value for the feedforward capacitor.

Notice also the onset of damped oscillations on the output rail.

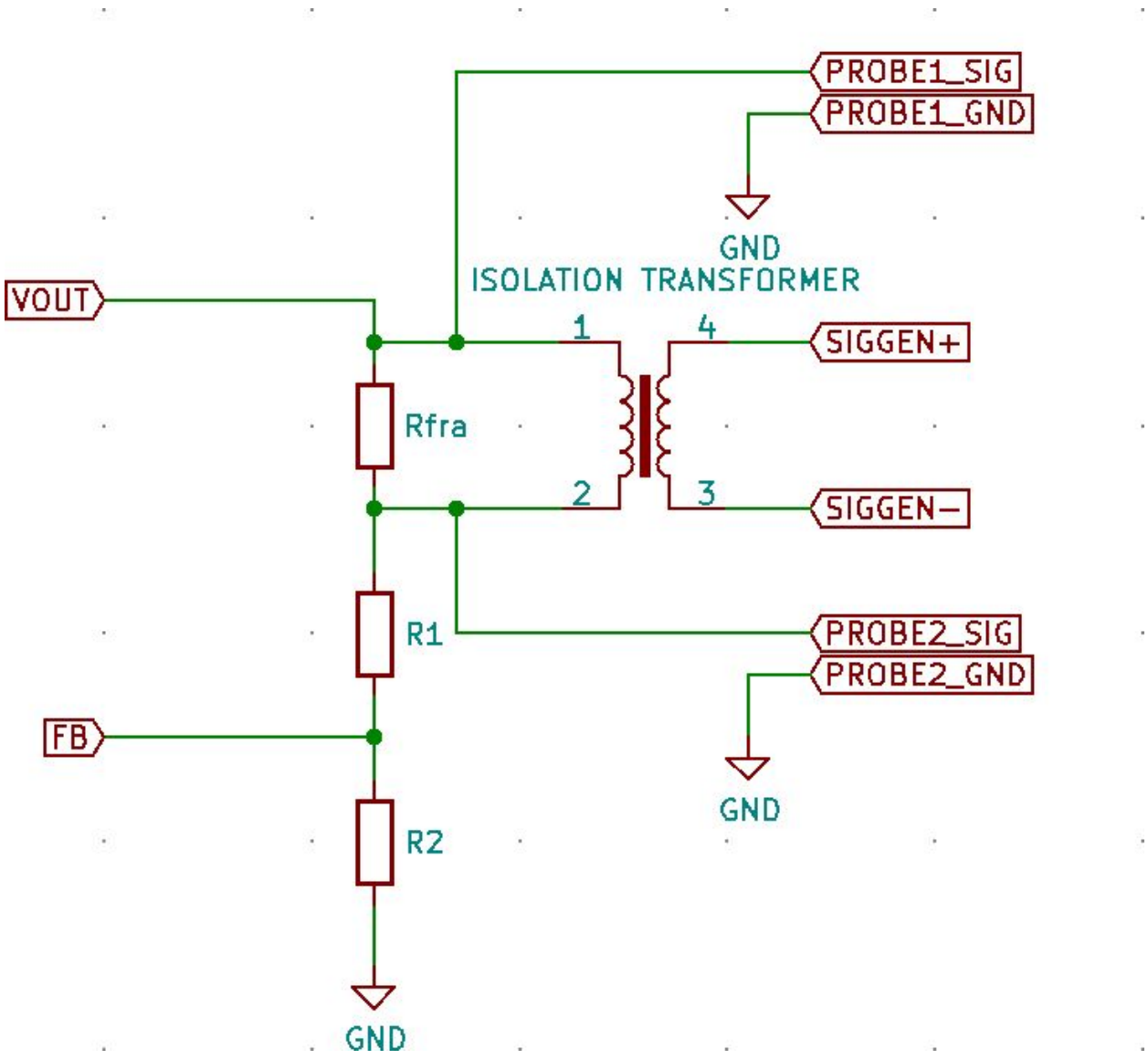


Measuring the Loop Bandwidth

A more detailed view of the loop bandwidth can be obtained by using a frequency response analyzer (FRA). Today the FRA functionality can be found as an add-on to an oscilloscope and they work by breaking the feedback loop at a specific point and injecting a sinusoidal signal the frequency of which is swept between two limits. Using the oscilloscope to measure the input and the output signal and calculating the transfer function at each frequency, thus obtaining a frequency response.

Other than oscilloscopes, the FRA functionality can be purchased separately, with tools that either rely on a separate oscilloscope or include the oscilloscope functionality.

The following picture shows the connections for measuring the loop response using a FRA.



Injecting the signal

As it can be seen the resistive divider path at the output of a DC/DC converter (R1/R2) is broken and an additional resistor is placed in series. The value of this resistor should be high enough to provide a load to the signal generator but small enough not to unbalance in any meaningful way the resistive divider. Typically any value between 10 and 50 Ohm will realistically work.

The signal is injected into the feedback loop with an isolation transformer so that, once again, the DC bias of the feedback loop is not modified.

The signal injected into the loop (PROBE2) then goes around the loop and the effect of the perturbation is then measured at the output (PROBE1).

Phase Margin

The result of this analysis is a chart that provides a plot of gain (usually in dB) and phase of the transfer function of the feedback loop. The phase margin is the most common figure of merit cited in a frequency response analysis and it is defined as the phase shift at the frequency at which the amplitude plot crosses the 0dB gain.

The load transient test and the phase margin test are performed in completely different ways bu there is a relationship between the two[2]: The higher the phase margin the smallest the overshoot. The problem then reduces to finding the largest phase margin that leaves us with an acceptable overshoot that avoids brownouts. As can be seen from Mr. Basso's article, whereas canonic stability theory claims that a phase margin of 45 degrees is enough for most systems, this small margin leads to a fairly large overshoot on the load transient response. For power supplies a much better choice would be to increase the phase margin to 60 to 75 degrees.

The Effect of the Output Capacitor

The output capacitor of the DC/DC converter has a considerable effect on the output ripple. A larger capacitor can act as a reservoir that will help smooth the transition on the output rail. Just for reference, the following picture shows the setup already described where the output capacitance has been increased from 100uF (in the previous tests) to 220 uF, keeping the rest of the setup identical. No feedforward capacitor has been added.

[2] https://cbasso.pagesperso-orange.fr/Downloads/Papers/Phase%20margin%20and%20quality%20factor.pdf

Increasing the output capacitance is a quick and easy way to reduce ripple but once the cost and durability of large capacitors are factored into the design the solution looks far less attractive. The quick fix of a large capacitor should not be a substitute for a well optimized DC/DC converter.

References:

- Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor, Texas Instruments SLVA280 Application Note. https://www.ti.com/lit/pdf/slva289
- Advantages of Constant-On-Time Control in DC/DC Converters, Monolithic Power, https://www.monolithicpower.com/en/advantages-of-constant-on-time-control-in-dc-dc-converters