MICHAEL B. SULLIVAN

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RESEARCH INTERESTS	I am interested in the design of dependable and efficient computer systems. My current research provides strong-yet-inexpensive reliability in computer memory and arithmetic.

PROFESSIONAL EXPERIENCE

NVIDIA Corporation, Santa Clara, CA
Research Scientist, Architecture Research Group (ARG) — 2015–

Research Assistant Positions
University of Texas, Austin, TX — 2010–2015
Los Alamos National Laboratory (LANL), Los Alamos, NM — 2011
George Mason University, Fairfax, VA — 2007–2008
Argonne National Laboratory, Argonne, IL — 2007
University of California at Irvine, Irvine, CA — 2007

EDUCATION

University of Texas, Austin, TX
Ph.D. in Computer Engineering — 2015
M.S.E. in Computer Engineering — 2011

George Mason University, Fairfax, VA
M.S. in Computer Science — 2009
B.S. in Computer Engineering and B.A. in Mathematics, summa cum laude — 2007

SELECTED PUBLICATIONS

"SwapCodes: Error Codes for Hardware-Software Cooperative GPU Pipeline Error Detection," in the *International Symposium on Microarchitecture (MICRO)*. — 2018

"Understanding Error Propagation in Deep Learning Neural Network (DNN) Accelerators and Applications," in the *Conference on High Performance Computing, Networking, Storage and Analysis (SC)*. — 2017

"All Inclusive ECC: Thorough End-to-End Protection for Reliable Computer Memory," in the *International Symposium on Computer Architecture (ISCA)*. — 2016

"Bamboo ECC: Strong, Safe, and Flexible Codes for Reliable Computer Memory," in the *Symposium on High Performance Computer Architecture (HPCA)*. — 2015

"Containment Domains: A Scalable, Efficient, and Flexible Resilience Scheme for Exascale Systems," in the *Conference on High Performance Computing, Networking, Storage and Analysis (SC)*. — 2012

SELECTED AWARDS

Cockrell School of Engineering Fellowship — 2011–13
National Defense Science & Engineering (NDSEG) Graduate Fellowship — 2008–11
Outstanding Achievement Award in Graduate Computer Science — 2009
GMU University Scholar — 2004–08

HARDWARE

VHDL/Verilog and the Synopsys tools for RTL design and analysis; binary instrumentation and workload characterization; microarchitectural simulation.

SOFTWARE

C/C++, Matlab, Python; Cuda/OpenCL/MPI/OpenMP; exact & heuristic optimization.