On Separable Arithmetic Error Detection for Reliable Computation

Michael Sullivan

Rising levels of integration and decreasing component reliabilities make error protection increasingly important. At the same time, the need for energy efficiency necessitates the careful evaluation of resilience techniques. Arithmetic error protection is typically more expensive than the protection of memory or data movement, requiring large amounts of redundant logic. Protection of the arithmetic pipeline has correspondingly been reserved for critical or high-availibility applications. Current trends, however, indicate that low-cost arithmetic error detection will be necessary in the future for more diverse application areas.

Arithmetic error coding offers the ability to lower the hardware and energy overheads of arithmetic error protection, but it does so at the expense of high design-effort and holes in error coverage. The goal of this work is to mitigate the deficiencies of duplication and arithmetic error coding to form a scheme that may be readily employed in future systems. Ultimately, this work will produce novel mechanisms that provide strong, non-intrusive error detection within an existing optimized arithmetic pipeline. Work will proceed in three steps, each of which is outlined below.

Low-Cost, Separable Error Detection for Addition

Addition is ubiquitous in computer systems, and errors in addition carry a high risk of silent data corruption. Despite this, error detection in adders remains costly. This work will introduce a family of separable error detection techniques that is flexible enough to provide superior error detection efficiency for a variety of adders, taking into account different adder designs, pipeline depths, and short-vector addition.

Approximate Duplication

The speed and integration of modern devices have risen to the point that arithmetic can be performed very fast and with high precision. While precise arithmetic is important in the arithmetic pipeline, full-precision duplication for error detection is an inefficient use of chip resources and energy. This work will develop reduced-precision fixed-point arithmetic units, focusing on the energy needed per bit of precision and the ability to provide multiple levels of precision at varying costs. Once developed, these units will be utilized for error detection through *approximate duplication*. Approximate duplicate units will provide low-cost error detection, comparable to traditional error coding techniques, while lowering error detection latencies and minimizing the magnitude of any undetected errors.

The reduced-precision functional units used for approximate duplication will be based on approximate logarithmic computations, with a focus on multiplication and division. While approximate logarithmic computations have the benefit of decades of prior arithmetic research, no existing work has focused on providing varying levels of precision or has addressed their use for error detection.

Separable Floating-Point Error Detection

While much academic research has focused on error detection for fixed-point operations, research in error detection for floating-point units is sparse. In addition, all prior low-cost code-based error detectors for floating-point arithmetic require communication between the floating-point unit and the code generation logic, violating separability.

Having developed precision-proportional fixed-point units, this work will extend the concept of approximate duplication to the realm of floating-point operations. These reduced-precision floating point checkers will be employed as the first low-cost/high-coverage separable error detection mechanism for floating-point arithmetic.