MICHAEL B. SULLIVAN

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RESEARCH INTERESTS

I am interested in the design of dependable and efficient computer systems. My current research provides strong-yet-inexpensive reliability in computer memory and arithmetic.

EDUCATION

University of Texas, Austin, TX
Ph.D. Student in Computer Engineering 2008–present
– Advisors: Mattan Erez & Earl E. Swartzlander, Jr.
– Dissertation:
On Separable Arithmetic Error Detection for Reliable Computation
M.S.E. in Computer Engineering May 2011

George Mason University, Fairfax, VA
M.S. in Computer Science Jan 2009
B.S. in Computer Engineering and B.A. in Mathematics, summa cum laude May 2007

SELECTED AWARDS

Cockrell School of Engineering Fellowship 2011–13
National Defense Science & Engineering (NDSEG) Graduate Fellowship 2008–11
Outstanding Achievement Award in Graduate Computer Science 2009
GMU University Scholar 2004–08

SELECTED PUBLICATIONS

"Bamboo ECC: Strong, Safe, and Flexible Codes for Reliable Computer Memory," in the *International Symposium on High Performance Computer Architecture (HPCA)*, February 2015.

"A Locality-Aware Memory Hierarchy for Energy-Efficient GPU Architectures," in the *International Symposium on Microarchitecture (MICRO)*, December 2013.

"Truncated Logarithmic Approximation," in the *International Symposium on Computer Arithmetic (ARITH)*, April 2013.

"Containment Domains: A Scalable, Efficient, and Flexible Resilience Scheme for Exascale Systems," in the *Conference on High Perf. Computing, Networking, Storage and Analysis (SC)*.

PROFESSIONAL EXPERIENCE

University of Texas, Austin, TX
Research Assistant, Locality Parallelism and Hierarchy Lab (LPH) 2010–present

Los Alamos National Laboratory (LANL), Los Alamos, NM
Research Assistant, Applied Computer Science(CCS-7) 2011

George Mason University, Fairfax, VA
Research Assistant, Lab for the Study and Simulation of Human Movement 2008
Research Assistant, Neural Engineering Lab 2007–08

Argonne National Laboratory, Argonne, IL
Research Assistant, Mathematics and Computer Science (MCS) 2007

University of California at Irvine, Irvine, CA
Research Assistant, Nanotechnology Lab 2006

HARDWARE

VHDL/Verilog and the Synopsys tools for RTL design and analysis; Pin for binary instrumentation and workload characterization;Gem5 for microarchitectural simulation.

SOFTWARE

C/C++, Matlab, Python; Cuda/OpenCL/MPI/OpenMP; exact & heuristic optimization.