

MICHAEL B. SULLIVAN

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RESEARCH INTERESTS	I am interested in the design of dependable and efficient computer systems. My current research provides strong-yet-inexpensive reliability in computer memory and arithmetic.	
EDUCATION	University of Texas, Austin, TX	
	<i>Ph.D. Student in Computer Engineering</i>	2008–2015
	– Advisors: Mattan Erez & Earl E. Swartzlander, Jr.	
	<i>M.S.E. in Computer Engineering</i>	May 2011
	George Mason University, Fairfax, VA	
	<i>M.S. in Computer Science</i>	Jan 2009
	<i>B.S. in Computer Engineering and B.A. in Mathematics, summa cum laude</i>	May 2007
SELECTED AWARDS	Cockrell School of Engineering Fellowship	2011–13
	National Defense Science & Engineering (NDSEG) Graduate Fellowship	2008–11
	Outstanding Achievement Award in Graduate Computer Science	2009
	GMU University Scholar	2004–08
SELECTED PUBLICATIONS	“Bamboo ECC: Strong, Safe, and Flexible Codes for Reliable Computer Memory,” in the <i>International Symposium on High Performance Computer Architecture (HPCA)</i> , February 2015.	
	“A Locality-Aware Memory Hierarchy for Energy-Efficient GPU Architectures,” in the <i>International Symposium on Microarchitecture (MICRO)</i> , December 2013.	
	“Truncated Logarithmic Approximation,” in the <i>International Symposium on Computer Arithmetic (ARITH)</i> , April 2013.	
	“Containment Domains: A Scalable, Efficient, and Flexible Resilience Scheme for Exascale Systems,” in the <i>Conference on High Perf. Computing, Networking, Storage and Analysis (SC)</i> .	
PROFESSIONAL EXPERIENCE	NVIDIA Corporation, Santa Clara, CA	
	<i>Research Scientist, Architecture Research Group (ARG)</i>	2015–present
	University of Texas, Austin, TX	
	<i>Research Assistant, Locality Parallelism and Hierarchy Lab (LPH)</i>	2010–2015
	Los Alamos National Laboratory (LANL), Los Alamos, NM	
	<i>Research Assistant, Applied Computer Science (CCS-7)</i>	2011
	George Mason University, Fairfax, VA	
	<i>Research Assistant, Lab for the Study and Simulation of Human Movement</i>	2008
	<i>Research Assistant, Neural Engineering Lab</i>	2007–08
	Argonne National Laboratory, Argonne, IL	
	<i>Research Assistant, Mathematics and Computer Science (MCS)</i>	2007
HARDWARE	University of California at Irvine, Irvine, CA	
	<i>Research Assistant, Nanotechnology Lab</i>	2006
	VHDL/Verilog and the Synopsys tools for RTL design and analysis; Pin for binary instrumentation and workload characterization; Gem5 for microarchitectural simulation.	
SOFTWARE	C/C++, Matlab, Python; Cuda/OpenCL/MPI/OpenMP; exact & heuristic optimization.	