**Commodore Semiconductor Group**

A division of Commodore Business Machine, Inc.

**390537 DMA Controller (Super DMAC)**

# Description

The 390537 Is a Direct Memory Access Controller designed using 2 micron CMOS gate-array technology for use with the Commodore Amiga rage of personal computers. The controller aims to reduce the cost of adding peripheral devices (i.e SCSI and XT/AT Devices) to the Amiga.

The controller is capable of full 32bit direct DMA and contains a FIFO capable of storing four 32bit longwords (16 Bytes), bus arbitration logic and a 16bit general IO port (this can be split into two 8bit ports). Address generation is not performed by the SDMAC itself due to restrictions on pin count. The RAM controller (Ramsey 390541) will generate the addresses during DMA cycles.

# Package

All known revisions of the IC are packaged as PLCC 84 (see below for pin numbering)

Diagram

Description automatically generated

# Revisions

There are two known production revisions and at least one prototype version of the of this IC.

## Rev 02

Commonly found in the Amiga 3000 Desktop machine.

## Rev 04

Commonly found in the Amiga 3000 Tower machine.

Addition of 2nd 8 bit peripheral device port, or option for combining as one 16 bit port.

## Rev AA3000 prototype

This version of the IC had some significant changes:

* Addition of i2c port on pins 56 & 57
* Increase the FIFO depth to 8 32bit long words (32 bytes).
* Introduction of additional registers and deprecating some of the original ones.

# Signals

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin | Rev2 | Rev4 | AA3000 | Description |
| 1..20 | D0..D19 | D0..D19 | D0..D19 | Processor Data Bus |
| 21 | VCC | VCC | VCC | +5V DC |
| 22..33 | D20..D31 | D20..D31 | D20..D31 | Processor Data Bus |
| 34 | INTB | INTB | INTB | Pulled up to VCC via 1k. not connected to anything else. |
| 35 | \_INT | \_INT | \_INT | Interrupt output (\_INT2) |
| 36 | SIZ1 | SIZ1 | SIZ1 | Transfer Size |
| 37 | R\_W | R\_W | R\_W | Read/Write |
| 38 | \_AS | \_AS | \_AS | Address Strobe |
| 39 | \_DS | \_DS | \_DS | Data Strobe |
| 40 | \_DSACK1 | \_DSACK1 | \_DSACK1 | Data transfer and size acknowledge |
| 41 | \_DSACK0 | \_DSACK0 | \_DSACK0 | Data transfer and size acknowledge |
| 42 | VSS | VSS | VSS | GND |
| 43 | \_STERM | \_STERM | \_STERM | Synchronous Termination (bus cycle) |
| 44 | SCLK | SCLK | SCLK | Clk input (CPUCLKB) 16/25MHz |
| 45 | \_CS | \_CS | \_CS | Chip select (\_SCSI) |
| 46 | \_RESET | \_RESET | \_RESET | Reset chip (connected to \_IORST) |
| 47 | \_BERR | \_BERR | \_BERR | Bus Error |
| 48..55 | PD0..PD7 | PD0..PD7 | PD0..PD7 | Peripheral device data port (SCSI) |
| 56 | NC | PD8 | CNT | Peripheral device data port (AA3000/+ i2c) |
| 57 | NC | PD9 | SP | Peripheral device data port (AA3000/+ i2c) |
| 58 | NC | PD10 | AP\_0 | Peripheral device data port (AA3000/+DSP) |
| 59 | NC | PD11 | AP\_1 | Peripheral device data port (AA3000/+DSP) |
| 60 | NC | PD12 | AP-2 | Peripheral device data port (AA3000/+DSP) |
| 61 | NC | PD13 | VSS | A3000 not connected (AA3000/+ GND) |
| 62 | NC | PD14 | AP\_3 | Peripheral device data port (AA3000/+DSP) |
| 63 | VCC | VCC | VCC | +5V DC |
| 64 | NC | PD15 | AP\_4 | Peripheral device data port (AA3000/+DSP) |
| 65 | \_DREQ | \_DREQ | \_DREQ | Peripheral Port Data Request |
| 66 | \_DACK | \_DACK | \_DACK | Peripheral Port Data Acknowledge |
| 67 | \_CSS | \_CSS | \_CSS | Peripheral Port 0 chip select (SCSI) |
| 68 | \_IOW | \_IOW | \_IOW | Peripheral Port Write |
| 69 | \_IOR | \_IOR | \_IOR | Peripheral Port Read |
| 70 | \_CSX0 | \_CSX0 | AP\_5 | Peripheral Port 1A chip select (AA3000/+DSP) |
| 71 | \_CSX1 | \_CSX1 | AP\_6 | Peripheral Port 2 chip select (AA3000/+DSP) |
| 72 | \_IORDY | \_IORDY | \_IORDY |  |
| 73 | INTA | INTA | INTA | Peripheral Port 0 interrupt request (SCSI) |
| 74 | INC\_ADD | INC\_ADD | AP\_7 | A3000 not connected, (AA3000/+ DSP) |
| 75 | \_DMAEN | \_DMAEN | \_DMAEN | Enable Ramsey as address generator for DMA cycle |
| 76..80 | A2..A6 | A2..A6 | A2..A6 | Processor Address Bus |
| 81 | \_BR | \_BR | \_BR | Bus Request |
| 82 | \_BG | \_BG | \_BG | Bus Grant |
| 83 | \_BGACK | \_BGACK | \_BGACK | Bus Grant Acknowledge |
| 84 | VSS |  | VSS | GND |

# Registers

Address decoding for the SDMAC is done by the gate array Fat Gary (390540) in the Amiga 3000. Fat Gary will assert the SCSI signal in the Address rage **0x00DD0000 - 0x00DD3FFF**.

The SCSI signal is connected to the chip select of the SDMAC (pin 45)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Address | Length | Name | Type | Description |
| $00 | 2bit | DAWR | Write | Data Acknowledge Width |
| $04 | 24Bit | WTC | R/W | Word Transfer Count |
| $08 | 8Bit | CNTR | R/W | Control Register |
| $0C | 32Bit | ACR | R/W | Address Control Register[[1]](#footnote-2) |
| $10 | 1bit | ST\_DMA | Strobe | Start DMA |
| $14 | 1bit | FLUSH | Strobe | Flush FIFO |
| $18 | 1bit | CLR\_INT | Strobe | Clear Interrupts |
| $1C | 32Bit | ISTR | Read | Interrupt Status Register |
| $20,$24,$28,$2C |  | - |  | \*RESERVED FOR FUTURE USE\* |
| $30,$34,$38 |  | - |  | \*RESERVED FOR FUTURE USE\* |
| $3C | 1bit | SP\_DMA | Strobe | Stop DMA |
| $40 - $4C | 8 bit | Port 0 | R/W | 8 bit Peripheral port (SCSI) |
| $50 - $5C | 8 bit | Port 1A | R/W | 8 bit Peripheral port (XT#0) |
| $60 -$6C | 8 bit | Port 2 | R/W | 8 bit Peripheral port (XT#1) |
| $70 -$7C | 16 bit | Port 1B | R/W | 16 bit Peripheral port (ATA/IDE) |

Text

Description automatically generated

Most DMAC control registers are not mapped strictly according to 68030 bus rules. All DMAC registers are accessed as longword-wide registers. However, they will always behave as whole longwords, even if accessed via word or byte instructions; it is impossible to independently access individual words or bytes within these registers. Therefore, any writes to DMAC registers must write all significant bits, and any reads from DMAC registers will appear to read the entire register, even if the machine op-code would claim otherwise.

/\* SuperDMAC CNTR bits. \*/

#define SCNTR\_TCEN (1<<5)

#define SCNTR\_PREST (1<<4)

#define SCNTR\_PDMD (1<<3)

#define SCNTR\_INTEN (1<<2)

#define SCNTR\_DDIR (1<<1)

#define SCNTR\_IO\_DX (1<<0)

/\* ISTR bits. \*/

#define ISTR\_INT\_F (1<<7) /\* Interrupt Follow \*/

#define ISTR\_INTS (1<<6) /\* SCSI or XT Peripheral Interrupt \*/

#define ISTR\_E\_INT (1<<5) /\* End-Of-Process Interrupt \*/

#define ISTR\_INT\_P (1<<4) /\* Interrupt Pending \*/

#define ISTR\_UE\_INT (1<<3) /\* Under-Run FIFO Error Interrupt \*/

#define ISTR\_OE\_INT (1<<2) /\* Over-Run FIFO Error Interrupt \*/

#define ISTR\_FF\_FLG (1<<1) /\* FIFO-Full Flag \*/

#define ISTR\_FE\_FLG (1<<0) /\* FIFO-Empty Flag \*/

1. The ACR is not contained in the SDMAC, this register is found in the RAM controller Ramsey, mapped at $00DD000C - $00DDFF8C repeats every $80 [↑](#footnote-ref-2)