MARK A. BUCKLER

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EDUCATION AND ACADEMIC RESEARCH

Cornell University, Ph.D. Electrical and Computer Engineering

Hardware-Software Co-Design for Efficient Embedded Vision **August 2014 – Present**

- Advised by Prof. Adrian Sampson. Dissertation is focused on leveraging full-stack knowledge of the computer vision pipeline to significantly reduce the time and energy needed for inference. Savings come from reducing *capture redundancy* via a configurable image capture pipeline, *temporal redundancy* via the estimation of and compensation for feature motion, and *spatial redundancy* via spatially compressed CNN computation.

University of Massachusetts Amherst, M.S. Electrical and Computer Engineering, May 2014
Coursework: Computer Architecture, VLSI Design, Reconfigurable Computing, Computer Networks, Entrepreneurship

Network-on-Chip Synchronization **September 2013 – May 2014**

- Advised by Prof. Wayne Burleson. Thesis centered on circuit level and Network-on-Chip (NoC) level simulation of novel synchronizer designs to reduce the impact of clock domain crossing latency on multi-core NoCs.

Rensselaer Polytechnic Institute, B.S. Electrical Engineering, May 2012
Coursework: Computer Hardware Design, Microprocessor Systems. VLSI, Microelectronics, Solid State Device Physics

Smart Lighting **January 2011 – May 2012**

- Improved color calibration and automatic gain scaling for a smart light sensor network.

SELECTED PUBLICATIONS

- *Buckler, M.*; Bedoukian, P.; Jayasuriya, S.; Sampson, A., "EVA^2: Exploiting Temporal Redundancy in Live Computer Vision" *ISCA,* June 2018
- *Buckler, M.*; Jayasuriya, S.; Sampson, A., "Reconfiguring the Imaging Pipeline for Computer Vision" *ICCV*, Oct. 2017
- *Buckler, M.*; Vaidya, A.; Liu, X.; Burleson, W., "Dynamic Latch Flip-Flop Performance in FinFET Technologies" *NOCS,* Sept. 2014
- *Buckler, M.*; Burleson, W., "Predictive Synchronization for DVFS-Enabled Multi-Processor Systems" *ISQED*, March 2014
- *Buckler, M.*; Burleson, W.; Sadowski, G., "Low-power Networks-on-Chip: Progress and remaining challenges," *ISLPED,* Sept. 2013

SELECTED PATENTS

- *Buckler, M.*, "Continuous frequency measurement for predictive periodic synchronization" US 9344099 B2, May 2016
- *Buckler, M.*; Burleson, W.; Manne, S., "Methods and systems of synchronizer selection" US 9294263 B2, March 2016
- *Buckler, M.*, "Synchronization circuits with failure-condition detection and correction" US 8,847,647 B1, Sept 2014
- *Buckler, M.,* "Video conferencing" US 8,289,363 B2, Oct 2012

PROFESSIONAL EXPERIENCE

Elucid Bioimaging Inc, Wenham, MA: *Research Contractor* **February 2018 - September 2018**

- Designed, built, and evaluated a novel image processing method for dataset augmentation and dimensionality reduction. This method alleviates challenges associated with training convolutional neural networks on moderately sized histology and radiology datasets. Applications include but are not limited to artery phenotype classification.

DeepScale Corporation, Mountain View, CA: *Summer Intern* **May 2018 - August 2018**

- Accomplished technology transfer by integrating Ph.D. research on temporal redundancy into DeepScale's self-diving vehicle computer vision pipeline. Additional responsibilities included giving internal talks on a variety of research topics and experimentation on techniques to enable smaller, faster, and more accurate convolutional neural networks.

Firebrand Innovations LLC, Wenham, MA: *Founder, CEO* **September 2012 - December 2015**

- Founded company to develop and monetize intellectual property (IP). Flagship product was VideoConversation, which started from IP held by self on advanced videoconferencing techniques. Funding was raised through prize money, a software developer was hired, and a fully functional prototype was completed.

AMD Corporation, Boxborough, MA: *Graduate Co-Op Researcher* **January 2013 - August 2013**

- Designed, developed, and simulated experimental synchronizers and clock domain crossing techniques to reduce clock domain crossing latency. Designs were verified with Verilog RTL simulations using 28nm foundry technology.

RF Diagnostics LLC, Niskayuna, NY: *Hardware Engineer* **May 2012 - August 2012**

- Designed RF PCBs including schematic capture and board layout. PCBs included a multi-channel MRI receiver board and an evaluation board for front end modules in phones.

Bose Corporation, Stowe, MA: *Summer Intern* **May 2011 - August 2011**

- Redesigned a digital signal timing test platform for Bose's automotive audio amplifiers. Improvements included system simplification and automation. Key skills included relationship management between Bose groups and contractors.

Ember Corporation (Silicon Labs as of 2012), Boston, MA: *Summer and Winter Intern* **May 2010 - January 2011**

- Tested crystal timing deviation and its effect on Ember's Zigbee network co-processor over a wide range of temperatures. Automated a temperature forcing chamber using Matlab test scripts. Brought three sets of PCBs through the entire hardware development process from researching specifications to final RF testing.

MITRE Corporation, Bedford, MA: *Summer and Winter Intern* **June 2007 - January 2010**

- Tested a prototype military communications system including a long-distance wireless link. Experience included assisting with setup/debug/calibration of prototype RF hardware. Improved software used to guide high gain dish antennas mounted on pan tilt devices to track GPS satellites.

TEACHING EXPERIENCE

Cornell University, Ithaca, NY: *Graduate Teaching Assistant* **Spring Semester, 2015**

- ECE 3140 (Embedded Systems): Assisted with grading, reviewing material with students, and debugging lab code.

TOOLS USED

Languages: Python, Halide, C, C++, Verilog, PyMTL, Matlab
Frameworks and Libraries: PyTorch, MXNet, Caffe, OpenCV, FFmpeg
Programs: Synopsys VCS, Design Compiler, and IC Compiler, Cadence Virtuoso, Quartus, PADs Layout, EAGLE

AWARDS RECEIVED

- *NVIDIA Graduate Fellowship Finalist 2018-2019*
- *Qualcomm Innovation Fellowship Abstract Selected 2018*
- *Jacobs Scholar 2014*: For strength and potential in academics, service, and leadership at Cornell
- *Inducted into Eta Kappa Nu in 2013*: IEEE's international honor society
- *Nicholas Bowen Fellowship 2013:* For excellence in computer engineering at UMass Amherst
- *Invented Here Honoree 2013:* Recognized by BPLA as one of New England's most innovative patent holders
- *UMass Innovation Challenge 2012:* Won total of $18,500 in non-dilutive and restriction free investment
- *Rensselaer Leadership Award 2008-2012:* For outstanding academic and personal achievement
- *First Place Awards:* Massachusetts State Science & Engineering Fair both 2006 and 2007
- *Eagle Scout 2007*