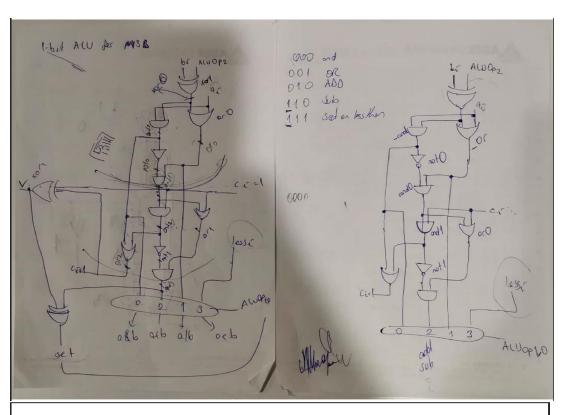
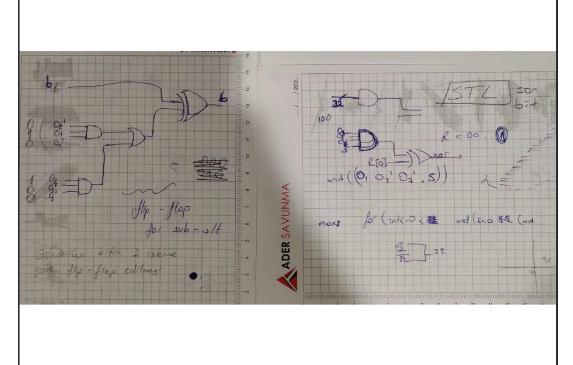
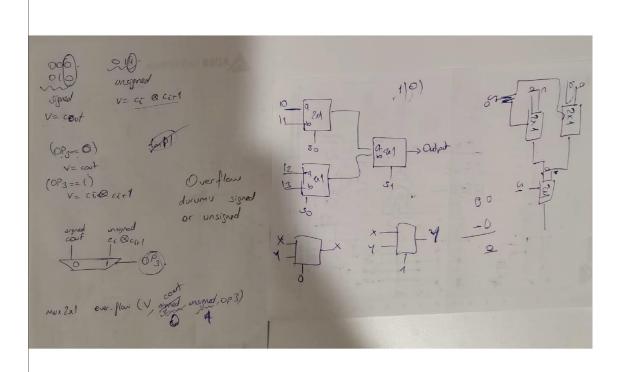
CSE 331 / Computer Organization HW3 ALU Verilog Report

Muhammed Bedir ULUCAY 1901042697

Work Notes:







Studies on how the system works in general.

In the Alu and other system details making according to the slides in class.

Part 1 is missing.

Other parts in part 2 wroking as wanted.

S -> Set less than bit if a < b then it is 1 else 0

V -> Over flow bit if an over flow occurd in add or sub it is 1 other 1

Ex: 0101 + 1011 => R = 0000 V-> 1 so result = 10000

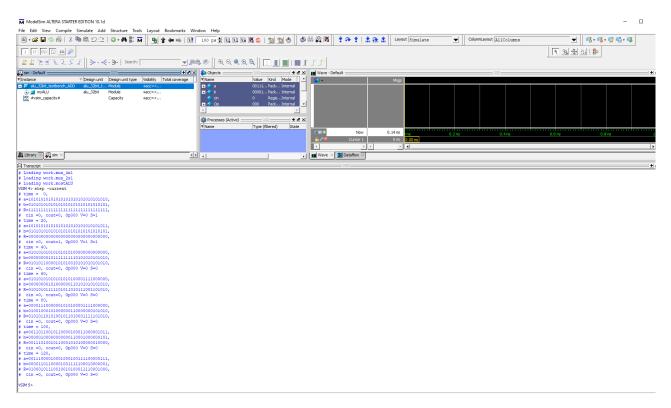
Cin is 1 sub operation

B value flip-flop in stl and sub operation for each bit.

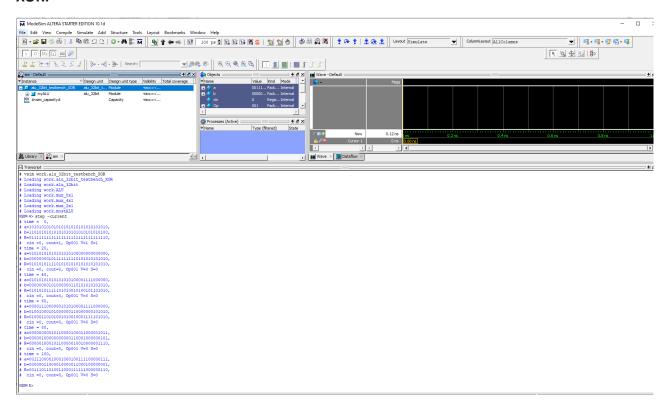
For stl operation after calculation R[0] bit rearrange the S's value after most significant bit operation

V is change using Op3, add and sub signed (V = cout), for mult (V = ci xor ci+1)

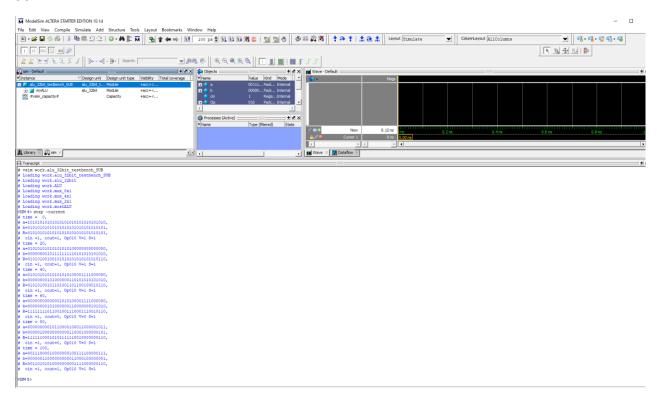
ADD:



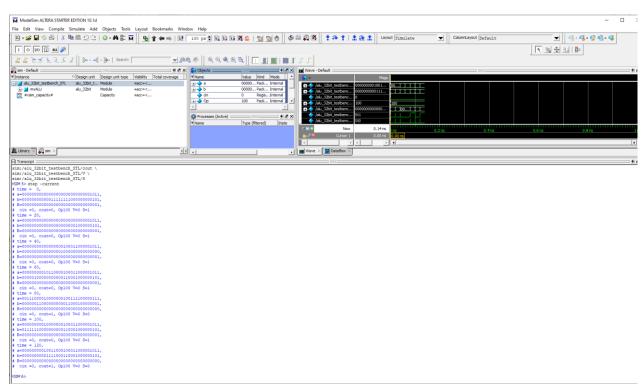
XOR:



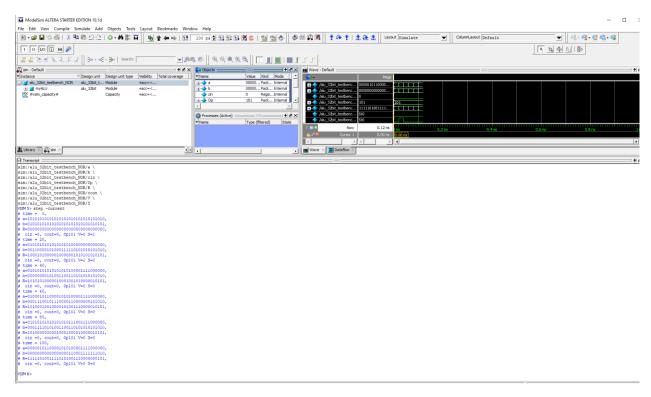
SUB:



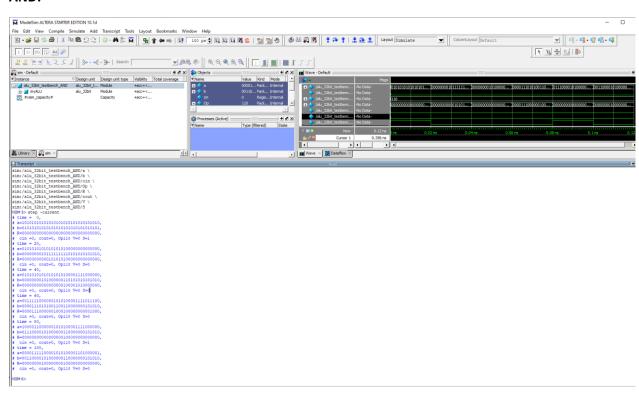
SLT:



NOR:



AND:



OR:

