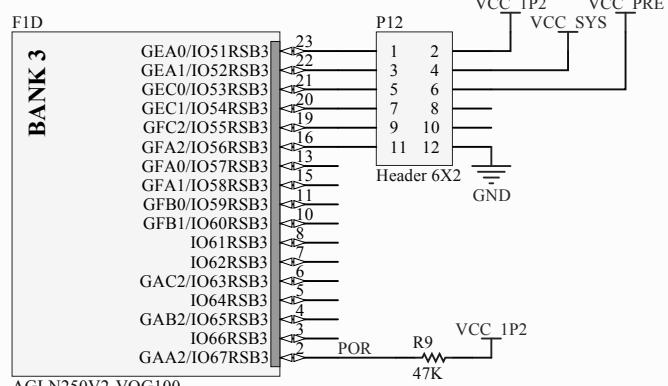
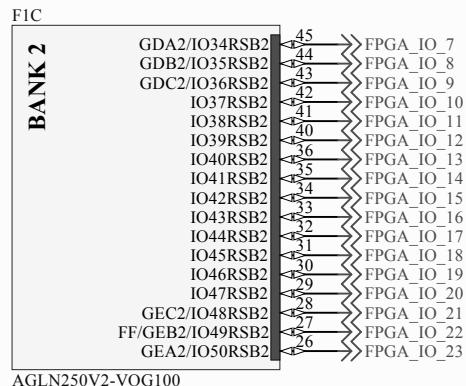
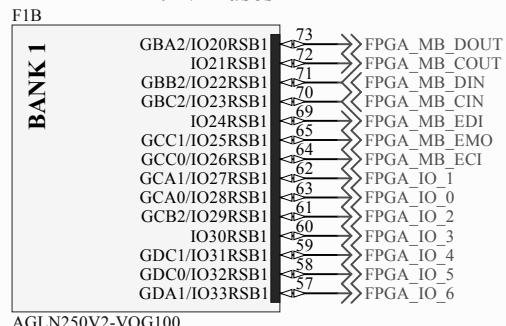
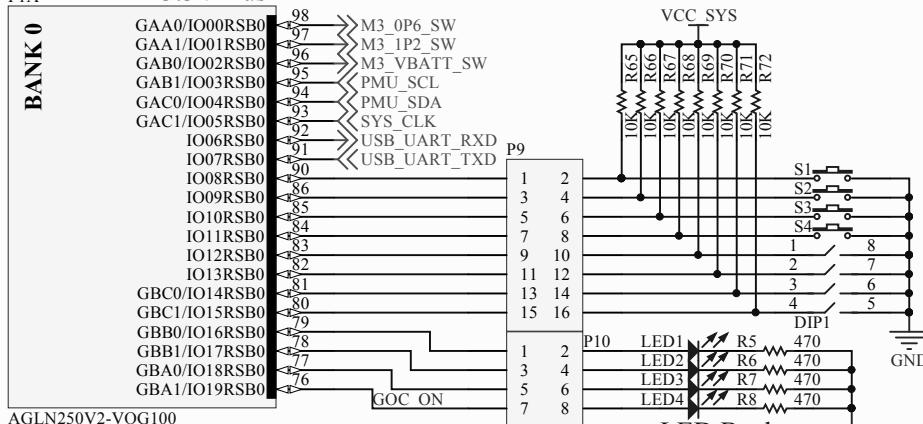


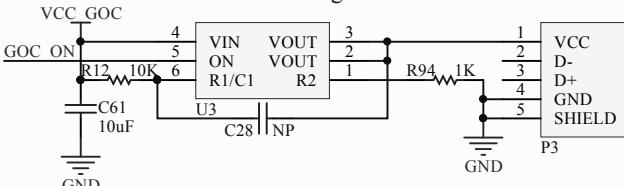
## 1.2V Buses



## 3.3V Bus



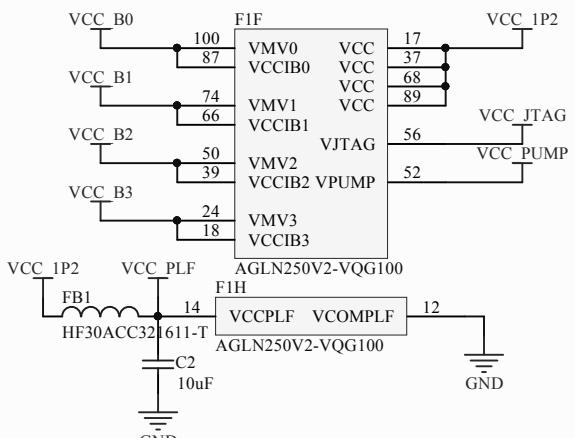
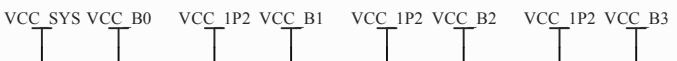
## GOC Light Switch



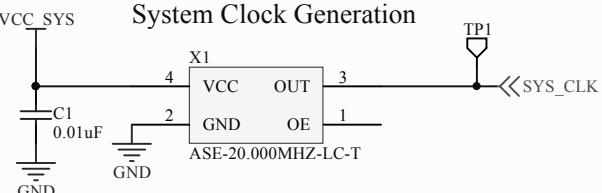
Title  
M3 ICE: FPGA I/O

Size	Number	Revision
A		
Date:	10/17/2014	Sheet of
File:	C:\Users\...\FPGA_Io.SchDoc	Drawn By:

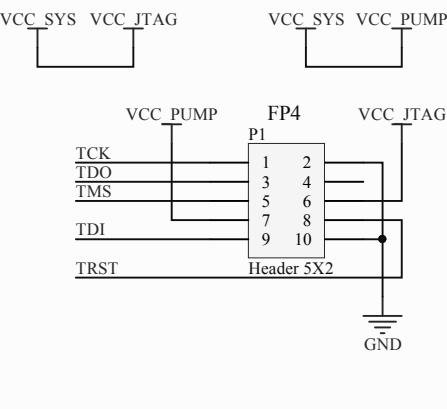
### FPGA Power



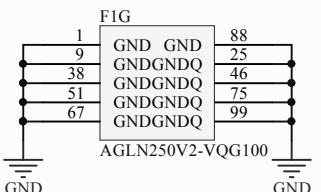
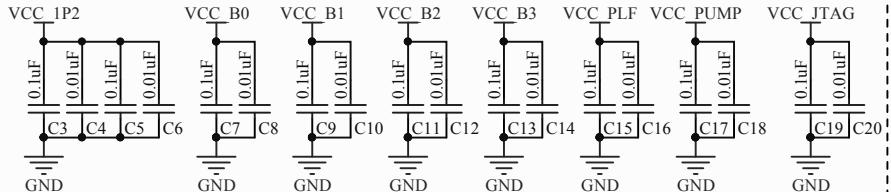
### System Clock Generation



### JTAG Connectors



### FPGA Decoupling Caps

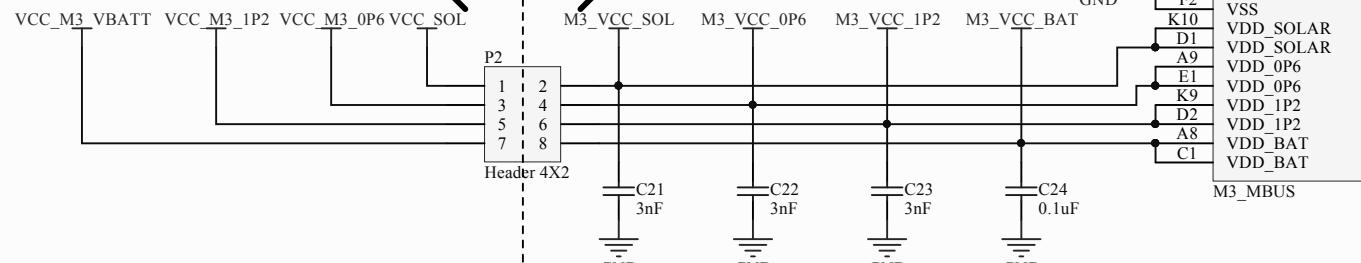


TODO: Is VCC\_JTAG supposed to be 3.3V?

Title M3 ICE: FPGA Power & Miscellaneous		
Size A	Number	Revision
Date: 10/17/2014		Sheet of
File: C:\Users...\FPGA misc.SchDoc		Drawn By:

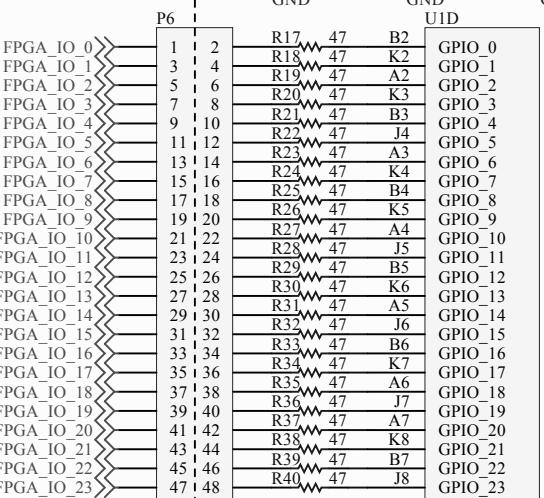
# PINT (Programming INTerface chip)

# M3 (Michigan Millimeter Mote)



## MBus Breakout

	P4
M3 VCC BAT	R77 0
M3 VCC 1P2	R78 0
M3 VCC 0P6	R79 0
GND	R80 0
ICE CIN	R81 0
ICE COUT	R82 0
ICE DIN	R83 0
ICE DOUT	R84 0
ICE EMO	R85 0
ICE ECI	R95 0
ICE EDI	R96 0
	R97 0
	12



U1C M3 MBUS

SPI\_TXD J3  
SPI\_CLKOUT K1  
SPI\_FSSOUT J2  
SPI\_RXD J1

U1B M3 MBUS

DIN E2  
DOUT F1  
CIN G1  
COUT G2

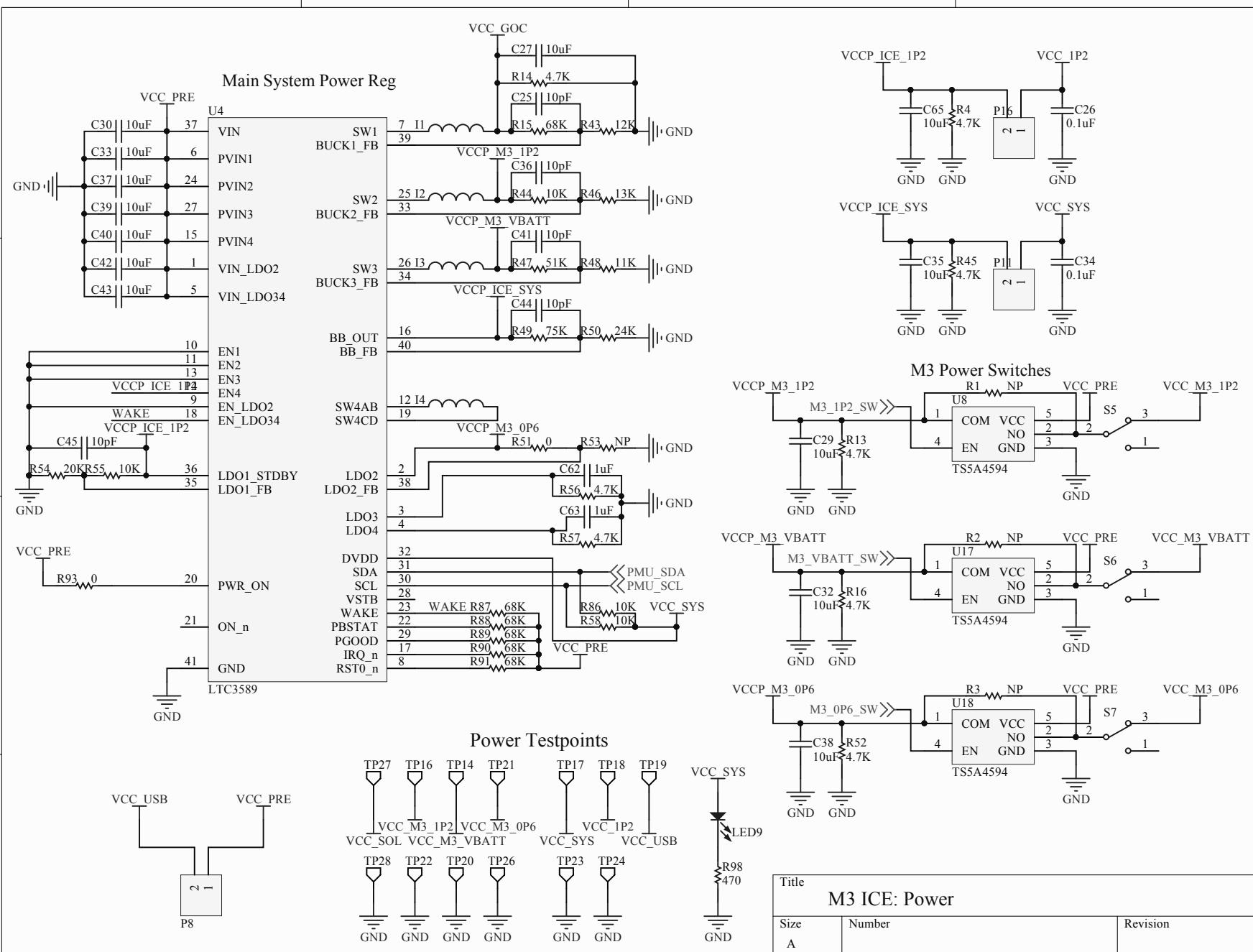
U1E M3 MBUS

EMO H1  
ECI H2  
EDI H2

M3 MBUS

## Title M3 ICE: PINT & M3 Chips

Size	Number	Revision
A		
Date:	10/17/2014	Sheet of
File:	C:\Users\...\M3_Chip.SchDoc	Drawn By:



A

A

B

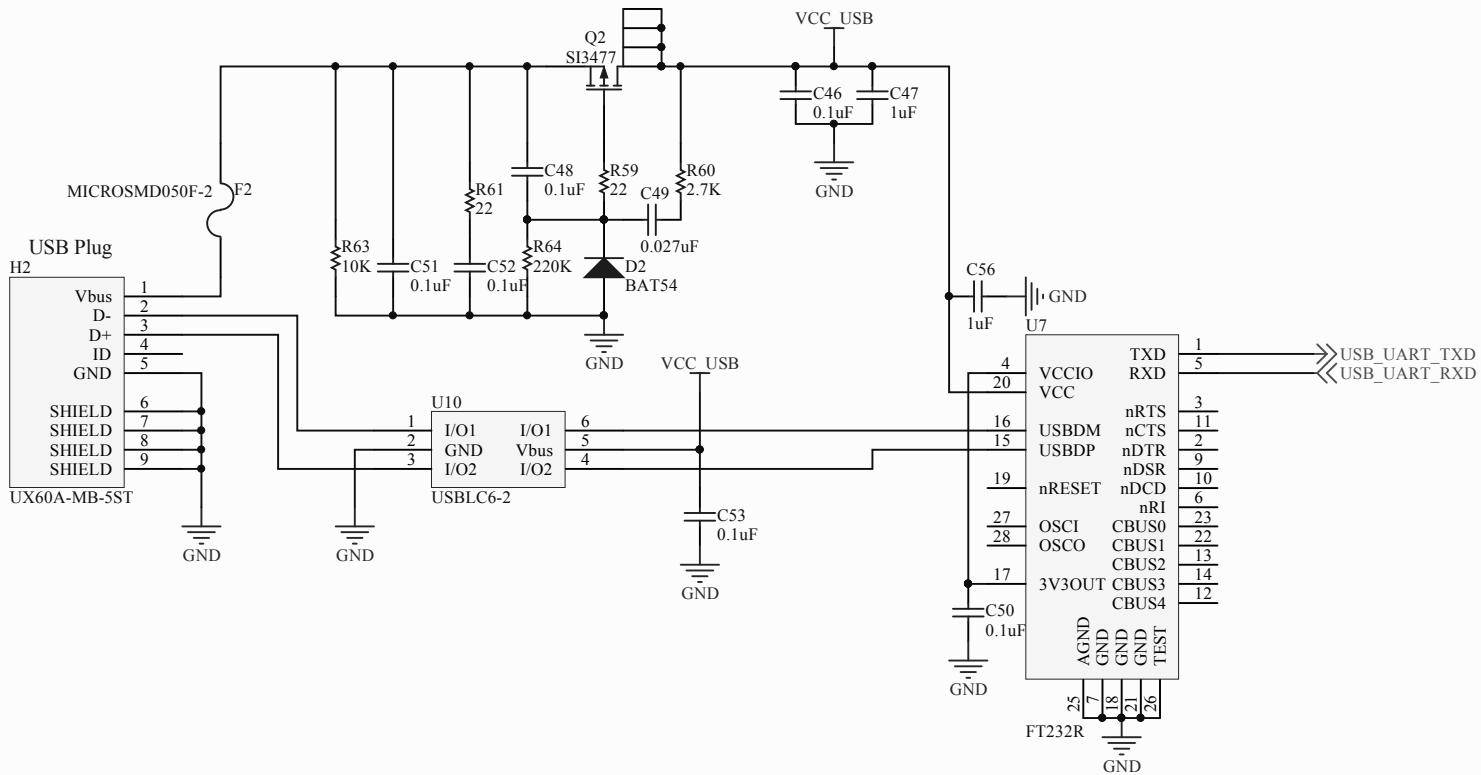
B

C

C

D

D



## Title

## M3 ICE: USB-to-UART Bridge

Size	Number	Revision
A		
Date:	10/17/2014	Sheet of
File:	C:\Users\...\USB to UART.SchDoc	Drawn By:

