University of Modena e Reggio Emilia
Department of Physics, Informatics and Mathematics

Master's degree in Computer Science

High Performance Computing

Author:
Francesco Mecatti

Academic Year 2024-2025

Table of Contents

1. Introduction

Introduction on heterogenous system, parallel programming models, hardware accelerators, etc.

1.1 Resources

Slides are generally enough + lab hands-on.

Further readings:

- An Introduction to Parallel Programming, Peter Pacheco
- CUDA reference manual

1.2 Course Overview, Prerequisites and Objectives

1.2.1 Objectives

We are going to see:

- architectural paradigms for parallel and accelerated computation such as multi-core CPU, GPU, FPGA, and NPU
- program profiling and performance evaluation, along with issues and optimization opportunities
- Intermediate OpenMP programming for Intel CPU programming
- Intermediate CUDA programming for NVIDIA GPU programming
- HLS - High Level Synthesis - for FPGA programming

1.2.2 Overview

Course units:

1. Theoretical unit about parallel and heterogenous computing architectures and common hardware models
2. Programming models for parallel architectures with hands-on labs: NVIDIA Tegra and Xilinx Zyqn architecture have been picked as platforms for lab sessions

We should rather talk about GPGPU, which stands for General Purpose GPU, since nowadays they are used improperly for tasks other than graphics rendering.

Be aware of the difference between dGPU and iGPU:

- iGPU - Integrated GPU - less powerful but data can be moved faster
- dGPU - Discrete GPU - much powerful but you pay the price of traversing a path far from the CPU

Development boards enable introspection on the system during development process: we can understand what's going on in the system.

1.2.3 Motivation

Supercomputing vs High Performance Computing. They are different: HPC moves the focus on SoC (not huge scale computers) and their heterogeneous/parallel composition. The same challenges that where thightly bound to supercomputers are now exhibited by this kind of smaller pocket systems.

Embedded Systems (ESs) are the central actors of this revolution. An escalation in this sector has been marked by the following concepts:

-

See Gordon Bell, Renesas R-CAR V3U, Hilisicon Kirin

Final objective: learn how to offload workload from main CPU to dedicated subsystems.

See big.LITTLE ARM architecture