Specification

資料中心參考文件用章
For Reference Only
2014.08.08
聯合聚晶股份有限公司
Integrated Solution Technology Inc

Written by Department	Written by / Date	Approved by QRA Manager	Issued by D.C.C.
Research & Development	Pochih Lin 08/08/2014	Bonnie Lee 08/08/2014	Bonnie Lee 08/08/2014

Controlled by DCC

Copy List

Code Name	100	200	300	400	500	600	700
Dept.	HR	S/M	MFG	R&D	CH	QRA	MIS
	--	--	--	✓	✓	✓	--

文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P001	--	New Release	E08090002	Pochih	08/05/2009
P002	Page1	Modified Feature description, take off Partial and two screen display.	E02100006	Shyang	02/06/2010
	Page16	Added RAM address mapping for Mono display			
	Page20	Added external power figure.			
	Page24	Took off the Interlace scan (INT) function.			
	Page29	Added Mono display function and Frame rate calculated formula.			
	Page33	Modified Oscillator frequency (CLS with CTN) at DC Character.			
	Page35,36	Modified 80/68/SPI AC timing.			
	Page41	Added ITO routing example figure diagram.			
P003	--	Modified" Mono up to 16G STN-LCD Driver/Controller"	E02010013	Shyang	02/11/2010
P004	Page33	Modify Oscillator frequency	E03100007	Pochih	03/05/2010
	Page33	Add Dynamic current consumption and value(TYP and Max)			
P005	Page11	Modify Vref Pin description	E04100004	Pochih	04/09/2010
	Page18	Modify VM value			
	Page 32,33	Added Power ON/OFF sequence			
	Page 35	Modify Fosc and Vref value			

接續頁 CONTINUATION --- ☒ 是 YES; ☐ 否 NO

文件變更履歷頁

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
P005	Page42	Modify ITO Resister Limitation	E04100004	Pochih	04/09/2010
	Page43	Modify ITO routing example			
P006	Page10	Modify REGON pin description	E04100006	Pochih	04/16/2010
	Page30	Add Frame Rate Table			
	Page36	Modify Static current consumption			
P007	Page34	Modify Power OFF Sequence	E06100009	Pochih	06/21/2010
001	Page16~18	Modify recommend Cap value	E07100007	Pochih	07/21/2010
		Delete “Preliminary”			
002		Change max VCC/VCI voltage to 3.6V	E01110005	Pochih	01/24/2011
		Change max VOUT1 voltage to 7.0V			
	Page16	Modify DCDC1 application figure			
	Page20	Correct External VOUT2 voltage			
	Page22	Remove R01h INT function			
	Page23	Remove INT function			
	Page24	Correct SHL function			
	Page36	Add OTP programming voltage			
	Page36	Correct Dynamic current consumption condition			
	Page36	Add VOUT1 DC spec.			
003	Page11	V0 and XV0 discharge notice	E06110008	Pochih	06/14/2011
	Page24	Add COM scan table			
	Page34	Add power off(discharge) notice			

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

Document Change History

版次 Rev.	變更項次 Change Items#	變更內容簡述 Change Description	變更依據文件號碼 ECN #	撰寫者 Writer	生效日期 Eff. Date
004	Page11	Change VDD capacitor to 10uF	E03120016	Pochih	03/19/2012
	Page19	Change VDD capacitor to 10uF			
	Page20	Change VDD capacitor to 10uf			
005	Page25	Modify SLP/STB mode description	E08130001	Sam	08/02/2013
006	Page35	Add Input voltage range (VIN)	E10130005	Pochih	10/29/2013
007	Page39	Add Note for tr,tf spec	E11130010	Pochih	11/18/2013
008	Page16,20,36	Change max VOUT1 voltage to 6.0V	E08140009	Pochih	08/08/2104

接續頁 CONTINUATION --- ☐ 是 YES; ☒ 否 NO

IST3257

256 x162 dot Graphics Mono up to 16 grayscale STN-LCD Driver/Controller

INTRODUCTION

The IST3257 is a single chip, 16-grayscale STN-LCD driver with controller for dot-matrix STN-LCD panel.

The IST3257 has 256 Segment outputs and 162 Common outputs, It can drives up to 256x162-dots STN-LCD panel.

The IST3257 provides 80/68-series 8/16-bit high-speed bus interface and 4-line Serial interface embedded bit-mapped display RAM, oscillator circuit and power circuit, so that it can minimize system's hardware effort with fewer components.

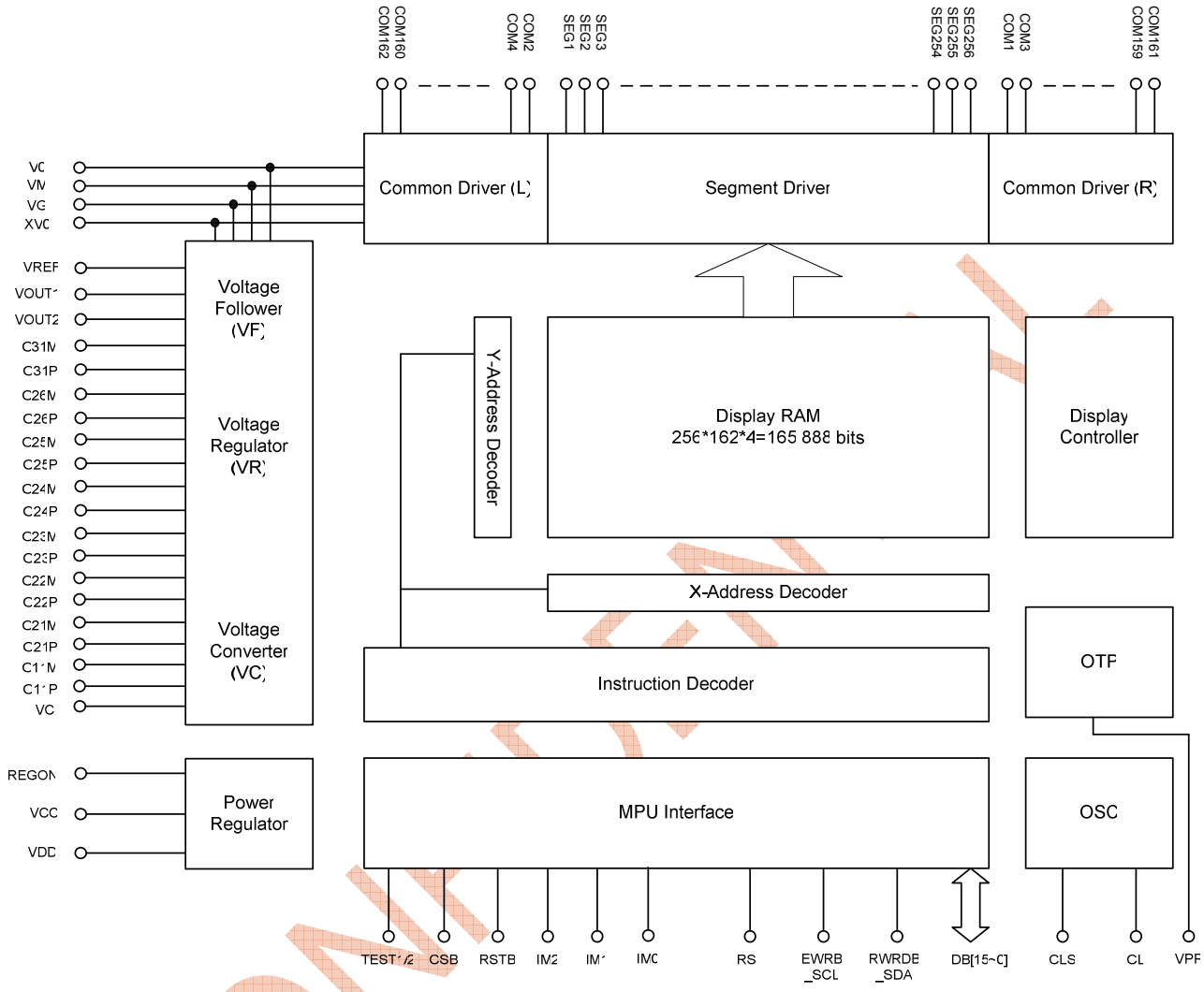
The IST3257 provides abundant commands for LCD display access, except the basic display functions.

The IST3257 is especially designed for low power consumption application. It also provides Standby and Sleep mode allows for precise power saving control.

FEATURES

- **LCD Drive Output**
  - Segment outputs : 256 outputs
  - Common outputs : 162 outputs
- **Display Function**
  - Display RAM size : 256*162*4 Bits
  - Gray scale level : 16 level
  - Duty ratios : 1/64, 1/128, 1/162
- **Power Circuit**
  - Logic power : 2.4V ~ 3.6V
  - LCD drive voltage : 30V (max V0 - XV0)
  - Boost circuit (step1) : x2 for VG
    (step2) : x2 ~ x7 for V0
    (step3) : for XV0
  - Temp. coefficient : 0.00%/℃, -0.05%/℃, -010%/℃,-015%/℃
  - Contrast adjust : 128 steps
  - Bias ratio : 1/6 ~ 1/13
- **Microprocessor Interface**
  - Parallel 68/80-series bi-directional 8/16 bit interface
  - 4-line serial interface
  - Min. Write cycle : 350 ns
  - Min. Read cycle : 500 ns
- **Chip Outline**
  - Package : COG
  - Pad pitch (min) : 26um.
  - Pad spacing (min) : 12um.
- **Oscillator Circuit**
  - On-chip RC oscillation circuit
- **LCD Drive Circuit**
  - Left-Right-interlaced COM disposition
  - Support vertical scroll display
- **Command Set**
  - Display data write/read
  - Addressing window auto-increment
  - Set display starting line
  - Set polarity alternated cycles
  - COM shift direction
  - SEG shift direction
  - Frame rate adjustment
  - Reverse display
  - Power saving mode
  - Internal register status read
- **Other**
  - OTP available (Contrast adjustable)

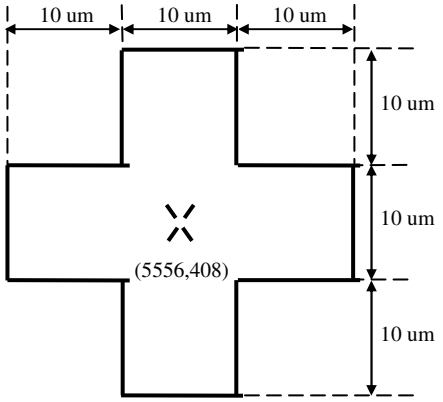
BLOCK DIAGRAM

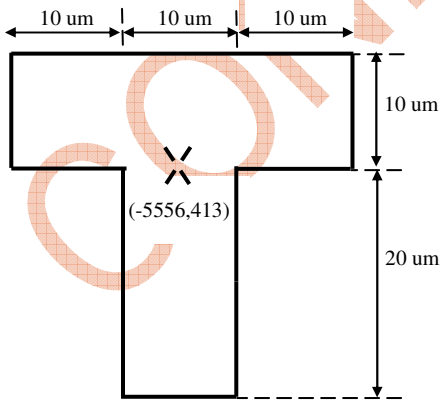


PAD ARRANGEMENT

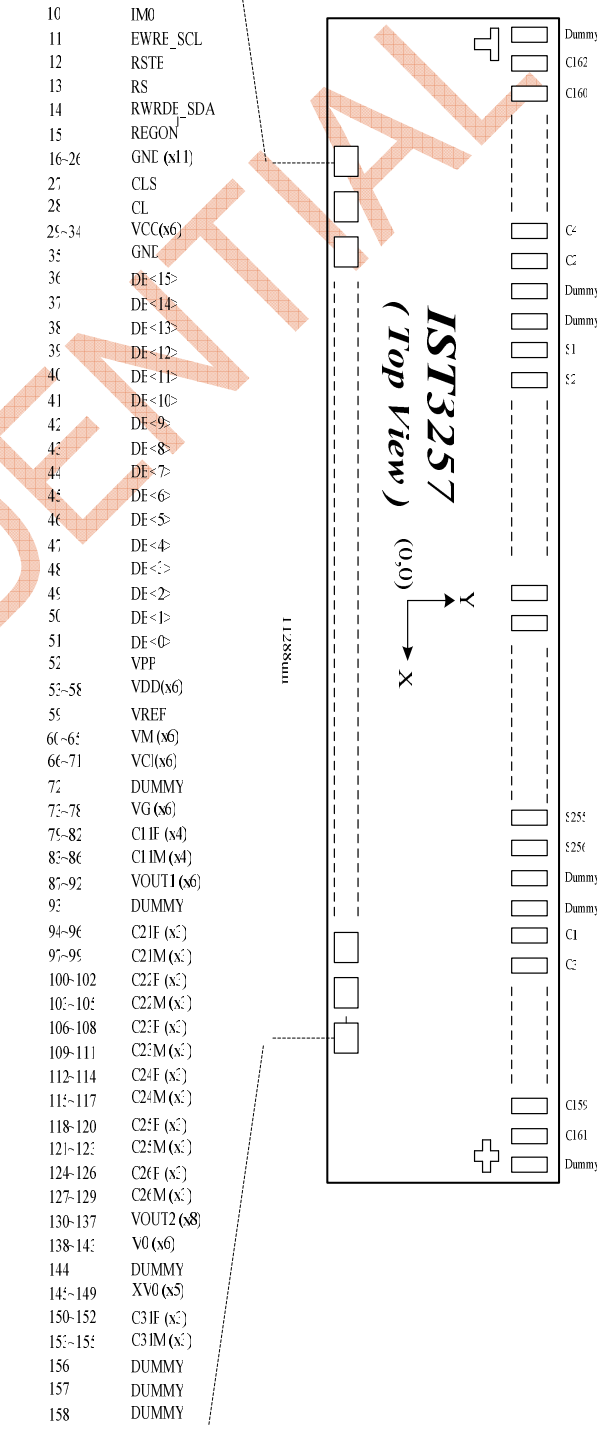
Chip Size	11288 (X) * 925.5 (Y) um^2
Chip Thickness	400 um
Pad Coordinate	Pad Centers
Coordinate origin	Chip center
Bump High	15 um
Au Bump Size (X*Y) um^2	
(1) 50 * 80 um^2	Pad 1 ~ 158
(2) 14 * 145 um^2	Pad 159 ~ 582

Alignment Mark





PIN NO	PIN NAME
1	DUMMY
2	DUMMY
3	DUMMY
4	TEST2
5	TEST1
6	GND
7	CSB
8	IM2
9	IM1
10	IM0
11	EWRE_SCL
12	RSTE
13	RS
14	RWRDE_SDA
15	REGON
16~26	GND (x11)
27	CLS
28	CL
29~34	VCC(x6)
35	GND
36	DE<15>
37	DE<14>
38	DE<13>
39	DE<12>
40	DE<11>
41	DE<10>
42	DE<9>
43	DE<8>
44	DE<7>
45	DE<6>
46	DE<5>
47	DE<4>
48	DE<3>
49	DE<2>
50	DE<1>
51	DE<0>
52	VPP
53~58	VDD(x6)
59	VREF
60~65	VM (x6)
66~71	VCI(x6)
72	DUMMY
73~78	VG (x6)
79~82	C1IF (x4)
83~86	C1IM (x4)
87~92	VOUT1 (x6)
93	DUMMY
94~96	C2IF (x3)
97~99	C2IM (x3)
100~102	C22F (x3)
103~105	C22M (x3)
106~108	C23F (x3)
109~111	C23M (x3)
112~114	C24F (x3)
115~117	C24M (x3)
118~120	C25F (x3)
121~123	C25M (x3)
124~126	C26F (x3)
127~129	C26M (x3)
130~137	VOUT2 (x8)
138~143	V0 (x6)
144	DUMMY
145~149	XV0 (x5)
150~152	C3IF (x3)
153~155	C3IM (x3)
156	DUMMY
157	DUMMY
158	DUMMY



PAD COORDINATE

No	Name	X	Y	No	Name	X	Y
1	DUMMY	-5495	-357	51	DB<0>	-1995	-357
2	DUMMY	-5425	-357	52	VPP	-1925	-357
3	DUMMY	-5355	-357	53	VDD	-1855	-357
4	TEST2	-5285	-357	54	VDD	-1785	-357
5	TEST1	-5215	-357	55	VDD	-1715	-357
6	GND	-5145	-357	56	VDD	-1645	-357
7	CSB	-5075	-357	57	VDD	-1575	-357
8	IM2	-5005	-357	58	VDD	-1505	-357
9	IM1	-4935	-357	59	VREF	-1435	-357
10	IM0	-4865	-357	60	VM	-1365	-357
11	EWRB_SCL	-4795	-357	61	VM	-1295	-357
12	RSTB	-4725	-357	62	VM	-1225	-357
13	RS	-4655	-357	63	VM	-1155	-357
14	RWRDB_SDA	-4585	-357	64	VM	-1085	-357
15	REGON	-4515	-357	65	VM	-1015	-357
16	GND	-4445	-357	66	VCI	-945	-357
17	GND	-4375	-357	67	VCI	-875	-357
18	GND	-4305	-357	68	VCI	-805	-357
19	GND	-4235	-357	69	VCI	-735	-357
20	GND	-4165	-357	70	VCI	-665	-357
21	GND	-4095	-357	71	VCI	-595	-357
22	GND	-4025	-357	72	DUMMY	-525	-357
23	GND	-3955	-357	73	VG	-455	-357
24	GND	-3885	-357	74	VG	-385	-357
25	GND	-3815	-357	75	VG	-315	-357
26	GND	-3745	-357	76	VG	-245	-357
27	CLS	-3675	-357	77	VG	-175	-357
28	CL	-3605	-357	78	VG	-105	-357
29	VCC	-3535	-357	79	C11P	-35	-357
30	VCC	-3465	-357	80	C11P	35	-357
31	VCC	-3395	-357	81	C11P	105	-357
32	VCC	-3325	-357	82	C11P	175	-357
33	VCC	-3255	-357	83	C11M	245	-357
34	VCC	-3185	-357	84	C11M	315	-357
35	GND	-3115	-357	85	C11M	385	-357
36	DB<15>	-3045	-357	86	C11M	455	-357
37	DB<14>	-2975	-357	87	VOUT1	525	-357
38	DB<13>	-2905	-357	88	VOUT1	595	-357
39	DB<12>	-2835	-357	89	VOUT1	665	-357
40	DB<11>	-2765	-357	90	VOUT1	735	-357
41	DB<10>	-2695	-357	91	VOUT1	805	-357
42	DB<9>	-2625	-357	92	VOUT1	875	-357
43	DB<8>	-2555	-357	93	DUMMY	945	-357
44	DB<7>	-2485	-357	94	C21P	1015	-357
45	DB<6>	-2415	-357	95	C21P	1085	-357
46	DB<5>	-2345	-357	96	C21P	1155	-357
47	DB<4>	-2275	-357	97	C21M	1225	-357
48	DB<3>	-2205	-357	98	C21M	1295	-357
49	DB<2>	-2135	-357	99	C21M	1365	-357
50	DB<1>	-2065	-357	100	C22P	1435	-357

No	Name	X	Y	No	Name	X	Y
101	C22P	1505	-357	151	C31P	5005	-357
102	C22P	1575	-357	152	C31P	5075	-357
103	C22M	1645	-357	153	C31M	5145	-357
104	C22M	1715	-357	154	C31M	5215	-357
105	C22M	1785	-357	155	C31M	5285	-357
106	C23P	1855	-357	156	DUMMY	5355	-357
107	C23P	1925	-357	157	DUMMY	5425	-357
108	C23P	1995	-357	158	DUMMY	5495	-357
109	C23M	2065	-357	159	DUMMY	5499	325.5
110	C23M	2135	-357	160	COM<161>	5473	325.5
111	C23M	2205	-357	161	COM<159>	5447	325.5
112	C24P	2275	-357	162	COM<157>	5421	325.5
113	C24P	2345	-357	163	COM<155>	5395	325.5
114	C24P	2415	-357	164	COM<153>	5369	325.5
115	C24M	2485	-357	165	COM<151>	5343	325.5
116	C24M	2555	-357	166	COM<149>	5317	325.5
117	C24M	2625	-357	167	COM<147>	5291	325.5
118	C25P	2695	-357	168	COM<145>	5265	325.5
119	C25P	2765	-357	169	COM<143>	5239	325.5
120	C25P	2835	-357	170	COM<141>	5213	325.5
121	C25M	2905	-357	171	COM<139>	5187	325.5
122	C25M	2975	-357	172	COM<137>	5161	325.5
123	C25M	3045	-357	173	COM<135>	5135	325.5
124	C26P	3115	-357	174	COM<133>	5109	325.5
125	C26P	3185	-357	175	COM<131>	5083	325.5
126	C26P	3255	-357	176	COM<129>	5057	325.5
127	C26M	3325	-357	177	COM<127>	5031	325.5
128	C26M	3395	-357	178	COM<125>	5005	325.5
129	C26M	3465	-357	179	COM<123>	4979	325.5
130	VOUT2	3535	-357	180	COM<121>	4953	325.5
131	VOUT2	3605	-357	181	COM<119>	4927	325.5
132	VOUT2	3675	-357	182	COM<117>	4901	325.5
133	VOUT2	3745	-357	183	COM<115>	4875	325.5
134	VOUT2	3815	-357	184	COM<113>	4849	325.5
135	VOUT2	3885	-357	185	COM<111>	4823	325.5
136	VOUT2	3955	-357	186	COM<109>	4797	325.5
137	VOUT2	4025	-357	187	COM<107>	4771	325.5
138	V0	4095	-357	188	COM<105>	4745	325.5
139	V0	4165	-357	189	COM<103>	4719	325.5
140	V0	4235	-357	190	COM<101>	4693	325.5
141	V0	4305	-357	191	COM<99>	4667	325.5
142	V0	4375	-357	192	COM<97>	4641	325.5
143	V0	4445	-357	193	COM<95>	4615	325.5
144	DUMMY	4515	-357	194	COM<93>	4589	325.5
145	XV0	4585	-357	195	COM<91>	4563	325.5
146	XV0	4655	-357	196	COM<89>	4537	325.5
147	XV0	4725	-357	197	COM<87>	4511	325.5
148	XV0	4795	-357	198	COM<85>	4485	325.5
149	XV0	4865	-357	199	COM<83>	4459	325.5
150	C31P	4935	-357	200	COM<81>	4433	325.5

No	Name	X	Y	No	Name	X	Y
201	COM<79>	4407	325.5	251	SEG<248>	3107	325.5
202	COM<77>	4381	325.5	252	SEG<247>	3081	325.5
203	COM<75>	4355	325.5	253	SEG<246>	3055	325.5
204	COM<73>	4329	325.5	254	SEG<245>	3029	325.5
205	COM<71>	4303	325.5	255	SEG<244>	3003	325.5
206	COM<69>	4277	325.5	256	SEG<243>	2977	325.5
207	COM<67>	4251	325.5	257	SEG<242>	2951	325.5
208	COM<65>	4225	325.5	258	SEG<241>	2925	325.5
209	COM<63>	4199	325.5	259	SEG<240>	2899	325.5
210	COM<61>	4173	325.5	260	SEG<239>	2873	325.5
211	COM<59>	4147	325.5	261	SEG<238>	2847	325.5
212	COM<57>	4121	325.5	262	SEG<237>	2821	325.5
213	COM<55>	4095	325.5	263	SEG<236>	2795	325.5
214	COM<53>	4069	325.5	264	SEG<235>	2769	325.5
215	COM<51>	4043	325.5	265	SEG<234>	2743	325.5
216	COM<49>	4017	325.5	266	SEG<233>	2717	325.5
217	COM<47>	3991	325.5	267	SEG<232>	2691	325.5
218	COM<45>	3965	325.5	268	SEG<231>	2665	325.5
219	COM<43>	3939	325.5	269	SEG<230>	2639	325.5
220	COM<41>	3913	325.5	270	SEG<229>	2613	325.5
221	COM<39>	3887	325.5	271	SEG<228>	2587	325.5
222	COM<37>	3861	325.5	272	SEG<227>	2561	325.5
223	COM<35>	3835	325.5	273	SEG<226>	2535	325.5
224	COM<33>	3809	325.5	274	SEG<225>	2509	325.5
225	COM<31>	3783	325.5	275	SEG<224>	2483	325.5
226	COM<29>	3757	325.5	276	SEG<223>	2457	325.5
227	COM<27>	3731	325.5	277	SEG<222>	2431	325.5
228	COM<25>	3705	325.5	278	SEG<221>	2405	325.5
229	COM<23>	3679	325.5	279	SEG<220>	2379	325.5
230	COM<21>	3653	325.5	280	SEG<219>	2353	325.5
231	COM<19>	3627	325.5	281	SEG<218>	2327	325.5
232	COM<17>	3601	325.5	282	SEG<217>	2301	325.5
233	COM<15>	3575	325.5	283	SEG<216>	2275	325.5
234	COM<13>	3549	325.5	284	SEG<215>	2249	325.5
235	COM<11>	3523	325.5	285	SEG<214>	2223	325.5
236	COM<9>	3497	325.5	286	SEG<213>	2197	325.5
237	COM<7>	3471	325.5	287	SEG<212>	2171	325.5
238	COM<5>	3445	325.5	288	SEG<211>	2145	325.5
239	COM<3>	3419	325.5	289	SEG<210>	2119	325.5
240	COM<1>	3393	325.5	290	SEG<209>	2093	325.5
241	DUMMY	3367	325.5	291	SEG<208>	2067	325.5
242	DUMMY	3341	325.5	292	SEG<207>	2041	325.5
243	SEG<256>	3315	325.5	293	SEG<206>	2015	325.5
244	SEG<255>	3289	325.5	294	SEG<205>	1989	325.5
245	SEG<254>	3263	325.5	295	SEG<204>	1963	325.5
246	SEG<253>	3237	325.5	296	SEG<203>	1937	325.5
247	SEG<252>	3211	325.5	297	SEG<202>	1911	325.5
248	SEG<251>	3185	325.5	298	SEG<201>	1885	325.5
249	SEG<250>	3159	325.5	299	SEG<200>	1859	325.5
250	SEG<249>	3133	325.5	300	SEG<199>	1833	325.5

No	Name	X	Y	No	Name	X	Y
301	SEG<198>	1807	325.5	351	SEG<148>	507	325.5
302	SEG<197>	1781	325.5	352	SEG<147>	481	325.5
303	SEG<196>	1755	325.5	353	SEG<146>	455	325.5
304	SEG<195>	1729	325.5	354	SEG<145>	429	325.5
305	SEG<194>	1703	325.5	355	SEG<144>	403	325.5
306	SEG<193>	1677	325.5	356	SEG<143>	377	325.5
307	SEG<192>	1651	325.5	357	SEG<142>	351	325.5
308	SEG<191>	1625	325.5	358	SEG<141>	325	325.5
309	SEG<190>	1599	325.5	359	SEG<140>	299	325.5
310	SEG<189>	1573	325.5	360	SEG<139>	273	325.5
311	SEG<188>	1547	325.5	361	SEG<138>	247	325.5
312	SEG<187>	1521	325.5	362	SEG<137>	221	325.5
313	SEG<186>	1495	325.5	363	SEG<136>	195	325.5
314	SEG<185>	1469	325.5	364	SEG<135>	169	325.5
315	SEG<184>	1443	325.5	365	SEG<134>	143	325.5
316	SEG<183>	1417	325.5	366	SEG<133>	117	325.5
317	SEG<182>	1391	325.5	367	SEG<132>	91	325.5
318	SEG<181>	1365	325.5	368	SEG<131>	65	325.5
319	SEG<180>	1339	325.5	369	SEG<130>	39	325.5
320	SEG<179>	1313	325.5	370	SEG<129>	13	325.5
321	SEG<178>	1287	325.5	371	SEG<128>	-13	325.5
322	SEG<177>	1261	325.5	372	SEG<127>	-39	325.5
323	SEG<176>	1235	325.5	373	SEG<126>	-65	325.5
324	SEG<175>	1209	325.5	374	SEG<125>	-91	325.5
325	SEG<174>	1183	325.5	375	SEG<124>	-117	325.5
326	SEG<173>	1157	325.5	376	SEG<123>	-143	325.5
327	SEG<172>	1131	325.5	377	SEG<122>	-169	325.5
328	SEG<171>	1105	325.5	378	SEG<121>	-195	325.5
329	SEG<170>	1079	325.5	379	SEG<120>	-221	325.5
330	SEG<169>	1053	325.5	380	SEG<119>	-247	325.5
331	SEG<168>	1027	325.5	381	SEG<118>	-273	325.5
332	SEG<167>	1001	325.5	382	SEG<117>	-299	325.5
333	SEG<166>	975	325.5	383	SEG<116>	-325	325.5
334	SEG<165>	949	325.5	384	SEG<115>	-351	325.5
335	SEG<164>	923	325.5	385	SEG<114>	-377	325.5
336	SEG<163>	897	325.5	386	SEG<113>	-403	325.5
337	SEG<162>	871	325.5	387	SEG<112>	-429	325.5
338	SEG<161>	845	325.5	388	SEG<111>	-455	325.5
339	SEG<160>	819	325.5	389	SEG<110>	-481	325.5
340	SEG<159>	793	325.5	390	SEG<109>	-507	325.5
341	SEG<158>	767	325.5	391	SEG<108>	-533	325.5
342	SEG<157>	741	325.5	392	SEG<107>	-559	325.5
343	SEG<156>	715	325.5	393	SEG<106>	-585	325.5
344	SEG<155>	689	325.5	394	SEG<105>	-611	325.5
345	SEG<154>	663	325.5	395	SEG<104>	-637	325.5
346	SEG<153>	637	325.5	396	SEG<103>	-663	325.5
347	SEG<152>	611	325.5	397	SEG<102>	-689	325.5
348	SEG<151>	585	325.5	398	SEG<101>	-715	325.5
349	SEG<150>	559	325.5	399	SEG<100>	-741	325.5
350	SEG<149>	533	325.5	400	SEG<99>	-767	325.5

No	Name	X	Y	No	Name	X	Y
401	SEG<98>	-793	325.5	451	SEG<48>	-2093	325.5
402	SEG<97>	-819	325.5	452	SEG<47>	-2119	325.5
403	SEG<96>	-845	325.5	453	SEG<46>	-2145	325.5
404	SEG<95>	-871	325.5	454	SEG<45>	-2171	325.5
405	SEG<94>	-897	325.5	455	SEG<44>	-2197	325.5
406	SEG<93>	-923	325.5	456	SEG<43>	-2223	325.5
407	SEG<92>	-949	325.5	457	SEG<42>	-2249	325.5
408	SEG<91>	-975	325.5	458	SEG<41>	-2275	325.5
409	SEG<90>	-1001	325.5	459	SEG<40>	-2301	325.5
410	SEG<89>	-1027	325.5	460	SEG<39>	-2327	325.5
411	SEG<88>	-1053	325.5	461	SEG<38>	-2353	325.5
412	SEG<87>	-1079	325.5	462	SEG<37>	-2379	325.5
413	SEG<86>	-1105	325.5	463	SEG<36>	-2405	325.5
414	SEG<85>	-1131	325.5	464	SEG<35>	-2431	325.5
415	SEG<84>	-1157	325.5	465	SEG<34>	-2457	325.5
416	SEG<83>	-1183	325.5	466	SEG<33>	-2483	325.5
417	SEG<82>	-1209	325.5	467	SEG<32>	-2509	325.5
418	SEG<81>	-1235	325.5	468	SEG<31>	-2535	325.5
419	SEG<80>	-1261	325.5	469	SEG<30>	-2561	325.5
420	SEG<79>	-1287	325.5	470	SEG<29>	-2587	325.5
421	SEG<78>	-1313	325.5	471	SEG<28>	-2613	325.5
422	SEG<77>	-1339	325.5	472	SEG<27>	-2639	325.5
423	SEG<76>	-1365	325.5	473	SEG<26>	-2665	325.5
424	SEG<75>	-1391	325.5	474	SEG<25>	-2691	325.5
425	SEG<74>	-1417	325.5	475	SEG<24>	-2717	325.5
426	SEG<73>	-1443	325.5	476	SEG<23>	-2743	325.5
427	SEG<72>	-1469	325.5	477	SEG<22>	-2769	325.5
428	SEG<71>	-1495	325.5	478	SEG<21>	-2795	325.5
429	SEG<70>	-1521	325.5	479	SEG<20>	-2821	325.5
430	SEG<69>	-1547	325.5	480	SEG<19>	-2847	325.5
431	SEG<68>	-1573	325.5	481	SEG<18>	-2873	325.5
432	SEG<67>	-1599	325.5	482	SEG<17>	-2899	325.5
433	SEG<66>	-1625	325.5	483	SEG<16>	-2925	325.5
434	SEG<65>	-1651	325.5	484	SEG<15>	-2951	325.5
435	SEG<64>	-1677	325.5	485	SEG<14>	-2977	325.5
436	SEG<63>	-1703	325.5	486	SEG<13>	-3003	325.5
437	SEG<62>	-1729	325.5	487	SEG<12>	-3029	325.5
438	SEG<61>	-1755	325.5	488	SEG<11>	-3055	325.5
439	SEG<60>	-1781	325.5	489	SEG<10>	-3081	325.5
440	SEG<59>	-1807	325.5	490	SEG<9>	-3107	325.5
441	SEG<58>	-1833	325.5	491	SEG<8>	-3133	325.5
442	SEG<57>	-1859	325.5	492	SEG<7>	-3159	325.5
443	SEG<56>	-1885	325.5	493	SEG<6>	-3185	325.5
444	SEG<55>	-1911	325.5	494	SEG<5>	-3211	325.5
445	SEG<54>	-1937	325.5	495	SEG<4>	-3237	325.5
446	SEG<53>	-1963	325.5	496	SEG<3>	-3263	325.5
447	SEG<52>	-1989	325.5	497	SEG<2>	-3289	325.5
448	SEG<51>	-2015	325.5	498	SEG<1>	-3315	325.5
449	SEG<50>	-2041	325.5	499	DUMMY	-3341	325.5
450	SEG<49>	-2067	325.5	500	DUMMY	-3367	325.5

No	Name	X	Y	No	Name	X	Y
501	COM<2>	-3393	325.5	551	COM<102>	-4693	325.5
502	COM<4>	-3419	325.5	552	COM<104>	-4719	325.5
503	COM<6>	-3445	325.5	553	COM<106>	-4745	325.5
504	COM<8>	-3471	325.5	554	COM<108>	-4771	325.5
505	COM<10>	-3497	325.5	555	COM<110>	-4797	325.5
506	COM<12>	-3523	325.5	556	COM<112>	-4823	325.5
507	COM<14>	-3549	325.5	557	COM<114>	-4849	325.5
508	COM<16>	-3575	325.5	558	COM<116>	-4875	325.5
509	COM<18>	-3601	325.5	559	COM<118>	-4901	325.5
510	COM<20>	-3627	325.5	560	COM<120>	-4927	325.5
511	COM<22>	-3653	325.5	561	COM<122>	-4953	325.5
512	COM<24>	-3679	325.5	562	COM<124>	-4979	325.5
513	COM<26>	-3705	325.5	563	COM<126>	-5005	325.5
514	COM<28>	-3731	325.5	564	COM<128>	-5031	325.5
515	COM<30>	-3757	325.5	565	COM<130>	-5057	325.5
516	COM<32>	-3783	325.5	566	COM<132>	-5083	325.5
517	COM<34>	-3809	325.5	567	COM<134>	-5109	325.5
518	COM<36>	-3835	325.5	568	COM<136>	-5135	325.5
519	COM<38>	-3861	325.5	569	COM<138>	-5161	325.5
520	COM<40>	-3887	325.5	570	COM<140>	-5187	325.5
521	COM<42>	-3913	325.5	571	COM<142>	-5213	325.5
522	COM<44>	-3939	325.5	572	COM<144>	-5239	325.5
523	COM<46>	-3965	325.5	573	COM<146>	-5265	325.5
524	COM<48>	-3991	325.5	574	COM<148>	-5291	325.5
525	COM<50>	-4017	325.5	575	COM<150>	-5317	325.5
526	COM<52>	-4043	325.5	576	COM<152>	-5343	325.5
527	COM<54>	-4069	325.5	577	COM<154>	-5369	325.5
528	COM<56>	-4095	325.5	578	COM<156>	-5395	325.5
529	COM<58>	-4121	325.5	579	COM<158>	-5421	325.5
530	COM<60>	-4147	325.5	580	COM<160>	-5447	325.5
531	COM<62>	-4173	325.5	581	COM<162>	-5473	325.5
532	COM<64>	-4199	325.5	582	DUMMY	-5499	325.5
533	COM<66>	-4225	325.5				
534	COM<68>	-4251	325.5				
535	COM<70>	-4277	325.5				
536	COM<72>	-4303	325.5				
537	COM<74>	-4329	325.5				
538	COM<76>	-4355	325.5				
539	COM<78>	-4381	325.5				
540	COM<80>	-4407	325.5				
541	COM<82>	-4433	325.5				
542	COM<84>	-4459	325.5				
543	COM<86>	-4485	325.5				
544	COM<88>	-4511	325.5				
545	COM<90>	-4537	325.5				
546	COM<92>	-4563	325.5				
547	COM<94>	-4589	325.5				
548	COM<96>	-4615	325.5				
549	COM<98>	-4641	325.5				
550	COM<100>	-4667	325.5				

PIN DESCRIPTION

Signals	I/O	Connected to	Functions
IM2,IM1,IM0	I	GND or VCC	Selects the MPU interface mode IM2 IM1 IM0 MPU interface mode GND GND GND 68-system 16-bit bus interface GND GND VCC 68-system 8-bit bus interface GND VCC GND 80-system 16-bit bus interface GND VCC VCC 80-system 8-bit bus interface VCC GND GND 4-line serial interface
CSB	I	MPU	Chip select; Low: chip enabled High: Chip disabled Must be fixed at VCC level when chip is not active.
RS	I	MPU	Register select Low: Index/status select High: Command select
EWRB_SCL	I	MPU	For 68-system bus interface, serves as an enable signal to activate data read/write operation. For 80-system bus interface, serves as a write strobe signal and writes data at the low level. For 4-line serial interface, serves as a synchronized clock signal
RWRDB_SDA	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level For 4-line serial interface, serves as the serial data pin for data transformation.
DB0–DB15	I/O	MPU	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8, fix unused DB7 ~ DB0 to the VCC or GND level. When in serial interface, fix unused DB15-DB0 to the VCC or GND level
RSTB	I	MPU or external RC circuit	Reset pin, Low active. The chip must be reset after power-on. ****A minimal 10ms wait period should be given after finish RESET action when send first command.**
CLS	I	GND or VCC	Build-in oscillator clock or external clock input select pin Low: External clock input with CL pin High: Build-in oscillator clock
CL	I	OPEN or external clock source	Display clock input pin.
REGON	I	VCC	Internal regulator for digital core power, keep connect to VCC.
TEST1,TEST2	I	OPEN	Test pin, keeps open.

Signals	I/O	Connected to	Functions
COM1 ~ COM162	O	LCD	Output signals for common drive. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The CMS bit will decide the shift direction of the COM outputs. CMS = 0, the shift direction is COM1 → COM162. CMS = 1, the shift direction is COM162 → COM1
SEG1 ~ SEG256	O	LCD	Output signals for segment driver. In the display-off period (D = 0), sleep mode (SLP = 1), or standby mode (STB = 1), all pins output GND level. The SGS bit will decide the image mapping of the SEG outputs. SGS = 0, the image mapping is normal SGS = 1, the image mapping is mirrored.
VCC	I	Power source	Power supply
VDD	I/O	Power source	Digital core power pad Connect them with the 10uF capacitor
GND	I	Ground	Ground
VCI	I	Power source	VCI is the reference voltage source of internal Booster circuit. When the internal Booster circuit is not used, must keep this pin open.
VREF	O	Open	For Testing. Please just keeps this pin open.
VOUT1, VOUT2	O	Capacitor to GND	VOUT1/2 is the internal booster output, step-up voltage based on the difference voltage of VCI & GND. VOUT1/2 can't over the defined absolute maximum rating
VG	I/O	Capacitor to GND	LCD segment high driver voltage
VM	I/O	Capacitor to GND	LCD common un-selected driver voltage
V0	I/O	Capacitor to GND	LCD common high selected driver voltage *** Please reference P34 power off sequence for discharge.**
XV0	I/O	Capacitor to GND	LCD common low-selected driver voltage *** Please reference P34 power off sequence for discharge.**
C11P, C11M	--	Capacitor +/-	Capacitor 1 positive/negative connection pin for booster1 circuit.
C21P, C21M	--	Capacitor +/-	Capacitor 1 positive/negative connection pin for booster2 circuit.
C22P, C22M	--	Capacitor +/-	Capacitor 2 positive/negative connection pin for booster2 circuit.
C23P, C23M	--	Capacitor +/-	Capacitor 3 positive/negative connection pin for booster2 circuit.
C24P, C24M	--	Capacitor +/-	Capacitor 4 positive/negative connection pin for booster2 circuit.
C25P, C25M	--	Capacitor +/-	Capacitor 5 positive/negative connection pin for booster2 circuit.
C26P, C26M	--	Capacitor +/-	Capacitor 6 positive/negative connection pin for booster2 circuit.
C31P, C31M	--	Capacitor +/-	Capacitor 1 positive/negative connection pin for booster3 circuit.
VPP	--	External power	VPP is the power pin of embedded OTP (One-Time-Programming) non-volatile memory circuit. Only during OTP programming cycle VPP should connect to an external power source (about 7.5V). On the other cases, just keep this pin open. (Please reserve ITO contact pad for OTP programming if using OTP function)

*Make sure of the relationship of LCD driving voltage as follows

1. V0>VG>VM>GND>XV0
2. V0-VM=VM-XV0
3. VG-VM=VM-GND

FUNCTION DESCRIPTION

System Interface

System interface configuration

- The IST3257 has three high-speed system interfaces: 80-system 16-bit/8-bit bus, 68-system 16-bit/8-bit bus and I 4-line serial interface.
- The MPU interface mode is selected by the IM2-0 pins.
- For 8-bit interface, only the DB15-DB8 are activated, keep DB7-DB0 to GND or VCC.
- The IST3257 adopts 16-bit bus architecture. For 8-bit interface access, a 16-bit data (index or command) must be transferred by two times; the first is the high byte & the second is the low byte.

Command write

- The IST3257 adopts indirect command addressing mechanism, first must specify the command index, then write the command data into the index-addressed register.
- Command write flow

Step	RS	Description
1	0	Write Command index to IR (Index Register).
2	1	Write Command data into the command register indexed by IR.

RAM data write

- RAM data write flow

Step	RS	Description
1	0	Write Command index = R08H.
2	1	Write the initial RAM address.
3	0	Write Command index = R09H.
4	1	Write RAM data consecutively, the RAM address will be auto-incremented.

Status read

- Status read flow

Step	RS	Description
1	0	Read internal Status (dummy read is not needed).

RAM data read

- RAM data read flow

Step	RS	Description
1	0	Write Command index = R08H.
2	1	Write the target RAM address.
3	0	Write Command index = R09H.
4	1	Read RAM data; the first 16bit is dummy-read, the second 16bit is the real RAM data. The RAM address will auto-incremented.
5	--	If want to read RAM another address data, then repeat Step 1 → 4.

RAM Addressing Mapping(Grayscale mode, DSPM=011)

Segment Driver		AY[7:0]	SEG 1				SEG 2				SEG 3				SEG 4				SEG 5	.....	SEG 8	SEG 9	.....	SEG 12	.....	SEG 253	.....	SEG 256
SGS =0	AX[5:0]		00H																01H			02H			.....	3FH		
	BIT		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	.....	D0	D15	.....	D0		D15	.....	D0
SGS =1	AX[5:0]		3FH																3EH			3DH			.....	00H		
	BIT		D3	D2	D1	D0	D7	D6	D5	D4	D11	D10	D9	D8	D15	D14	D13	D12	D3		D12	D3		D12	.....	D3		D12
COM1		00H	Address: "0000"H																"0001"H			"0002"H			.....	"003F"H		
COM2		01H	Address: "0100"H																"0101"H			"0102"H			.....	"013F"H		
COM3		02H	Address: "0200"H																"0201"H			"0202"H			.....	"023F"H		
COM4		03H	Address: "0300"H																"0301"H			"0302"H			.....	"033F"H		
COM5		04H	Address: "0400"H																"0401"H			"0402"H			.....	"043F"H		
COM6		05H	Address: "0500"H																"0501"H			"0502"H			.....	"053F"H		
COM7		06H	Address: "0600"H																"0601"H			"0602"H			.....	"063F"H		
COM8		07H	Address: "0700"H																"0701"H			"0702"H			.....	"073F"H		
COM9		08H	Address: "0800"H																"0801"H			"0802"H			.....	"083F"H		
COM10		09H	Address: "0900"H																"0901"H			"0902"H			.....	"093F"H		
COM11		0AH	Address: "0A00"H																"0A01"H			"0A02"H			.....	"0A3F"H		
COM12		0BH	Address: "0B00"H																"0B01"H			"0B02"H			.....	"0B3F"H		
COM13		0CH	Address: "0C00"H																"0C01"H			"0C02"H			.....	"0C3F"H		
COM14		0DH	Address: "0D00"H																"0D01"H			"0D02"H			.....	"0D3F"H		
COM15		0EH	Address: "0E00"H																"0E01"H			"0E02"H			.....	"0E3F"H		
COM16		0FH	Address: "0F00"H																"0F01"H			"0F02"H			.....	"0F3F"H		
COM17		10H	Address: "1000"H																"1001"H			"1002"H			.....	"103F"H		
COM18		11H	Address: "1100"H																"1101"H			"1102"H			.....	"113F"H		
COM19		12H	Address: "1200"H																"1201"H			"1202"H			.....	"123F"H		
COM20		13H	Address: "1300"H																"1301"H			"1302"H			.....	"133F"H		
.....		.....	.....																.....			.....			.....	.....		
COM159		9EH	Address: "9E00"H																"9E01"H			"9E02"H			.....	"9E3F"H		
COM160		9FH	Address: "9F00"H																"9F01"H			"9F02"H			.....	"9F3F"H		
COM161		A0H	Address: "A000"H																"A001"H			"A002"H			.....	"A03F"H		
COM162		A1H	Address: "A100"H																"A101"H			"A102"H			.....	"A13F"H		

MSB D[4n+3]	D[4n+2]	D[4n+1]	LSB D[4n]	LCD
0	0	0	0	Non-selection display (unlit)
0	0	0	1	2/16 level grayscale display
0	0	1	0	3/16 level grayscale display
0	0	1	1	4/16 level grayscale display
0	1	0	0	5/16 level grayscale display
0	1	0	1	6/16 level grayscale display
0	1	1	0	7/16 level grayscale display
0	1	1	1	8/16 level grayscale display
1	0	0	0	9/16 level grayscale display
1	0	0	1	10/16 level grayscale display
1	0	1	0	11/16 level grayscale display
1	0	1	1	12/16 level grayscale display
1	1	0	0	13/16 level grayscale display
1	1	0	1	14/16 level grayscale display
1	1	1	0	15/16 level grayscale display
1	1	1	1	Selection display (lit)

Note : **n = 0, 1, 2, 3**

RAM Addressing Mapping (Mono mode, DSPM=100)

Segment Driver		AY[7:0]	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	SEG 8	SEG 9	SEG 10	SEG 11	SEG 12	SEG 13	SEG 14	SEG 15	SEG 16	SEG 17	.....	SEG 32	SEG 33	.....	SEG 48	.....	SEG 241	.....	SGE 256
SGS =0	AX[5:0]		00H																01H			02H			.....	0FH		
	BIT		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	.....	D0	D15	.....	D0		D15	.....	D0
SGS =1	AX[5:0]		0FH																12H			11H			.....	00H		
	BIT		D3	D2	D1	D0	D7	D6	D5	D4	D11	D10	D9	D8	D15	D14	D13	D12	D3		D12	D3		D12	.....	D3		D12
COM1		00H	Address: "0000"H																"0001"H			"0002"H			.....	"000F"H		
COM2		01H	Address: "0100"H																"0101"H			"0102"H			.....	"010F"H		
COM3		02H	Address: "0200"H																"0201"H			"0202"H			.....	"020F"H		
COM4		03H	Address: "0300"H																"0301"H			"0302"H			.....	"030F"H		
COM5		04H	Address: "0400"H																"0401"H			"0402"H			.....	"040F"H		
COM6		05H	Address: "0500"H																"0501"H			"0502"H			.....	"050F"H		
COM7		06H	Address: "0600"H																"0601"H			"0602"H			.....	"060F"H		
COM8		07H	Address: "0700"H																"0701"H			"0702"H			.....	"070F"H		
COM9		08H	Address: "0800"H																"0801"H			"0802"H			.....	"080F"H		
COM10		09H	Address: "0900"H																"0901"H			"0902"H			.....	"090F"H		
COM11		0AH	Address: "0A00"H																"0A01"H			"0A02"H			.....	"0A0F"H		
COM12		0BH	Address: "0B00"H																"0B01"H			"0B02"H			.....	"0B0F"H		
COM13		0CH	Address: "0C00"H																"0C01"H			"0C02"H			.....	"0C0F"H		
COM14		0DH	Address: "0D00"H																"0D01"H			"0D02"H			.....	"0D0F"H		
COM15		0EH	Address: "0E00"H																"0E01"H			"0E02"H			.....	"0E0F"H		
COM16		0FH	Address: "0F00"H																"0F01"H			"0F02"H			.....	"0F0F"H		
COM17		10H	Address: "1000"H																"1001"H			"1002"H			.....	"100F"H		
COM18		11H	Address: "1100"H																"1101"H			"1102"H			.....	"110FH		
COM19		12H	Address: "1200"H																"1201"H			"1202"H			.....	"120F"H		
COM20		13H	Address: "1300"H																"1301"H			"1302"H			.....	"130F"H		
.....		.....	.....																.....			.....			.....	.....		
COM159		9EH	Address: "9E00"H																"9E01"H			"9E02"H			.....	"9E0F"H		
COM160		9FH	Address: "9F00"H																"9F01"H			"9F02"H			.....	"9F0F"H		
COM161		A0H	Address: "A000"H																"A001"H			"A002"H			.....	"A00F"H		
COM162		A1H	Address: "A100"H																"A101"H			"A102"H			.....	"A10F"H		

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip oscillator and its frequency is nearly independent of Vcc. This oscillator signal is used in the voltage converter and display timing generation circuit. The oscillator circuit is only enabled when CLS = “H”. When on-chip oscillator is not used, CLS pin must be “L” condition. In this time, external clock must be input from CL pin.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL generated by oscillation clock, generates a clock to the line counter and a latch signal to the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 256-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data which is read to the LCD driver is completely independent of the access to the display data RAM from the microprocessor. The LCD AC signal, M is generated from the display clock. 2-frame AC driver waveforms with internal timing signal are shown in figure 1. It can generate n-line reversal alternating drive waveforms by setting data (NW-1) to the n-line reversal drive register.

LCD DRIVER CIRCUIT

This driver circuit is configured by 162-channel common driver and 256-channel segment driver. This LCD panel driver voltage Depends on the combination of display data and M signal (positive/negative frame).

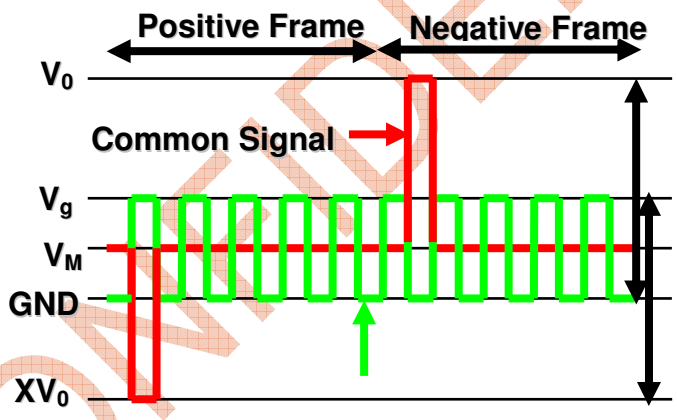


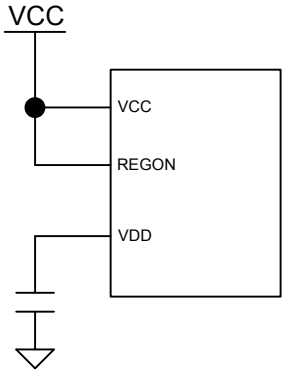
Figure 1. 2-frame AC driver waveforms with internal timing signal

POWER SUPPLY CIRCUIT

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are power regulator circuit, voltage converter circuits, and voltage regulator circuits. For details, refers to “Instruction Description”.

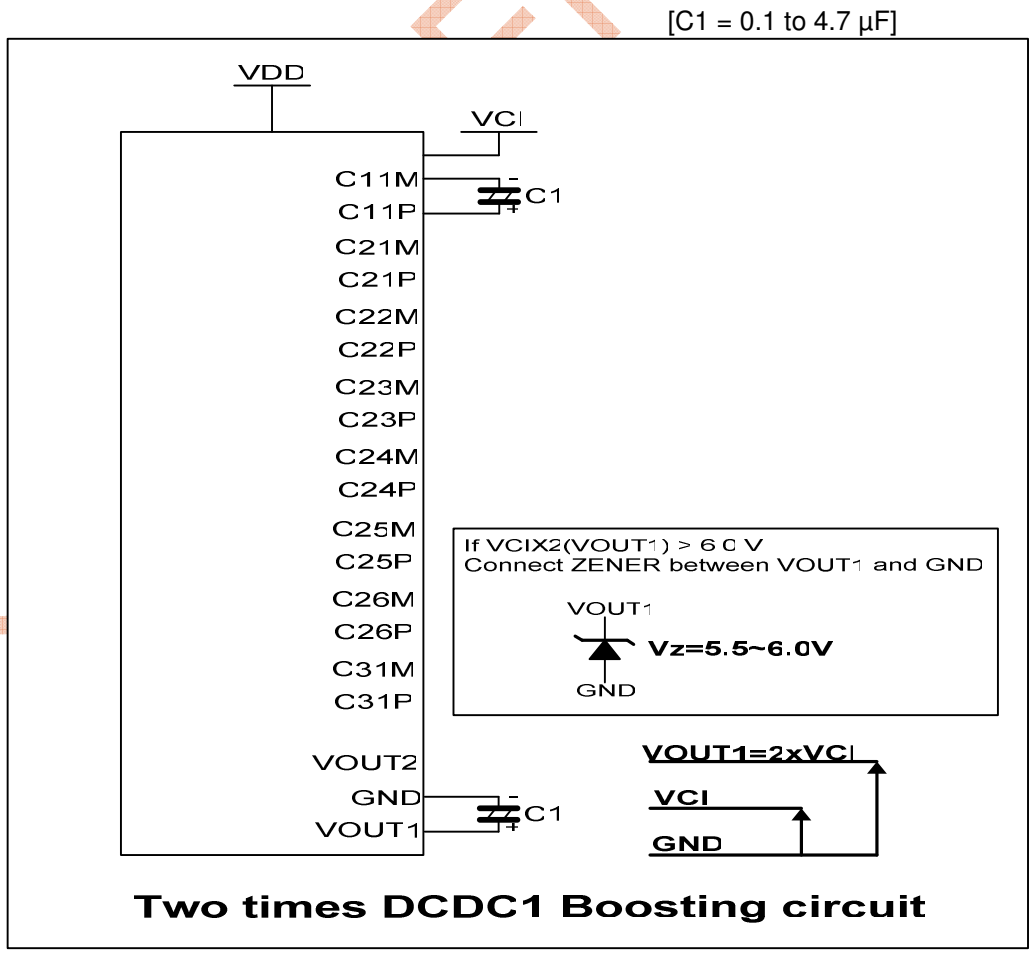
POWRE REGULATOR CIRCUIT

The IST3257 has a regulator circuit for VDD supply, the on-chip regulator configuration is shown as follows:

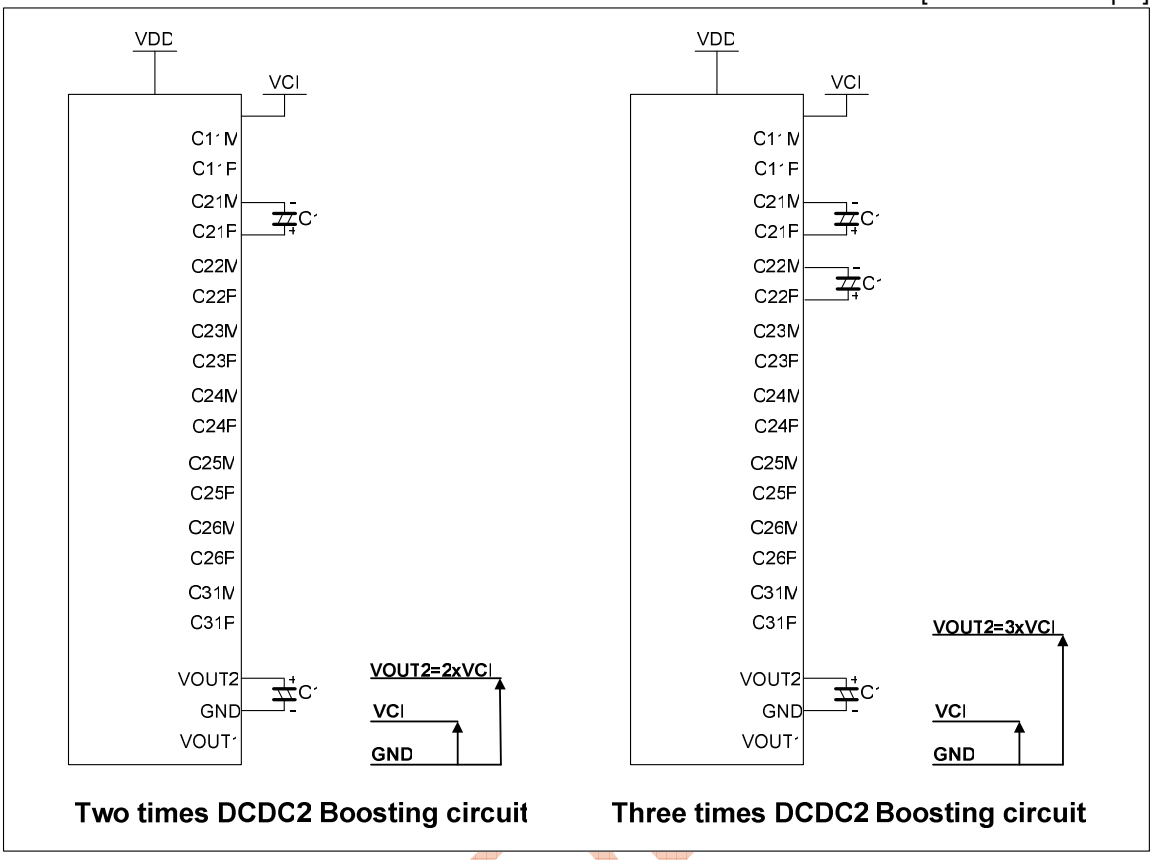


VOLTAGE CONVERTER CIRCUIT

These circuits boost up the electric potential between VCI and GND to 2, 3, 4, 5, 6, 7 times toward positive side and boosted voltage is outputted from VOUT1 and VOUT2 pin.

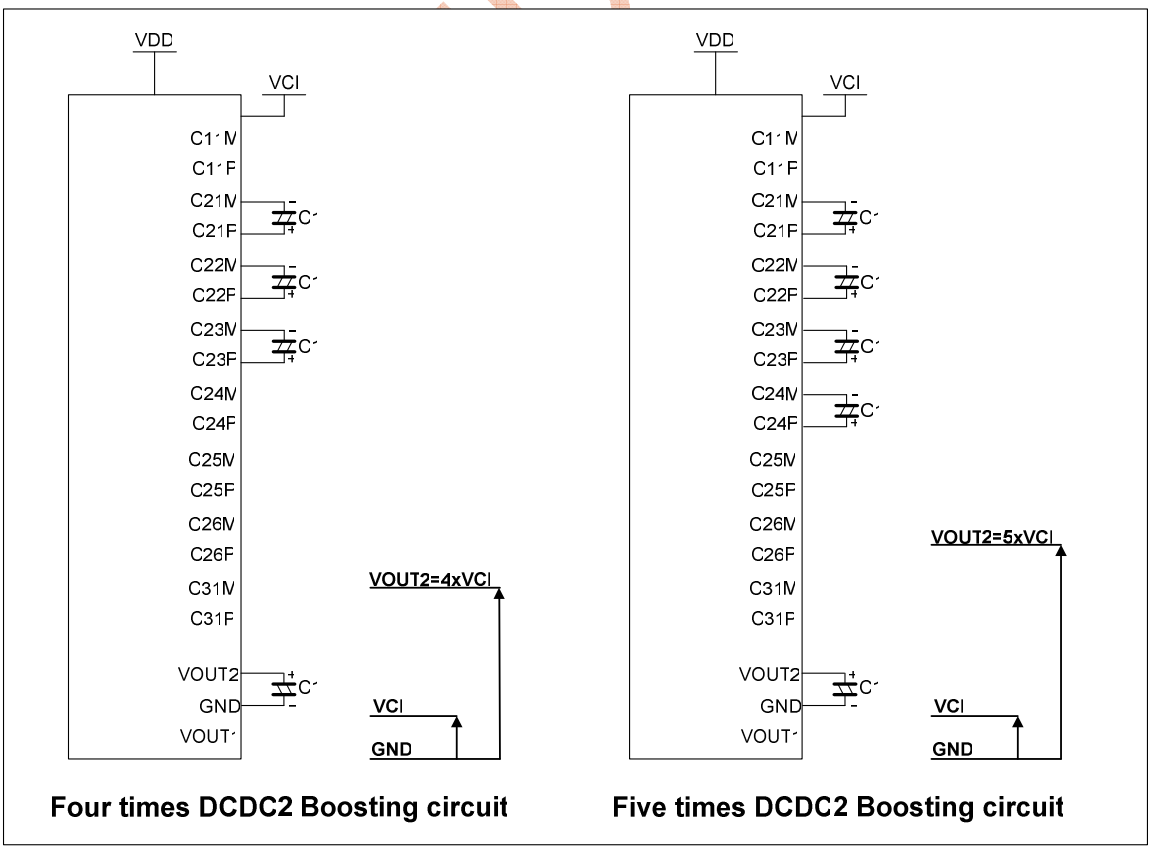


[C1 = 0.1 to 4.7 µF]



Two times DCDC2 Boosting circuit

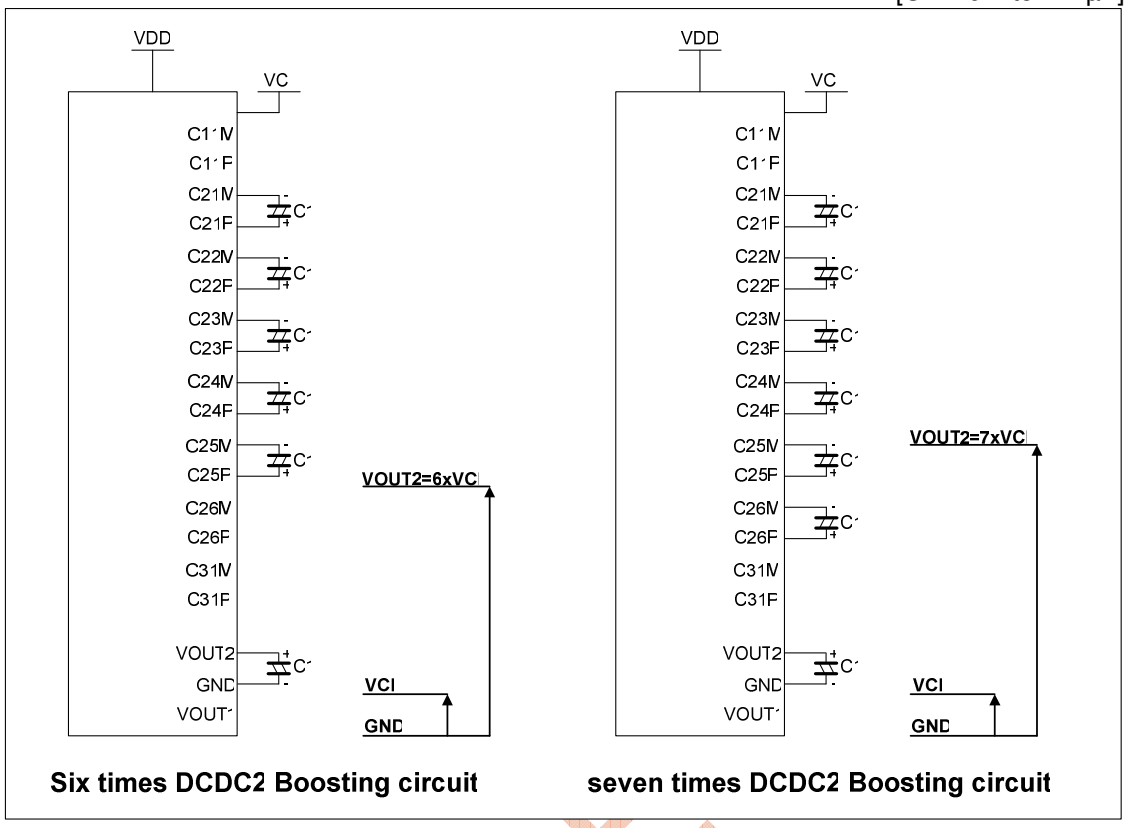
Three times DCDC2 Boosting circuit



Four times DCDC2 Boosting circuit

Five times DCDC2 Boosting circuit

[C1 = 0.1 to 4.7 µF]



Six times DCDC2 Boosting circuit **seven times DCDC2 Boosting circuit**

VOLTAGE REGULATOR CIRCUITS

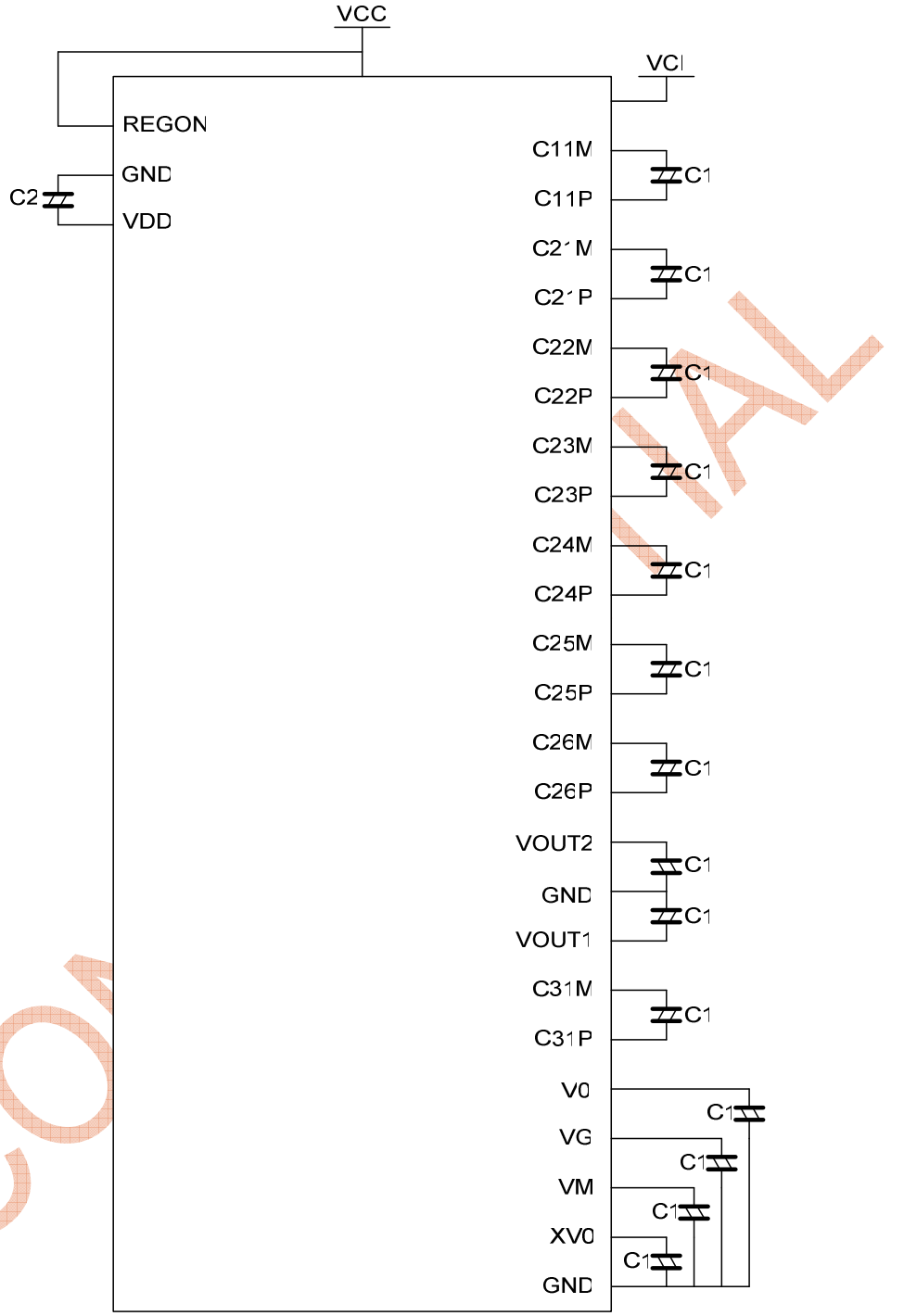
The IST3257 has an internal high accuracy fixed voltage power supply with 128 steps electronic volume function for VM OP-AMP. Through the use of VM electronic volume function, the LCD driver voltage VM can be controlled by contrast control command to adjust the VM voltage from 0.7V to 1.462V by 6mV per step which then makes it possible to adjust LCD brightness. The booster 1 circuit generates VM/VG used for power supply of internal OP-AMP.

CT[6:0]	Value	VM
0000000	0	0.700
0000001	1	0.706
0000010	2	0.712
:	:	:
1111101	125	1.450
1111110	126	1.456
1111111	127	1.462

The high selected voltage VM is to generate voltage VG and relation keep VG=2 x VM. And through the booster 2 circuit, V0 can be controlled by bias set command and this keeps the relation V0 – VM = N x VM (bias ration is 1/N). Finally, the booster 3 circuit inverts the V0 that refers to VM to generate XV0. The V0 and XV0 are both common select voltage.

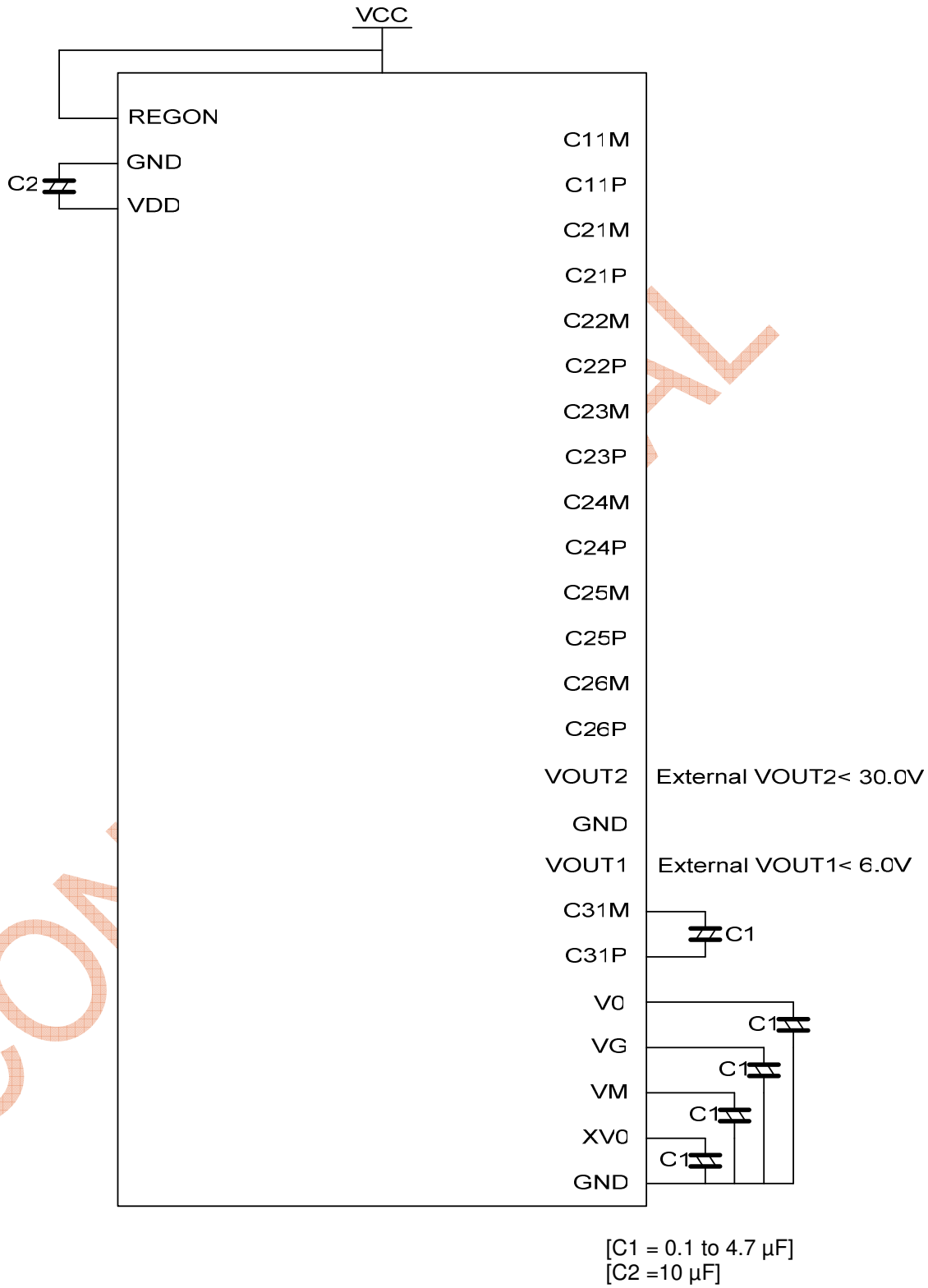
REFERENCE CIRCUIT EXAMPLES

Internal Power mode



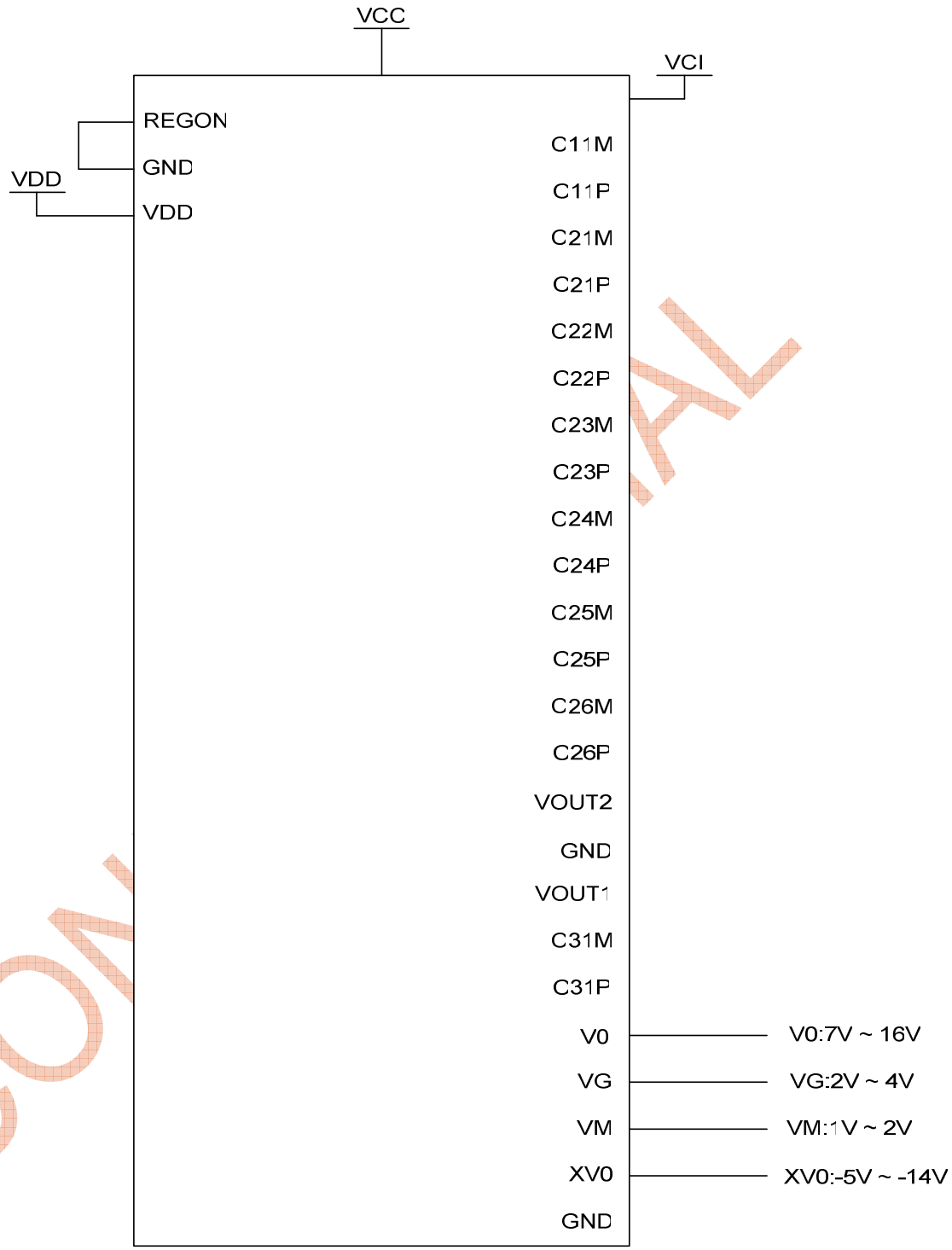
(REGON) : VCC , (DCDC3 , DCDC2 , DCDC1 , VMEN , VGEN , V0EN) : ON

External Power mode (External VOUT1 and VOUT2)



(REGON) : VCC , (DCDC2 , DCDC1) : OFF , (DCDC3 , VMEN , VGEN , V0EN) : ON

External Power mode (External All Power)



(REGON) : VCC , (DCDC3 , DCDC2 , DCDC1 , VMEN , VGEN , V0EN) : OFF

* C1 is determined by the size of the LCD being driven.Slect a value that will stabilize the liquid crystal drive voltage.

Command Table

ID	Command	R=1 W=0	RS	Upper Byte								Lower Byte							
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IR	Index	0	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R00h	Start Oscillator	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSC
	Device code	1	1	0	0	1	1	0	0	1	0	0	1	0	1	0	1	1	1
R01h	Driver control	0/1	1	0	0	0	0	0	0	0	0	0	0	SHL	SGS	0	0	NL1	NL0
R02h	Polarity control	0/1	1	0	0	0	0	0	0	EOR	BC	0	0	NW5	NW4	NW3	NW2	NW1	NW0
R03h	Power control (1)	0/1	1	0	0	0	0	VSON	DC3	DC2	DC1	1	VMEN	VGEN	V0EN	0	0	SLP	STB
R04h	Power control (2)	0/1	1	0	0	0	0	0	0	TC1	TC0	0	BS2	BS1	BS0	0	BT2	BT1	BT0
R05h	Contrast control	0/1	1	0	0	0	0	0	0	0	0	0	CT6	CT5	CT4	CT3	CT2	CT1	CT0
R06h	Entry mode	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	AM	ID1	ID0
R07h	Display control	0/1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	BW	REV	D
R08h	RAM Address	0/1	1	AY7	AY6	AY5	AY4	AY3	AY2	AY1	AY0	0	0	AX5	AX4	AX3	AX2	AX1	AX0
R09h	RAM data	0/1	1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0Ah	Starting Address	0/1	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R0Dh	RAM Window H-start/end	0/1	1	0	0	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	0	0	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R0Eh	RAM Window V-start/end	0/1	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R23h	Display Mode Control	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSPM2	DSPM1	DSPM0
R28h	Frame Rate Control	0/1	1	0	0	0	0	0	0	0	CSEL2	CTN1	CTN0	CSEL1	CSEL0	1	0	0	0
R30h	OTP program enable	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTE	0
R31h	OTP program start	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PGM
R3Bh	OTP Contrast offset	0	1	0	0	0	0	0	0	0	0	0	0	0	CTO4	CTO3	CTO2	CTO1	CTO0

Command Initialization

ID	Command	Initialization						
ID	Index	ID=00000000						
R00H	Start Oscillator	OSC=1						
R01h	Driver control	SHL=0	SGS=0	NL=11				
R02h	Polarity control	EOR=0	BC=0	NW=000000				
R03h	Power control (1)	VSON=0	DC=000	VMEN=0	VGEN=0	V0EN=0	SLP=0	STB=0
R04h	Power control (2)	TC=00	BS=000	BT=000				
R05h	Contrast control	CT=0000000						
R06h	Entry mode	AM=0	ID=11					
R07h	Display control	VLE2=0	VLE1=0	PTE2=0	PTE1=0	BW=0	REV=0	D=0
R08h	RAM Address	AY=00000000	AX=000000					
R09h	RAM data	DB=0						
R0Ah	Starting Address	VL=00000000						
R0Dh	RAM Window H-start/end	HEA=111111	HAS=000000					
R0Eh	RAM Window V-start/end	VEA=10100001	VSA=00000000					
R23h	Display Mode control	DSPM=000						
R28h	Frame Rate Control	CSEL=0	CTN=00					
R30h	OTP program enable	CTE=0						
R31h	OTP program start	PGM=0						
R3Bh	Contrast offset	CTO=00000000						

INSTRUCTION DESCRIPTION

Index

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
IR	0	0	0	0	0	0	0	0	0	0	ID							

ID Select the register are used to access by MPU, the ID provide 128 register number (00H ~ FFH), IST3257 only used 16 registers.

Oscillator control and Device code

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OSC
	0	1	0	0	1	1	0	0	1	0	0	1	0	1	0	1	1	1

OSC This command starts the operation of the built-in oscillator circuit, when OSC=1, oscillator ON, OSC=0, oscillator OFF.

If RS=0 & read through parallel interface, "3257"H is read, It can't be read through serial interface.

Driver control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
01	0	0/1	0	0	0	0	0	0	0	0	0	0	SHL	SGS	0	0	NL	

SHL This command is used to set common shift format and direction according to module.

SHL	**0**	COM1→COM2…COM79→COM80→COM81→ COM82…COM160→COM161→COM162
	1	COM162→COM161…COM82→COM81→COM80 →COM79…COM3→COM2→COM1

SGS Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.
SGS = 0 : normal direction (SEG1 to SEG256)
SGS = 1 : reverse direction (SEG256 to SEG1)

NL Duty Select

NL1	NL0	DUTY
0	0	1/162
0	1	1/64
1	0	1/128
1	1	NA

DUTY	COM SCAN
1/162	COM1~COM162
1/128	COM1~COM128
1/64	COM1~COM64

Polarity Control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
02	0	0/1	0	0	0	0	0	0	EOR	BC	0	0	NW					

Polarity alternating pattern select.

BC	EOR	Pattern	Description
0	X	B-pattern	Polarity alternating by frame
1	0	C-pattern	Polarity alternating by line(1~64), which is specified by NW
1	1	C-pattern	B-pattern & C-pattern EXOR to generate the alternating timing control

BC=1 , NW=0 : 1 line select
NW=63 : 64 line select

Power Control (1)

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
03	0	0/1	0	0	0	0	**VSON**	DC3	DC2	DC1	1	**VMEN**	**VGEN**	**V0EN**	0	0	SLP	STB

VSON Control the status of internal Vref circuit. When VSON=1, the internal Vref circuit is enable. And when VSON=0, the internal Vref circuit is disable.
DC3/DC2/DC1 The value of 3-bits registers decided that the DCDC3, DCDC2 and DCDC1 circuits is ON/OFF, individually.
VMEN/VGEN/V0EN Determine the status of VM OP-AMP circuit, VG regulator, V0 regulator and XV0 regulator, individually. An external power supply and part of internal power supply functions can be used simultaneously.

DC3	DC2	DC1	VMEN	VGEN	V0EN	Status of internal power supply circuits
0 1						Internal DCDC3(XV0) circuit is OFF Internal DCDC3(XV0) circuit is ON
	0 1					Internal DCDC2(V0) circuit is OFF Internal DCDC2(V0) circuit is ON
		0 1				Internal DCDC1(VG) circuit is OFF Internal DCDC1(VG) circuit is ON
			0 1			Internal VM OP-AMP circuit is OFF Internal VM OP-AMP circuit is ON
				0 1		Internal VG regulator is OFF Internal VG regulator is ON
					0 1	Internal V0 regulator is OFF Internal V0 regulator is ON

SLP/STB The power save mode consists of the sleep and stand-by mode. The display data RAM can also be accessed from the MPU in the power save mode.The suggest sleep/stand-by mode flow is listed as below:

Sleep Mode **:** DISPLAY OFF,POWER OFF,OSC Normally

STEP	ID	RS	RW	COMMAND	DESCRIPTION
1	07	0	0	0000h	Display off
2	03	0	0	0000h	Power off
3	03	0	0	0002h	Enter into Sleep mode

Stand-by Mode **:** DISPLAY OFF,POWER OFF,OSC OFF

STEP	ID	RS	RW	COMMAND	DESCRIPTION
1	07	0	0	0000h	Display off
2	03	0	0	0000h	Power off
3	03	0	0	0001h	Enter into Stand-by mode

Power Control (2)

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
04	0	0/1	0	0	0	0	0	0	TC		0	BS			0	BT		

Temperature coefficient curve select

TC1	TC0	V_{REF}	T.C curve
0	0	0.7v	-0.00 %/℃
0	1	0.7v	-0.05 %/℃
1	0	0.7v	-0.10 %/℃
1	1	0.7v	-0.15 %/℃

Bias select

BS2	BS1	BS0	Bias
0	0	0	1/6
0	0	1	1/7
0	1	0	1/8
0	1	1	1/9
1	0	0	1/10
1	0	1	1/11
1	1	0	1/12
1	1	1	1/13

Booster multiple select

BT2	BT1	BT0	Boost2 (Vout2)
0	0	0	VCI x 2
0	0	1	VCI x 3
0	1	0	VCI x 4
0	1	1	VCI x 5
1	0	0	VCI x 6
1	0	1	VCI x 7
1	1	0	NA
1	1	1	NA

Contrast Control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
05	0	0/1	0	0	0	0	0	0	0	0	0	CT						

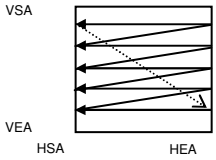
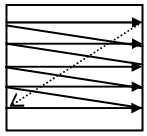
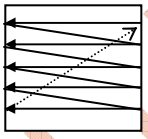
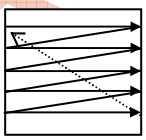
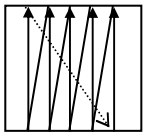
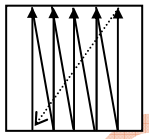
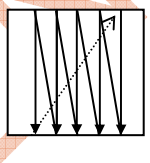
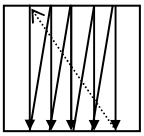
CT6	CT5	CT4	CT3	CT2	CT1	CT0	Reference voltage Parameter (α)	VM	Contrast
0	0	0	0	0	0	0	0 (default)	Minimum	Low
0	0	0	0	0	0	1	1		
	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	64	:	:
	:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126		
1	1	1	1	1	1	1	127	Maximum	High

Entry mode

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
06	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	AM	ID	

ID AX/AY address auto-increment/decrement control after data is written to display RAM. AX/AY address will auto back to the confront corner of the addressing window set by HEA, HSA & VEA, VSA.

AM Horizontal/Vertical mode select. When AM=0/1, the data is continuously written in horizontal/vertical direction.

	ID = "00" H: Decrement V: Decrement	ID= "01" H: Increment V: Decrement	ID = "10" H: Decrement V: Increment	ID = "11" H: Increment V: Increment
AM=0				
AM=1				

Display control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
07	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	BW	REV	D

BW All display shows black On/Off. When BW=1 all the display images will shows deepest grayscale.

REV Reverse display On /Off. When REV=1 all the display images will reverse the grayscale.

D This bit is used to turn on the LCD state, When D=1, LCD will be drived.

RAM address

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
08	0	0/1	AY								0	0	AX					

This command is used to specify a row address (AY) and column address (AX) of internal RAM. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

AY7	AY6	AY5	AY4	AY3	AY2	AY1	AY0	Row address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	1	0	0	0	0	0	160
1	0	1	0	0	0	0	1	161

AX5	AX4	AX3	AX2	AX1	AX0	Column address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

RAM data

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
09	0	0/1	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

This command is used to write/read data to the display RAM.
When the display RAM data is accessed, the column or row address is incremented by one. To exit the state specified with this command, input another command.

Starting address

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0A	0	0/1	0	0	0	0	0	0	0	0	VL							

VL Sets the line address of the Display RAM to determine the initial display line. The display data of the specified line address is displayed at the COM0 of the LCD panel , the range is 0 to 161.

RAM window horizontal start/end

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0D	0	0/1	0	0	HEA						0	0	HSA					

HSA/HEA Horizontal addressing window range define. HSA defines the AX starting position, HEA defines the AX ending position. When AX is automatically incremented or decremented, if AX reaches the boundary (HEA or HSA), it will automatically back to the opposite starting position, the range of HSA and HEA are 0 to 63.

RAM window vertical start/end

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0E	0	0/1	VEA								VSA							

VSA/VEA Vertical addressing window range define. VSA defines the AY starting position, VEA defines the AY ending position. When AY is automatically incremented or decremented, if AY reaches the boundary (VEA or VSA), it will automatically back to the opposite starting position, the range of VSA and VEA are 0 to 161.

Display Mode control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
23	0	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0	DSPM		

DSPM It offers a flexible display type and supports a variety of display interface, the 16 gray levels are formed by pure FRC, please setup the type before display on command. see below as type selection.

DSPM	Display type
011	Pure FRC (gray levels)
100	Mono

Frame rate control

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
28	0	0/1	0	0	0	0	0	0	0	CSEL 2	CTN		CSEL		1	0	0	0

CTN/CSEL/RTN The frame rate adjust depends on duty selection(NL), CTN and CSEL, see the below mapping table.

$$f_{Frame\ (Hz)} = \frac{f_{osc}}{(duty \times factor \times 64)}$$

CSEL2	CSEL	factor
0	00	1.5
0	01	2.0
0	10	2.5
0	11	3.0
1	xx	1.0

Frame Rate Table

		DUTY (NL[1:0])		
Fosc(KHz)	CSEL[2:0]	64	128	162
760 (CTN=00)	100	186	93	73
	000	124	62	49
	001	93	46	37
	010	74	37	29
	011	62	31	24
1300 (CTN=01)	100	317	159	125
	000	212	106	84
	001	159	79	63
	010	127	63	50
	011	106	53	42
2000 (CTN=10)	100	488	244	193
	000	326	163	129
	001	244	122	96
	010	195	98	77
	011	163	81	64
2100 (CTN=11)	100	513	256	203
	000	342	171	135
	001	256	128	101
	010	205	103	81
	011	171	85	68

OTP program enable

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTE	0

CTE It identified contrast offset parameters for OTP to program.

OTP program start

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PGM

PGM When PGM enable, the OTP control logic enters the programming state and the BUSY flag immediately toggle to high until program done, the duration of program about 10ms

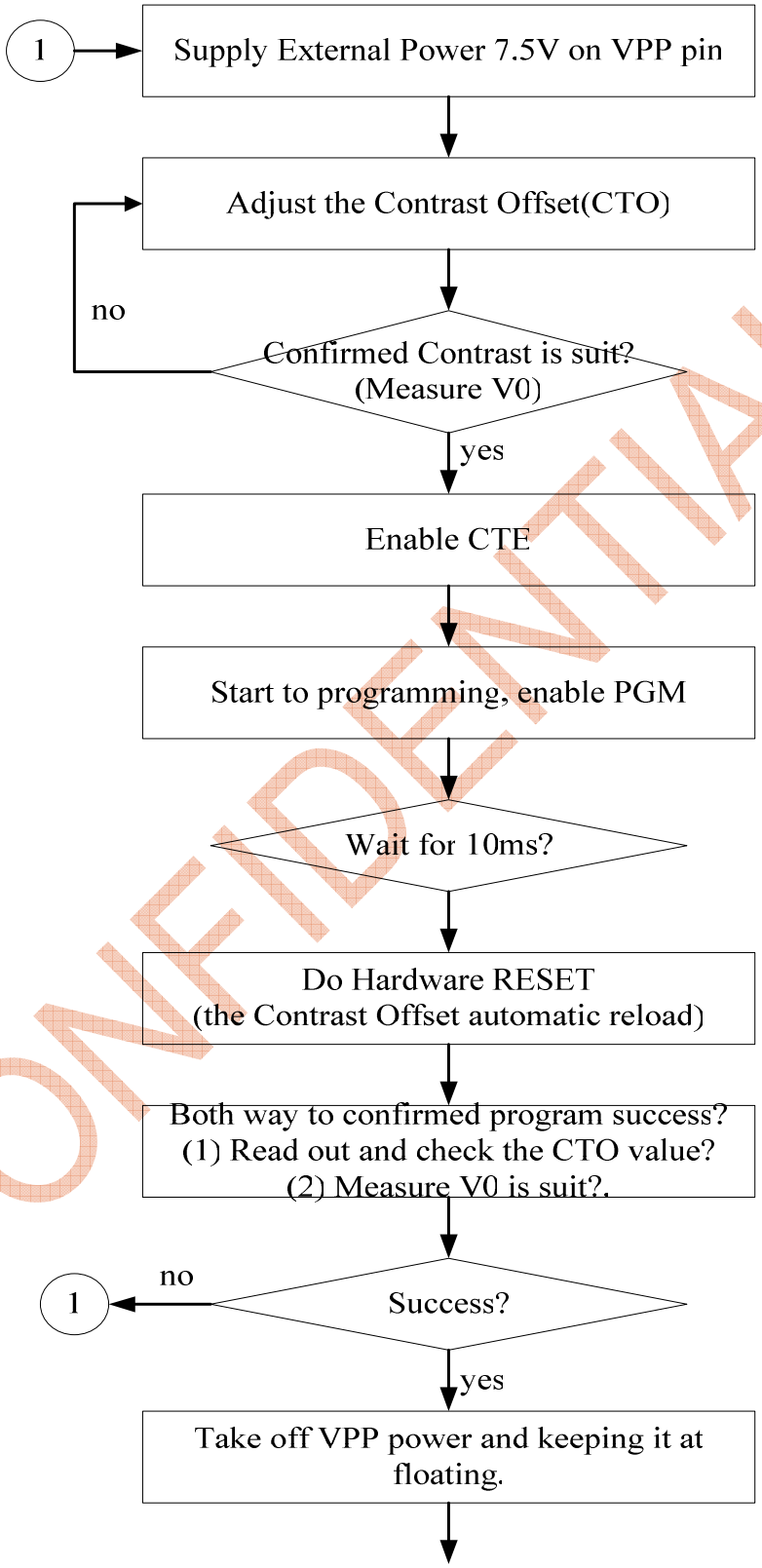
Contrast offset adjustment

ID	RS	RW	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
3B	0	0/1	0	0	0	0	0	0	0	0	0	CTO						

CTO this offset parameters that is more flexible to adjust the electronic contrast level, the total of 32 steps can cover the range from +15 to -16, the actual contrast level as CT (base level) + CTO (offset level).
Notice that the CTO only supply for two times to program, when it was programmed, the last contents of CTO was ignored.

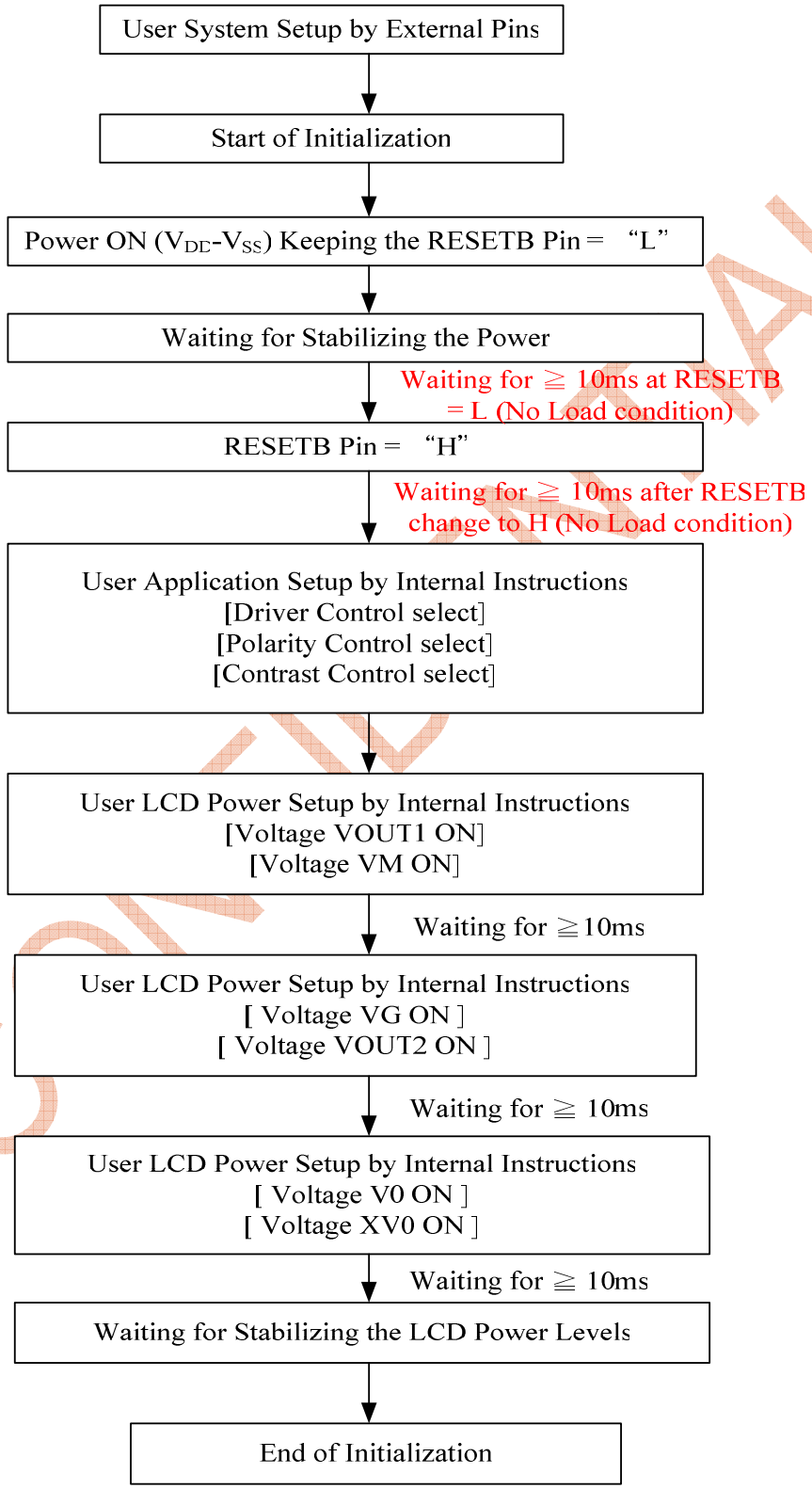
CTO4	CTO3	CTO2	CTO1	CTO0	Offset level
0	1	1	1	1	+15
0	1	1	1	0	+14
:	:	:	:	:	:
0	0	0	0	1	+1
0	0	0	0	0	0
1	1	1	1	1	-1
:	:	:	:	:	:
1	0	0	0	1	-15
1	0	0	0	0	-16

OTP Programming Flow

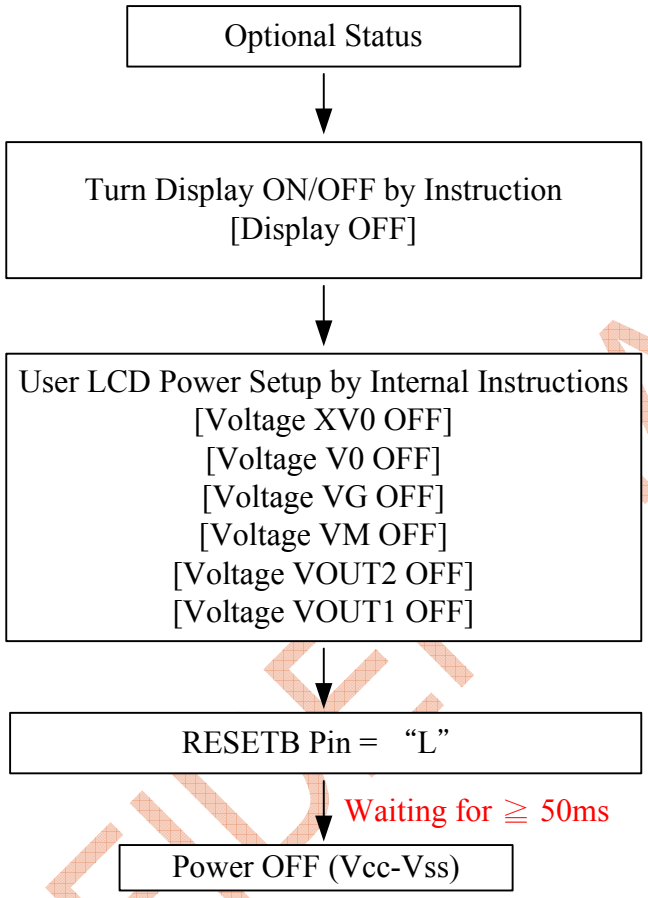


Power On Sequence

Initializing with the Built-in Power Supply Circuits



Power Off Sequence



* Avoid to abnormal display for power off , strongly suggest connect 1MΩ resistor from V0 and XV0 to GND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage range	VCC	-0.3 to +8.0	V
	VOUT1	-0.3 to +8.0	V
	VOUT2	-0.3 to +35V	V
Input voltage range	V_{IN}	-0.3 to VCC + 0.3	V
Operating temperature range	T_{OPR}	-40 to +85	℃
Storage temperature range	T_{STR}	-55 to +110	℃

NOTES

1. VCC and VOUT are measured based on GND = 0V
2. Voltages V0 ≧ VG ≧ VM ≧ GND ≧ XV0 must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
4. It is desirable to use this LSI under electrical characteristic conditions during general operation, otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERS

(VCC = 2.4 to 3.6V, VOUT2=12 ~30V, Ta = -30 to +80℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin
Operating Voltage	V_{CC}		2.4	-	3.6	V	VCC
Input voltage	V_{IH}		0.8 * V_{CC}	-	V_{CC}	V	RSTB, IM2-0, DB15-0, EWRB_SCL, RWRDB_SDA, RS, CSB, IRS, CLS, REGON
	V_{IL}		GND	-	0.2 * V_{CC}		
Output voltage	V_{OH}	I_{OH} = -0.4mA	0.8 * V_{CC}	-	V_{CC}	V	DB15-0
	V_{OL}	I_{OL} = 0.4mA	GND	-	0.2 * V_{CC}		
Input leakage current	I_{IL}	V_{IN} = V_{CC} or GND	-1.0		1.0	µA	RSTB, IM2-0, DB15-0, EWRB_SCL, RWRDB_SDA, RS, CSB, CLS, REGON
LCD driver ON Resistance	R_{ON}				2	kΩ	COMn, SEGn (*1)
Oscillator frequency	Fosc	CLS = 1, CTN = 00	600	760	910	KHz	Test2(*2)
		CLS = 1, CTN = 01	1040	1300	1560	KHz	Test2(*2)
		CLS = 1, CTN = 10	1600	2000	2400	KHz	Test2(*2)
		CLS = 1, CTN = 11	1680	2100	2520	KHz	Test2(*2)
Voltage converter input voltage	VCI		2.4	-	3.6	V	VCI (*3)
Voltage converter operating voltage	VOUT1		4.0		6.0	V	VOUT1(*3)
OTP programming voltage	VPP		7.25	7.5	7.75	V	
Reference voltage	VREF	VCC = 3.0v TC=00	0.6	0.7	0.8	V	VREF (Ta=25℃)
		VCC = 3.0v TC=01	0.6	0.7	0.8		
		VCC = 3.0v TC=10	0.6	0.7	0.8		
		VCC = 3.0v TC=11	0.6	0.7	0.8		
Driver Operating Voltage	V0			-	16	V	V0
Dynamic current consumption	Idy	V_{CC} = 3.0V Internal OSC on Frame Rate=70Hz Internal Power on (VCI = V_{CC}, x6 boost) CT<6:0>=30H Bias =1/13 1/160 duty ratio Display pattern : 2-pixel Checker	-	300	500	µA	COMn, SEGn floating (no load) (Ta=25℃)
Static current consumption	Istat	V_{CC} = 3.0V Display OFF Power OFF OSC OFF	-	-	20	µA	(Ta=25℃)

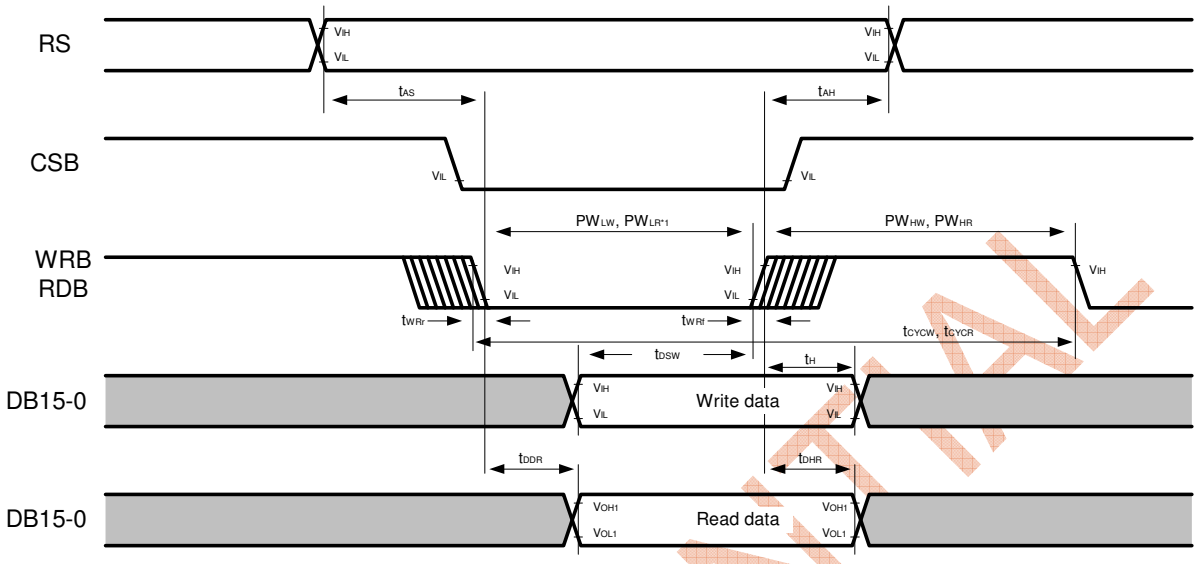
Note:
(1) Resistance value when +/- 0.1mA is applied during the ON status of the output pins SEGn & COMn
R_{ON} = ΔV / 0.1 (KΩ) (ΔV: voltage change when +/- 0.1mA is applied)

(2) Need into test mode (VCC=3.0V)

(3) VCI x Boost1 gain (x2) must lower than 6.0V (VOUT1).

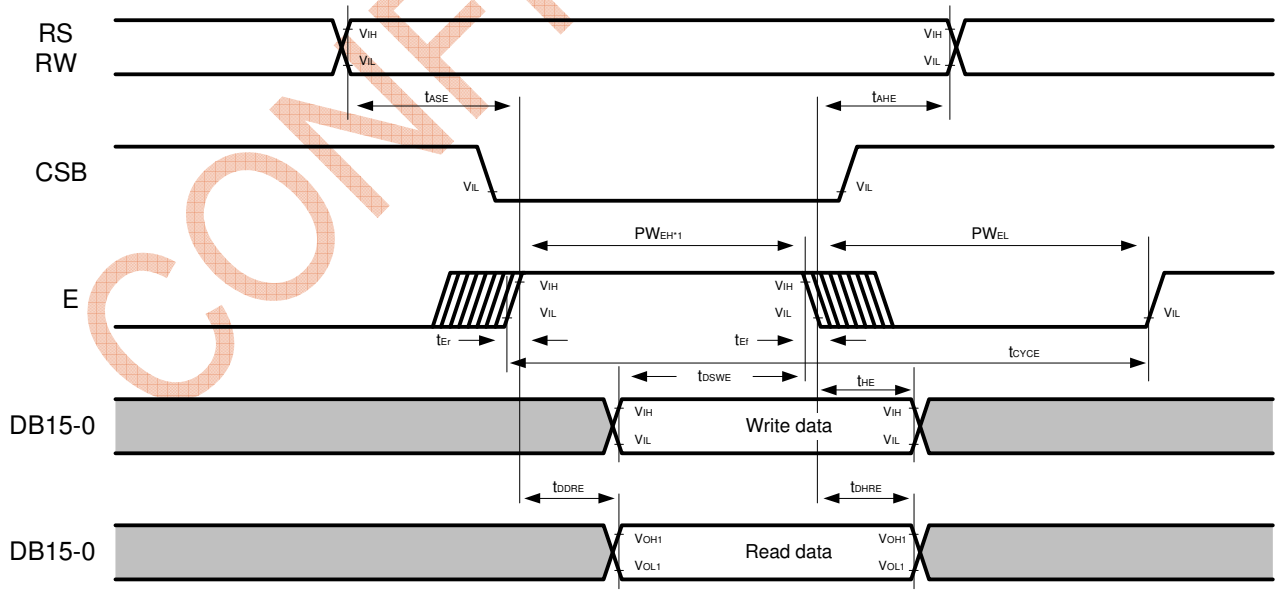
AC CHARACTERS

80-System Bus Operation



Note : PW_{LW} and PW_{HR} are specified in the overlapped period when CSB is low and WRB or RDB is low.

68-System Bus Operation



Note : PW_{EH} is specified in the overlapped period when CSB is low and E is high.

80-System Bus Interface Timing Characteristics

VCC = 2.4 to 3.6 V **Temp = -30 to +80℃**

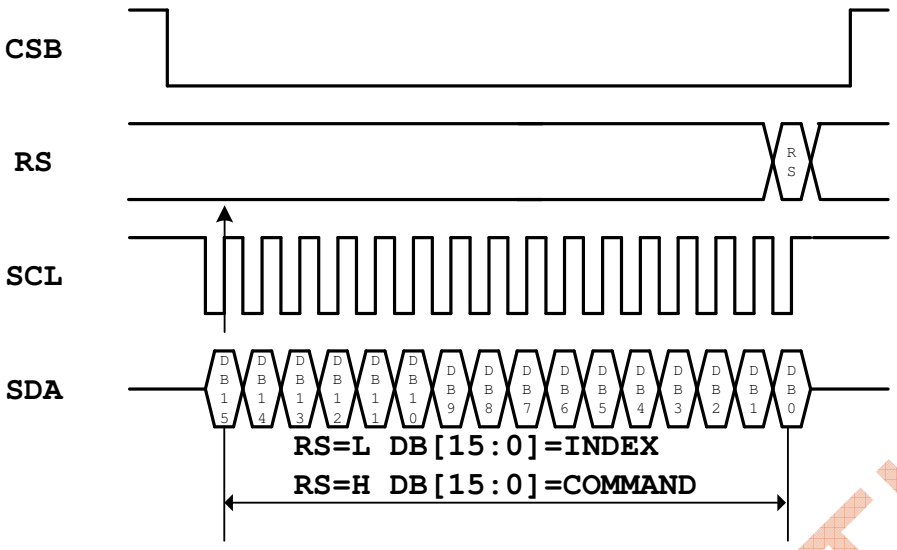
Item		Symbol	Min	Typ	Max	Unit
Bus cycle time	Write	t_{CYCW}	350			ns
	Read	t_{CYCR}	500			ns
Write low-level pulse width		PW_{LW}	170			ns
Read low-level pulse width		PW_{LR}	250			ns
Write high-level pulse width		PW_{HW}	180			ns
Read high-level pulse width		PW_{HR}	250			ns
Write/Read rise/fall time		t_{WRr} , $_{WRf}$			15	ns
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50			ns
Address hold time		t_{AH}	20			ns
Write data setup time		t_{DSW}	70			ns
Write data hold time		t_{H}	60			ns
Read data delay time		t_{DDR}			200	ns
Read data hold time		t_{DHR}	5			ns

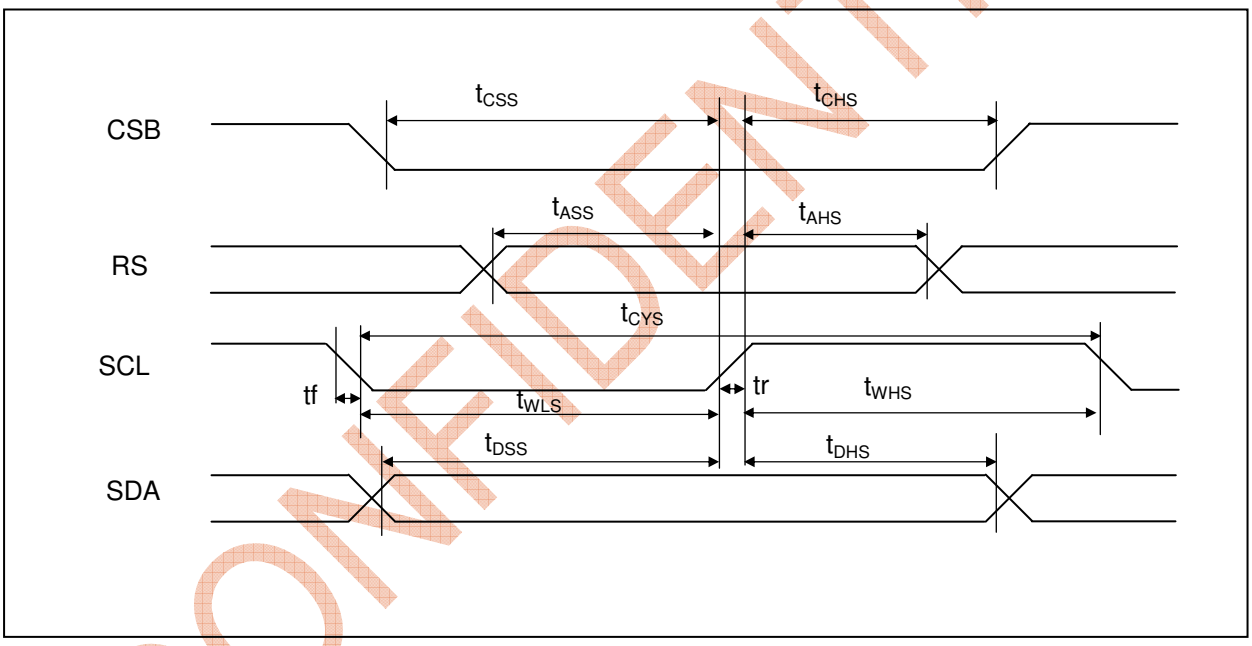
68-System Bus Interface Timing Characteristics

VCC = 2.4 to 3.6 V **Temp = -30 to +80℃**

Item		Symbol	Min	Typ	Max	Unit
Enable cycle time	Write	t_{CYCE}	350			ns
	Read	t_{CYCE}	500			ns
Enable high-level pulse width	Write	PW_{EH}	170			ns
	Read	PW_{EH}	250			ns
Enable low-level pulse width	Write	PW_{EL}	180			ns
	Read	PW_{EL}	250			ns
Enable rise/fall time		t_{WRr} , $_{WRf}$			15	ns
Setup time (RS to CS*, WR*, RD*)		t_{ASE}	50			ns
Address hold time		t_{AHE}	20			ns
Write data setup time		t_{DSWE}	70			ns
Write data hold time		t_{HE}	60			ns
Read data delay time		t_{DDRE}			200	ns
Read data hold time		t_{DHRE}	5			ns

4 Line Serial Interface Timing Characteristics





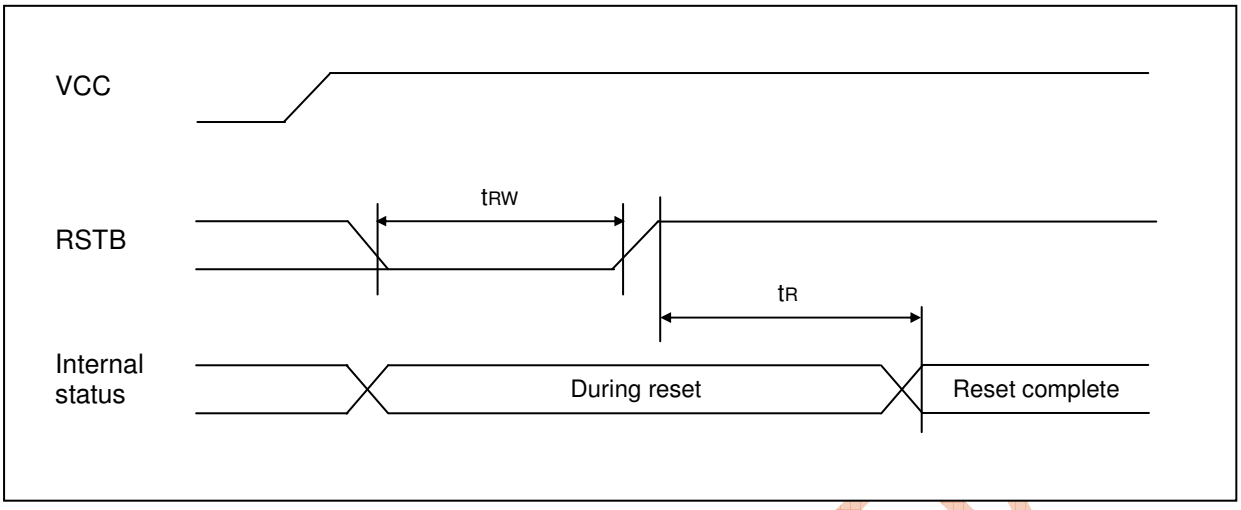
VCC = 2.4 to 3.6V **Temp = -30 to +80℃**

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle	SCL	tCYS	250	-	-	ns	
SCLK high pulse width	SCL	tWHS	125	-	-		
SCLK low pulse width	SCL	tWLS	125	-	-		
RS setup time	RS	tASS	110	-	-	ns	
RS hold time	RS	tAHS	110	-	-		
Data setup time	SDA	tDSS	110	-	-	ns	
Data hold time	SDA	tDHS	110	-	-		
CSB setup time	CSB	tCSS	110	-	-	ns	
CSB hold time	CSB	tCHS	110	-	-		

*Note1 : The Input signal rise and fall time (tr,tf) are specified at 15ns or less.

*Note2 : All timing is specified using 20% and 80% of VCC as the standard.

Reset Input Timing

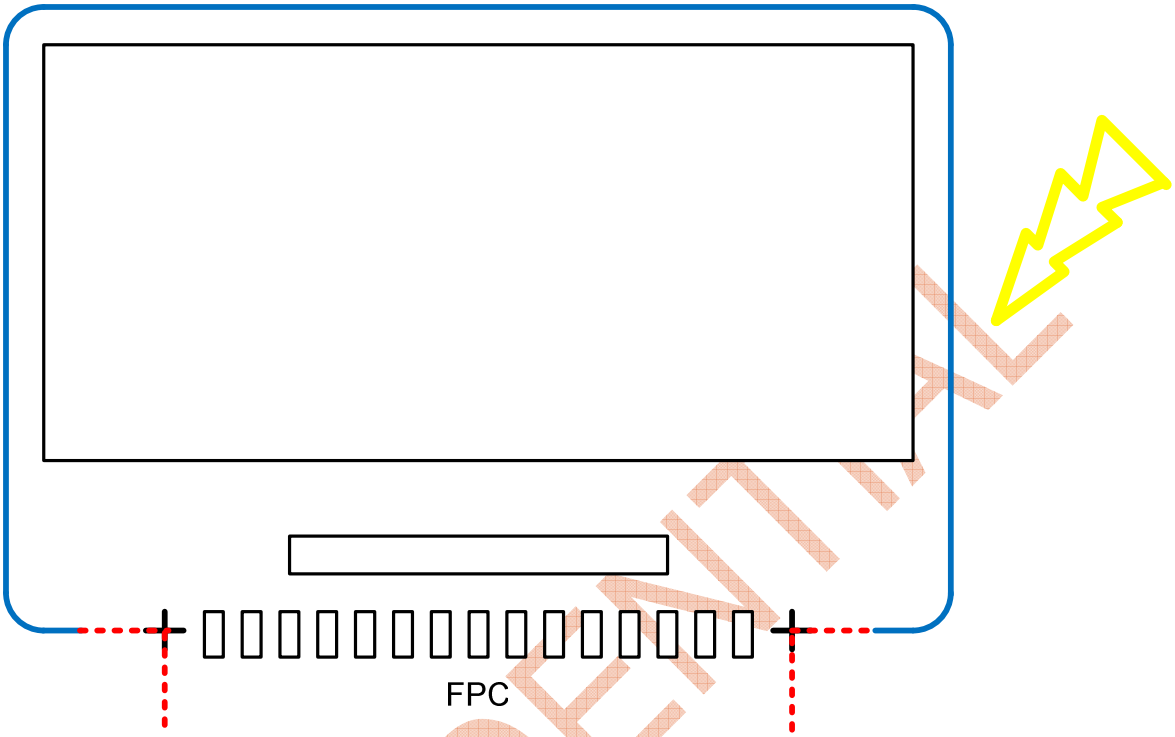


VCC = 2.4 to 3.6V **Temp = -30 to +80℃**

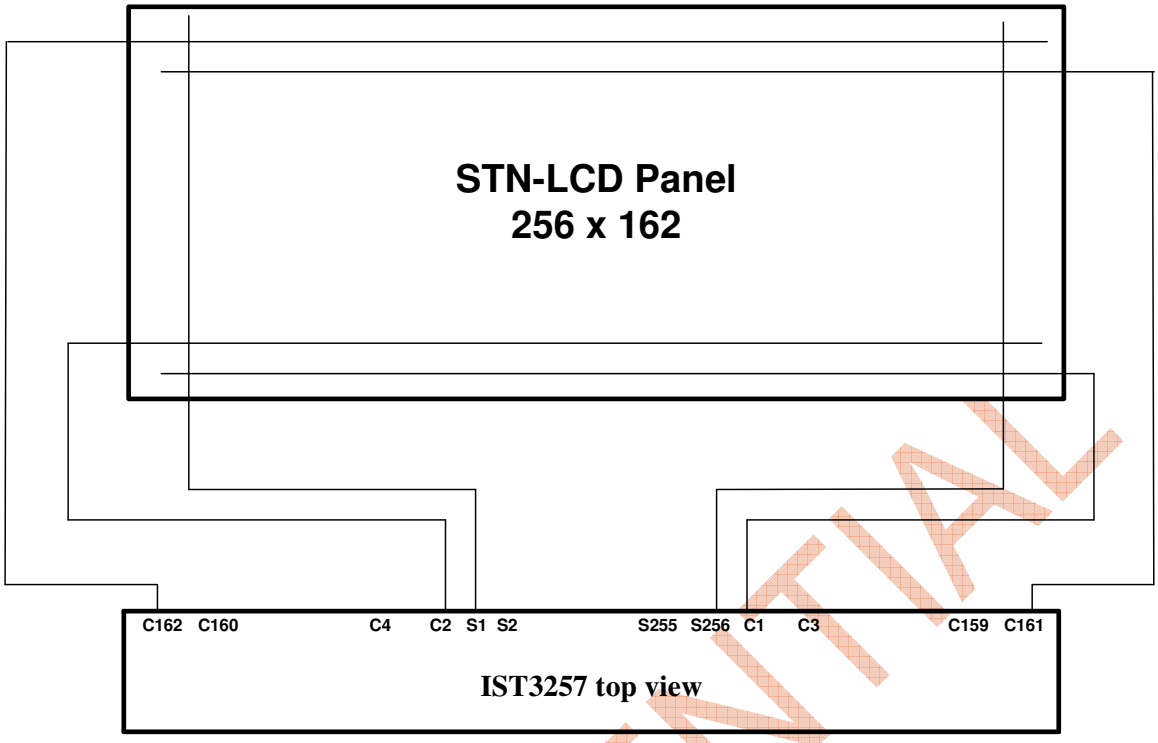
Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	RSTB	t_{RW}	2	-	-	us	
Reset time	-	t_R	10	-	-	ms	

APPLICATION NOTE

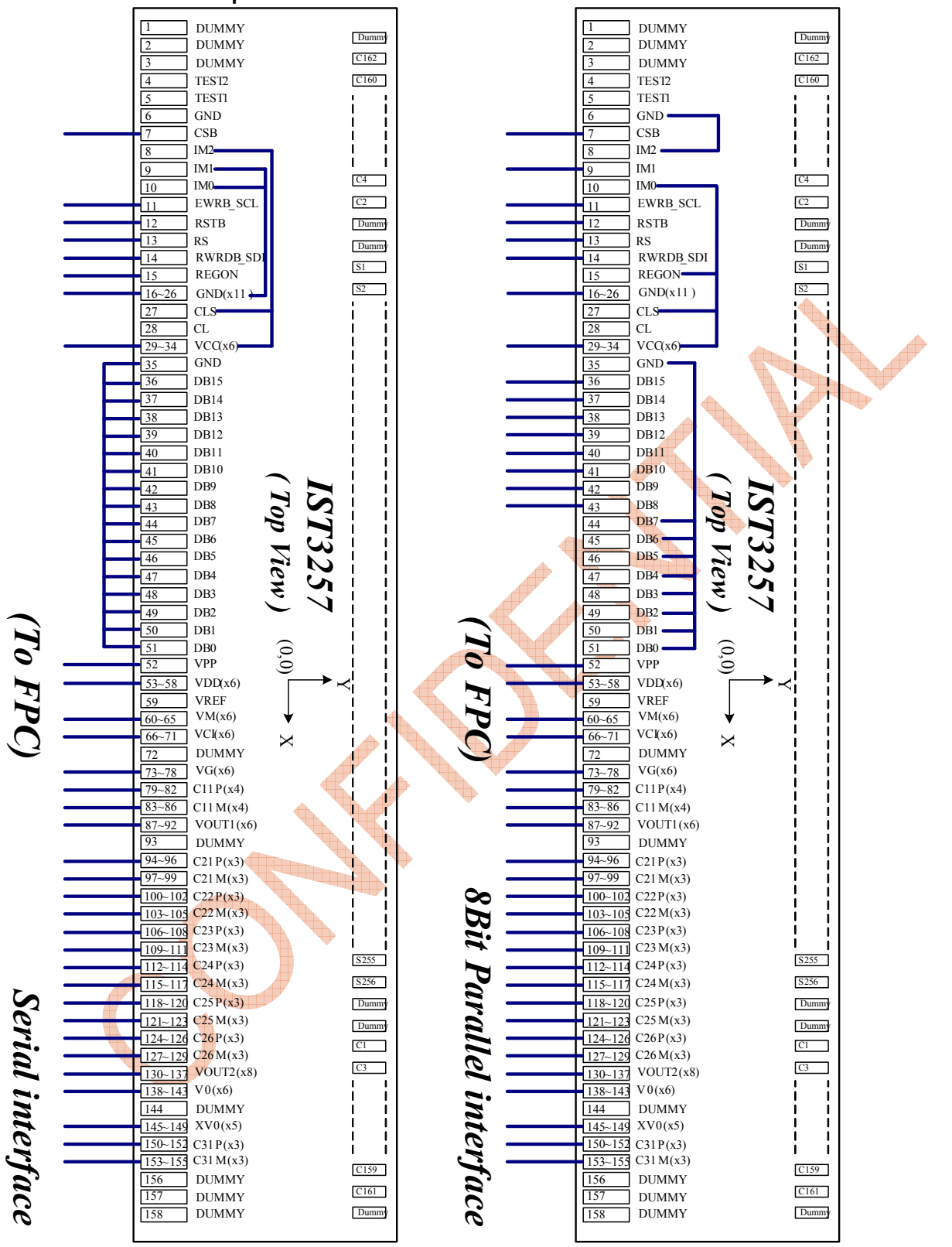
1. Add ESD protection ring



2. Driver side

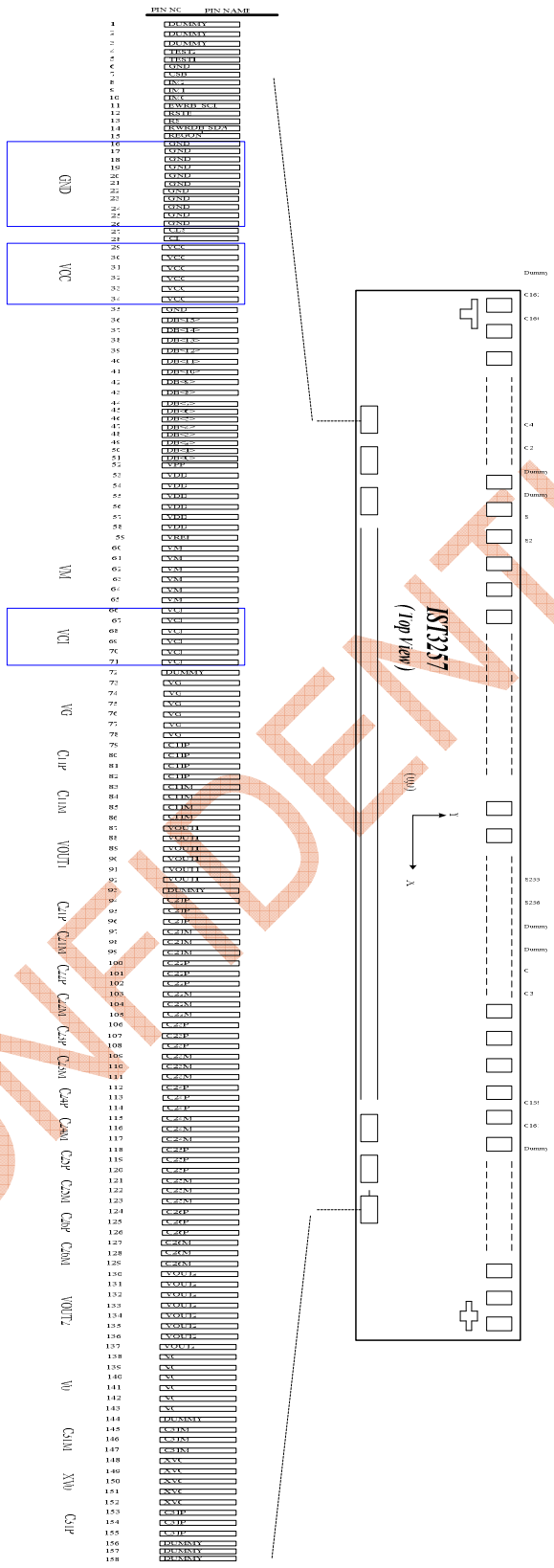


3. ITO connection example



- **ITO Resister Limitation**
  - **VCC,VCI,GND < 50 ohm**
  - **VDD,VG,VM,V0,XV0,VOUT1,VOUT2 C11P/M,C21P~C26P,C21M~C26M,C31P/M < 100 ohm**
  - **RSTB < 10K ohm**
  - **Other < 1K ohm**

4. Power System ITO routing example



- **Please make sure the “VCC” , “GND” , “VCI” main power ITO resistance as small as possible.**

CAUTIONS:

1.This Specification will be subjected to modify without notice.

2.Precutions on Light:

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light ,therefore ,can potentially lead to its malfunctioning.

2.1Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation .

2.2Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

2.3The IC must be shielded from light in the front , back and side faces.

3.ESD control and prevention:

3.1Humidity Control:30~70% relative humidity is recommended.

3.2To reduce the risk of ESD, all equipment at the wok surface should be properly grounded and all sources of static fields removed.(Example: Station ionizers).

3.3Grounding all personnel who come in contact with parts will eliminate a possible source of ESD. (Example: Wrist straps remove charge from the body and constitute a central part of ESD control).

4.Storage Conditions:

Before open package	After open package
Temp.=25±5℃ Humidity:50~70% Less than 1 Years	Temp.=25±5℃ Humidity:50~70% Less than 3 Months