■ INTERODUCTION

The RW1095 is a driver & controller LSI for 4-level gray scale graphic dot-matrix liquid crystal display systems. It contains 256 segment and 162 common driver circuits(4 pin option for other resolutions).
This chip is connected directly to a microprocessor, accepts 4-line/3-line serial interface(SPI) or 8-bit parallel interface or IIC serial interface, display data can stores in an on-chip display data RAM of 160 x 320 x 2 bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits to drive liquid crystal, it is possible to make a display system with the fewest components.

■ FEATURES

Single chip LCD controller/driver for 4 GRAY SCALE STN LCD

4-level (White, Light Gray, Dark Gray, Black) Gray Scale Display with PWM

DDRAM data [2n: 2n+1]	00	01	10	11
Gray scale	White	Light gray	Dark gray	Dark

Driver Output Circuits:

-256 segment outputs/ 161 common outputs
-256 segment outputs/ 129 common outputs
-256 segment outputs/ 105 common outputs
-320 segment outputs/ 81 common outputs
-320 segment outputs/ 65 common outputs
-320 segment outputs/ 49 common outputs
-320 segment outputs/ 33 common outputs
-320 segment outputs/ 17 common outputs
-320 segment outputs/ 9 common outputs
-320 segment outputs/ 5 common outputs
-320 segment outputs/ 4 common outputs
-320 segment outputs/ 1 common outputs

Microprocessor Interface

- 8 bit parallel bi-directional interface with 6800 or 8080 series.
- 3/4-line SPI (serial peripheral interface) available (only support write operation)
- IIC serial interface (only support write operation)

On-chip Display Data Ram

- Capacity: 160 X 320 X 2 =102400 bits

-Logic power supply: VDD-VSS=1.8V to 3.6V
-Booster reference voltage: VDD2-VSS=2.4V to 3.6V
-Booster maximum voltage limited VOUT=18.0V
-Liquid crystal drive power supply:V0-VSS= 3.3V to 17.1V

Wide range of operating temperatures:
-40 to + 85 degree

On-Chip Low Power Analog Circuit

- Generation of LCD supply voltage (external VOUT voltage supply is possible).
- Generation of intermediate LCD bias voltages.
- Oscillator requires no external components (external clock also possible).
- Voltage converter (X2, X3 ,X4 ,X5 ,X6 ,X7).
- Voltage regulator.
- Voltage follower.
- On-chip electronic contrast control function (128 steps).
- Adjustment frame frequency is available highest possible frame frequency is 200Hz.

RW1095 Revision History		
Version	**Date**	**Description**
0.0	2013/8/7	First Edition
0.1	2014/9/22	Change name of pad 84 and pad 85 to VSS2. Add I/O pin ito resistance limitation Modify inductor type switching regulator circuit. Modify the range table of internal resistance ratio. The range of Internal ratio is from 2.6 to 8.3. Modify absolute maximum rating. Add standard circuit for all duty. Add frame frequency adjustment instruction. Change name of “extra instruction” to inductor regulator circuit on/off
0.2	2015/7/01	Modify logic power supply form 1.8V~3.6V. Add voltage converter circuits. P24~26 Add detail explanation for SPI interface P.42 modify default status after reset.
0.3	2016/1/12	Update Static stander circuit to version B Modify P.7 P.9 CLL and A0 Description

■ Pad Arrangement (COG)

Chip Size: 12766 um X 985 um

Bump Pitch:

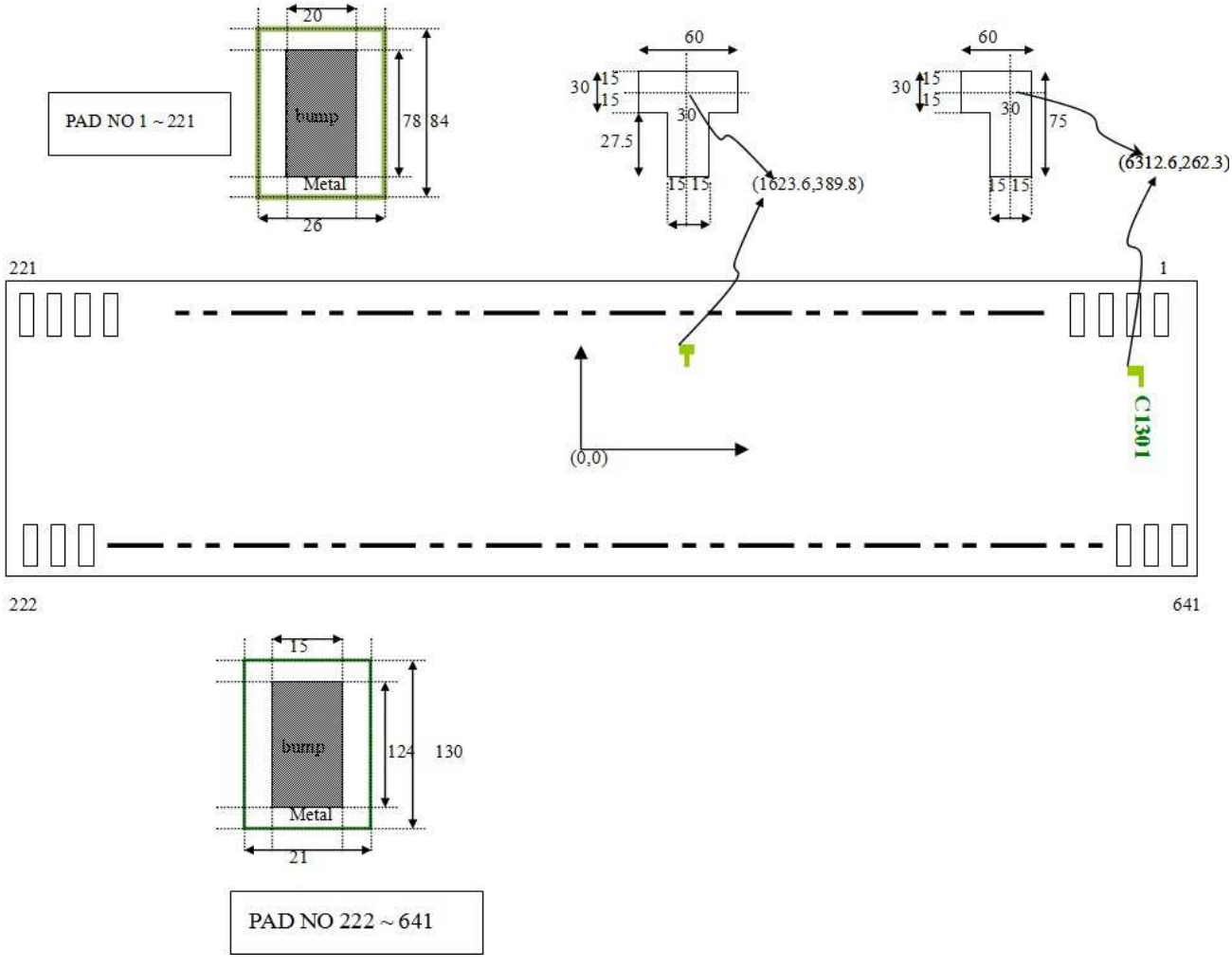
PAD NO.	Pitch	PAD NO.	Pitch	PAD NO.	Pitch
1~21	40 um	80~81	890 um	154~155	44.8 um
21~54	80 um (dummy)	81~139	40 um (I/O)	155~162	40.3 um
54~55	93.1 um	139~140	44 um (I/O)	162~163	44.9 um
55~74	40 um (analog)	140~152	40 um (I/O)	163~201	80 um (dummy)
74~75	42 um	152~153	44 um (I/O)	201~221	40 um
75~80	40 um (analog)	153~154	40.2 um (I/O)	222~641	30 um (com/seg)

Bump Size:

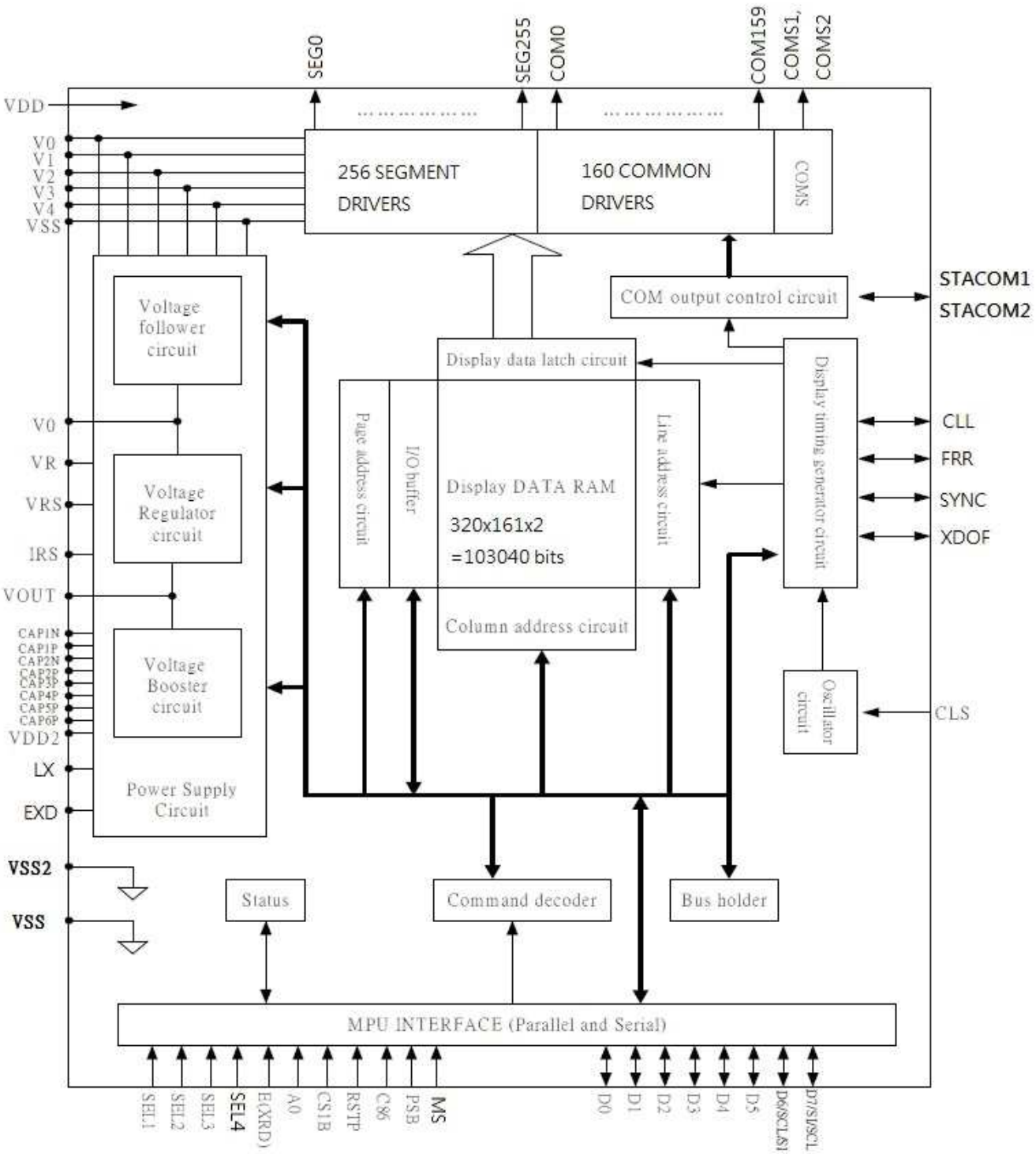
PAD NO. 1~221: 20(x) um X 78(y) um

PAD NO. 222~641: 15(x) um X 124(y) um

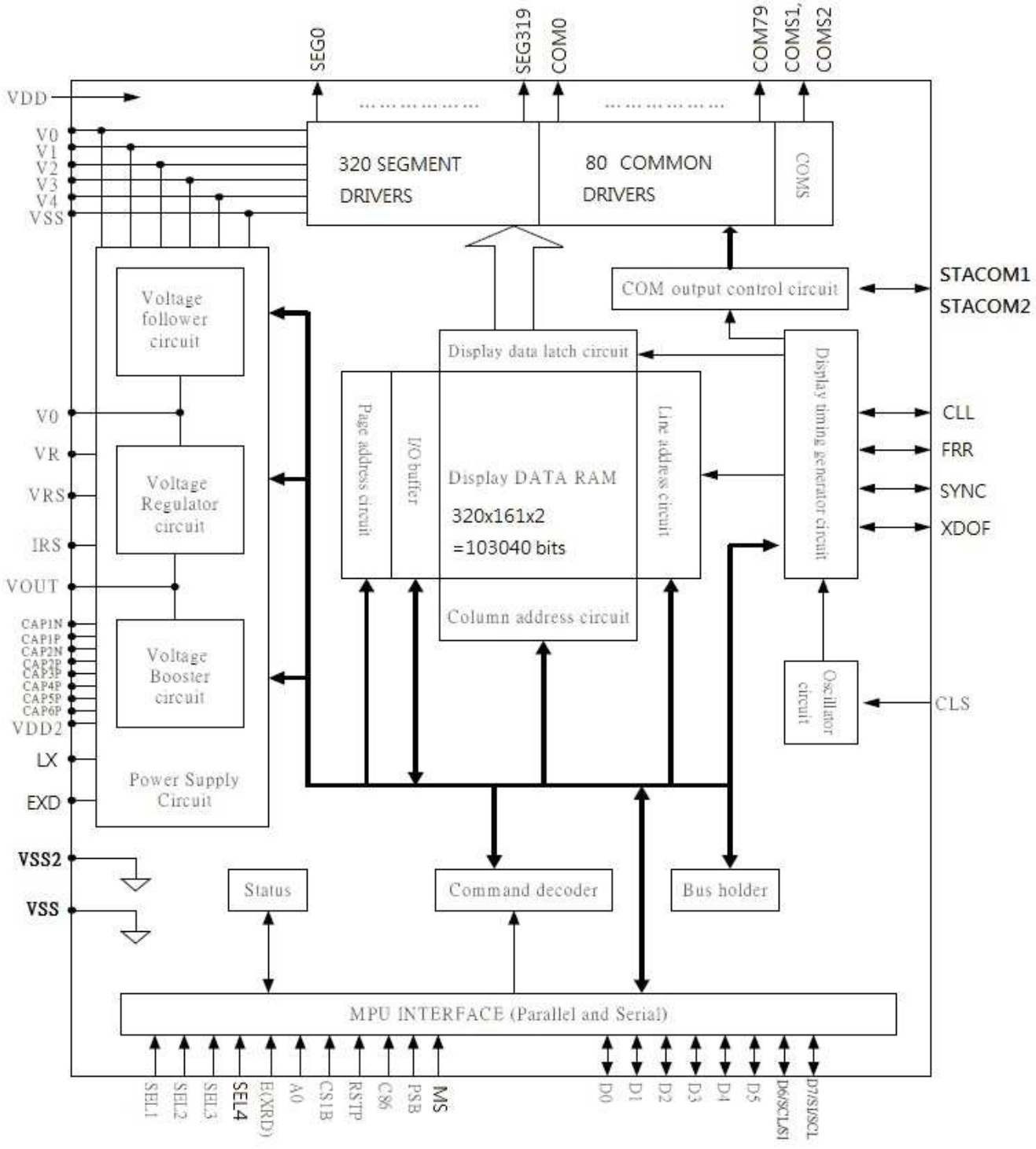
Bump Height: 15 um (Typ) **Chip Thickness: 500 um**



■ BLOCK DIAGRAM for duty 161, 129, 105



■ BLOCK DIAGRAM for duty 81,65,49,33,17,9,5, 4,static



■ PIN DESCRIPTIONS

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">LCD driver outputs</td></tr>
<tr><td>SEG0 to SEG255</td><td>O</td><td>LCD segment driver outputs
This display data and the FRR signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">FRR</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>VLCD</td><td>V_2</td></tr>
<tr><td>H</td><td>L</td><td>V_{SS}</td><td>V_3</td></tr>
<tr><td>L</td><td>H</td><td>V_2</td><td>VLCD</td></tr>
<tr><td>L</td><td>L</td><td>V_3</td><td>V_{SS}</td></tr>
<tr><td colspan="2">Power save mode</td><td>V_{SS}</td><td>V_{SS}</td></tr>
</table></td><td>256</td></tr>
<tr><td>COM0 to COM159</td><td>O</td><td>LCD common driver outputs
This internal scanning data and FRR signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">FRR</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">V_{SS}</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">VLCD</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V_1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V_4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">V_{SS}</td></tr>
</table>
＊COM0~31,COM80~COM111,COMS1 will become segment driver for duty under 81(included).</td><td>160</td></tr>
<tr><td>COMS1, COMS2</td><td>O</td><td>Common output for the icons
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
<tr><td>STACOM1,
STACOM2</td><td>O</td><td>Common output for static drive
The output signals of two pins are same. When not used, this pin should be left open.</td><td>2</td></tr>
</table>

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">LCD Driver Setting pins and signal output pins</td></tr>
<tr><td>PSB</td><td>I</td><td>Microprocessor interface select input pin
PSB= " H ": parallel data input.
PSB= " L ": serial data input. (3-line/4-line serial or IIC serial interface)
When 4-line serial interface is applied, D0 to D5 are fixed to " H ". XRD (E) and XWR(R/W) are fixed to " H ".
When 3-line serial interface is applied, D0 to D5 are fixed to " H ". XRD (E) and XWR(R/W) are fixed to " H ".A0 is fixed to "L"</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>Input mode select
<table>
<tr><th>PSB</th><th>C86</th><th>Interface</th></tr>
<tr><td>" H "</td><td>" H "</td><td>6800-series parallel MPU interface</td></tr>
<tr><td>" H "</td><td>" L "</td><td>8080-series parallel MPU interface</td></tr>
<tr><td>" L "</td><td>" H "</td><td>4 Pin-SPI MPU interface</td></tr>
<tr><td>" L "</td><td>" L "</td><td>IIC serial interface</td></tr>
</table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>The master or slave LSI operation select
M/S= " H ": master mode
M/S= " L ": slave mode
<table>
<tr><th>M/S</th><th>Operating Mode</th><th>FRR</th><th>CLL</th><th>SYNC XDOF</th><th>V0~V4</th><th>Internal OSC</th></tr>
<tr><td>High</td><td>Master</td><td>Output</td><td>See CLS</td><td>Output</td><td>On</td><td>See CLS</td></tr>
<tr><td>Low</td><td>Slave</td><td>Input</td><td>Input</td><td>Input</td><td>On</td><td>Off</td></tr>
</table></td><td>1</td></tr>
<tr><td>CLL</td><td>I/O</td><td>Input/output.
I/O selection
● M/S = "H" & CLS = "H" ：Output
● M/S = "L" & CLS = "L" ：Input

This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges.</td><td>1</td></tr>
<tr><td>FRR</td><td>I/O</td><td>Input/output.
This is the liquid crystal alternating current signal I/O terminal
I/O selection
● M/S = "H"：Output
● M/S = "L"：Input</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Input/output.
This is the synchronization signal for master slave mode
I/O selection
● M/S = "H"：Output
● M/S = "L" : Input</td><td>1</td></tr>
</table>

<table>
<tr><td>XDOF</td><td>I/O</td><td>Input/output.
This is power save control signal for master slave mode I/O selection
● M/S = “H”：Output
● M/S = “L” : Input</td><td>1</td></tr>
<tr><td>CLS</td><td>I</td><td>Oscillator select
When the on-chip oscillator is used, this input must be connected to VDD.
When the external clock input is used, this input must be connected to VSS.
An external clock is connected to CLL pin.</td><td>1</td></tr>
<tr><td>SEL1,
SEL2,
SEL3,
SEL4</td><td>I</td><td>Use these pins can select duty mode:

<table>
<tr><th>SEL4</th><th>SEL3</th><th>SEL2</th><th>SEL1</th><th>Duty Select</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>161 x 256</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>129 x 256</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>105 x 256</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>105 x 160
(KS0719 mode)</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>81 x 320</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>65 x 320</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>49 x320</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>33 x 320</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>17 x 320</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>9 x 320</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>5 x 320</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>4 x 320</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1 x 320 (Static)</td></tr>
</table>
</td><td>4</td></tr>
</table>

RW1095 I/O PIN ITO resistance Limitation

PIN Name	ITO Resister
C86 , PSB ,SEL1,SEL2,SEL3,SEL4 , CLS ,IRS,MSP	No Limitation
VDD, VDD2,VSS,VSS2, VOUT ,V0, VRAB,EXD,LX	<100Ω
V1 , V2 , V3 , V4 , CAP1P , CAP1N , CAP2P , CAP2N , CAP3P , CAP4P , CAP5P,CAP6P	<500Ω
CS1B ,CS2 ,STACOM, E(XRD) , RW(XWR) , A0 , D0~D7,CLL,FRR,SYNC,XDOF	<1KΩ
RSTP	<10KΩ
TEST0…8	Floating

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>No. of Pins</th></tr>
<tr><td colspan="4">System Bus Connection Pins</td></tr>
<tr><td>CS1B,CS2</td><td>I</td><td>Chip select input pins
Data/instruction I/O is enabled only when CS1B is “ L “ and CS2 is “H”.
When chip select is non-active, DB0 to DB7 is high impedance.</td><td>2</td></tr>
<tr><td>RSTP</td><td>I</td><td>Reset input pin
When RSTP is “ L “, initialization is executed.</td><td>1</td></tr>
<tr><td>A0</td><td>I</td><td>It determines whether the data bits are data or a command.
A0=" H “: Indicates that D0 to D7 are display data.
A0=" L “: Indicates that D0 to D7 are control data.
There is no A0 pin in IIC interface, so this pin can fix to ” L”</td><td>1</td></tr>
<tr><td>RW/XWR</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>C86</th><th>MPU type</th><th>XWR (RW)</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read/Write control input pin
RW=" H “: read
RW=" L” : write</td></tr>
<tr><td>L</td><td>8080-series</td><td>XWR</td><td>Write enable clock input pin
The data on D0 to D7 are latched at the rising edge of the RWR signal</td></tr>
</table>
When in the serial interface must fixed to " H ".</td><td>1</td></tr>
<tr><td>E/XRD</td><td>I</td><td>Read/Write execution control pin
<table>
<tr><th>C86</th><th>MPU Type</th><th>E/ XRD</th><th>Description</th></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read/Write control input pin
R/W=" H “: When E is " H ", D0 to D7 are in an output status.
R/W=" L “: The data on D0 to D7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>XRD</td><td>Read enable clock input pin
When XRD is " L ", D0 to D7 are in an output status.</td></tr>
</table>
When in the serial interface must fixed to " H ".</td><td>1</td></tr>
</table>

D5 to D0 D6 (SI) D7 (SCL)	**I/O**	**When the Parallel interface is selected** **(PSB=" H "): 8-bit interface** 8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When chip select is not active, D0 to D7 is high impedance. **When the serial interface is selected** **(PSB="L" & C86="H"):3/4-line SPI Interface** D7: serial input data (SI) D6: serial input clock (SCLK) D5, D4, D3, D2, D1, D0: must fix to "H".. When chip select is not active, D0 to D7 is high impedance. **When the IIC serial interface is selected** **(PSB="L" & C86="L"): IIC Interface** D0 is SA0 D1 is SA1 SA1, SA0 : Is slave address bit1, 0, must fix to "H" or "L". D2,D3 are SDA_OUT D4,D5,D6 are SDA_IN D7 is SCLK SDA_IN: serial input data SDA_OUT: serial data acknowledge output for the I^2C interface. SCL: serial clock input By connecting SDA_OUT to SDA_IN externally, the SDA line becomes fully 2-line interface compatible. Having the acknowledge output separated from the serial data line is advantageous in chip on glass (COG) applications. In COG application where the track resistance from the SDA_OUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the ITO track resistance. It is possible the during the acknowledge cycle the RW1095 will not be able to create a valid logic 0 level. By splitting the SDA_IN input from the SDA_OUT output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDA_OUT pad to the system SDA line to guarantee a valid low level. **All Pad of SDA_IN, SDA_OUT must be connected together (SDA)**	**8**

Power Supply Pins			
VSS	**Power Supply**	Analog Ground. The 2 supply rails VSS and VSS2 must be connected together at the FPC side	**4**
VSS2	**Power Supply**	Digital Ground The 2 supply rails VSS and VSS2 must be connected together at the FPC side	**2**
VDD	**Power Supply**	Digital Supply voltage. The 2 supply rails V_{DD} and V_{DD2} could be connected together. If Digital Option pin is high, must be this level.	**4**
VDD2	**Power Supply**	Power supply for DC/DC voltage converter The 2 supply rails V_{DD} and V_{DD2} could be connected together.	**4**
VOUT	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and VSS. If an external supply is used this pin must be left open.	**5**
CAP1P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	**2**
CAP1N	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.	**4**
CAP2P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	**2**
CAP2N	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.	**4**
CAP3P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	**2**
CAP4P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	**2**
CAP5P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.	**2**
CAP6P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.	**2**
V0, V1, V2, V3, V4	**Power Supply**	This is a multi-level power supply for the liquid crystal. VOUT ≥V0 ≥V1≥V2≥V3≥V4≥VSS	**12**
VRS	**Power Supply**	Monitor Voltage Regulator level, must be left open.	**1**
IRS	**I**	This terminal selects the resistors for the V0 voltage level adjustment. IRS = “H”: Use the internal resistors. IRS = “L”: Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider attached to the VRAB terminal	**1**
VRAB	**I**	Output voltage regulator terminal. Provides the voltage between VSS and V0 through a resistive voltage divider. IRS = “L” : the V0 voltage regulator internal resistors are not used . IRS = “H” : the V0 voltage regulator internal resistors are used .	**1**
LX,EXD	**I/O**	Inductor type regulator pins	**2**
Test Pin			
Test0~Test8		To test used. Test0~Test8 must floating	**9**

■ PAD Coordinate

Duty 161 (SHL=0)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	6282.5	440.5	**41**	NC	3882.5	440.5	**81**	VDD	857.4	440.5
2	NC	6242.5	440.5	**42**	NC	3802.5	440.5	**82**	EXD	817.4	440.5
3	NC	6202.5	440.5	**43**	NC	3722.5	440.5	**83**	EXD	777.4	440.5
4	NC	6162.5	440.5	**44**	NC	3642.5	440.5	**84**	VSS2	737.4	440.5
5	NC	6122.5	440.5	**45**	NC	3562.5	440.5	**85**	VSS2	697.4	440.5
6	NC	6082.5	440.5	**46**	NC	3482.5	440.5	**86**	VSS	657.4	440.5
7	NC	6042.5	440.5	**47**	NC	3402.5	440.5	**87**	VSS	617.4	440.5
8	NC	6002.5	440.5	**48**	NC	3322.5	440.5	**88**	VSS	577.4	440.5
9	NC	5962.5	440.5	**49**	NC	3242.5	440.5	**89**	VSS	537.4	440.5
10	NC	5922.5	440.5	**50**	NC	3162.5	440.5	**90**	VDD2	497.4	440.5
11	NC	5882.5	440.5	**51**	NC	3082.5	440.5	**91**	VDD2	457.4	440.5
12	NC	5842.5	440.5	**52**	NC	3002.5	440.5	**92**	VDD2	417.4	440.5
13	NC	5802.5	440.5	**53**	NC	2922.5	440.5	**93**	VDD2	377.4	440.5
14	NC	5762.5	440.5	**54**	NC	2842.5	440.5	**94**	VDD	337.4	440.5
15	NC	5722.5	440.5	**55**	CAP6P	2749.4	440.5	**95**	VDD	297.4	440.5
16	NC	5682.5	440.5	**56**	CAP6P	2709.4	440.5	**96**	VDD	257.4	440.5
17	NC	5642.5	440.5	**57**	CAP2N	2669.4	440.5	**97**	VDD	217.4	440.5
18	NC	5602.5	440.5	**58**	CAP2N	2629.4	440.5	**98**	FRR	177.4	440.5
19	NC	5562.5	440.5	**59**	CAP4P	2589.4	440.5	**99**	CLL	137.4	440.5
20	NC	5522.5	440.5	**60**	CAP4P	2549.4	440.5	**100**	SYNC	97.4	440.5
21	NC	5482.5	440.5	**61**	CAP2N	2509.4	440.5	**101**	XDOF	57.4	440.5
22	NC	5402.5	440.5	**62**	CAP2N	2469.4	440.5	**102**	VSS	17.4	440.5
23	NC	5322.5	440.5	**63**	CAP2P	2429.4	440.5	**103**	CS1BP	-22.6	440.5
24	NC	5242.5	440.5	**64**	CAP2P	2389.4	440.5	**104**	CS2	-62.6	440.5
25	NC	5162.5	440.5	**65**	CAP1P	2349.4	440.5	**105**	VDD	-102.6	440.5
26	NC	5082.5	440.5	**66**	CAP1P	2309.4	440.5	**106**	RSTP	-142.6	440.5
27	NC	5002.5	440.5	**67**	CAP1N	2269.4	440.5	**107**	A0	-182.6	440.5
28	NC	4922.5	440.5	**68**	CAP1N	2229.4	440.5	**108**	VSS	-222.6	440.5
29	NC	4842.5	440.5	**69**	CAP3P	2189.4	440.5	**109**	RW	-262.6	440.5
30	NC	4762.5	440.5	**70**	CAP3P	2149.4	440.5	**110**	E	-302.6	440.5
31	NC	4682.5	440.5	**71**	CAP1N	2109.4	440.5	**111**	VDD	-342.6	440.5
32	NC	4602.5	440.5	**72**	CAP1N	2069.4	440.5	**112**	D0	-382.6	440.5
33	NC	4522.5	440.5	**73**	CAP5P	2029.4	440.5	**113**	D1	-422.6	440.5
34	NC	4442.5	440.5	**74**	CAP5P	1989.4	440.5	**114**	D2	-462.6	440.5
35	NC	4362.5	440.5	**75**	VOUT	1947.4	440.5	**115**	D3	-502.6	440.5
36	NC	4282.5	440.5	**76**	VOUT	1907.4	440.5	**116**	D4	-542.6	440.5
37	NC	4202.5	440.5	**77**	VOUT	1867.4	440.5	**117**	D5	-582.6	440.5
38	NC	4122.5	440.5	**78**	VOUT	1827.4	440.5	**118**	D6	-622.6	440.5
39	NC	4042.5	440.5	**79**	VOUT	1787.4	440.5	**119**	D7	-662.6	440.5
40	NC	3962.5	440.5	**80**	LX	1747.4	440.5	**120**	VSS	-702.7	440.5

Duty 161 (SHL=0)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	M/S	-742.6	440.5	**161**	T[7]	-2357.33	440.5	**201**	NC	-5482.5	440.5
122	CLS	-782.6	440.5	**162**	T[8]	-2397.63	440.5	**202**	NC	-5522.5	440.5
123	VDD	-822.6	440.5	**163**	NC	-2442.5	440.5	**203**	NC	-5562.5	440.5
124	C86	-862.6	440.5	**164**	NC	-2522.5	440.5	**204**	NC	-5602.5	440.5
125	VSS	-902.6	440.5	**165**	NC	-2602.5	440.5	**205**	NC	-5642.5	440.5
126	PSB	-942.6	440.5	**166**	NC	-2682.5	440.5	**206**	NC	-5682.5	440.5
127	VDD	-982.6	440.5	**167**	NC	-2762.5	440.5	**207**	NC	-5722.5	440.5
128	IRS	-1022.6	440.5	**168**	NC	-2842.5	440.5	**208**	NC	-5762.5	440.5
129	VSS	-1062.6	440.5	**169**	NC	-2922.5	440.5	**209**	NC	-5802.5	440.5
130	SEL1	-1102.6	440.5	**170**	NC	-3002.5	440.5	**210**	NC	-5842.5	440.5
131	VDD	-1142.6	440.5	**171**	NC	-3082.5	440.5	**211**	NC	-5882.5	440.5
132	SEL2	-1182.6	440.5	**172**	NC	-3162.5	440.5	**212**	NC	-5922.5	440.5
133	VSS	-1222.6	440.5	**173**	NC	-3242.5	440.5	**213**	NC	-5962.5	440.5
134	SEL3	-1262.6	440.5	**174**	NC	-3322.5	440.5	**214**	NC	-6002.5	440.5
135	VDD	-1302.6	440.5	**175**	NC	-3402.5	440.5	**215**	NC	-6042.5	440.5
136	SEL4	-1342.6	440.5	**176**	NC	-3482.5	440.5	**216**	NC	-6082.5	440.5
137	VSS	-1382.6	440.5	**177**	NC	-3562.5	440.5	**217**	NC	-6122.5	440.5
138	VRS	-1422.6	440.5	**178**	NC	-3642.5	440.5	**218**	NC	-6162.5	440.5
139	VDD2	-1462.6	440.5	**179**	NC	-3722.5	440.5	**219**	NC	-6202.5	440.5
140	V4	-1506.6	440.5	**180**	NC	-3802.5	440.5	**220**	NC	-6242.5	440.5
141	V4	-1546.6	440.5	**181**	NC	-3882.5	440.5	**221**	NC	-6282.5	440.5
142	V3	-1586.6	440.5	**182**	NC	-3962.5	440.5	**222**	NC	-6285	-418.5
143	V3	-1626.6	440.5	**183**	NC	-4042.5	440.5	**223**	**COM[79]**	-6255	-418.5
144	V2	-1666.6	440.5	**184**	NC	-4122.5	440.5	**224**	**COM[78]**	-6225	-418.5
145	V2	-1706.6	440.5	**185**	NC	-4202.5	440.5	**225**	**COM[77]**	-6195	-418.5
146	V1	-1746.6	440.5	**186**	NC	-4282.5	440.5	**226**	**COM[76]**	-6165	-418.5
147	V1	-1786.6	440.5	**187**	NC	-4362.5	440.5	**227**	**COM[75]**	-6135	-418.5
148	V0	-1826.6	440.5	**188**	NC	-4442.5	440.5	**228**	**COM[74]**	-6105	-418.5
149	V0	-1866.6	440.5	**189**	NC	-4522.5	440.5	**229**	**COM[73]**	-6075	-418.5
150	V0	-1906.6	440.5	**190**	NC	-4602.5	440.5	**230**	**COM[72]**	-6045	-418.5
151	V0	-1946.6	440.5	**191**	NC	-4682.5	440.5	**231**	**COM[71]**	-6015	-418.5
152	VRAB	-1986.6	440.5	**192**	NC	-4762.5	440.5	**232**	**COM[70]**	-5985	-418.5
153	VDD	-2030.6	440.5	**193**	NC	-4842.5	440.5	**233**	**COM[69]**	-5955	-418.5
154	T[0]	-2070.7	440.5	**194**	NC	-4922.5	440.5	**234**	**COM[68]**	-5925	-418.5
155	T[1]	-2115.5	440.5	**195**	NC	-5002.5	440.5	**235**	**COM[67]**	-5895	-418.5
156	T[2]	-2155.8	440.5	**196**	NC	-5082.5	440.5	**236**	**COM[66]**	-5865	-418.5
157	T[3]	-2196.1	440.5	**197**	NC	-5162.5	440.5	**237**	**COM[65]**	-5835	-418.5
158	T[4]	-2236.4	440.5	**198**	NC	-5242.5	440.5	**238**	**COM[64]**	-5805	-418.5
159	T[5]	-2276.7	440.5	**199**	NC	-5322.5	440.5	**239**	**COM[63]**	-5775	-418.5
160	T[6]	-2317.0	440.5	**200**	NC	-5402.5	440.5	**240**	**COM[62]**	-5745	-418.5

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Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	**COM[61]**	-5715	-418.5	**281**	**COM[21]**	-4515	-418.5	**321**	SEG[17]	-3315	-418.5
242	**COM[60]**	-5685	-418.5	**282**	**COM[20]**	-4485	-418.5	**322**	SEG[18]	-3285	-418.5
243	**COM[59]**	-5655	-418.5	**283**	**COM[19]**	-4455	-418.5	**323**	SEG[19]	-3255	-418.5
244	**COM[58]**	-5625	-418.5	**284**	**COM[18]**	-4425	-418.5	**324**	SEG[20]	-3225	-418.5
245	**COM[57]**	-5595	-418.5	**285**	**COM[17]**	-4395	-418.5	**325**	SEG[21]	-3195	-418.5
246	**COM[56]**	-5565	-418.5	**286**	**COM[16]**	-4365	-418.5	**326**	SEG[22]	-3165	-418.5
247	**COM[55]**	-5535	-418.5	**287**	**COM[15]**	-4335	-418.5	**327**	SEG[23]	-3135	-418.5
248	**COM[54]**	-5505	-418.5	**288**	**COM[14]**	-4305	-418.5	**328**	SEG[24]	-3105	-418.5
249	**COM[53]**	-5475	-418.5	**289**	**COM[13]**	-4275	-418.5	**329**	SEG[25]	-3075	-418.5
250	**COM[52]**	-5445	-418.5	**290**	**COM[12]**	-4245	-418.5	**330**	SEG[26]	-3045	-418.5
251	**COM[51]**	-5415	-418.5	**291**	**COM[11]**	-4215	-418.5	**331**	SEG[27]	-3015	-418.5
252	**COM[50]**	-5385	-418.5	**292**	**COM[10]**	-4185	-418.5	**332**	SEG[28]	-2985	-418.5
253	**COM[49]**	-5355	-418.5	**293**	**COM[9]**	-4155	-418.5	**333**	SEG[29]	-2955	-418.5
254	**COM[48]**	-5325	-418.5	**294**	**COM[8]**	-4125	-418.5	**334**	SEG[30]	-2925	-418.5
255	**COM[47]**	-5295	-418.5	**295**	**COM[7]**	-4095	-418.5	**335**	SEG[31]	-2895	-418.5
256	**COM[46]**	-5265	-418.5	**296**	**COM[6]**	-4065	-418.5	**336**	SEG[32]	-2865	-418.5
257	**COM[45]**	-5235	-418.5	**297**	**COM[5]**	-4035	-418.5	**337**	SEG[33]	-2835	-418.5
258	**COM[44]**	-5205	-418.5	**298**	**COM[4]**	-4005	-418.5	**338**	SEG[34]	-2805	-418.5
259	**COM[43]**	-5175	-418.5	**299**	**COM[3]**	-3975	-418.5	**339**	SEG[35]	-2775	-418.5
260	**COM[42]**	-5145	-418.5	**300**	**COM[2]**	-3945	-418.5	**340**	SEG[36]	-2745	-418.5
261	**COM[41]**	-5115	-418.5	**301**	**COM[1]**	-3915	-418.5	**341**	SEG[37]	-2715	-418.5
262	**COM[40]**	-5085	-418.5	**302**	**COM[0]**	-3885	-418.5	**342**	SEG[38]	-2685	-418.5
263	**COM[39]**	-5055	-418.5	**303**	**COMS1**	-3855	-418.5	**343**	SEG[39]	-2655	-418.5
264	**COM[38]**	-5025	-418.5	**304**	SEG[0]	-3825	-418.5	**344**	SEG[40]	-2625	-418.5
265	**COM[37]**	-4995	-418.5	**305**	SEG[1]	-3795	-418.5	**345**	SEG[41]	-2595	-418.5
266	**COM[36]**	-4965	-418.5	**306**	SEG[2]	-3765	-418.5	**346**	SEG[42]	-2565	-418.5
267	**COM[35]**	-4935	-418.5	**307**	SEG[3]	-3735	-418.5	**347**	SEG[43]	-2535	-418.5
268	**COM[34]**	-4905	-418.5	**308**	SEG[4]	-3705	-418.5	**348**	SEG[44]	-2505	-418.5
269	**COM[33]**	-4875	-418.5	**309**	SEG[5]	-3675	-418.5	**349**	SEG[45]	-2475	-418.5
270	**COM[32]**	-4845	-418.5	**310**	SEG[6]	-3645	-418.5	**350**	SEG[46]	-2445	-418.5
271	**COM[31]**	-4815	-418.5	**311**	SEG[7]	-3615	-418.5	**351**	SEG[47]	-2415	-418.5
272	**COM[30]**	-4785	-418.5	**312**	SEG[8]	-3585	-418.5	**352**	SEG[48]	-2385	-418.5
273	**COM[29]**	-4755	-418.5	**313**	SEG[9]	-3555	-418.5	**353**	SEG[49]	-2355	-418.5
274	**COM[28]**	-4725	-418.5	**314**	SEG[10]	-3525	-418.5	**354**	SEG[50]	-2325	-418.5
275	**COM[27]**	-4695	-418.5	**315**	SEG[11]	-3495	-418.5	**355**	SEG[51]	-2295	-418.5
276	**COM[26]**	-4665	-418.5	**316**	SEG[12]	-3465	-418.5	**356**	SEG[52]	-2265	-418.5
277	**COM[25]**	-4635	-418.5	**317**	SEG[13]	-3435	-418.5	**357**	SEG[53]	-2235	-418.5
278	**COM[24]**	-4605	-418.5	**318**	SEG[14]	-3405	-418.5	**358**	SEG[54]	-2205	-418.5
279	**COM[23]**	-4575	-418.5	**319**	SEG[15]	-3375	-418.5	**359**	SEG[55]	-2175	-418.5
280	**COM[22]**	-4545	-418.5	**320**	SEG[16]	-3345	-418.5	**360**	SEG[56]	-2145	-418.5

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Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
361	SEG[57]	-2115	-418.5	**401**	SEG[97]	-915	-418.5	**441**	SEG[137]	285	-418.5
362	SEG[58]	-2085	-418.5	**402**	SEG[98]	-885	-418.5	**442**	SEG[138]	315	-418.5
363	SEG[59]	-2055	-418.5	**403**	SEG[99]	-855	-418.5	**443**	SEG[139]	345	-418.5
364	SEG[60]	-2025	-418.5	**404**	SEG[100]	-825	-418.5	**444**	SEG[140]	375	-418.5
365	SEG[61]	-1995	-418.5	**405**	SEG[101]	-795	-418.5	**445**	SEG[141]	405	-418.5
366	SEG[62]	-1965	-418.5	**406**	SEG[102]	-765	-418.5	**446**	SEG[142]	435	-418.5
367	SEG[63]	-1935	-418.5	**407**	SEG[103]	-735	-418.5	**447**	SEG[143]	465	-418.5
368	SEG[64]	-1905	-418.5	**408**	SEG[104]	-705	-418.5	**448**	SEG[144]	495	-418.5
369	SEG[65]	-1875	-418.5	**409**	SEG[105]	-675	-418.5	**449**	SEG[145]	525	-418.5
370	SEG[66]	-1845	-418.5	**410**	SEG[106]	-645	-418.5	**450**	SEG[146]	555	-418.5
371	SEG[67]	-1815	-418.5	**411**	SEG[107]	-615	-418.5	**451**	SEG[147]	585	-418.5
372	SEG[68]	-1785	-418.5	**412**	SEG[108]	-585	-418.5	**452**	SEG[148]	615	-418.5
373	SEG[69]	-1755	-418.5	**413**	SEG[109]	-555	-418.5	**453**	SEG[149]	645	-418.5
374	SEG[70]	-1725	-418.5	**414**	SEG[110]	-525	-418.5	**454**	SEG[150]	675	-418.5
375	SEG[71]	-1695	-418.5	**415**	SEG[111]	-495	-418.5	**455**	SEG[151]	705	-418.5
376	SEG[72]	-1665	-418.5	**416**	SEG[112]	-465	-418.5	**456**	SEG[152]	735	-418.5
377	SEG[73]	-1635	-418.5	**417**	SEG[113]	-435	-418.5	**457**	SEG[153]	765	-418.5
378	SEG[74]	-1605	-418.5	**418**	SEG[114]	-405	-418.5	**458**	SEG[154]	795	-418.5
379	SEG[75]	-1575	-418.5	**419**	SEG[115]	-375	-418.5	**459**	SEG[155]	825	-418.5
380	SEG[76]	-1545	-418.5	**420**	SEG[116]	-345	-418.5	**460**	SEG[156]	855	-418.5
381	SEG[77]	-1515	-418.5	**421**	SEG[117]	-315	-418.5	**461**	SEG[157]	885	-418.5
382	SEG[78]	-1485	-418.5	**422**	SEG[118]	-285	-418.5	**462**	SEG[158]	915	-418.5
383	SEG[79]	-1455	-418.5	**423**	SEG[119]	-255	-418.5	**463**	SEG[159]	945	-418.5
384	SEG[80]	-1425	-418.5	**424**	SEG[120]	-225	-418.5	**464**	SEG[160]	975	-418.5
385	SEG[81]	-1395	-418.5	**425**	SEG[121]	-195	-418.5	**465**	SEG[161]	1005	-418.5
386	SEG[82]	-1365	-418.5	**426**	SEG[122]	-165	-418.5	**466**	SEG[162]	1035	-418.5
387	SEG[83]	-1335	-418.5	**427**	SEG[123]	-135	-418.5	**467**	SEG[163]	1065	-418.5
388	SEG[84]	-1305	-418.5	**428**	SEG[124]	-105	-418.5	**468**	SEG[164]	1095	-418.5
389	SEG[85]	-1275	-418.5	**429**	SEG[125]	-75	-418.5	**469**	SEG[165]	1125	-418.5
390	SEG[86]	-1245	-418.5	**430**	SEG[126]	-45	-418.5	**470**	SEG[166]	1155	-418.5
391	SEG[87]	-1215	-418.5	**431**	SEG[127]	-15	-418.5	**471**	SEG[167]	1185	-418.5
392	SEG[88]	-1185	-418.5	**432**	SEG[128]	15	-418.5	**472**	SEG[168]	1215	-418.5
393	SEG[89]	-1155	-418.5	**433**	SEG[129]	45	-418.5	**473**	SEG[169]	1245	-418.5
394	SEG[90]	-1125	-418.5	**434**	SEG[130]	75	-418.5	**474**	SEG[170]	1275	-418.5
395	SEG[91]	-1095	-418.5	**435**	SEG[131]	105	-418.5	**475**	SEG[171]	1305	-418.5
396	SEG[92]	-1065	-418.5	**436**	SEG[132]	135	-418.5	**476**	SEG[172]	1335	-418.5
397	SEG[93]	-1035	-418.5	**437**	SEG[133]	165	-418.5	**477**	SEG[173]	1365	-418.5
398	SEG[94]	-1005	-418.5	**438**	SEG[134]	195	-418.5	**478**	SEG[174]	1395	-418.5
399	SEG[95]	-975	-418.5	**439**	SEG[135]	225	-418.5	**479**	SEG[175]	1425	-418.5
400	SEG[96]	-945	-418.5	**440**	SEG[136]	255	-418.5	**480**	SEG[176]	1455	-418.5

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Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
481	SEG[177]	1485	-418.5	**521**	SEG[217]	2685	-418.5	**561**	**COM[81]**	3885	-418.5
482	SEG[178]	1515	-418.5	**522**	SEG[218]	2715	-418.5	**562**	**COM[82]**	3915	-418.5
483	SEG[179]	1545	-418.5	**523**	SEG[219]	2745	-418.5	**563**	**COM[83]**	3945	-418.5
484	SEG[180]	1575	-418.5	**524**	SEG[220]	2775	-418.5	**564**	**COM[84]**	3975	-418.5
485	SEG[181]	1605	-418.5	**525**	SEG[221]	2805	-418.5	**565**	**COM[85]**	4005	-418.5
486	SEG[182]	1635	-418.5	**526**	SEG[222]	2835	-418.5	**566**	**COM[86]**	4035	-418.5
487	SEG[183]	1665	-418.5	**527**	SEG[223]	2865	-418.5	**567**	**COM[87]**	4065	-418.5
488	SEG[184]	1695	-418.5	**528**	SEG[224]	2895	-418.5	**568**	**COM[88]**	4095	-418.5
489	SEG[185]	1725	-418.5	**529**	SEG[225]	2925	-418.5	**569**	**COM[89]**	4125	-418.5
490	SEG[186]	1755	-418.5	**530**	SEG[226]	2955	-418.5	**570**	**COM[90]**	4155	-418.5
491	SEG[187]	1785	-418.5	**531**	SEG[227]	2985	-418.5	**571**	**COM[91]**	4185	-418.5
492	SEG[188]	1815	-418.5	**532**	SEG[228]	3015	-418.5	**572**	**COM[92]**	4215	-418.5
493	SEG[189]	1845	-418.5	**533**	SEG[229]	3045	-418.5	**573**	**COM[93]**	4245	-418.5
494	SEG[190]	1875	-418.5	**534**	SEG[230]	3075	-418.5	**574**	**COM[94]**	4275	-418.5
495	SEG[191]	1905	-418.5	**535**	SEG[231]	3105	-418.5	**575**	**COM[95]**	4305	-418.5
496	SEG[192]	1935	-418.5	**536**	SEG[232]	3135	-418.5	**576**	**COM[96]**	4335	-418.5
497	SEG[193]	1965	-418.5	**537**	SEG[233]	3165	-418.5	**577**	**COM[97]**	4365	-418.5
498	SEG[194]	1995	-418.5	**538**	SEG[234]	3195	-418.5	**578**	**COM[98]**	4395	-418.5
499	SEG[195]	2025	-418.5	**539**	SEG[235]	3225	-418.5	**579**	**COM[99]**	4425	-418.5
500	SEG[196]	2055	-418.5	**540**	SEG[236]	3255	-418.5	**580**	**COM[100]**	4455	-418.5
501	SEG[197]	2085	-418.5	**541**	SEG[237]	3285	-418.5	**581**	**COM[101]**	4485	-418.5
502	SEG[198]	2115	-418.5	**542**	SEG[238]	3315	-418.5	**582**	**COM[102]**	4515	-418.5
503	SEG[199]	2145	-418.5	**543**	SEG[239]	3345	-418.5	**583**	**COM[103]**	4545	-418.5
504	SEG[200]	2175	-418.5	**544**	SEG[240]	3375	-418.5	**584**	**COM[104]**	4575	-418.5
505	SEG[201]	2205	-418.5	**545**	SEG[241]	3405	-418.5	**585**	**COM[105]**	4605	-418.5
506	SEG[202]	2235	-418.5	**546**	SEG[242]	3435	-418.5	**586**	**COM[106]**	4635	-418.5
507	SEG[203]	2265	-418.5	**547**	SEG[243]	3465	-418.5	**587**	**COM[107]**	4665	-418.5
508	SEG[204]	2295	-418.5	**548**	SEG[244]	3495	-418.5	**588**	**COM[108]**	4695	-418.5
509	SEG[205]	2325	-418.5	**549**	SEG[245]	3525	-418.5	**589**	**COM[109]**	4725	-418.5
510	SEG[206]	2355	-418.5	**550**	SEG[246]	3555	-418.5	**590**	**COM[110]**	4755	-418.5
511	SEG[207]	2385	-418.5	**551**	SEG[247]	3585	-418.5	**591**	**COM[111]**	4785	-418.5
512	SEG[208]	2415	-418.5	**552**	SEG[248]	3615	-418.5	**592**	**COM[112]**	4815	-418.5
513	SEG[209]	2445	-418.5	**553**	SEG[249]	3645	-418.5	**593**	**COM[113]**	4845	-418.5
514	SEG[210]	2475	-418.5	**554**	SEG[250]	3675	-418.5	**594**	**COM[114]**	4875	-418.5
515	SEG[211]	2505	-418.5	**555**	SEG[251]	3705	-418.5	**595**	**COM[115]**	4905	-418.5
516	SEG[212]	2535	-418.5	**556**	SEG[252]	3735	-418.5	**596**	**COM[116]**	4935	-418.5
517	SEG[213]	2565	-418.5	**557**	SEG[253]	3765	-418.5	**597**	**COM[117]**	4965	-418.5
518	SEG[214]	2595	-418.5	**558**	SEG[254]	3795	-418.5	**598**	**COM[118]**	4995	-418.5
519	SEG[215]	2625	-418.5	**559**	SEG[255]	3825	-418.5	**599**	**COM[119]**	5025	-418.5
520	SEG[216]	2655	-418.5	**560**	**COM[80]**	3855	-418.5	**600**	**COM[120]**	5055	-418.5

Duty 161 (SHL=0)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
601	**COM[121]**	5085	-418.5	**641**	NC	6285	-418.5				
602	**COM[122]**	5115	-418.5								
603	**COM[123]**	5145	-418.5								
604	**COM[124]**	5175	-418.5								
605	**COM[125]**	5205	-418.5								
606	**COM[126]**	5235	-418.5								
607	**COM[127]**	5265	-418.5								
608	**COM[128]**	5295	-418.5								
609	**COM[129]**	5325	-418.5								
610	**COM[130]**	5355	-418.5								
611	**COM[131]**	5385	-418.5								
612	**COM[132]**	5415	-418.5								
613	**COM[133]**	5445	-418.5								
614	**COM[134]**	5475	-418.5								
615	**COM[135]**	5505	-418.5								
616	**COM[136]**	5535	-418.5								
617	**COM[137]**	5565	-418.5								
618	**COM[138]**	5595	-418.5								
619	**COM[139]**	5625	-418.5								
620	**COM[140]**	5655	-418.5								
621	**COM[141]**	5685	-418.5								
622	**COM[142]**	5715	-418.5								
623	**COM[143]**	5745	-418.5								
624	**COM[144]**	5775	-418.5								
625	**COM[145]**	5805	-418.5								
626	**COM[146]**	5835	-418.5								
627	**COM[147]**	5865	-418.5								
628	**COM[148]**	5895	-418.5								
629	**COM[149]**	5925	-418.5								
630	**COM[150]**	5955	-418.5								
631	**COM[151]**	5985	-418.5								
632	**COM[152]**	6015	-418.5								
633	**COM[153]**	6045	-418.5								
634	**COM[154]**	6075	-418.5								
635	**COM[155]**	6105	-418.5								
636	**COM[156]**	6135	-418.5								
637	**COM[157]**	6165	-418.5								
638	**COM[158]**	6195	-418.5								
639	**COM[159]**	6225	-418.5								
640	**COMS2**	6255	-418.5								

■ PAD Coordinate

Duty 161 (SHL=1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	NC	6282.5	440.5	**41**	NC	3882.5	440.5	**81**	VDD	857.4	440.5
2	NC	6242.5	440.5	**42**	NC	3802.5	440.5	**82**	EXD	817.4	440.5
3	NC	6202.5	440.5	**43**	NC	3722.5	440.5	**83**	EXD	777.4	440.5
4	NC	6162.5	440.5	**44**	NC	3642.5	440.5	**84**	VSS2	737.4	440.5
5	NC	6122.5	440.5	**45**	NC	3562.5	440.5	**85**	VSS2	697.4	440.5
6	NC	6082.5	440.5	**46**	NC	3482.5	440.5	**86**	VSS	657.4	440.5
7	NC	6042.5	440.5	**47**	NC	3402.5	440.5	**87**	VSS	617.4	440.5
8	NC	6002.5	440.5	**48**	NC	3322.5	440.5	**88**	VSS	577.4	440.5
9	NC	5962.5	440.5	**49**	NC	3242.5	440.5	**89**	VSS	537.4	440.5
10	NC	5922.5	440.5	**50**	NC	3162.5	440.5	**90**	VDD2	497.4	440.5
11	NC	5882.5	440.5	**51**	NC	3082.5	440.5	**91**	VDD2	457.4	440.5
12	NC	5842.5	440.5	**52**	NC	3002.5	440.5	**92**	VDD2	417.4	440.5
13	NC	5802.5	440.5	**53**	NC	2922.5	440.5	**93**	VDD2	377.4	440.5
14	NC	5762.5	440.5	**54**	NC	2842.5	440.5	**94**	VDD	337.4	440.5
15	NC	5722.5	440.5	**55**	CAP6P	2749.4	440.5	**95**	VDD	297.4	440.5
16	NC	5682.5	440.5	**56**	CAP6P	2709.4	440.5	**96**	VDD	257.4	440.5
17	NC	5642.5	440.5	**57**	CAP2N	2669.4	440.5	**97**	VDD	217.4	440.5
18	NC	5602.5	440.5	**58**	CAP2N	2629.4	440.5	**98**	FRR	177.4	440.5
19	NC	5562.5	440.5	**59**	CAP4P	2589.4	440.5	**99**	CLL	137.4	440.5
20	NC	5522.5	440.5	**60**	CAP4P	2549.4	440.5	**100**	SYNC	97.4	440.5
21	NC	5482.5	440.5	**61**	CAP2N	2509.4	440.5	**101**	XDOF	57.4	440.5
22	NC	5402.5	440.5	**62**	CAP2N	2469.4	440.5	**102**	VSS	17.4	440.5
23	NC	5322.5	440.5	**63**	CAP2P	2429.4	440.5	**103**	CS1BP	-22.571	440.5
24	NC	5242.5	440.5	**64**	CAP2P	2389.4	440.5	**104**	CS2P	-62.571	440.5
25	NC	5162.5	440.5	**65**	CAP1P	2349.4	440.5	**105**	VDD	-102.571	440.5
26	NC	5082.5	440.5	**66**	CAP1P	2309.4	440.5	**106**	RSTP	-142.571	440.5
27	NC	5002.5	440.5	**67**	CAP1N	2269.4	440.5	**107**	A0	-182.571	440.5
28	NC	4922.5	440.5	**68**	CAP1N	2229.4	440.5	**108**	VSS	-222.571	440.5
29	NC	4842.5	440.5	**69**	CAP3P	2189.4	440.5	**109**	RW	-262.571	440.5
30	NC	4762.5	440.5	**70**	CAP3P	2149.4	440.5	**110**	E	-302.571	440.5
31	NC	4682.5	440.5	**71**	CAP1N	2109.4	440.5	**111**	VDD	-342.571	440.5
32	NC	4602.5	440.5	**72**	CAP1N	2069.4	440.5	**112**	D0	-382.571	440.5
33	NC	4522.5	440.5	**73**	CAP5P	2029.4	440.5	**113**	D1	-422.571	440.5
34	NC	4442.5	440.5	**74**	CAP5P	1989.4	440.5	**114**	D2	-462.571	440.5
35	NC	4362.5	440.5	**75**	VOUT	1947.4	440.5	**115**	D3	-502.571	440.5
36	NC	4282.5	440.5	**76**	VOUT	1907.4	440.5	**116**	D4	-542.571	440.5
37	NC	4202.5	440.5	**77**	VOUT	1867.4	440.5	**117**	D5	-582.571	440.5
38	NC	4122.5	440.5	**78**	VOUT	1827.4	440.5	**118**	D6	-622.571	440.5
39	NC	4042.5	440.5	**79**	VOUT	1787.4	440.5	**119**	D7	-662.571	440.5
40	NC	3962.5	440.5	**80**	LX	1747.4	440.5	**120**	VSS	-702.671	440.5

Duty 161 (SHL=1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
121	M/S	-742.6	440.5	**161**	T[7]	-2357.3	440.5	**201**	NC	-5482.5	440.5
122	CLS	-782.6	440.5	**162**	T[8]	-2397.6	440.5	**202**	NC	-5522.5	440.5
123	VDD	-822.6	440.5	**163**	NC	-2442.5	440.5	**203**	NC	-5562.5	440.5
124	C86	-862.6	440.5	**164**	NC	-2522.5	440.5	**204**	NC	-5602.5	440.5
125	VSS	-902.6	440.5	**165**	NC	-2602.5	440.5	**205**	NC	-5642.5	440.5
126	PSB	-942.6	440.5	**166**	NC	-2682.5	440.5	**206**	NC	-5682.5	440.5
127	VDD	-982.6	440.5	**167**	NC	-2762.5	440.5	**207**	NC	-5722.5	440.5
128	IRS	-1022.6	440.5	**168**	NC	-2842.5	440.5	**208**	NC	-5762.5	440.5
129	VSS	-1062.6	440.5	**169**	NC	-2922.5	440.5	**209**	NC	-5802.5	440.5
130	SEL1	-1102.6	440.5	**170**	NC	-3002.5	440.5	**210**	NC	-5842.5	440.5
131	VDD	-1142.6	440.5	**171**	NC	-3082.5	440.5	**211**	NC	-5882.5	440.5
132	SEL2	-1182.6	440.5	**172**	NC	-3162.5	440.5	**212**	NC	-5922.5	440.5
133	VSS	-1222.6	440.5	**173**	NC	-3242.5	440.5	**213**	NC	-5962.5	440.5
134	SEL3	-1262.6	440.5	**174**	NC	-3322.5	440.5	**214**	NC	-6002.5	440.5
135	VDD	-1302.6	440.5	**175**	NC	-3402.5	440.5	**215**	NC	-6042.5	440.5
136	SEL4	-1342.6	440.5	**176**	NC	-3482.5	440.5	**216**	NC	-6082.5	440.5
137	VSS	-1382.6	440.5	**177**	NC	-3562.5	440.5	**217**	NC	-6122.5	440.5
138	VRS	-1422.6	440.5	**178**	NC	-3642.5	440.5	**218**	NC	-6162.5	440.5
139	VDD2	-1462.6	440.5	**179**	NC	-3722.5	440.5	**219**	NC	-6202.5	440.5
140	V4	-1506.6	440.5	**180**	NC	-3802.5	440.5	**220**	NC	-6242.5	440.5
141	V4	-1546.6	440.5	**181**	NC	-3882.5	440.5	**221**	NC	-6282.5	440.5
142	V3	-1586.6	440.5	**182**	NC	-3962.5	440.5	**222**	NC	-6285	-418.5
143	V3	-1626.6	440.5	**183**	NC	-4042.5	440.5	**223**	**COM[80]**	-6255	-418.5
144	V2	-1666.6	440.5	**184**	NC	-4122.5	440.5	**224**	**COM[81]**	-6225	-418.5
145	V2	-1706.6	440.5	**185**	NC	-4202.5	440.5	**225**	**COM[82]**	-6195	-418.5
146	V1	-1746.6	440.5	**186**	NC	-4282.5	440.5	**226**	**COM[83]**	-6165	-418.5
147	V1	-1786.6	440.5	**187**	NC	-4362.5	440.5	**227**	**COM[84]**	-6135	-418.5
148	V0	-1826.6	440.5	**188**	NC	-4442.5	440.5	**228**	**COM[85]**	-6105	-418.5
149	V0	-1866.6	440.5	**189**	NC	-4522.5	440.5	**229**	**COM[86]**	-6075	-418.5
150	V0	-1906.6	440.5	**190**	NC	-4602.5	440.5	**230**	**COM[87]**	-6045	-418.5
151	V0	-1946.6	440.5	**191**	NC	-4682.5	440.5	**231**	**COM[88]**	-6015	-418.5
152	VRAB	-1986.6	440.5	**192**	NC	-4762.5	440.5	**232**	**COM[89]**	-5985	-418.5
153	VDD	-2030.6	440.5	**193**	NC	-4842.5	440.5	**233**	**COM[90]**	-5955	-418.5
154	T[0]	-2070.7	440.5	**194**	NC	-4922.5	440.5	**234**	**COM[91]**	-5925	-418.5
155	T[1]	-2115.5	440.5	**195**	NC	-5002.5	440.5	**235**	**COM[92]**	-5895	-418.5
156	T[2]	-2155.8	440.5	**196**	NC	-5082.5	440.5	**236**	**COM[93]**	-5865	-418.5
157	T[3]	-2196.1	440.5	**197**	NC	-5162.5	440.5	**237**	**COM[94]**	-5835	-418.5
158	T[4]	-2236.4	440.5	**198**	NC	-5242.5	440.5	**238**	**COM[95]**	-5805	-418.5
159	T[5]	-2276.7	440.5	**199**	NC	-5322.5	440.5	**239**	**COM[96]**	-5775	-418.5
160	T[6]	-2317.0	440.5	**200**	NC	-5402.5	440.5	**240**	**COM[97]**	-5745	-418.5

Duty 161 (SHL=1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
241	COM[98]	-5715	-418.5	281	COM[138]	-4515	-418.5	321	SEG[17]	-3315	-418.5
242	COM[99]	-5685	-418.5	282	COM[139]	-4485	-418.5	322	SEG[18]	-3285	-418.5
243	COM[100]	-5655	-418.5	283	COM[140]	-4455	-418.5	323	SEG[19]	-3255	-418.5
244	COM[101]	-5625	-418.5	284	COM[141]	-4425	-418.5	324	SEG[20]	-3225	-418.5
245	COM[102]	-5595	-418.5	285	COM[142]	-4395	-418.5	325	SEG[21]	-3195	-418.5
246	COM[103]	-5565	-418.5	286	COM[143]	-4365	-418.5	326	SEG[22]	-3165	-418.5
247	COM[104]	-5535	-418.5	287	COM[144]	-4335	-418.5	327	SEG[23]	-3135	-418.5
248	COM[105]	-5505	-418.5	288	COM[145]	-4305	-418.5	328	SEG[24]	-3105	-418.5
249	COM[106]	-5475	-418.5	289	COM[146]	-4275	-418.5	329	SEG[25]	-3075	-418.5
250	COM[107]	-5445	-418.5	290	COM[147]	-4245	-418.5	330	SEG[26]	-3045	-418.5
251	COM[108]	-5415	-418.5	291	COM[148]	-4215	-418.5	331	SEG[27]	-3015	-418.5
252	COM[109]	-5385	-418.5	292	COM[149]	-4185	-418.5	332	SEG[28]	-2985	-418.5
253	COM[110]	-5355	-418.5	293	COM[150]	-4155	-418.5	333	SEG[29]	-2955	-418.5
254	COM[111]	-5325	-418.5	294	COM[151]	-4125	-418.5	334	SEG[30]	-2925	-418.5
255	COM[112]	-5295	-418.5	295	COM[152]	-4095	-418.5	335	SEG[31]	-2895	-418.5
256	COM[113]	-5265	-418.5	296	COM[153]	-4065	-418.5	336	SEG[32]	-2865	-418.5
257	COM[114]	-5235	-418.5	297	COM[154]	-4035	-418.5	337	SEG[33]	-2835	-418.5
258	COM[115]	-5205	-418.5	298	COM[155]	-4005	-418.5	338	SEG[34]	-2805	-418.5
259	COM[116]	-5175	-418.5	299	COM[156]	-3975	-418.5	339	SEG[35]	-2775	-418.5
260	COM[117]	-5145	-418.5	300	COM[157]	-3945	-418.5	340	SEG[36]	-2745	-418.5
261	COM[118]	-5115	-418.5	301	COM[158]	-3915	-418.5	341	SEG[37]	-2715	-418.5
262	COM[119]	-5085	-418.5	302	COM[159]	-3885	-418.5	342	SEG[38]	-2685	-418.5
263	COM[120]	-5055	-418.5	303	COMS1	-3855	-418.5	343	SEG[39]	-2655	-418.5
264	COM[121]	-5025	-418.5	304	SEG[0]	-3825	-418.5	344	SEG[40]	-2625	-418.5
265	COM[122]	-4995	-418.5	305	SEG[1]	-3795	-418.5	345	SEG[41]	-2595	-418.5
266	COM[123]	-4965	-418.5	306	SEG[2]	-3765	-418.5	346	SEG[42]	-2565	-418.5
267	COM[124]	-4935	-418.5	307	SEG[3]	-3735	-418.5	347	SEG[43]	-2535	-418.5
268	COM[125]	-4905	-418.5	308	SEG[4]	-3705	-418.5	348	SEG[44]	-2505	-418.5
269	COM[126]	-4875	-418.5	309	SEG[5]	-3675	-418.5	349	SEG[45]	-2475	-418.5
270	COM[127]	-4845	-418.5	310	SEG[6]	-3645	-418.5	350	SEG[46]	-2445	-418.5
271	COM[128]	-4815	-418.5	311	SEG[7]	-3615	-418.5	351	SEG[47]	-2415	-418.5
272	COM[129]	-4785	-418.5	312	SEG[8]	-3585	-418.5	352	SEG[48]	-2385	-418.5
273	COM[130]	-4755	-418.5	313	SEG[9]	-3555	-418.5	353	SEG[49]	-2355	-418.5
274	COM[131]	-4725	-418.5	314	SEG[10]	-3525	-418.5	354	SEG[50]	-2325	-418.5
275	COM[132]	-4695	-418.5	315	SEG[11]	-3495	-418.5	355	SEG[51]	-2295	-418.5
276	COM[133]	-4665	-418.5	316	SEG[12]	-3465	-418.5	356	SEG[52]	-2265	-418.5
277	COM[134]	-4635	-418.5	317	SEG[13]	-3435	-418.5	357	SEG[53]	-2235	-418.5
278	COM[135]	-4605	-418.5	318	SEG[14]	-3405	-418.5	358	SEG[54]	-2205	-418.5
279	COM[136]	-4575	-418.5	319	SEG[15]	-3375	-418.5	359	SEG[55]	-2175	-418.5
280	COM[137]	-4545	-418.5	320	SEG[16]	-3345	-418.5	360	SEG[56]	-2145	-418.5

Duty 161 (SHL=1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
361	SEG[57]	-2115	-418.5	**401**	SEG[97]	-915	-418.5	**441**	SEG[137]	285	-418.5
362	SEG[58]	-2085	-418.5	**402**	SEG[98]	-885	-418.5	**442**	SEG[138]	315	-418.5
363	SEG[59]	-2055	-418.5	**403**	SEG[99]	-855	-418.5	**443**	SEG[139]	345	-418.5
364	SEG[60]	-2025	-418.5	**404**	SEG[100]	-825	-418.5	**444**	SEG[140]	375	-418.5
365	SEG[61]	-1995	-418.5	**405**	SEG[101]	-795	-418.5	**445**	SEG[141]	405	-418.5
366	SEG[62]	-1965	-418.5	**406**	SEG[102]	-765	-418.5	**446**	SEG[142]	435	-418.5
367	SEG[63]	-1935	-418.5	**407**	SEG[103]	-735	-418.5	**447**	SEG[143]	465	-418.5
368	SEG[64]	-1905	-418.5	**408**	SEG[104]	-705	-418.5	**448**	SEG[144]	495	-418.5
369	SEG[65]	-1875	-418.5	**409**	SEG[105]	-675	-418.5	**449**	SEG[145]	525	-418.5
370	SEG[66]	-1845	-418.5	**410**	SEG[106]	-645	-418.5	**450**	SEG[146]	555	-418.5
371	SEG[67]	-1815	-418.5	**411**	SEG[107]	-615	-418.5	**451**	SEG[147]	585	-418.5
372	SEG[68]	-1785	-418.5	**412**	SEG[108]	-585	-418.5	**452**	SEG[148]	615	-418.5
373	SEG[69]	-1755	-418.5	**413**	SEG[109]	-555	-418.5	**453**	SEG[149]	645	-418.5
374	SEG[70]	-1725	-418.5	**414**	SEG[110]	-525	-418.5	**454**	SEG[150]	675	-418.5
375	SEG[71]	-1695	-418.5	**415**	SEG[111]	-495	-418.5	**455**	SEG[151]	705	-418.5
376	SEG[72]	-1665	-418.5	**416**	SEG[112]	-465	-418.5	**456**	SEG[152]	735	-418.5
377	SEG[73]	-1635	-418.5	**417**	SEG[113]	-435	-418.5	**457**	SEG[153]	765	-418.5
378	SEG[74]	-1605	-418.5	**418**	SEG[114]	-405	-418.5	**458**	SEG[154]	795	-418.5
379	SEG[75]	-1575	-418.5	**419**	SEG[115]	-375	-418.5	**459**	SEG[155]	825	-418.5
380	SEG[76]	-1545	-418.5	**420**	SEG[116]	-345	-418.5	**460**	SEG[156]	855	-418.5
381	SEG[77]	-1515	-418.5	**421**	SEG[117]	-315	-418.5	**461**	SEG[157]	885	-418.5
382	SEG[78]	-1485	-418.5	**422**	SEG[118]	-285	-418.5	**462**	SEG[158]	915	-418.5
383	SEG[79]	-1455	-418.5	**423**	SEG[119]	-255	-418.5	**463**	SEG[159]	945	-418.5
384	SEG[80]	-1425	-418.5	**424**	SEG[120]	-225	-418.5	**464**	SEG[160]	975	-418.5
385	SEG[81]	-1395	-418.5	**425**	SEG[121]	-195	-418.5	**465**	SEG[161]	1005	-418.5
386	SEG[82]	-1365	-418.5	**426**	SEG[122]	-165	-418.5	**466**	SEG[162]	1035	-418.5
387	SEG[83]	-1335	-418.5	**427**	SEG[123]	-135	-418.5	**467**	SEG[163]	1065	-418.5
388	SEG[84]	-1305	-418.5	**428**	SEG[124]	-105	-418.5	**468**	SEG[164]	1095	-418.5
389	SEG[85]	-1275	-418.5	**429**	SEG[125]	-75	-418.5	**469**	SEG[165]	1125	-418.5
390	SEG[86]	-1245	-418.5	**430**	SEG[126]	-45	-418.5	**470**	SEG[166]	1155	-418.5
391	SEG[87]	-1215	-418.5	**431**	SEG[127]	-15	-418.5	**471**	SEG[167]	1185	-418.5
392	SEG[88]	-1185	-418.5	**432**	SEG[128]	15	-418.5	**472**	SEG[168]	1215	-418.5
393	SEG[89]	-1155	-418.5	**433**	SEG[129]	45	-418.5	**473**	SEG[169]	1245	-418.5
394	SEG[90]	-1125	-418.5	**434**	SEG[130]	75	-418.5	**474**	SEG[170]	1275	-418.5
395	SEG[91]	-1095	-418.5	**435**	SEG[131]	105	-418.5	**475**	SEG[171]	1305	-418.5
396	SEG[92]	-1065	-418.5	**436**	SEG[132]	135	-418.5	**476**	SEG[172]	1335	-418.5
397	SEG[93]	-1035	-418.5	**437**	SEG[133]	165	-418.5	**477**	SEG[173]	1365	-418.5
398	SEG[94]	-1005	-418.5	**438**	SEG[134]	195	-418.5	**478**	SEG[174]	1395	-418.5
399	SEG[95]	-975	-418.5	**439**	SEG[135]	225	-418.5	**479**	SEG[175]	1425	-418.5
400	SEG[96]	-945	-418.5	**440**	SEG[136]	255	-418.5	**480**	SEG[176]	1455	-418.5

Duty 161 (SHL=1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
481	SEG[177]	1485	-418.5	**521**	SEG[217]	2685	-418.5	**561**	**COM[78]**	3885	-418.5
482	SEG[178]	1515	-418.5	**522**	SEG[218]	2715	-418.5	**562**	**COM[77]**	3915	-418.5
483	SEG[179]	1545	-418.5	**523**	SEG[219]	2745	-418.5	**563**	**COM[76]**	3945	-418.5
484	SEG[180]	1575	-418.5	**524**	SEG[220]	2775	-418.5	**564**	**COM[75]**	3975	-418.5
485	SEG[181]	1605	-418.5	**525**	SEG[221]	2805	-418.5	**565**	**COM[74]**	4005	-418.5
486	SEG[182]	1635	-418.5	**526**	SEG[222]	2835	-418.5	**566**	**COM[73]**	4035	-418.5
487	SEG[183]	1665	-418.5	**527**	SEG[223]	2865	-418.5	**567**	**COM[72]**	4065	-418.5
488	SEG[184]	1695	-418.5	**528**	SEG[224]	2895	-418.5	**568**	**COM[71]**	4095	-418.5
489	SEG[185]	1725	-418.5	**529**	SEG[225]	2925	-418.5	**569**	**COM[70]**	4125	-418.5
490	SEG[186]	1755	-418.5	**530**	SEG[226]	2955	-418.5	**570**	**COM[69]**	4155	-418.5
491	SEG[187]	1785	-418.5	**531**	SEG[227]	2985	-418.5	**571**	**COM[68]**	4185	-418.5
492	SEG[188]	1815	-418.5	**532**	SEG[228]	3015	-418.5	**572**	**COM[67]**	4215	-418.5
493	SEG[189]	1845	-418.5	**533**	SEG[229]	3045	-418.5	**573**	**COM[66]**	4245	-418.5
494	SEG[190]	1875	-418.5	**534**	SEG[230]	3075	-418.5	**574**	**COM[65]**	4275	-418.5
495	SEG[191]	1905	-418.5	**535**	SEG[231]	3105	-418.5	**575**	**COM[64]**	4305	-418.5
496	SEG[192]	1935	-418.5	**536**	SEG[232]	3135	-418.5	**576**	**COM[63]**	4335	-418.5
497	SEG[193]	1965	-418.5	**537**	SEG[233]	3165	-418.5	**577**	**COM[62]**	4365	-418.5
498	SEG[194]	1995	-418.5	**538**	SEG[234]	3195	-418.5	**578**	**COM[61]**	4395	-418.5
499	SEG[195]	2025	-418.5	**539**	SEG[235]	3225	-418.5	**579**	**COM[60]**	4425	-418.5
500	SEG[196]	2055	-418.5	**540**	SEG[236]	3255	-418.5	**580**	**COM[59]**	4455	-418.5
501	SEG[197]	2085	-418.5	**541**	SEG[237]	3285	-418.5	**581**	**COM[58]**	4485	-418.5
502	SEG[198]	2115	-418.5	**542**	SEG[238]	3315	-418.5	**582**	**COM[57]**	4515	-418.5
503	SEG[199]	2145	-418.5	**543**	SEG[239]	3345	-418.5	**583**	**COM[56]**	4545	-418.5
504	SEG[200]	2175	-418.5	**544**	SEG[240]	3375	-418.5	**584**	**COM[55]**	4575	-418.5
505	SEG[201]	2205	-418.5	**545**	SEG[241]	3405	-418.5	**585**	**COM[54]**	4605	-418.5
506	SEG[202]	2235	-418.5	**546**	SEG[242]	3435	-418.5	**586**	**COM[53]**	4635	-418.5
507	SEG[203]	2265	-418.5	**547**	SEG[243]	3465	-418.5	**587**	**COM[52]**	4665	-418.5
508	SEG[204]	2295	-418.5	**548**	SEG[244]	3495	-418.5	**588**	**COM[51]**	4695	-418.5
509	SEG[205]	2325	-418.5	**549**	SEG[245]	3525	-418.5	**589**	**COM[50]**	4725	-418.5
510	SEG[206]	2355	-418.5	**550**	SEG[246]	3555	-418.5	**590**	**COM[49]**	4755	-418.5
511	SEG[207]	2385	-418.5	**551**	SEG[247]	3585	-418.5	**591**	**COM[48]**	4785	-418.5
512	SEG[208]	2415	-418.5	**552**	SEG[248]	3615	-418.5	**592**	**COM[47]**	4815	-418.5
513	SEG[209]	2445	-418.5	**553**	SEG[249]	3645	-418.5	**593**	**COM[46]**	4845	-418.5
514	SEG[210]	2475	-418.5	**554**	SEG[250]	3675	-418.5	**594**	**COM[45]**	4875	-418.5
515	SEG[211]	2505	-418.5	**555**	SEG[251]	3705	-418.5	**595**	**COM[44]**	4905	-418.5
516	SEG[212]	2535	-418.5	**556**	SEG[252]	3735	-418.5	**596**	**COM[43]**	4935	-418.5
517	SEG[213]	2565	-418.5	**557**	SEG[253]	3765	-418.5	**597**	**COM[42]**	4965	-418.5
518	SEG[214]	2595	-418.5	**558**	SEG[254]	3795	-418.5	**598**	**COM[41]**	4995	-418.5
519	SEG[215]	2625	-418.5	**559**	SEG[255]	3825	-418.5	**599**	**COM[40]**	5025	-418.5
520	SEG[216]	2655	-418.5	**560**	**COM[79]**	3855	-418.5	**600**	**COM[39]**	5055	-418.5

Duty 161 (SHL=1)

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
601	**COM[38]**	5085	-418.5	**641**	NC	6285	-418.5				
602	**COM[37]**	5115	-418.5								
603	**COM[36]**	5145	-418.5								
604	**COM[35]**	5175	-418.5								
605	**COM[34]**	5205	-418.5								
606	**COM[33]**	5235	-418.5								
607	**COM[32]**	5265	-418.5								
608	**COM[31]**	5295	-418.5								
609	**COM[30]**	5325	-418.5								
610	**COM[29]**	5355	-418.5								
611	**COM[28]**	5385	-418.5								
612	**COM[27]**	5415	-418.5								
613	**COM[26]**	5445	-418.5								
614	**COM[25]**	5475	-418.5								
615	**COM[24]**	5505	-418.5								
616	**COM[23]**	5535	-418.5								
617	**COM[22]**	5565	-418.5								
618	**COM[21]**	5595	-418.5								
619	**COM[20]**	5625	-418.5								
620	**COM[19]**	5655	-418.5								
621	**COM[18]**	5685	-418.5								
622	**COM[17]**	5715	-418.5								
623	**COM[16]**	5745	-418.5								
624	**COM[15]**	5775	-418.5								
625	**COM[14]**	5805	-418.5								
626	**COM[13]**	5835	-418.5								
627	**COM[12]**	5865	-418.5								
628	**COM[11]**	5895	-418.5								
629	**COM[10]**	5925	-418.5								
630	**COM[9]**	5955	-418.5								
631	**COM[8]**	5985	-418.5								
632	**COM[7]**	6015	-418.5								
633	**COM[6]**	6045	-418.5								
634	**COM[5]**	6075	-418.5								
635	**COM[4]**	6105	-418.5								
636	**COM[3]**	6135	-418.5								
637	**COM[2]**	6165	-418.5								
638	**COM[1]**	6195	-418.5								
639	**COM[0]**	6225	-418.5								
640	**COMS2**	6255	-418.5								

■ DESCRIPTON OF FUNCTION

◆ The MPU Interface

With the RW1095 chips, data transfers are done through an 8-bit parallel data bus (D7 to D0) or through a serial data input (SI). Through selecting the PSB/ C86 terminal polarity to the “H” or “L” it is possible to select either parallel data input or serial data input as shown in Table 1.

Table 1

Interface	PSB	C86	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
6800	H	H	CS1B	CS2	A0	E	RW	D7	D6	D5~D0
8080	H	L	CS1B	CS2	A0	XRD	XWR	D7	D6	D5~ D0
4SPI	L	H	CS1B	H	A0	H	H	SI	SCLK	H
3SPI	L	H	CS1B	H	L	H	H	SI	SCLK	H
IIC	L	L	H	H	L	H	H	SCL	SDA_IN:D6~D5 SDA_OUT: D3~D2 SA[1:0]: D1~ D0	

“—” indicates fixed to either “H” or to “L”

● The Parallel Interface

When the parallel interface has been selected (PSB=“H”), then it is possible to connect directly to either an 8080-system MPU or a 6800 Series MPU (shown in Table 2) by selecting the C86 terminal to either “H” or to “L”.

Table 2

C86 (PSB=H)	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7~D0
H: 6800 Series	CS1B	CS2	A0	E	RW	D7~D0
L: 8080 Series	CS1B	CS2	A0	XRD	XWR	D7~D0

Moreover, data bus signals are recognized by a combination of A0, XRD (E), XWR (RW) signals, as shown in Table 3.

Table 3

Shared	6800 Series	8080 Series		Function
A0	RW	XRD	XWR	
1	1	0	1	Reads the display data
1	0	1	0	Writes the display data
0	1	0	1	Status read
0	0	1	0	Write control data (command)

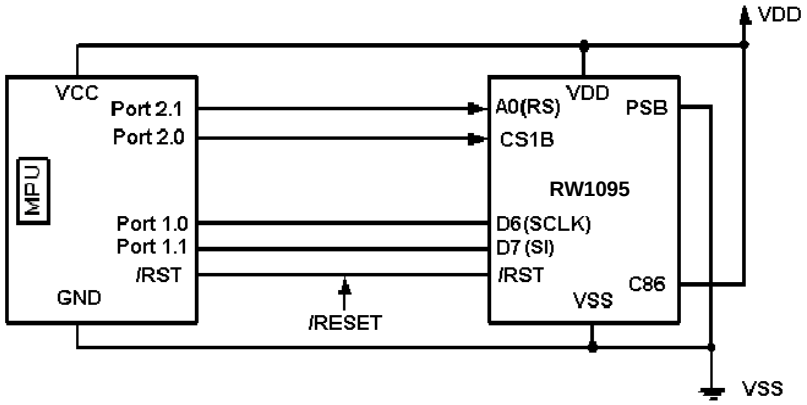
● SPI Interface

When the SPI interface has been selected (PSB="L",C86="H"),then it is possible to connect directly to an MPU through 4 pins serial interface configuration (A0 pin,CS1B pin, SCLK pin, SI pin) or 3 pins serial interface (CS1B pin, SCLK pin , SI pin) configuration . Pins configuration is only difference between 4-SPI and 3-SPI.

Interface	PSB	C86	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
4SPI	L	H	CS1B	H	A0	H	H	SI	SCLK	H
3SPI	L	H	CS1B	H	L	H	H	SI	SCLK	H

The 4-SPI serial interface(PSB="L",C86="H")

When 4 pins serial interface configuration is used,A0 is used to realize incoming data is instruction/display data.
A0 must be a certain state("L" or "H") when chip is in active mode(CS1B="L", and CS2="H").A0 can not be kept tri-state or floating when chip is in active mode. It should be fine if A0 is low while power up.



The 4-SPI example of timing sequence is shown below Figure 1,

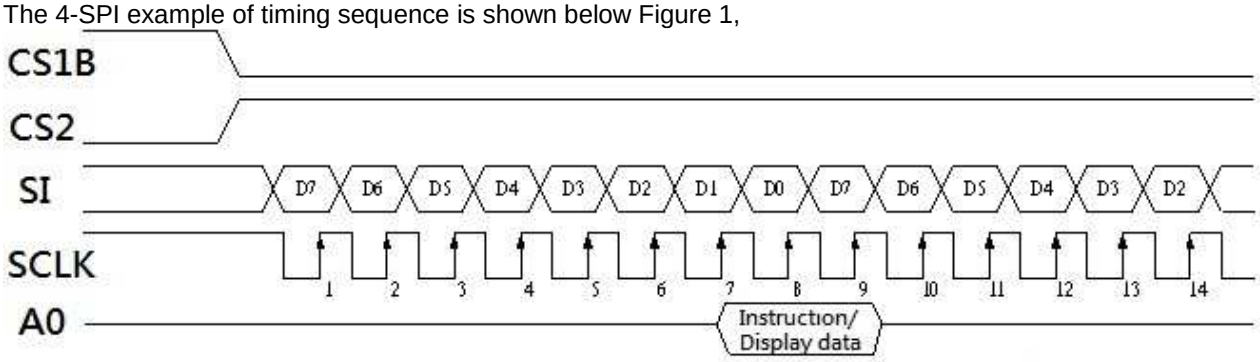


Figure 1

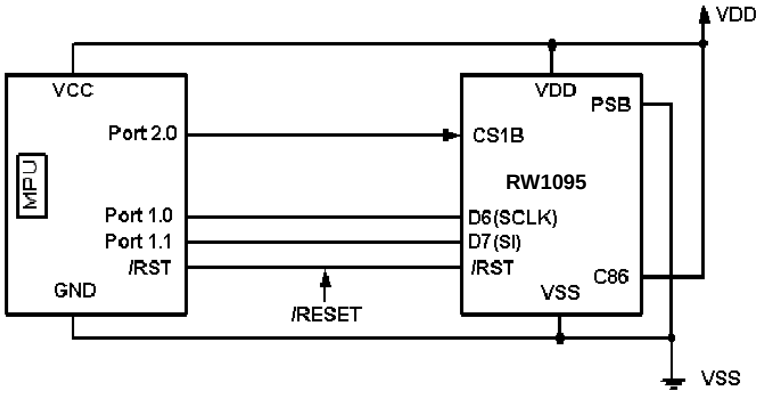
The 3-SPI serial interface(PSB="L",C86="H")

When 3 pins serial interface configuration is used , A0 must be kept "L" or connected to VSS.

Data length instruction is used to realize incoming data is instruction/display data .IC will recognize the incoming data that after "Set Data length for 3-SPI instruction " as display data.

User must set data length of the incoming data that after Data length instruction .

Interface	PSB	C86	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
4SPI	L	H	CS1B	H	A0	H	H	SI	SCLK	H
3SPI	L	H	CS1B	H	L	H	H	SI	SCLK	H



The 3-SPI example of timing sequence is shown below figure2, data length instruction is followed by Display data set.

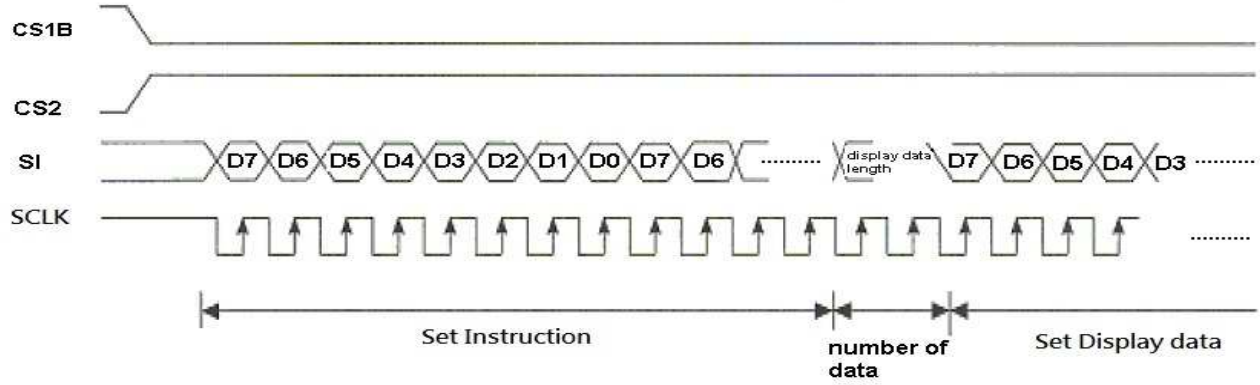


Figure 2

* When the chip is not active, the shift registers and the counter are reset to their initial states.
* Reading is not possible while in serial interface mode.
* Caution is required on the SCLK signal when it comes to line-end reflections and external noise. We recommend that operation be rechecked on the actual equipment.

● IIC Interface(PSB="L", C86="L")

The IIC interface receives and executes the commands sent via the IIC Interface. It also receives RAM data and sends it to the RAM.
The IIC Interface is for bi-directional, two-line communication between different ICs or modules.

The two lines are a Serial Data line SDA and a Serial Clock line SCL. Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

➢ BIT Transfer

One data bit is transferred during each clock pulse. The data on the SDA(DB6) line must remain stable during the HIGH period of the clock pulse because changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 4.

➢ START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 5.

➢ SYSTEM CONFIGURATION

The system configuration is illustrated in Figure 6.
· Transmitter: the device, which sends the data to the bus.
· Receiver: the device, which receives the data from the bus.
· Master: the device, which initiates a transfer, generates clock signals and terminates a transfer.
· Slave: the device addressed by a master.
· Multi-Master: more than one master can attempt to control the bus at the same time without corrupting the message.
· Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.
· Synchronization: procedure to synchronize the clock signals of two or more devices.

➢ ACKNOWLEDGE

Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. A master receiver must also generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition. Acknowledgement on the IIC Interface is illustrated in Figure 7.

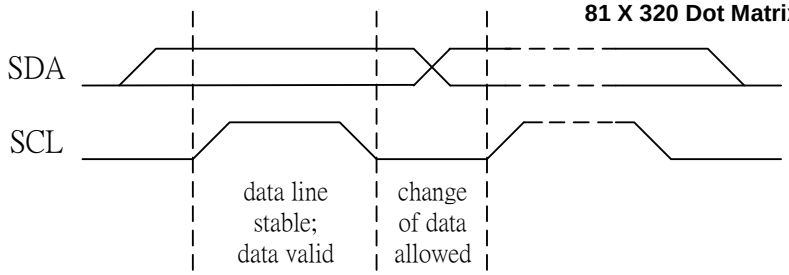


Figure 4 Bit transfer

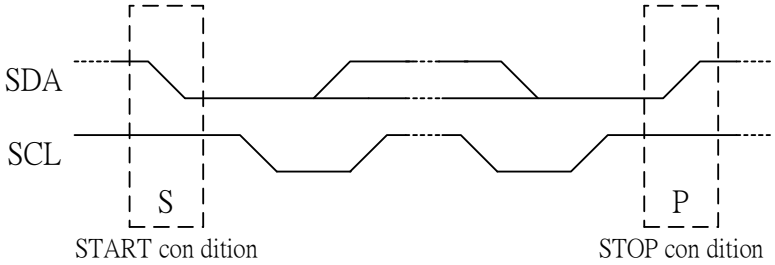


Figure 5 Definition of START and STOP conditions

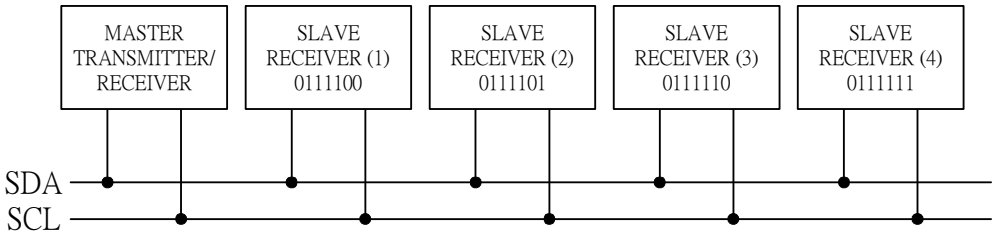


Figure 6 System configuration

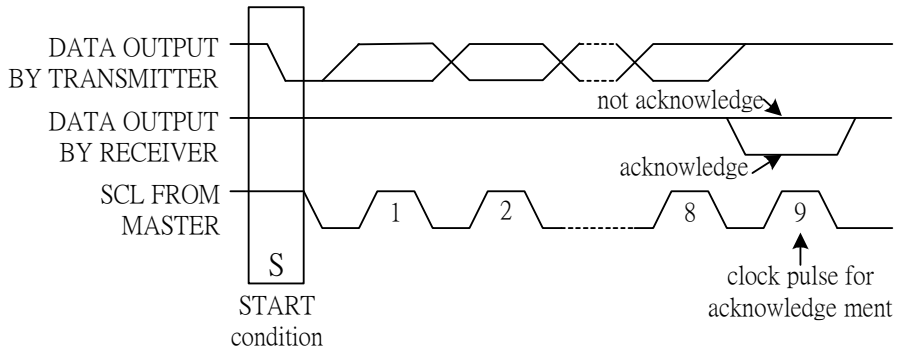


Figure 7 Acknowledgement on the 2-line Interface

➢ IIC Interface Protocol

The RW1095 supports command, data write addressed slaves on the bus.
Before any data is transmitted on the IIC Interface, the device, which should respond, is addressed first. Four 7-bit slave addresses (0111100, 0111101, 0111110 and 0111111) are reserved for the RW1095.
The least significant bit of the slave address is set by connecting the input SA0 and SA1 to either logic 0 (VSS) or logic 1 (VDD).
The IIC Interface protocol is illustrated in Figure 8.

The sequence is initiated with a START condition (S) from the IIC Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the IIC Interface transfer. After acknowledgement, one or more command words follow which define the status of the addressed slaves.
A command word consists of a control byte, which defines Co and A0, plus a data byte.
The last control byte is tagged with a cleared most significant bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data bytes will follow. The state of the A0 bit defines whether the data byte is interpreted as a command or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, depending on the A0 bit setting; either a series of display data bytes or command data bytes may follow. If the A0 bit is set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended RW1095 device. If the A0 bit of the last control byte is set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the IIC INTERFACE-bus master issues a STOP condition (P).

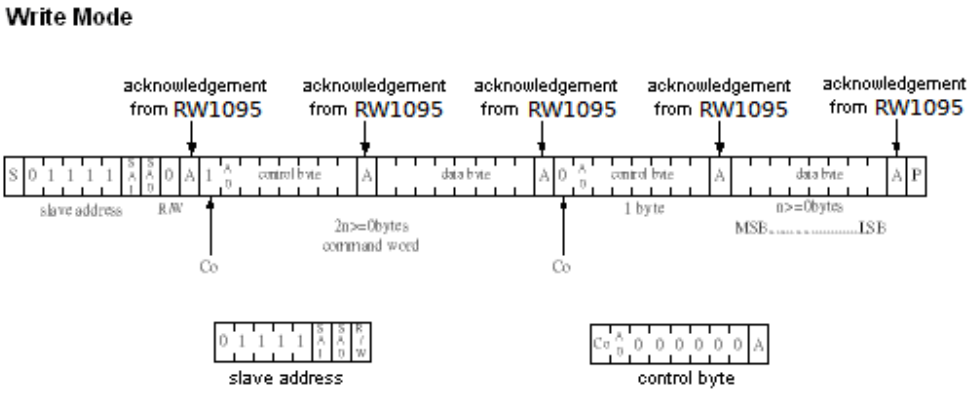


Figure 8 2-line Interface protocol

Co	0	Last control byte to be sent. Only a stream of data bytes is allowed to follow. This stream may only be terminated by s STOP or RE-START condition.
	1	Another control byte will follow the data byte unless a STOP or RE-START condition is received.

◆ The Chip Select

The RW1095 have two chip select terminals: CS1B and CS2. The MPU interface or the serial interface is enabled only when CS1B = “L” and CS2 = “H”.
When the chip select is inactive, D0 to D7 enter a high impedance state, and the A0, XRD, and XWR inputs are inactive. When the serial interface is selected, the shift register and the counter are reset.

◆ Data Transfer

The RW1095 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 9. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 9-1. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

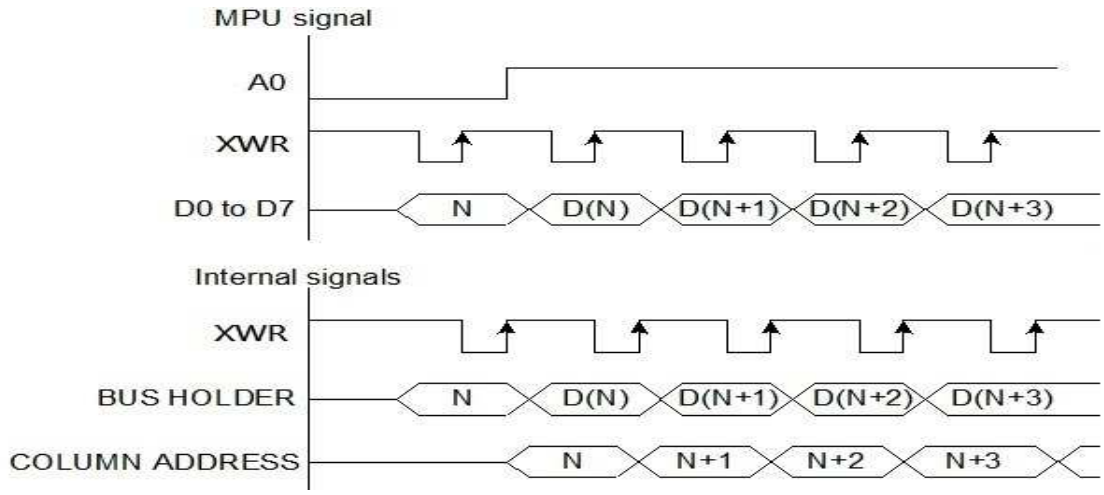


Figure 9. Write Timing

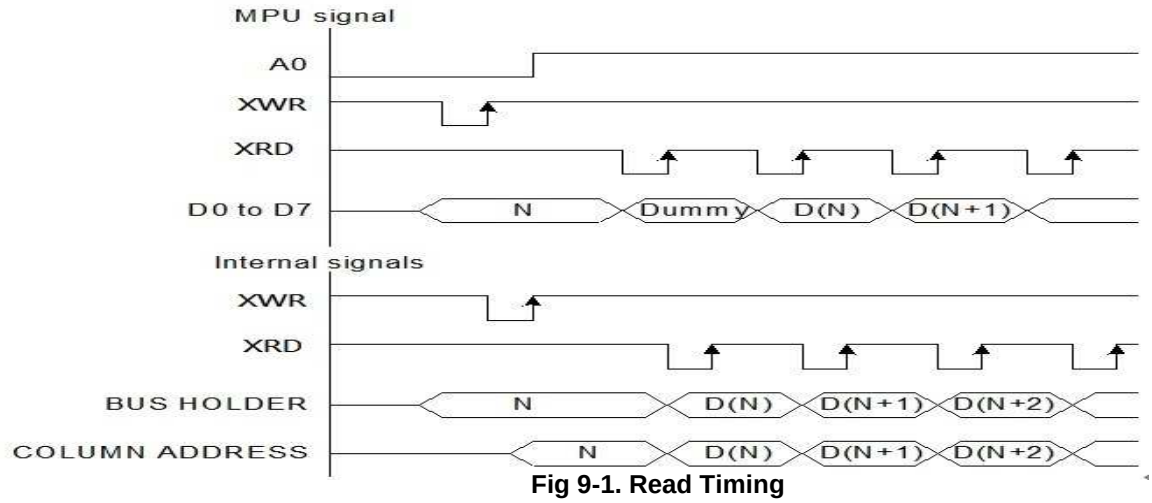


Fig 9-1. Read Timing

◆ The Busy Flag

The Busy Flag indicates whether the RW1095 is operating or not. When D7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

◆ Display Data RAM

The RW1095 contains 161X320X2 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. It has a 161(20pageX8 bit +1 pageX1 bit) X320 X2. There is a direct correspondence between X-address and column output number. It is 161-row by 320-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 161 rows are divided into 8 pages of 8 lines (0~159 COM) and the last page with a single line (D0 only)(161 row—COMS (ICON)). Data is read from or written to the 8 lines of each page directly through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

◆ The Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 14. It incorporates 5-bit Page Address register changed by only the “Set Page address” instruction. Page Address 31 is a special RAM area for the Icons(COMS) and display data D0 is only valid.

◆ The Line Address Circuit

This circuit assigns DDRAM a Line Address corresponding to the first line (COM0) of the display. Therefore, by setting Line Address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 14. It incorporates 9-bit Line Address register changed by only the initial display line instruction and 9-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the line address for transferring the 102-bit RAM data to the display data latch circuit. When icon is selected by setting icon page address, display data of icons are not scrolled because the MPU cannot access Line Address of icons.

◆ The Column Address Circuit

Column Address Circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 11 figure 11-1 . The display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read/write command. This allows the MPU display data to be accessed continuously.

Register ADC and SHL selection instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 10.

SEG Output

SEG Output ADC	SEG0 SEG255/SEG319
"0" (duty 161,129,105)	Seg0 → Segment Address → Seg255
"0" (duty under 81)	Seg0 → Segment Address → Seg319
"1" (duty 161,129,105)	Seg255 ← Segment Address ← Seg0
"1" (duty under 81)	Seg319 ← Segment Address ← Seg0

COM Output

COM Output SHL	Com0 Com159	Coms (ICON)
0"	Com0 → Common Address → ComN	Coms
"1"	ComN ← Common Address ← Com0	Coms

＊Please refer to Appendix table for details

Figure .10 ADC and SHL Select Instruction

SEG output	SEG 0		SEG 1		SEG 2		SEG 3		…	SEG 252		SEG 253		SEG 254		SEG 255	
Column address	00H		01H		02H		03H		…	FCH		FDH		FEH		FFH	
Internal column address	00 HEX	01 HEX	02 HEX	03 HEX	04 HEX	05 HEX	06 HEX	07 HEX	…	1F8 HEX	1F9 HEX	1FA HEX	1FB HEX	1FC HEX	1FD HEX	1FE HEX	1FF HEX
Display data (ADC=0)	1	1	1	0	0	0	0	1	…	1	0	1	1	0	0	0	1
LCD panel display									…								
Display data (ADC=1)	0	1	0	0	1	1	1	0	…	0	1	0	0	1	0	1	1
LCD panel display									…								

Figure 11.The Relationship between the Column Address and The Segment Outputs for duty 161,129,105

SEG output	SEG 0		SEG 1		SEG 2		SEG 3		…	SEG 316		SEG 317		SEG 318		SEG 319	
Column address	00H		01H		02H		03H		…	13CH		13DH		13EH		13FH	
Internal column address	00 HEX	01 HEX	02 HEX	03 HEX	04 HEX	05 HEX	06 HEX	07 HEX	…	277 HEX	278D HEX	279 HEX	27A HEX	27B HEX	27C HEX	27D HEX	27E HEX
Display data (MX=0)	1	1	1	0	0	0	0	1	…	1	0	1	1	0	0	0	1
LCD panel display									…								
Display data (MX=1)	0	1	0	0	1	1	1	0	…	0	1	0	0	1	0	1	1
LCD panel display									…								

Figure .11-1.The Relationship between the Column Address and The Segment Outputs for duty under 81(included)

◆ RAM FORMAT ADDRESSING

Data is downloaded in bytes into the RAM matrix of RW1095 as indicated in Figs.12, 13. The display RAM has a matrix of 161 by 320 × 2 bits. The address pointer addresses the columns. Column address increments after each byte (see Fig.11).

After the last X address.

After the very last address (X = 255 or 319) the address pointers wrap around to address (X = 0)

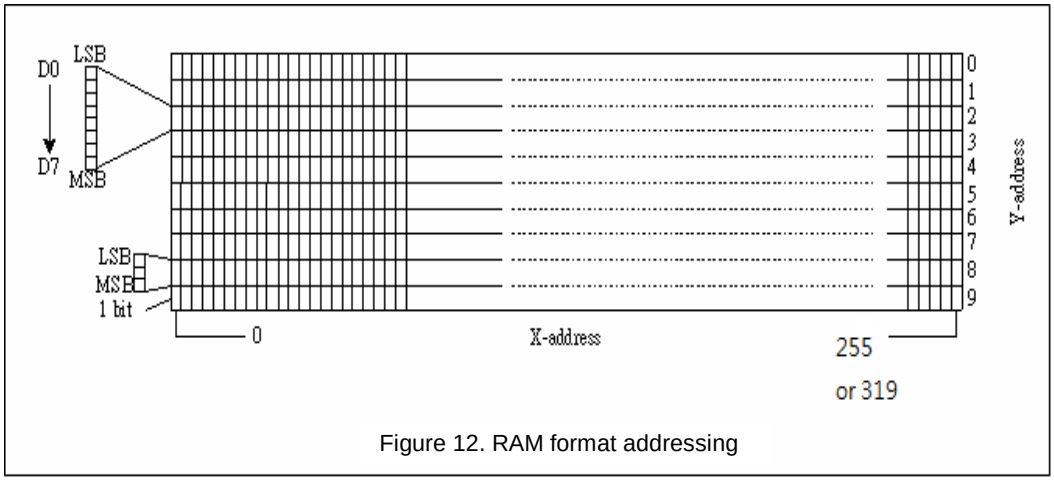


Figure 12. RAM format addressing

0	1	2			0
256	257	258			1
512	513	514			2
768	769	770			3
768	769	770			4
768	769	770			5
768	769	770			6
768	769	770			7
768	769	770			8
768	769	770			9
				5119	19
0----------				255 or 319	

Fig.13 sequence of writing data bytes into RAM with horizontal addressing

Display Data RAM MAP

P4	P3	P2	P1	P0																		
0	0	0	0	0	D0	■	■	■	■	■	■						Page0						00H		COM0
					D1	■	■				■												01H		COM1
					D2	■	■				■												02H		COM2
					D3	■	■	■	■	■	■												03H		COM3
					D4	■	■		■														04H		COM4
					D5	■	■			■													05H		COM5
					D6	■	■				■												06H		COM6
					D7																		07H		COM7
0	0	0	0	1	D0		■	■	■	■	■						Page1						08H		COM8
					D1	■	■				■												09H		COM9
					D2	■	■				■												0AH		COM10
					D3	■	■				■												0BH		COM11
					D4	■	■				■												0CH		COM12
					D5	■	■				■												0DH		COM13
					D6		■	■	■	■	■												0EH		COM14
					D7																		0FH		COM15
⋮																									
1	0	0	1	1	D0	■	■				■						Page19						98H		COM152
					D1	■	■			■													99H		COM153
					D2	■	■		■														9AH		COM154
					D3	■	■	■															9BH		COM155
					D4	■	■		■														9CH		COM156
					D5	■	■			■													9DH		COM157
					D6	■	■				■												9EH		COM158
					D7																		9FH		COM159
1	1	1	1	1	D0												Page31								COMS1&2

0	1	2	3	4	5	6	7	8	.....	0FB	0FC	0FD	0FE	0FF	0	D0	ADC
0FF	0FE	0FD	0FC	0FB	0FA	0F9	0F8	0F7	.....	4	3	2	1	0	1	D0	(column)
S0	S1	S2	S3	S4	S5	S6	S7	S8	.....	S25	S25	S25	S25	S25	LCD Output		

Fig.14 Line Address Circuit for 160,128,104 duty mode(expect KS0719 mode)

Display Data RAM MAP

P4	P3	P2	P1	P0																
0	0	0	0	0	D0										Page0						00H	COM0
					D1																01H	COM1
					D2																02H	COM2
					D3																03H	COM3
					D4																04H	COM4
					D5																05H	COM5
					D6																06H	COM6
					D7																07H	COM7
0	0	0	0	1	D0										Page1						08H	COM8
					D1																09H	COM9
					D2																0AH	COM10
					D3																0BH	COM11
					D4																0CH	COM12
					D5																0DH	COM13
					D6																0EH	COM14
					D7																0FH	COM15
															⋮							
0	1	0	0	1	D0										Page9						48H	COM72
					D1																49H	COM73
					D2																4AH	COM74
					D3																4BH	COM75
					D4																4CH	COM76
					D5																4DH	COM77
					D6																4EH	COM78
					D7																4FH	COM79
1	1	1	1	1	D0										Page31							COMS1&2

0	1	2	3	4	5	6	7	8	.....	13B	13C	13D	13E	13F	0	D0	ADC
13F	13E	13D	13C	13B	13A	139	138	137		4	3	2	1	0	1	D0	(column)
S0	S1	S2	S3	S4	S5	S6	S7	S8	.....	S31	S31	S31	S31	S31	LCD Output		

Fig.14 Line Address Circuit for 80,64,48,32,16,8,4,3 duty mode

Display Data RAM MAP

P3	P2	P1	P0																		
0	0	0	0	D0	■	■	■	■						Page0						00H	COM0
				D1	■				■											01H	COM1
				D2	■				■											02H	COM2
				D3	■	■	■	■												03H	COM3
				D4	■		■													04H	COM4
				D5	■			■												05H	COM5
				D6	■				■											06H	COM6
				D7																07H	COM7
0	0	0	1	D0		■	■	■						Page1						08H	COM8
				D1	■				■											09H	COM9
				D2	■				■											0AH	COM10
				D3	■				■											0BH	COM11
				D4	■				■											0CH	COM12
				D5	■				■											0DH	COM13
				D6		■	■	■												0EH	COM14
				D7																0FH	COM15
⋮																					
1	1	0	0	D0	■				■					Page12						60H	COM96
				D1	■			■												61H	COM97
				D2	■		■													62H	COM98
				D3	■	■														63H	COM99
				D4	■		■													64H	COM100
				D5	■			■												65H	COM101
				D6	■				■											66H	COM102
				D7																67H	COM103
1	1	1	1	D0										Page31						-	COMS1&2

0	1	2	3	4	5	6	7	8	.....	9B	9C	9D	9E	9F	0	D0	ADC
9F	9E	9D	9C	9B	9A	99	98	97		4	3	2	1	0	1	D0	(column)
S0	S1	S2	S3	S4	S5	S6	S7	S8	.....	S15	S15	S15	S15	S15	LCD Output		

Fig.14 Line Address Circuit for KS0719 mode

◆ LCD DISPLAY CIRCUIT

- Gray Scale Table of 12 PWM (Pulse Width Modulation)

Dec	Hex	4-bits	PWM (on width)	Note
0	00	0000	0(0/12)	Brighter
1	01	0001	1/12	
2	02	0010	2/12	
3	03	0011	3/12	
4	04	0100	4/12	
5	05	0101	5/12	
6	06	0110	6/12	
7	07	0111	7/12	
8	08	1000	8/12	
9	09	1001	9/12	
10	0A	1010	10/12	
11	0B	1011	11/12	
12	0C	1100	1(12/12)	Darker
13	0D	1101	1(12/12)	This area is selected to OFF level (0/12 level)
14	0E	1110	1(12/12)	
15	0F	1111	1(12/12)	

◆ The Oscillator Circuit

The on-chip oscillator provides the clock signal for the display system. No external components are required and the CLS input must be connected to VDD. If used external clock signal, CLS input must be connected to VSS.

◆ Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CLL (internal), generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock and the display data latch circuit latches the 102-bit display data in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (FRR) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame signal or the line signal changes the FRR by setting internal instruction. Driving waveform and internal timing signal are shown in Figure 15.

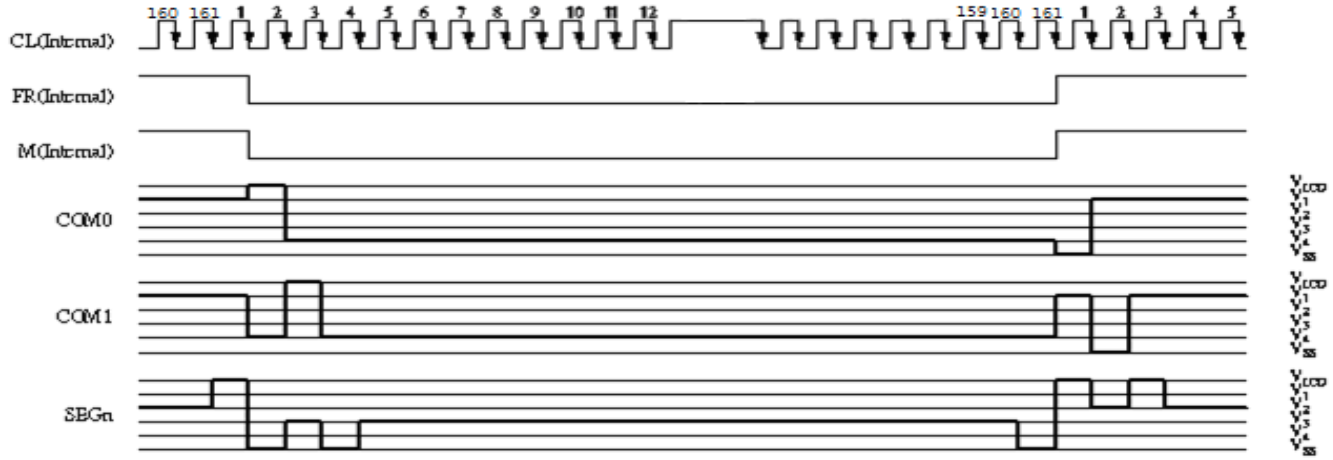


Figure 15 2-frame AC Driving Waveform (Duty Ratio: 1/161)

■ The LCD DRIVER CIRCUIT

These are a 417-channel that generates four voltage levels for driving the LCD .

The combination of the display data, the COM scan signal, and the FRR(M) signal produces the liquid crystal drive voltage output. Figure 16 shows examples of the SEG and COM output waveform.

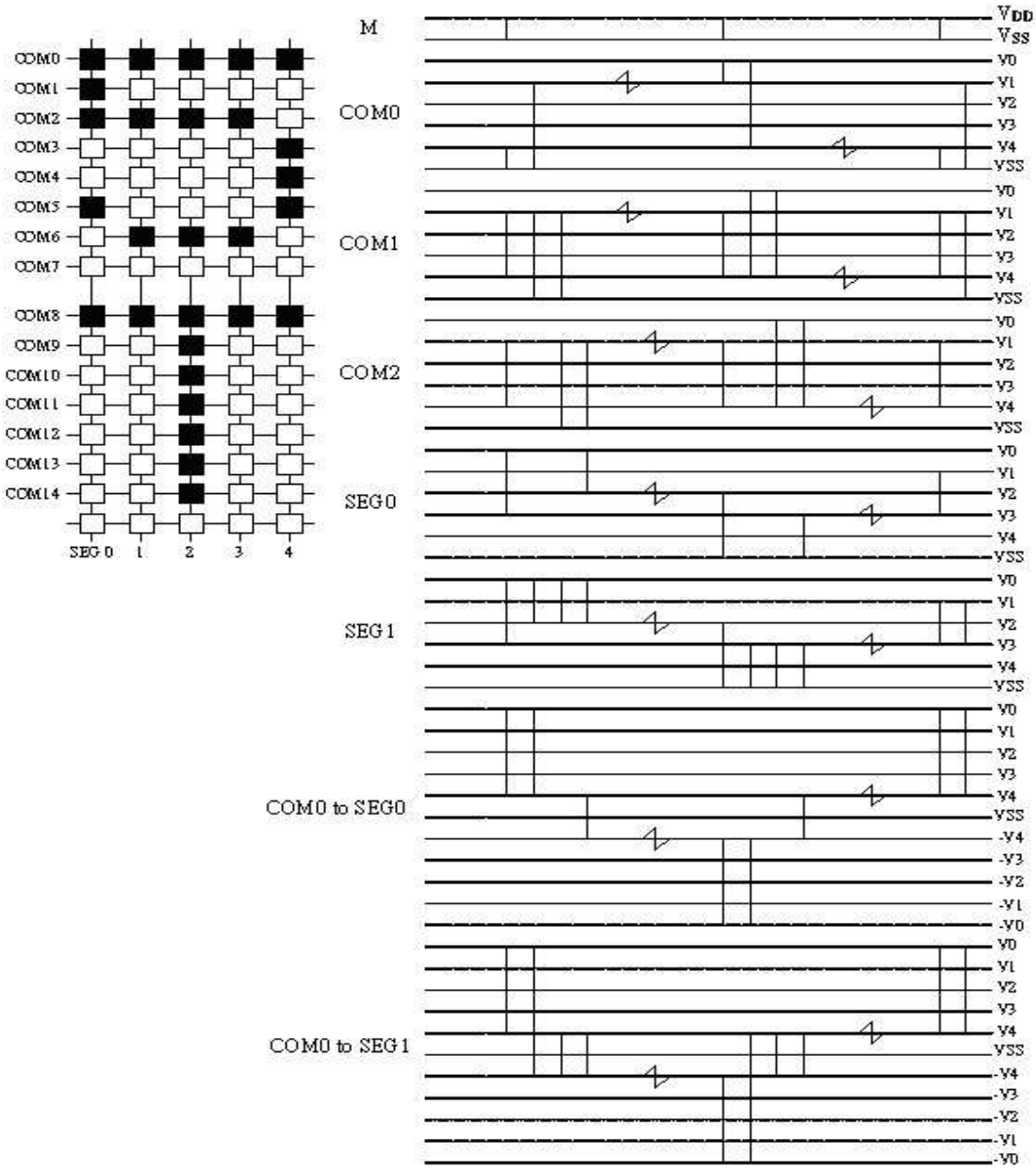


Figure 16. COM and SEG output waveform

■ Partial Display on LCD

The RW1095 realizes the Partial Display function on LCD with low-duty driving for saving power consumption and showing the various display duty. To show the various display duty on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages.

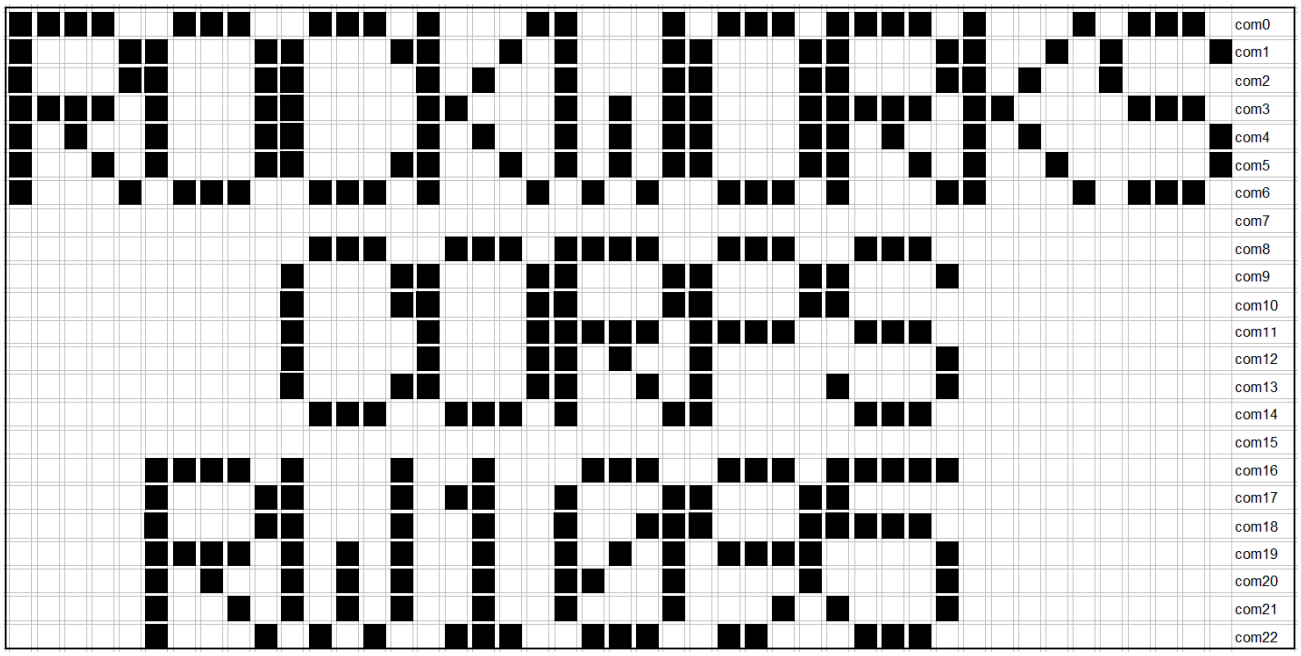


Figure 17.Reference Example for Partial Display

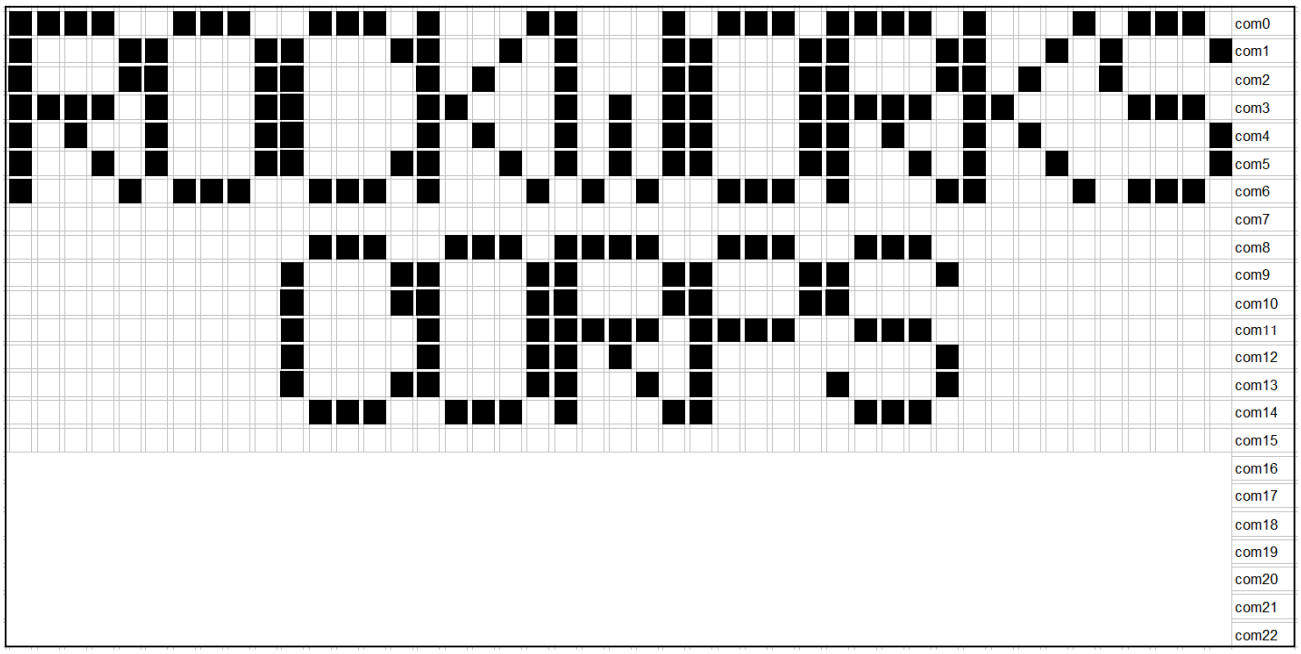


Figure 18.Partial Display (Partial Display Duty=16,initial COM0=0)

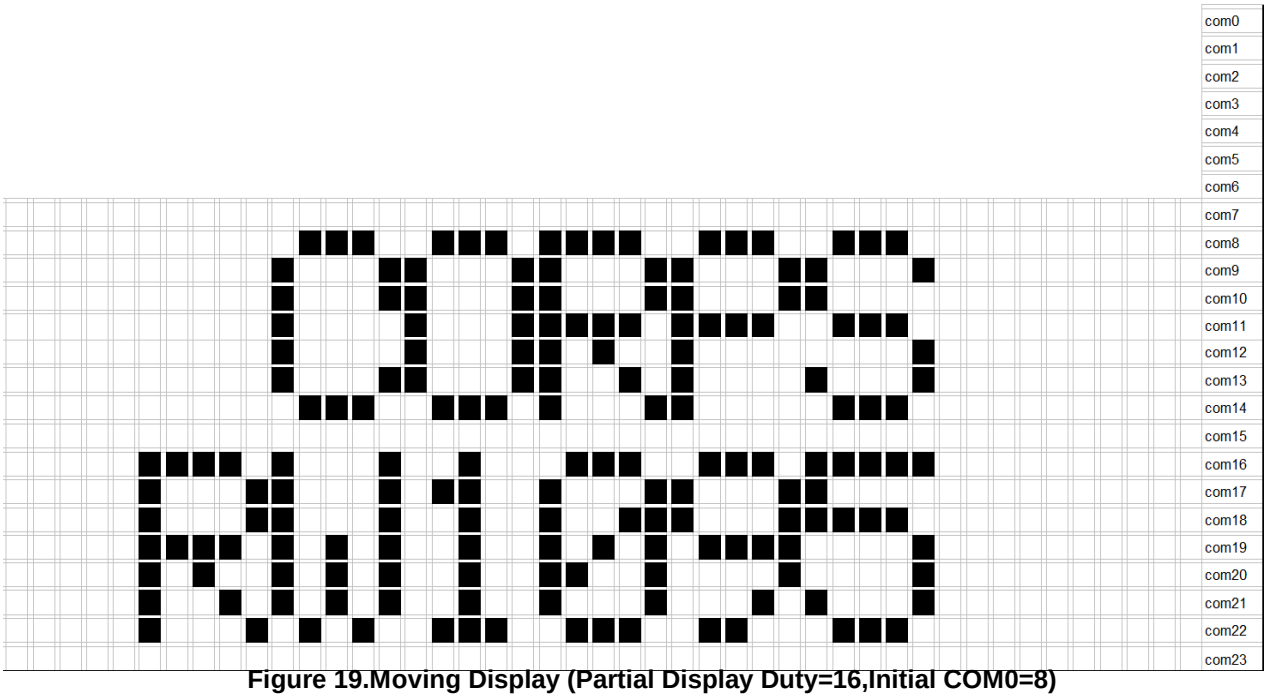


Figure 19.Moving Display (Partial Display Duty=16,Initial COM0=8)

■ The Power Supply Circuits (Power control set instruction)

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are controlled by power control set instruction .Table 4 shows the Power control set command 3-bit data control function and Table 4-1 shows the referenced combinations in using Power Supply circuits.

Table 4

bit	function	Status "1"	Status "0"
D2	Voltage booster circuit control bit (VB circuit)	ON	OFF
D1	Voltage regulator circuit control bit (VR circuit)	ON	OFF
D0	Voltage follower circuit control bit (VF circuit)	ON	OFF

User setup	Power Control set (VB VR VF)	VB circuits	VR circuits	VF circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Without capacitor	Without capacitor	Without capacitor
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Without capacitor	Without capacitor
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	External input	External input	Without capacitor
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	External input	External input	External input

Table 4-1 Recommended Power Supply Combinations

■ Voltage Converter Circuits

These circuits boost up the electric potential between VDD2 and VSS to 2~7 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

7X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,between CAP1N and CAP5P, between CAP2N and CAP6P and between VSS and VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 7 times the voltage level between VSS and VDD2.

4X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, and between VSS and VOUT, and short between CAP4P,CAP5P,CAP6P to VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 4 times the voltage level between VSS and VDD2.

6X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,between CAP1N and CAP5P, and between VSS and VOUT, and short CAP6P to VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 6 times the voltage level between VSS and VDD2.

3X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P and between VSS and VOUT, and short between CAP3P.,CAP4P,CAP5P and CAP6P to VOUT, to produce a voltages level in the positive direction at the VOUT terminal that is 3 times the voltage difference between VSS and VDD2.

5X step-up: Connect capacitor C1 between CAP1N and CAP1P, between CAP2N and CAP2P, between CAP1N and CAP3P, between CAP2N and CAP4P,and between VSS and VOUT, and short between CAP5P and CAP6P to VOUT, to produce a voltage level in the positive direction at the VOUT terminal that is 5 times the voltage level between VSS and VDD2.

2X step-up: Connect capacitor C1 between CAP1N and CAP1P, and between VSS and VOUT, leave CAP2N open, and short between CAP2P,AP3P,CAP4P,CAP5P and CAP6P to VOUT, to produce a voltage in the positive direction at the VOUT terminal that Is twice the voltage between VSS and VDD2.

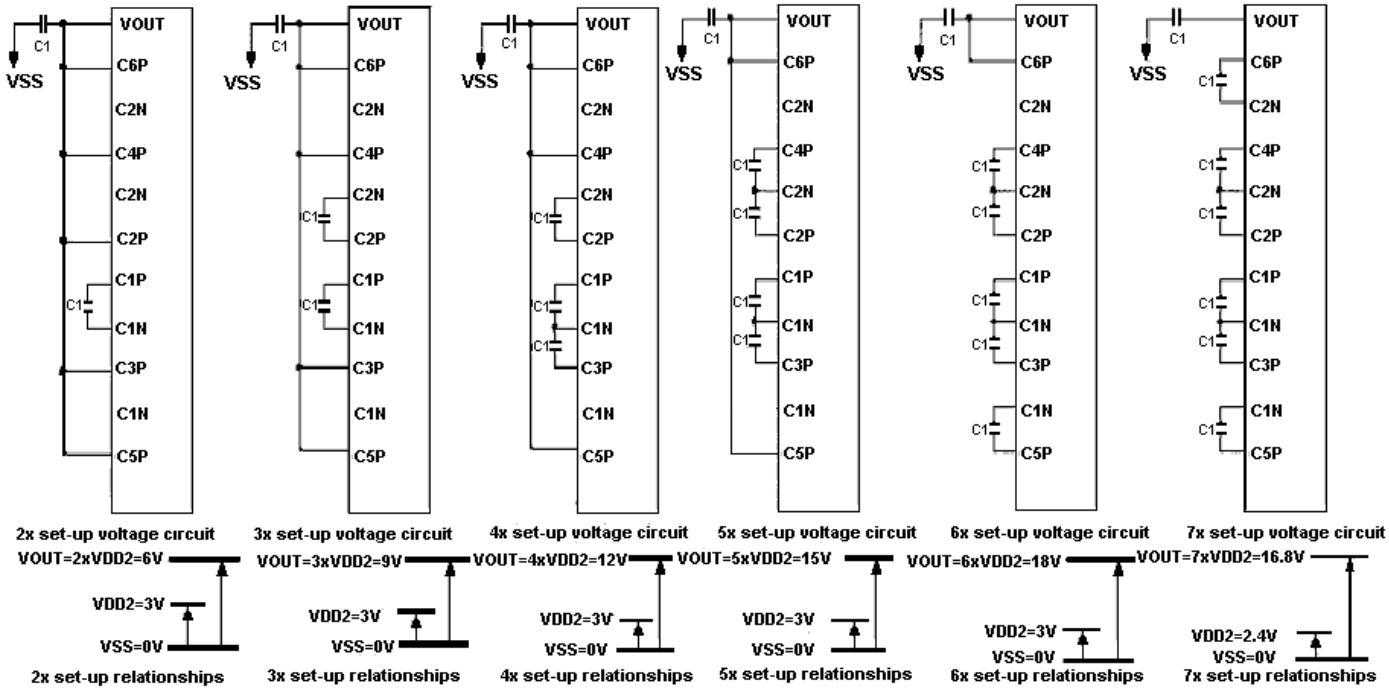
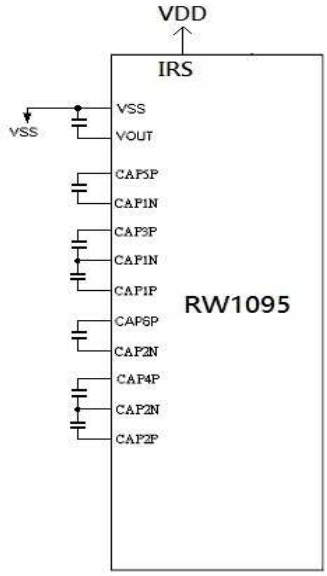


Figure 20.Booster Circuit setting

- The VDD2 voltage range must be set so that the VOUT terminal voltage does not exceed the absolute maximum rated value.

By Select DC-DC Set-up (2X,3X, 4X, 5X, 6X, 7X) instruction, we could easily set the built-in capacitor type booster performance with suitable current consumption.

Booster Circuit is setting 7X



If external booster circuit are setting 7X.the Select DC-DC Set-up instruction it can setting to 2X~7X(Maximum) ,please reference below:

Select DC-DC Set-up instruction:

DC2	DC1	DC0	Selected DC-DC Set-up
0	1	*	2 times boosting circuit
1	0	0	3 times boosting circuit
1	0	1	4 times boosting circuit
1	1	0	5 times boosting circuit
1	1	1	6 times boosting circuit
0	0	*	7 times boosting circuit

■ Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in Figure 21.,it is necessary to be applied internally or externally.
For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by IRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. VREF voltage at Ta= 25°C is shown in Table 5.

(A) When the V0 Voltage Regulator internal resistors are used (IRS =H)

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where| V0 | < | VOUT |.

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV\ [V] \text{ ------ (Eq. 1)}$$

$$VEV = (1 - \frac{(63 - \alpha)}{162}) \times VREF\ [V] \text{ ------ (Eq. 2)}$$

Table 5. **VREF Voltage at Ta = 25°C**

Temp. coefficient	VREF [V]
-0.125% / °C	2.1

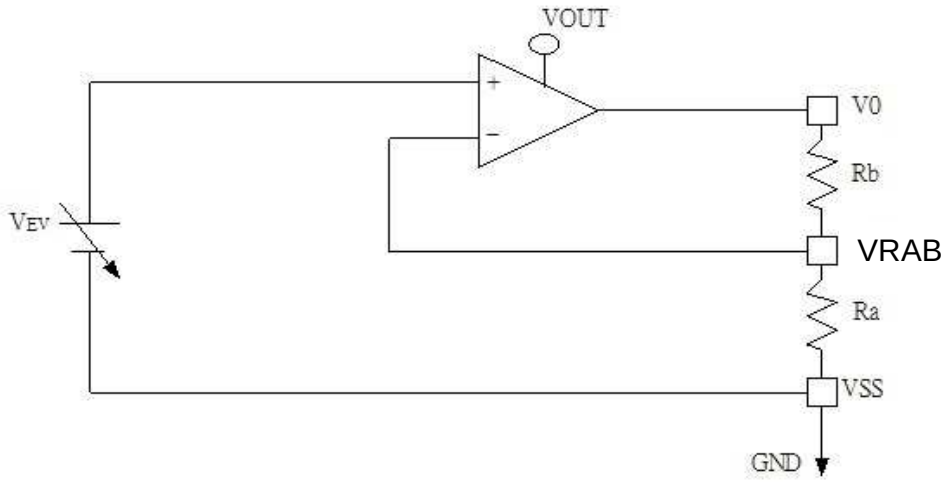


Figure 21. **Internal Voltage Regulator Circuit**

VREG is the IC-internal fixed voltage supply, and its voltage at Ta = 25℃ is as shown in Table 5

Table 5

Part no.	Equipment Type	Thermal Gradient	VREG
RW1095	Internal Power Supply	–0.05 %/℃	2.1V

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume registers. Table 6 shows the value for α depending on the electronic volume register settings.
Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1 + Rb/Ra) ratio assumes the values shown in Table 7 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 6

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			:			:
			:			:
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

V0 voltage regulator internal resistance ratio register value and (1 + Rb/Ra) ratio (Reference value)

Table 7

Register			RW1095
D2	D1	D0	(1) –0.05 %/℃
0	0	0	2.6
0	0	1	3.4
0	1	0	4.2
0	1	1	5.0
1	0	0	5.8
1	0	1	6.6
1	1	0	7.4
1	1	1	8.3

When IRS pin is **"H"**, resistor Ra is connected internally between VRAB pin and VSS, and Rb is connected between V0 and VRAB. We determine V0 by two instructions, " Select Regulator resistor " and "Select electronic volume register".

Table 8. Internal Rb / Ra Ratio depending on 3-bit Data (D2 D1 D0)

	3-bit data settings (D2 D1 D0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.6	3.4	4.2	5.0	5.8	6.6	7.4	8.3

Figure 22. shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

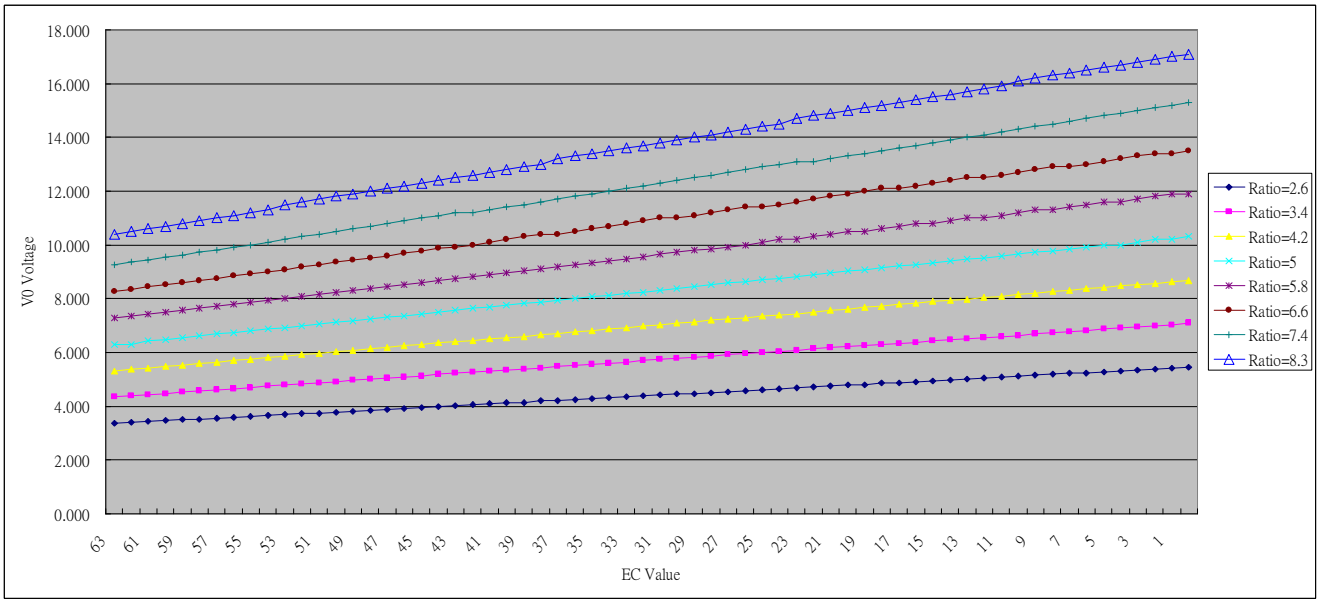


Figure 22. Electronic volume register (0 to 63)

(B) When an External Resistance is used (IRS =L)

When IRS pin is **"L"**, it is necessary to connect external regulator resistor Ra between VRAB and VSS, and Rb between V0 and VRAB.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V.
2. Electronic volume level (EC Value) D5~D0 = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1.5 uA

From Eq. 1

$$10=(1+\frac{Rb}{Ra})\times VEV\ [V]----------(Eq.\ 3)$$

From Eq. 1

$$VEV=(1-\frac{(63-32)}{162})\times 2.1=1.70\ [V]-------(Eq.\ 4)$$

From requirement 3

$$\frac{10}{Ra+Rb}=1.6\ [uA]-------(Eq.\ 5)$$

From equations Eq.3,4 and 5

Ra=1.06 [M ohms]

Rb=5.16 [M ohms]

Table 9 Shows the Range of V0 depending on the above Requirements.

Table 9. The Range of V0

	Electronic volume level (EC Value)				
	0	**.....**	**.....**	**.....**	**63**
V0 voltage	3.3V	**.....**	**.....**	**.....**	17.1V

■ Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 9 shows the relationship between V1 to V4 level and each duty ratio.

Table 9. The Relationship between V1 to V4 Level and Each Duty Ratio

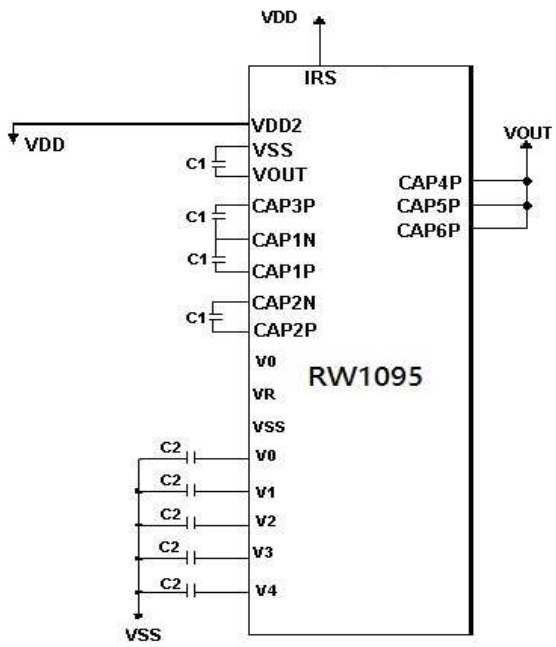
LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-2)/N x V0	2/N x V0	1/N x V0	N = 5 to 14
1/N	(N-1)/N x V0	(N-1)/N x V0	(N-1)/N x V0	(N-1)/N x V0	N=2
1/N	(N-1)/N x V0	(N-1)/N x V0	(N-2)/N x V0	(N-2)/N x V0	N=3
1/N	(N-1)/N x V0	(N-2)/N x V0	(N-2)/N x V0	(N-3)/N x V0	N=4

➢ Follower voltage reference circuit

Internal Booster:

1) When the V0 voltage regulator internal resistor is used.

(Example when VDD2= VDD, with 4x set-up)

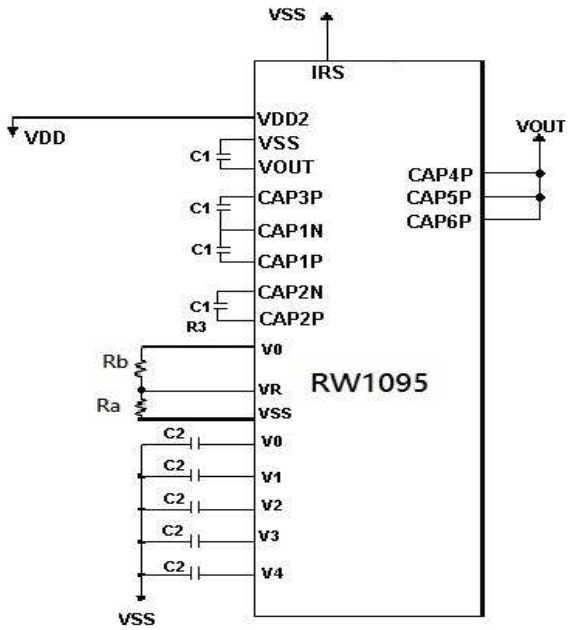


C1=2.2uF/25V~4.7uF/25V

C2=2.2uF/25V ~4.7uF/25V

(2) When the V0 voltage regulator internal resistor is not used.

(Example when VDD2= VDD, with 4x set-up)

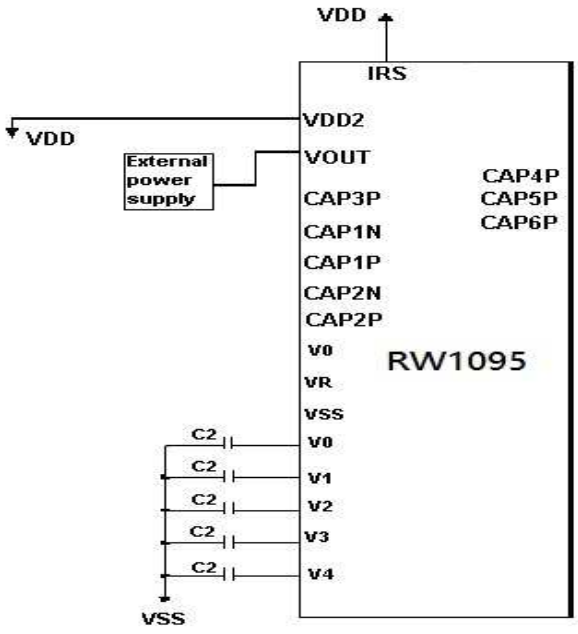


C1=2.2uF/25V ~4.7uF/25V

C2=2.2uF/25V ~4.7uF/25V

External Booster:

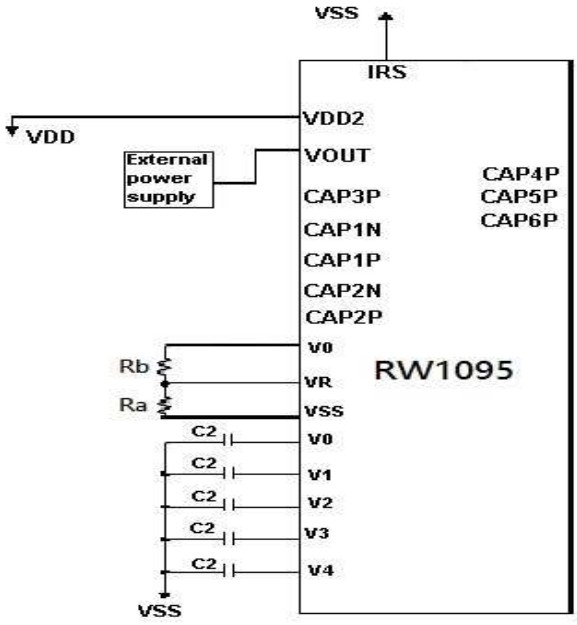
(1) When the V0 voltage regulator internal resistor is used.



External VOUT Voltage= 18V (Maximum)

C2=2.2uF/25V ~4.7uF/25V

(2) When the V0 voltage regulator internal resistor is not used.

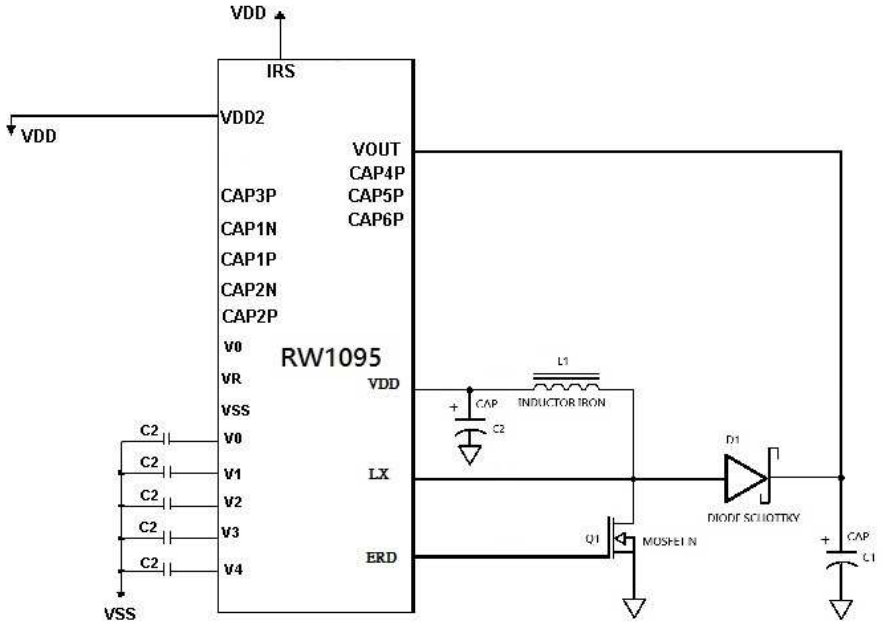


External VOUT Voltage= 18V (Maximum)

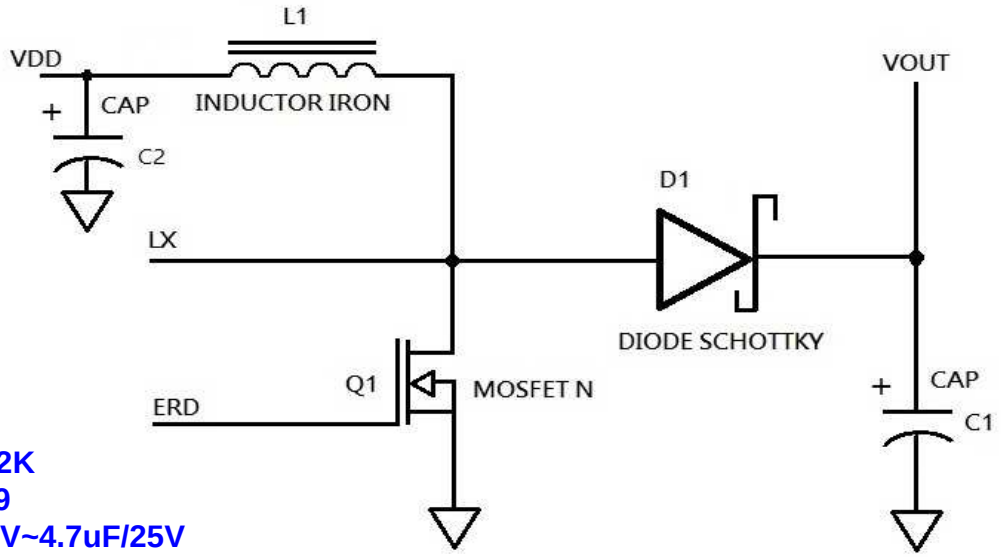
C2=2.2uF/25V ~4.7uF/25V

■ Inductor type regulator circuit setup:

RW1095 has built-in a inductor type switching regulator as well, which can be selected by software, the turn on inductor type regulator circuit sequence please reference page 74.



Inductor Type Switching Regulator Circuit



Q1:2N7002K
D1:1N5819
C1:1uF/25V~4.7uF/25V
C2:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

■ RESET CIRCUIT

Setting RSTP to "L" or Reset instruction can initialize internal function.
When RSTP becomes "L", following procedure is occurred.

1.Set Page Address: 0
2.Set Column Address: 0
3.Set read-modify-write: OFF
4.Display ON / OFF: OFF
5.Set initial display register: 0 (first)
6.Set initial COM0 register: 0 (COM0)
7.Reverse display ON / OFF: OFF (normal)
8.Set N-line inversion register: 0 (disable)
9.Entire Display ON/OFF: OFF
10.Power control set: 0,0,0
11. ADC select: 0
12. SHL select: 0
13.Oscillator on start: OFF
14.Set Power Save Mode: Release
15.Set Data Length for 3-SPI: 0
16.Set Gray scale mode: 0 (Mono mode)
17.Set White mode and light gray mode pulse width (WA3, WA2, WA1, WA0) = (0, 0, 0, 0)
18. Set White mode and light gray mode pulse width (LA3, LA2, LA1, LA0) = (0, 0, 1, 1)
19. Set dark gray mode and black mode pulse width (DA3, DA2, DA1, DA0) = (1, 0, 0, 0)
20. Set dark gray mode and black mode pulse width r (BA3, BA2, BA1, BA0) = (1, 1, 0, 0)
22.Column address counter [8:0] = 0, Page address counter [4:0] = 0
23.After power-on, RAM data are undefined

While RSTP is "L" or reset instruction is executed, no instruction except read status can be accepted, any instruction can be accepted. RSTP must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RSTP is essential before used.

■ INSTRUCTION TABLE

Instruction	A0	E	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1												
Mode Set	0	1	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**EXT**	EXT register set
EXT=0												
(1)Read display data	1	0	1	**Read data**								Read data into DDRAM
(2)Write display data	1	1	0	**Write data**								Write data into DDRAM
(3)Read status	0	0	1	**BUSY**	**ADC**	**ON/ OFF**	**RESET**	**0**	**0**	**0**	**0**	Read the internal status
(4)Set Page Address	0	1	0	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	Set page address
				0	**0**	**0**	**P4**	**P3**	**P2**	**P1**	**P0**	
(5)Set Page Address for KS0719 mode	0	1	0	**1**	**0**	**1**	**1**	**P3**	**P2**	**P1**	**P0**	Set page address for KS 0719 mode
(6)Set Column Address MSB	0	1	0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	Set column address MSB
				0	**0**	**0**	**Y8**	**Y7**	**Y6**	**Y5**	**Y4**	
(6-1)Set Column Address LSB	0	1	0	**0**	**0**	**0**	**0**	**Y3**	**Y2**	**Y1**	**Y0**	Set column address LSB
(7)Set Column Address MSB for KS0719 mode	0	1	0	**0**	**0**	**0**	**1**	**Y7**	**Y6**	**Y5**	**Y4**	Set column address MSB for KS0719 mode
(7-1)Set Column Address LSB for KS0719 mode	0	1	0	**0**	**0**	**0**	**0**	**Y3**	**Y2**	**Y1**	**Y0**	Set column address LSB for KS0719 mode
(8)Set read -modify-write	0	1	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	Set read-modify-write (default=0)
(9)Reset read-modify-write	0	1	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**	Release read –modify-write
(10)Display ON/OFF	0	1	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**D**	D=0:Display OFF(default) D=1:Display ON

Instruction	A0	E	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1												
Mode Set	0	1	0	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**EXT**	EXT register set
EXT=0												
(11)Set initial display register	0	1	0	**0**	**1**	**0**	**0**	**0**	**0**	**X**	**X**	2-bytes instruction to specify the initial display line to realize vertical scrolling
				S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**	
(12)Set initial COM0 register	0	1	0	**0**	**1**	**0**	**0**	**0**	**1**	**X**	**X**	2-bytes instruction to specify the initial COM0 to realize window scrolling
				C7	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**	
(13)Set partial display duty ratio	0	1	0	**0**	**1**	**0**	**0**	**1**	**0**	**X**	**X**	2-bytes instruction to set partial display duty ratio **(valid for 8~104,128,160)**
				D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
(14)Set N-line inversion register	0	1	0	**0**	**1**	**0**	**0**	**1**	**1**	**X**	**X**	2-bytes instruction to set N-line inversion **(N-line number should be smaller than partial duty ratio)**
				X	**X**	**X**	**N4**	**N3**	**N2**	**N1**	**N0**	
(15)Release N-line inversion register	0	1	0	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	Release N-line inversion mode
(16)Reverse display ON/OFF	0	1	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	**REV**	REV=0:normal display(default) REV=1:revese display
(17)Entire display ON/OFF	0	1	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**ALL ON**	ALLON=0:normal display(default) ALLON=1:entire display ON
(18)Power control set	0	1	0	**0**	**0**	**1**	**0**	**1**	**VB**	**VR**	**VF**	Control power circuit operation
(19)Select DC-DC Set-up	0	1	0	**0**	**1**	**1**	**0**	**0**	**DC2**	**DC1**	**DC0**	Select the step-up of internal voltage converter
(20)Select Regulator resistor	0	1	0	**0**	**0**	**1**	**0**	**0**	**R2**	**R1**	**R0**	Select internal resistor ratio(Rb/Ra) mode
(21)Select electronic volume register	0	1	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	Set the V0 output voltage electronic volume register
				X	**X**	**EV5**	**EV4**	**EV3**	**EV2**	**EV1**	**EV0**	
(22)Select LCD bias	0	1	0	**0**	**1**	**0**	**1**	**B3**	**B2**	**B1**	**B0**	Select bias 1/2~1/14 bias

Instruction	A0	E	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
EXT=0 or 1												
Mode Set	0	1	0	1	1	0	1	0	0	0	EXT	EXT register set
EXT=0												
(23)SHL select	0	1	0	1	1	0	0	SHL	X	X	X	COM bi-direction selection SHL=0:normal (default) SHL=1:reverse
(24)ADC select	0	1	0	1	0	1	0	0	0	0	ADC	SEG bi-direction selection ADC=0:normal (default) ADC=1:reverse
(25)Oscillator on start	0	1	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
(26)Set Power Save mode	0	1	0	1	0	1	0	1	0	0	P	P=0:standby mode P=1:sleep mode
(27)Release Power Save mode	0	1	0	1	1	1	0	0	0	0	1	Release power save mode
(28)Set Data Length for 3-SPI	0	1	0	0	1	1	1	0	0	0	0	Set data length for 3-SPI (only valid for 3-SPI mode)
				SPA7	SPA6	SPA5	SPA4	SPA3	SPA2	SPA1	SPA0	
(29)Frame Frequency adjustment	0	1	0	1	1	1	1	0	0	1	1	FRR*2=0: normal (default) FRR*2=1: double Frame frequency DFR3~DFR0:Frame frequency adjustment.**(FRR*2 only support duty under 1/81)**
				0	0	0	FRR *2	DFR3	DFR2	DFR1	DFR0	
(30)Inductor type regulator circuit ON/OFF	0	1	0	1	1	1	1	0	1	0	0	LVON:LV follower on/off SWON:=0:switching regulator off SWON=1:switching regulator on
				1	1	LVON	0	0	0	0	SWON	
(31)Reset	0	1	0	1	1	1	0	0	0	1	0	Initial the internal function
(32)Nop	0	1	0	1	1	1	0	0	0	1	1	No operation
EXT=1												
(33)Set Gray scale mode	0	1	0	1	0	0	1	1	0	1	GRAY	Set mono mode and 4-gray mode
(34) Set White mode and light gray mode pulse width	0	1	0	1	0	0	1	1	0	0	0	Set white mode and light gray mode
				WA3	WA2	WA1	WA0	LA3	LA2	LA1	LA0	
(35) Set dark gray mode and black mode pulse width	0	1	0	1	0	0	1	1	0	0	1	Set dark gray and black mode
				DA3	DA2	DA1	DA0	BA3	BA2	BA1	BA0	

■ INSTRUCTION DESCRIPTION

(1) Read display data (EXT="0")

This command reads 8-bit data from the specified display data RAM address. Since the column address is automatically incremented by "1" after the read, the CPU can continuously read multiple-word data. One dummy read is required immediately after the column address has been set. See the function explanation in "Display Data RAM" for the explanation of accessing the internal registers. When the serial interface is used, reading of the display data becomes unavailable.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	1	Read Data							

(2) Write display data (EXT="0")

This command writes 8-bit data to the specified display data RAM address. Since the column address is automatically incremented by "1" after the write, the MPU can write the display data.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	0	Write Data							

(3) Read status (EXT="0")

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	BUSY	ADC	ON/ OFF	RESET	0	0	0	0

BUSY	**BUSY=1**:it indicates that either processing is occurring internally or a reset condition is in process **BUSY=0**:A new command can be accepted. If the cycle time can be satisfied , there us no need to check for BUSY condition.
ADC	This shows the relationship between the column address and the segment driver . **0:Normal** (column address n ↔ SEG n) **1:Reverse** (column address 252-n ↔ SEG n)
ON/OFF	ON/OFF: indicates the display ON/OFF state. **0:Display ON** **1:Display OFF**
RESET	This indicates that the chip is in the process of initialization either because of a RSTP signal or because of a reset command. **0:Operating state** **1:Reset in progress**

(4) Set Page Address (EXT="0")

Sets the Page Address of display data RAM from the microprocessor into the page address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't affect the display status. ICON page is to set the page address to "31".

Set Page Command for all mode except KS0719 Mode (double command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	1	0	0	0	0
			0	0	0	P4	P3	P2	P1	P0

P4	P3	P2	P1	P0	Page address
0	0	0	0	0	0
0	0	0	0	1	1
:	:	:	:	:	:
1	0	0	1	0	18
1	0	0	1	1	19
1	1	1	1	1	31(Icon Page)

(5) Set Page Address for KS0719 mode (EXT="0")

Set Page Command for KS0719 Mode only (single command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Page address
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
1	0	1	0	11
1	1	0	0	12
1	1	0	1	13(Icon Page)
1	1	1	0	Not accessible page .
1	1	1	1	Don't use these pages

(6) Set Column Address MSB (EXT="0")

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data.
When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB for all modes except KS0719 mode (double command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	1	0	0	0	0
			0	0	0	Y8	Y7	Y6	Y5	Y4

(6-1) Set Column Address LSB (EXT="0")

Set Column Address LSB for all modes expect KS0719 mode

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	Y3	Y2	Y1	Y0

Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address [Y8:Y0]
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1
	:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	0	254
0	1	1	1	1	1	1	1	1	255
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	0	318
1	0	0	1	1	1	1	1	1	319

(7)Set Column Address MSB for KS0719 mode(EXT="0")

Set Column Address MSB for KS0719 mode only

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	1	Y7	Y6	Y5	Y4

(7-1)Set Column Address LSB for KS0719 mode(EXT="0")

Set Column Address LSB for KS0719 mode only

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	0	0	Y3	Y2	Y1	Y0

Set Column Address for KS0719 mode:

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address [Y7:Y0]
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159
:	:	:	:	:	:	:	:	Not accessible column

(8) Set read-modify-write (EXT="0")

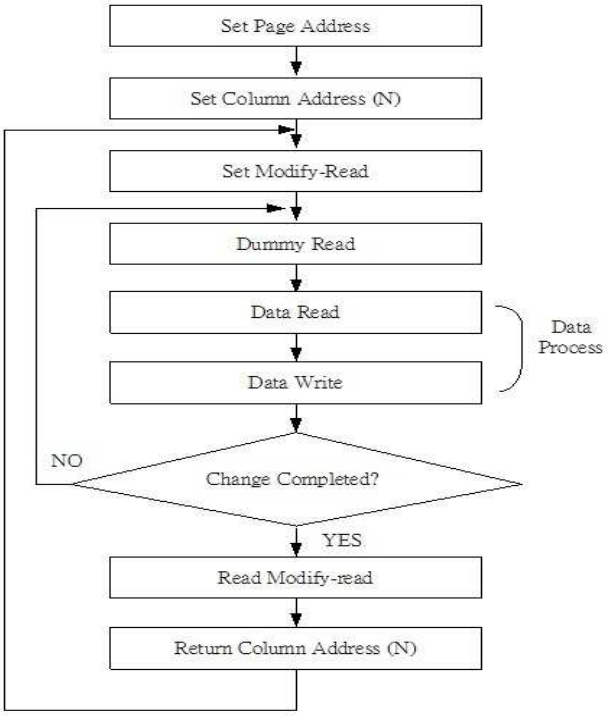
This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Read-modify-rite instruction.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	0	0

(9) Reset read-modify-write (EXT="0")

This instruction cancels the Modify-Read mode, and makes the column address return to its initial value just before the set Read-modify-Write instruction is started.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	1	1	1	0



Command Sequence for Read-Modify-Write

(10) Display ON/OFF (EXT="0")

This command turns the display ON or OFF.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	1	1	1	D

D=0:display off
D=1:display on

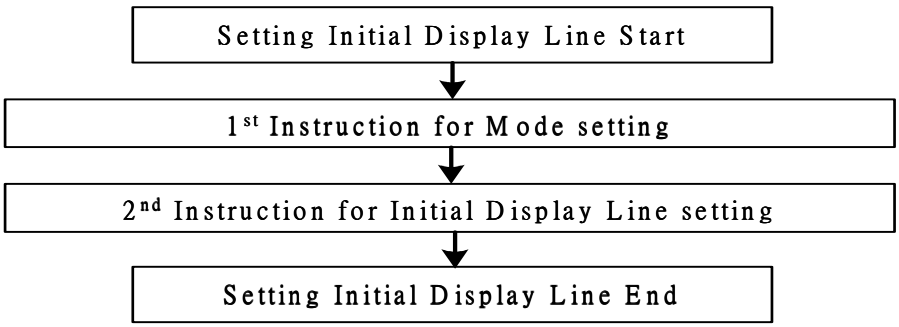
(11) Set initial display register (EXT="0")

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top of row (COM0) of LCD panel.

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	0	0	0	0	X	X
			S7	S6	S5	S4	S3	S2	S1	S0

S7	S6	S5	S4	S3	S2	S1	S0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	0	156
1	0	0	1	1	1	0	1	157
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159



Sequence For Setting Initial Display Line

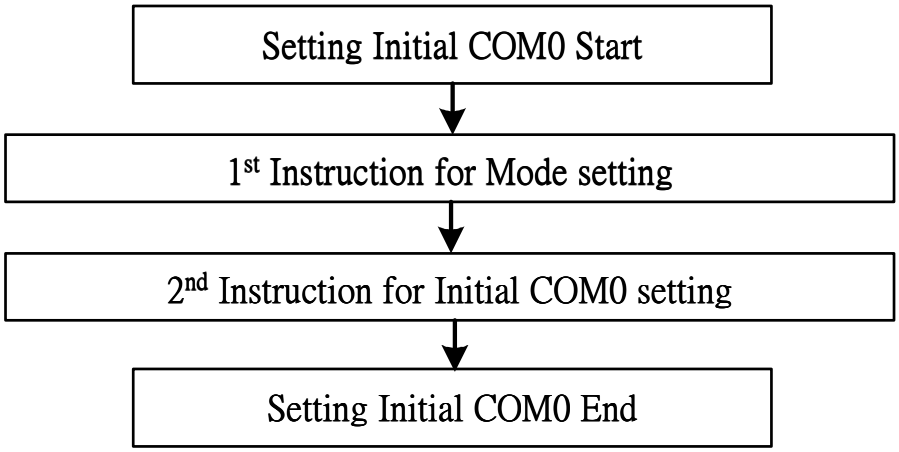
(12) Set initial COM0 register (EXT="0")

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	0	0	0	1	X	X
			C7	C6	C5	C4	C3	C2	C1	C0

C7	C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	0	156
1	0	0	1	1	1	0	1	157
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159



Sequence For Setting Initial COM0

(13) Set partial display duty ratio (EXT="0")

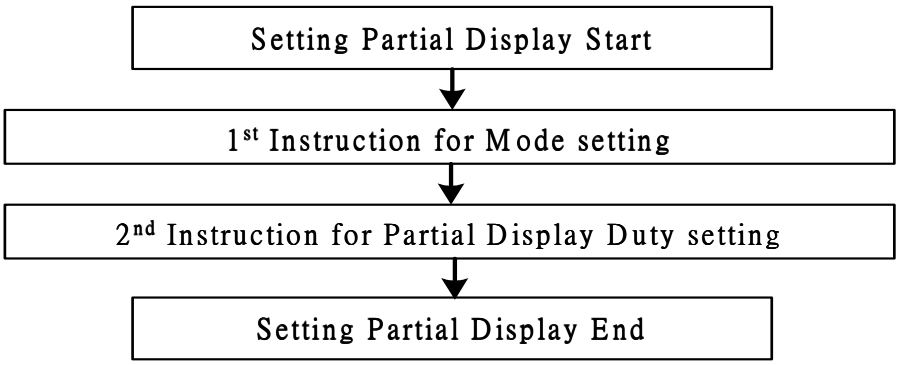
Sets the duty ratio within range of 16 to 128 (ICON disabled) or 17 to 129 (ICON enabled) to realize partial display by using the 2-byte instruction.

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	0	0	1	0	X	X
			D7	D6	D5	D4	D3	D2	D1	D0

***set partial duty 9~105,129,161 only**

D7	D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio mode (ICON enabled)
0	0	0	0	0	0	0	0	No operation
:	:	:	:	:	:	:	:	
0	0	0	0	0	1	1	1	
0	0	0	0	1	0	0	0	1/9
0	0	0	0	1	0	0	1	1/10
:	:	:	:	:	:	:	:	:
0	1	0	0	1	0	0	0	1/73
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	1/129
:	:	:	:	:	:	:	:	No Operation
:	:	:	:	:	:	:	:	
1	0	1	0	0	0	0	0	1/161
1	0	0	1	0	0	0	1	No Operation
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	1	



Sequence For Setting Partial Display

(14) Set N-line inversion register (EXT="0")

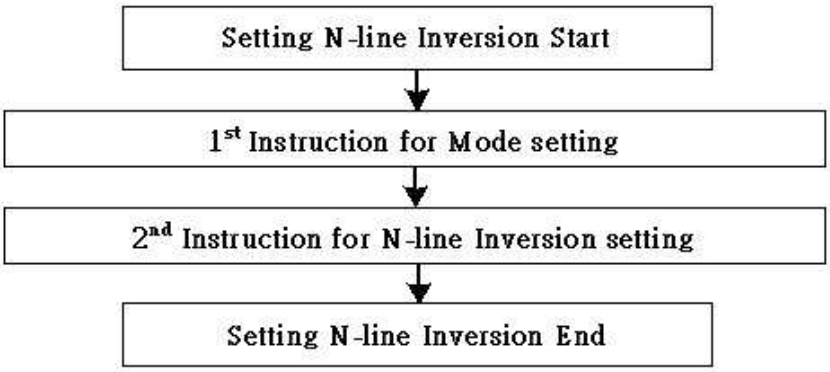
Sets the inverted line number within range of 2 to 32 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

N : N for N-line inversion (N is selectable by customers).

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	0	0	1	1	X	X
			X	X	X	N4	N3	N2	N1	N0

N4	N3	N2	N1	N0	Selected N-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	2-line inversion
0	0	0	1	0	3-line inversion
0	0	0	1	1	4-line inversion
:	:	:	:	:	:
1	1	1	0	1	30-line inversion
1	1	1	1	0	31-line inversion
1	1	1	1	1	32-line inversion



Sequence For N-line Inversion

(15) Release N-line inversion register (EXT="0")

Returns to the frame inversion condition from the n-line inversion condition.

A0	E(XRD)	RW(XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	1	0	0

(16) Reverse display ON/OFF (EXT="0")

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	1	1	REV

(17) Entire display ON/OFF (EXT="0")

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the Reverse Display ON / OFF instruction.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	1	0	ALLON

ALLON=0:Normal display (default)
ALLON=1:Entire display ON

(18) Power control set (EXT="0")

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	0	1	VB	VR	VF

VB	VR	VF	Status of internal power supply circuits
0 1			Internal voltage booster circuit is OFF Internal voltage booster circuit is ON
	0 1		Internal voltage regulator circuit is OFF Internal voltage regulator circuit is ON
		0 1	Internal voltage follower circuit is OFF Internal voltage follower circuit is ON

(19) Select DC-DC Set-up (EXT="0")

Selects one of 7 DC-DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	1	0	0	DC2	DC1	DC0

DC2	DC1	DC0	Selected DC-DC Set-up
0	1	*	2 times boosting circuit
1	0	0	3 times boosting circuit
1	0	1	4 times boosting circuit
1	1	0	5 times boosting circuit
1	1	1	6 times boosting circuit
0	0	*	7 times boosting circuit

(20) Select Regulator resistor (EXT="0")

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	1+(Rb/Ra)
0	0	0	2.6
0	0	1	3.4
0	1	0	4.2
0	1	1	5.0
1	0	0	5.8
1	0	1	6.6
1	1	0	7.4
1	1	1	8.3

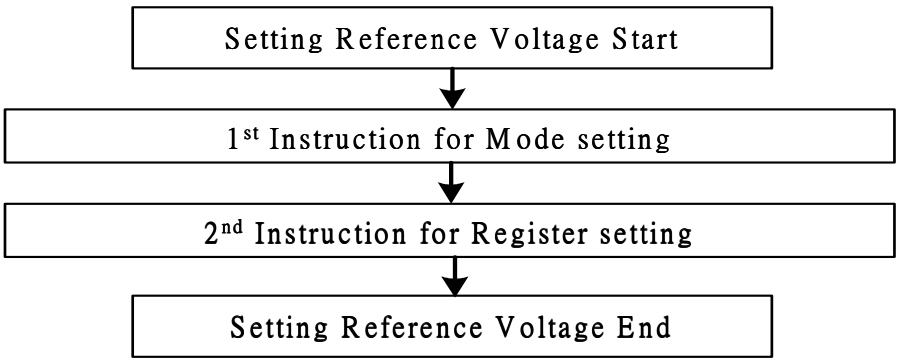
(21) Select electronic volume register (EXT="0")

Consist of 2-byte Instructions
The 1st instruction set Reference Voltage mode, the 2nd one updates the contents of reference voltage register.
After second instruction, Reference Voltage mode is released.

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	0	0	0	0	1
			X	X	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage parameter (α)
0	0	0	0	0	0	63
0	0	0	0	0	1	62
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	1
1	1	1	1	1	1	0



Sequence For Setting the Electronic Volume

(22) Select LCD bias (EXT="0")

Selects LCD bias ratio of the voltage required for driving the LCD.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	0	1	B3	B2	B1	B0

B3	B2	B1	B0	LCD bias
0	0	0	0	1/4
0	0	0	1	1/5
0	0	1	0	1/6
0	0	1	1	1/7
0	1	0	0	1/8
0	1	0	1	1/9
0	1	1	0	1/10
0	1	1	1	1/11
1	0	0	0	1/2
1	0	0	1	1/3
1	0	1	0	1/12
1	0	1	1	1/13
1	1	0	0	1/14

(23) SHL Select (EXT="0")

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	0	0	SHL	X	X	X

SHL = 0: normal direction (COM0 → COM-N)

SHL = 1: reverse direction (COM-N → COM0)

(24) ADC Select (EXT="0")

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG-N)

ADC = 1: reverse direction (SEG-N → SEG0)

(25) Oscillator on start (EXT="0")

This instruction enables the built-in oscillator circuit.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	1	0	1	1

(26) Set Power Save mode (EXT="0")

The RW1095 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

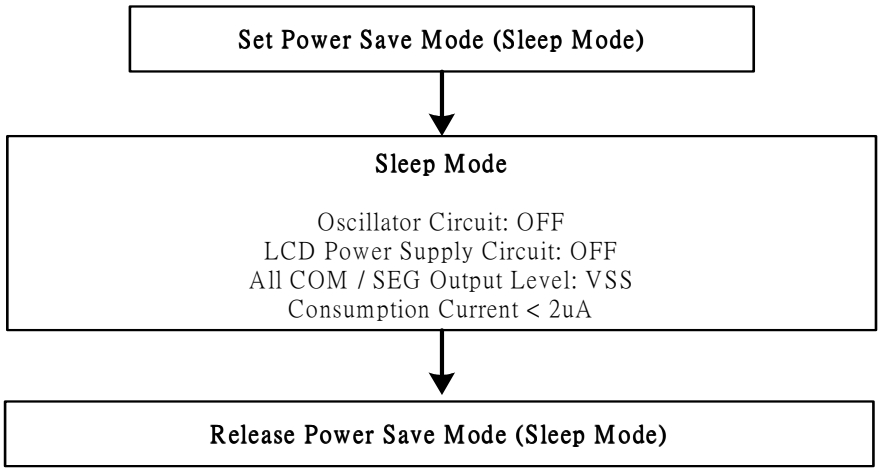
A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	1	0	1	0	0	P

P = 0: normal mode

P = 1: sleep mode

(27) Release Power Save mode (EXT="0")

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	0	1



Power Save Routine

(28) Set Data Length for 3-SPI (EXT="0")

Consists of 2 bytes instruction.

This command is used in 3-Line SPI mode only . It will be two continuous commands, the first byte control the data direction(write mode only) and inform the LCD driver the second byte will be number of data bytes will be write. When A0 is not used, the Display Data Length instruction is used to indicate that a specified number of display data bytes are to be transmitted. The next byte after the display data string is handled as command data.

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	1	1	1	0	0	0	0
			SPA7	SPA6	SPA5	SPA4	SPA3	SPA2	SPA1	SPA0

SPA7	SPA 6	SPA 5	SPA 4	SPA 3	SPA 2	SPA 1	SPA 0	Display Data Length
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	1	1	4
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	1	254
1	1	1	1	1	1	1	0	255
1	1	1	1	1	1	1	1	256

(29) Frame Frequency adjustment (EXT="0")

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	1	0	0	1	1
			0	0	0	FRR*2	DFR3	DFR2	DFR1	DFR0

FRR*2=0: normal (default)
FRR*2=1: double frame frequency
(Double frame frequency feature supported only in 81,65,49,33,17,9,5,4 and static Duties. Double frame frequency feature not supported in 161,129 and 105 duties)

DFR3~DFR0: Frame Frequency adjustment from 0000 (slow) ~1111 (fast)

Frame Frequency adjustment table: (+/- 10%)

Valid for 161,129 and 105 duties

DFR3	DFR2	DFR1	DFR0	FRR (Hz)
0	0	0	0	78 (default)
0	0	0	1	54
0	0	1	0	57
0	0	1	1	60
0	1	0	0	61
0	1	0	1	64
0	1	1	0	68
0	1	1	1	73
1	0	0	0	75
1	0	0	1	79
1	0	1	0	82
1	0	1	1	86
1	1	0	0	91
1	1	0	1	94
1	1	1	0	98
1	1	1	1	102

Valid for 81,65,49,33,17,9,5,4 and static duties

DFR3	DFR2	DFR1	DFR0	FRR (Hz)	FRR*2 (Hz)
0	0	0	0	76 (default)	152
0	0	0	1	55	111
0	0	1	0	58	115
0	0	1	1	60	121
0	1	0	0	62	124
0	1	0	1	65	132
0	1	1	0	69	139
0	1	1	1	71	143
1	0	0	0	76	152
1	0	0	1	79	159
1	0	1	0	81	164
1	0	1	1	86	175
1	1	0	0	89	182
1	1	0	1	94	192
1	1	1	0	100	200
1	1	1	1	102	204

(30) Inductor type regulator circuit ON/OFF (EXT="0")

RW1095 has built-in inductor type regulator circuit for big current drive application, when internal switching regulator is used, please combine with internal regulator command together.

First, turn on the internal regulator(power control set command) VR=1

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	0	0	1	0	1	VB	1 (VR)	VF

Second ,set the SWON=1

(double-command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	1	0	1	0	0
			1	1	LVON	0	0	0	0	SWON

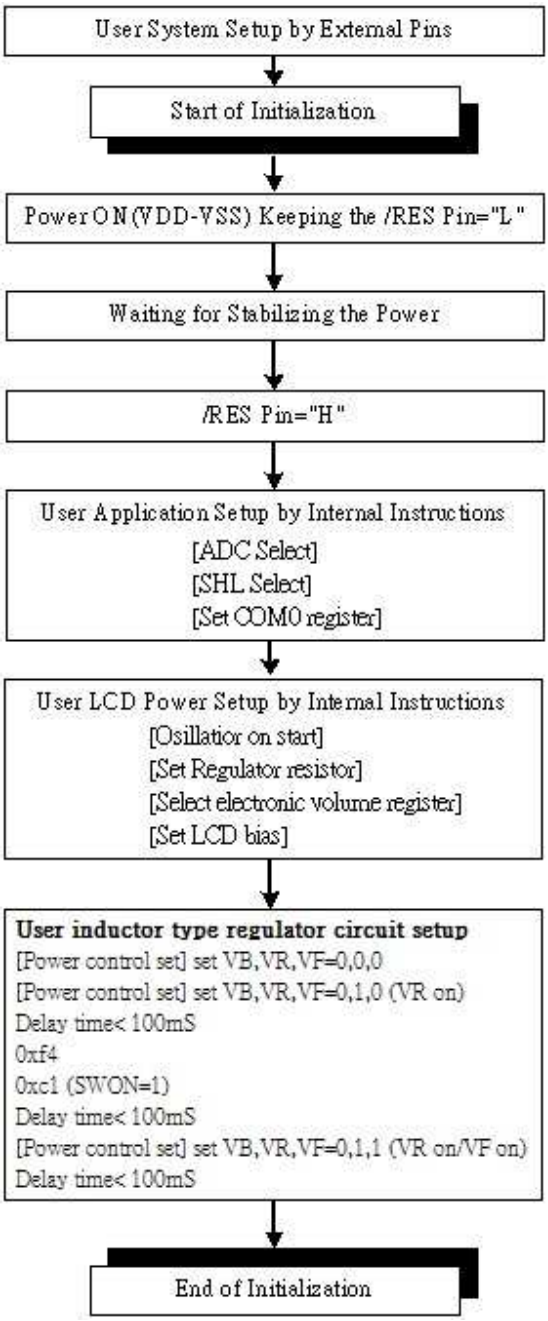
LVON=0: LV follower off
LVON=1: LV follower on

SWON=0: switching regulator off
SWON =1: switching regulator on

LVON and VF can not be "1" at the same time.
※V2=1/2 V0 if use internal low power regulator

For 1/2 bias application, RW1095 provides a low power consumption regulator to reduce current consumption by setting LVON to "1", a normal regulator VR has to be set to "0" while using low voltage regulator circuit, and connect V1,V2,V3 and V4 have to be connected externally.

Initial sequence for using inductor type regulator circuit:



(31) Reset (EXT="0")

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RSTP pin.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	1	0

(32) Nop (EXT="0")

No operation

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	0	0	0	1	1

Test Instruction (EXT="0")

This instruction is for testing IC. Please do not use it.

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	1	1	1	X	X	X	X

(33) Set Gray scale mode (EXT="1")

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	1	1	0	1	GRAY

GRAY = 0: mono color mode
GRAY = 1: 4-grey scale mode

Consists of 2 bytes instruction. The first byte sets grayscale mode and the second byte updates the contents of gray scale register without issuing any other instruction.

(34) Set white mode and light gray mode pulse width (EXT="1") (double command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	1	1	0	0	0
			WA3	WA2	WA1	WA0	LA3	LA2	LA1	LA0

(35) Set dark gray mode and black mode pulse width (EXT="1") (double command)

A0	E (XRD)	RW (XWR)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	0	1	0	0	1	1	0	0	1
			DA3	DA2	DA1	DA0	BA3	BA2	BA1	BA0

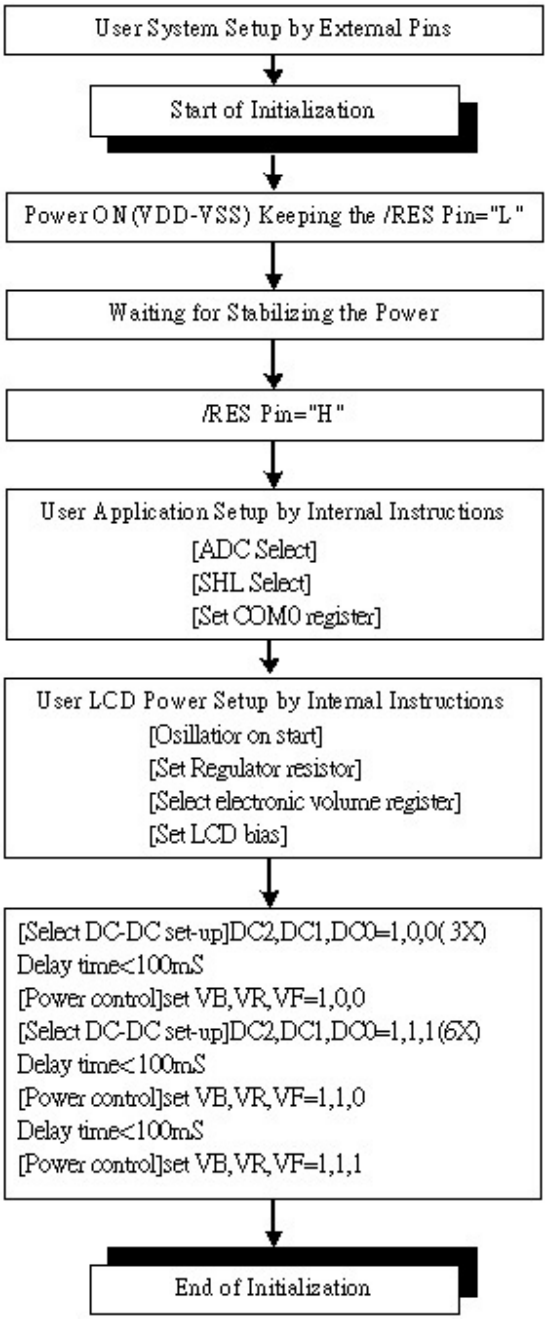
LA3/WA3/DA3/BA3	LA2/WA2/DA2/BA2	LA1/WA1/DA1/BA1	LA0/WA0/DA0/BA0	Pulse width(12 PWM)
0	0	0	0	0/12
0	0	0	1	1/12
0	0	1	0	2/12
0	0	1	1	3/12
0	1	0	0	4/12
0	1	0	1	5/12
0	1	1	0	6/12
0	1	1	1	7/12
1	0	0	0	8/12
1	0	0	1	9/12
1	0	1	0	10/12
1	0	1	1	11/12
1	1	0	0	12/12
1	1	0	1	12/12
1	1	1	0	12/12
1	1	1	1	12/12

■ COMMAND DESCRIPTION

(1):Instruction Setup: Reference

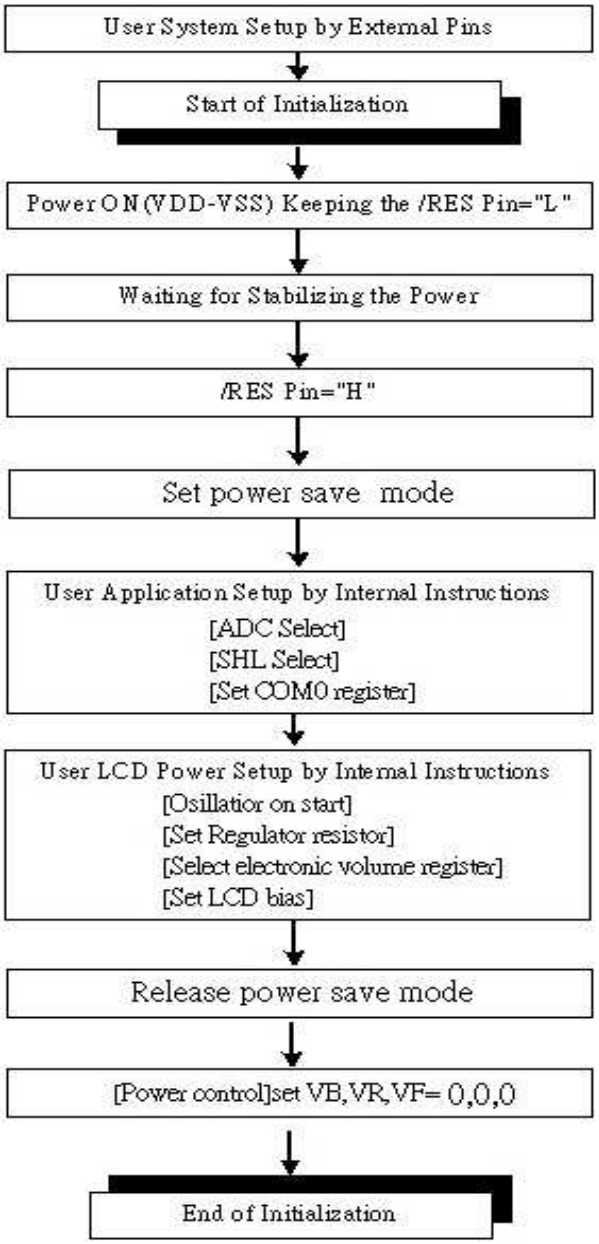
Note: After RW1095 is reset, the voltage level of the LCD driving output pins SEG and COM is VSS

a. When the built-in is being used immediately after turning on the power.



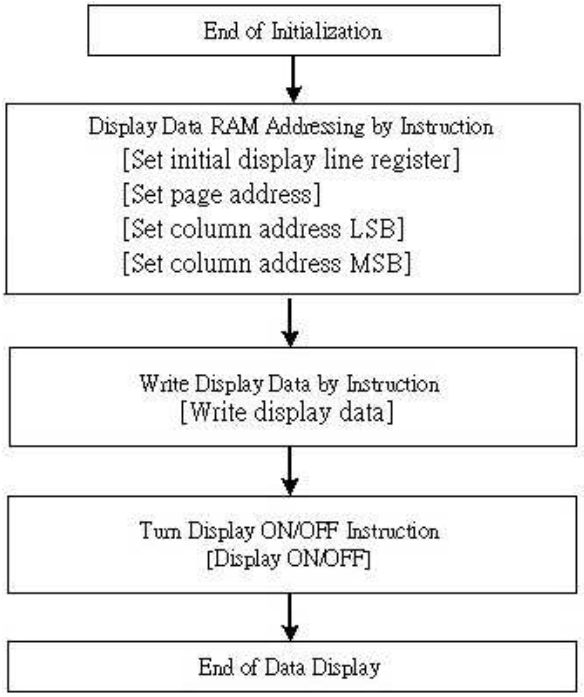
Initializing with the Built-in power supply circuits

b. When the built-in power is not being used immediately after turning on the power:

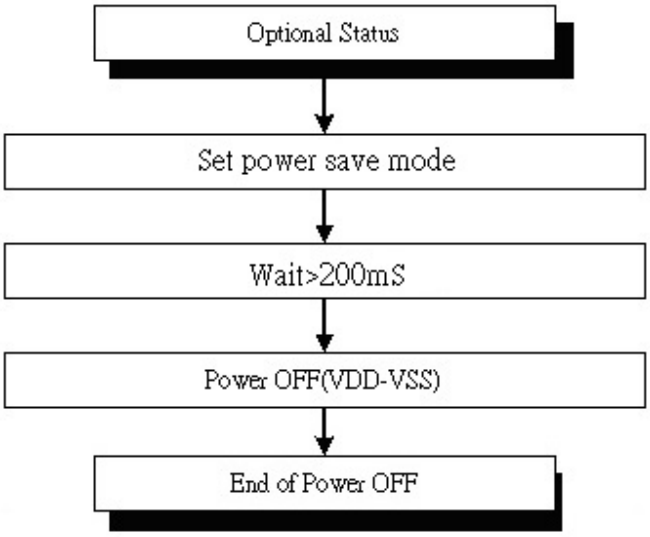


Initializing with the external power supply circuits

(2) Data Display



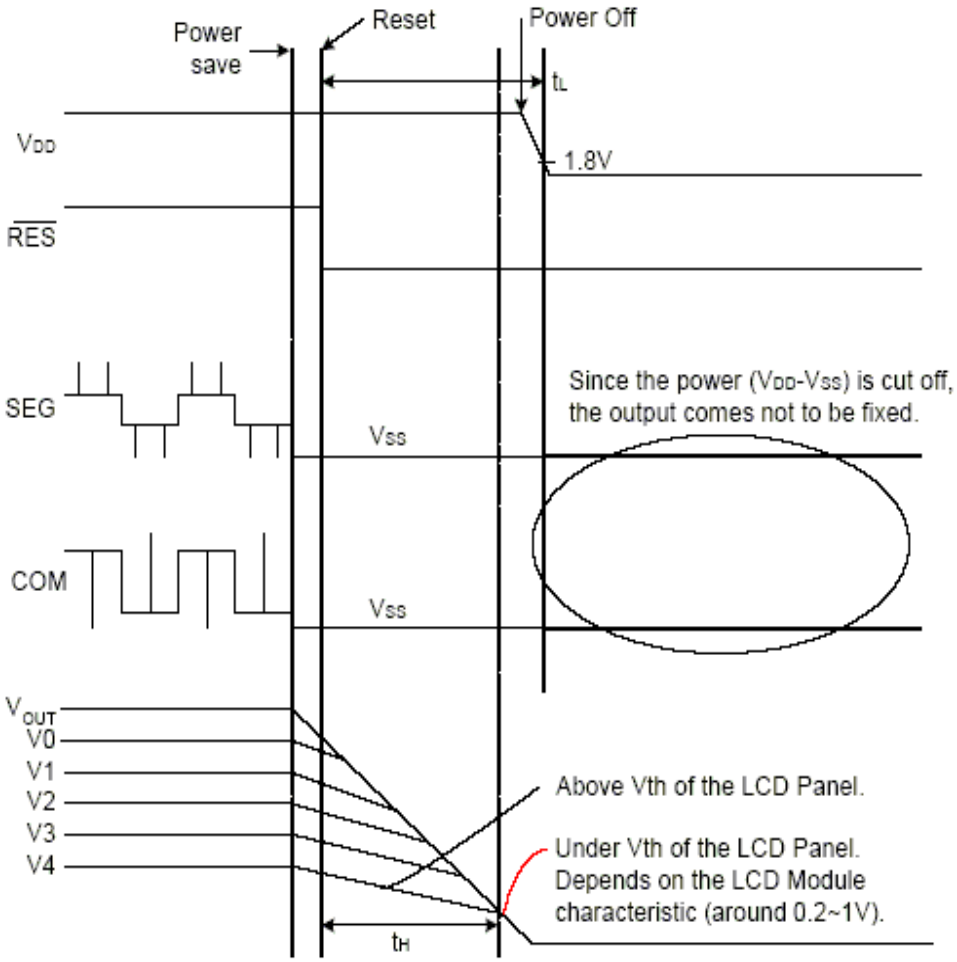
(3) Power OFF



Notes: Reference items
The logic circuit of this IC's power supply VDD - VSS controls the driver of the LCD power supply VSS – V0. So, if the power supply VDD - VSS is cut off when the LCD power supply VSS – V0 has still any residual voltage, the driver (COM/SEG) may output any uncontrolled voltage. When turning off the power, observe the following basic procedures:
After turning off the internal power supply, make sure that the potential V0 ~ V4 has become below the threshold voltage of the LCD panel, and then turn off this IC's power supply (VDD - VSS).

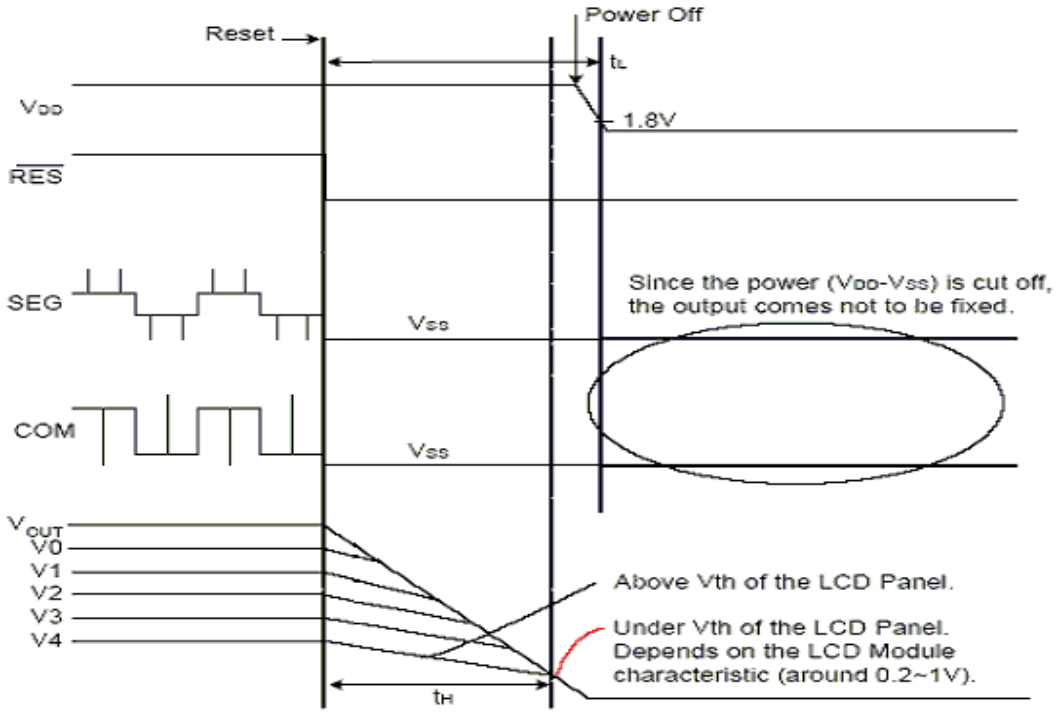
■ Precautions on Turning off the Power

<Turning the power (VDD - VSS) off>
1) Power Save (The LCD powers (V0 - VSS) are off.) → Reset input → Power (VDD - VSS) OFF
• Observe tL > tH.
• When tL < tH, an irregular display may occur.
Set tL on the MPU according to the software. tH is determined according to the external capacity C2 (smoothing capacity of V0 ~ V4) and the driver's discharging capacity.



<Turning the power (VDD - VSS) off : When command control is not possible.>

2) Reset (The LCD powers (VDD - VSS) are off.) → Power (VDD - VSS) OFF
• Observe tL > tH.
• When tL < tH, an irregular display may occur.
For tL, make the power (VDD - VSS) falling characteristics longer or consider any other method. tH is determined according to the external capacity C2 (smoothing capacity of V4 to V0) and the driver's discharging capacity.



<Reference Data>
V0 voltage falling (discharge) time (tH) after the process of operation → power save → reset.
V0 voltage falling (discharge) time (tH) after the process of operation → reset.

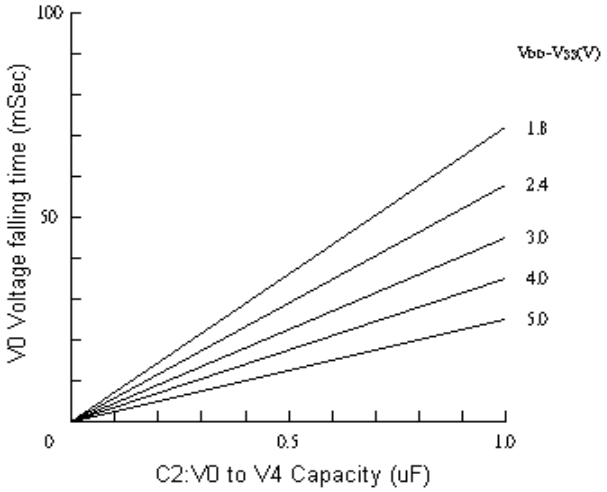
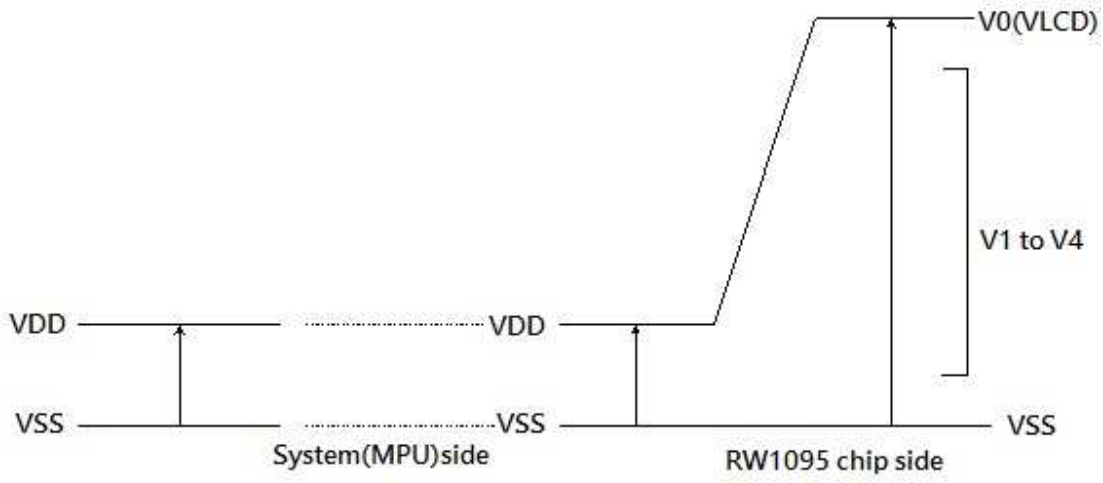


Figure 23

■ ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; see notes 1 and 2.

Parameter		Symbol	Conditions	Unit
Power Supply Voltage		VDD	-0.3 ~ 5.0	V
Power supply voltage (VDD standard)		VDD2	-0.3 ~ 4.0	V
Power supply voltage (VDD standard)		V0, VOUT	-0.3 ~ 18.0	V
Power supply voltage (VDD standard)		V1, V2, V3, V4	V0 to -0.3	V
Operating temperature		TOPR	–40 to +85	℃
Storage temperature	Bare chip	TSTR	–55 to +125	℃



Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
3. Insure that the voltage levels of V1, V2, V3, and V4 are always such that
   Vout ≧ V0 ≧ V1 ≧ V2 ≧ V3 ≧ V4 ≧ Vss

■ DC CHARACTERISTICS

Unless otherwise specified, VSS = 0 V, VDD = 3.0 V ± 10%, Ta = –40 to 85℃

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage (1)		VDD			1.8	—	3.6	V	Vss*1
Operating Voltage (2)		VDD2	(Relative to VSS)		2.4	—	3.6	V	VSS
High-level Input Voltage		VIHC			0.7 x VDD	—	VDD	V	*2
Low-level Input Voltage		VILC			VSS	—	0.3 x VDD	V	*2
High-level Output Voltage		VOHC			0.7 x VDD	—	VDD	V	*3
Low-level Output Voltage		VOLC			VSS	—	0.3 x VDD	V	*3
Input leakage current		ILI	VIN = VDD or VSS		–1.0	—	1.0	μA	*4
Output leakage current		ILO	VIN = VDD or VSS		–3.0	—	3.0	μA	*5
Liquid Crystal Driver ON Resistance		RON	Ta = 25℃ (Relative To VSS)	V0= 13.0 V	—	2.0	3.5	KΩ	SEGn COMn *6
				V0 = 8.0 V	—	3.2	5.4		
Oscillator Frequency	Internal Oscillator	fOSC	1/65 duty	Ta = 25℃ 15 PWM	—	5	6	kHz	*7
	External Input	fCL			—	5	6	kHz	OSC
	Frame frequency	fFRAME			—	77	80.3	Hz	

Item		Symbol	Condition	Rating			Units	Applicable Pin
				Min.	Typ.	Max.		
Internal Power	Input voltage	VDD	(Relative To VSS)	1.8	—	3.6	V	
	Input voltage	VDD2	(Relative To VSS)	2.4	—	3.6	V	
	Supply Step-up output voltage Circuit	VOUT	(Relative To VSS)	—	—	16	V	VOUT
	Supply Regulator output voltage Circuit	VOUT	(Relative To VSS)	6.0	—	18.0	V	VOUT
	Supply Follower output voltage Circuit	V0	(Relative To VSS)	3.3	—	17.1	V	V0 *9
	Base voltage	VREG	Ta = 25℃ -0.05%/℃	2.07	2.1	2.13	V	

■ Dynamic Consumption Current :

During Display, with the Internal Power Supply OFF Current consumed by total ICs when an external power supply is used .

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	IVSS	VDD = 3.0 V, V0 – VSS = 9.0 V	—	300	400	μA	*8
Power Save mode	IVSS	Ta = 25℃	—	0.01	2	μA	

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. Power Save mode. During power down all static currents are switched off.
4. If external V_{LCDIN}, the display load current is not transmitted to I_{DD}.
5. V_{OUT} external voltage applied to VLCDIN pin; VLCDIN disconnected from VLCDOUT (no connect)

References for items market with *

*1 While a broad range of operating voltages is guaranteed, performance cannot be guaranteed if there are sudden fluctuations to the voltage while the MPU is being accessed.

*2 The A0, D0 to D5, D6 (SI), D7 (SCL), XRD (E),XWR (RW), CS1B, C86, OSC, PSB, XDOF, RSTP ,and MODE terminals.

*3 The D0 to D7, and OSC terminals.

*4 The A0 (RS),XRD (E), XWR (R/W), CS1B, C86, OSC, PSB, XDOF, RSTP ,and MODE terminals.

*5 Applies when the D0 to D5, D6 (SI), D7 (SCL) terminals are in a high impedance state.

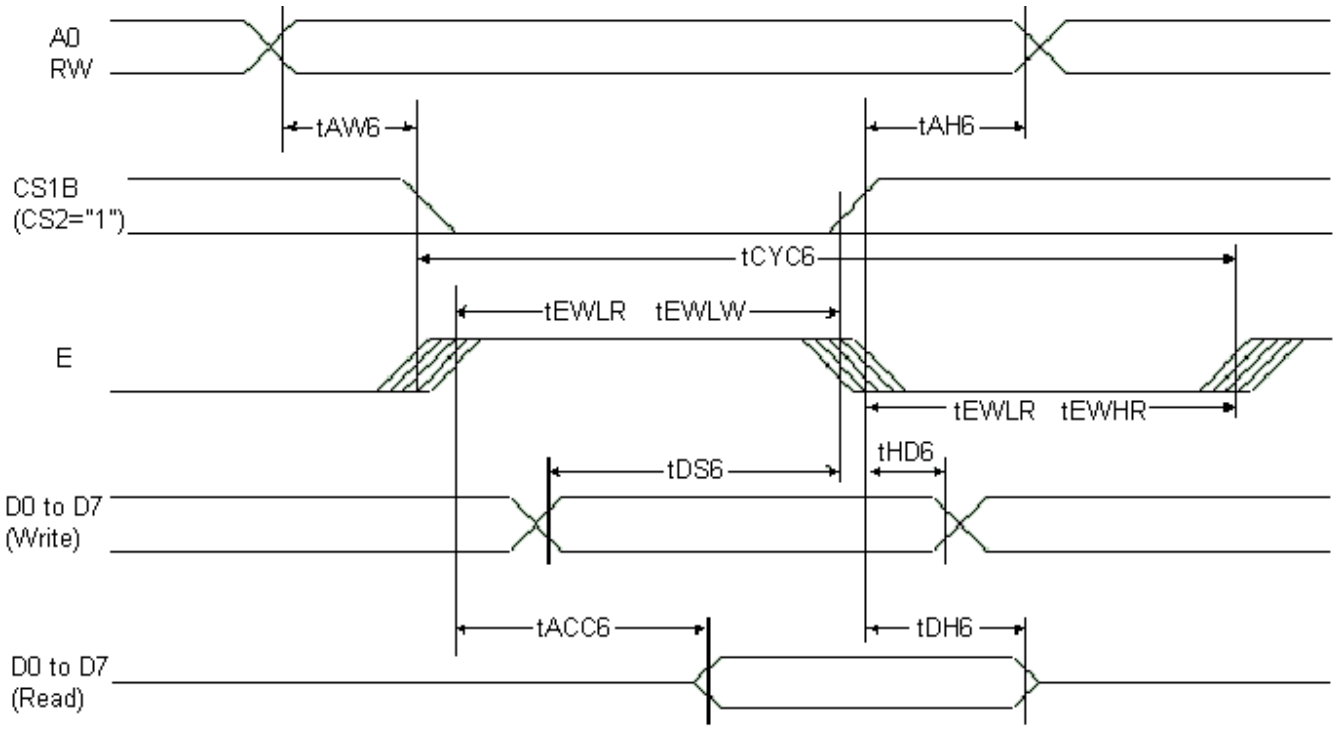
*6 These are the resistance values for when a 0.1 V voltage is applied between the output terminal SEGn or COMn and the various power supply terminals (V1, V2, V3, and V4). These are specified for the operating voltage range. RON = 0.1 V /ΔI (Where ΔI is the current that flows when 0.1 V is applied while the power supply is ON.)

*7 The relationship between the oscillator frequency and the frame rate frequency.

*8,9 It indicates the current consumed on ICs alone when the internal oscillator circuit and display are turned on.

■ TIMING CHARACTERISTICS

(36) System Bus Read/Write Characteristics 1(For the 6800 Series MPU)



(VDD = 3.3 V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		240	—	
Enable L pulse width (WRITE)	E	tEWLW		80	—	
Enable H pulse width (WRITE)		tEWHW		80	—	
Enable L pulse width (READ)	E	tEWLR		80	—	
Enable H pulse width (READ)		tEWHR		140		
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	70	
READ Output disable time		tOH6	CL = 100 pF	5	50	

(VDD = 2.7V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		400	—	
Enable L pulse width (WRITE)	E	tEWLW		220	—	
Enable H pulse width (WRITE)		tEWHW		180	—	
Enable L pulse width (READ)	E	tEWLR		220	—	
Enable H pulse width (READ)		tEWHR		180	—	
WRITE Data setup time	D0 to D7	tDS6		40	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	140	
READ Output disable time		tOH6	CL = 100 pF	10	100	

Table 29

(VDD =1.8V , Ta =25℃)

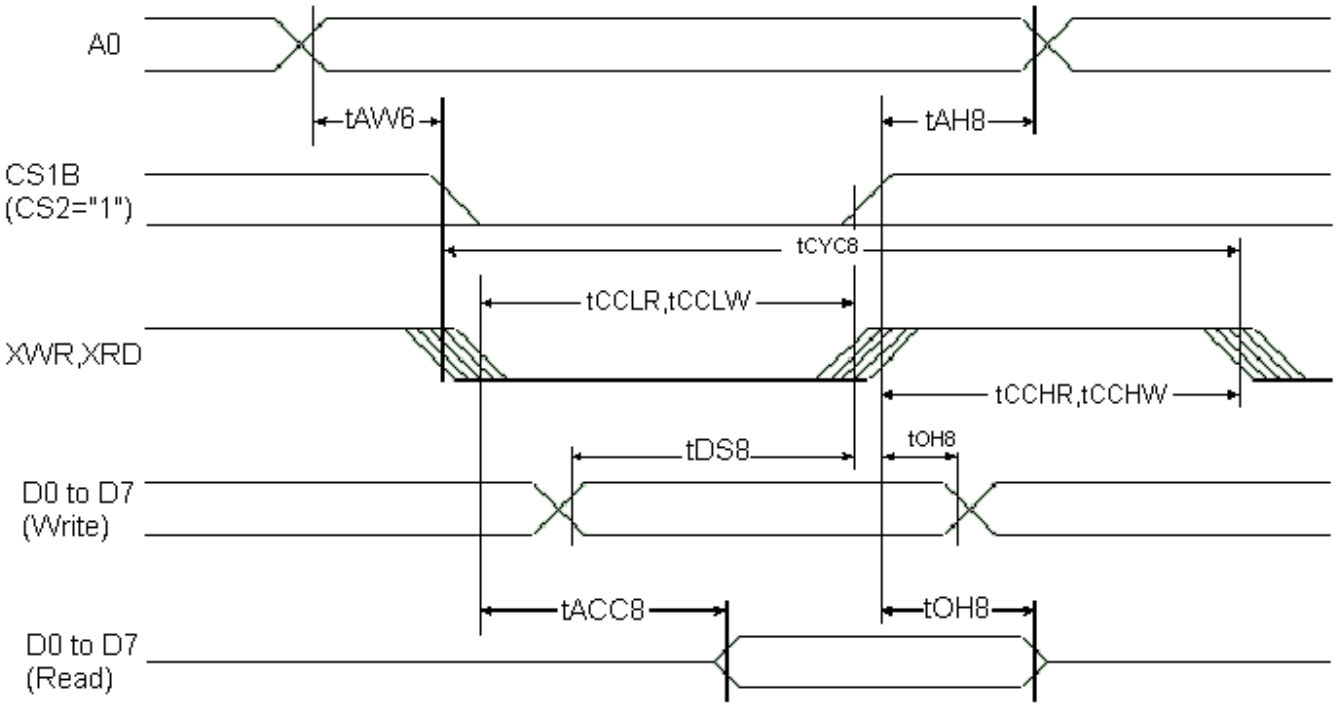
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH6		0	—	ns
Address setup time		tAW6		0	—	
System cycle time		tCYC6		640	—	
Enable L pulse width (WRITE)	E	tEWLW		360	—	
Enable H pulse width (WRITE)		tEWHW		280	—	
Enable L pulse width (READ)	E	tEWLR		360	—	
Enable H pulse width (READ)		tEWHR		280	—	
WRITE Data setup time	D0 to D7	tDS6		80	—	
WRITE Address hold time		tDH6		0	—	
READ access time		tACC6	CL = 100 pF	—	240	
READ Output disable time		tOH6	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC6 – tEWLW – tEWHW) for (tr + tf) ≦ (tCYC6 – tEWLR – tEWHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tEWLW and tEWLR are specified as the overlap between CS1B being “L” and E.

(37) System Bus Read/Write Characteristics 1(For the 8080 Series MPU)



(VDD = 3.3V , Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

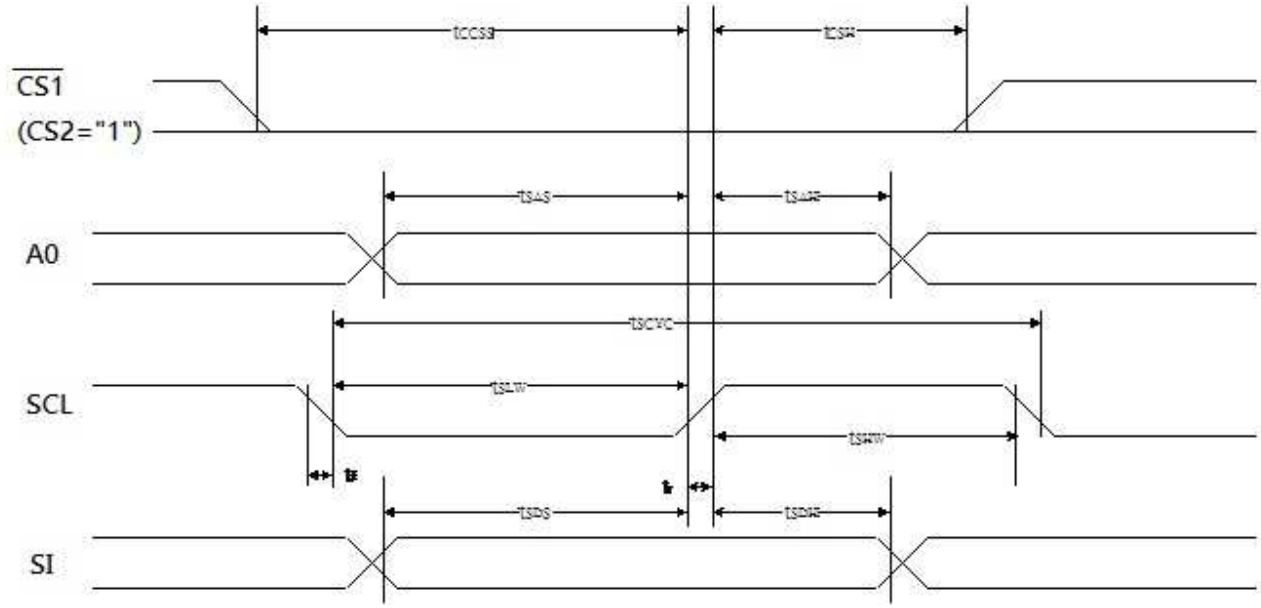
Table 26

(VDD = 1.8V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.
*2 All timing is specified using 20% and 80% of VDD as the reference.
*3 tCCLW and tCCLR are specified as the overlap between CS1B being “L” (CS2 = “H”) and XWR and XRD being at the “L” level.

➢ **The Serial Interface**



(VDD = 3.3V, Ta =25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	Tscyc		50	—	ns
SCL “H” pulse width		Tshw		25	—	
SCL “L” pulse width		TSLW		25	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

(VDD =2.7V , Ta =25℃)

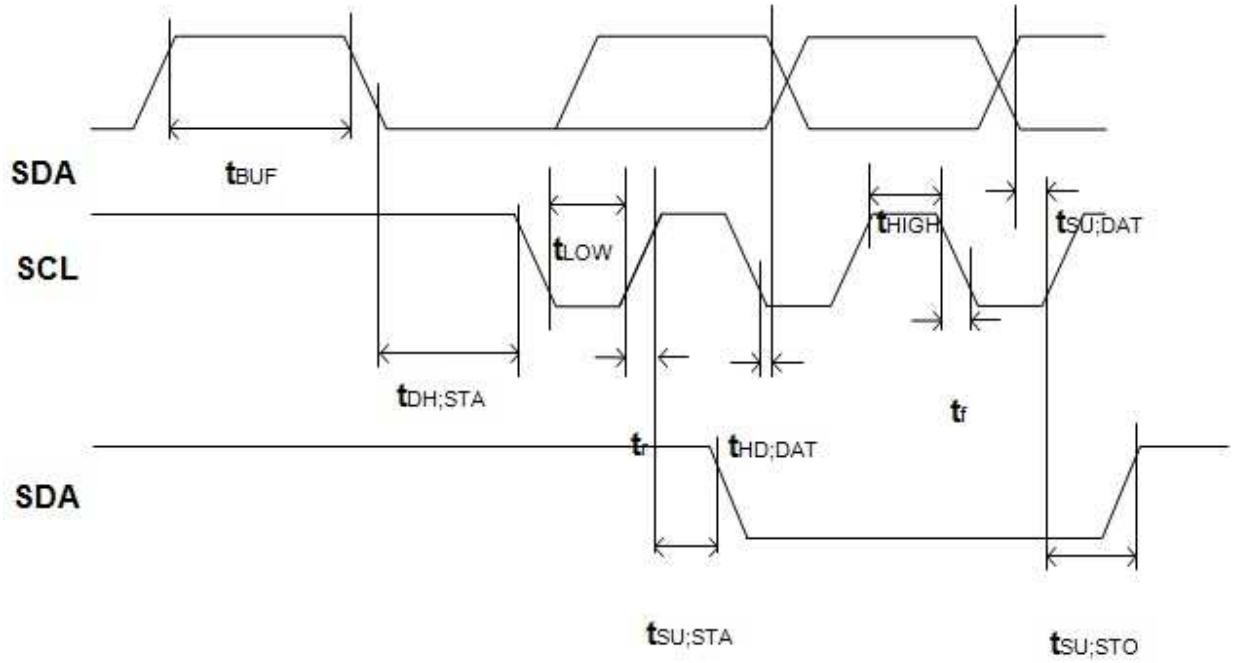
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	Tscyc		100	—	ns
SCL “H” pulse width		TSHW		50	—	
SCL “L” pulse width		TSLW		50	—	
Address setup time	A0	TSAS		30	—	
Address hold time		TSAH		20	—	
Data setup time	SI	TSDS		30	—	
Data hold time		TSDH		20	—	
CS-SCL time	CS	TCSS		30	—	
CS-SCL time		TCSH		60	—	

(VDD = 1.8V , Ta = 25℃)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	TSCYC		200	—	ns
SCL “H” pulse width		TSHW		80	—	
SCL “L” pulse width		TSLW		80	—	
Address setup time	A0	TSAS		60	—	
Address hold time		TSAH		30	—	
Data setup time	SI	TSDS		60	—	
Data hold time		TSDH		30	—	
CS-SCL time	CS	TCSS		40	—	
CS-SCL time		TCSH		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
*2 All timing is specified using 20% and 80% of VDD as the standard.

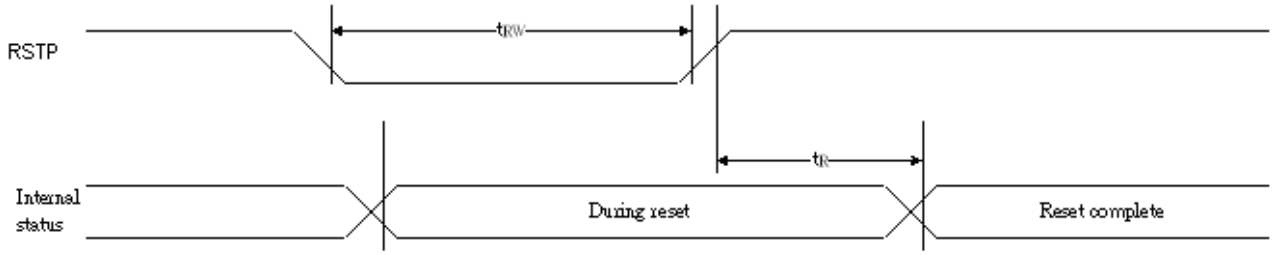
➢ **The IIC Interface**



(Ta = 25℃)

Item	Signal	Symbol	Condition	VDD=1.8 to 2.7V Rating		VDD=2.7 to 3.6V Rating		Units
				Min.	Max.	Min.	Max.	
SCL clock frequency	SCL	f_{SCLK}	—	DC	400	DC	400	KHz
SCL clock low period		t_{LOW}		1.3	—	1.3	—	us
SCL clock high period		t_{HIGH}		0.6	–	0.6	–	
Data set-up time	SDA	$t_{SU;DAT}$	—	180	–	80	–	ns
Data hold time		$t_{HD:DAT}$		0	0.9	0	0.9	us
SCL,SDA rise time	SCL, SDA	t_r	—	20+0.1C_b	300	20+0.1C_b	300	ns
SCL,SDA fall time		t_f		20+0.1C_b	300	20+0.1C_b	300	
Capacitive load represent by each bus line		C_b	—	–	400	–	400	pf
Setup time for a repeated START condition	SDA	$t_{SU;STA}$	—	0.6	–	0.6	–	us
Start condition hold time		$t_{HD;STA}$	—	0.6	–	0.6	–	us
Setup time for STOP condition		$t_{SU;STO}$	—	0.6	–	0.6	–	us
Bus free time between a Stop and START condition	SCL	t_{BUF}	—	1.3	–	1.3	–	us

■ RESET TIMING



(VDD = 3.3V , Ta = –40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1	us
Reset “L” pulse width	RESB	tRW		1	—	—	us

(VDD = 2.7V , Ta = –40 to 85℃)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.5	us
Reset “L” pulse width	RESB	tRW		1.5	—	—	us

(VDD = 1.8V , Ta = –40 to 85℃)

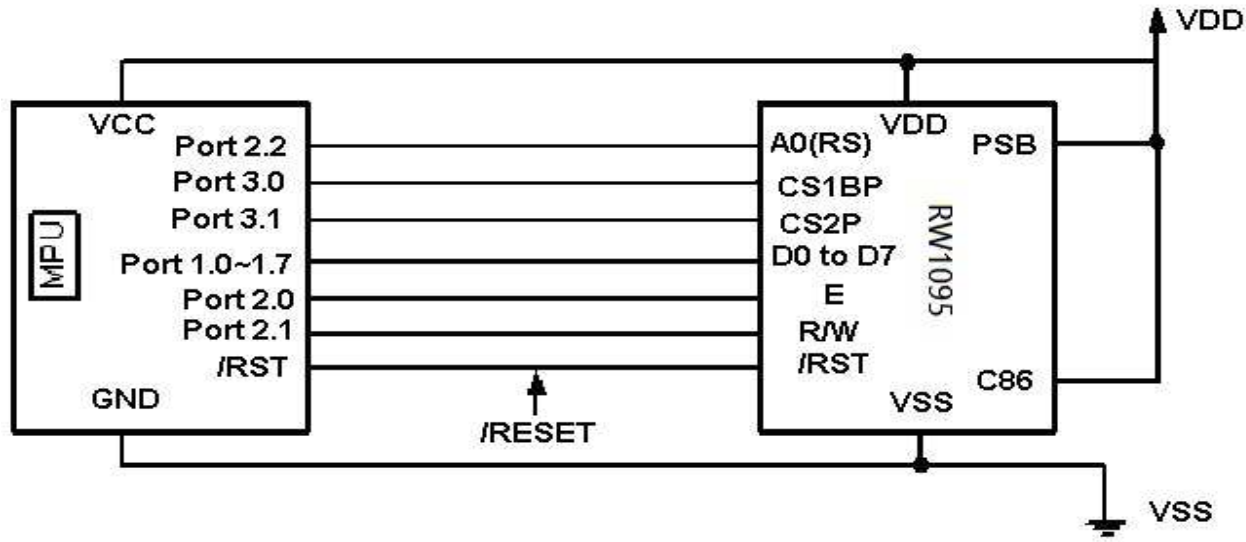
Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset “L” pulse width	RESB	tRW		2.0	—	—	us

■ THE MPU INTERFACE (REFERENCE EXAMPLES)

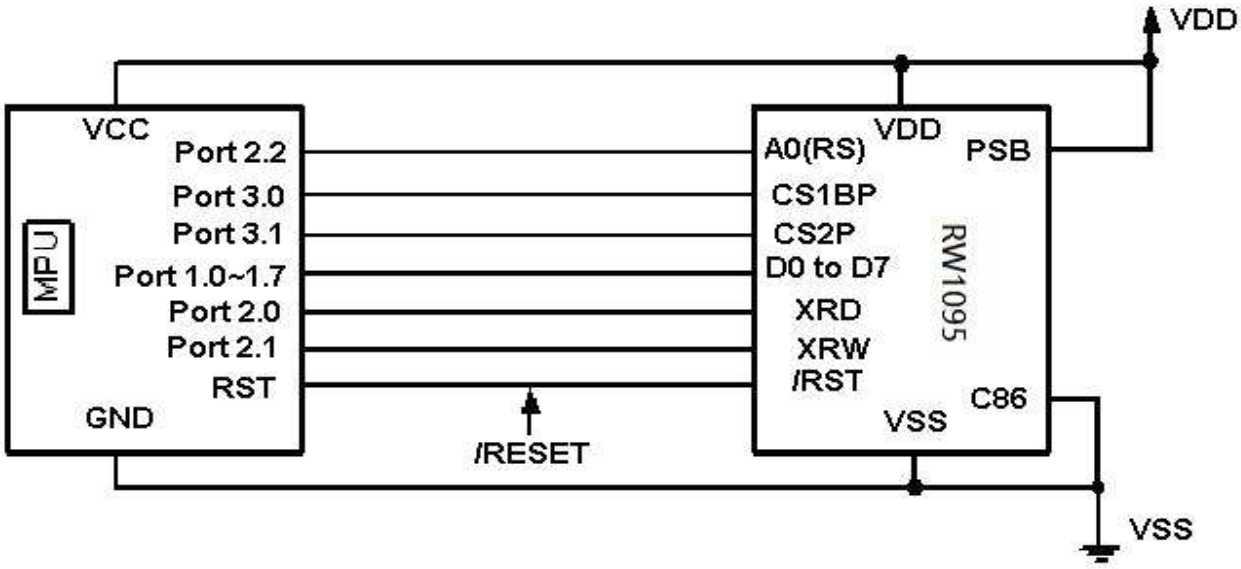
The RW1095 Series can be connected to either 60X86 Series MPUs or to 6800 Series MPUs. Moreover, using the serial interface it is possible to operate the RW1095 series chips with fewer signal lines.

The display area can be enlarged by using multiple RW1095 Series chips. When this is done, the chip select signal can be used to select the individual Ics to access.

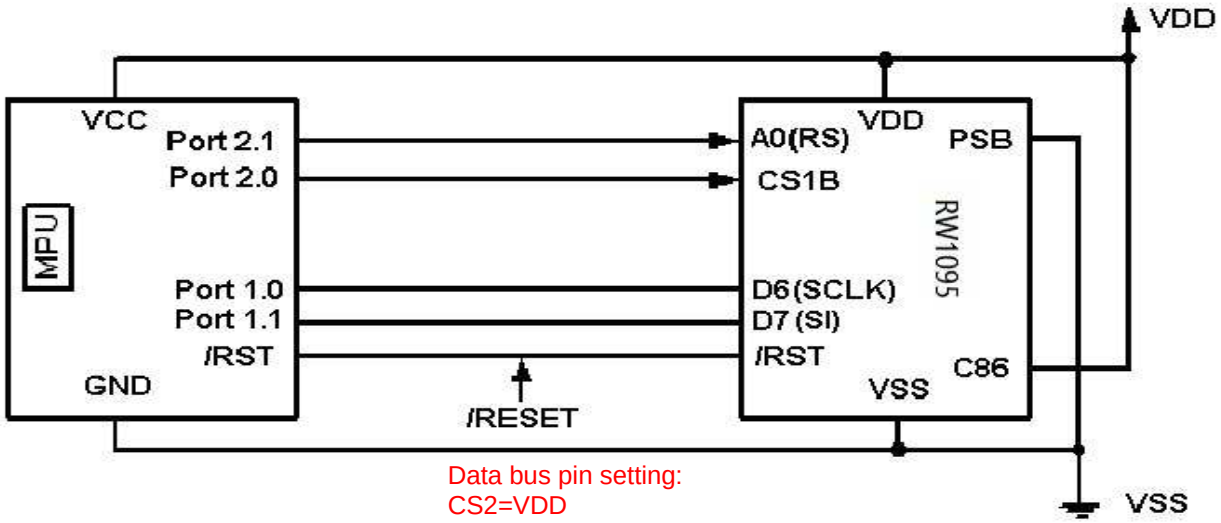
(1) 6800 Series MPUs(PSB="H",C86="H")



(2) 8080 Series MPUs(PSB="H",C86="L")

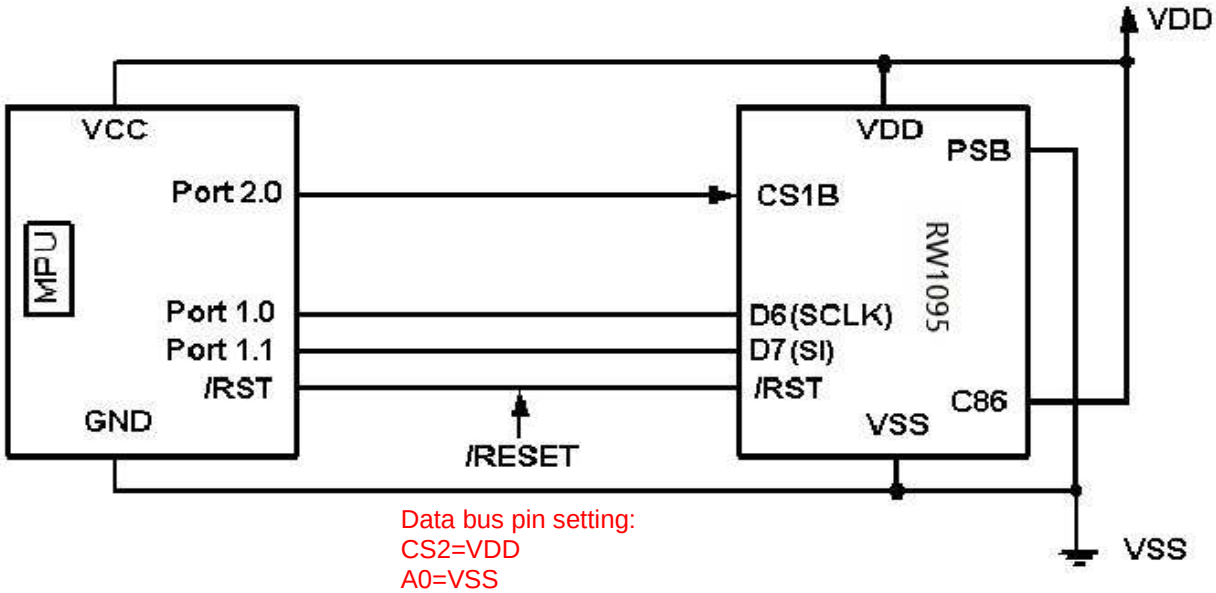


(3) 4-SPI Interface (PSB="L",C86="H")



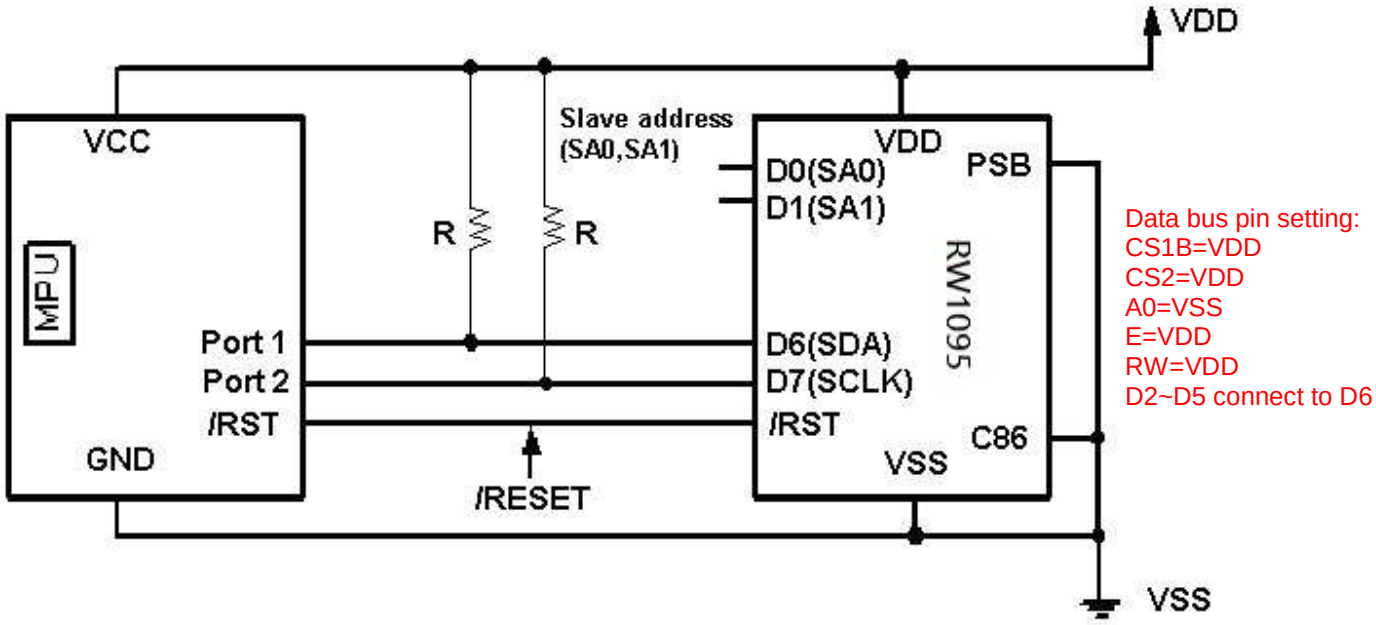
Data bus pin setting:
CS2=VDD
E=VDD
RW=VDD
D2~D5 =VDD

(4) 3-SPI Interface (PSB="L",C86="H")



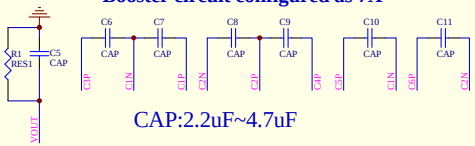
Data bus pin setting:
CS2=VDD
A0=VSS
E=VDD
RW=VDD
D2~D5 =VDD

(5) IIC Interface(PSB="L",C86="L")



Booster Circuit

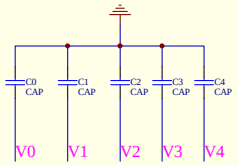
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

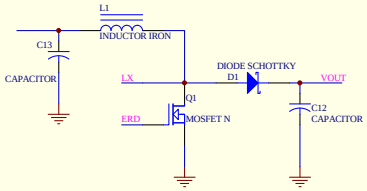
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



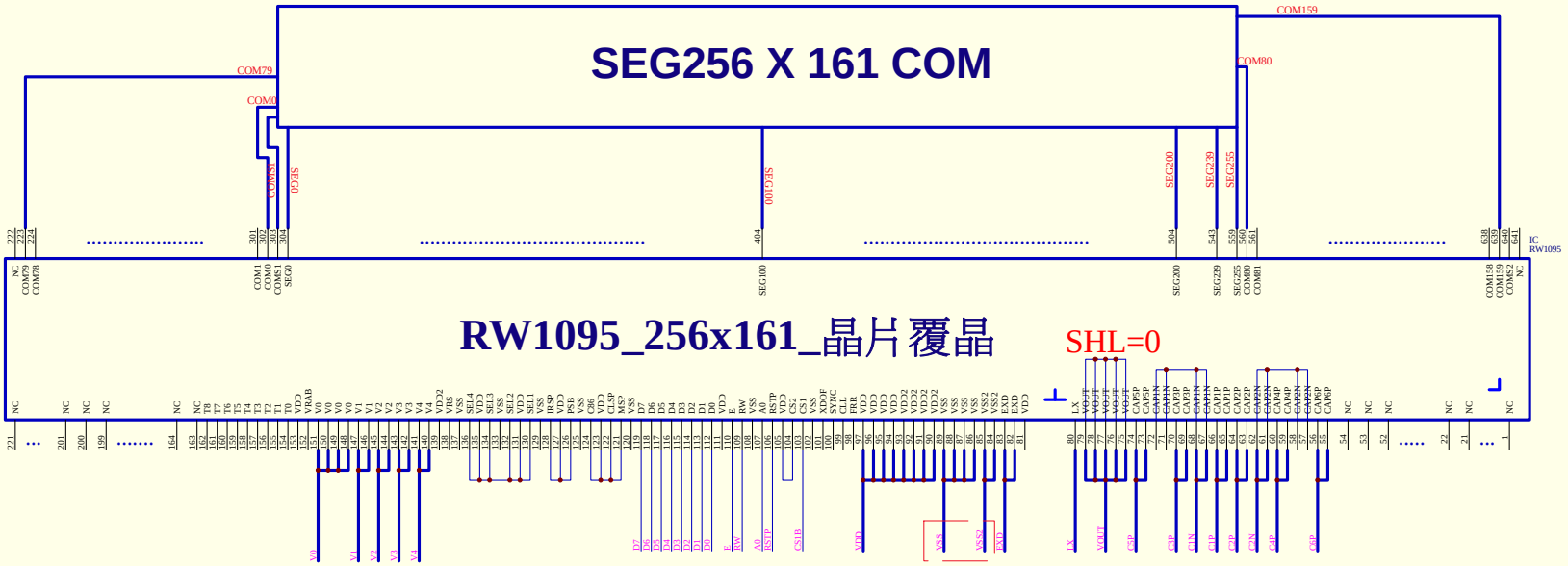
CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.



VSS and VSS2 must be connected together at FPC side

IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface	
0	0	IIC	
0	1	3/4 SPI	
1	0	8bit_8080	
1	1	8bit_6800	← Current setting

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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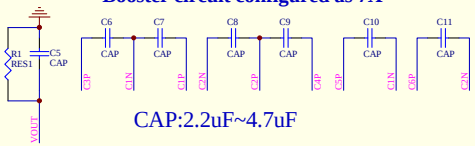
Booster Circuit

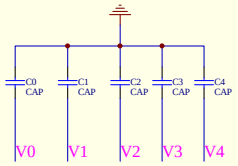
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

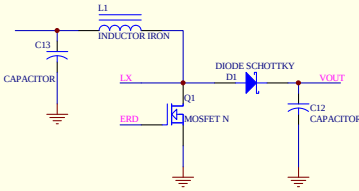
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



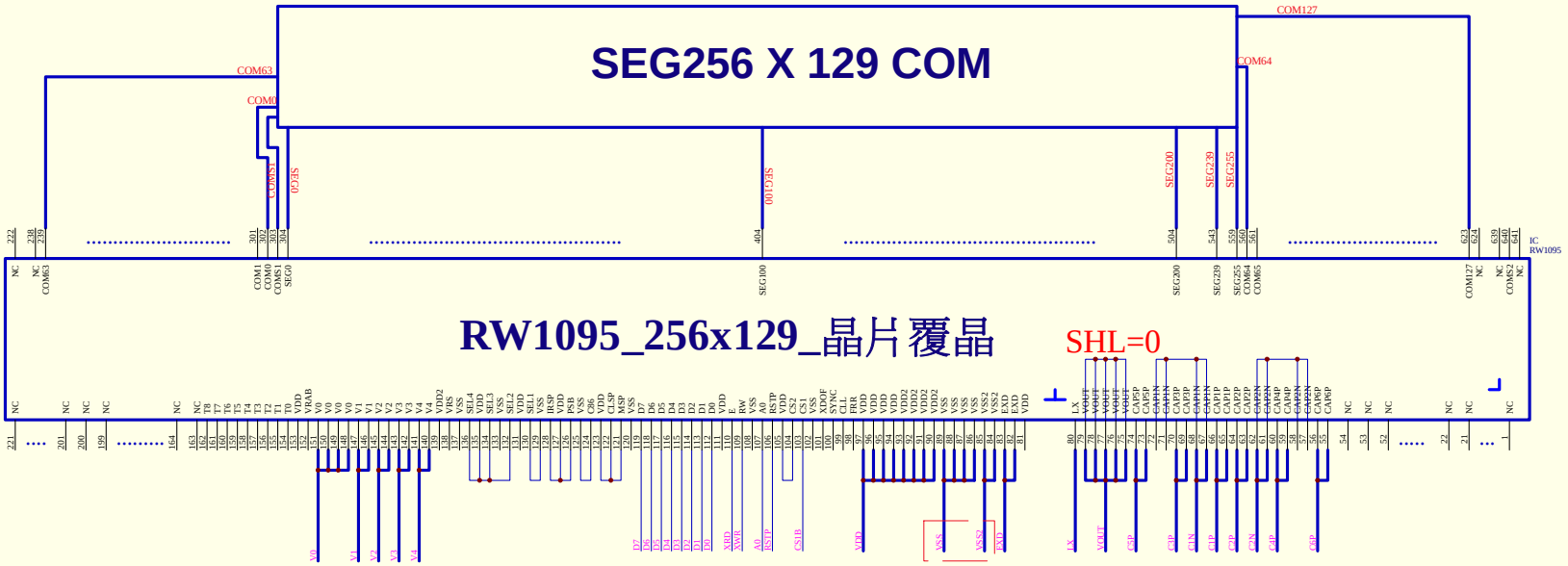
CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8bit_8080
1	1	8bit_6800

← Current setting

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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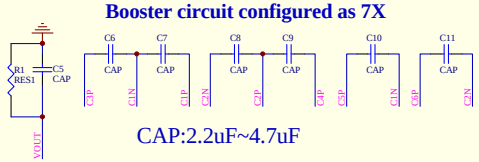
Booster Circuit

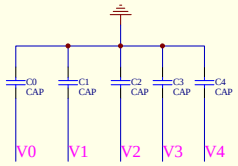
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

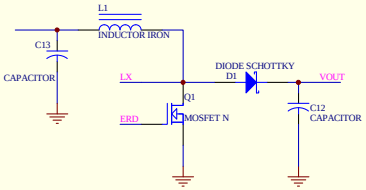
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



CAP:2.2uF~4.7uF

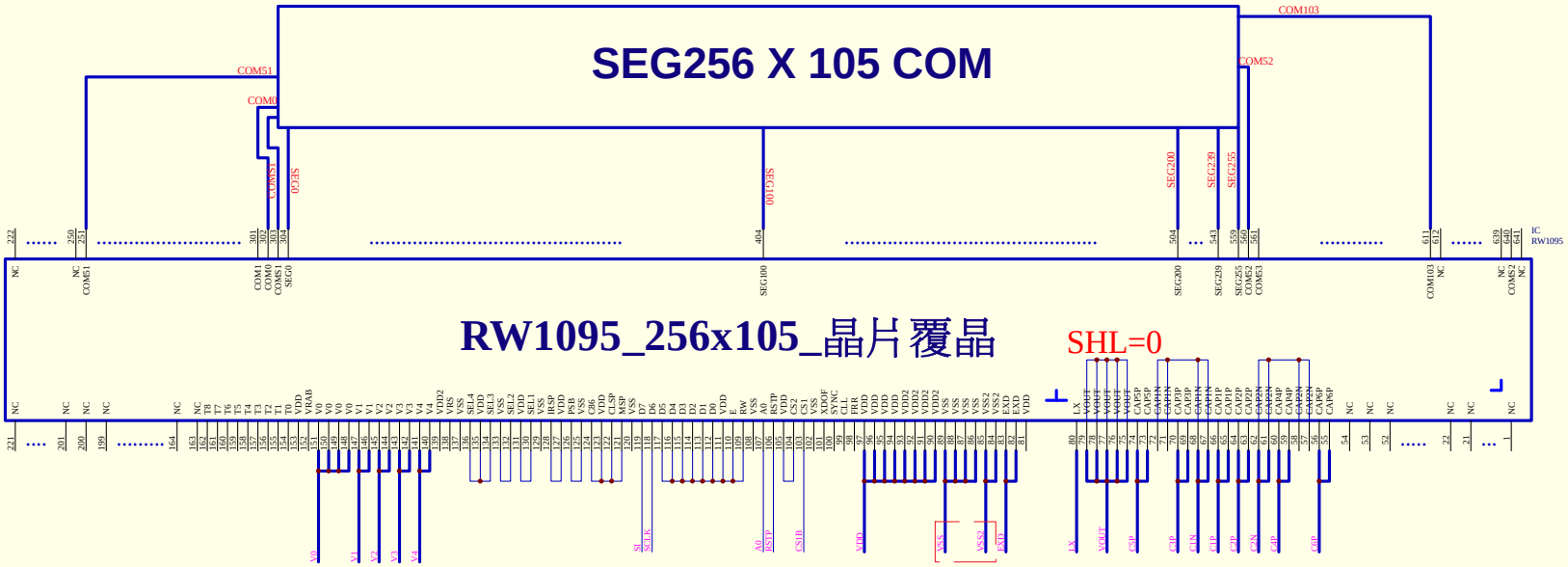
Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.

SEG256 X 105 COM



VSS and VSS2 must be connected together at FPC side

IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface	
0	0	IIC	
0	1	3/4 SPI	← Current setting
1	0	8bit_8080	
1	1	8bit_6800	

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLk	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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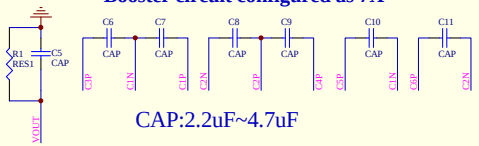
Booster Circuit

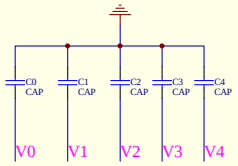
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

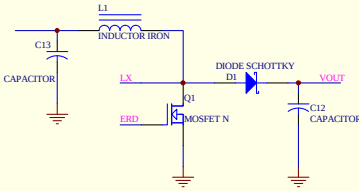
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



CAP:2.2uF~4.7uF

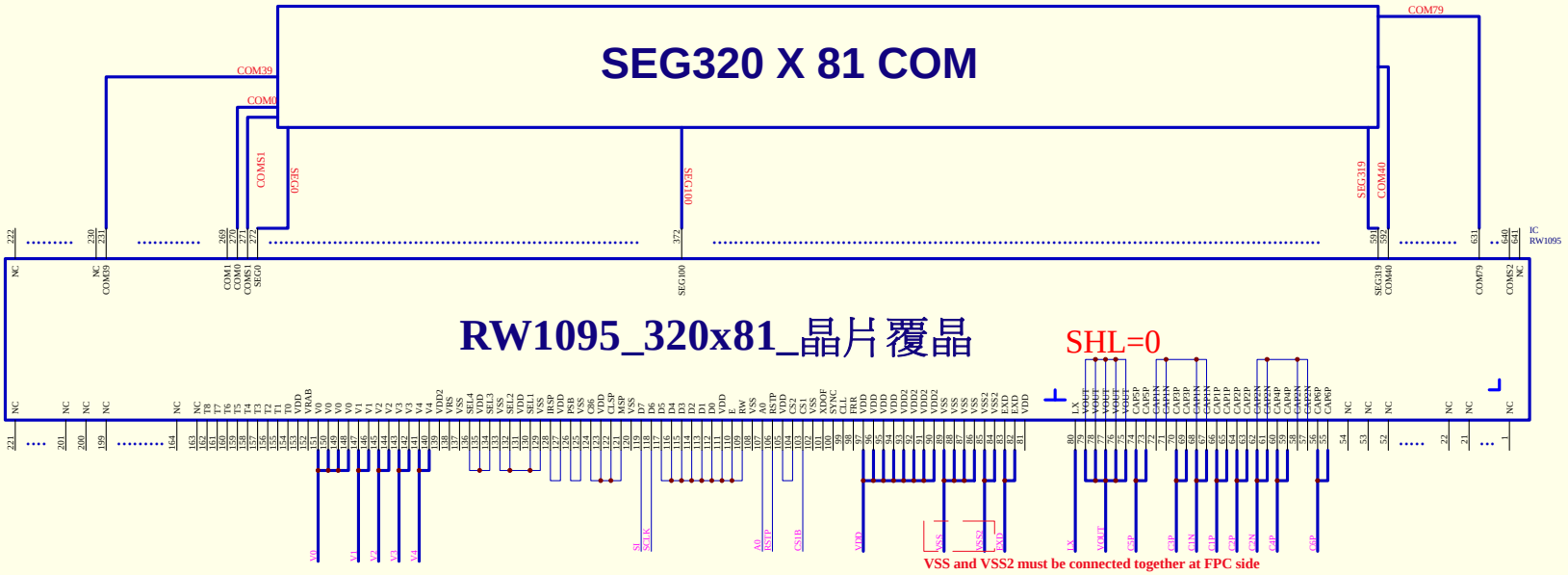
Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.

SEG320 X 81 COM



VSS and VSS2 must be connected together at FPC side

IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface	
0	0	IIC	
0	1	3/4 SPI	← Current setting
1	0	8bit_8080	
1	1	8bit_6800	

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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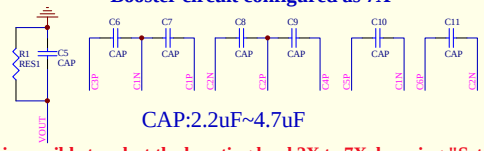
Booster Circuit

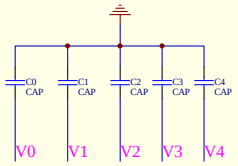
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

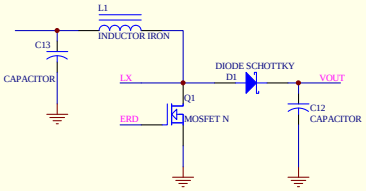
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



CAP:2.2uF~4.7uF

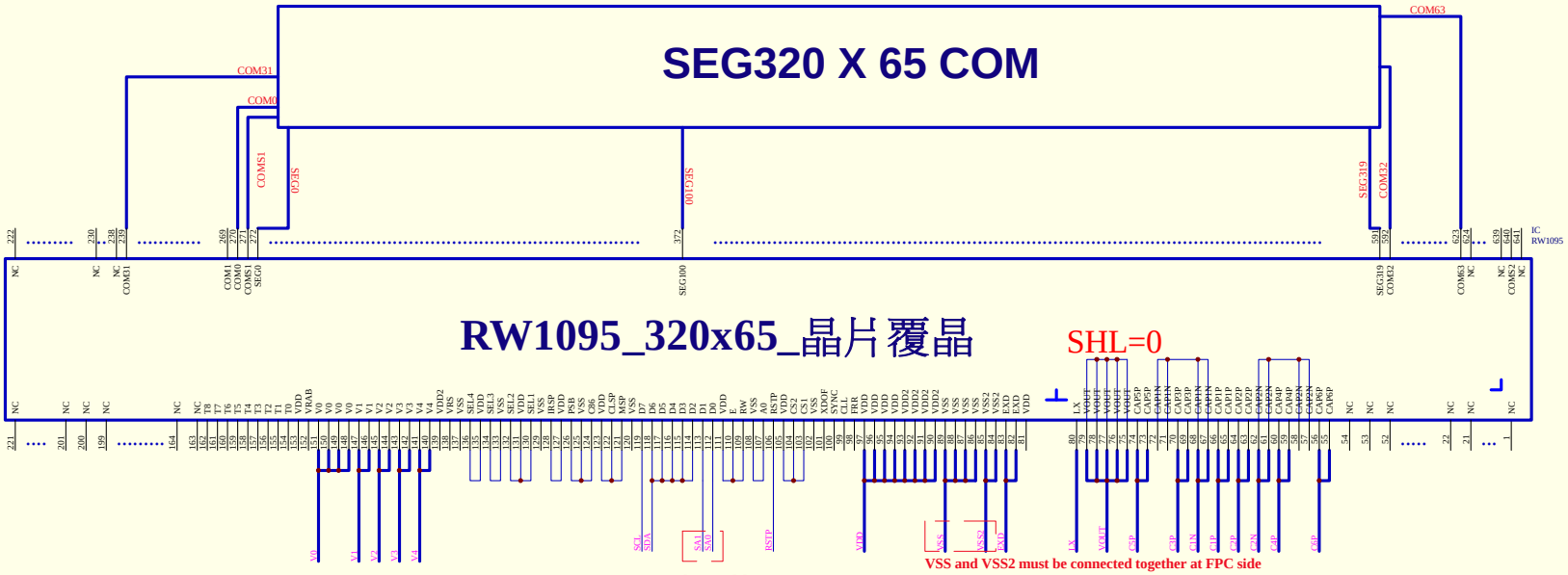
Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.

SEG320 X 65 COM



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface	
0	0	IIC	← Current setting
0	1	3/4 SPI	
1	0	8bit_8080	
1	1	8bit_6800	

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

SA1	SA0	Slave address
0	0	0x78
0	1	0x7a
1	0	0x7c
1	1	0x7e

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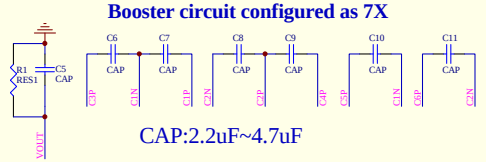
Booster Circuit

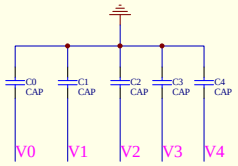
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

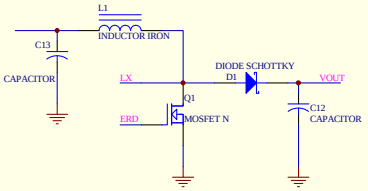
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



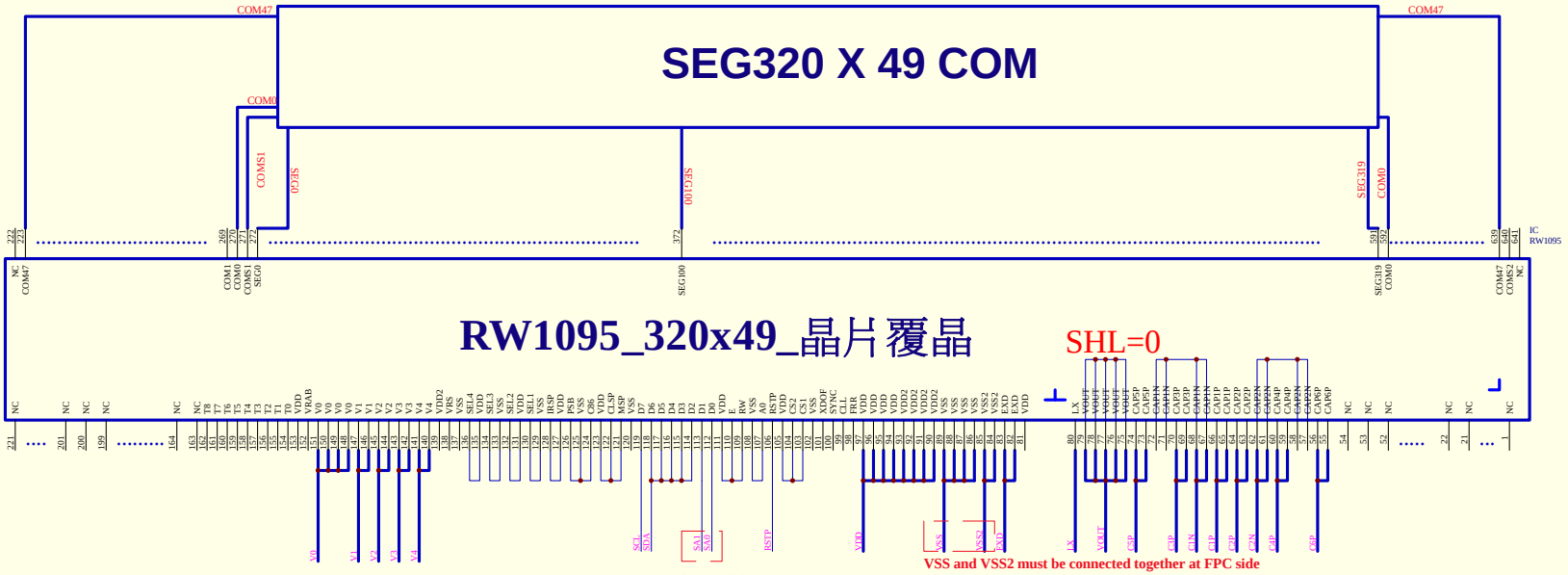
CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8bit_8080
1	1	8bit_6800

← Current setting

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

SA1	SA0	Slave address
0	0	0x78
0	1	0x7a
1	0	0x7c
1	1	0x7e

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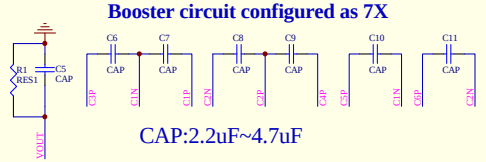
Booster Circuit

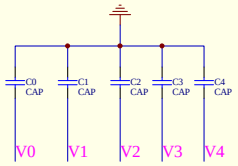
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

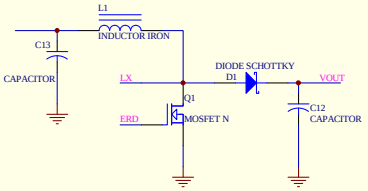
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



CAP:2.2uF~4.7uF

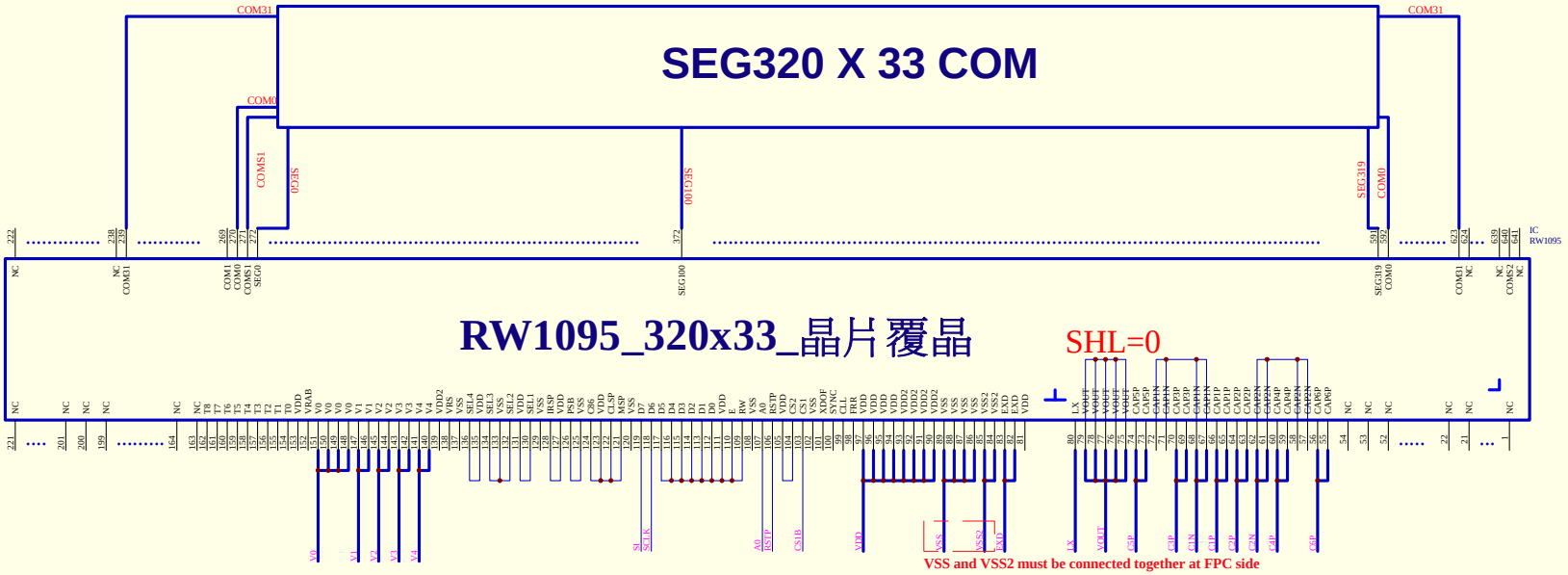
Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.

SEG320 X 33 COM



VSS and VSS2 must be connected together at FPC side

IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI ← Current setting
1	0	8bit_8080
1	1	8bit_6800

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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Date: 22-Sep-2014		Sheet of	
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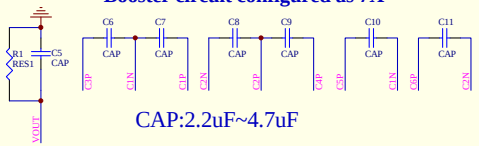
Booster Circuit

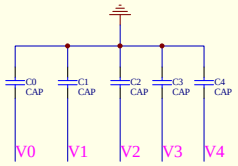
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

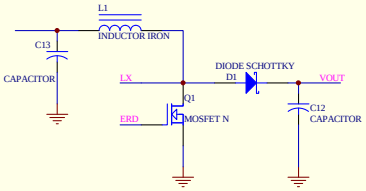
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



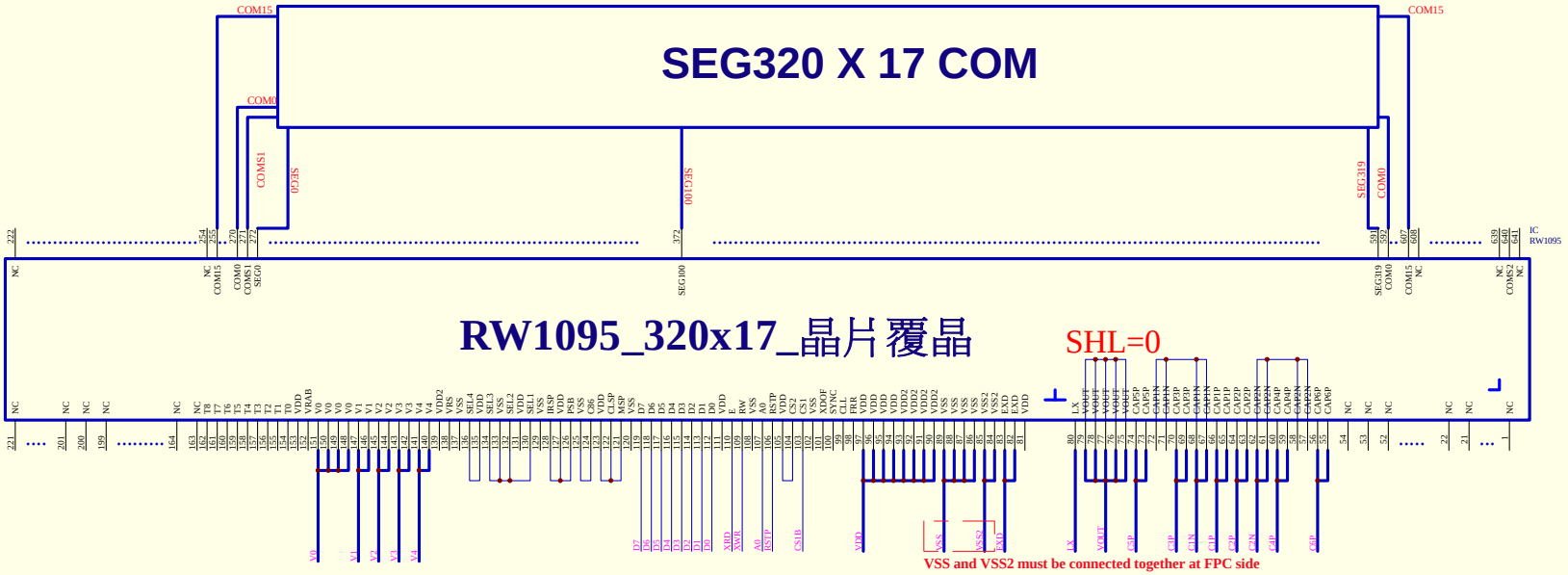
CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8bit_8080
1	1	8bit_6800

← Current setting

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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Size: C	Number: RW1095_320x17	Revision: A	
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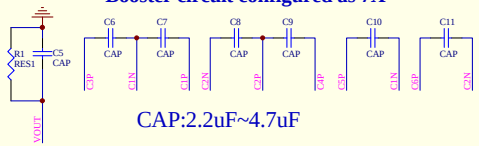
Booster Circuit

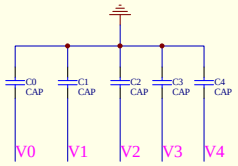
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

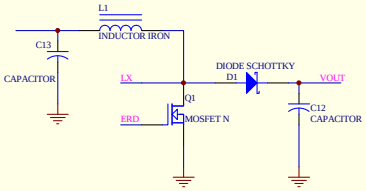
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



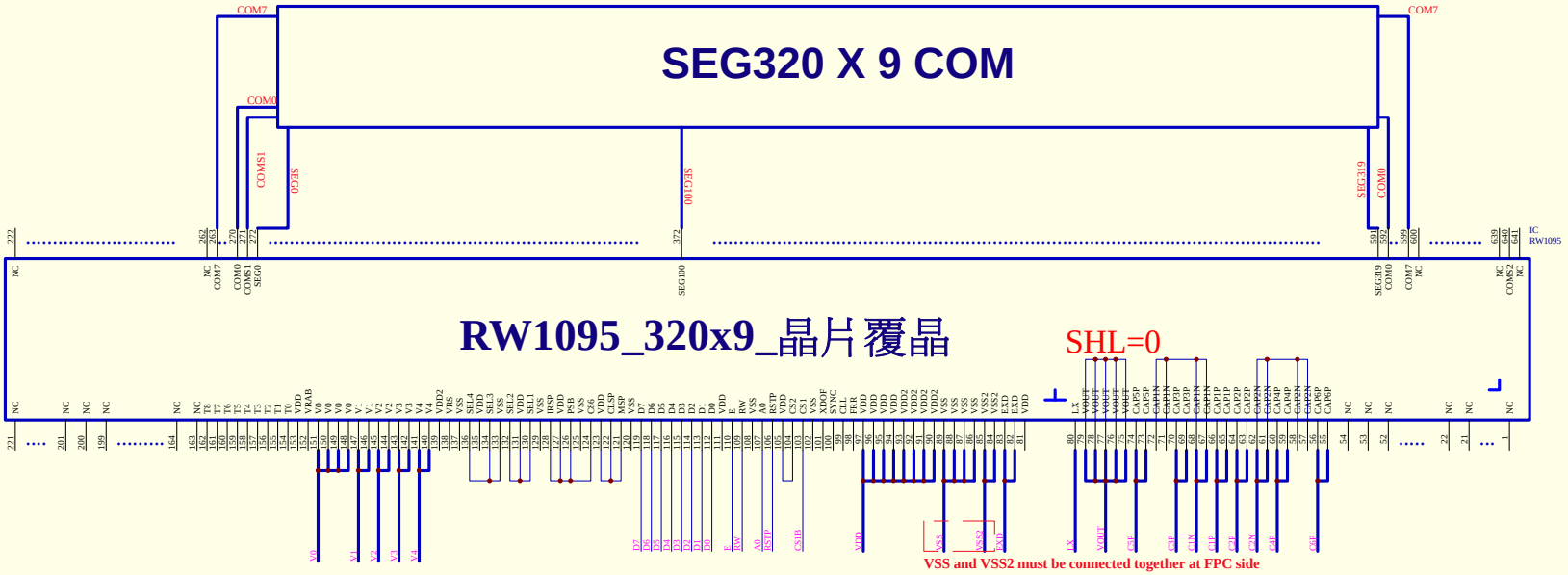
CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



Q1:2N7002K
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8bit_8080
1	1	8bit_6800

← Current setting

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
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4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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Size: C	Number: RW1095_320x9	Revision: A	
Date: 22-Sep-2014	Sheet of		
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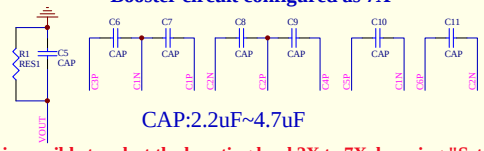
Booster Circuit

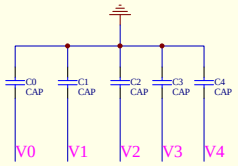
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

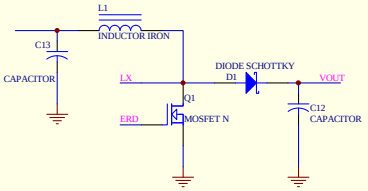
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



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C12:1uF/25V~4.7uF/25V
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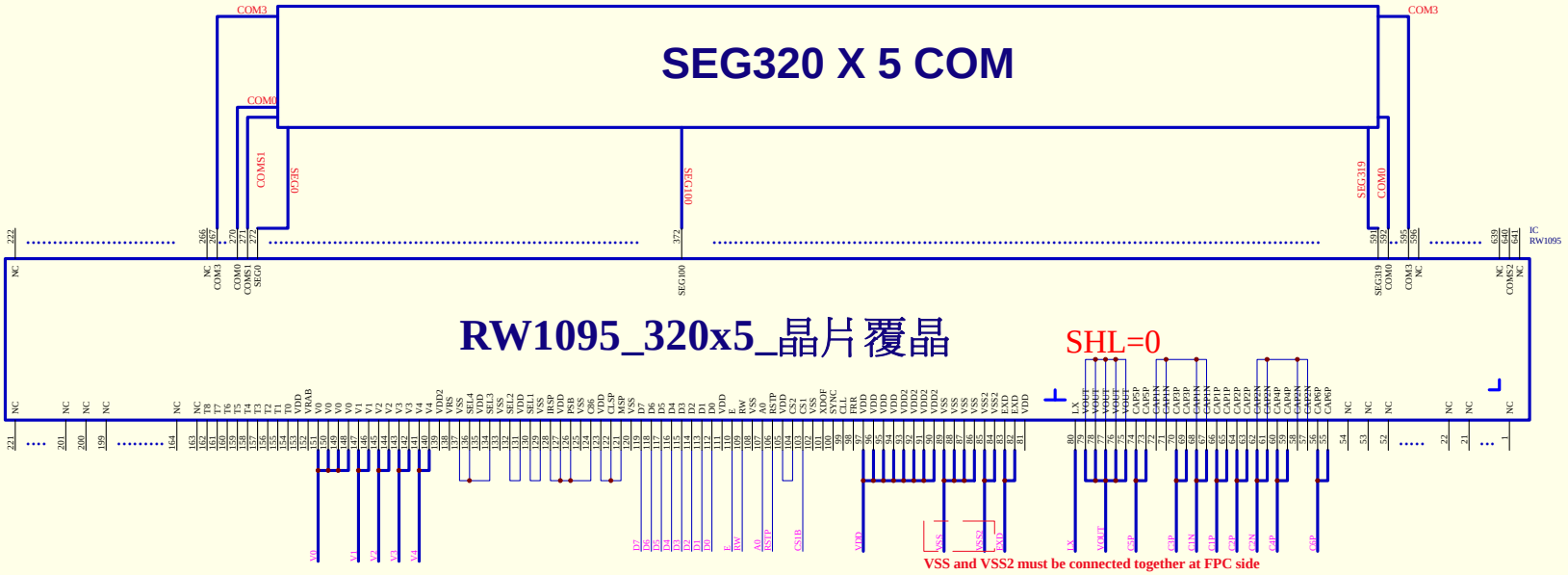
The capacitors of booster circuit must be removed when inductot type regulator circuit is used.



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface
0	0	IIC
0	1	3/4 SPI
1	0	8bit_8080
1	1	8bit_6800

← Current setting

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
3SPI	CS1B	VDD	VSS	VDD	VDD	SI	SCLK	VDD
4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

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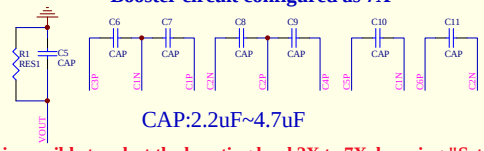
Booster Circuit

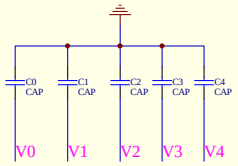
Booster circuit configured as 7X



CAP:2.2uF~4.7uF

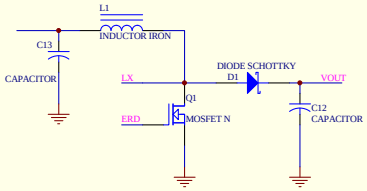
It is possible to select the boosting level 2X to 7X by using "Set DC-DC Set-up" instruction when external booster circuit is configured as 7X

Regulator/Follower Circuit



CAP:2.2uF~4.7uF

Inductor Type Regulator Circuit



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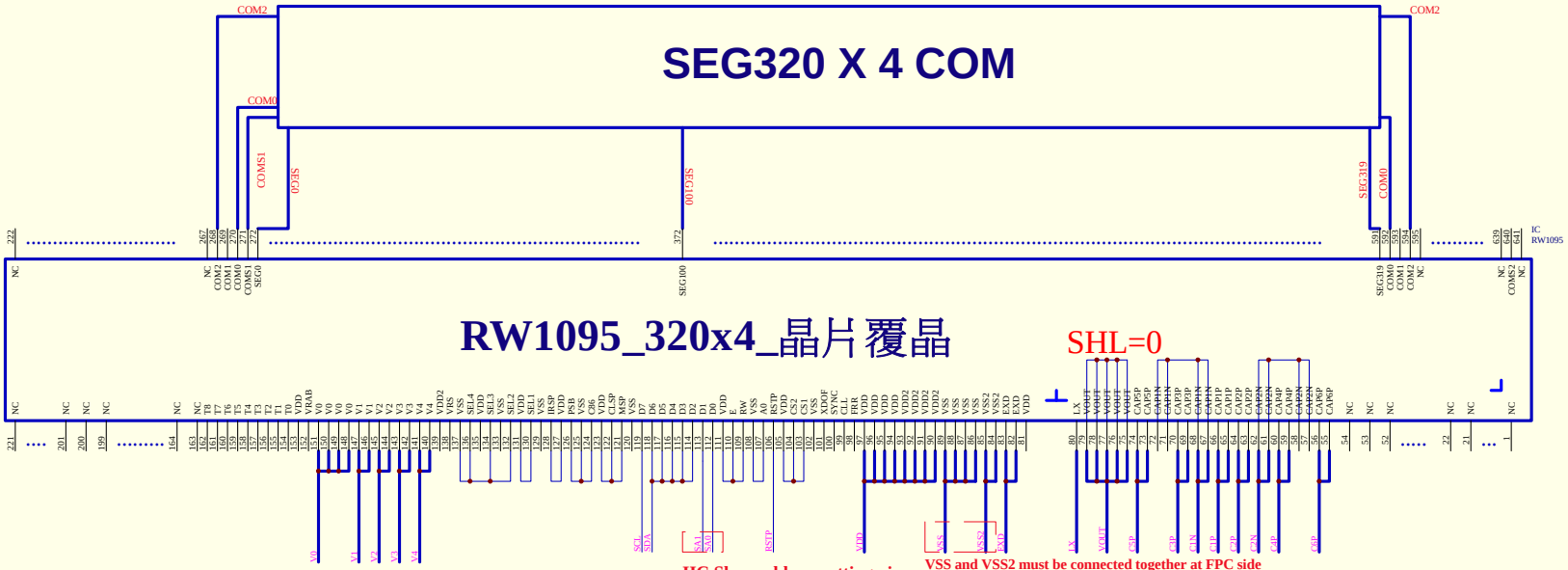
D1:1N5819
C12:1uF/25V~4.7uF/25V
C13:1uF/16V~10uF/16V
L1:2.2uH~10uH (IDC=80mA~100mA)

The capacitors of booster circuit must be removed when inductot type regulator circuit is used.

SEG320 X 4 COM



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface	
0	0	IIC	← Current setting
0	1	3/4 SPI	
1	0	8bit_8080	
1	1	8bit_6800	

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
IIC	VDD	VDD	VSS	VDD	VDD	SCL	SDA	D2~D5 connect to D6 D0,D1 is Slave address
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4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

SA1	SA0	Slave address
0	0	0x78
0	1	0x7a
1	0	0x7c
1	1	0x7e

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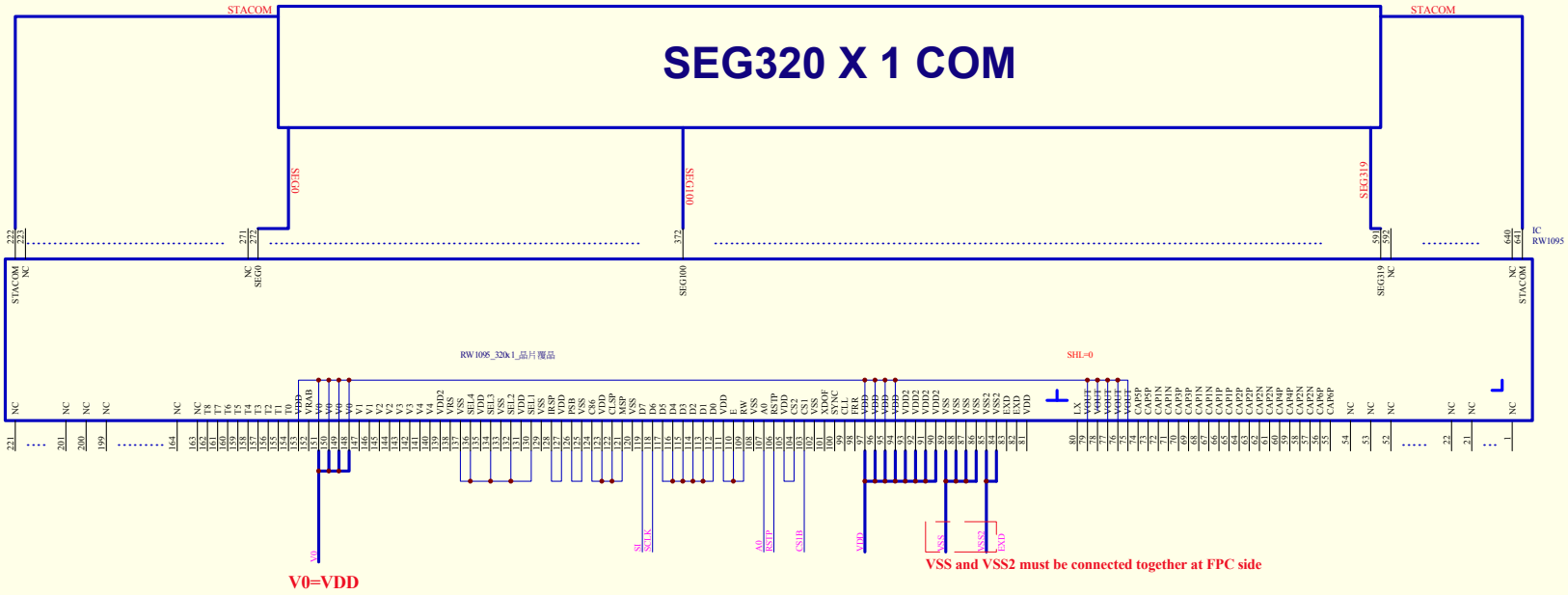
SEG320 X 1 COM



IRS="H": Internal resistors are selected

CLSP="H": Internal oscillator circuit is selected

Interface Selection

PSB	C86	Interface	
0	0	IIC	
0	1	3/4 SPI	← Current setting
1	0	8bit_8080	
1	1	8bit_6800	

Interface selection pins

Interface	CS1B	CS2	A0	E(XRD)	RW(XWR)	D7	D6	D5~D0
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4SPI	CS1B	VDD	A0	VDD	VDD	SI	SCLK	VDD
8080	CS1B	VDD	A0	XRD	XWR	D7	D6	D5~D0
6800	CS1B	VDD	A0	E	RW	D7	D6	D5~D0

Title: RockWorks		
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