# INTRODUCTION

S6A0073 is a dot matrix LCD driver & controller LSI which is fabricated by low power CMOS technology. It can display 1, 2 or 4 lines with $5 \times 8$ or $6 \times 8$ dots format.

## FUNCTIONS

- Character type dot matrix LCD driver & controller

- Internal driver : 34 common and 60 segment signal output

- Easy interface with 4-bit or 8-bit MPU

- Clock synchronized serial Interface

- $5 \times 8$ or $6 \times 8$ dots matrix possible

- Extension driver interface possible

- Bi-directional shift function

- All character reverse display

- Display shift per line

- Voltage converter for LCD drive voltage : 13V max (2 times / 3 times)

- Various instruction functions

- Automatic power on reset

## FEATURES

- Internal Memory
  - Character Generator ROM (CGROM) : 9,600 bits (240 characters $\times 5 \times 8$ dot)
  - Character Generator RAM (CGRAM) : $64 \times 8$ bits (8 characters $\times 5 \times 8$ dot)
  - Segment Icon RAM (SEGRAM) : $16 \times 8$ bits (96 icons max.)
  - Display Data RAM (DDRAM) : $80 \times 8$ bits (80 characters max.)
- Low power operation
  - Power supply voltage range: 2.7 to  5.5V ($V_{DD}$)
  - LCD Drive voltage range: 3.0 to 13.0V ($V_{DD}$ - V5)
- CMOS process
- Programmable duty cycle : 1/17, 1/33 (refer to Table 1)
- Internal oscillator with an external resistor
- Low power consumption
- TCP or bare chip available
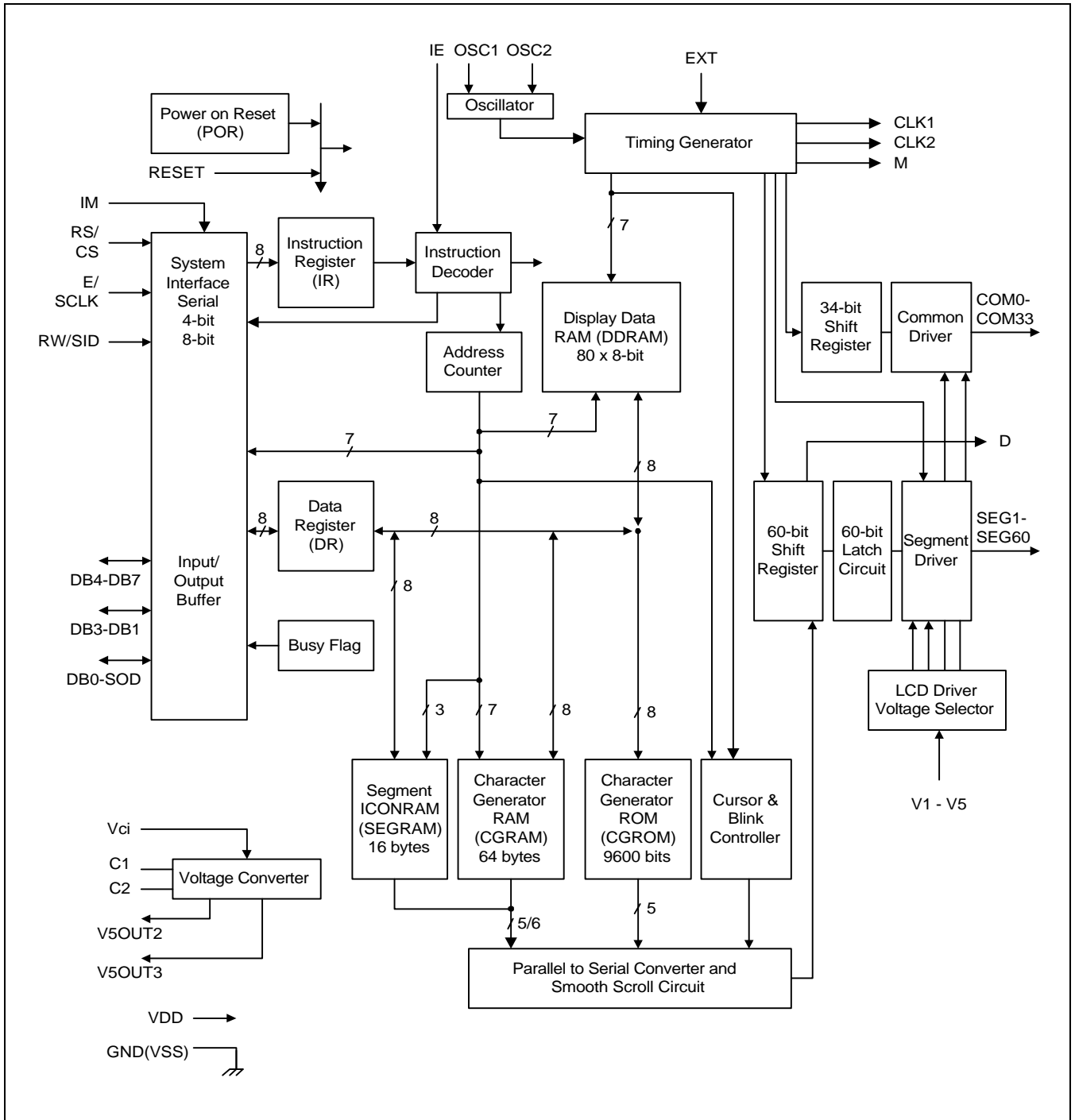
**Table 1. Programmable Duty Cycles**

1) 5-dot Font Width

| Display Line Numbers | Duty Ratio | Single-chip Operation | | With Extension Driver | |
|---|---|---|---|---|---|
| | | **Displayable characters** | **Possible icons** | **Displayable characters** | **Possible icons** |
| 1 | 1/17 | 1 line of 24 characters | 60 | 1 line of 52 characters | 80 |
| 2 | 1/33 | 2 lines of 24 characters | 60 | 2 lines of 32 characters | 80 |
| 4 | 1/33 | 4 lines of 12 characters | 60 | 4 lines of 20 characters | 80 |

2) 6-dot Font Width

| Display Line Numbers | Duty Ratio | Single-chip Operation | | With Extension Driver | |
|---|---|---|---|---|---|
| | | **Displayable characters** | **Possible icons** | **Displayable characters** | **Possible icons** |
| 1 | 1/17 | 1 line of 20 characters | 60 | 1 line of 50 characters | 96 |
| 2 | 1/33 | 2 lines of 20 characters | 60 | 2 lines of 30 characters | 96 |
| 4 | 1/33 | 4 lines of 10 characters | 60 | 4 lines of 20 characters | 96 |

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# BLOCK DIAGRAM

## PAD CONFIGURATION

CHIP SIZE: 4870 x 5770
PAD SIZE: 100 x 100
UNIT: μm

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 3 | SEG46 | | 100 | SEG15 |
| 4 | SEG47 | | 99 | SEG14 |
| 5 | SEG48 | | 98 | SEG13 |
| 6 | SEG49 | | 97 | SEG12 |
| 7 | SEG50 | | 96 | SEG11 |
| 8 | SEG51 | | 95 | SEG10 |
| 9 | SEG52 | | 94 | SEG9 |
| 10 | SEG53 | | 93 | SEG8 |
| 11 | SEG54 | | 92 | SEG7 |
| 12 | SEG55 | | 91 | SEG6 |
| 13 | SEG56 | | 90 | SEG5 |
| 14 | SEG57 | | 89 | SEG4 |
| 15 | SEG58 | | 88 | SEG3 |
| 16 | SEG59 | | 87 | SEG2 |
| 17 | SEG60 | | 86 | SEG1 |
| 18 | COM9 | | 85 | COM0 |
| 19 | COM10 | | 84 | COM1 |
| 20 | COM11 | | 83 | COM2 |
| 21 | COM12 | | 82 | COM3 |
| 22 | COM13 | | 81 | COM4 |
| 23 | COM14 | | 80 | COM5 |
| 24 | COM15 | | 79 | COM6 |
| 25 | COM16 | | 78 | COM7 |
| 26 | COM25 | | 77 | COM8 |
| 27 | COM26 | | 76 | COM17 |
| 28 | COM27 | | 75 | COM18 |
| 29 | COM28 | | 74 | COM19 |
| 30 | COM29 | | 73 | COM20 |
| 31 | COM30 | | 72 | COM21 |
| 32 | COM31 | | 71 | COM22 |
| 33 | COM32 | | 70 | COM23 |
| 34 | COM33 | | 69 | COM24 |
| 35 | VDD | | 68 | V1 |
| 36 | OSC2 | | 67 | V2 |

Top pads (left to right): 2 SEG45, 1 SEG44, 128 SEG43, 127 SEG42, 126 SEG41, 125 SEG40, 124 SEG39, 123 SEG38, 122 SEG37, 121 SEG36, 120 SEG35, 119 SEG34, 118 SEG33, 117 SEG32, 116 SEG31, 115 SEG30, 114 SEG29, 113 SEG28, 112 SEG27, 111 SEG26, 110 SEG25, 109 SEG24, 108 SEG23, 107 SEG22, 106 SEG21, 105 SEG20, 104 SEG19, 103 SEG18, 102 SEG17, 101 SEG16

Bottom pads (left to right): 37 OSC1, 38 CLK1, 39 CLK2, 40 D, 41 M, 42 RESET, 43 IM, 44 EXT, 45 IE, 46 VSS1, 47 RS/CS, 48 RW/SID, 49 E/SCLK, 50 DB0/SOD, 51 DB1, 52 DB2, 53 DB3, 54 DB4, 55 DB5, 56 DB6, 57 DB7, 58 Vci, 59 C2, 60 C1, 61 VSS2, 62 V5OUT2, 63 V5OUT3, 64 V5, 65 V4, 66 V3

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## PAD CENTER COORDINATES

| PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | SEG44 | -1687 | 2719 | 44 | EXT | -986 | -2719 | 87 | SEG2 | 2269 | 497 |
| 2 | SEG45 | -1812 | 2719 | 45 | IE | -861 | -2719 | 88 | SEG3 | 2269 | 622 |
| 3 | SEG46 | -2269 | 2122 | 46 | VSS1 | -736 | -2719 | 89 | SEG4 | 2269 | 747 |
| 4 | SEG47 | -2269 | 1997 | 47 | RS/CS | -611 | -2719 | 90 | SEG5 | 2269 | 872 |
| 5 | SEG48 | -2269 | 1872 | 48 | RW/SID | -486 | -2719 | 91 | SEG6 | 2269 | 997 |
| 6 | SEG49 | -2269 | 1747 | 49 | E/SCLK | -361 | -2719 | 92 | SEG7 | 2269 | 1122 |
| 7 | SEG50 | -2269 | 1622 | 50 | DB0/SOD | -236 | -2719 | 93 | SEG8 | 2269 | 1247 |
| 8 | SEG51 | -2269 | 1497 | 51 | DB1 | -111 | -2719 | 94 | SEG9 | 2269 | 1372 |
| 9 | SEG52 | -2269 | 1372 | 52 | DB2 | 14 | -2719 | 95 | SEG10 | 2269 | 1497 |
| 10 | SEG53 | -2269 | 1247 | 53 | DB3 | 139 | -2719 | 96 | SEG11 | 2269 | 1622 |
| 11 | SEG54 | -2269 | 1122 | 54 | DB4 | 264 | -2719 | 97 | SEG12 | 2269 | 1747 |
| 12 | SEG55 | -2269 | 997 | 55 | DB5 | 389 | -2719 | 98 | SEG13 | 2269 | 1872 |
| 13 | SEG56 | -2269 | 872 | 56 | DB6 | 514 | -2719 | 99 | SEG14 | 2269 | 1997 |
| 14 | SEG57 | -2269 | 747 | 57 | DB7 | 639 | -2719 | 100 | SEG15 | 2269 | 2122 |
| 15 | SEG58 | -2269 | 622 | 58 | Vci | 764 | -2719 | 101 | SEG16 | 1813 | 2719 |
| 16 | SEG59 | -2269 | 497 | 59 | C2 | 889 | -2719 | 102 | SEG17 | 1688 | 2719 |
| 17 | SEG60 | -2269 | 372 | 60 | C1 | 1014 | -2719 | 103 | SEG18 | 1563 | 2719 |
| 18 | COM9 | -2269 | 134 | 61 | VSS2 | 1139 | -2719 | 104 | SEG19 | 1438 | 2719 |
| 19 | COM10 | -2269 | 9 | 62 | V5OUT2 | 1264 | -2719 | 105 | SEG20 | 1313 | 2719 |
| 20 | COM11 | -2269 | -116 | 63 | V5OUR3 | 1389 | -2719 | 106 | SEG21 | 1188 | 2719 |
| 21 | COM12 | -2269 | -241 | 64 | V5 | 1514 | -2719 | 107 | SEG22 | 1063 | 2719 |
| 22 | COM13 | -2269 | -366 | 65 | V4 | 1639 | -2719 | 108 | SEG23 | 938 | 2719 |
| 23 | COM14 | -2269 | -491 | 66 | V3 | 1764 | -2719 | 109 | SEG24 | 813 | 2719 |
| 24 | COM15 | -2269 | -616 | 67 | V2 | 2269 | -2116 | 110 | SEG25 | 688 | 2719 |
| 25 | COM16 | -2269 | -741 | 68 | V1 | 2269 | -1991 | 111 | SEG26 | 563 | 2719 |
| 26 | COM25 | -2269 | -866 | 69 | COM24 | 2269 | -1866 | 112 | SEG27 | 438 | 2719 |
| 27 | COM26 | -2269 | -991 | 70 | COM23 | 2269 | -1741 | 113 | SEG28 | 313 | 2719 |
| 28 | COM27 | -2269 | -1116 | 71 | COM22 | 2269 | -1616 | 114 | SEG29 | 188 | 2719 |
| 29 | COM28 | -2269 | -1241 | 72 | COM21 | 2269 | -1491 | 115 | SEG30 | 63 | 2719 |
| 30 | COM29 | -2269 | -1366 | 73 | COM20 | 2269 | -1366 | 116 | SEG31 | -62 | 2719 |
| 31 | COM30 | -2269 | -1491 | 74 | COM19 | 2269 | -1241 | 117 | SEG32 | -187 | 2719 |
| 32 | COM31 | -2269 | -1616 | 75 | COM18 | 2269 | -1116 | 118 | SEG33 | -312 | 2719 |

## PAD CENTER COORDINATES (Continued)

| PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y | PAD NUM. | PAD NAME | COORDINATE X | COORDINATE Y |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 33 | COM32 | -2269 | -1741 | 76 | COM17 | 2269 | -991 | 119 | SEG34 | -437 | 2719 |
| 34 | COM33 | -2269 | -1866 | 77 | COM8 | 2269 | -866 | 120 | SEG35 | -562 | 2719 |
| 35 | VDD | -2269 | -1991 | 78 | COM7 | 2269 | -741 | 121 | SEG36 | -687 | 2719 |
| 36 | OSC2 | -2269 | -2116 | 79 | COM6 | 2269 | -616 | 122 | SEG37 | -812 | 2719 |
| 37 | OSC1 | -1861 | -2719 | 80 | COM5 | 2269 | -491 | 123 | SEG38 | -937 | 2719 |
| 38 | CLK1 | -1736 | -2719 | 81 | COM4 | 2269 | -366 | 124 | SEG39 | -1062 | 2719 |
| 39 | CLK2 | -1611 | -2719 | 82 | COM3 | 2269 | -241 | 125 | SEG40 | -1187 | 2719 |
| 40 | D | -1486 | -2719 | 83 | COM2 | 2269 | -116 | 126 | SEG41 | -1312 | 2719 |
| 41 | M | -1361 | -2719 | 84 | COM1 | 2269 | 9 | 127 | SEG42 | -1437 | 2719 |
| 42 | RESET | -1236 | -2719 | 85 | COM0 | 2269 | 134 | 128 | SEG43 | -1562 | 2719 |
| 43 | IM | -1111 | -2719 | 86 | SEG1 | 2269 | 372 | | | | |

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# PIN CONFIGURATION OF TCP

## TCP OUTLINE



OUTPUT SIDE

S6A0073

NC VDD OSC2 OSC1 CLK1 CLK2 D M RESET IM EXT IE VSS1 RS/CS RW/SID E/SCLK DB0/SOD DB1 DB2 DB3 DB4 DB5 DB6 DB7 Vci C2 C1 VSS2 V5OUT2 V5OUT3 V5 V4 V3 V2 V1 NC

Top pads: NC, NC, COM33, ..., COM9, SEG60, ......, SEG1, COM0, ..., COM24, NC, NC

Left pads (top to bottom): 2, 1, 128, 127, 126, 125, 124, 123, 122, 121, 120, 119, 118, 117, 116, 115, 114, 113, 112, 111, 110, 109, 108, 107, 106, 105, 104, 103, 102, 101

Left column: 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36

Right column: 100, 99, 98, 97, 96, 95, 94, 93, 92, 91, 90, 89, 88, 87, 86, 85, 84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73, 72, 71, 70, 69, 68, 67

**S6A0073 PAD DIAGRAM**
**134-TCP-35mm**

Bottom pads: 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66

Bottom labels: NC, VDD, OSC2, OSC1, CLK1, CLK2, D, M, RESET, IM, EXT, IE, VSS1, RS/CS, RW/SID, E/SCLK, DB0/SOD, DB1, DB2, DB3, DB4, DB5, DB6, DB7, Vci, C2, C1, VSS2, V5OUT2, V5OUT3, V5, V4, V3, V2, V1, NC

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## PIN DESCRIPTION

| Pin (No) | I/O | Name | Description | Interface |
|---|---|---|---|---|
| VDD(35) | - | Power supply | for logical circuit (+3V, +5V) | Power Supply |
| VSS1, VSS2 (46, 61) | | | 0V (GND) | |
| V1-V5 (68 - 64) | | | Bias voltage level for LCD driving | |
| Vci (58) | I | | Input voltage to the voltage converter to generate LCD drive voltage (Vci = 1.0 to 4.5V). | |
| SEG1 - SEG60 (86 -128, 1- 17) | O | Segment output | Segment signal output for LCD drive. | LCD |
| COM0 - COM33 (85 - 69, 18 - 34) | O | Common output | Common signal output for LCD drive | LCD |
| OSC1, OSC2 (37, 36) | I(OSC1), O(OSC2) | Oscillator | When using internal oscillator, connect external Rf resistor. If external clock is used, connect it to OSC1. | External resistor/oscillator (OSC1) |
| CLK1, CLK2 (38, 39) | O | Latch (CLK1)/ Shift (CLK2) clock | When EXT = "High", each outputs latch clock and shift clock for extension driver. | Extension driver |
| C1, C2 (60, 59) | I | External capacitance input | To use the voltage converter (2 times /3 times), these pins must be connected to the external capacitance. | External capacitance |
| M (41) | O | Alternated signal for LCD driver output | When EXT = "High", outputs the alternating signal to convert LCD driver waveform to AC for Extension driver. | Extension driver |
| D(40) | O | Display data interface | When EXT = "High", outputs extension driver data (the 61th dot's data) | Extension driver |
| EXT(44) | I | Extension driver control signal | When EXT = "High", makes extension driver control signal enable, When EXT = "Low", suppress extra current consumption and CLK1,CLK2,M,D should be open. | - |
| RESET (42) | I | Reset pin | Initialized to Low | - |
| IE (45) | I | Selection pin of instruction set. | When IE = "High", instruction set is selected as Table 6. When IE = "Low", instruction set is selected as Table 10. | - |

# PIN DESCRIPTION (continued)

| Pin(No) | I/O | Name | Description | Interface |
|---|---|---|---|---|
| V5OUT2 (62) | O | Two times converter output | The value of Vci is converted two times. To use three times converter, the same capacitance as that of C1-C2 should be connected here. | V5 / capacitance |
| V5OUT3 (63) | | Three times converter output | The value of Vci is converted three times. | V5 |
| IM (43) | I | Interface mode selection | Select Interface mode with the MPU. When IM = "Low" : serial mode, When IM = "High" : 4-bit/8-bit bus mode. | - |
| RS/CS (47) | I | Register select /Chip select | When bus mode, used as register selection input. When RS/CS = "High", Data register is selected. When RS/CS = "Low", Instruction register is selected. In serial mode, used as chip selection input. When RS/CS = "Low", selected. When RS/CS = "High", not selected.(Low access enable) | MPU |
| RW/SID (48) | I | Read, write /Serial input data | In bus mode, used as read/write selection input. When RW/SID = "High", read operation When RW/SID = "Low", write operation. In serial mode, used for data input pin. | MPU |
| E/SCLK (49) | I | Read, write enable /Serial clock | When bus mode, used as read, write enable signal. When serial mode, used as serial clock input pin. | MPU |
| DB0/SOD (50) | I/O, O | Data bus 0 bit /Serial output data | In 8-bit bus mode, used as lowest bidirectional data bit. During 4-bit bus mode, Open this pin. In serial mode, used as serial data output pin. If not in read operation, open this pin. | MPU |
| DB1 - DB3 (51 - 53) | I/O | Data bus 1- 7 | In 8-bit bus mode, used as low order bidirectional data bus. During 4-bit bus mode or serial mode, open these pins. | MPU |
| DB4 - DB7 (54 - 57) | | | In 8-bit bus mode, used as high order bidirectional data bus. In case of 4-bit bus mode, used as both high and low order. DB7 used for Busy Flag output. During serial mode, open these pins. | MPU |

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# FUNCTION DESCRIPTION

### System Interface

This chip has all three kinds of interface type with MPU : serial, 4-bit bus and 8-bit bus. Serial and bus(4-bit/8-bit) are selected by IM input, and 4-bit bus and 8-bit bus are selected by DL bit in the instruction register. During read or write operation, two 8-bit registers are used. one is data register (DR), the other is instruction register(IR). The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM/SEGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. Hence, after MPU reads DR data, the data in the next DDRAM/CGRAM/SEGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM/SEGRAM automatically. The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data. To select register, use RS/CS input pin in 4-bit/8-bit bus mode(IM = "High") or RS bit in serial mode(IM = "Low").

#### Table 2. Various Kinds of Operations according to RS and R/W Bits

| RS | R/W | Operation |
|---|---|---|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| L | H | Read Busy flag(DB7) and address counter (DB0 – DB6) |
| H | L | Data Write operation (MPU writes data into DR) |
| H | H | Data Read operation (MPU reads data from DR) |

### Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7. Before executing the next instruction, be sure that BF is not High.

### Display Data RAM (DDRAM)

DDRAM stores display data of maximum $80 \times 8$ bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number. (refer to Figure 1.)

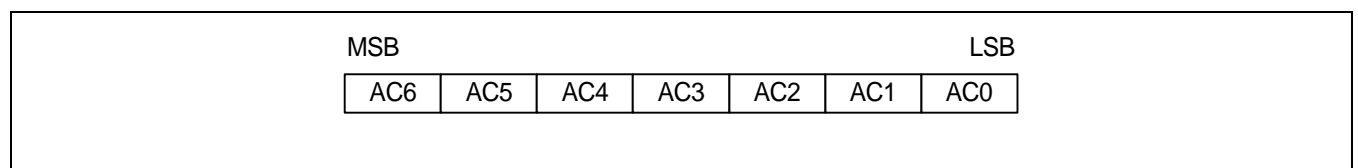| MSB | | | | | | LSB |
|---|---|---|---|---|---|---|
| AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

**Figure 1. DDRAM Address**

**1) Display of 5-dot Font Width Character**

(1) 5-dot 1-line Display

In case of 1 line display with 5-dot font, the address range of DDRAM is 00H - 4FH (refer to Figure 2). When EXT = "High", extension driver will be used. Figure 3 shows the example that 40 segment extension driver is added
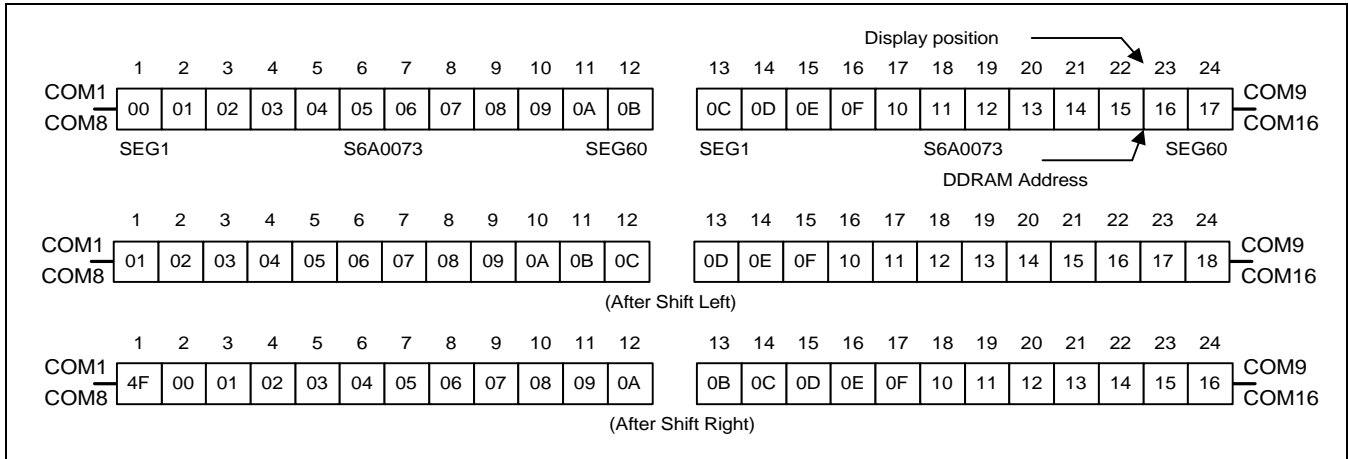


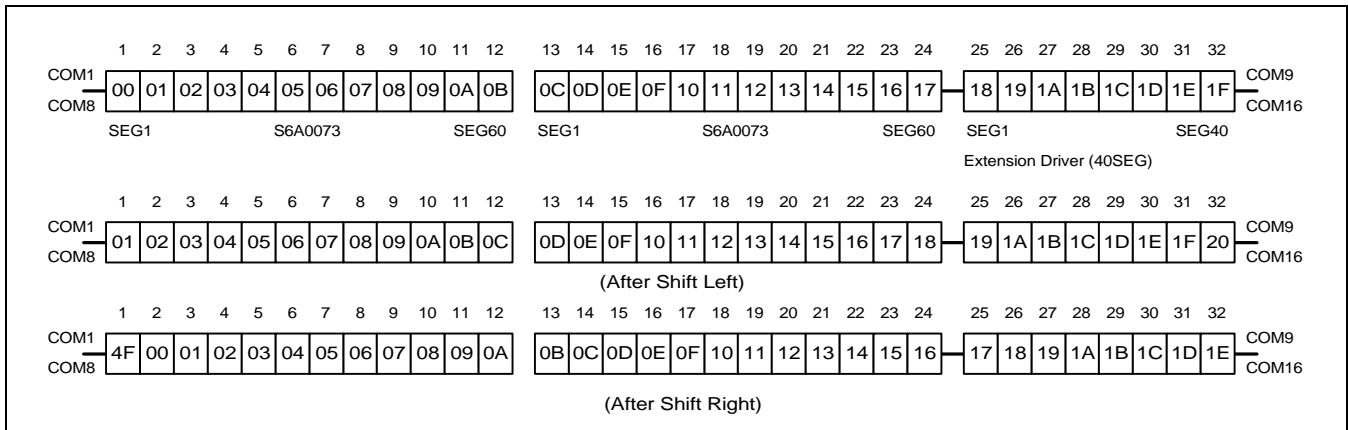**Figure 2. 1-line ´ 24ch. Display (5-dot font width)**



**Figure 3. 1-line ´ 32ch. Display with 40 SEG. extension driver (5-dot font width)**

(2) 5-dot 2-line Display

In case of 2 line display with 5-dot font, the address range of DDRAM is 00H - 27H,40H - 67H (refer to Figure 4). When EXT = "High", extension driver will be used. Figure 5 shows the example that 40 segment extension driver is added.
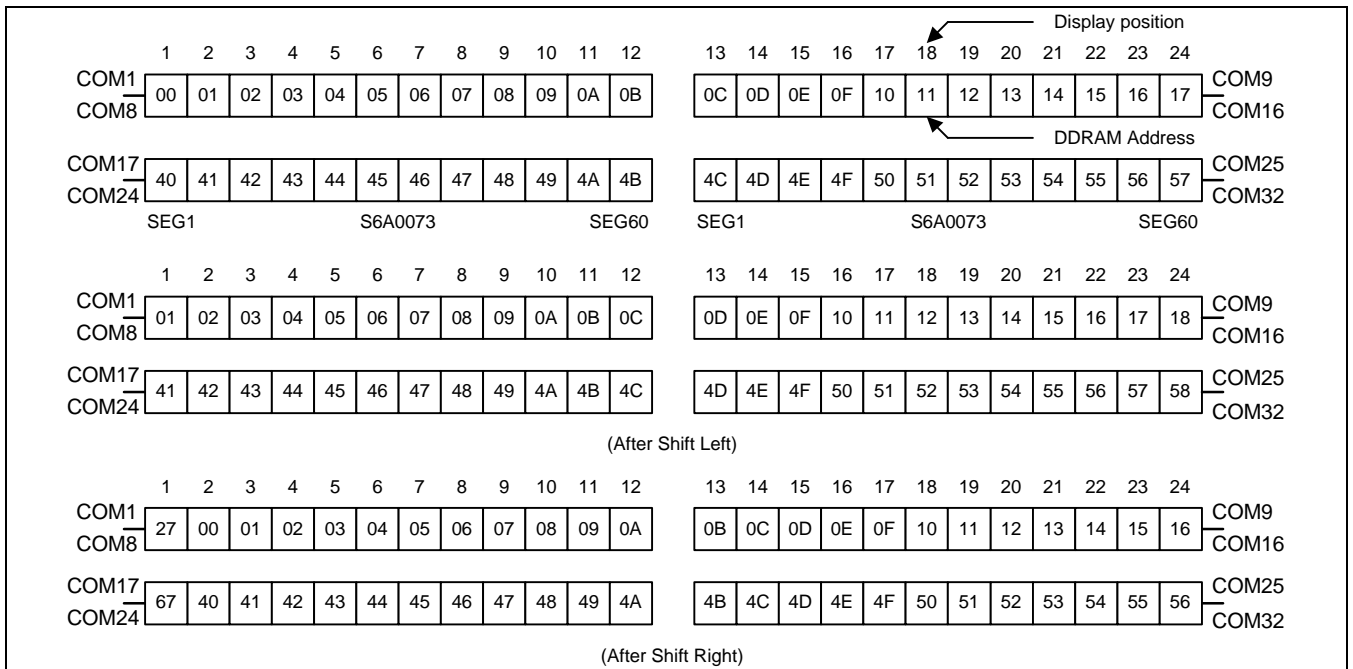


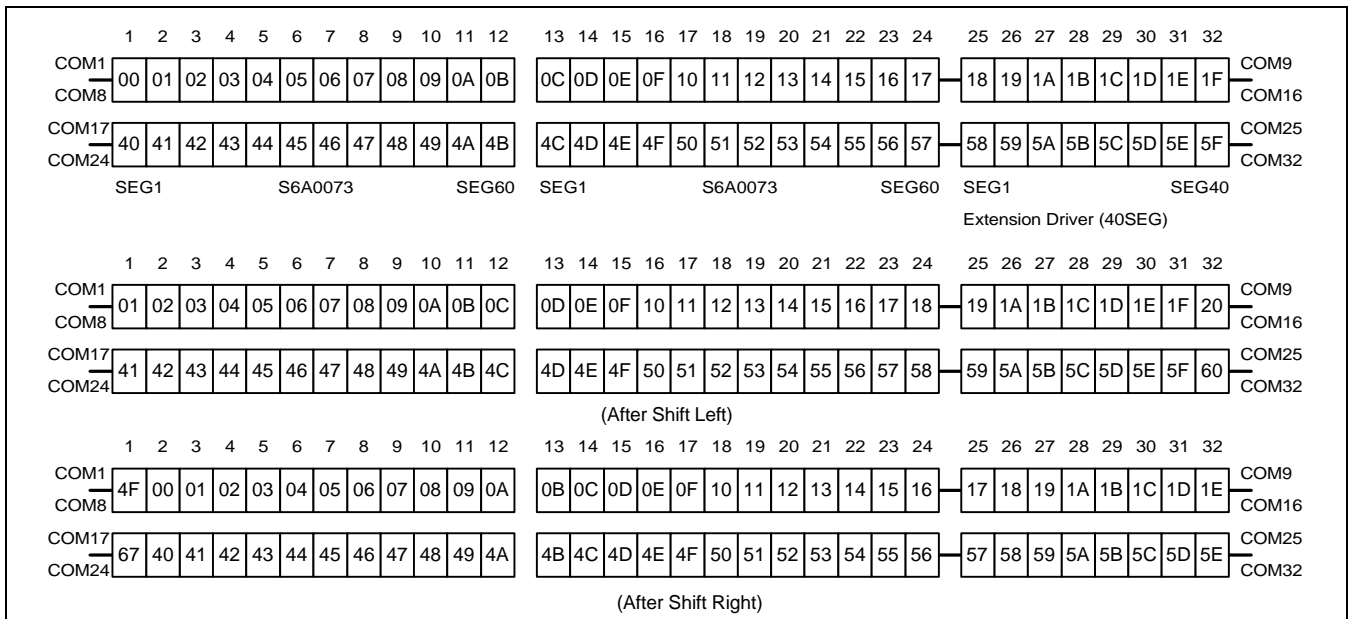**Figure 4. 2-line ´ 24ch. Display (5-dot Font Width)**



**Figure 5. 2-line ´ 32ch. Display with 40 SEG. Extension Driver (5-dot Font Width)**

(3) 5-dot 4-line Display

In case of 4 line display with 5-dot font, the address range of DDARM is 00H - 13H, 20H - 33H, 40H - 53H, 60H - 73H (refer to Figure 6). When EXT = "High", extension driver will be used. Figure 7 shows the example that 40 segment extension driver is added.
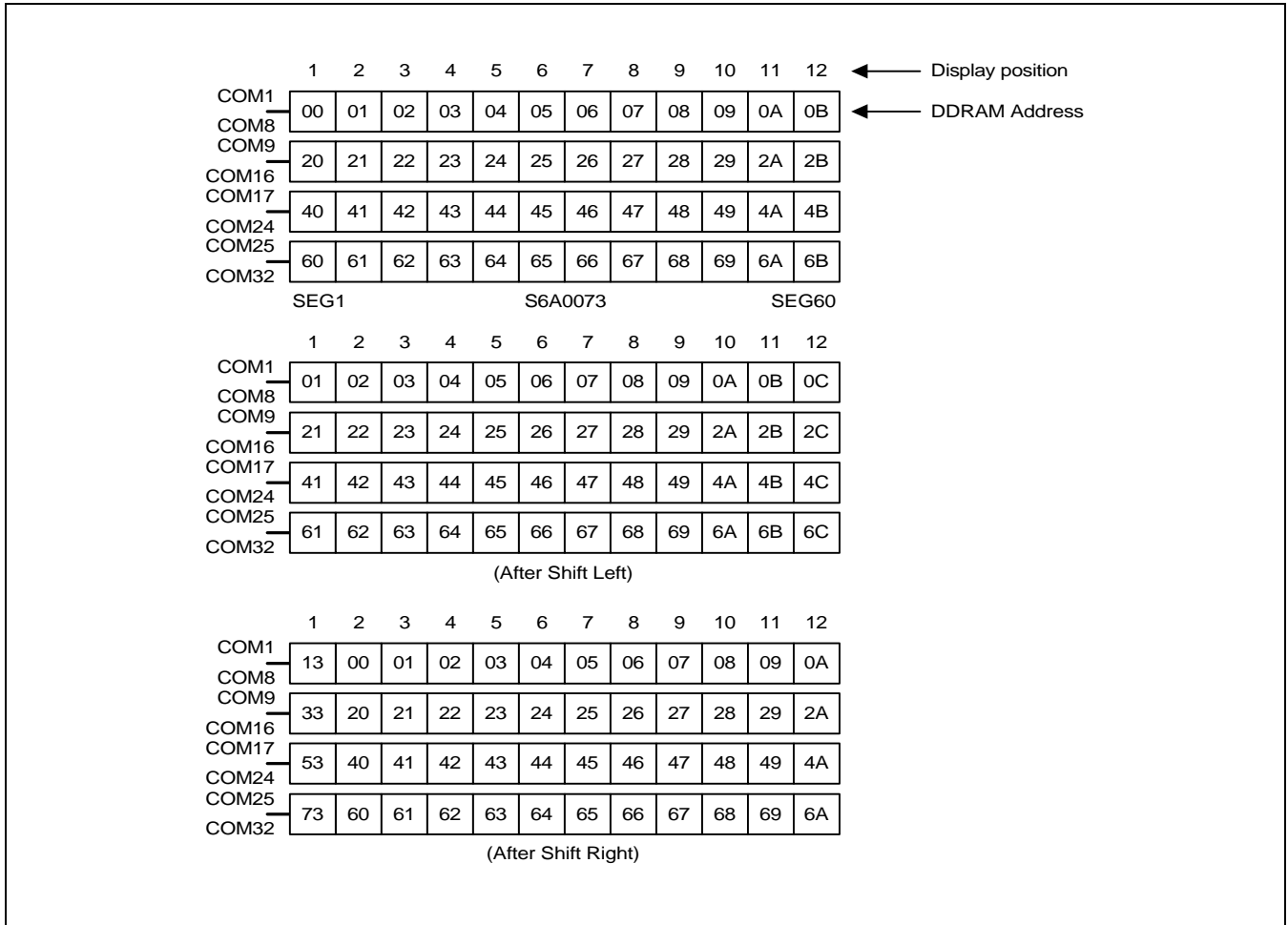


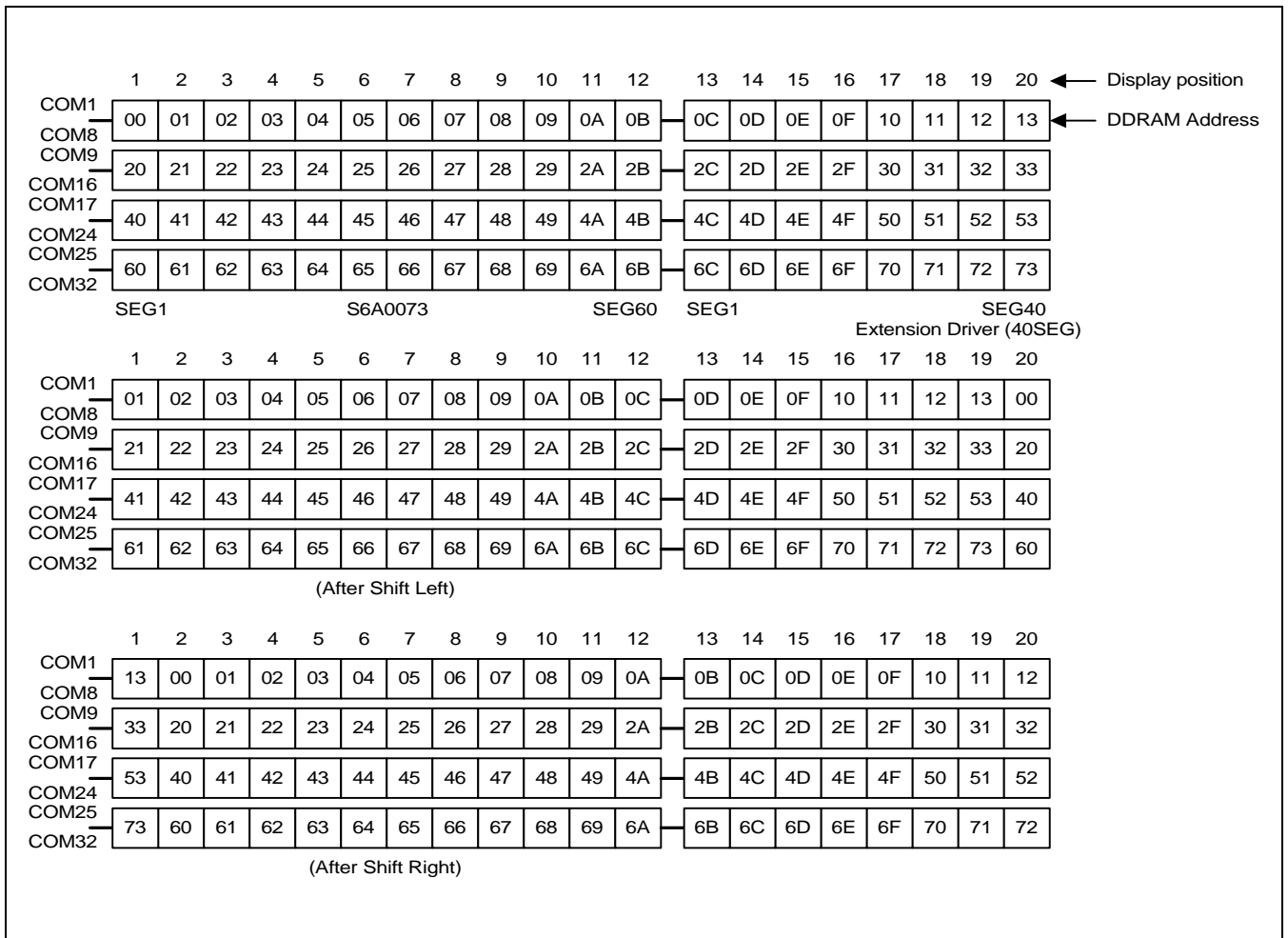**Figure 6. 4-line ´ 12ch. Display (5-dot Font Width)**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | ← Display position |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM1<br>COM8 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 | ← DDRAM Address |
| COM9<br>COM16 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | | 2C | 2D | 2E | 2F | 30 | 31 | 32 | 33 | |
| COM17<br>COM24 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 | |
| COM25<br>COM32 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B | | 6C | 6D | 6E | 6F | 70 | 71 | 72 | 73 | |

SEG1        S6A0073        SEG60   SEG1                              SEG40
                                           Extension Driver (40SEG)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM1<br>COM8 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | | 0D | 0E | 0F | 10 | 11 | 12 | 13 | 00 |
| COM9<br>COM16 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | | 2D | 2E | 2F | 30 | 31 | 32 | 33 | 20 |
| COM17<br>COM24 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | | 4D | 4E | 4F | 50 | 51 | 52 | 53 | 40 |
| COM25<br>COM32 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B | 6C | | 6D | 6E | 6F | 70 | 71 | 72 | 73 | 60 |

(After Shift Left)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COM1<br>COM8 | 13 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 |
| COM9<br>COM16 | 33 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | | 2B | 2C | 2D | 2E | 2F | 30 | 31 | 32 |
| COM17<br>COM24 | 53 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 |
| COM25<br>COM32 | 73 | 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | | 6B | 6C | 6D | 6E | 6F | 70 | 71 | 72 |

(After Shift Right)

**Figure 7. 4-line ´ 20ch. Display with 40 SEG. Extension Driver (5-dot Font Width)**

**2) Display of 6-dot Font Width Character**

(1) 6-dot 1-line Display

In case of 1 line display with 6-dot font, the address range of DDRAM is 00H - 4FH (refer to Figure 8). When EXT = "High", extension driver will be used. Figure 9 shows the example that 40 segment extension driver is added.
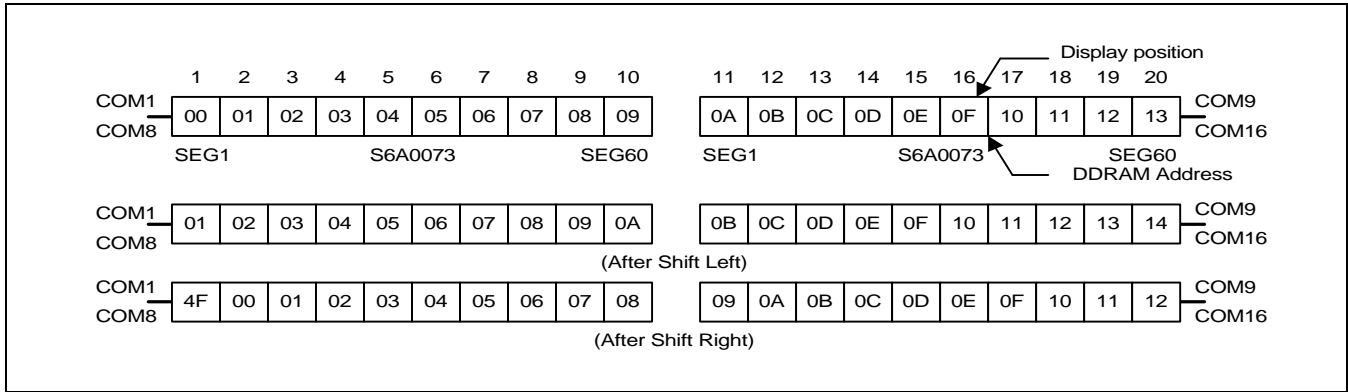


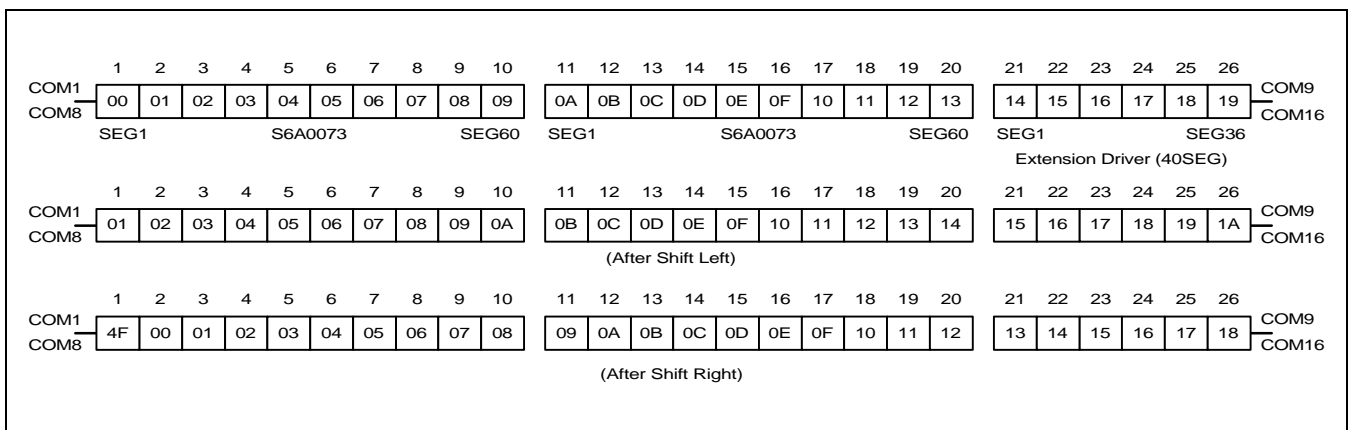**Figure 8. 1-line ´ 20ch. Display (6-dot Font Width)**



**Figure 9. 1-line ´ 26ch. Display with 40 SEG. Extension Driver (6-dot Font Width)**

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(2) 6-dot 2-line Display

In case of 2 line display with 6-dot font, the address range of DDRAM is 00H - 27H, 40H - 67H. (refer to Figure 10) When EXT = "High", extension driver will be used. Figure 11 shows the example that 40 segment extension driver is added.
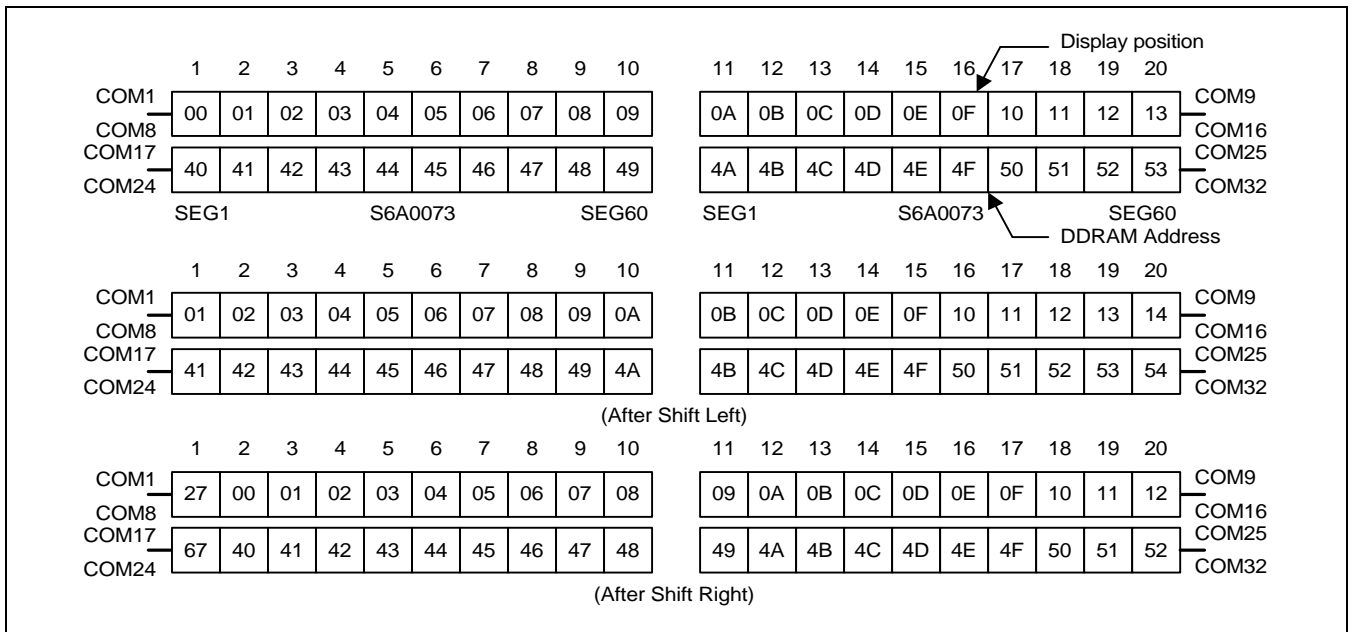


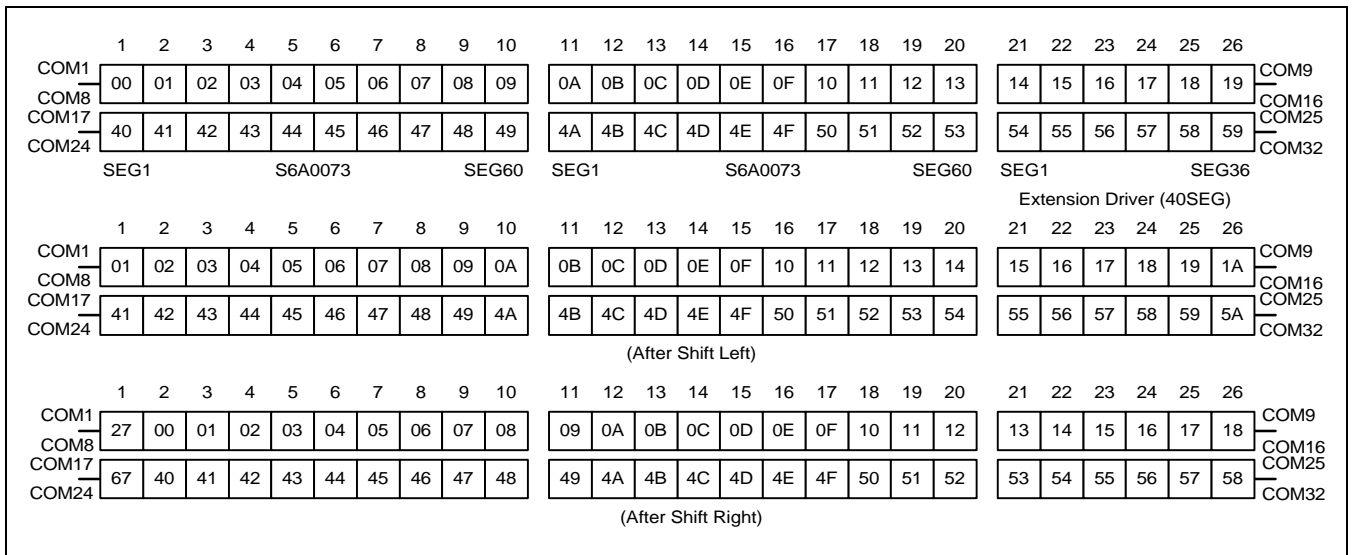**Figure 10. 2-line ´ 20ch. Display (6-dot Font Width)**



**Figure 11. 2-line ´ 26ch. Display with 40 SEG. Extension Driver (6-dot Font Width)**

 (3) 6-dot 4-line Display

In case of 4 line display with 6-dot font, the address range of DDARM is 00H-13H, 20H-33H, 40H-53H, 60H-73H (refer to Figure 12). When EXT = "High", extension driver will be used. Figure 13 shows the example that 40 segment extension driver is added.
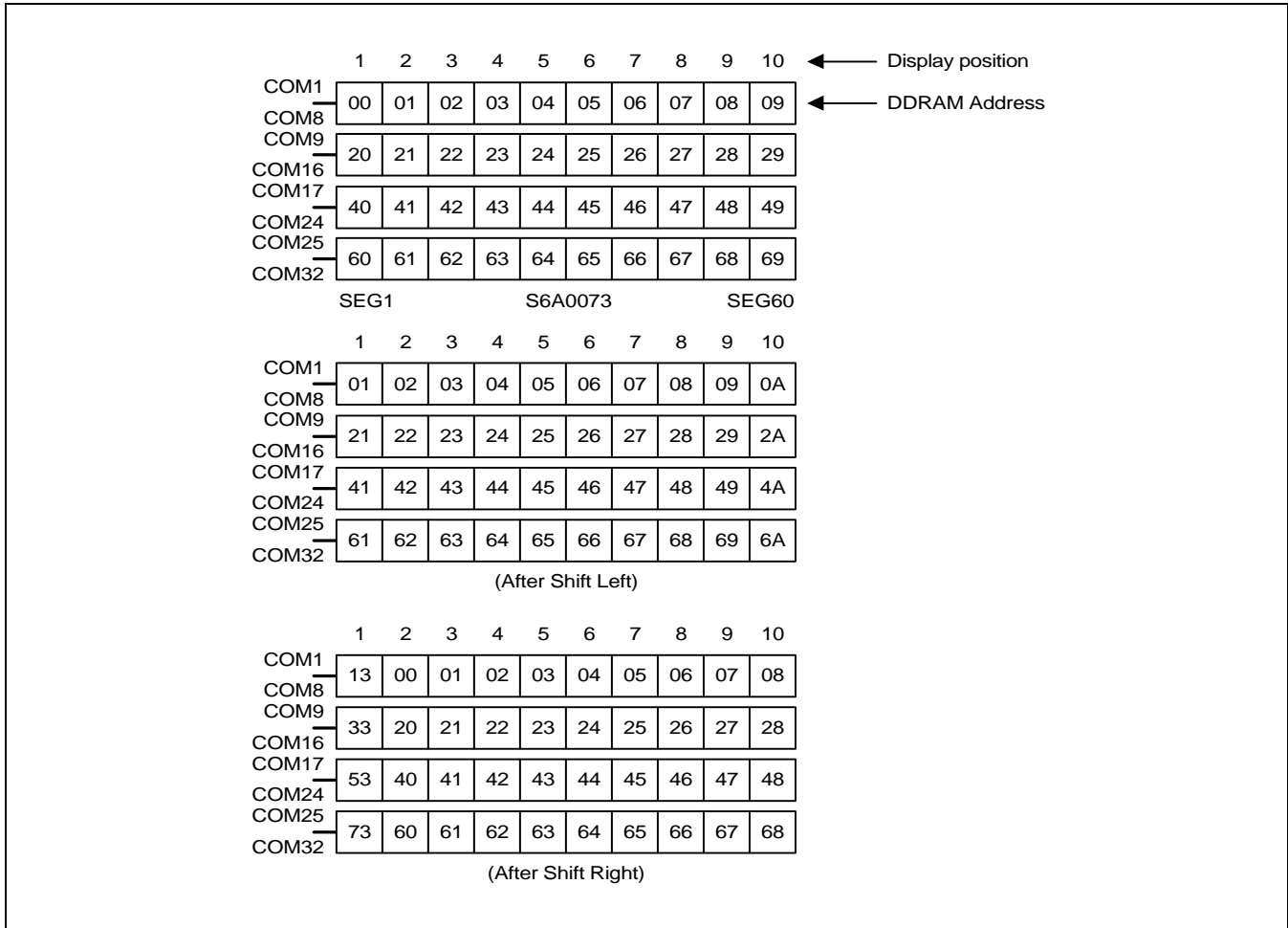


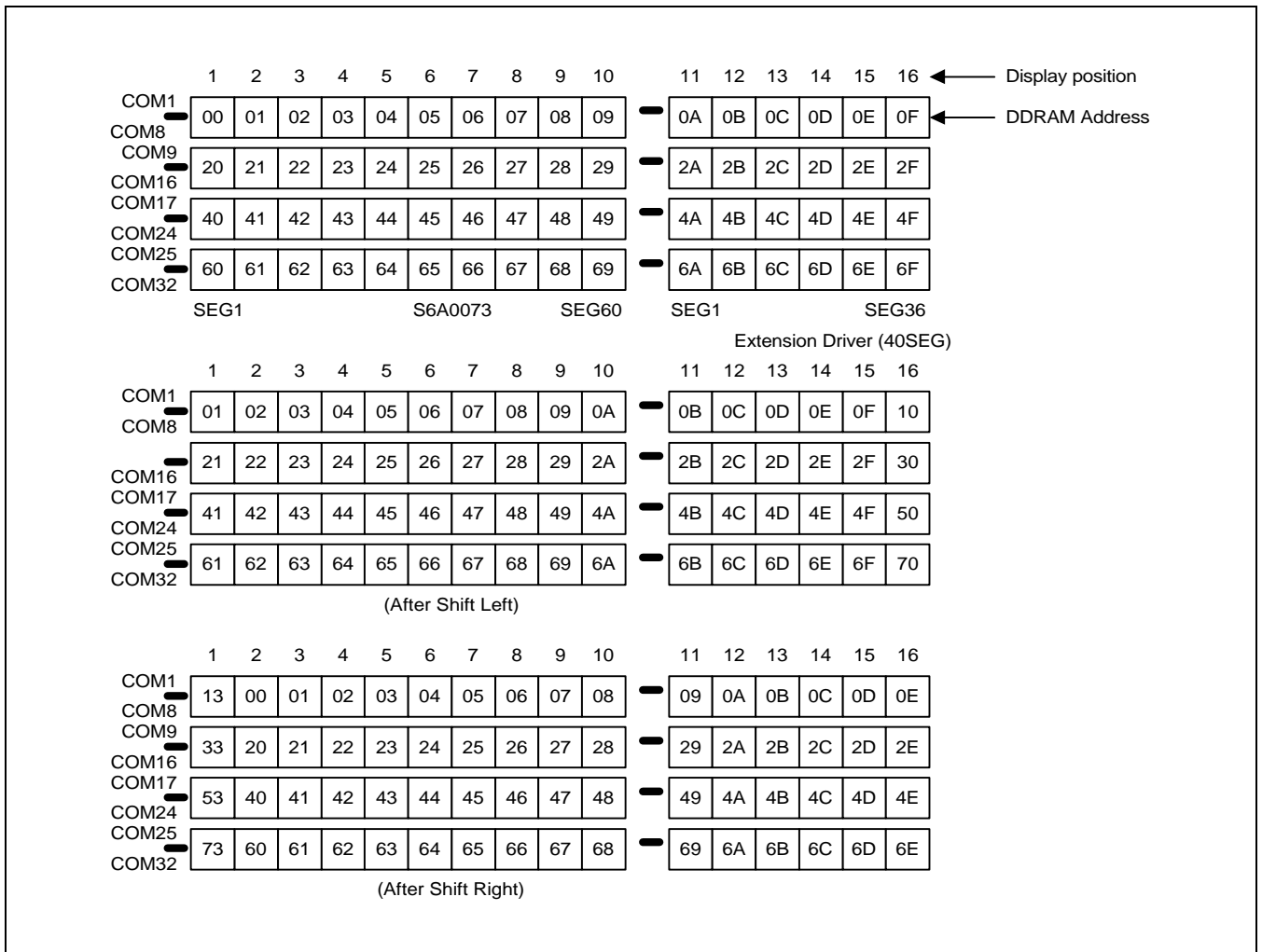**Figure 12. 4-line ´ 10 ch. Display (6-dot Font Width)**

**Figure 13. 4-line ´ 16ch. Display with 40 SEG. Driver (6-dot Font Width)**

**Timing Generation Circuit**

Timing generation circuit generates clock signals for the internal operations.

**Address Counter (AC)**

Address Counter(AC) stores DDRAM/CGRAM/SEGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM/SEGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0-DB6 ports.

**Cursor/Blink Control Circuit**

It controls cursor/blink ON/OFF and black/white inversion at cursor position.

**LCD Driver Circuit**

LCD Driver circuit has 34 common and 60 segment signals for LCD driving. Data from SEGRAM/CGRAM/CGROM is transferred to 60-bit segment latch serially, which is then stored to a 60-bit shift latch. When each com is selected by 34-bit common register, segment data also output through segment driver from 100-bit segment latch. In case of 1-line display mode, COM0 - COM17 have a 1/17 duty ratio, and in 2-line or 4-line mode, COM0-COM33 have a 1/33 duty ratio.

**CGROM (Character Generator ROM)**

CGROM has $5 \times 8$-dot 240 character pattern.

**CGRAM (Character Generator RAM)**

CGRAM has up to $5 \times 8$-dot 8 characters. By writing font data to CGRAM, user defined character can be used (refer to Table 4).

### Table 4. Relationship between Character Code (DDRAM) and Character Pattern (CGRAM)

1) $5 \times 8$ dots Character Pattern

| Character Code (DDRAM data) | | | | | | | | CGRAM Address | | | | | | CGRAM Data | | | | | | | | Pattern Number |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | |
| 0 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | B1 | B0 | x | 0 | 1 | 1 | 1 | 0 | Pattern 1 |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | . | | | | | | . | | 0 | 1 | 1 | | . | | 1 | 1 | 1 | 1 | 1 | |
| | | | . | | | | | | . | | 1 | 0 | 0 | | . | | 1 | 0 | 0 | 0 | 1 | |
| | | | . | | | | | | . | | 1 | 0 | 1 | | . | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |
| | | | . | | | | | | . | | | . | | | | . | | | | . | | . |
| | | | . | | | | | | . | | | . | | | | . | | | | . | | . |
| 0 | 0 | 0 | 0 | x | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | B1 | B0 | x | 1 | 0 | 0 | 0 | 1 | Pattern 8 |
| | | | | | | | | | | | 0 | 0 | 1 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | . | | | | | | . | | 0 | 1 | 1 | | . | | 1 | 1 | 1 | 1 | 1 | |
| | | | . | | | | | | . | | 1 | 0 | 0 | | . | | 1 | 0 | 0 | 0 | 1 | |
| | | | . | | | | | | . | | 1 | 0 | 1 | | . | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | | 0 | 0 | 0 | 0 | 0 | |

2) 6 × 8 dots Character Pattern

| Character Code (DDRAM data) | | | | | | | | CGRAM Address | | | | | | CGRAM Data | | | | | | | | Pattern Number |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | A5 | A4 | A3 | A2 | A1 | A0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | |
| 0 | 0 | 0 | 0 | x | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | B1 | B0 | 0 | 0 | 1 | 1 | 1 | 0 | Pattern 1 |
| | | | | | | | | | | | 0 | 0 | 1 | | | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | . | | | | | . | | 0 | 1 | 1 | | . | 0 | 1 | 1 | 1 | 1 | 1 | |
| | | | | . | | | | | . | | 1 | 0 | 0 | | . | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | . | | | | | . | | 1 | 0 | 1 | | . | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | 0 | 0 | 0 | 0 | 0 | 0 | |
| | | | | . | | | | | . | | | . | | | | | . | | | | | . |
| 0 | 0 | 0 | 0 | x | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | B1 | B0 | 0 | 1 | 0 | 0 | 0 | 1 | Pattern 8 |
| | | | | | | | | | | | 0 | 0 | 1 | | | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 0 | 1 | 0 | | | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | . | | | | | . | | 0 | 1 | 1 | | . | 0 | 1 | 1 | 1 | 1 | 1 | |
| | | | | . | | | | | . | | 1 | 0 | 0 | | . | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | . | | | | | . | | 1 | 0 | 1 | | . | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 0 | | | 0 | 1 | 0 | 0 | 0 | 1 | |
| | | | | | | | | | | | 1 | 1 | 1 | | | 0 | 0 | 0 | 0 | 0 | 0 | |

**NOTES:**

1. When Be(Blink Enable bit) = "High", blink is controlled by B1 and B0 bit. In case of 5-dot font width, when B1 = "1", enabled dots of P0 - P4 will blink, and when B1 = "0" and B0 = "1", enabled dots in P4 will blink, when B1 = "0" and B0 = "0", blink will not happen.

   In case of 6-dot font width, when B1 = "1", enabled dots of P0-P5 will blink, and when B1 = "0" and B0 = "1", enabled dots of P5 will blink, when B1 = "0" and B0 = "0", blink will not happen.

2. "X" : don't care

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### SEGRAM (Segment Icon RAM)

SEGRAM has segment control data and segment pattern data. During 1-line display mode, COM0(COM17) makes the data of SEGRAM enable to display icons. When used in 2/4-line display mode COM0(COM33) does that. Its higher 2-bits are blinking control data, and lower 6-bits are pattern data (refer to Table 5 and Figure 8).

**Table 5. Relationship between SEGRAM Address and Display Pattern**

| SEGRAM Address | | | | SEGRAM Data Display Pattern | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 5-dot Font Width | | | | | | | | 6-dot Font Width | | | | | | | |
| A3 | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | B1 | B0 | X | S1 | S2 | S3 | S4 | S5 | B1 | B0 | S1 | S2 | S3 | S4 | S5 | S6 |
| 0 | 0 | 0 | 1 | B1 | B0 | X | S6 | S7 | S8 | S9 | S10 | B1 | B0 | S7 | S8 | S9 | S10 | S11 | S12 |
| 0 | 0 | 1 | 0 | B1 | B0 | X | S11 | S12 | S13 | S14 | S15 | B1 | B0 | S13 | S14 | S15 | S16 | S17 | S18 |
| 0 | 0 | 1 | 1 | B1 | B0 | X | S16 | S17 | S18 | S19 | S20 | B1 | B0 | S19 | S20 | S21 | S22 | S23 | S24 |
| 0 | 1 | 0 | 0 | B1 | B0 | X | S21 | S22 | S23 | S24 | S25 | B1 | B0 | S25 | S26 | S27 | S28 | S29 | S30 |
| 0 | 1 | 0 | 1 | B1 | B0 | X | S26 | S27 | S28 | S29 | S30 | B1 | B0 | S31 | S32 | S33 | S34 | S35 | S36 |
| 0 | 1 | 1 | 0 | B1 | B0 | X | S31 | S32 | S33 | S34 | S35 | B1 | B0 | S37 | S38 | S39 | S40 | S41 | S42 |
| 0 | 1 | 1 | 1 | B1 | B0 | X | S36 | S37 | S38 | S39 | S40 | B1 | B0 | S43 | S44 | S45 | S46 | S47 | S48 |
| 1 | 0 | 0 | 0 | B1 | B0 | X | S41 | S42 | S43 | S44 | S45 | B1 | B0 | S49 | S50 | S51 | S52 | S53 | S54 |
| 1 | 0 | 0 | 1 | B1 | B0 | X | S46 | S47 | S48 | S49 | S50 | B1 | B0 | S55 | S56 | S57 | S58 | S59 | S60 |
| 1 | 0 | 1 | 0 | B1 | B0 | X | S51 | S52 | S53 | S54 | S55 | B1 | B0 | S61 | S62 | S63 | S64 | S65 | S66 |
| 1 | 0 | 1 | 1 | B1 | B0 | X | S56 | S57 | S58 | S59 | S60 | B1 | B0 | S67 | S68 | S69 | S70 | S71 | S72 |
| 1 | 1 | 0 | 0 | B1 | B0 | X | S61 | S62 | S63 | S64 | S65 | B1 | B0 | S73 | S74 | S75 | S76 | S77 | S78 |
| 1 | 1 | 0 | 1 | B1 | B0 | X | S66 | S67 | S68 | S69 | S70 | B1 | B0 | S79 | S80 | S81 | S82 | S83 | S84 |
| 1 | 1 | 1 | 0 | B1 | B0 | X | S71 | S72 | S73 | S74 | S75 | B1 | B0 | S85 | S86 | S87 | S88 | S89 | S90 |
| 1 | 1 | 1 | 1 | B1 | B0 | X | S76 | S77 | S78 | S79 | S80 | B1 | B0 | S91 | S92 | S93 | S94 | S95 | S96 |

**NOTES:**

1.   B1, B0 : Blinking control bit

| Control Bit | | | Blinking Port | |
|---|---|---|---|---|
| BE | B1 | B0 | 5-dot font width | 6-dot font width |
| 0 | X | X | No blink | No blink |
| 1 | 0 | 0 | No blink | No blink |
| 1 | 0 | 1 | D4 | D5 |
| 1 | 1 | X | D4 - D0 | D5 - D0 |

2.   S1 - S80 : Icon pattern ON/OFF in 5-dot font width
     S1 - S96 : Icon pattern ON/OFF in 6-dot font width
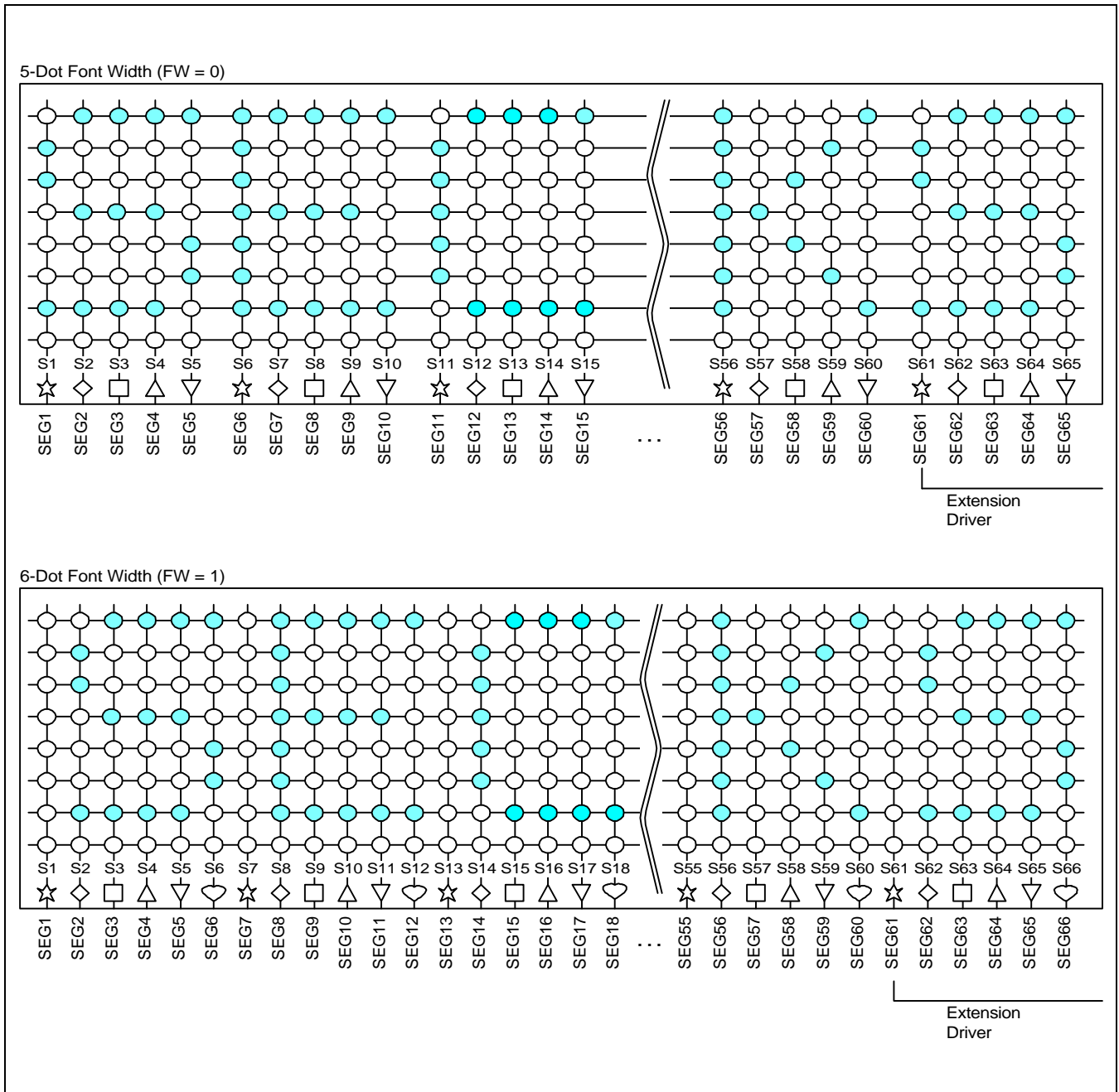
3.    "X" : don't care

**Figure 14. Relationship between SEGRAM and Segment Display**

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## INSTRUCTION DESCRIPTION

### OUTLINE

To overcome the speed difference between internal clock of S6A0073 and MPU clock, S6A0073 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. Instruction can be divided largely four kinds,

      (1) S6A0073 function set instructions ( set display methods, set data length, etc.)
      (2) address set instructions to internal RAM
      (3) data transfer instructions with internal RAM
      (4) others .
      The address of internal RAM is automatically increased or decreased by 1.
      When IE = "High", S6A0073 is operated according to Instruction Set 1 (Table 6) and
      when IE = "Low", S6A0073 is operated according to Instruction Set 2 (Table 10).

**NOTE:**  During internal operation, Busy Flag (DB7) is read High. Busy Flag check must be preceded the next instruction. When an MPU program with Busy Flag (DB7) checking is made, $1/2$ $f_{OSC}$ is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "LOW".

## (1) INSTRUCTION DESCRIPTION 1 (IE = "HIGH")

**Table 6. Instruction Set 1**

| Instruction | Instruction Code | | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RE | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | (fosc=270kHz) |
| Clear display | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20" to DDRAM, and set DDRAM address to "00H" from AC. | 1.53ms |
| Return home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.53ms |
| Power down mode | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | PD | Set power down mode bit. (PD = "1" : power down mode set, PD = "0" : power down mode disable) | 39μs |
| Entry mode set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Assign cursor moving direction, (I/D = "1": increment, I/D = "0": decrement, and display shift enable bit. (S = "1": make display shift of the enabled lines by the DS4-DS1 bits in the shift Enable instruction S = "0": display shift disable) | 39μs |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | B/D | Segment bidirectional function. (BID = "1": Seg60 →Seg1 BID = "0": Seg1 →Seg60) | |
| Display ON/OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display/cursor/blink on/off D = "1" : display on, D = "0" : display off, C = "1" : cursor on, C = "0" : cursor off, B = "1" : blink on, B = "0" : blink off. | 39μs |
| Extended function set | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | FW | B/W | NW | Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1" : 6-dot font width, FW = "0" : 5-dot font width, B/W = "1" : black/white inverting of cursor enable, B/W = "0" : black/white inverting of cursor disable. NW = "1" : 4-line display mode, NW = "0" : 1-line or 2-line display mode. | 39μs |

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## Table 6. Instruction Set 1 Continued

| Instruction | Instruction Code | | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RE | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | (fosc=270kHz) |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Cursor or display shift. S/C = "1" : display shift, S/C = "0" : cursor shift, R/L = "1" : shift to right, R/L = "0" : shift to left. | 39μs |
| Shift Enable | 1 | 0 | 0 | 0 | 0 | 0 | 1 | DS4 | DS3 | DS2 | DS1 | (when DH = "1") Determine the line for display shift . DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable. | 39μs |
| Scroll Enable | 1 | 0 | 0 | 0 | 0 | 0 | 1 | HS4 | HS3 | HS2 | SH1 | (when DH = "0") Determine the line for horizontal smooth scroll. HS1 = "1/0" : 1st line dot scroll enable/disable HS2 = "1/0" : 2nd line dot scroll enable/disable HS3 = "1/0" : 3rd line dot scroll enable/disable HS4 = "1/0" : 4th line dot scroll enable/disable. | 39μs |
| Function Set | 0 | 0 | 0 | 0 | 0 | 1 | DL | N | RE (0) | DH | REV | Set interface data length (DL = "1" : 8-bit, DL = "0" : 4-bit), numbers of display line when NW = "0", (N = "1" : 2-line, N = "0" : 1-line), extension register, RE("0"), shift/scroll enable DH = "1" : display shift enable DH = "0" : dot scroll enable. And reverse  bit REV = "1" : reverse display, REV = "0" : normal display. | 39μs |
| | 1 | 0 | 0 | 0 | 0 | 1 | DL | N | RE (1) | BE | LP | Set DL, N, RE("1") and CGRAM/SEGRAM blink enable (BE) BE = " 1/0" : CGRAM/SEGRAM blink enable/disable LP = "1" : low power mode LP = "0" : normal operation mode | 39μs |

**Table 6. Instruction Set 1 continued**

| Instruction | Instruction Code | | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | RE | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | (fosc=270kHz) |
| Set CGRAM Address | 0 | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 39µs |
| Set SEGRAM Address | 1 | 0 | 0 | 0 | 1 | X | X | AC3 | AC2 | AC1 | AC0 | Set SEGRAM address in address counter. | 39µs |
| Set DDRAM Address | 0 | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 39µs |
| Set Scroll Quantity | 1 | 0 | 0 | 1 | X | SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ0 | Set the quantity of horizontal dot scroll. | 39µs |
| Read Busy flag and Address | x | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF = "1" : busy state, BF = "0" : ready state. | 0µs |
| Write Data | X | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM / CGRAM / SEGRAM). | 43µs |
| Read Data | X | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM / CGRAM / SEGRAM). | 43µs |

**NOTE:** When an MPU program with Busy Flag (DB7) checking is mode, 1/2 $f_{OSC}$ is necessary for executing the next instruction by the falling edge of the "E" signal after the Busy Flag (DB7) goes to "low".

"X": Don't care

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### 1) Display Clear

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

### 2) Return Home: (RE = 0)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | X   |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

### 3) Power Down Mode Set: (RE = 1)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | PD  |

Power down mode enable bit set instruction. When PD = "High", it makes S6A0073 suppress current consumption except the current needed for data storage by executing next three functions.

- Make the output value of all the COM/SEG ports VDD

- Make the COM/SEG output value of extension driver VDD by setting D output to "High" and M output to "Low"

- Disable voltage converter to remove the current through the divide resistor of power supply.

This instruction can be used s power sleep mode. When PD = "Low", power down mode becomes disabled.

## 4) Entry Mode Set

(1) RE = 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | S   |

Set the moving direction of cursor and display.
I/D : Increment/decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the display of enabled line by DS1 - DS4 bits in the Shift Enable instruction is shifted to the right (I/D = "0") or to the left(I/D = "1").  But it will seem as if the cursor does not move. When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of display as the above function is not performed.

(2) RE = 1

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | BID |

Set the data shift direction of segment in the application set.
BID : Data Shift Direction of Segment
When BID = "Low", segment data shift direction is set to normal order from SEG1 to SEG100.
When BID = "High", segment data shift direction is set to reversely from SEG100 to SEG1.
By using this instruction, the efficiency of application board area can be raised.
* The BID setting instruction is recommended to be set at the same time level of function set instruction.
* DB1 bit must be set to "1".

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**5) Display ON/OFF Control ( RE = 0 )**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.
D : Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.

B : Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has frequency of 270kHz, blinking has 370 ms interval.
When B = "Low", blink is off.

**6) Extended Function Set ( RE = 1 )**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | F/W | B/W | NW |

FW : Font Width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width. The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the left most space bit of CGRAM.(refer to Figure 15)
When FW = "Low", 5-dot font width is set.

B/W : Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270kHz, inversion has 370 ms intervals.

NW : 4 Line mode enable bit
When NW = "High", 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.
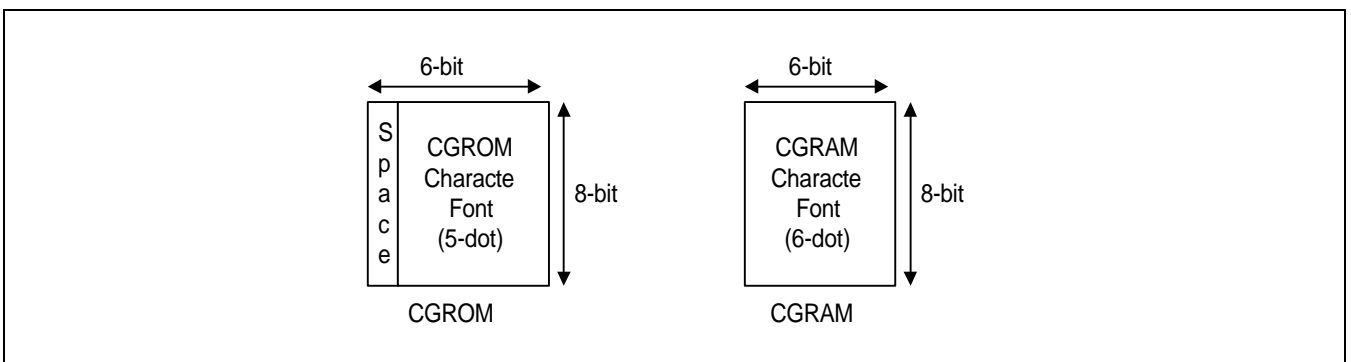


**Figure 15. 6-dot Font Width CGROM/CGRAM**

**7) Cursor or Display Shift (RE = 0)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | S/C | R/L | -   | -   |

Shift right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (refer to Table 7). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note that display shift is performed simultaneously in all the line enabled by DS1 - DS4 in the Shift Enable instruction. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed. During low power consumption mode, display shift may not be performed normally.

**Table 7. Shift Patterns according to S/C and R/L Bits**

| S/C | R/L | Operation |
|-----|-----|-----------|
| 0   | 0   | Shift cursor to the left, ADDRESS COUNTER is decreased by 1 |
| 0   | 1   | Shift cursor to the right, ADDRESS COUNTER is increased by 1 |
| 1   | 0   | Shift all the display to the left, cursor moves according to the display |
| 1   | 1   | Shift all the display to the right, cursor moves according to the display |

**8) Shift/Scroll Enable (RE = 1)**

(1) DH = 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | HS4 | HS3 | HS2 | HS1 |

HS : Horizontal Scroll per Line Enable. This instruction makes valid dot shift by a display line unit. HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line. If you want to scroll the line in 1-line display mode or the 1st line in 2-line display mode, set HS1 and HS2 to "High". If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "High". (refer to Table 8)

(2) DH = 1

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | DS4 | DS3 | DS2 | DS1 |

DS : Display Shift per Line Enable. This instruction selects shifting line to be shifted according to each line mode in display shift right/left instruction. DS1, DS2, DS3 and DS4 indicate each line to be shifted, and each shift is performed individually in each line. If you set DS1 and DS2 to "High" (enable) in 2 line mode, only the 1st line is shifted and the 2nd line is not shifted. When only DS1 = "High", only the half of the 1st line is shifted. If all the DS bits (DS1 to DS4) are set to "Low" (disable), no display is shifted.

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**Table 8. Relationship between DS and COM signal**

| Enable bit | Enabled common signal during shift | Description |
|:---:|:---:|:---:|
| HS1/DS1 | COM1 - COM8 | The part of display line that corresponds to enabled common signal can be shifted. |
| HS2/DS2 | COM9 - COM16 | |
| HS3/DS3 | COM17 - COM24 | |
| HS4/DS4 | COM25 - COM32 | |

## 9) Function Set

(1) RE = 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL  | N   | RE(0) | DH | REV |

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode. In 4-bit bus mode, it needs to transfer 4-bit data by two times.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
At this instruction, RE must be "Low".

DH : Display shift enable selection bit.
When DH = "High", enables display shift per line.
When DH = "Low", enables smooth dot scroll.
This bit can be accessed only when IE pin input is "High".

REV : Reverse enable bit
When REV = "High", all the display data are reversed. i.e., all the white dots become black and black dots become white. When REV = "Low", the display mode set normal display.

(2) RE = 1

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-------|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL  | N   | RE(0) | DH  | REV |

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it is required to transfer 4-bit data by two times.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, BID bit, HS/DS bits of
shift/scroll enable instruction and BE bits of function set register can be accessed.

BE : CGRAM/SEGRAM data blink enable bit
BE = "High", makes user font of CGRAM and segment of SEGRAM blinking. The quantity of blink is assigned the
highest 2 bit of CGRAM/SEGRAM.

LP : Low power consumption mode enable bit
When EXT input is "Low"(without extension driver) and LP bit is set to "High", S6A0073 operates in low power
consumption mode.
During 1-line mode S6A0073 operates on a 4-division clock, and in 2-line or 4-line mode it operates on a 2-
division clock. According to this instruction, execution time becomes 4 or 2 times longer.
Note not to use display shift instruction, as it may result incorrect operation.
And the frame frequency is lower to 5/6 times lower than that of normal operation.

**10) Set CGRAM Address (RE = 0)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.
This instruction makes CGRAM data available from MPU.

**11) Set SEGRAM Address (RE = 1)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | X | X | AC3 | AC2 | AC1 | AC0 |

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

**12) Set DDRAM Address (RE = 0)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".
In 4-line display mode (NW = 1), DDRAM address is from "00H" to "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" to "53H" in the 3rd line and  from "60H" to "73H" in the 4th line.

**13) Set Scroll Quantity (RE = 1)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | X | SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ0 |

As set SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. (refer to Table 9).
In this case S6A0073 can show hidden areas of DDRAM by executing smooth scroll from 1 to 48 dots.

**Table 9. Scroll Quantity According to HDS bits**

| SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ0 | Function |
|-----|-----|-----|-----|-----|-----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | No shift |
| 0 | 0 | 0 | 0 | 0 | 1 | shift left by 1-dot |
| 0 | 0 | 0 | 0 | 1 | 0 | shift left by 2-dot |
| 0 | 0 | 0 | 0 | 1 | 1 | shift left by 3-dot |
| : | : | : | : | : | : | : |
| 1 | 0 | 1 | 1 | 1 | 1 | shift left by 47-dot |
| 1 | 1 | X | X | X | X | shift left by 48-dot |

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## 14) Read Busy Flag & Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 1   | BF  | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether S6A0073 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF to be Low, which by then the next instruction can be performed. In this instruction the value of address can also be read.

## 15) Write Data to RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction :
DDRAM address set, CGRAM address set, SEGRAM address set.
RAM set instruction can also determines the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

## 16) Read Data from RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, as the direction of AC is not determined.
If RAM data read several times without RAM address set instruction before read operation, the correct RAM data can be obtained from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, AC is increased/decreased by 1 like read operation after this.
In this time, AC indicates the next address position, but the previous data can only be read  by instruction.

## (2) INSTRUCTION DESCRIPTION 2 (IE = "LOW")

### Table 10. Instruction Set 2

| Instruction | RE | Instruction Code | | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | (fosc=270kHz) |
| Clear Display | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | Write "20H" to DDRAM. and set DRAM address to "00H" from AC. | 1.53ms |
| Return Home | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.53ms |
| Entry Mode Set | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | | Assign cursor moving direction. I/D = "1" : increment, I/D = "0" : decrement. and display shift enable bit. S = "1" :make entire display shift of all lines during DDRAM write, S = "0":display shift disable | 39μs |
| Display ON/OFF Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | | Set display/cursor/blink on/off D = "1" : display on, D = "0" : display off, C = "1" : cursor on, C = "0" : cursor off, B = "1" : blink on, B = "0" : blink off. | 39μs |
| Extended function set | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | FW | BW | NW | | Assign font width, black/white inverting of cursor, and 4-line display mode  control bit. FW = "1" : 6-dot font width, FW = "0" : 5-dot font width, B/W = "1" : black/white inverting of cursor enable, B/W = "0" : black/white inverting of cursor disable NW = "1" : 4-line display mode, NW = "0" : 1-line or 2-line display mode | 39μs |
| Cursor or Display Shift | 0 | 0 | 0 | 00 | 0 | 0 | 1 | S/C | R/L | X | X | | Cursor or display shift. S/C = "1" : display shift, S/C = "0" : cursor shift, R/L = "1" : shift to right, R/L = "0" : shift to left | 39μs |

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## Table 10. Instruction Set 2 (continued)

| Instruction | RE | Instruction Code | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | (fosc=270kHz) |
| Scroll Enable | 1 | | | | | | 1 | HS4 | HS3 | HS2 | HS1 | Determine the line for horizontal smooth scroll.<br>HS1 = "1/0" :<br>1st line dot scroll  enable/disable<br>HS2 = "1/0" :<br>2nd line dot scroll enable/disable<br>HS3 = "1/0" :<br>3rd line dot scroll  enable/disable<br>HS4 = "1/0" :<br>4th line dot scroll enable/disable | 39μs |
| Function Set | 0 | | | | | 1 | DL | N | RE (0) | X | X | Set interface data length<br>DL = "1" : 8-bit,<br>DL = "0" : 4-bit<br>numbers of display line when NW = "0",<br>N = "1" : 2-line,<br>N = "0" : 1-line<br>extension register, RE("0"), | 39μs |
| | 1 | | | | | 1 | DL | N | RE (1) | BE | LP | Set DL, N, RE("1") and<br>CGRAM/SEGRAM blink enable (BE)<br>BE = " 1/0" : CGRAM/SEGRAM  blink enable/disable<br>LP = "1" : low power mode<br>LP = "0" : normal operation mode | 39μs |
| Set CGRAM Address | 0 | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. | 39μs |
| Set SEGRAM Address | 1 | 0 | 0 | 0 | 1 | X | X | AC3 | AC2 | AC1 | AC0 | Set SEGRAM address in address counter. | 39μs |

**Table 10. Instruction Set 2 (continued)**

| Instruction | RE | Instruction Code | | | | | | | | | | Description | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | (fosc=270kHz) |
| Set DDRAM Address | 0 | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. | 39μs |
| Set Scroll Quantinty | 1 | | | 1 | X | SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ1 | Set the quantity of horizontal dot scroll. | 39μs |
| Read Busy flag and Address | X | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF = "1" : busy state, BF = "0" : ready state. | 0μs |
| Write Data | X | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM / CGRAM / SEGRAM). | 43μs |
| Read Data | X | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM / CGRAM / SEGRAM). | 43μs |

**NOTE:** When an MPU program with Busy Flag (DB7) checking is made, 1/2 $f_{OSC}$ (is necessary) for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "low".

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**1) Display Clear**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. And entry mode is set to increment mode (I/D = "1").

**2) Return Home**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | X   |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

**3) Entry Mode Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | S   |

Set the moving direction of cursor and display.
I/D : Increment / decrement of DDRAM address (cursor or blink)
When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM/SEGRAM operates the same as DDRAM, when read from or write to CGRAM/SEGRAM.

When S = "High", after DDRAM write, the entire display of all lines is shifted to the right (I/D = "low") or to the left(I/D = "high").    But it will seem as if the cursor is not moving. When S = "Low", or DDRAM read, or CGRAM/SEGRAM read/write operation, shift of entire display is not performed.

## 4) Display ON/OFF Control ( RE = 0 )

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   |

Control display/cursor/blink ON/OFF 1 bit register.
D : Display ON/OFF control bit
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.

C : Cursor ON/OFF control bit
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register preserves its data.

B : Cursor Blink ON/OFF control bit
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position. If fosc has 270kHz frequency, blinking has 370ms interval.
When B = "Low", blink is off.

## 5) Extended Function Set ( RE = 1 )

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | FW  | BW  | NW  |

FW : Font Width control
When FW = "High", display character font width is assigned to 6-dot and execution time becomes 6/5 times than that of 5-dot font width. The user font, specified in CGRAM, is displayed into 6-dot font width, bit-5 to bit-0,including the leftmost space bit of CGRAM.(refer to Figure 16). When FW = "Low", 5-dot font width is set.

B/W : Black/White Inversion enable bit
When B/W = "High", black/white inversion at the cursor position is set. In this case C/B bit of display ON/OFF control instruction becomes don't care condition. If fosc has frequency of 270kHz, inversion has 370ms intervals.

NW : 4 Line mode enable bit
When NW = "High", 4 line display mode is set. In this case N bit of function set instruction becomes don't care condition.

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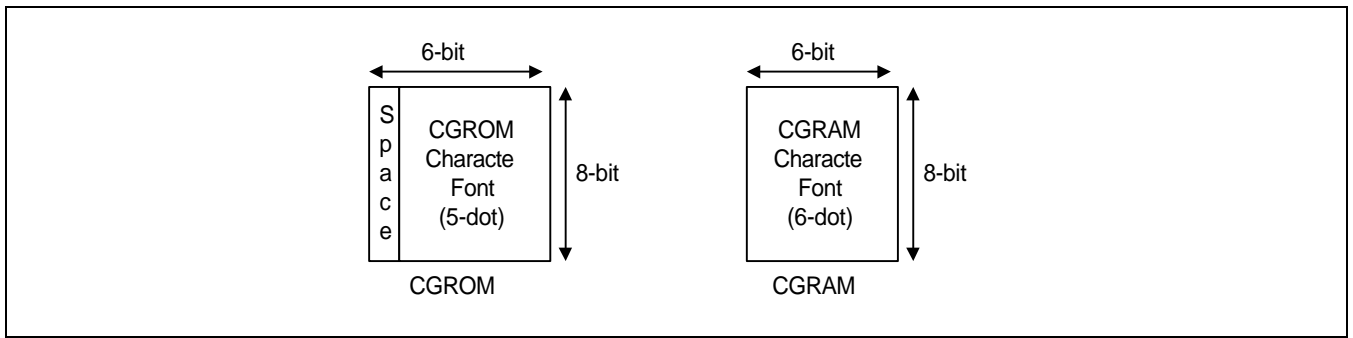
**Figure 16. 6-dot Font Width CGROM/CGRAM**

## 6) Cursor or Display Shift (RE = 0)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | SC | R/L | - | - |

Shift right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data (refer to Table 7). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. In 4-line mode, cursor moves to the next line, only after every 20th digit of the current line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

**Table 11. Shift Patterns According to S/C and R/L bits**

| S/C | R/L | Operation |
|-----|-----|-----------|
| 0 | 0 | Shift cursor to the left, ADDRESS COUNTER is decreased by 1 |
| 0 | 1 | Shift cursor to the right, ADDRESS COUNTER is increased by 1 |
| 1 | 0 | Shift all the display to the left, cursor moves according to the display |
| 1 | 1 | Shift all the display to the right, cursor moves according to the display |

## 7) Scroll Enable (RE = 1)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | HS4 | HS3 | HS2 | HS1 |

HS : Horizontal Scroll per Line Enable
This instruction makes valid dot shift by a display line unit.
HS1, HS2, HS3 and HS4 indicate each line to be dot scrolled, and each scroll is performed individually in each line.
If the line in 1-line display mode or the 1st line in 2-line display mode is to be scrolled, set HS1 and HS2 to "high". If the 2nd line scroll is needed in 2-line mode, set HS3 and HS4 to "high". (Refer to table 8)

## 8) Function Set

(1) RE = 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2   | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-------|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL  | N   | RE(0) | -   | -   |

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.
When 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
At this instruction, RE must be "Low".

(2) RE = 1

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL  | N   | RE(1) | RE | LP |

DL : Interface data length control bit
When DL = "High", it means 8-bit bus mode with MPU.
When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.  When 4-bit bus mode, it is required to transfer 4-bit data twice.

N : Display line number control bit
It is variable only when NW bit of extended function set instruction is Low.
When N = "Low", 1-line display mode is set.
When N = "High", 2-line display mode is set.
When NW = "High", N bit is invalid, it means 4-line mode independent of N bit.

RE : Extended function registers enable bit
When RE = "High", extended function set registers, SEGRAM address set registers, HS bits of scroll enable instruction and BE bits of function set register can be accessed.

BE : CGRAM/SEGRAM data blink enable bit
BE = "High", makes user font of CGRAM and segment of SEGRAM blinking. The quantity of blink is assigned the highest 2 bit of CGRAM/SEGRAM.

LP : Low power consumption mode enable bit
When EXT port input is "Low"(without extension driver) and LP bit is set to "High", S6A0073 operates in low power  consumption mode.
During 1-line mode S6A0073 operates on a 4-division clock, and in 2-line or 4-line mode it operates on a 2-division clock.  According to this instruction, execution time becomes 4 or 2 times longer.
Note not to use display shift instruction, it may happen wrong operation.
And the frame frequency is lower to 5/6 than that of normal operation.

### 9) Set CGRAM Address (RE = 0)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

**10) Set SEGRAM Address (RE = 1)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | X | X | AC3 | AC2 | AC1 | AC0 |

Set SEGRAM address to AC.
This instruction makes SEGRAM data available from MPU.

**11) Set DDRAM Address (RE = 0)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.
This instruction makes DDRAM data available from MPU.
In 1-line display mode (N = 0, NW = 0), DDRAM address is from "00H" to "4FH".
In 2-line display mode (N = 1, NW = 0), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".
In 4-line display mode (NW = 1), DDRAM address is from "00H" to "13H" in the 1st line, from "20H" to "33H" in the 2nd line, from "40H" to "53H" in the 3rd line and  from "60H" to "73H" in the 4th line.

**12) Set Scroll Quantity (RE = 1)**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | X | SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ0 |

Setting SQ5 to SQ0, horizontal scroll quantity can be controlled in dot units. (refer to Table 12). In this case S6A0073 execute dot smooth scroll from 1 to 48 dots.

**Table 12. Scroll Quantity According to HDS bits**

| SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ0 | Function |
|-----|-----|-----|-----|-----|-----|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | No shift |
| 0 | 0 | 0 | 0 | 0 | 1 | shift left by 1-dot |
| 0 | 0 | 0 | 0 | 1 | 0 | shift left by 2-dot |
| 0 | 0 | 0 | 0 | 1 | 1 | shift left by 3-dot |
| : | : | : | : | : | : | : |
| 1 | 0 | 1 | 1 | 1 | 1 | shift left by 47-dot |
| 1 | 1 | X | X | X | X | shift left by 48-dot |

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## 13) Read Busy Flag & Address

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether S6A0073 is in internal operation or not. If the resultant BF is High, the internal operation is in progress and should wait until BF becomes "LOW", which by then the next instruction can be performed. In this instruction value of address counter can also be read.

## 14) Write data to RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Write binary 8-bit data to DDRAM/CGRAM/SEGRAM.
The selection of RAM from DDRAM, CGRAM, or SEGRAM, is set by the previous address set instruction :
DDRAM address set, CGRAM address set, SEGRAM address set. RAM set instruction can also determines the AC direction to RAM.
After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

## 15) Read data from RAM

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Read binary 8-bit data from DDRAM/CGRAM/SEGRAM.
The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If the RAM data several is read times without RAM address set instruction before read operation, the correct RAM data from the second, but the first data would be incorrect, as there is no time margin to transfer RAM data.
In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register.
After read operation address counter is automatically increased/decreased by 1 according to the entry mode.
After CGRAM/SEGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 as in read operation after this. In this time, AC indicates the next address position, but the previous data can only be read by read instruction.

## INTERFACE WITH MPU

S6A0073 can transfer data in bus mode (4-bit or 8-bit) or serial mode with MPU. Hence, both types 4 or 8-bit MPU can be used. In case of 4-bit bus mode, data transfer is performed by two times to transfer 1 byte data.

(1) When interfacing data length are 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times.
Busy Flag outputs "High" after the second transfer are ended.

(2) When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

(3) If IM is set to "Low", serial transfer mode is set.

## INTERFACE WITH MPU IN BUS MODE

### 1) Interface with 8-bits MPU

If 8-bits MPU is used, S6A0073 can connect directly with that. In this case, port E, RS, R/W and DB0 to DB7 need to interface each other. Example of timing sequence is shown below.
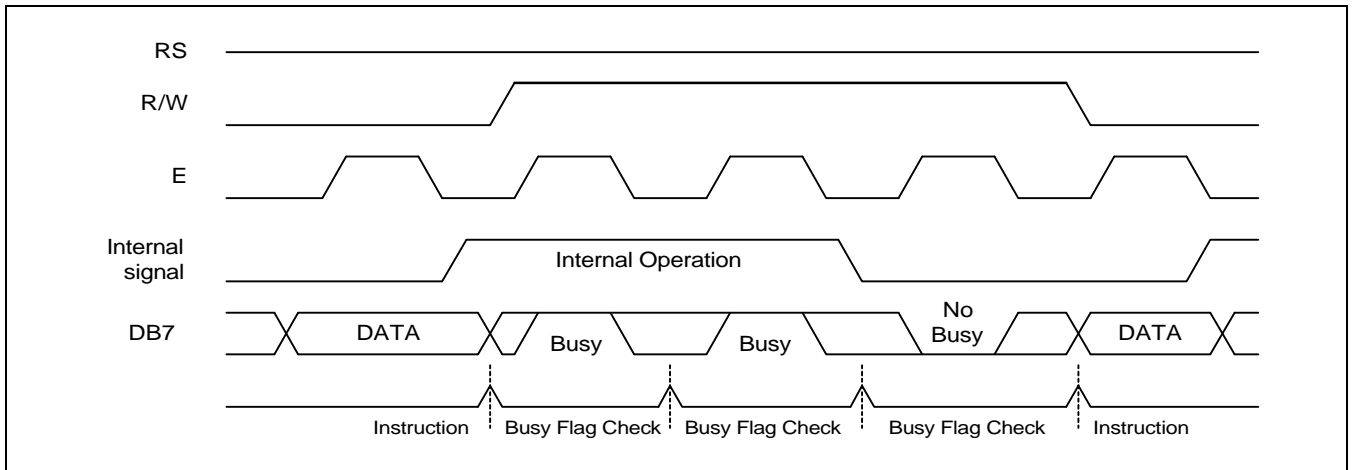


**Figure 17. Example of 8-bit Bus Mode Timing Sequence**

### 2) Interface with 4-bits MPU

If 4-bits MPU is used, S6A0073 can connect directly with this. In this case, E, RS, R/W and DB4 to DB7 need to interface each other. The transfer is performed by twice. Example of timing sequence is shown below.
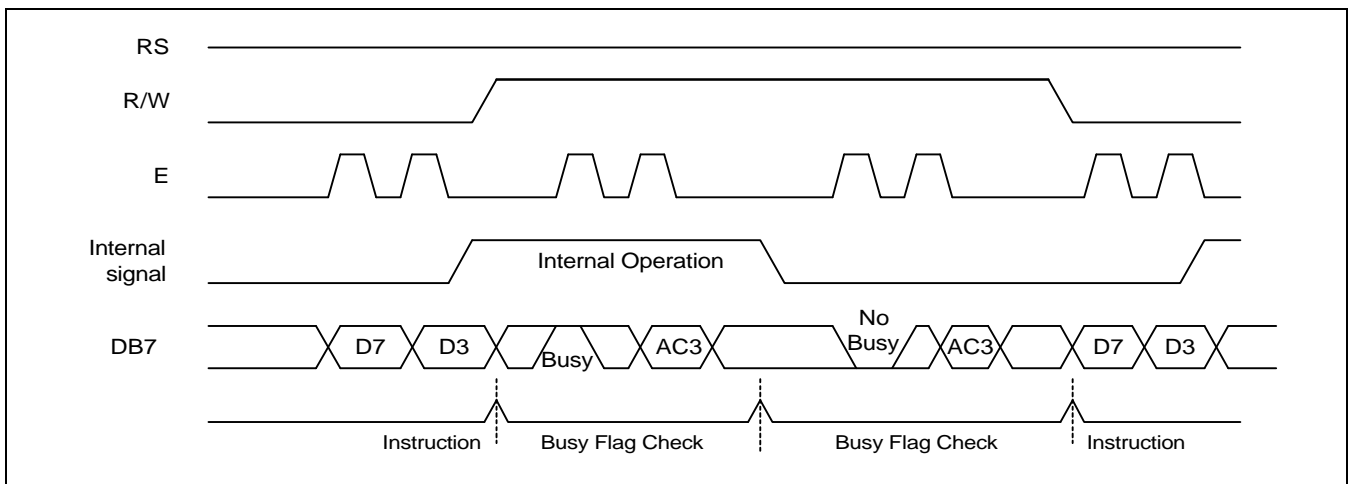


**Fig 18. Example of 4-bit Bus Mode Timing Sequence**

**Interface with MPU in Serial Mode**

When IM input is "Low", serial interface mode is started. At this time, all three ports, SCLK (synchronizing transfer clock), SID (serial input data), and SOD (serial output data), are used. If S6A0073 is to be used with other chips, chip select port (CS) can be used. By setting CS to "Low", S6A0073 can receive SCLK input. If CS is set to "High", S6A0073 reset the internal transfer counter.

Before transfer real data, start byte has to be transferred. It is composed of succeeding 5 "High" bits, register read write control bit (R/W), register selection bit (RS) and end bit that indicates the end of start byte. Whenever succeeding 5 "High" bits are detected by S6A0073, it resets the serial transfer counter and prepares to receive next information. The next input data is the register selection bit which determines which register will be used, and read write control bit that determine the direction of data. Then end bit is transferred, which must have "Low" value to show the end of start byte. (refer to Figure 19, Figure 20)

**(1) Write Operation (R/W = 0)**

After start byte is transferred from MPU to S6A0073, 8-bit data is transferred which is divided into 2 bytes, each byte has 4 bit's real data and 4 bit's partition token data. For example, if real data is "10110001" (D0 - D7), then serially transferred data becomes "1011 0000 0001 0000" where 2nd and 4th 4 bits must be "0000" for safe transfer. To transfer several bytes continuously without changing RS bit and RW bit, start byte transfer is needed only at first starting time, I, e, after first start byte is transferred, real data succeeding can be transferred.

**(2) Read Operation (R/W = 1)**

After start byte is transferred to S6A0073, MPU can receive 8-bit data through the SOD at a time from the LSB. Waiting time is needed to insert between start byte and data reading, as internal reading from RAM requires some delay. Continuous data reading is possible such as serial write operation. It also needs only one start bytes, only if some delay between reading operations of each byte is inserted. During the reading operation, S6A0073 observes succeeding 5 "High" from MPU. If it is detected, S6A0073 restarts serial operation at once and prepares to receive RS bit. So in continuous reading operation, SID port must be "low".

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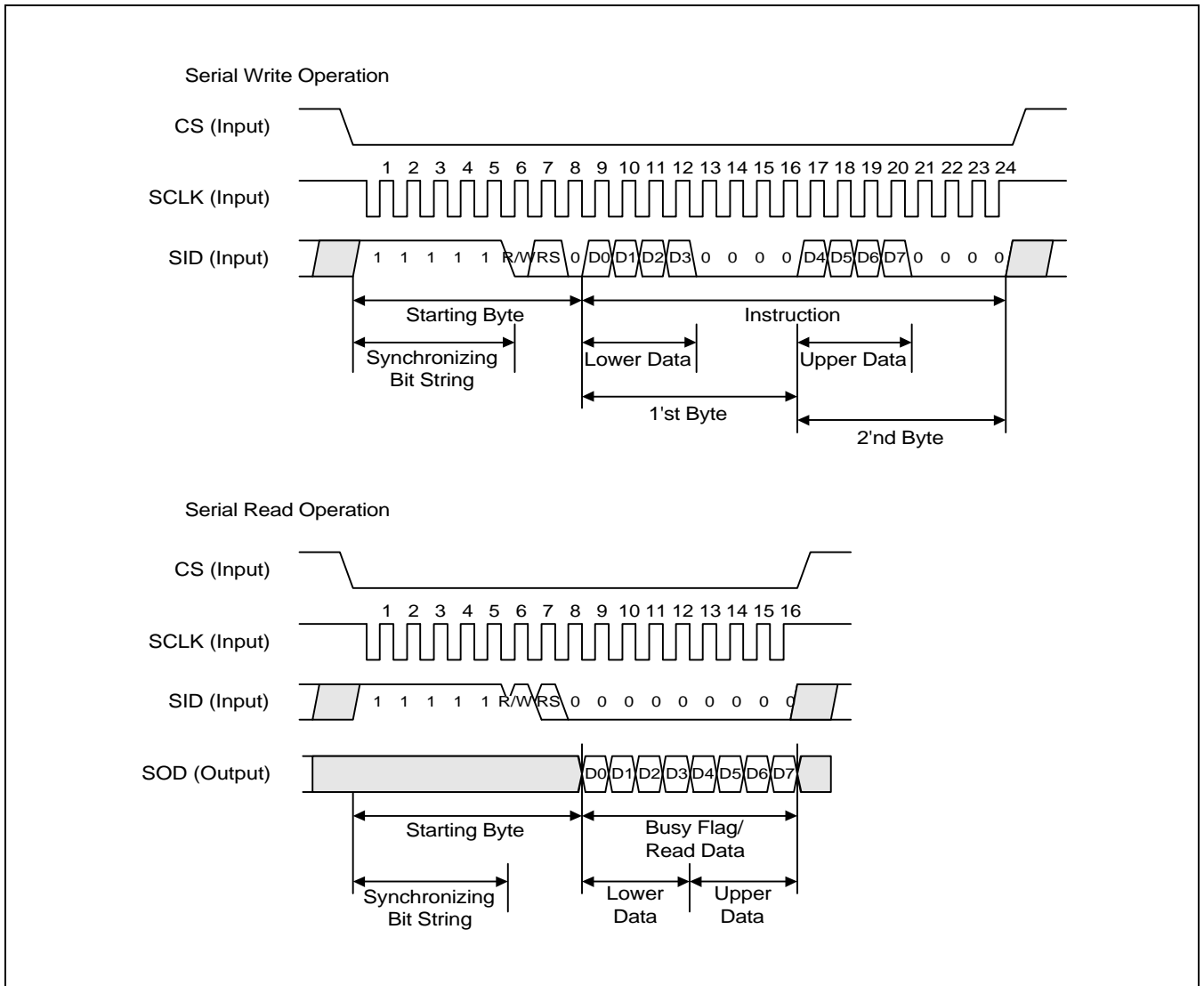
**Figure 19. Timing Diagram of Serial Data Transfer**
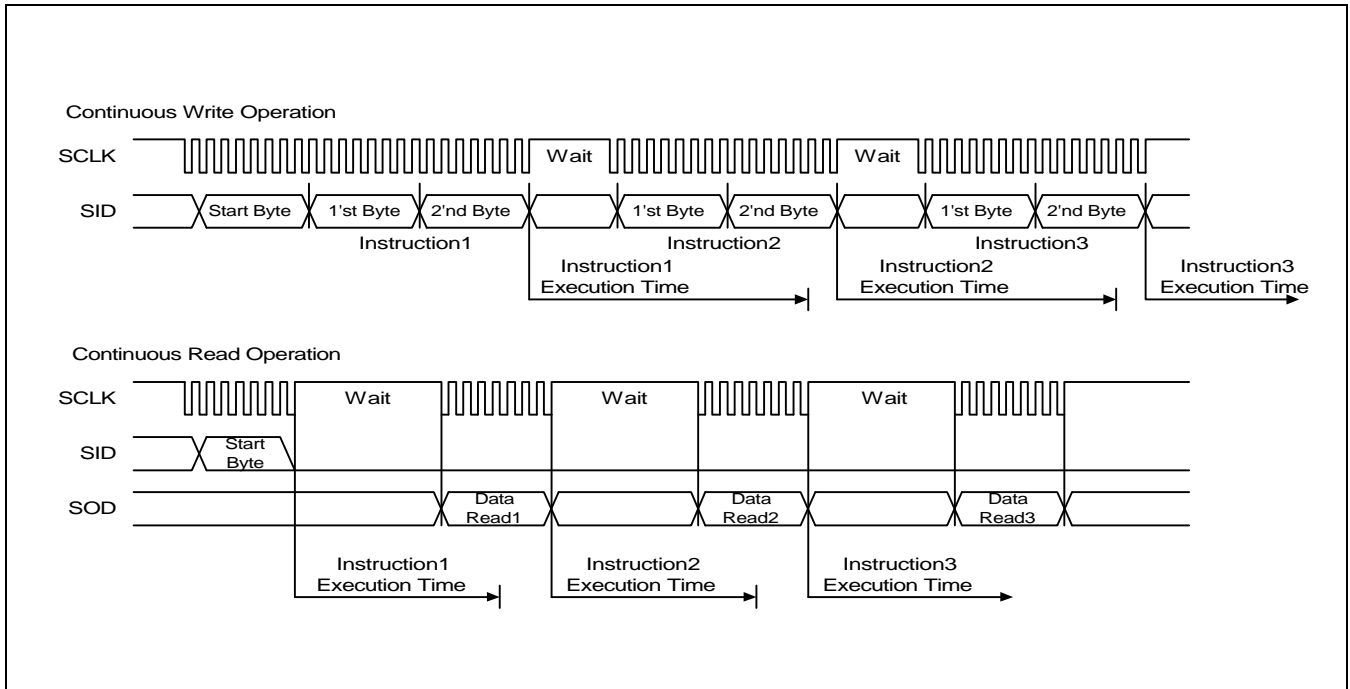
**Fig 20. Timing Diagram of Continuous Data Transfer**

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## APPLICATION INFORMATION ACCORDING TO LCD PANEL

**1) LCD Panel: 24 Character x 1-line Format (5-dot Font,1/17 Duty)**
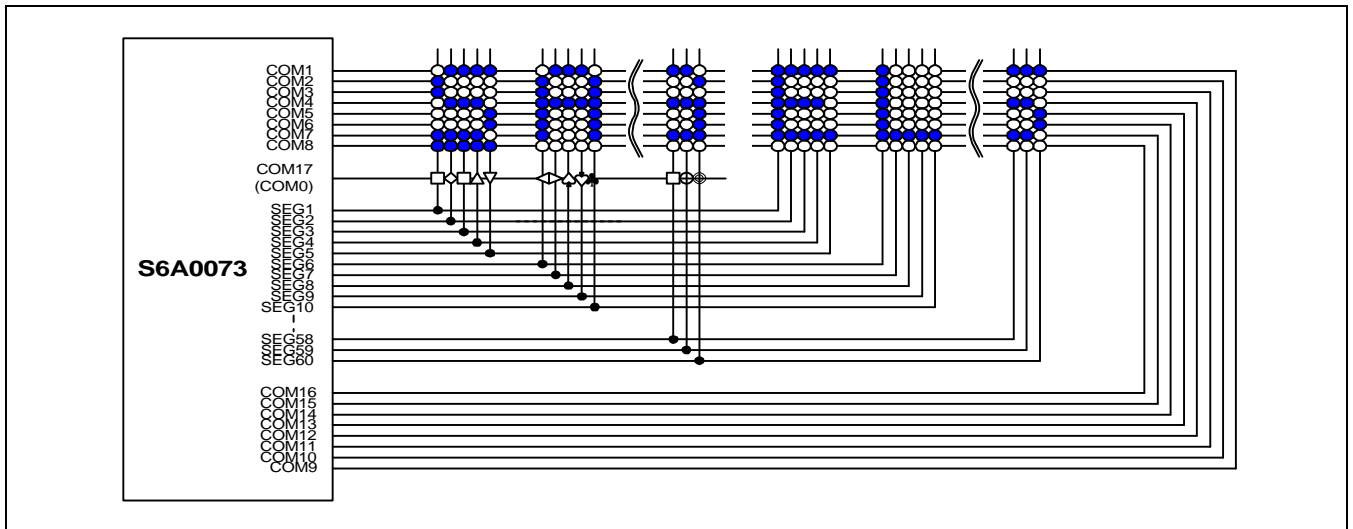


**2) LCD Panel: 24 Character x 2-line Format (5-dot Font, 1/33 Duty)**

**3) LCD Panel: 12 Character x 4-line Format (5-dot Font, 1/33 Duty)**
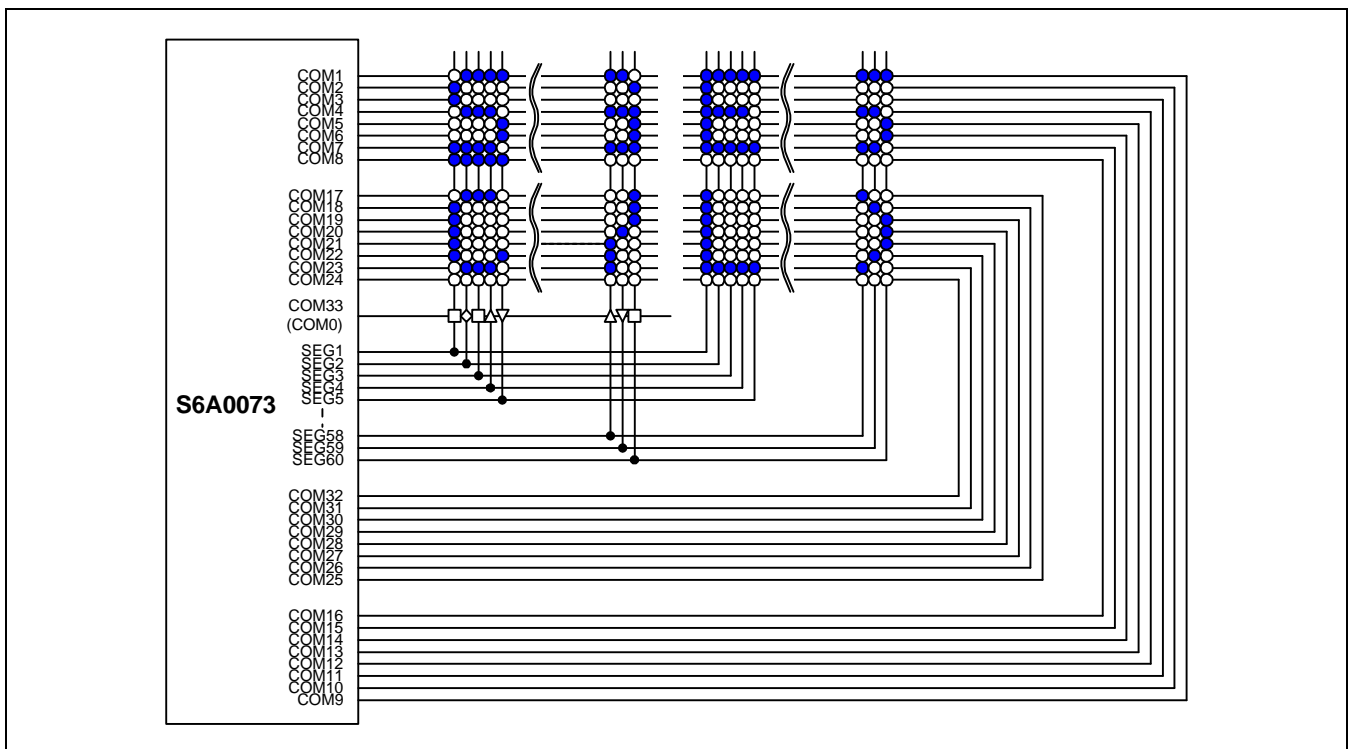
**4) LCD Panel: 10 Character ´ 4-line Format (6-dot Font, 1/33 Duty)**
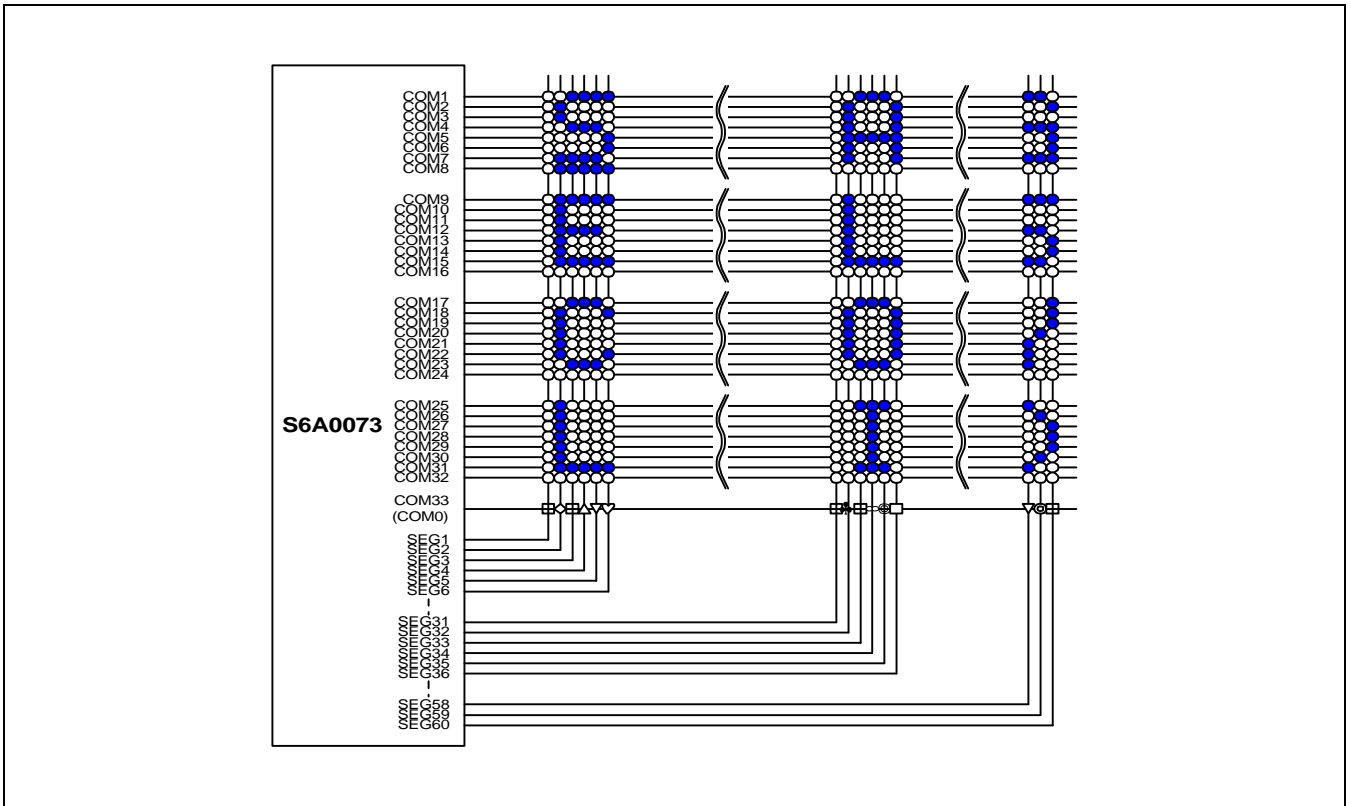
## 5) LCD Panel: 20 Character ´ 4-line Format (5-dot Font, 1/33 Duty)
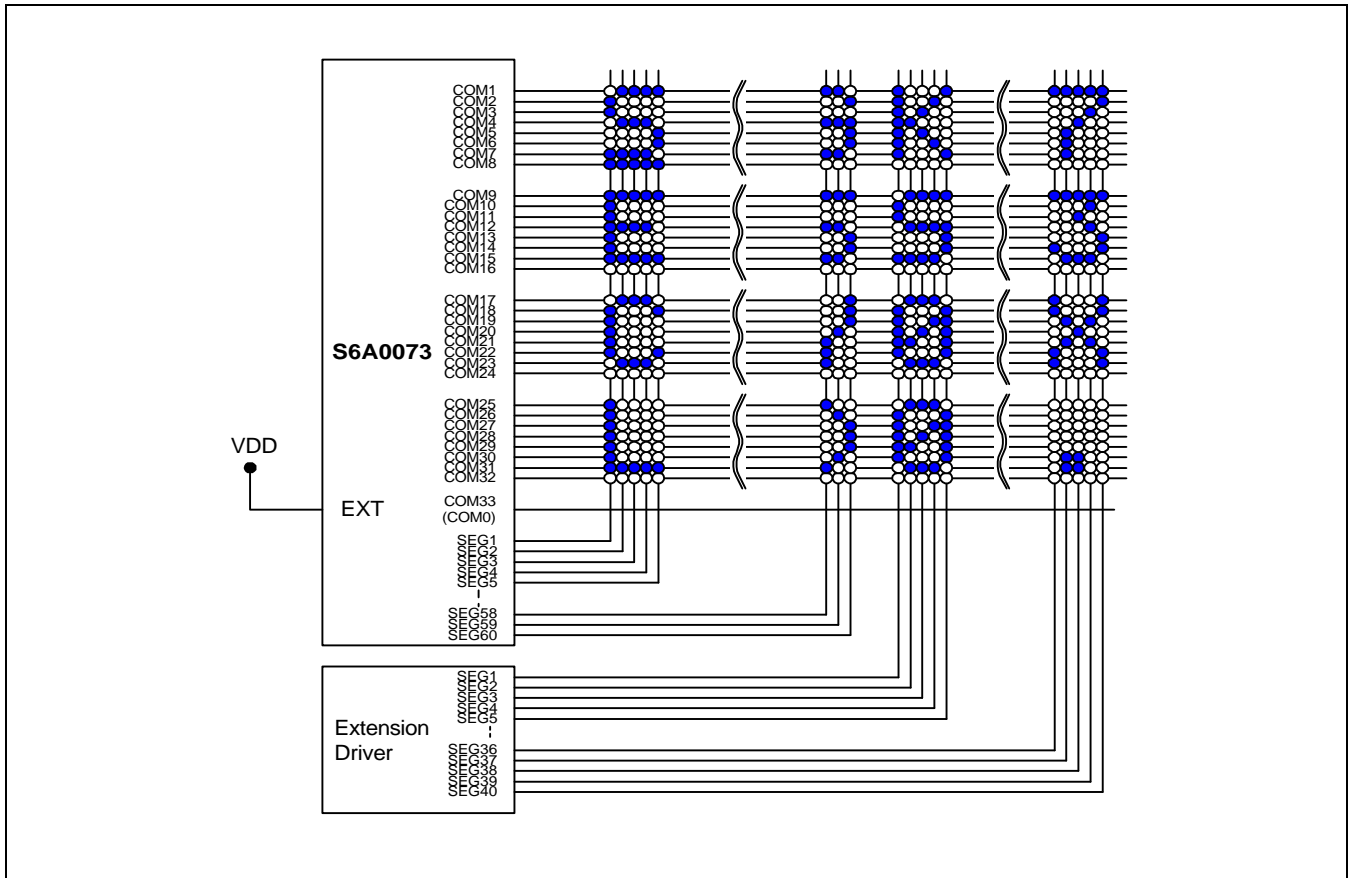
**INITIALIZING**

1) Initializing by Internal Reset Circuit

When the power is turned on, S6A0073 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

(1) Display Clear instruction
Write "20H" to all DDRAM

(2) Set Functions instruction
DL = 1 : 8-bit bus mode
N  = 1 : 2-line display mode
RE = 0 : Extension register disable
BE = 0 : CGRAM/SEGRAM blink OFF
LP = 0 : Operate in normal mode (Not in Low Power Mode)
DH = 0 : Horizontal scroll enable
REV = 0 : Normal display mode (Not reversed display)

(3)Control Display ON/OFF instruction
D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF

(4) Set Entry Mode instruction
I/D = 1 : Increment by 1
S  = 0 : No entire display shift
BID = 0 : Normal direction segment port

(5) Set Extension Function instruction
FW  = 0 : 5-dot font width character display
B/W = 0 : Normal cursor (8th line)
NW  = 0 : Not 4-line display mode, 2-line mode is set because of N("1")

(6) Enable Scroll/Shift instruction
HS = 0000 : Scroll per line disable
DS = 0000 : Shift per line disable

(7) Set scroll Quantity instruction
SQ = 000000 : Not scroll


2) Initializing by Hardware RESET input

When RESET pin = "Low", S6A0073 can be initialized like the case of power on reset. During the power on reset operation, this pin is ignored.

## INITIALIZING BY INSTRUCTION

### 1) 8-bit Interface Mode

```
                    ┌─────────────────────┐
                    │      Power On        │
                    └─────────────────────┘
                               │
                               ▼
        ┌──────────────────────────────────────────┐
        │ Wait for more than 20ms after V_DD rises to 4.5V │        Condition: fosc = 270kHz
        │ Wait for more than 30ms after V_DD rises to 2.7V │
        └──────────────────────────────────────────┘
```

| Function Set |
| --- |

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 1 | DL(1) | N | 0 | X | X |

| | 0 | 4-bit interface |
| --- | --- | --- |
| DL | 1 | 8-bit interface |

| Wait for more than 39μs |
| --- |

| | 0 | 1-line mode |
| --- | --- | --- |
| N | 1 | 2-line mode |

| Display ON/OFF Control |
| --- |

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

| | 0 | Display off |
| --- | --- | --- |
| D | 1 | Display on |

| | 0 | Cursor off |
| --- | --- | --- |
| C | 1 | Cursor on |

| Wait for more than 39μs |
| --- |

| | 0 | Blink off |
| --- | --- | --- |
| B | 1 | Blink on |

| Display Clear |
| --- |

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Wait for more than 1.58ms |
| --- |

| | 0 | Decrement mode |
| --- | --- | --- |
| I/D | 1 | Increment mode |

| Entry Mode Set |
| --- |

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

| | 0 | Entire shift off |
| --- | --- | --- |
| S | 1 | Entire shift on |

| Initialization End |
| --- |

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## 2) 4-bit Interface Mode

```
┌─────────────────────┐
│      Power On        │
└─────────────────────┘
           │
           ▼
┌──────────────────────────────────────────────┐
│ Wait for more than 20ms after VDD rises to 4.5V │
│ Wait for more than 30ms after VDD rises to 2.7V │
└──────────────────────────────────────────────┘
```

Condition: fosc = 270kHz

| DL | 0 | 4-bit interface |
|----|---|-----------------|
|    | 1 | 8-bit interface |

| N | 0 | 1-line mode |
|---|---|-------------|
|   | 1 | 2-line mode |

**Function Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL(0) | X | X | X | X |

Wait for more than 39μs

**Function Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 0   | X   | X   | X   | X   |
| 0  | 0   | N   | 0   | X   | X   | X   | X   | X   | X   |

Wait for more than 39μs

**Display ON/OFF Control**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | X   | X   | X   | X   |
| 0  | 0   | 1   | D   | C   | B   | X   | X   | X   | X   |

| D | 0 | Display off |
|---|---|-------------|
|   | 1 | Display on  |

| C | 0 | Cursor off |
|---|---|------------|
|   | 1 | Cursor on  |

| B | 0 | Blink off |
|---|---|-----------|
|   | 1 | Blink on  |

Wait for more than 39μs

**Clear Display**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | X   | X   | X   | X   |
| 0  | 0   | 0   | 0   | 0   | 1   | X   | X   | X   | X   |

Wait for more than 1.53ms

**Entry Mode Set**

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | X   | X   | X   | X   |
| 0  | 0   | 0   | 1   | I/D | SH  | X   | X   | X   | X   |

| I/D | 0 | Decrement mode |
|-----|---|----------------|
|     | 1 | Increment mode |

| SH | 0 | Entire shift off |
|----|---|------------------|
|    | 1 | Entire shift on  |

```
┌─────────────────────┐
│  Initialization End  │
└─────────────────────┘
```

# EXAMPLE OF INSTRUCTION AND DISPLAY CORRESPONDENCE

**1) IE = "Low"**

1. Power supply on: Initialized by the internal power on reset circuit

LCD DISPLAY

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|    |     |     |     |     |     |     |     |     |     |

2. Function Set: 8-bit, 1-line, RE (0)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 0   | 0   | X   | X   |

3. Display ON/OFF Control: Display/Cursor on

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1   | 0   |

_

4. Entry Mode Set: Increment

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 0   |

_

5. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 1   |

S_

6. Write Data to DDRAM: Write A

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 0   | 0   | 0   | 1   |

SA_

7. Write Data to DDRAM: Write M

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | 1   |

SAM_

8. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 1   |

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9. Write Data to DDRAM: Write U

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 1   | 0   | 1   |

LCD DISPLAY

SAMSU_

10. Write Data to DDRAM: Write N

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 1   | 0   |

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11. Write Data to DDRAM: Write G

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 1   | 1   |

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12. Cursor or Display Shift: Cursor shift to right

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 0   | 1   | X   | X   |

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13. Entry Mode Set: Entire Display Shift Enable

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 0   |

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14. Write Data to DDRAM: Write K

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 1   | 0   | 1   | 1   |

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15. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 1   |

MSUNG KS_

16. Write Data to DDRAM: Write 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 0   | 1   | 1   | 0   | 0   | 0   | 0   |

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17. Write Data to DDRAM: Write 0

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 0   | 1   | 1   | 0   | 0   | 0   | 0   |

LCD DISPLAY

**UNG KS00_**

18. Write Data to DDRAM: Write 7

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 0   | 1   | 1   | 0   | 1   | 1   | 1   |

**NG KS007_**

19. Write Data to DDRAM: Write 2

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 0   | 1   | 1   | 0   | 0   | 1   | 0   |

**G KS0073_**

20. Cursor or Display Shift: Cursor shift left

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 0   | 0   | x   | x   |

**G KS0073**

21. Write Data to DDRAM: Write 8

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 0   | 1   | 1   | 0   | 0   | 1   | 1   |

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22. Return Home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | x   |

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23. Clear Display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

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## 2) IE = "High"

1. Power Supply on: Initialized by the internal power on reset circuit

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|    |     |     |     |     |     |     |     |     |     |

2. Function Set: 8-bit, RE(1)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 1   | 1   | 0   | 0   |

3. Extended Function Set: 5-font, 4-line

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | 0   | 0   | 1   |

4. Function Set: RE(0)

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 1   | 0   | 0   | 0   |

5. Display ON/OFF Control: Display/Cursor on

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | 1   | 1   | 0   |

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6. Write Data to DDRAM: Write S

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 1   |

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7. Write Data to DDRAM: Write A

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 0   | 0   | 0   | 1   |

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12. Write Data to DDRAM: Write G

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 0   | 1   | 1   | 1   |

13. Set DDRAM Address 20H

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 1   | 0   | 1   | 0   | 0   | 0   | 0   | 0   |

14. Write Data to DDRAM: Write K

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 1   | 0   | 1   | 1   |

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19. Write Data to DDRAM: Write 3

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 0   | 1   | 1   | 0   | 1   | 1   | 1   |

20. Set DDRAM Address 40H

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 1   | 1   | 0   | 0   | 0   | 0   | 0   | 0   |

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| **SAMSUNG**<br>**K_** | |
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21. Write Data to DDRAM: Write L

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 0   | 1   | 1   | 0   | 0   |

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30. Write Data to DDRAM: Write R

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 0   |

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31. Set DDRAM Address 60H

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 1   | 1   | 1   | 0   | 0   | 0   | 0   | 0   |

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43. Write Data to DDRAM: Write R

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0   | 0   | 1   | 0   | 1   | 0   | 0   | 1   | 0   |

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```

44. Function Set: RE("0"), DH("1")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 1   | 0   | 1   | 0   |

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45. Function Set: RE("1")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 1   | 1   | 0   | 0   |

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46. Shift/Scroll Enable: DS4("1"), DS3/2/1("0")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 1   | 0   | 0   | 0   |

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47. Function Set: RE("0")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | 1   | 1   | 0   | 1   | 0   |

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48. Cursor or Display Shift: Display shift to left

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 1   | 0   | x   | x   |

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49. Cursor or Display Shift: Display shift to left

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 1   | 0   | x   | x   |

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50. Cursor or Display Shift: Display shift to left

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 1   | 0   | x   | x   |

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51. Cursor or Display Shift: Display shift to left

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | 1   | 0   | x   | x   |

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52. Return Home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

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53. Function Set: RE("0), REV("1")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |

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54. Cursor or Display Shift: Display shift to right

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | x | x |

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55. Cursor or Display Shift: Display shift to right

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | x | x |

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56. Return Home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

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57. Function Set: RE("0"), REV("0")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

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58. Function Set: RE("1")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |

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59. Entry Mode Set: BID("1")

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

60. Write Data to DDRAM: Write B

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

61. Write Data to DDRAM: Write I

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

62. Write Data to DDRAM: Write D

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

63. Clear Display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## FRAME FREQUENCY

### 1) 1/17 Duty Cycle
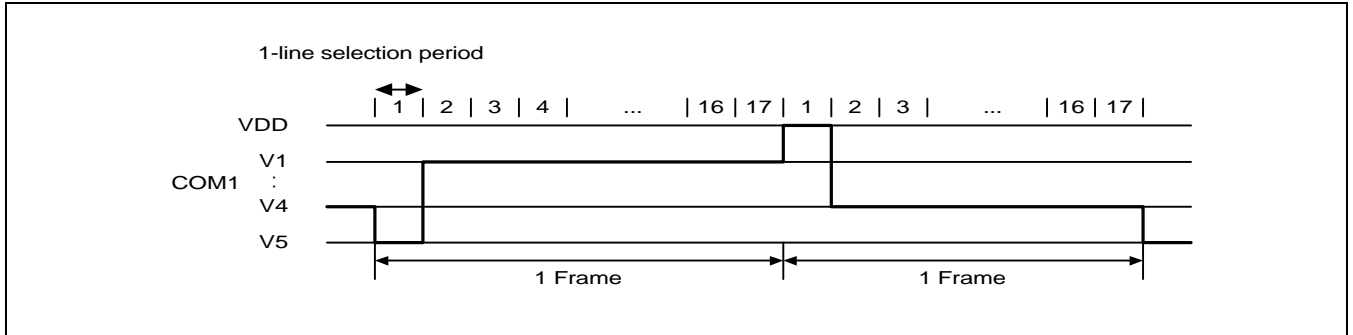


| Item | Normal Display Mode (LP = 0) | |
|---|---|---|
| | 5-dot font width | 6-dot font width |
| 1-line selection period | 200 clocks | 240 clocks |
| Frame frequency | 79.4Hz | 66.2Hz |

| Item | Low Power Mode (LP = 1) | |
|---|---|---|
| | 5-dot font width | 6-dot font width |
| 1-line selection period | 60 clocks | 72 clocks |
| Frame frequency | 66.2Hz | 55.1Hz |

* $f_{osc}$ = 270kHz (1 clock = 3.7$\mu$s)

## 2) 1/33 Duty Cycle
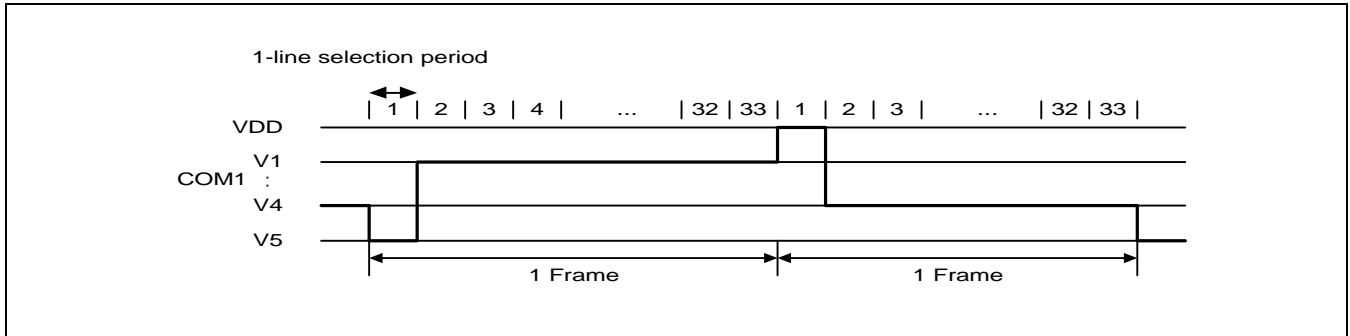


| Item | Normal Display Mode (LP = 0) | |
|---|---|---|
| | 5-dot font width | 6-dot font width |
| 1-line selection period | 100 clocks | 120 clocks |
| Frame frequency | 81.8Hz | 68.2Hz |

| Item | Normal Display Mode (LP = 1) | |
|---|---|---|
| | 5-dot font width | 6-dot font width |
| 1-line selection period | 60 clocks | 72 clocks |
| Frame frequency | 68.2Hz | 56.8Hz |

¡ Øfosc = 270kHz (1 clock = 3.7µs)

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# POWER SUPPLY FOR DRIVING LCD PANEL

## 1) When an external power supply is used
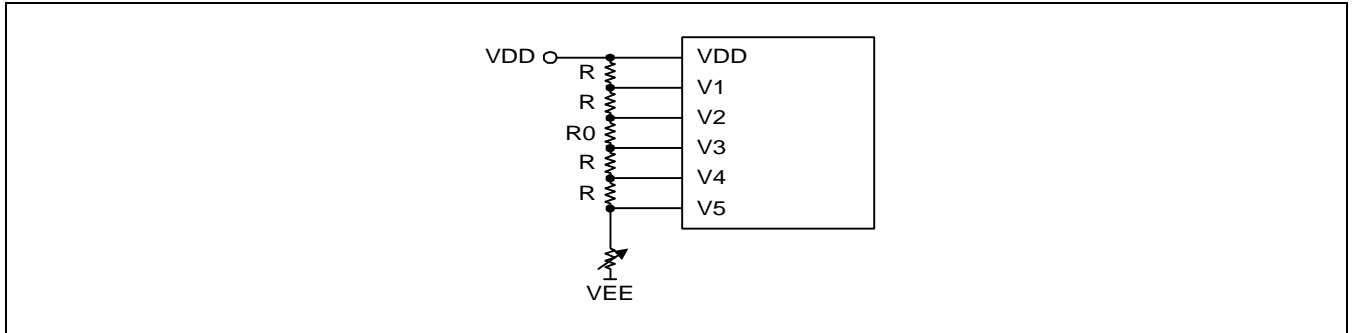


## 2) When an internal booster is used
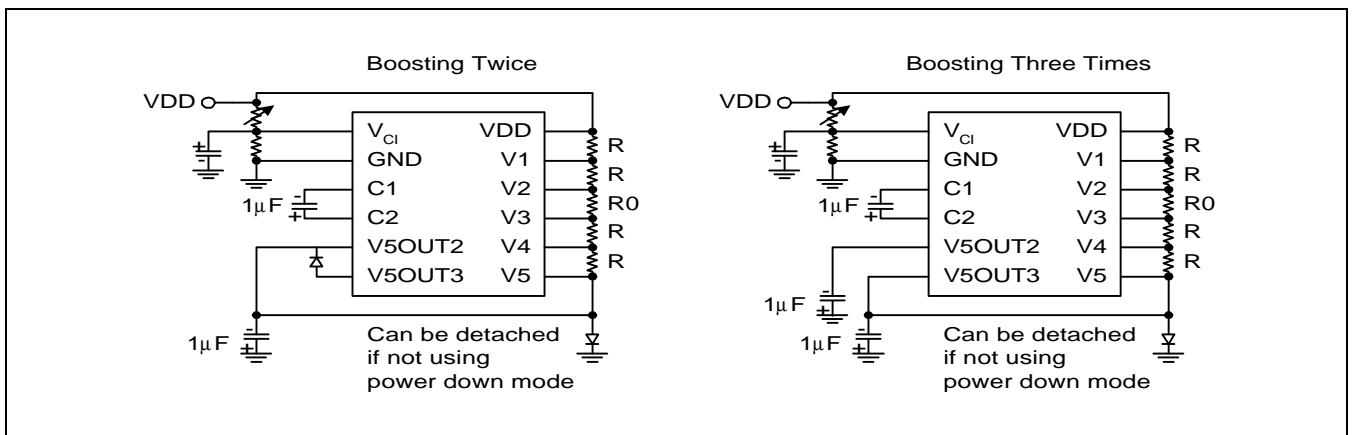


**NOTES:**

1.   Boosted  output voltage should not exceed the maximum value (13 V) of the LCD driving voltage. Especially, a voltage
of        over 4.3V should not be input to the reference voltage(Vci) when boosting three  times.
2.   A voltage of over 5.5V should not be input to  the reference voltage (Vci) when boosting twice.
3.   The value of resistance, according to the number of lines, duty ratio and the bias, is shown below. (Refer to Table 13)

**Table 13. Duty Ratio and Power Supply for LCD Driving**

| Item | | Data | |
|---|---|---|---|
| Number of lines | | 1 | 2 or 4 |
| Duty ratio | | 1/17 | 1/33 |
| Bias | | 1/5 | 1/6.7 |
| Divided resistance | R | R | R |
| | R0 | R | 2.7R |

## MAXIMUM ABSOLUTE RATE

| Characteristic | Symbol | Value | UNIT |
|---|---|---|---|
| Power Supply Voltage (1) | $V_{DD}$ | -0.3 to +7.0 | V |
| Power Supply Voltage (2) | $V_{LCD}$ | $V_{DD}$ -15.0 to $V_{DD}$ +0.3 | V |
| Input Voltage | $V_{IN}$ | -0.3 to $V_{DD}$ +0.3 | V |
| Operating Temperature | $T_{OPR}$ | -30 to +80 | °C |
| Storage Temperature | $T_{STG}$ | -55 to +125 | °C |

¡ Ø Voltage greater than above may damage to the circuit ($V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$)

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## ELECTRICAL CHARACTERISTICS

### DC Characteristics

$(V_{DD} = 2.7V$ to $5.5V$, $Ta = -30$ to $+85°C)$

| Characteristic | Symbol | Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | - | | 2.7 | - | 5.5 | V |
| Supply Current | $I_{DD}$ | Internal oscillation or external clock. ($V_{DD}$=3.0V, $f_{OSC}$ = 270kHz) | | - | 0.15 | 0.3 | mA |
| Input Voltage (1) | $V_{IH1}$ | - | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| (except OSC1) | $V_{IL1}$ | $V_{DD}$ = 2.7 to 3.0 | | -0.3 | - | $0.2V_{DD}$ | |
| | | $V_{DD}$ = 3.0 to 5.5 | | -0.3 | - | 0.6 | |
| Input Voltage (2) | $V_{IH2}$ | - | | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| (OSC1) | $V_{IL2}$ | - | | - | - | $0.2V_{DD}$ | |
| Output Voltage (1) | $V_{OH1}$ | $I_{OH}$ = -0.1mA | | $0.75V_{DD}$ | - | - | V |
| (DB0 to DB7) | $V_{OL1}$ | $I_{OL}$ = 0.1mA | | - | - | $0.2V_{DD}$ | |
| Output Voltage (2) | $V_{OH2}$ | $I_O$ = -40μA | | $0.8V_{DD}$ | - | - | V |
| (expect DB0 to DB7) | $V_{OL2}$ | $I_O$ = 40μA | | - | - | $0.2V_{DD}$ | |
| Voltage Drop | $Vd_{COM}$ | $I_O$ = ± 0.1mA | | - | - | 1 | V |
| | $vd_{SEG}$ | | | - | - | 1 | |
| Input Leakage Current | $I_{IL}$ | $V_{IN}$ = 0V to $V_{DD}$ | | -1 | - | 1 | μA |
| Low Input Current | $I_{IN}$ | $V_{IN}$ = 0V, $V_{DD}$ = 3V (pull up) | | -10 | -50 | -120 | |
| Internal Clock (external $R_f$) | $f_{OSC}$ | Rf = 91kΩ ± 2% ($V_{DD}$ = 5V) | | 190 | 270 | 350 | kHz |
| | $f_{EC}$ | | | 125 | 270 | 410 | kHz |
| External Clock | Duty | - | | 45 | 50 | 55 | % |
| | $t_R$, $t_F$ | | | - | - | 0.2 | μs |
| Voltage Converter Out2 (Vci = 4.5V) | $V_{OUT2}$ | Ta = 25°C, C = 1μF, $I_{OUT}$ = 0.25mA, | | -3.0 | -4.2 | - | V |
| Voltage Converter Out3 (Vci = 2.7V) | $V_{OUT3}$ | $f_{OSC}$ = 270kHz | | -4.3 | -5.1 | - | |
| Voltage Converter Input | Vci | - | | 2.5 | - | 4.5 | |
| LCD Driving Voltage | $V_{LCD}$ | $V_{DD}$-V5 | 1/5 bias | 3.0 | - | 13.0 | V |
| | | | 1/6.7 bias | 3.0 | - | 13.0 | |

## AC Characteristics

$(V_{DD} = 4.5 \text{ to } 5.5V, Ta = -30 \text{ to } +85°C)$

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| (1) Write Mode ( refer to Figure 21) | E Cycle Time | $t_C$ | 500 | - | - | ns |
| | E Rise / Fall Time | $t_R, t_F$ | - | - | 20 | |
| | E Pulse Width (High, Low) | $t_W$ | 230 | - | - | |
| | R/W and RS Setup Time | $t_{SU1}$ | 40 | - | - | |
| | R/W and RS Hold Time | $t_{H1}$ | 10 | - | - | |
| | Data Setup Time | $t_{SU2}$ | 60 | - | - | |
| | Data Hold Time | $t_{H2}$ | 10 | - | - | |
| (2) Read Mode (refer to Figure 22) | E Cycle Time | $t_C$ | 500 | - | - | ns |
| | E Rise / Fall Time | $t_R, t_F$ | - | - | 20 | |
| | E Pulse Width (High, Low) | $t_W$ | 230 | - | - | |
| | R/W and RS Setup Time | $t_{SU}$ | 40 | - | - | |
| | R/W and RS Hold Time | $t_H$ | 10 | - | - | |
| | Data Output Delay Time | $t_D$ | - | - | 160 | |
| | Data Hold Time | $t_{DH}$ | 5 | - | - | |
| (3) Serial Interface Mode (refer to Figure 23) | Serial Clock Cycle Time | $t_C$ | 0.5 | - | 20 | μs |
| | Serial Clock Rise / Fall Time | $t_R, t_F$ | - | - | 50 | ns |
| | Serial Clock Width (High, Low) | $t_W$ | 200 | - | - | |
| | Chip Select Setup Time | $t_{SU1}$ | 60 | - | - | |
| | Chip Select Hold Time | $tH1$ | 20 | - | - | |
| | Serial Input Data Setup Time | $t_{SU2}$ | 100 | - | - | |
| | Serial Input Data Hold Time | $t_{H2}$ | 100 | - | - | |
| | Serial Output Data Delay Time | $t_D$ | - | - | 160 | |
| | Serial Output Data Hold Time | $t_{DH}$ | 5 | - | - | |

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## AC Characteristics (Continued)

$(V_{DD} = 2.7$ to $4.5V$, $Ta = -30$ to $+85°C)$

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|------|------|--------|-----|-----|-----|------|
| (4) Write Mode ( refer to Figure 21) | E Cycle Time | $t_C$ | 1000 | - | - | ns |
| | E Rise / Fall Time | $t_R, t_F$ | - | - | 25 | |
| | E Pulse Width (High, Low) | $t_W$ | 450 | - | - | |
| | R/W and RS Setup Time | $t_{SU1}$ | 60 | - | - | |
| | R/W and RS Hold Time | $t_{H1}$ | 20 | - | - | |
| | Data Setup Time | $t_{SU2}$ | 195 | - | - | |
| | Data Hold Time | $t_{H2}$ | 10 | - | - | |
| (5) Read Mode (refer to Figure 22) | E Cycle Time | $t_C$ | 1000 | - | - | ns |
| | E Rise / Fall Time | $t_R, t_F$ | - | - | 25 | |
| | E Pulse Width (High, Low) | $t_W$ | 450 | - | - | |
| | R/W and RS Setup Time | $t_{SU}$ | 60 | - | - | |
| | R/W and RS Hold Time | $t_H$ | 20 | - | - | |
| | Data Output Delay Time | $t_D$ | - | - | 360 | |
| | Data Hold Time | $t_{DH}$ | 5 | - | - | |
| (6) Serial Interface Mode (refer to Figure 23) | Serial Clock Cycle Time | $t_C$ | 1 | - | 20 | µs |
| | Serial Clock Rise / Fall Time | $t_R, t_F$ | - | - | 50 | ns |
| | Serial Clock Width (High, Low) | $t_W$ | 400 | - | - | |
| | Chip Select Setup Time | $t_{SU1}$ | 60 | - | - | |
| | Chip Select Hold Time | $t_{H1}$ | 20 | - | - | |
| | Serial Input Data Setup Time | $t_{SU2}$ | 200 | - | - | |
| | Serial Input Data Hold Time | $t_{H2}$ | 200 | - | - | |
| | Serial Output Data Delay Time | $t_D$ | - | - | 360 | |
| | Serial Output Data Hold Time | $t_{DH}$ | 5 | - | - | |

## AC Characteristics (Continued)

$(V_{DD} = 2.7$ to $5.5V$, Ta = -30 to + 85°C)

| Mode | Item | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| (7) Interface Mode with Extension Driver (refer to Figure 24) | Clock Pulse Width (High, Low) | $t_W$ | 800 | - | - | ns |
| | Clock Rise / Fall Time | $t_R, t_F$ | - | - | 100 | |
| | Clock Setup Time | $t_{SU1}$ | 500 | - | - | |
| | Data Setup Time | $t_{SU2}$ | 300 | - | - | |
| | Data Hold Time | $t_{DH}$ | 300 | - | - | |
| | M Delay Time | $t_{DM}$ | -1000 | - | 1000 | |
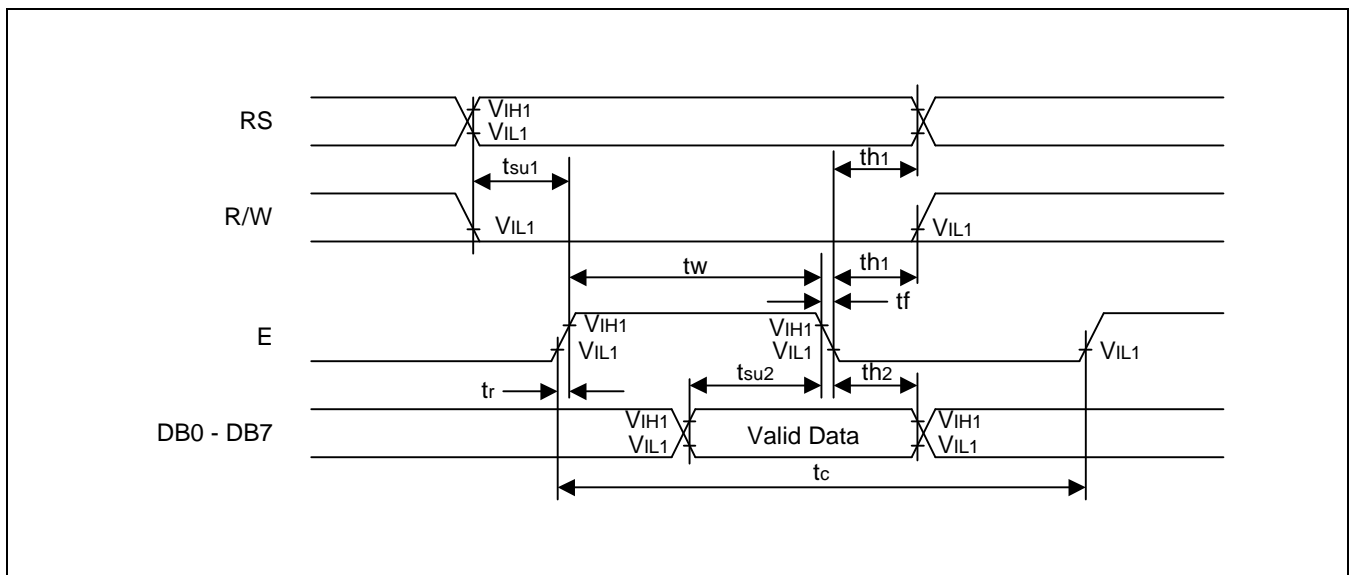


**Figure 21. Write Mode**

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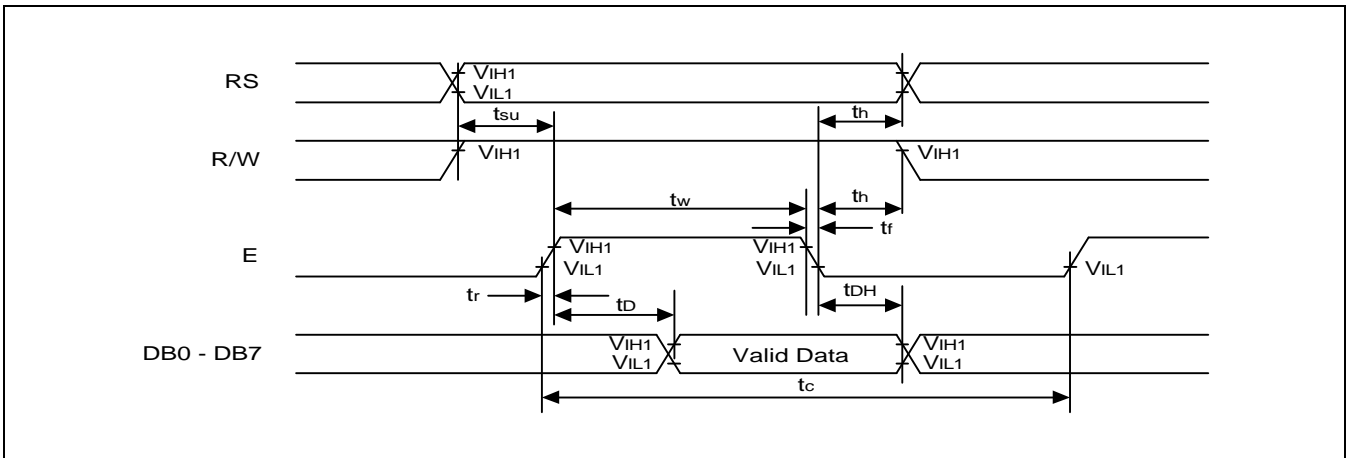
**Figure 22. Read Mode**
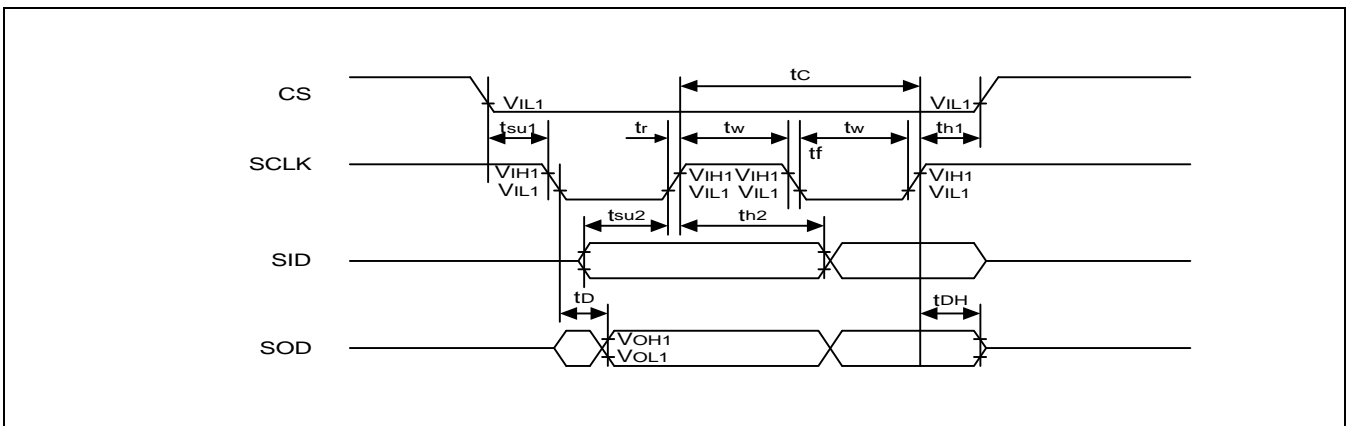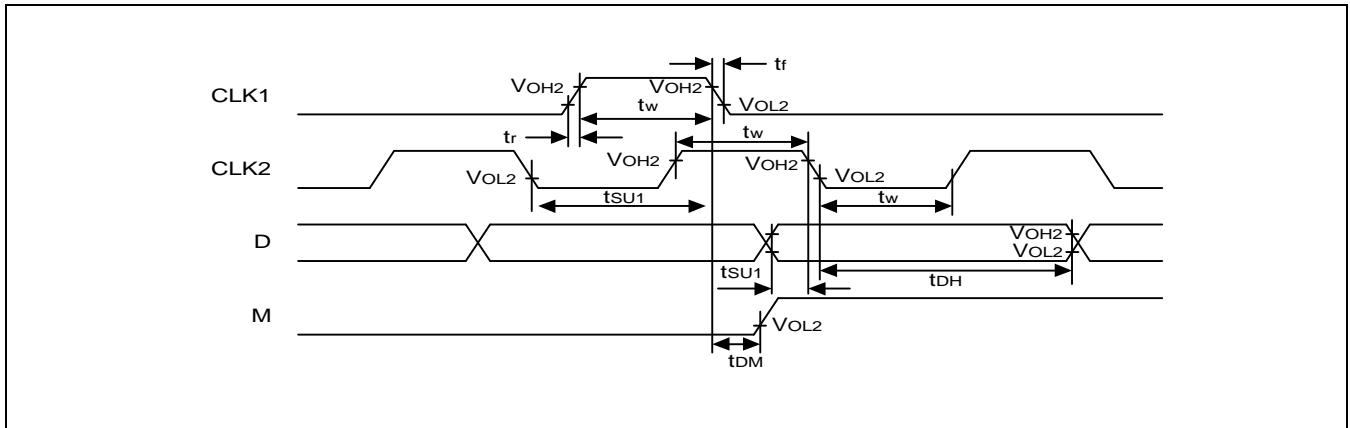


**Figure 23. Serial Interface Mode**

**Figure 24. Interface Mode with Extension Driver**

**RESET TIMING**

$(V_{DD} = 2.7$ to $5.5V$, $Ta = -30$ to $+85°C)$

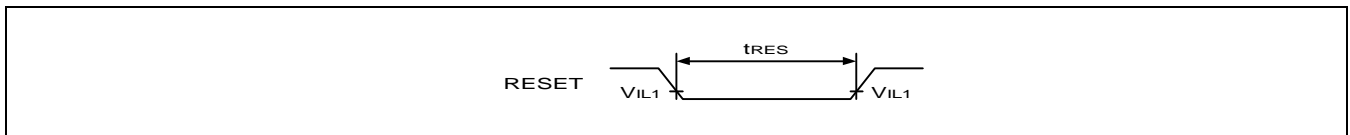| Item | Symbol | Min | Typ | Max | Unit |
|------|--------|-----|-----|-----|------|
| Reset low level width (refer to Figure 25) | $t_{RES}$ | 10 | - | - | ms |



**Figure 25. Reset Timing Diagram**

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