S6B0719

160 SEG / 105 COM SEG DRIVER & CONTROLLER FOR STN LCD

Jan. 2000.

Ver. 0.4

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S6B0719 Specification Revision History		
Version	**Content**	**Date**
0.0	- Original	Feb.1999
0.1	- Append pad center coordinate (refer to table 2) - Append display data RAM map (refer to figure 8)	Mar.1999
0.2	- Modify display data RAM map (refer to figure 8) - Append reference circuit examples (refer to page 22)	May.1999
0.3	- Change the low power consumption V0 = 13V -> 15V (refer to page 1) - Modify page address circuit description ; DB3, DB2 and DB1 are "H", but DB1 is "L" -> DB3, DB2 and DB0 are "H", but DB1 is "L" (refer to page 20) - Modify set partial display duty ratio (refer to page 27) - Add partial duty changing "waiting for discharging the LCD power levels (refer to figure 34)	Jun.1999
0.4	- Change the condition of power consumption : (VDD = 3V, x6 boosting, V0 = 15V) → (VDD = 3V, x5 boosting, V0 = 13V) (refer to page 1) - Change the absolute maximum ratings of V0 and VOUT : 20V → 17V (refer to page 50) - Change the operating voltage of V0 and VOUT : 17V → 15V (refer to page 1 and 51) - Change the operating voltage of VDD : (2.4 to 5.5V) → (2.4 to 3.6V) (refer to page 1 and 51) - Modify Figure20 (refer to page 24)	Jan.2000

CONTENTS

INTRODUCTION

The S6B0719 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 105 common and 160 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 105 x 160 bits. It provides a highly flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no external-operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 105 common outputs / 160 segment outputs

Applicable Duty-ratios

Programmable duty ratio	Applicable LCD bias	Maximum display area
1/9 to 1/105	1/4 to 1/11	105 × 160

– Various partial display
– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 105 x 160 = 16,800 bits
– Bit data "1": a dot of display is illuminated
– Bit data "0": a dot of display is not illuminated

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface (only write operation) available

On-chip Low Power Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x3, x4, x5 or x6)
– Voltage regulator (temperature coefficient: -0.05%/°C or external input)
– On-chip electronic contrast control function (64 steps)
– Voltage follower (LCD bias: 1/4 to 1/11)

Operating Voltage Range

– Supply voltage (V_{DD}): 2.4 to 3.6 V
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 15.0 V

Low Power Consumption

– TBD μA Typ. (V_{DD} = 3V, x6 boosting, V0 = 13V, Internal power supply ON and display OFF)
– TBD μA Max. (during power save [standby] mode)

Package Type

– Gold bumped chip or TCP

BLOCK DIAGRAM

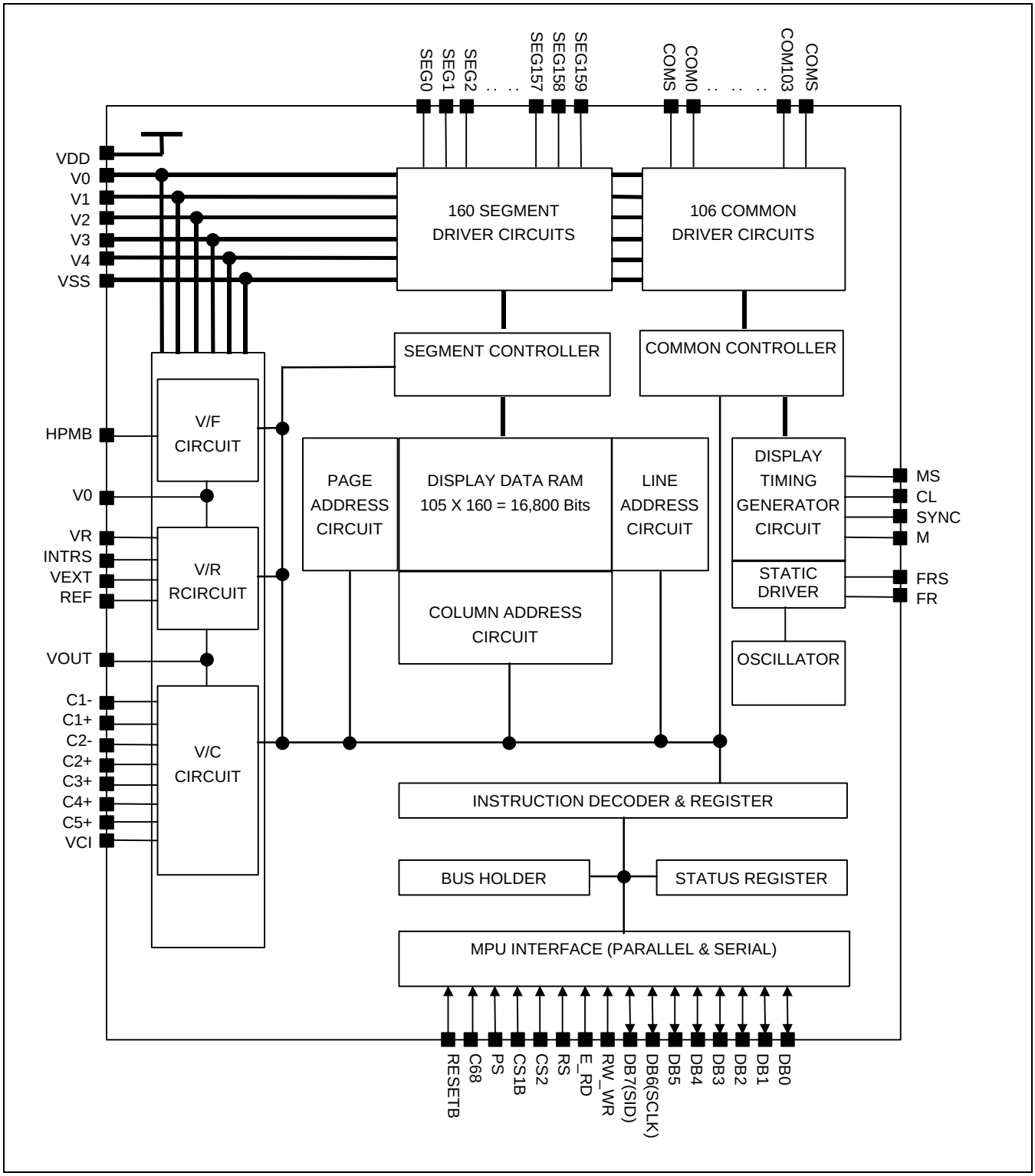


Figure 1. Block Diagram

PAD CONFIGURATION

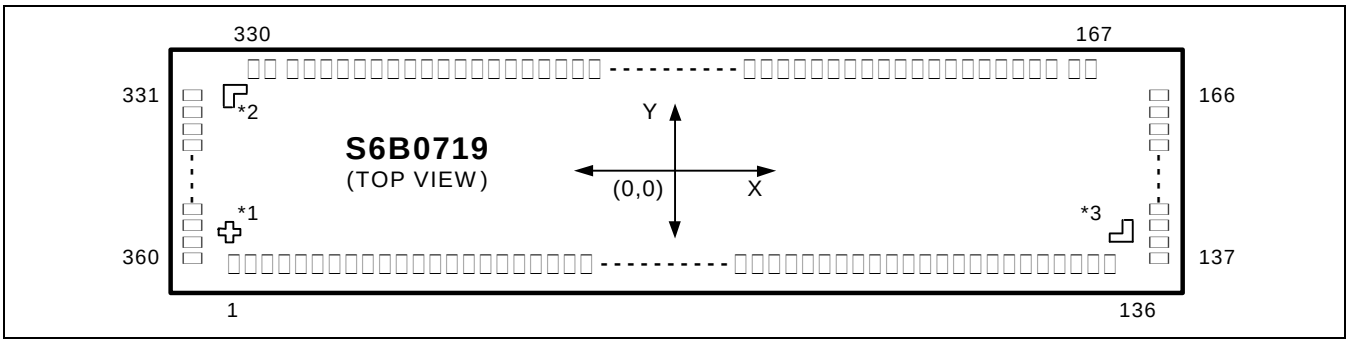
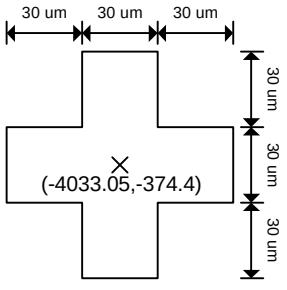


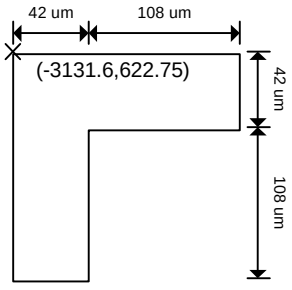
Figure 2. S6B0719 Chip Configuration

Table 1. S6B0719 Pad Dimensions

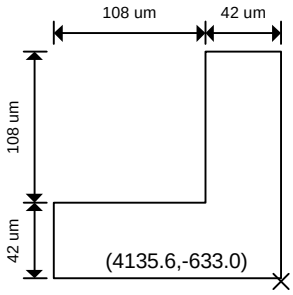
Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	9370	2220	mm
Pad pitch	29 to 108	70 (Min.)		
	1 to 28, 109 to 136, 137 to 360	54 (Min.)		
Bumped `pad size	30 to 107	60	78	
	138 to 165, 332 to 359	78	44	
	3 to 27, 110 to 134 169 to 328	44	78	
	1, 2, 28, 29, 108, 109, 135, 136, 167, 168, 329 and 330	70	78	
	137, 166, 331 and 360	78	70	
Bumped pad height	1 to 360	14 (Typ.)		



*1 : COG Align Key



*2 : ILB Align Key 1



*3 : ILB Align Key 2

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY	-4453	-985	51	RW_WR	-1225	-985	101	VR	2275	-985	151	COM13	4560	-27
2	DUMMY	-4373	-985	52	E_RD	-1155	-985	102	VSS	2345	-985	152	COM12	4560	27
3	COM80	-4293	-985	53	VDD	-1085	-985	103	REF	2415	-985	153	COM11	4560	81
4	COM81	-4239	-985	54	DB0	-1015	-985	104	VEXT	2485	-985	154	COM10	4560	135
5	COM82	-4185	-985	55	DB1	-945	-985	105	VDD	2555	-985	155	COM9	4560	189
6	COM83	-4131	-985	56	DB2	-875	-985	106	INTRS	2625	-985	156	COM8	4560	243
7	COM84	-4077	-985	57	DB3	-805	-985	107	VSS	2695	-985	157	COM7	4560	297
8	COM85	-4023	-985	58	DB4	-735	-985	108	DUMMY	2775	-985	158	COM6	4560	351
9	COM86	-3969	-985	59	DB5	-665	-985	109	DUMMY	2917	-985	159	COM5	4560	405
10	COM87	-3915	-985	60	DB6	-595	-985	110	COM51	2997	-985	160	COM4	4560	459
11	COM88	-3861	-985	61	DB7	-525	-985	111	COM50	3051	-985	161	COM3	4560	513
12	COM89	-3807	-985	62	VDD	-455	-985	112	COM49	3105	-985	162	COM2	4560	567
13	COM90	-3753	-985	63	VDD	-385	-985	113	COM48	3159	-985	163	COM1	4560	621
14	COM91	-3699	-985	64	VDD	-315	-985	114	COM47	3213	-985	164	COM0	4560	675
15	COM92	-3645	-985	65	VDD	-245	-985	115	COM46	3267	-985	165	COMS	4560	729
16	COM93	-3591	-985	66	VCI	-175	-985	116	COM45	3321	-985	166	DUMMY	4560	809
17	COM94	-3537	-985	67	VCI	-105	-985	117	COM44	3375	-985	167	DUMMY	4453	985
18	COM95	-3483	-985	68	VSS	-35	-985	118	COM43	3429	-985	168	DUMMY	4373	985
19	COM96	-3429	-985	69	VSS	35	-985	119	COM42	3483	-985	169	SEG0	4293	985
20	COM97	-3375	-985	70	VSS	105	-985	120	COM41	3537	-985	170	SEG1	4239	985
21	COM98	-3321	-985	71	VSS	175	-985	121	COM40	3591	-985	171	SEG2	4185	985
22	COM99	-3267	-985	72	VOUT	245	-985	122	COM39	3645	-985	172	SEG3	4131	985
23	COM100	-3213	-985	73	VOUT	315	-985	123	COM38	3699	-985	173	SEG4	4077	985
24	COM101	-3159	-985	74	C5+	385	-985	124	COM37	3753	-985	174	SEG5	4023	985
25	COM102	-3105	-985	75	C5+	455	-985	125	COM36	3807	-985	175	SEG6	3969	985
26	COM103	-3051	-985	76	C3+	525	-985	126	COM35	3861	-985	176	SEG7	3915	985
27	COMS	-2997	-985	77	C3+	595	-985	127	COM34	3915	-985	177	SEG8	3861	985
28	DUMMY	-2917	-985	78	C1-	665	-985	128	COM33	3969	-985	178	SEG9	3807	985
29	DUMMY	-2775	-985	79	C1-	735	-985	129	COM32	4023	-985	179	SEG10	3753	985
30	FRS	-2695	-985	80	C1+	805	-985	130	COM31	4077	-985	180	SEG11	3699	985
31	FR	-2625	-985	81	C1+	875	-985	131	COM30	4131	-985	181	SEG12	3645	985
32	TEST1	-2555	-985	82	C2+	945	-985	132	COM29	4185	-985	182	SEG13	3591	985
33	TEST2	-2485	-985	83	C2+	1015	-985	133	COM28	4239	-985	183	SEG14	3537	985
34	TEST3	-2415	-985	84	C2-	1085	-985	134	COM27	4293	-985	184	SEG15	3483	985
35	CL	-2345	-985	85	C2-	1155	-985	135	DUMMY	4373	-985	185	SEG16	3429	985
36	M	-2275	-985	86	C4+	1225	-985	136	DUMMY	4453	-985	186	SEG17	3375	985
37	SYNC	-2205	-985	87	C4+	1295	-985	137	DUMMY	4560	-809	187	SEG18	3321	985
38	VSS	-2135	-985	88	VSS	1365	-985	138	COM26	4560	-729	188	SEG19	3267	985
39	HPMB	-2065	-985	89	VSS	1435	-985	139	COM25	4560	-675	189	SEG20	3213	985
40	MS	-1995	-985	90	V4	1505	-985	140	COM24	4560	-621	190	SEG21	3159	985
41	VDD	-1925	-985	91	V4	1575	-985	141	COM23	4560	-567	191	SEG22	3105	985
42	PS	-1855	-985	92	V3	1645	-985	142	COM22	4560	-513	192	SEG23	3051	985
43	C68	-1785	-985	93	V3	1715	-985	143	COM21	4560	-459	193	SEG24	2997	985
44	VSS	-1715	-985	94	V2	1785	-985	144	COM20	4560	-405	194	SEG25	2943	985
45	CS1B	-1645	-985	95	V2	1855	-985	145	COM19	4560	-351	195	SEG26	2889	985
46	CS2	-1575	-985	96	V1	1925	-985	146	COM18	4560	-297	196	SEG27	2835	985
47	VDD	-1505	-985	97	V1	1995	-985	147	COM17	4560	-243	197	SEG28	2781	985
48	RESETB	-1435	-985	98	V0	2065	-985	148	COM16	4560	-189	198	SEG29	2727	985
49	RS	-1365	-985	99	V0	2135	-985	149	COM15	4560	-135	199	SEG30	2673	985
50	VSS	-1295	-985	100	VR	2205	-985	150	COM14	4560	-81	200	SEG31	2619	985

Table 2 (Continued)

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
201	SEG32	2565	985	251	SEG82	-135	985	301	SEG132	-2835	985	351	COM71	-4560	-297
202	SEG33	2511	985	252	SEG83	-189	985	302	SEG133	-2889	985	352	COM72	-4560	-351
203	SEG34	2457	985	253	SEG84	-243	985	303	SEG134	-2943	985	353	COM73	-4560	-405
204	SEG35	2403	985	254	SEG85	-297	985	304	SEG135	-2997	985	354	COM74	-4560	-459
205	SEG36	2349	985	255	SEG86	-351	985	305	SEG136	-3051	985	355	COM75	-4560	-513
206	SEG37	2295	985	256	SEG87	-405	985	306	SEG137	-3105	985	356	COM76	-4560	-567
207	SEG38	2241	985	257	SEG88	-459	985	307	SEG138	-3159	985	357	COM77	-4560	-621
208	SEG39	2187	985	258	SEG89	-513	985	308	SEG139	-3213	985	358	COM78	-4560	-675
209	SEG40	2133	985	259	SEG90	-567	985	309	SEG140	-3267	985	359	COM79	-4560	-729
210	SEG41	2079	985	260	SEG91	-621	985	310	SEG141	-3321	985	360	DUMMY	-4560	-809
211	SEG42	2025	985	261	SEG92	-675	985	311	SEG142	-3375	985				
212	SEG43	1971	985	262	SEG93	-729	985	312	SEG143	-3429	985				
213	SEG44	1917	985	263	SEG94	-783	985	313	SEG144	-3483	985				
214	SEG45	1863	985	264	SEG95	-837	985	314	SEG145	-3537	985				
215	SEG46	1809	985	265	SEG96	-891	985	315	SEG146	-3591	985				
216	SEG47	1755	985	266	SEG97	-945	985	316	SEG147	-3645	985				
217	SEG48	1701	985	267	SEG98	-999	985	317	SEG148	-3699	985				
218	SEG49	1647	985	268	SEG99	-1053	985	318	SEG149	-3753	985				
219	SEG50	1593	985	269	SEG100	-1107	985	319	SEG150	-3807	985				
220	SEG51	1539	985	270	SEG101	-1161	985	320	SEG151	-3861	985				
221	SEG52	1485	985	271	SEG102	-1215	985	321	SEG152	-3915	985				
222	SEG53	1431	985	272	SEG103	-1269	985	322	SEG153	-3969	985				
223	SEG54	1377	985	273	SEG104	-1323	985	323	SEG154	-4023	985				
224	SEG55	1323	985	274	SEG105	-1377	985	324	SEG155	-4077	985				
225	SEG56	1269	985	275	SEG106	-1431	985	325	SEG156	-4131	985				
226	SEG57	1215	985	276	SEG107	-1485	985	326	SEG157	-4185	985				
227	SEG58	1161	985	277	SEG108	-1539	985	327	SEG158	-4239	985				
228	SEG59	1107	985	278	SEG109	-1593	985	328	SEG159	-4293	985				
229	SEG60	1053	985	279	SEG110	-1647	985	329	DUMMY	-4373	985				
230	SEG61	999	985	280	SEG111	-1701	985	330	DUMMY	-4453	985				
231	SEG62	945	985	281	SEG112	-1755	985	331	DUMMY	-4560	809				
232	SEG63	891	985	282	SEG113	-1809	985	332	COM52	-4560	729				
233	SEG64	837	985	283	SEG114	-1863	985	333	COM53	-4560	675				
234	SEG65	783	985	284	SEG115	-1917	985	334	COM54	-4560	621				
235	SEG66	729	985	285	SEG116	-1971	985	335	COM55	-4560	567				
236	SEG67	675	985	286	SEG117	-2025	985	336	COM56	-4560	513				
237	SEG68	621	985	287	SEG118	-2079	985	337	COM57	-4560	459				
238	SEG69	567	985	288	SEG119	-2133	985	338	COM58	-4560	405				
239	SEG70	513	985	289	SEG120	-2187	985	339	COM59	-4560	351				
240	SEG71	459	985	290	SEG121	-2241	985	340	COM60	-4560	297				
241	SEG72	405	985	291	SEG122	-2295	985	341	COM61	-4560	243				
242	SEG73	351	985	292	SEG123	-2349	985	342	COM62	-4560	189				
243	SEG74	297	985	293	SEG124	-2403	985	343	COM63	-4560	135				
244	SEG75	243	985	294	SEG125	-2457	985	344	COM64	-4560	81				
245	SEG76	189	985	295	SEG126	-2511	985	345	COM65	-4560	27				
246	SEG77	135	985	296	SEG127	-2565	985	346	COM66	-4560	-27				
247	SEG78	81	985	297	SEG128	-2619	985	347	COM67	-4560	-81				
248	SEG79	27	985	298	SEG129	-2673	985	348	COM68	-4560	-135				
249	SEG80	-27	985	299	SEG130	-2727	985	349	COM69	-4560	-189				
250	SEG81	-81	985	300	SEG131	-2781	985	350	COM70	-4560	-243				

PIN DESCRIPTION

Table 3. Power Supply Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="5">Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td colspan="5">Power supply</td></tr>
<tr><td>Vss</td><td>Supply</td><td colspan="5">Ground</td></tr>
<tr><td rowspan="4">V0
V1
V2
V3
V4</td><td rowspan="4">I/O</td><td colspan="5">LCD drivers supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</td></tr>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1)/N x V0</td><td>(N-2)/N x V0</td><td>2/N x V0</td><td>1/N x V0</td></tr>
<tr><td colspan="5">NOTE : *N = 4 to 11</td></tr>
</table>

Table 4. LCD Driver Supply Pins

Name	I/O	Description
C1-, C2-	I/O	Capacitor negative connection pins for voltage converter
C1+, C2+ C3+, C4+ C5+	I/O	Capacitor positive connection pins for voltage converter
VOUT	I/O	Voltage converter input/output pin
VCI	I	Voltage converter input voltage pin Voltages should have the following relationship: VDD ≤ VCI ≤ V0
VR	I	V0 voltage adjustment pin It is valid only when on-chip resistors are not used. (INTRS = “L”)
REF	I	Selects the external VREF voltage via VEXT pin – REF = "L": using the external VREF – REF = "H": using the internal VREF
VEXT	I	Externally input reference voltage (VREF) for the internal voltage regulator. It is valid only when REF is “L”.

Table 5. System Control Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td rowspan="5">MS</td><td rowspan="5">I</td><td>Master / Slave operations select pin
– MS = "H": master operation
– MS = "L": slave operation
The following table depends on the MS status.</td></tr>
<tr><td>
<table>
<tr><td rowspan="2">MS</td><td colspan="2">Internal analog circuits</td><td colspan="3">Display timing signals</td></tr>
<tr><td>Oscillator</td><td>Power supply</td><td>CL</td><td>SYNC</td><td>M</td></tr>
<tr><td>H</td><td>Enabled</td><td>Enabled</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disabled</td><td>Disabled</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
</td></tr>
<tr><td></td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin
When the S6B0719 is used in master / slave mode (multi-chip), the CL pins must be connected each other.</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Display sync input / output pin
When the S6B0719 is used in master/slave mode (multi-chip), the SYNC pins must be connected each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC input / output pin
When the S6B0719 is used in master/slave mode (multi-chip), the M pins must be connected each other.</td></tr>
<tr><td>FR</td><td>O</td><td>Static driver common output pin
This pin is used together with the FRS pin.</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output pin
This pin is used together with the FR pin.</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistors select pin
This pin selects the resistors for adjusting V0 voltage level.
– INTRS = "H": use the internal resistors.
– INTRS = "L": use the external resistors. VR pin and external resistive divider control V0 voltage.</td></tr>
<tr><td>HPMB</td><td>I</td><td>Power control pin of the power supplies circuit for LCD driver
– HPMB = "L": high power mode
– HPMB = "H": normal mode
This pin is valid in master operation.</td></tr>
<tr><td>TEST1
to
TEST3</td><td>I</td><td>Test pins
Don't use these pins.</td></tr>
</table>

NOTE: **DUMMY – These pins should be opened (floated).**

Table 6. Microprocessor Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="6">Description</th></tr>
<tr><td>RESETB</td><td>I</td><td colspan="6">Reset input pin
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="5">PS</td><td rowspan="5">I</td><td colspan="6">Parallel / Serial data input select input</td></tr>
<tr><td>PS</td><td>Interface mode</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
<tr><td colspan="6">*NOTE: When PS is “L”, DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td>C68</td><td>I</td><td colspan="6">Microprocessor interface select input pin
– C68 = "H": 6800-series MPU interface
– C68 = "L": 8080-series MPU interface</td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td colspan="6">Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”.
When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td colspan="6">Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="4">RW_WR</td><td rowspan="4">I</td><td colspan="6">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>RW_WR</td><td colspan="2">Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td colspan="2">Read/Write control input pin
– RW = “H”: read
– RW = “L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td colspan="2">Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table>

Table 6. (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="5">E_RD</td><td rowspan="5">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU Type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID).
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

Table 7. LCD driver output pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG159</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM103</td><td rowspan="8">O</td><td colspan="3">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td>Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td>Vss</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td></tr>
<tr><td colspan="3"></td></tr>
<tr><td>COMS</td><td>O</td><td colspan="3">Common output for the icons
The output signals of two pins are same. When not used, these pins should be left open.</td></tr>
</table>

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0719 can interface with an MPU only when CS1B is “L” and CS2 is “H”. When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

The S6B0719 has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 8.

Table 8. Parallel / Serial Interface Mode.

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	*×	Serial-mode

*×: Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 9. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table 10.

Table 9. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register (instruction)

Serial Interface (PS = "L")

When the S6B0719 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

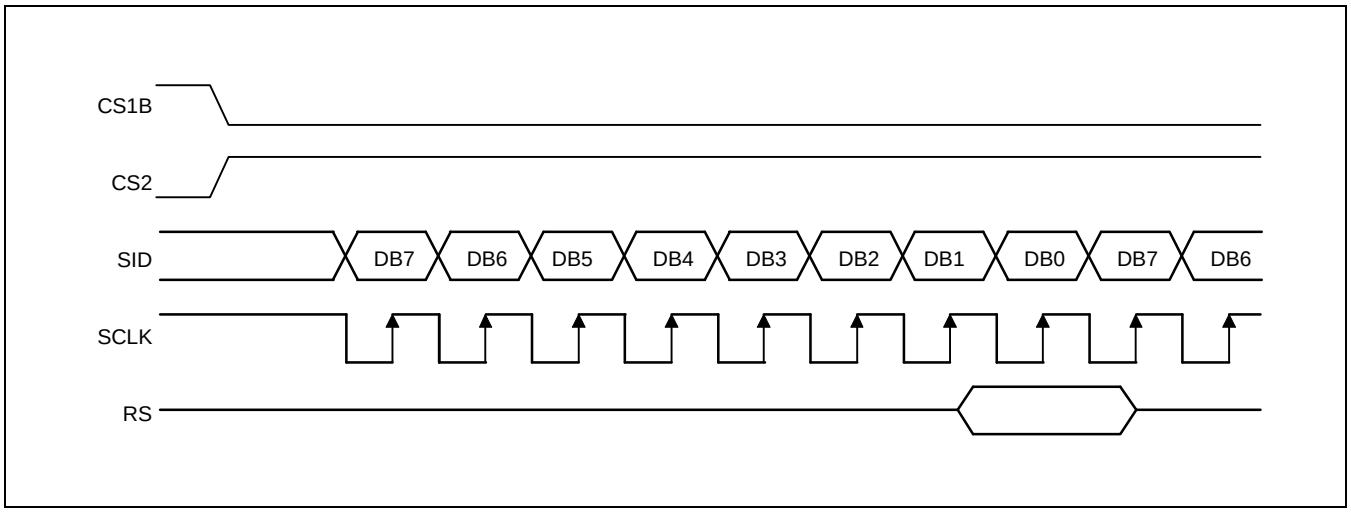


Figure 3. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the S6B0719 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0719 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

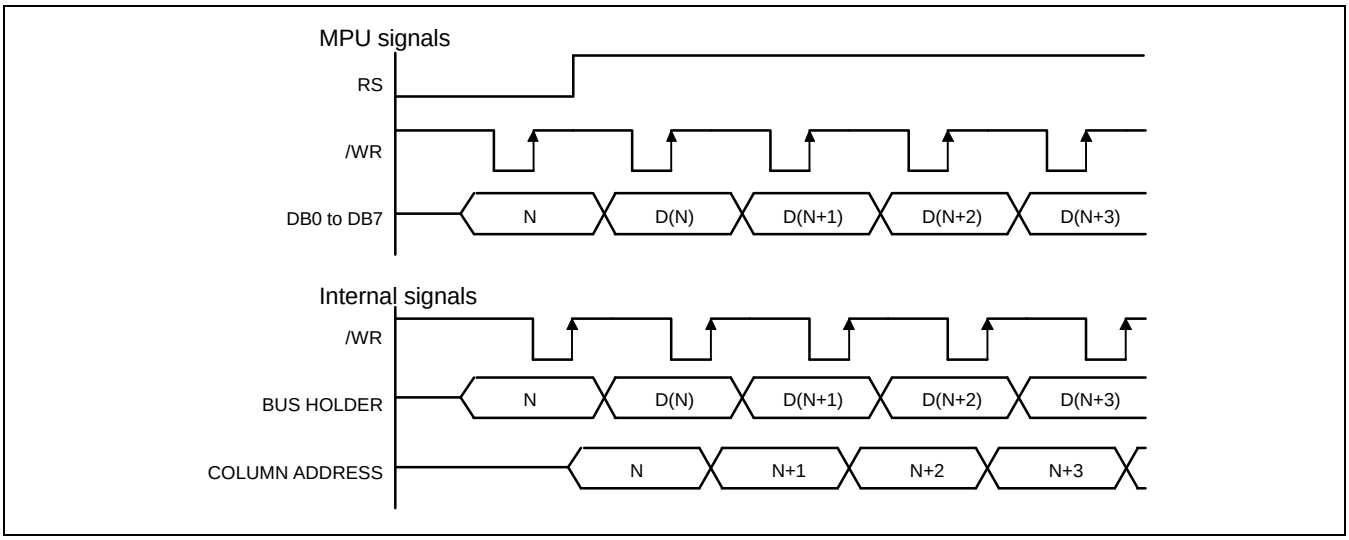


Figure 4. Write Timing

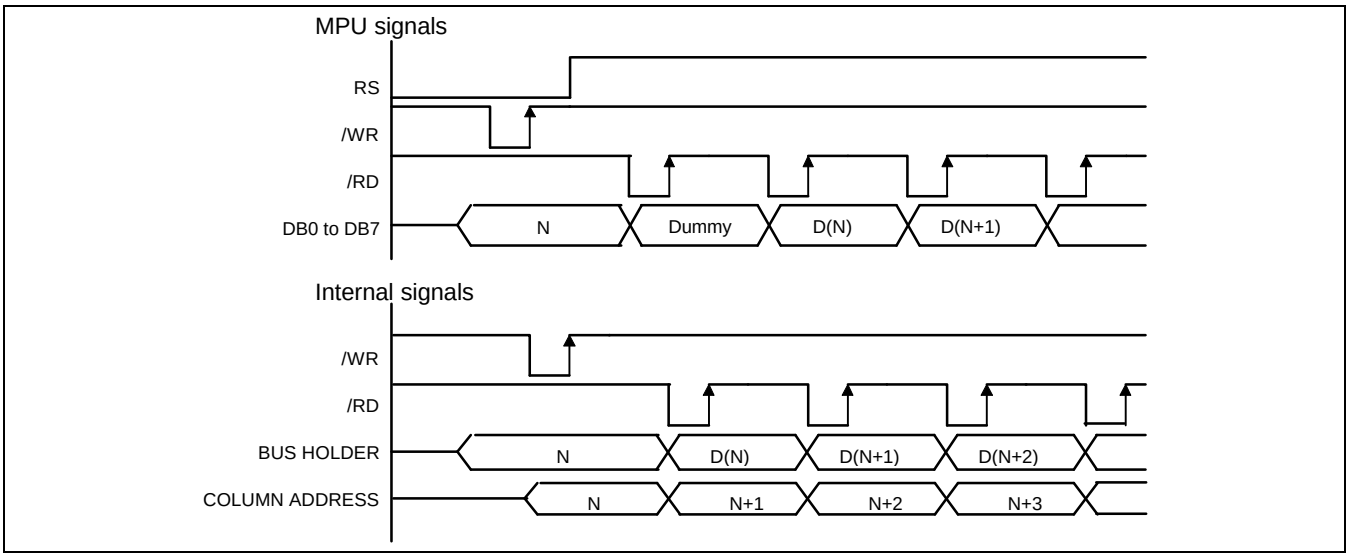


Figure 5. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 105-row by 160-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 105 rows are divided into 13 pages of 8 lines and the 13th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

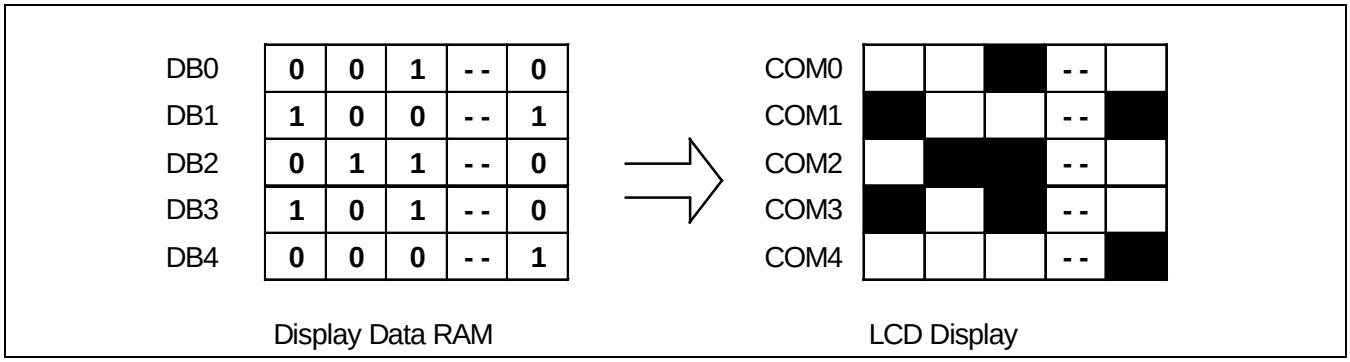


Figure 6. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a Page Address to Display Data RAM shown in figure 8. It incorporates 4-bit Page Address register changed by only the "Set Page" instruction. Page Address 13 (DB3, DB2 and DB0 are "H", but DB1 is "L") is a special RAM area for the icons and display data DB0 is only valid.

Line Address Circuit

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 7. It incorporates 7-bit line address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by CL signal and generates the Line Address for transferring the 160-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not incremented and locked if a non-existing address above 9FH. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

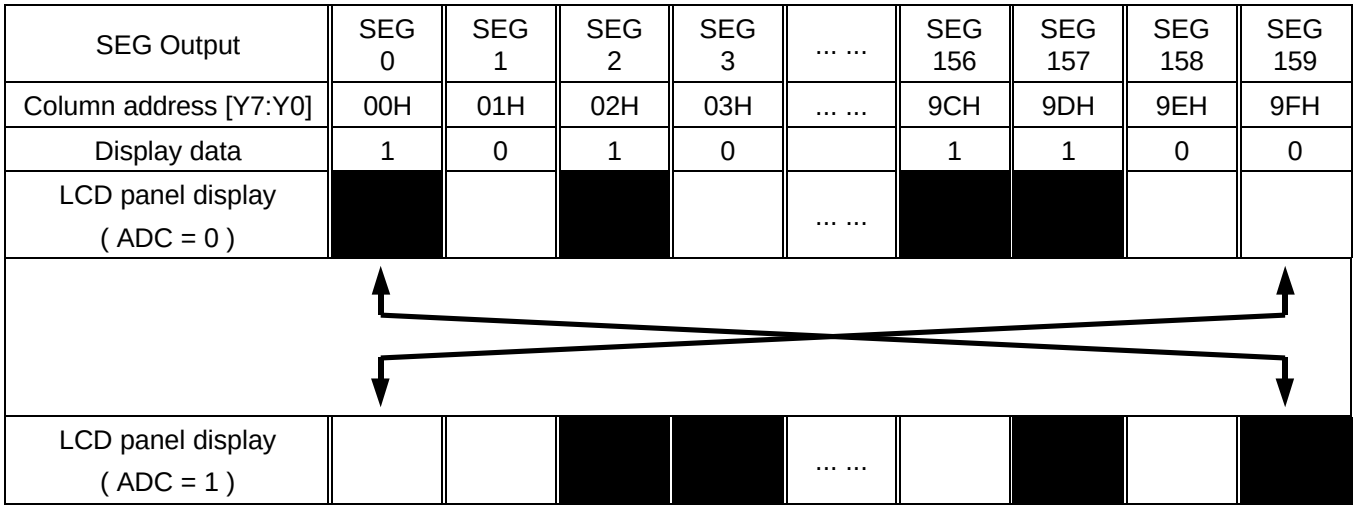


Figure 7. The Relationship between the Column Address and The Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

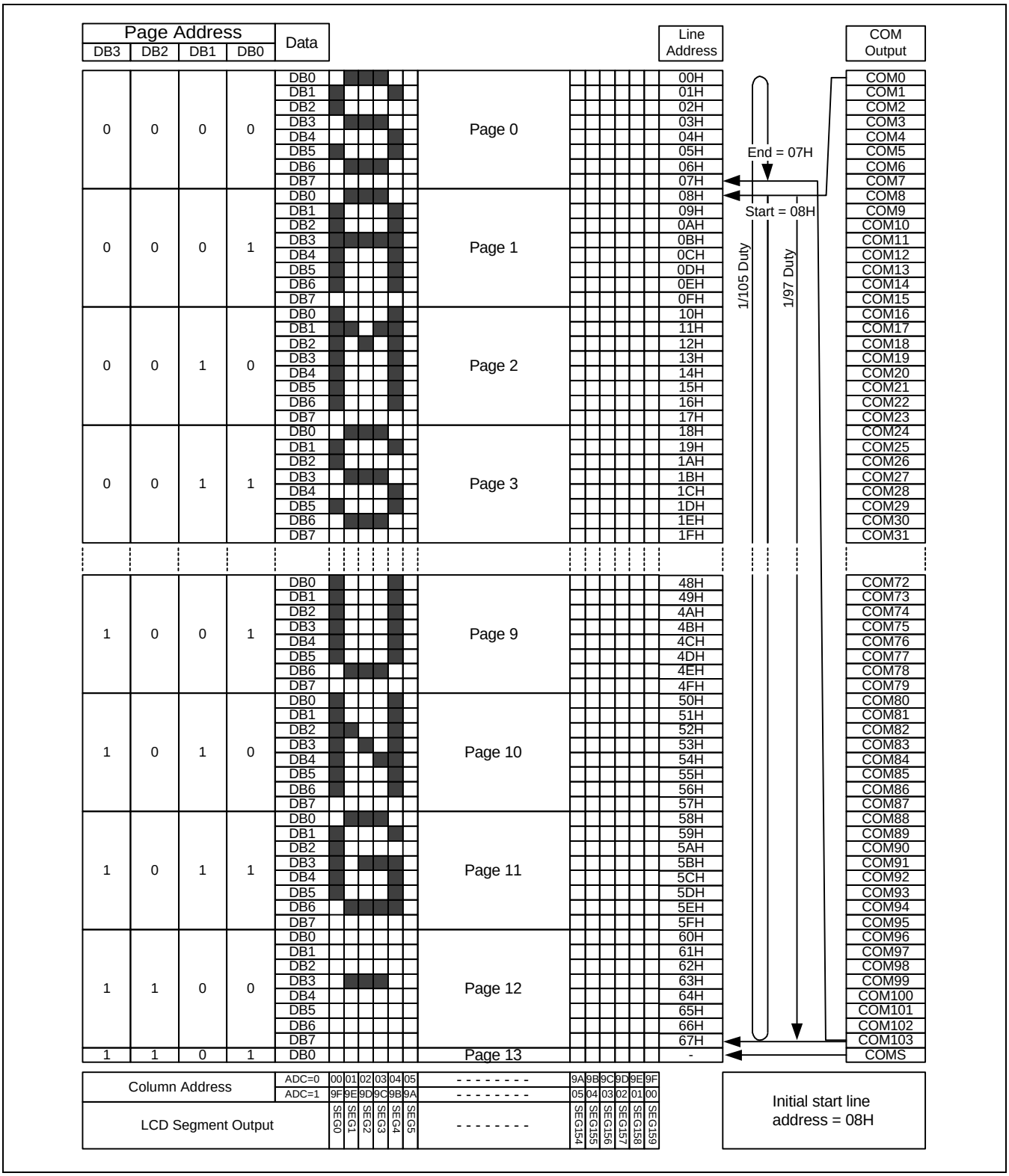


Figure 8. Display Data RAM Map

SAMSUNG ELECTRONICS

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the display data latch circuit in synchronization latches the 160-bit display data with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame or the line changes the phase of M by setting internal instruction. Driving waveform and internal timing signal are shown in figure 10.

In a multiple-chip configuration, the slave chip requires the CL, M and SYNC signals from the master. Table 11 shows the CL, SYNC, and M status.

Table 11. Master and Slave Timing Signal Status

Operation mode	Oscillator	CL	SYNC	M
Master	ON (internal clock used)	Output	Output	Output
Slave	OFF (external clock used)	Input	Input	Input

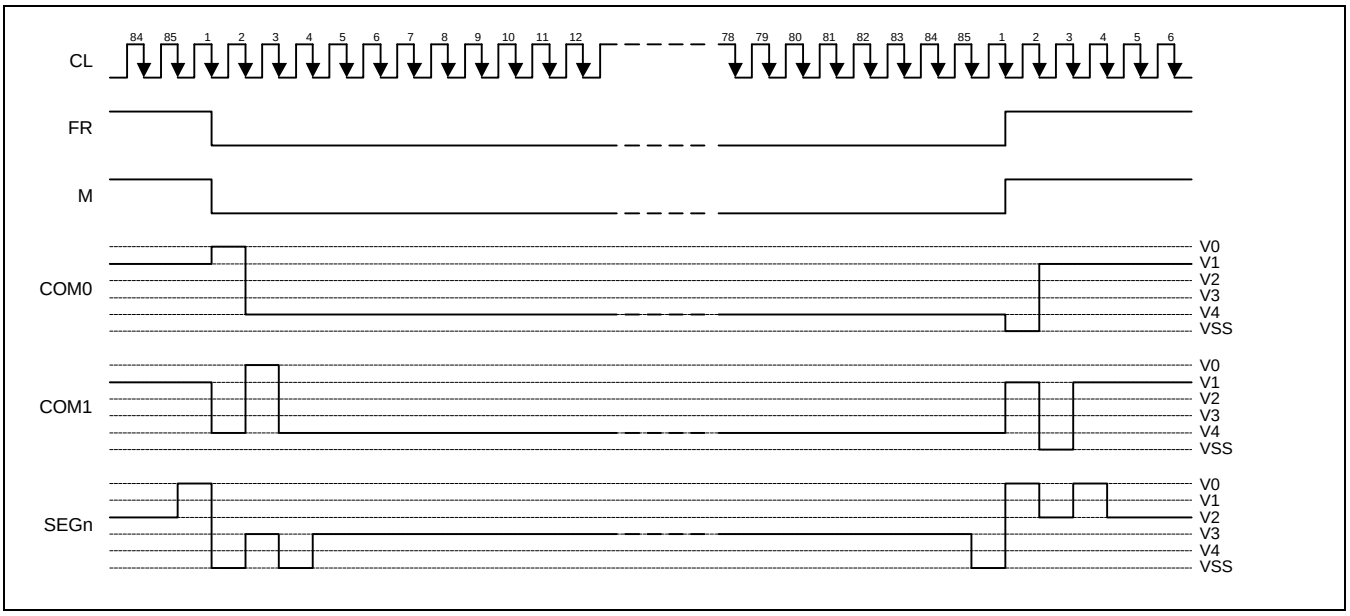


Figure 9. 2-frame AC Driving Waveform (Duty Ratio = 1/85)

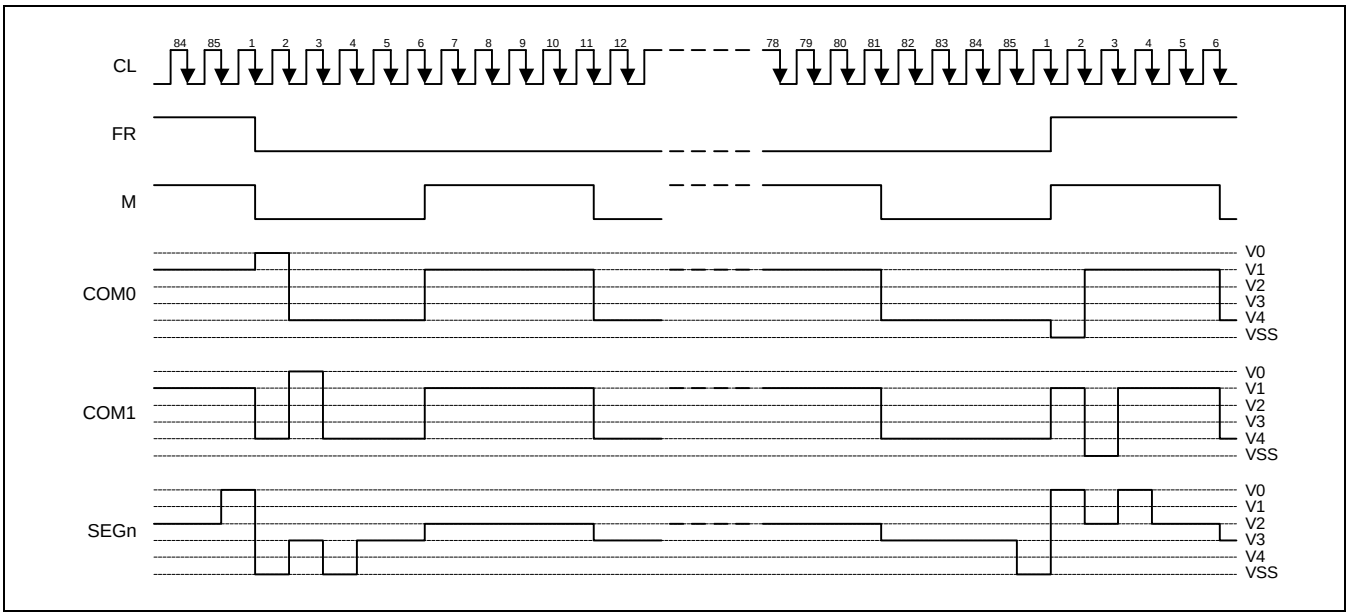


Figure 10. N-line Inversion Driving Waveform (N = 5, Duty Ratio = 1/85)

LCD DRIVER CIRCUIT

106-channel common driver and 160-channel segment driver configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

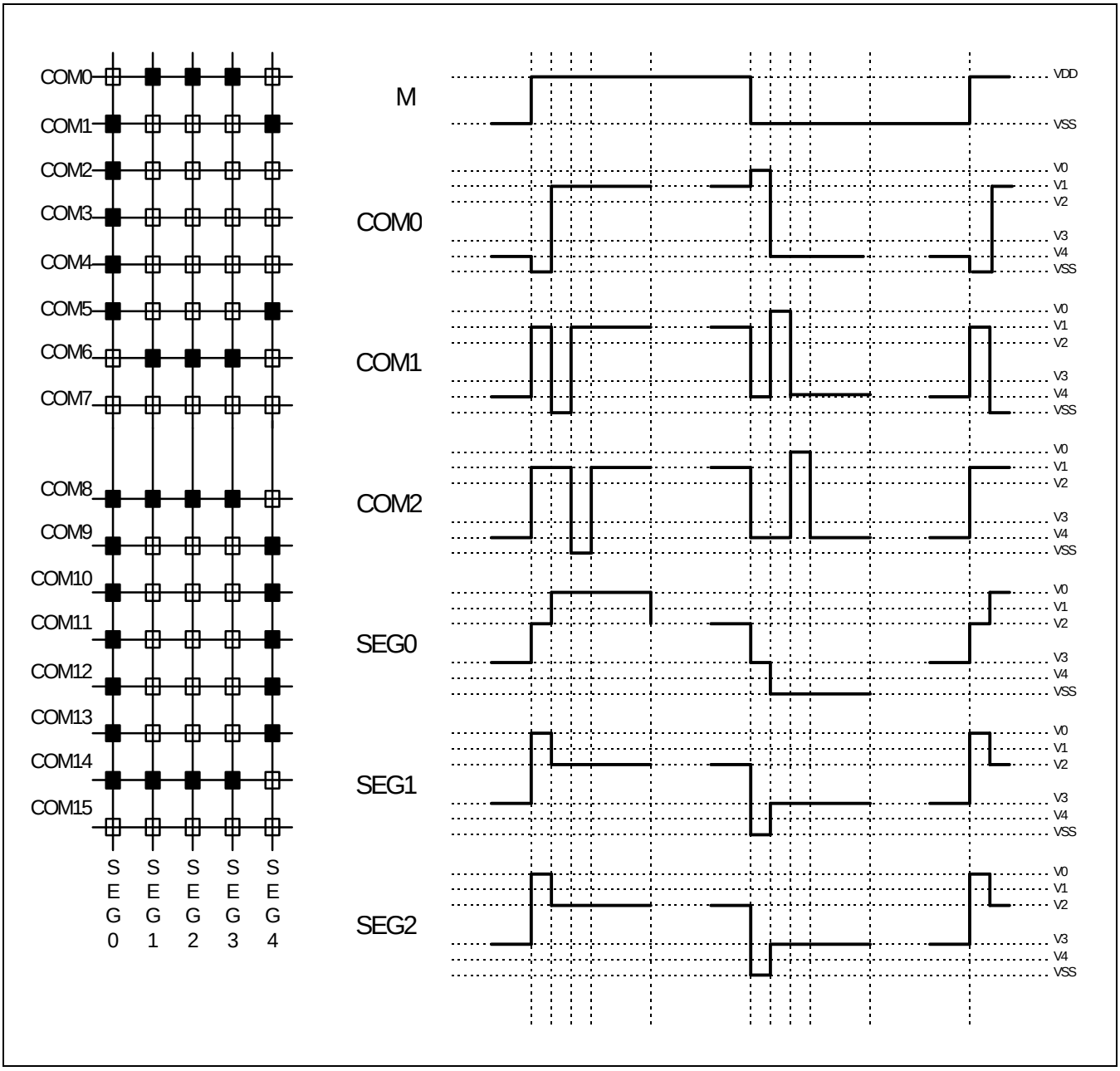


Figure 11. Segment and Common Timing

Partial Display on LCD

The S6B0719 realizes the partial display function on LCD with low-duty driving for saving power consumption and showing the various display duties. To show the various display duties on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

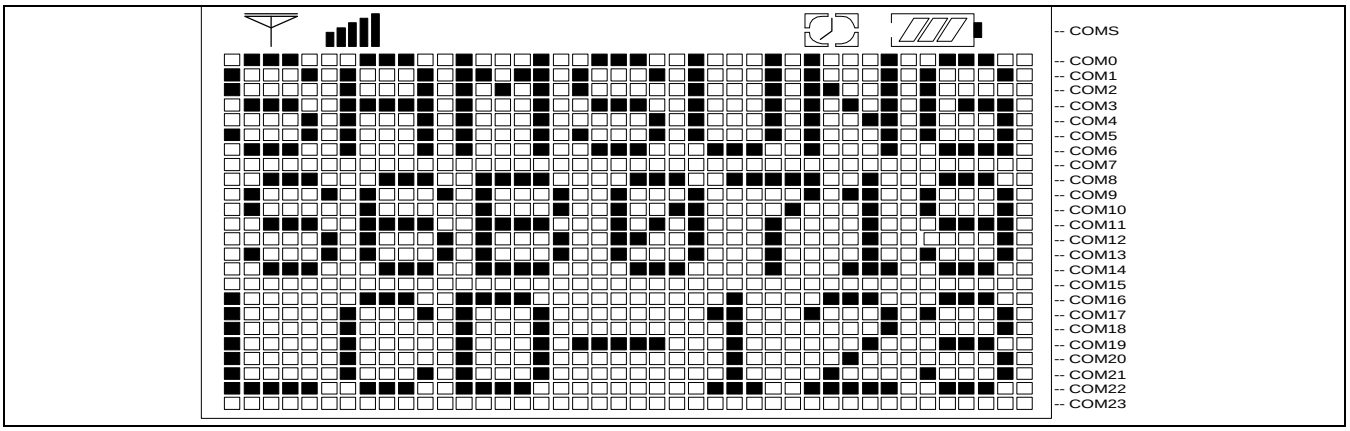


Figure 12. Reference Example for Partial Display (Display Duty = 25)

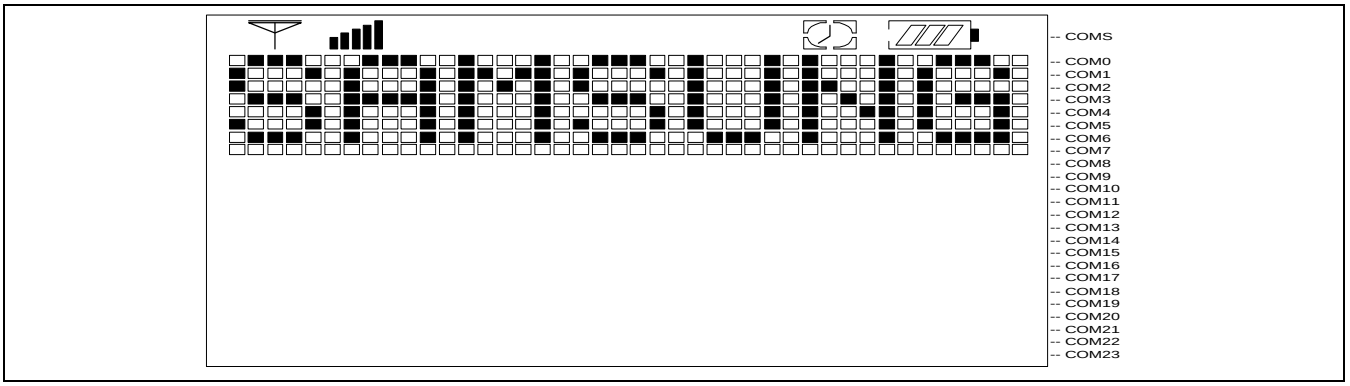


Figure 13. Partial Display (Partial Display Duty = 9, Initial COM0 = 0)

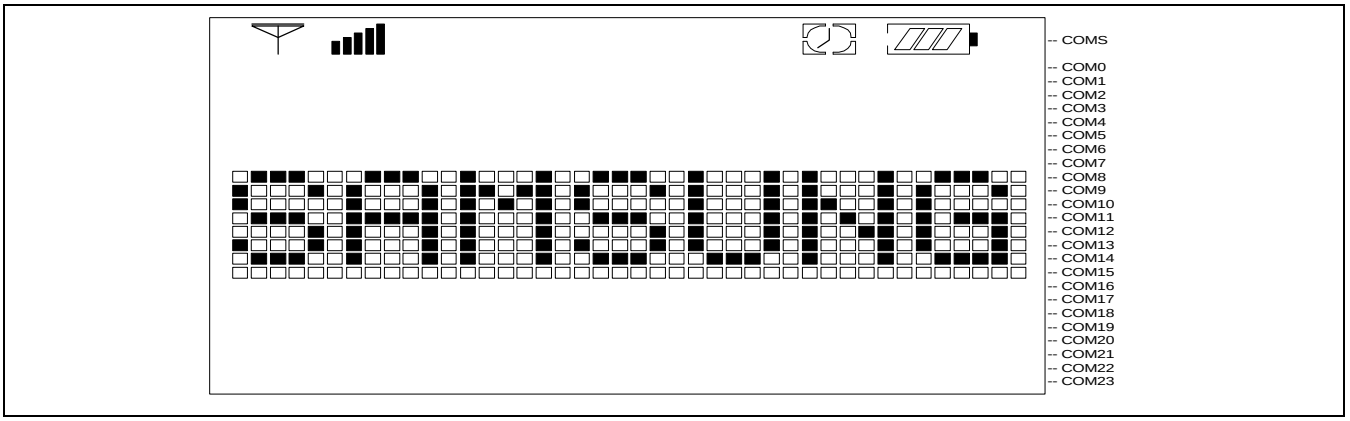


Figure 14. Moving Display (Partial Display Duty = 9, Initial COM0 = 8)

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 12 shows the referenced combinations in using Power Supply circuits.

Table 12. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	External input	Open	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5 or 6 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 μF]

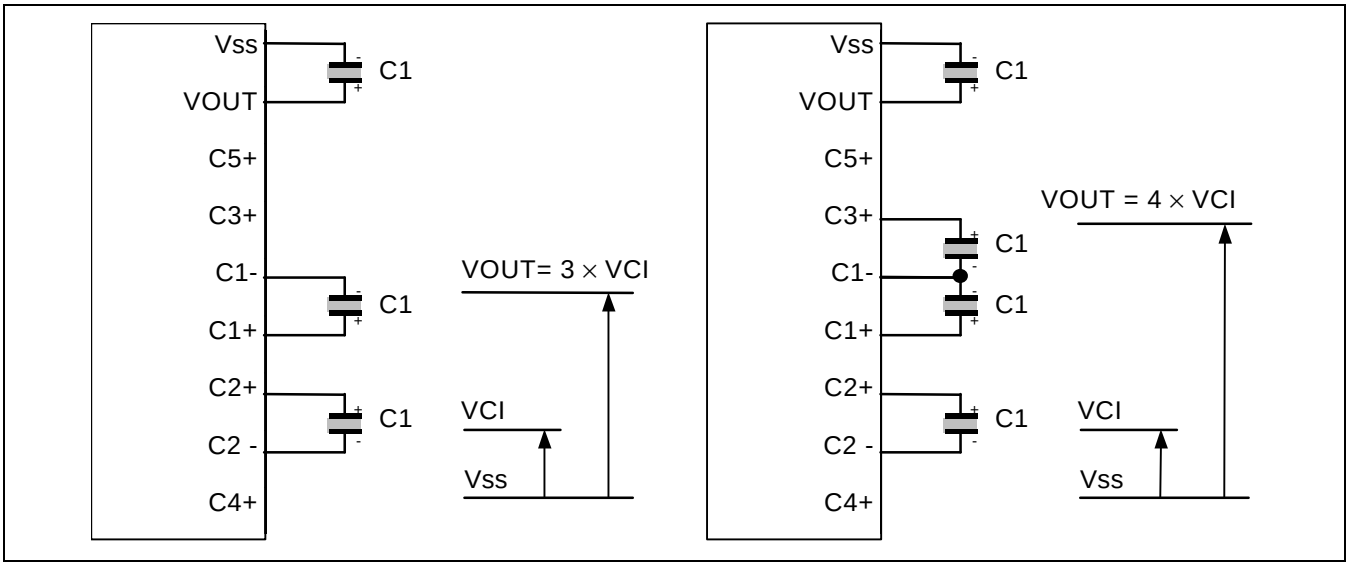


Figure 15. Three Times Boosting Circuit

Figure 16. Four Times Boosting Circuit

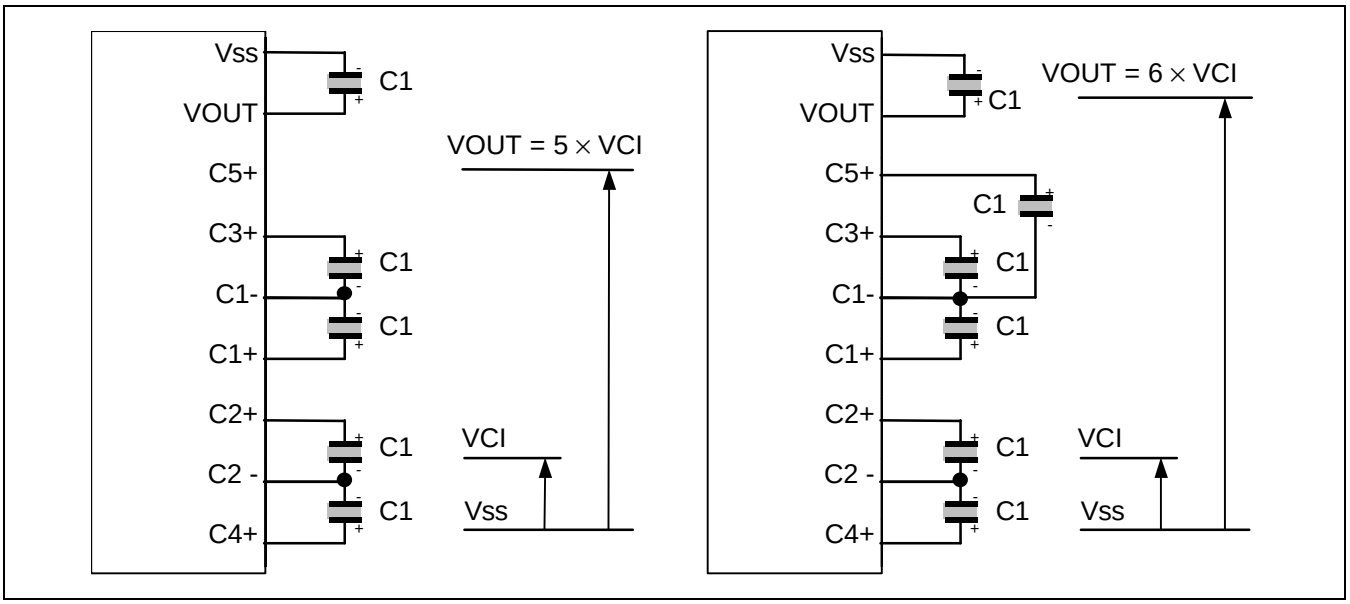


Figure 17. Five Times Boosting Circuit

Figure 18. Six Times Boosting Circuit

Voltage Regulator Circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 19, it is necessary to be applied internally or externally.

For the Eq. 6-1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 6-2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in Table 13.

$$V0 = \{ 1 + (Rb / Ra) \} \times V_{EV} [V] \text{ ------ (Eq. 6-1)}$$

$$V_{EV} = \{ 1 - (63 - \alpha) / 200 \} \times 2.0 = 1.69 [V] \text{ ------ (Eq. 6.2)}$$

Table 13. V_{REF} Voltage at Ta = 25°C

REF	Temp. coefficient	V_{REF} [V]
1	-0.05% / °C	2.0
0	External input	VEXT

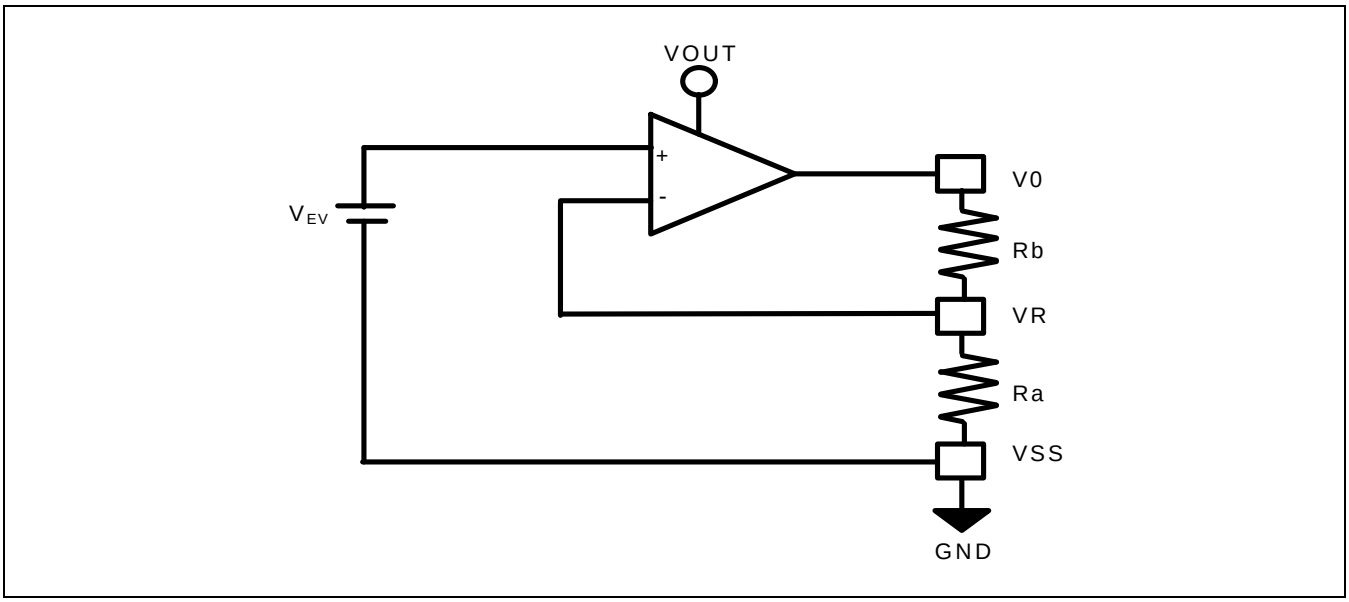


Figure 19. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.6	3.4	4.2	5.0	5.8	6.6	7.4	8.3

Table 14. Internal Rb / Ra ratio Depending on 3-bit Data (R2 R1 R0)

Figure 20 shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

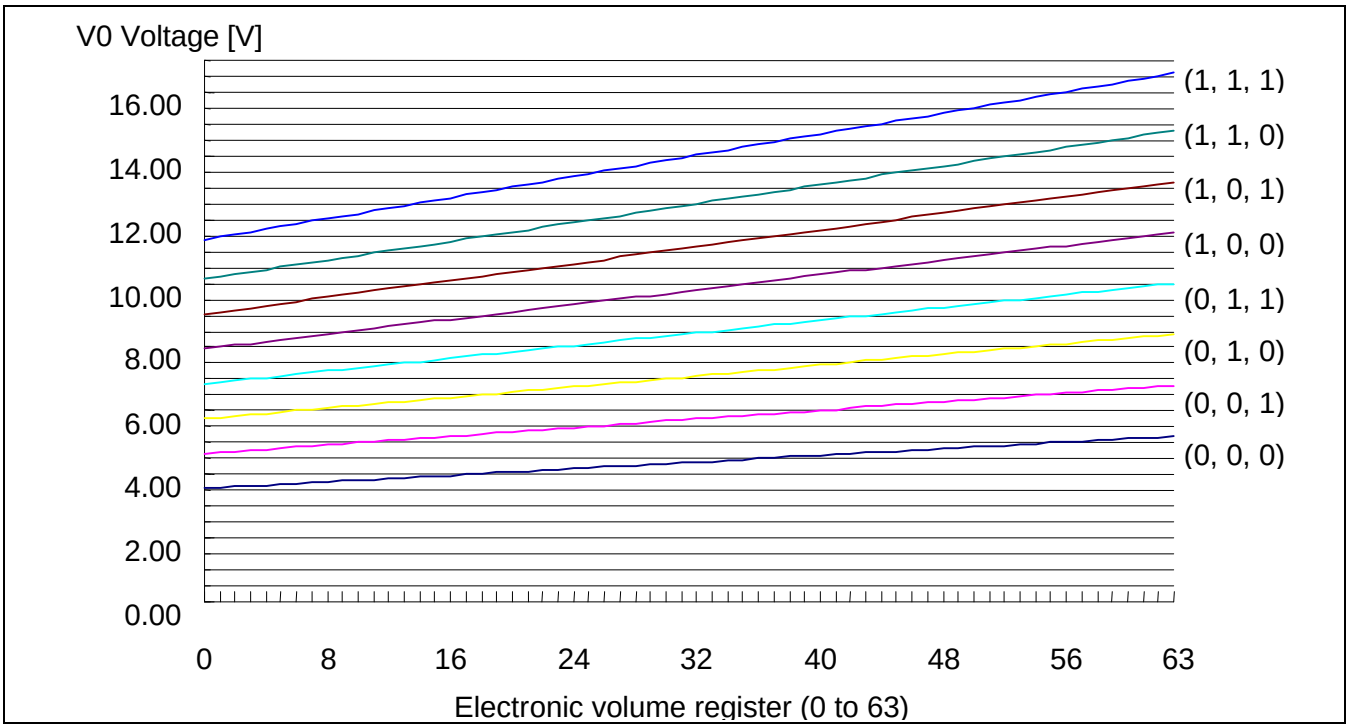


Figure 20. V0 Voltage by 1 + (Rb / Ra) and Electronic Volume Levels

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is “L”, it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 *u*A

From Eq. 6.1
$10 = \{ 1 + (Rb / Ra) \} \times V_{EV}$ [V] ------ (Eq. 6.3)

From Eq. 6.2
$V_{EV} = \{ 1 - (63 - 32) / 200 \} \times 2.0 = 1.69$ [V] ------ (Eq. 6.4)

From requirement 3
$10 / (Ra + Rb) = 1$ [uA] ------ (Eq. 6.5)

From equations Eq. 6.3, 6.4 and 6.5
Ra = 1.69 [MΩ]
Rb = 8.31 [MΩ]

Table 15 shows the range of V0 depending on the above requirements.

Table 15. The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.10	.....	10.00	.....	11.83

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and these output impedance are converted by the Voltage Follower for increasing drive capability. Table 16 shows the relationship between V1 to V4 level and each duty ratio.

Table 16. V1 to V4 Level

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-1)/N x V0	2/N x V0	1/N x V0	N = 4 to 11

REFERENCE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [㎷F], C2 = 0.1 to 0.47 [㎷F]]

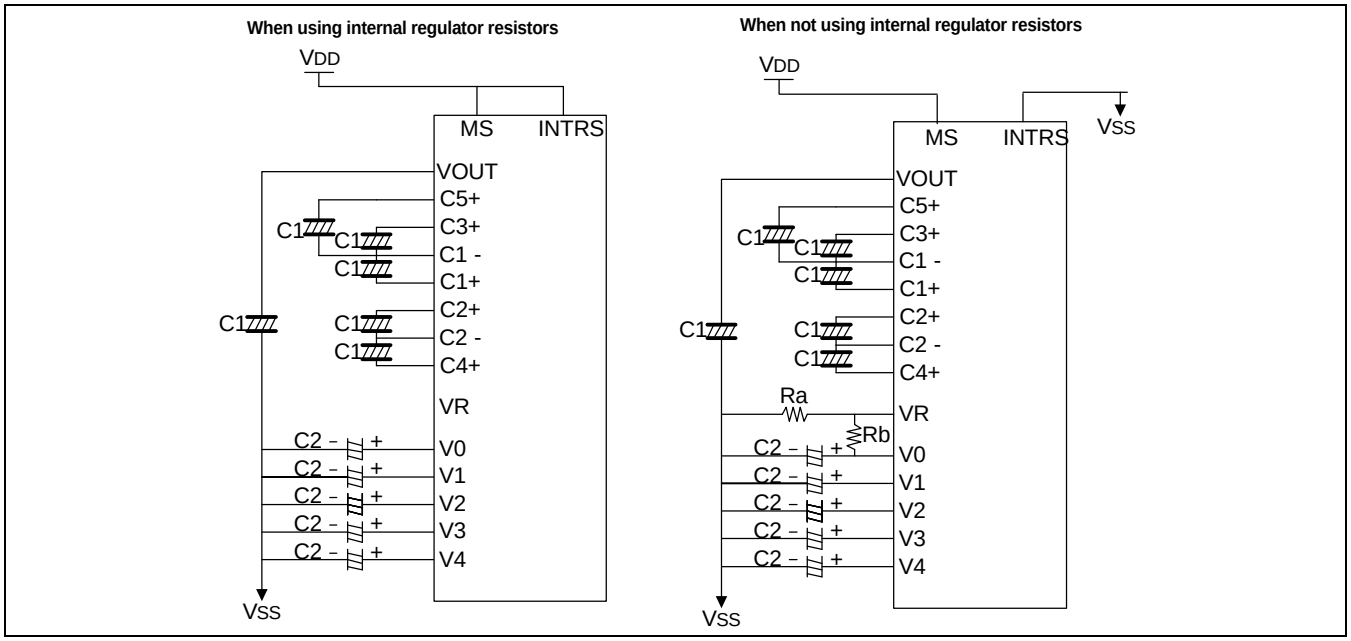


Figure 21. When Using all LCD Power Circuits (6-Time V/C: ON, V/R: ON, V/F: ON)

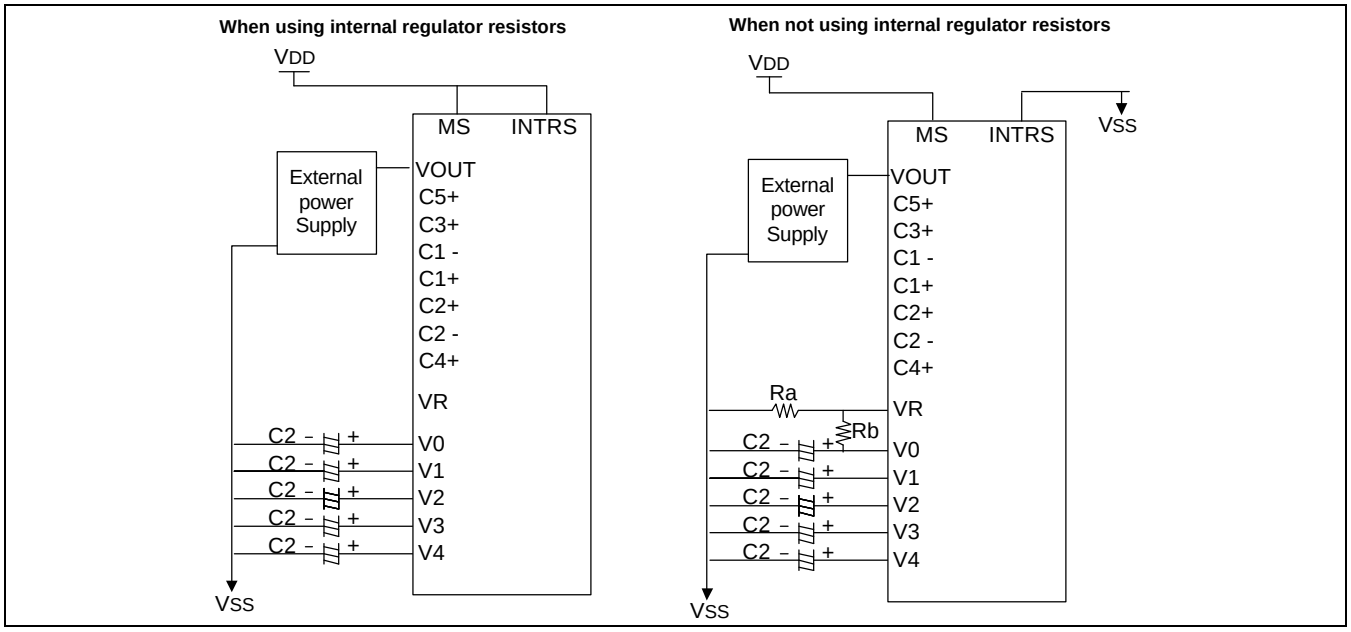


Figure 22. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

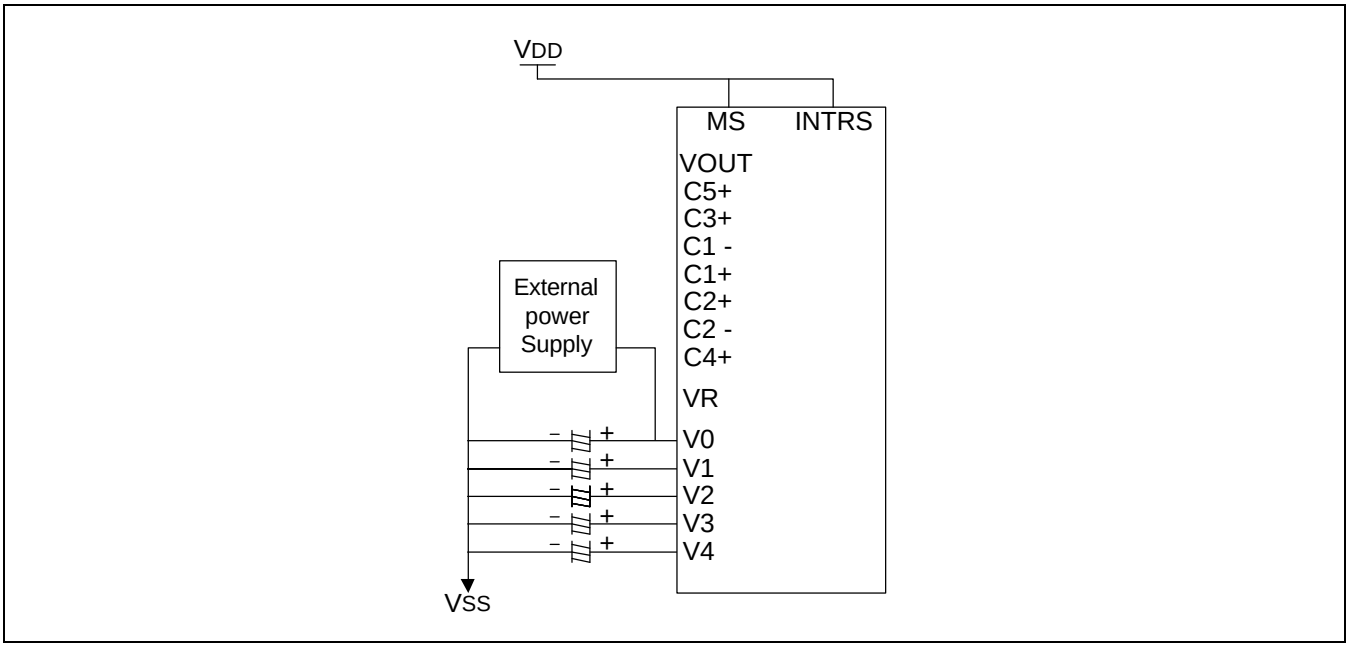


Figure 23. When Using only Voltage Follower Circuit (V/C: OFF, V/R: OFF, V/F: ON)

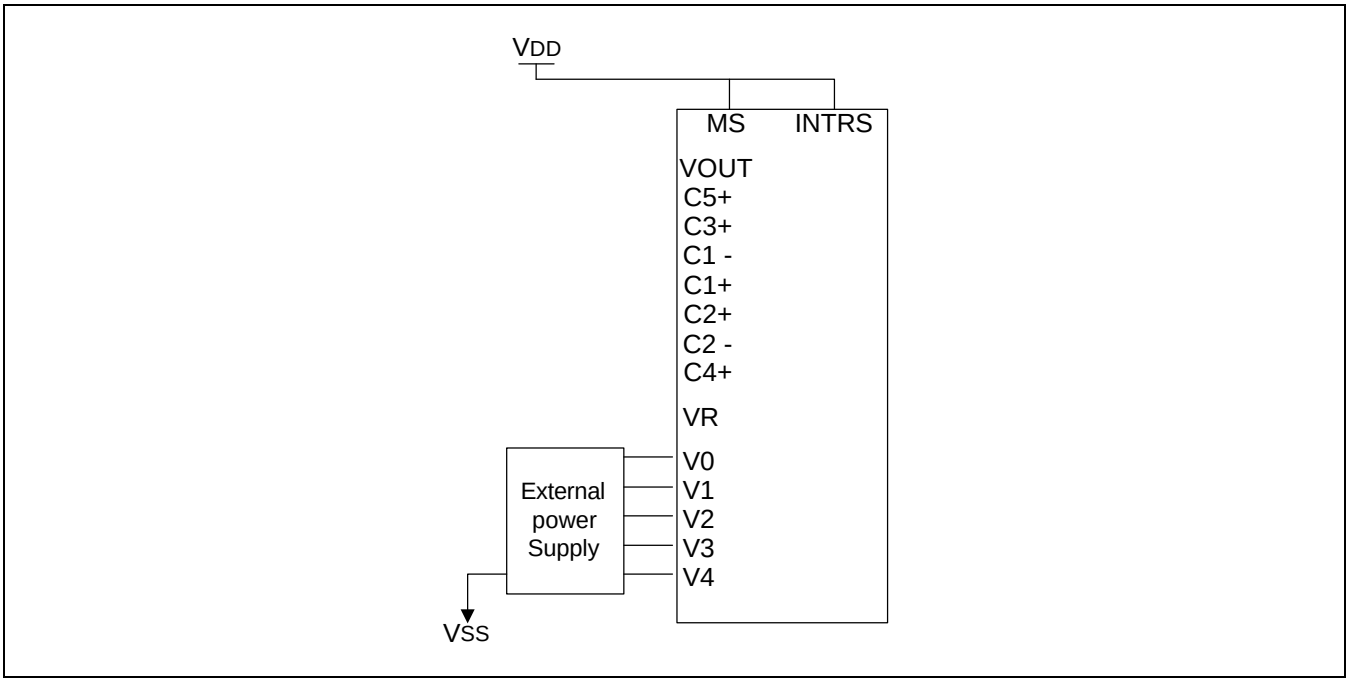


Figure 24. When Not Using all LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Display ON / OFF: OFF
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/105
Reverse display ON / OFF: OFF (normal)
n-line inversion register: 0 (disable)
Entire display ON / OFF: OFF (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC step up: 3 times converter circuit = (0, 0)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register: (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
LCD bias ratio: 1/11
SHL select: OFF (normal)
ADC select: OFF (normal)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
Oscillator status: OFF
Power save mode: release

When RESET instruction is issued, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: OFF
Initial display line: 0 (First)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)

While RESETB is “L” or reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 17. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON	RES	0	0	0	0	Read the internal status
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON / OFF	0	0	1	0	1	0	1	1	1	D	D = 0: display OFF D = 1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial display duty ratio
	0	0	×	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set n-line inversion register
	0	0	×	×	×	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line Inversion mode
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	REV = 0: normal display REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	EON = 0: normal display EON = 1: entire display ON

Table 17. Instruction Table (Continued)

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	1	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the electronic volume register
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL = 0: normal direction SHL = 1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC = 0: normal direction ADC = 1: reverse direction
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	2-byte instruction to specify the static indicator mode
Set static indicator register	0	0	×	×	×	×	×	×	S1	S0	
Oscillator ON start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	P	P = 0: standby mode P = 1: sleep mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
NOP	0	0	1	1	1	0	0	0	1	1	***No operation***
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is incremented by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is incremented by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

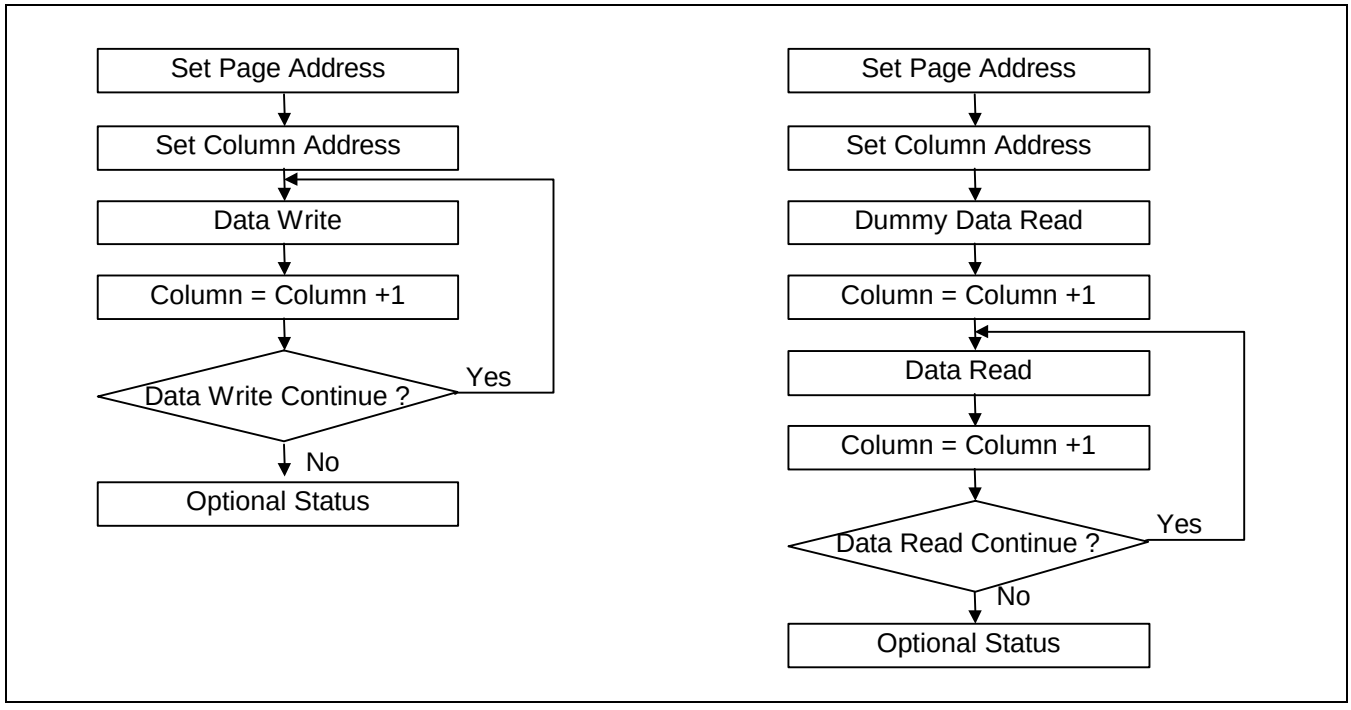


Figure 25. Sequence for Writing Display Data

Figure 26. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B0719

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON	RES	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG159 → SEG0), 1: normal direction (SEG0 → SEG159)
ON	Indicates display ON / OFF status 0: display ON, 1: display OFF
RES	Indicates the initialization is in progress by RESETB signal 0: chip is active, 1: chip is being reset.

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Selected page	Description
0	0	0	0	0	Accessible pages for displaying dot-matrix display data
0	0	0	1	1	
0	0	1	0	2	
:	:	:	:	:	
1	0	0	1	10	
1	0	1	0	11	
1	0	1	1	12	
1	1	0	0	13	Accessible page for displaying icons
1	1	0	1	14	Not accessible page. Do not use these pages.
1	1	1	0	15	

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically incremented.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Selected column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	0	1	157
1	0	0	1	1	1	1	0	158
1	0	0	1	1	1	1	1	159
1	0	1	0	0	0	0	0	Not accessible column
1	0	1	0	0	0	0	1	
1	0	1	0	0	0	1	0	

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

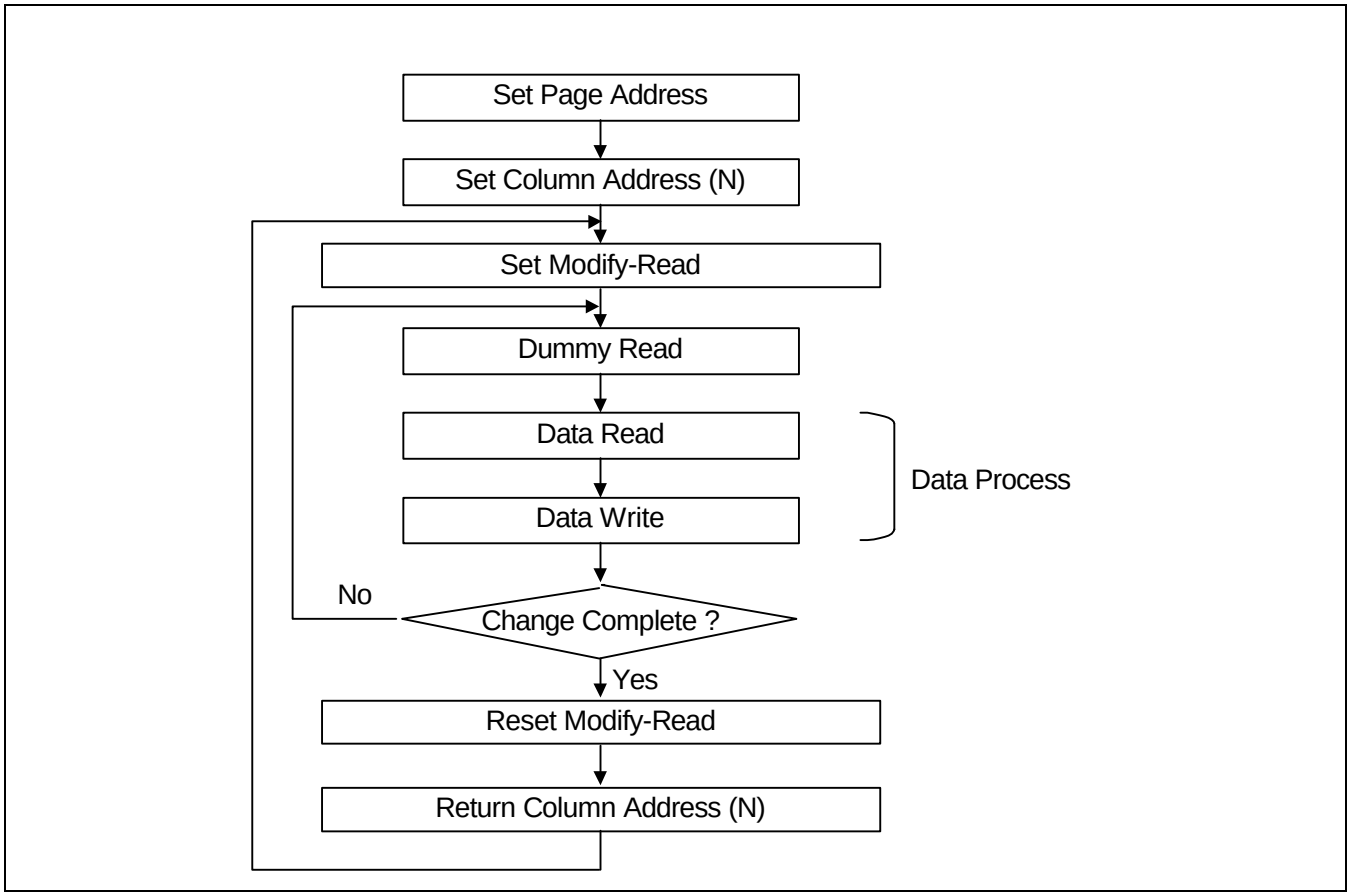


Figure 27. Sequence for Cursor Display

Display ON / OFF

Turns the Display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	D

D = 1: display ON
D = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top row (COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Selected line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	0	0	1	1	0	102
1	1	0	0	1	1	1	103
1	1	0	1	0	0	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

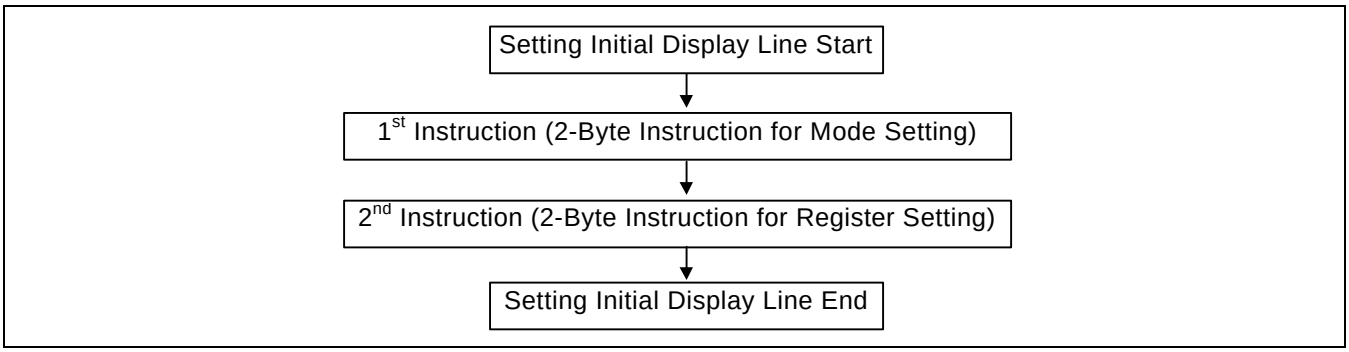


Figure 28. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
:	:	:	:	:	:	:	:
1	1	0	0	1	0	1	COM101
1	1	0	0	1	1	0	COM102
1	1	0	0	1	1	1	COM103
1	1	0	1	0	0	0	No operation
:	:	:	:	:	:	:	
1	1	1	1	1	1	1	

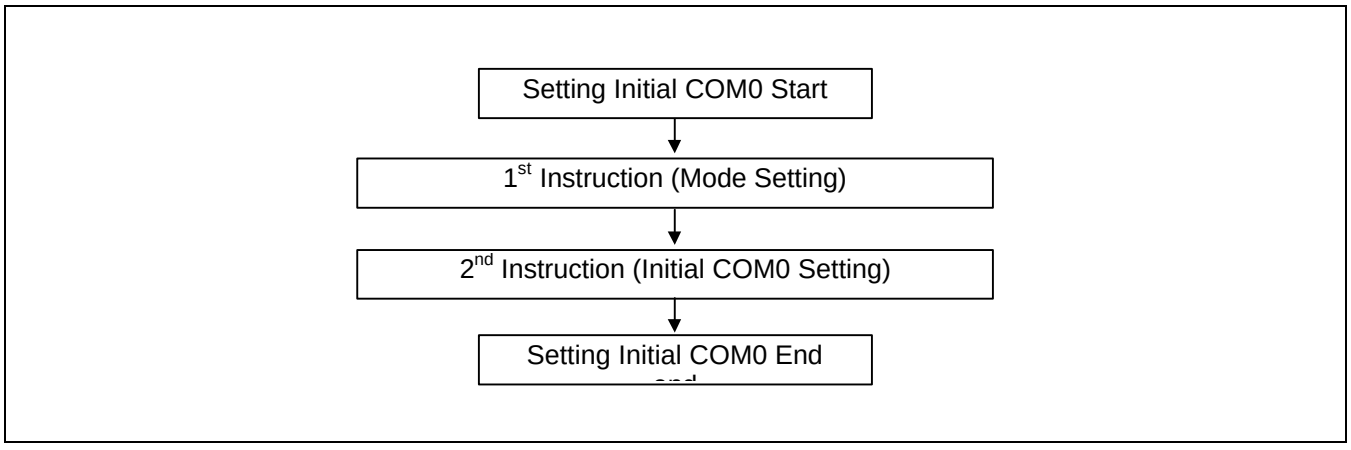


Figure 29. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

Sets the duty ratio within range of 9, 17 and 32 to 105 to realize Partial Display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	D6	D5	D4	D3	D2	D1	D0

D6	D5	D4	D3	D2	D1	D0	Selected partial duty ratio
0	0	0	1	0	0	1	1/9
0	0	1	0	0	0	1	1/17
0	1	0	0	0	0	0	1/32
0	1	0	0	0	0	1	1/33
:	:	:	:	:	:	:	:
1	0	1	0	1	0	0	1/104
1	0	1	0	1	0	1	1/105
Other combinations							No operation

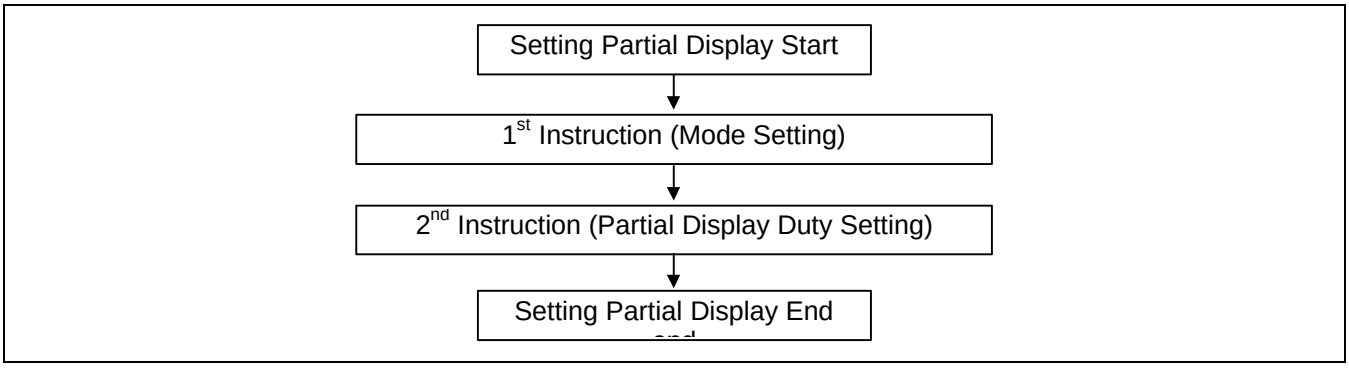


Figure 30. Sequence for Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 2 to 32 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	´	´	´	**N4**	**N3**	**N2**	**N1**	**N0**

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	2-line inversion
0	0	0	1	0	3-line inversion
0	0	0	1	1	4-line inversion
:	:	:	:	:	:
1	1	1	0	1	30-line inversion
1	1	1	1	0	31-line inversion
1	1	1	1	1	32-line inversion

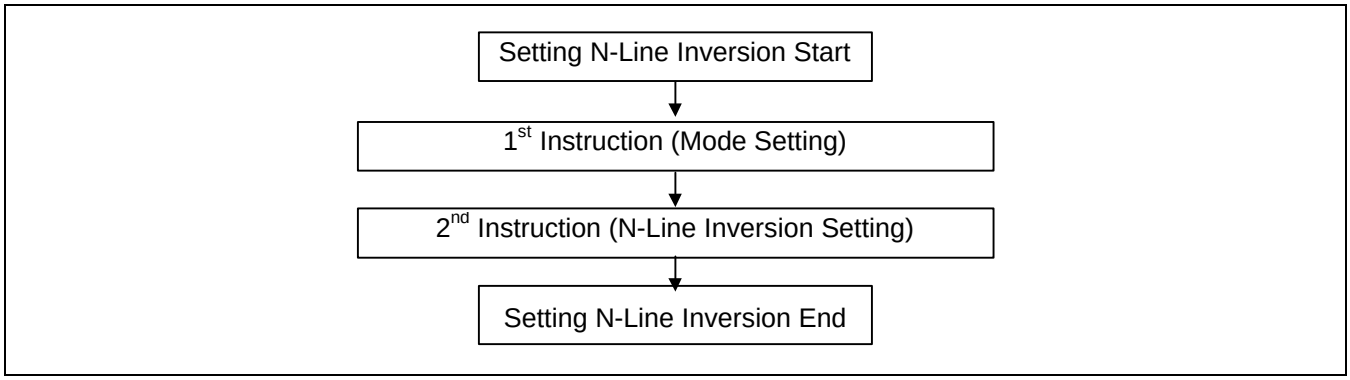


Figure 31. Sequence for Setting Partial Display

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = "1"	RAM bit data = "0"
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse Display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	RAM bit data = "1"	RAM bit data = "0"
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Entire)	LCD pixel is illuminated	LCD pixel is illuminated

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

Select DC/DC Step-up

Selects one of 4 DC/DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	1	DC1	DC0

DC1	DC0	Selected DC-DC converter circuit
0	0	3 times boosting circuit
0	1	4 times boosting circuit
1	0	5 times boosting circuit
1	1	6 times boosting circuit

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb / Ra] ratio
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

Set Electronic Volume Register

Consists of 2-byte instruction. The 1st instruction sets Electronic Volume mode, the 2nd one updates the contents of Electronic Volume register. After second instruction, Electronic Volume mode is released.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

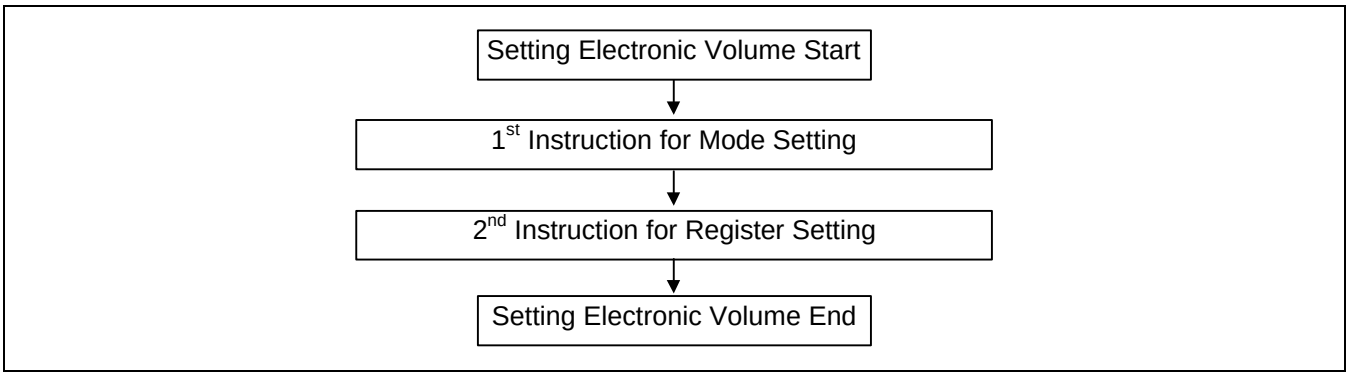


Figure 32. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD Bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	Selected LCD bias
0	0	0	1/4
0	0	1	1/5
0	1	0	1/6
0	1	1	1/7
1	0	0	1/8
1	0	1	1/9
1	1	0	1/10
1	1	1	1/11

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

SHL = 0: normal direction (COM0 → COM103)
SHL = 1: reverse direction (COM103 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG159)
ADC = 1: reverse direction (SEG159 → SEG0)

Set Static Indicator State

Consists of two bytes instruction. The first byte instruction (set Static Indicator mode) enables the second byte instruction (set Static Indicator register) to be valid. The first byte sets the Static Indicator ON / OFF. When it is on, the second byte updates the contents of Static Indicator register without issuing any other instruction and this Static Indicator state is released after setting the data of indicator register.

The 1st Instruction: Set Static Indicator Mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The 2nd Instruction: Set Static Indicator Register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	×	×	×	×	S1	S0

S1	S0	Status of static indicator output
0	0	OFF
0	1	ON (about 0.5 second blinking)
1	0	ON (about 1 second blinking)
1	1	ON (always ON)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply that is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Power Save

The S6B0719 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	P

P = 0: standby mode
P = 1: sleep mode

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

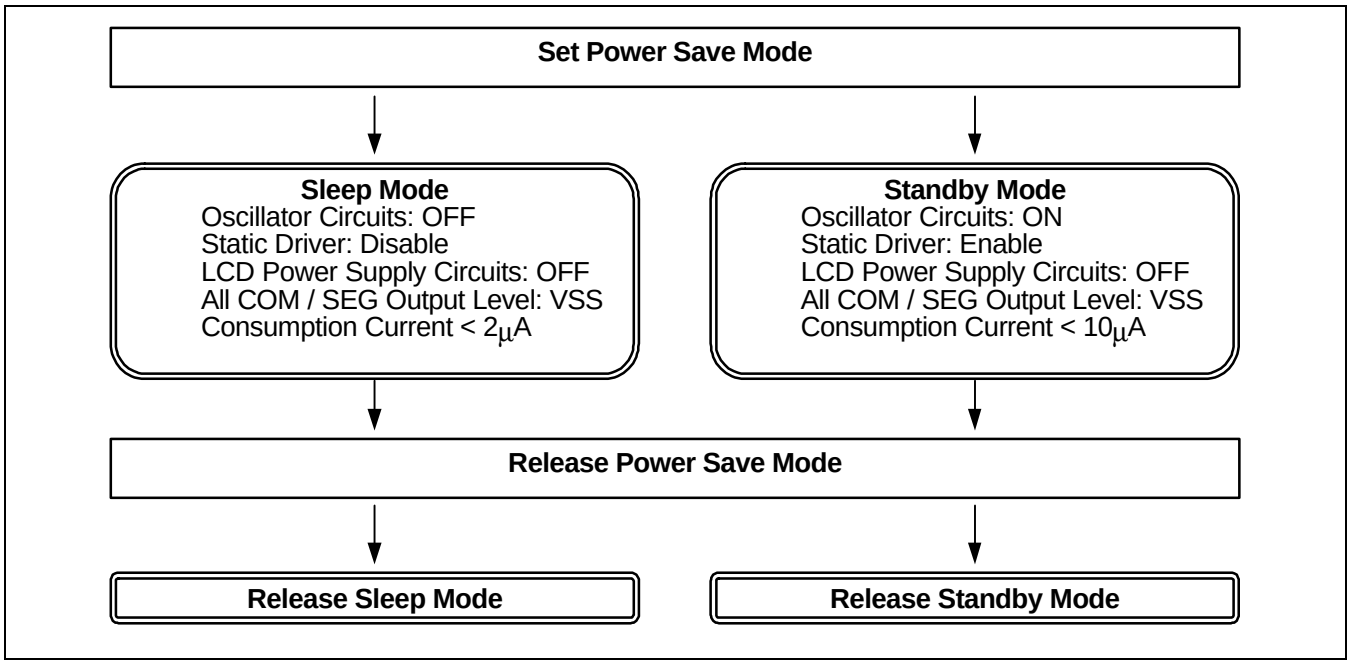


Figure 33. Power Save Routine

NOP

Non-operation

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

Referential Instruction Setup Flow: Initializing with the Built-in Power Supply Circuits

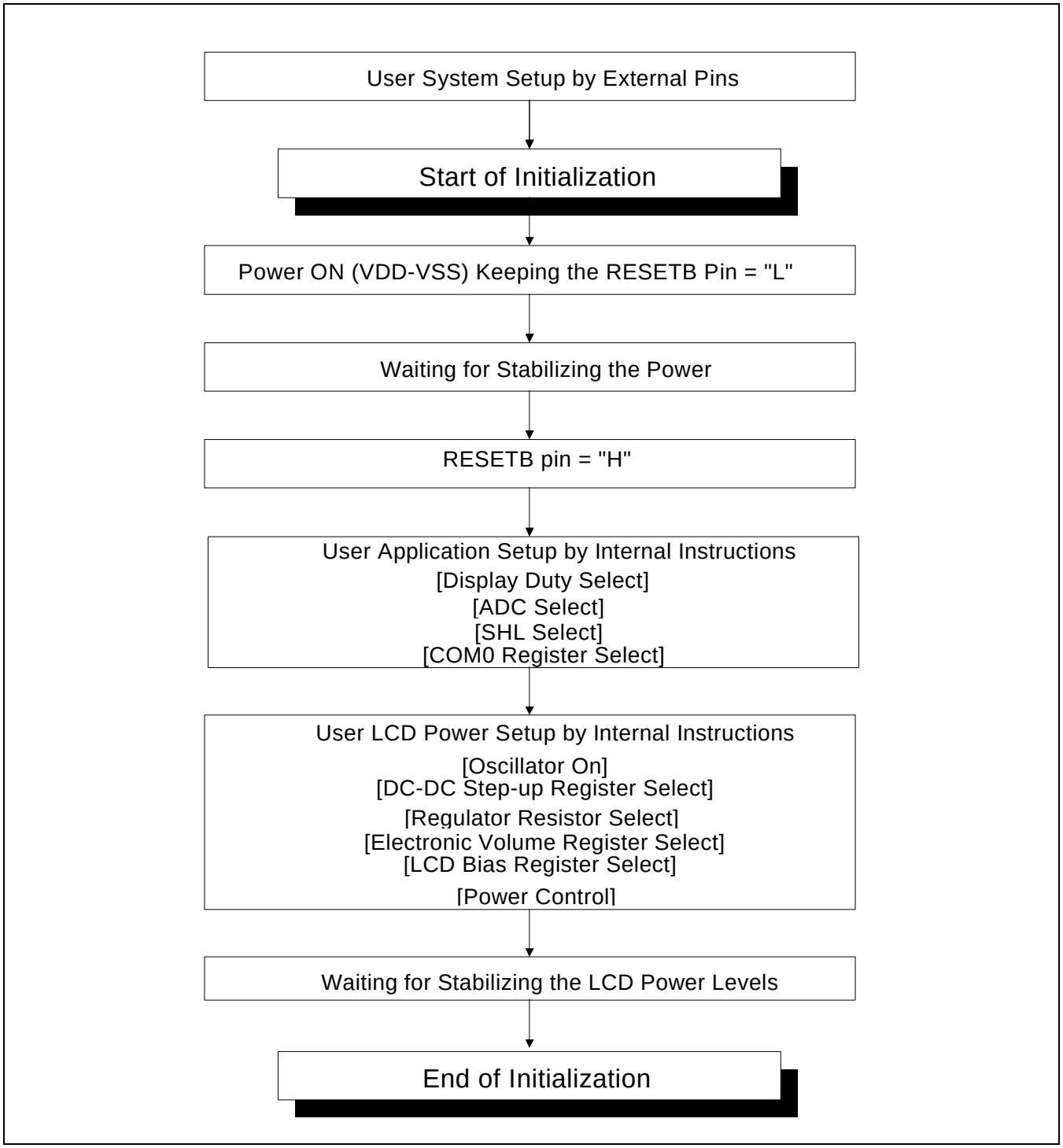


Figure 34. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the Built-in Power Supply Circuits

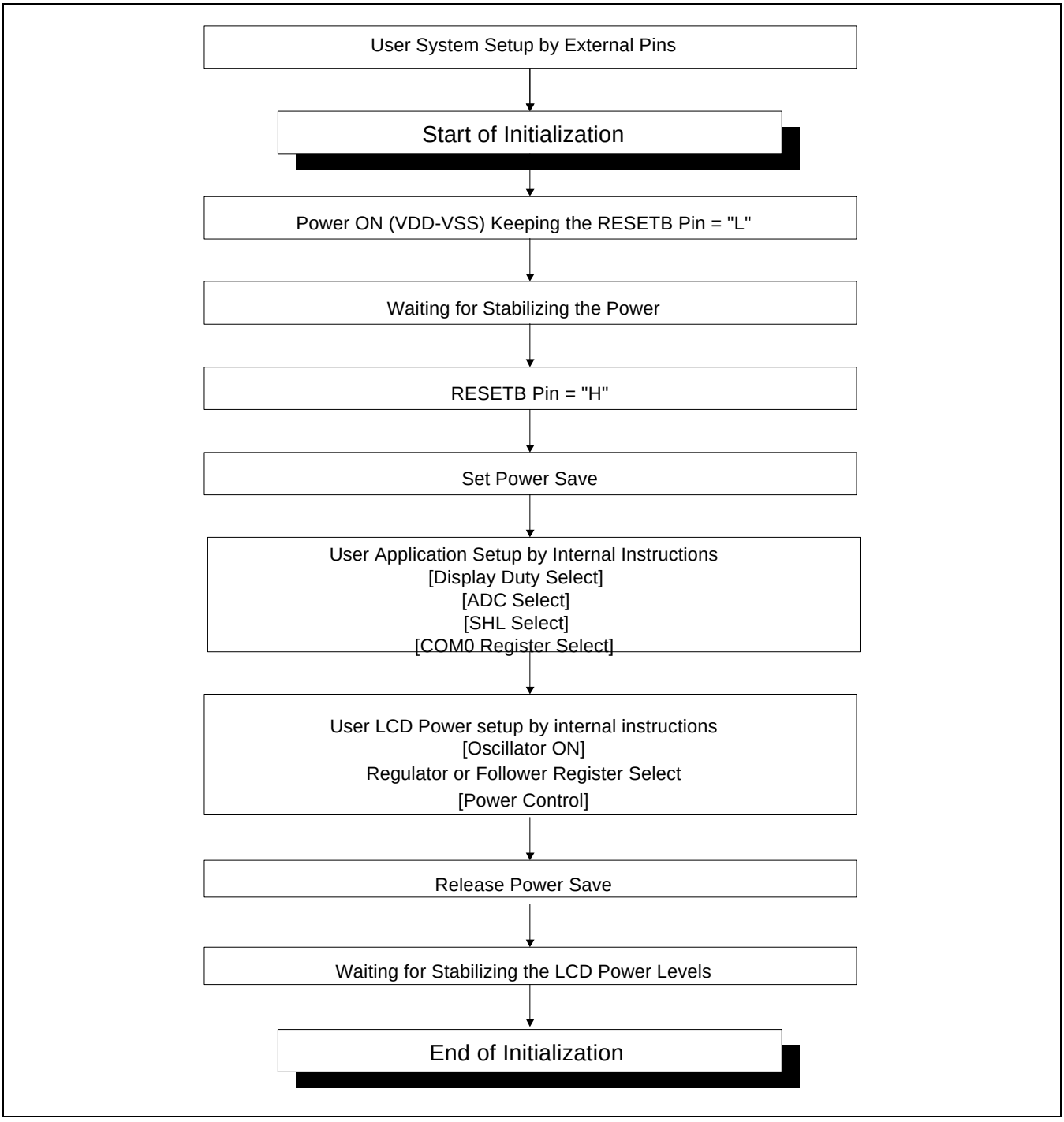


Figure 35. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

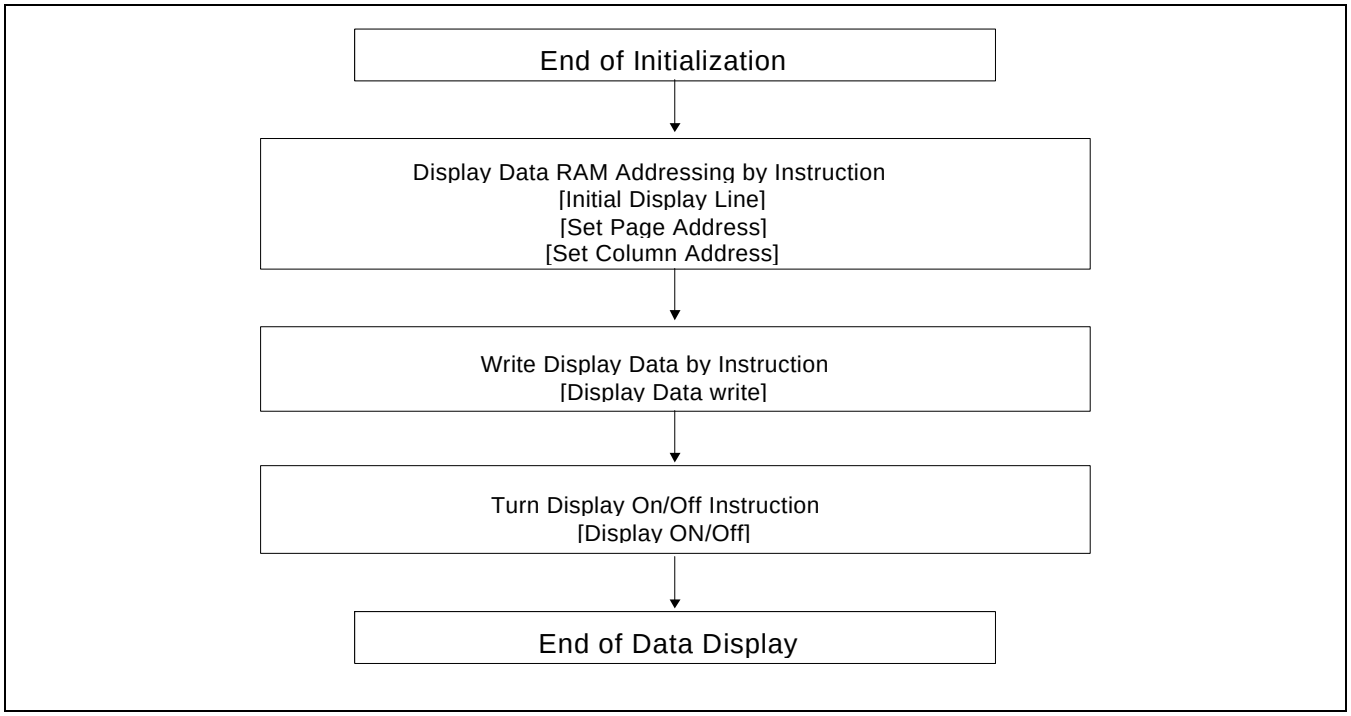


Figure 36. Data Displaying

Referential Instruction Setup Flow: Power OFF

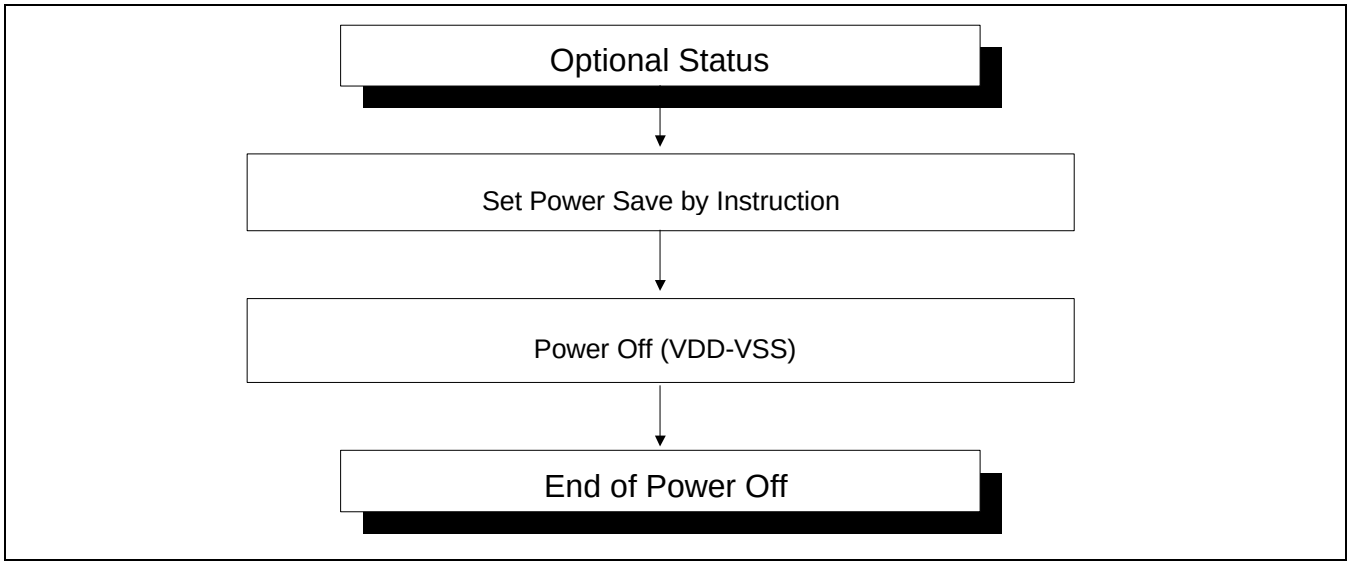


Figure 37. Power OFF

Referential Instruction Setup Flow: Partial Duty Changing

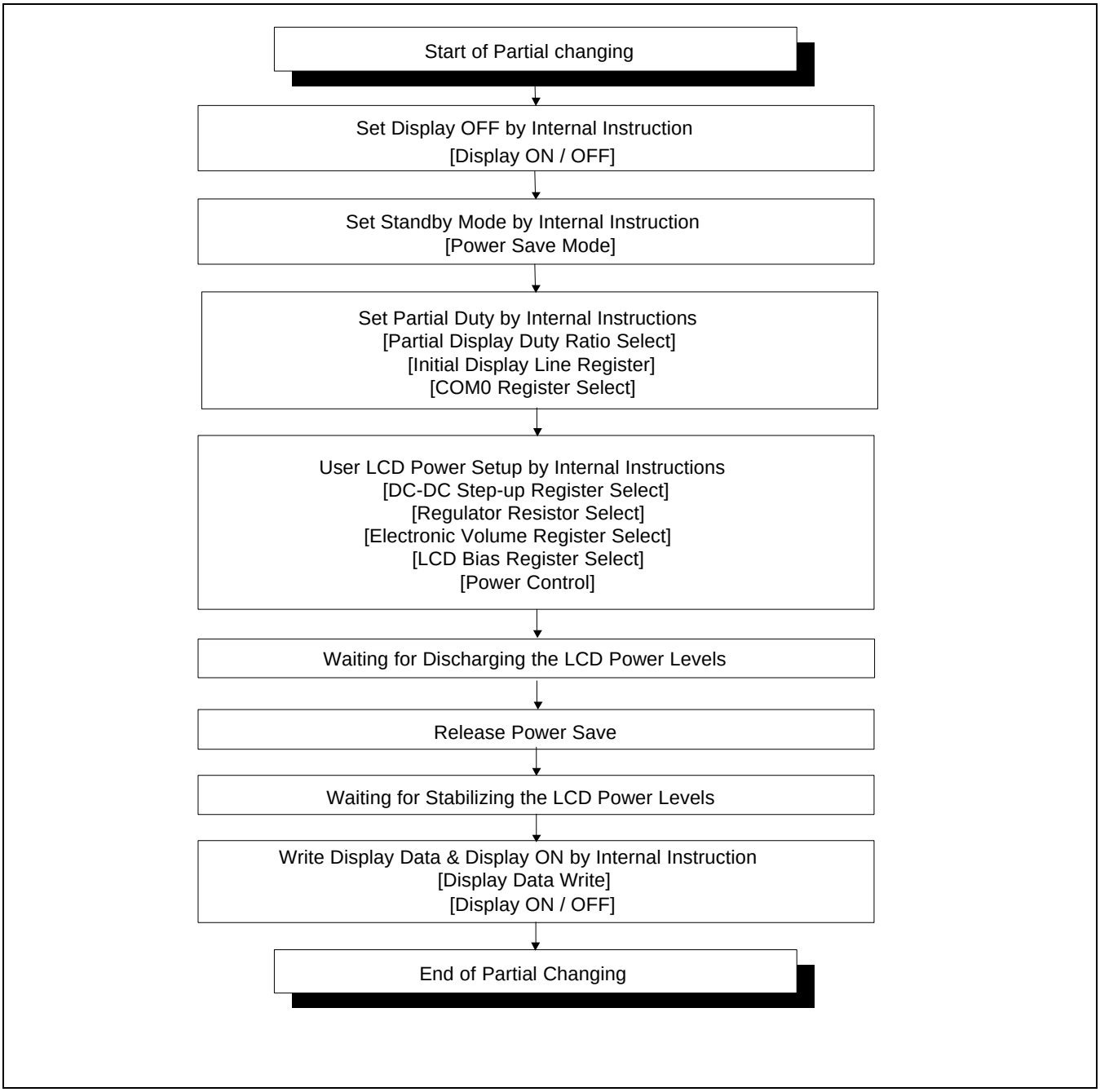


Figure 38. Partial Duty Changing

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 18. Absolute Maximum Ratings

(Vss = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 ~ + 7.0	V
	V0, VOUT	+ 0.3 ~ + 17.0	V
	V1, V2, V3, V4	+ 0.3 ~ V0	V
External reference voltage	VEXT	+0.3 ~ V_{DD}	
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STR}	- 55 ~ + 125	°C

NOTES:

1. VDD, V0, VOUT, V1 to V4, VEXT and VCI are based on Vss = 0V.
2. Voltage VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 19. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40~85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		2.4	-	3.6	V	V_{DD} *1
Operating voltage (2)		V0		4.0	-	15.0	V	V0, *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*3
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*5
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *6
Frame frequency		f_{FR}	Ta = 25°C	70	85	100	Hz	*7 FR

Table 20. DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Voltage converter circuit output voltage	VOUT	×3 / ×4 / ×5 / ×6 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator circuit operating voltage	VOUT		6.0	-	17.0	V	VOUT
Voltage follower circuit operating voltage	V0		4.0	-	15.0	V	V0 *8
Reference voltage	V_{REF}	Ta = 25°C	1.94	2.00	2.06	V	*9

Dynamic Current Consumption (1) when an External Power Supply is used.

Table 21. Display OFF

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V0 - Vss = 7.0V, duty = 1/33			TBD	µA	*10
		V0 - Vss = 10.0V, duty = 1/65			TBD		
		V0 - Vss = 13.0V, duty = 1/105			TBD		

Table 22. Checker Pattern

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	I_{DD1}	V0 - Vss = 7.0V, duty = 1/33			TBD	µA	*10
		V0 - Vss = 10.0V, duty = 1/65			TBD		
		V0 - Vss = 13.0V, duty = 1/105			TBD		

Dynamic Current Consumption (2) when the Internal Power Supply is ON

Table 23. Display OFF

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	IDD2	V0 - Vss = 7.0V, X3 boosting, duty = 1/33, normal mode	-	-	TBD	µA	*10
		V0 - Vss = 7.0V, X3 boosting, duty = 1/33, high power mode	-	-	TBD		
		V0 - Vss = 10.0V, X4 boosting, duty = 1/65, normal mode	-	-	TBD	µA	*10
		V0 - Vss = 10.0V, X4 boosting, duty = 1/65, high power mode	-	-	TBD		
		V0 - Vss = 13.0V, X5 boosting, duty = 1/105, normal mode	-	-	TBD	µA	*10
		V0 - Vss = 13.0V, X5 boosting, duty = 1/105, high power mode	-	-	TBD		

Table 24. Check Pattern

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	IDD2	V0 - Vss = 7.0V, X3 boosting, duty = 1/33, normal mode	-	-	TBD	µA	*10
		V0 - Vss = 7.0V, X3 boosting, duty = 1/33, high power mode	-	-	TBD		
		V0 - Vss = 10.0V, X4 boosting, duty = 1/65, normal mode	-	-	TBD	µA	*10
		V0 - Vss = 10.0V, X4 boosting, duty = 1/65, high power mode	-	-	TBD		
		V0 - Vss = 13.0V, X5 boosting, duty = 1/105, normal mode	-	-	TBD	µA	*10
		V0 - Vss = 13.0V, X5 boosting, duty = 1/105, high power mode	-	-	TBD		

Dynamic Current Consumption during Power Save Mode

Table 25. Power Save Mode

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Sleep mode current	IDDS1	During sleep	-	-	2	µA	
Standby mode current	IDDS2	During standby	-	-	10	µA	

Table 26. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	F_{osc}
1/N	On-chip oscillator circuit is used	f_{FR} x N	f_{FR} x 4 x N

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 9 to 105)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, C68, PS, INTRS, HPMB, REF, CL, M and SYNC.
*4. DB0 to DB7, FR, FRS, SYNC, M and CL.
*5. Applies when the DB0 to DB7, SYNC, M, and CL pins are in high impedance.
*6. Resistance value when -0.1[mA] is applied during the On status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
*7. See Table 26 for the relationship between oscillation frequency and frame frequency.
*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is on or OFF.
The current flowing through voltage regulation resistors (Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

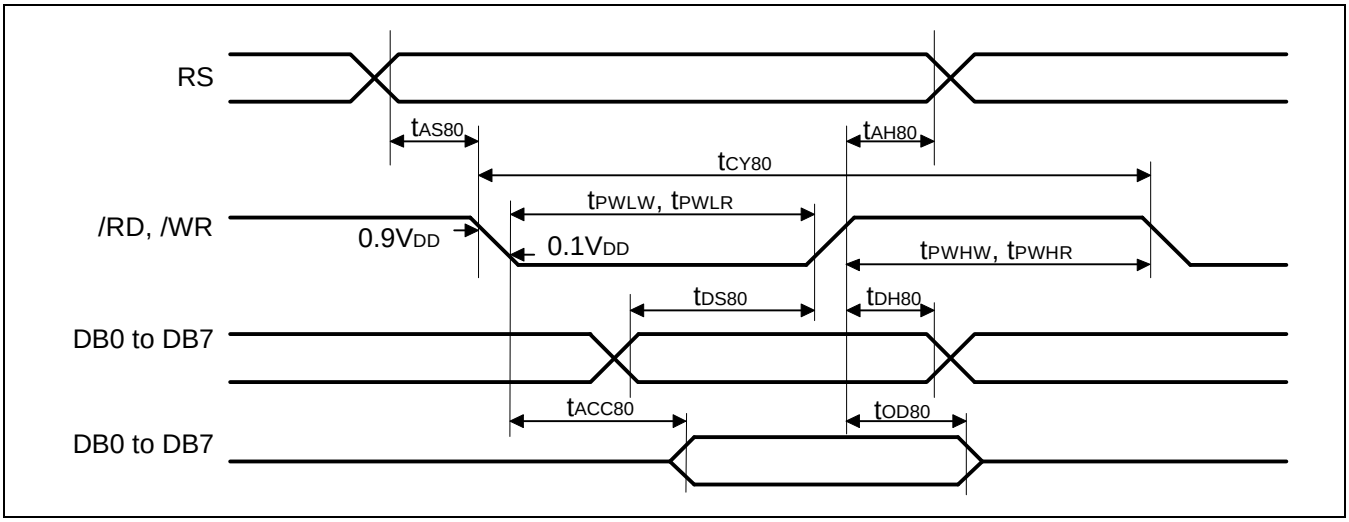


Figure 39. Parallel Interface (8080-series MPU) Timing Diagram

Table 27. AC Characteristics (8080-series Parallel Mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		0 0	- -	ns
System cycle time		t_{CY80}		300	-	ns
Pulse width low for write Pulse width High for write	RW_WR (/WR)	t_{PWLW} t_{PWHW}		60 60	- -	ns
Pulse width low for read Pulse width high for read	E_RD (/RD)	t_{PWLR} t_{PWHR}		120 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		40 15	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	- 10	140 100	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY80 - tPWLW - tPWHW) for write, (tr + tf) < (tCY80 - tPWLR - tPWHR) for read

Read / Write Characteristics (6800-series Microprocessor)

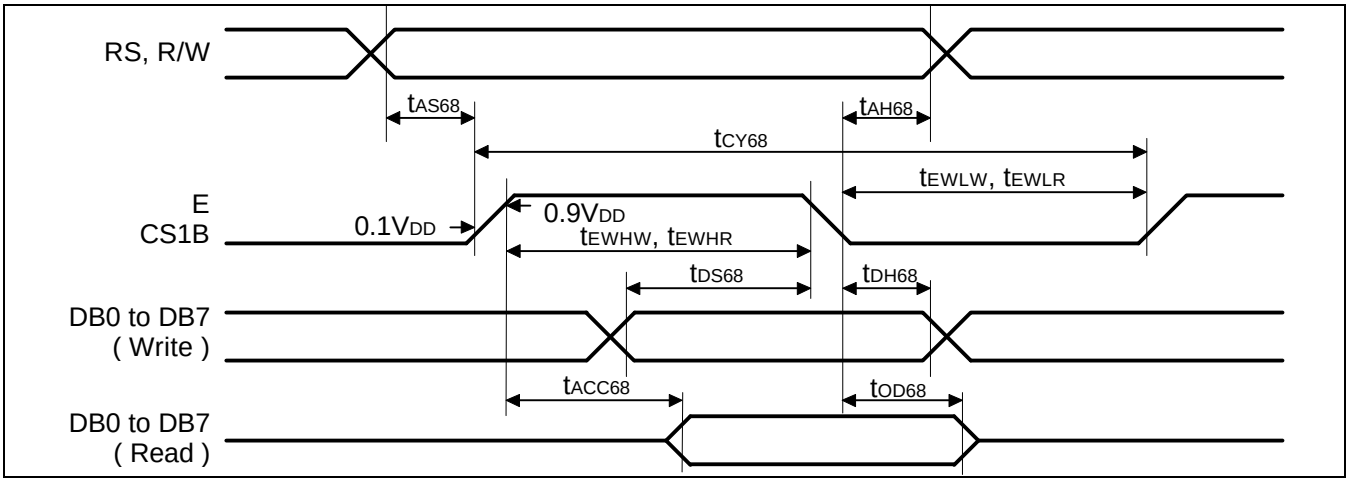


Figure 40. Parallel Interface (6800-series MPU) Timing Diagram

Table 28. AC Characteristics (6800-series Parallel Mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		0 0	- -	ns
System cycle time		t_{CY68}		300	-	ns
Enable width high for write Enable width low for write	E_RD (E)	t_{EWHW} t_{EWLW}		60 60	- -	ns
Enable width high for read Enable width low for read	E_RD (E)	t_{EWHR} t_{EWLR}		120 60	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		40 15	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	- 10	140 100	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY68 - tEWHW - tEWLW) for write, (tr + tf) < (tCY68 - tEWHR - tEWLR) for read

Serial Interface Characteristics

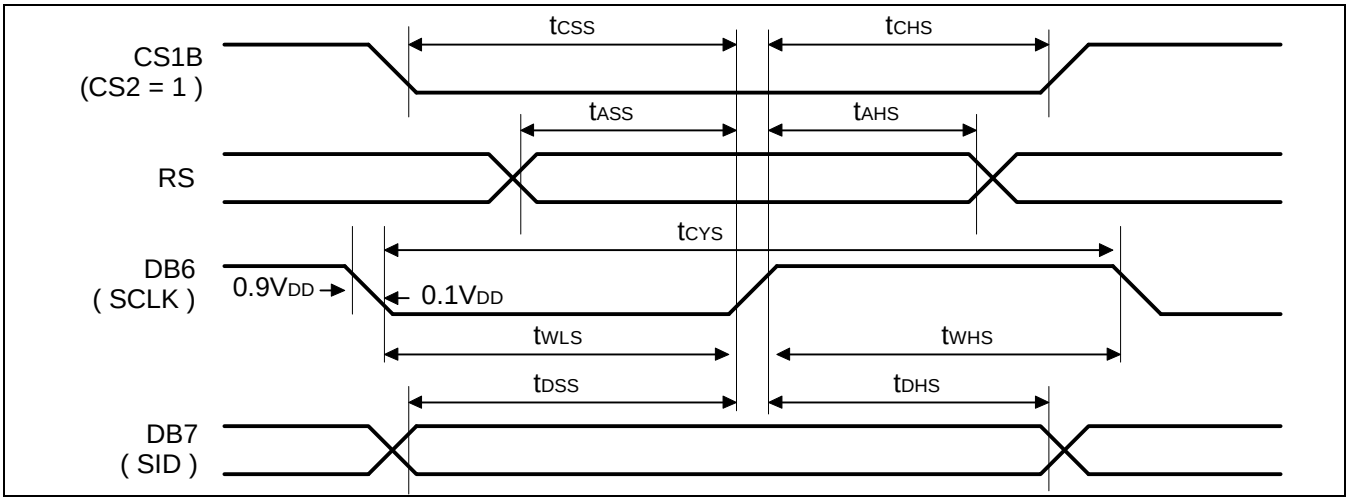


Figure 41. Serial Interface Timing Diagram

Table 29. AC Characteristics (Serial Mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{SCY} t_{SHW} t_{SLW}		250 100 100	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		150 150	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		100 100	- -	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}		150 150	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

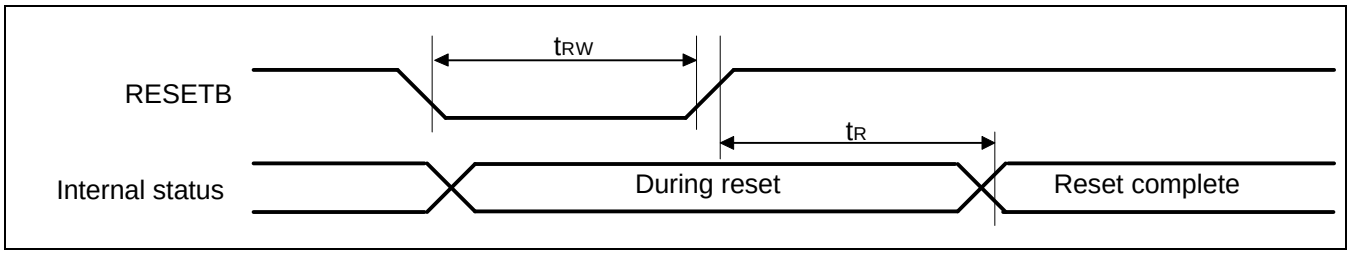


Figure 42. Reset Input Timing Diagram

Table 30. AC Characteristics (Reset mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

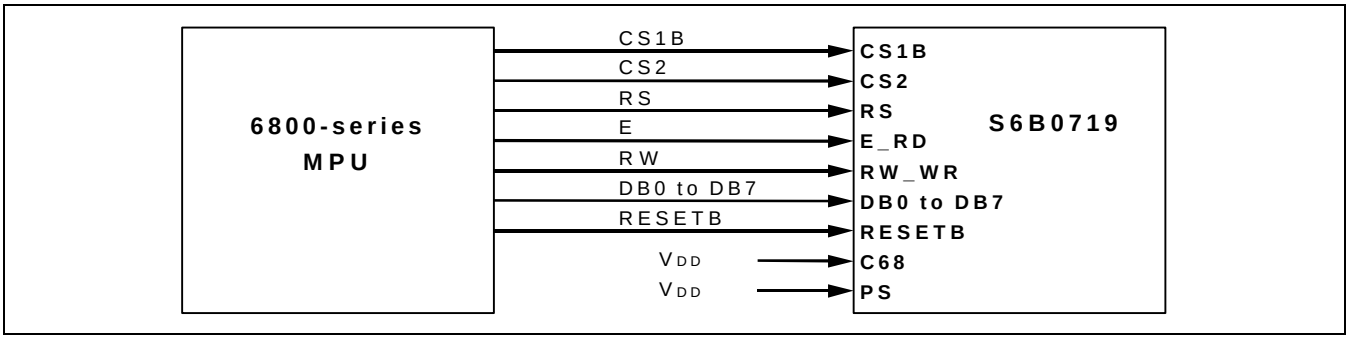


Figure 43. In Case of Interfacing with 6800-series (PS = “H”, C68 = “H”)

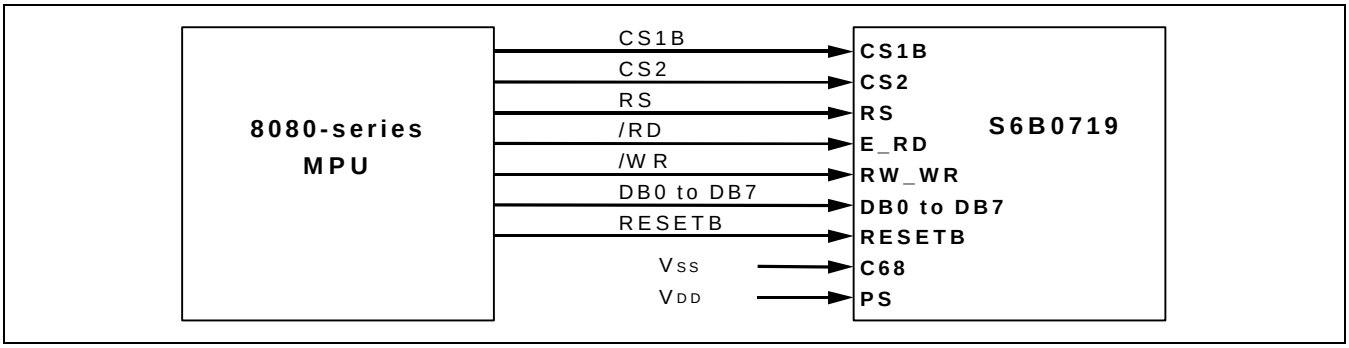


Figure 44. In Case of Interfacing with 8080-series (PS = “H”, C68 = “L”)

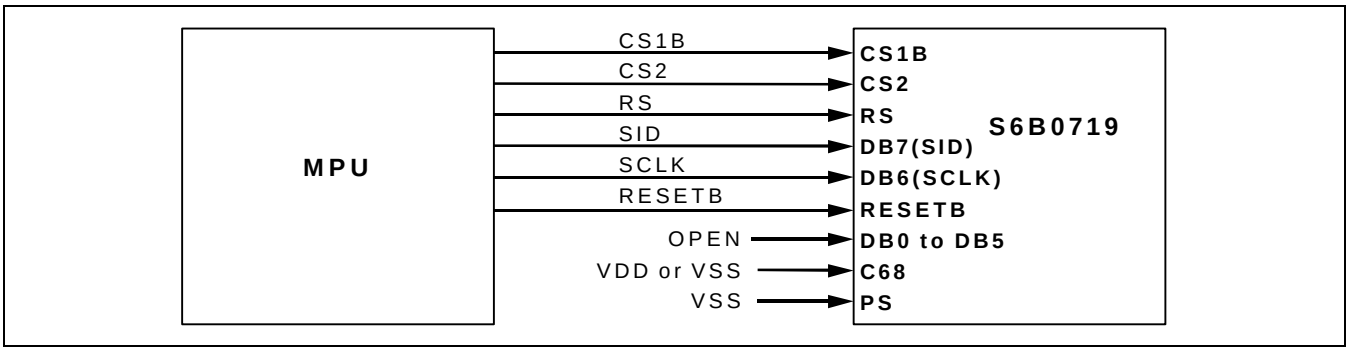


Figure 45. In Case of Serial Interface (PS = “L”, C68 = “H/L”)

CONNECTIONS BETWEEN S6B0719 AND LCD PANEL

Single Chip Configuration (1/105 Duty configurations)

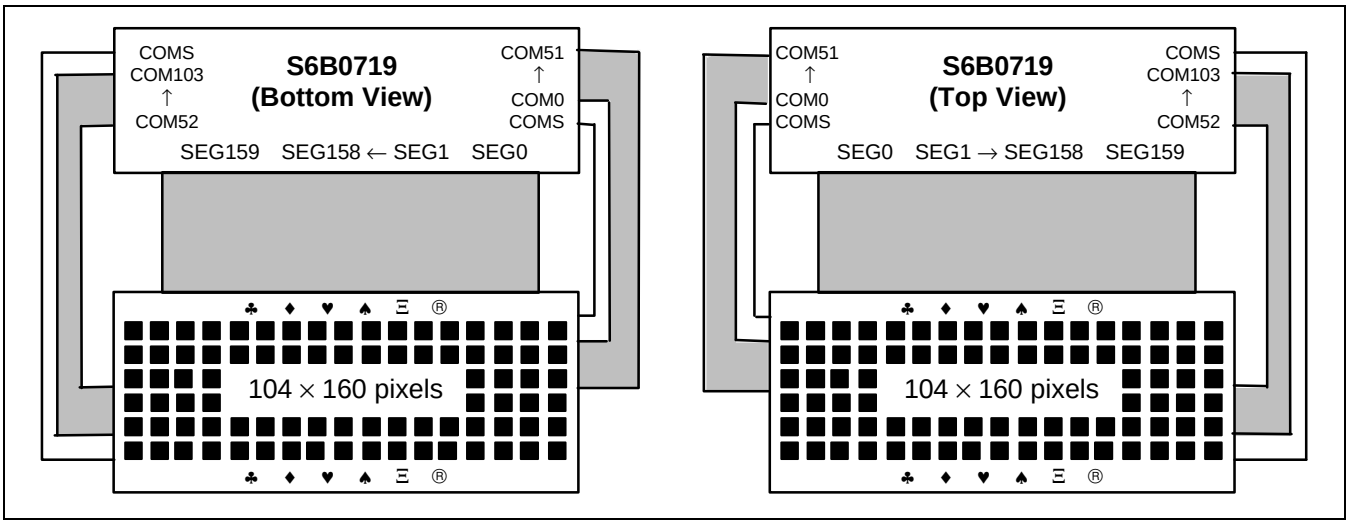


Figure 46. SHL = 0, ADC = 0

Figure 47. SHL = 0, ADC = 1

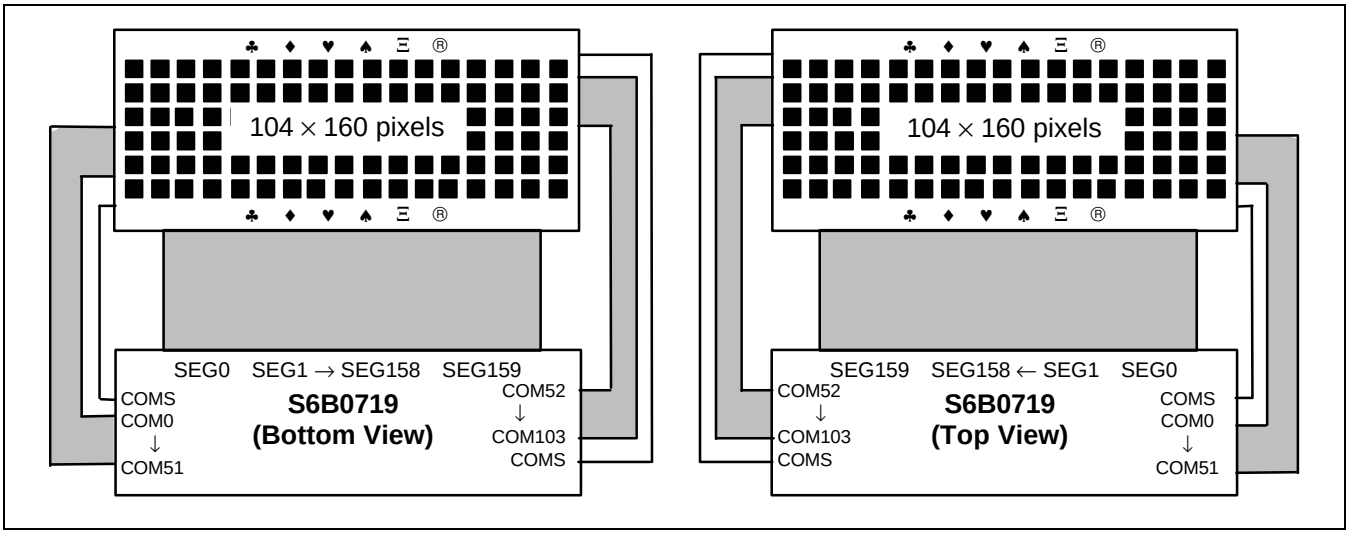


Figure 48. SHL = 1, ADC = 0

Figure 49. SHL = 1, ADC = 1

SAMSUNG ELECTRONICS

Multiple Chip Configuration

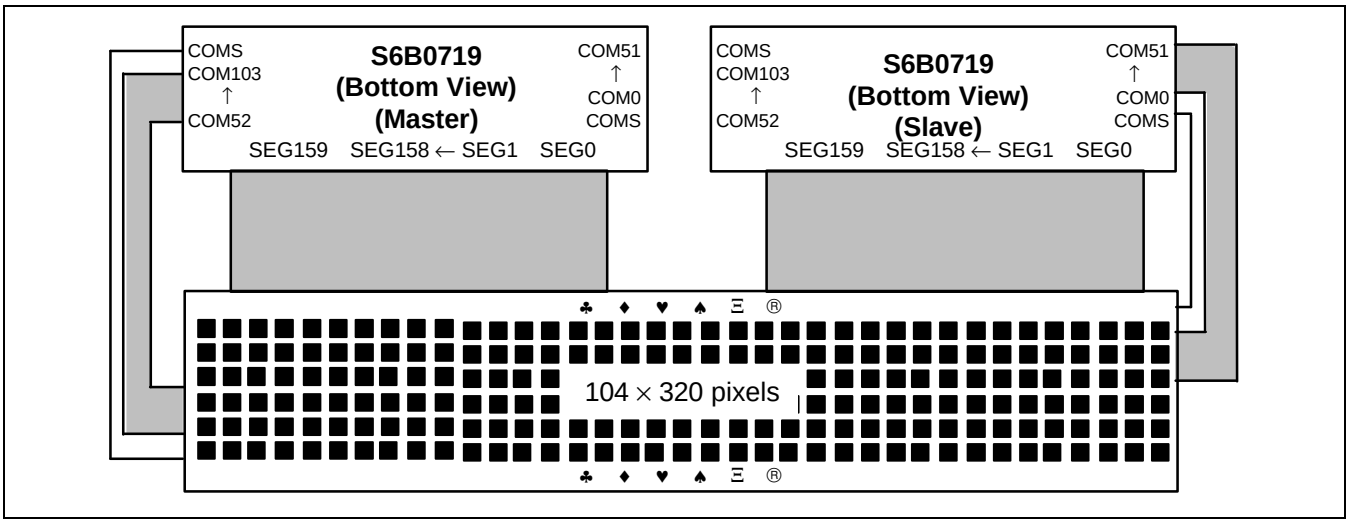


Figure 50. SHL = 0, ADC = 1

♦ Connect the following pins of two chips each other:
- Display clock pins: CL, M, SYNC
- LCD power pins: V0, V1, V2, V3, V4

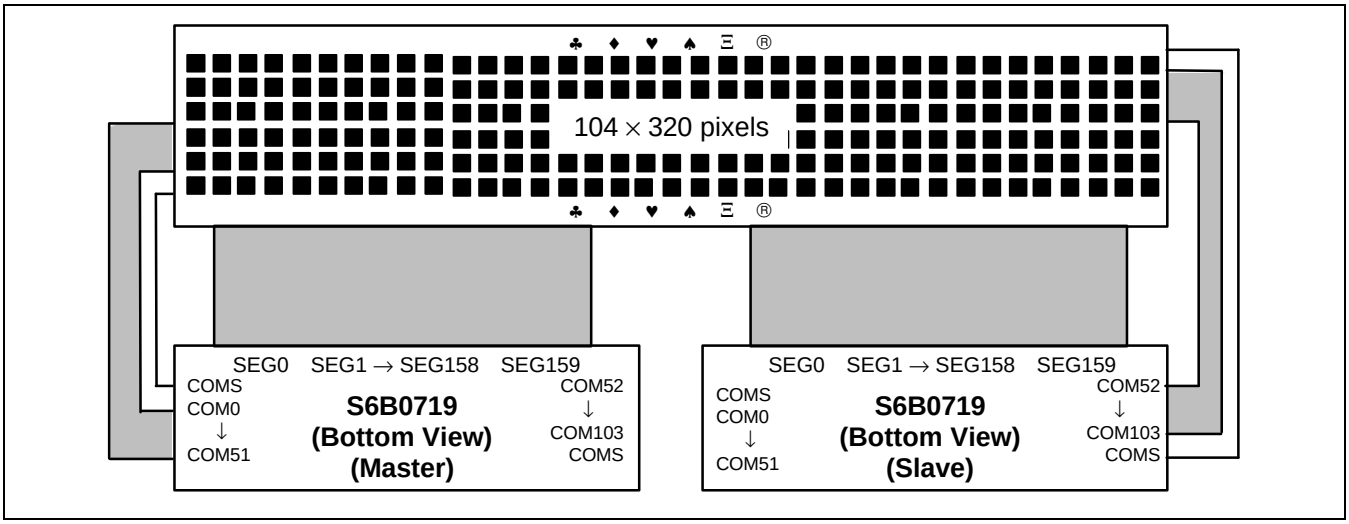


Figure 51. SHL = 1, ADC = 0

♦ Connect the following pins of two chips each other:
- Display clock pins: CL, M, SYNC
- LCD power pins: V0, V1, V2, V3, V4