ST8016S

COM/SEG LCD Driver

Datasheet

Version 0.24

2009/10/01

Note: This is not a final specification.
Some parameters are subject to change.

Sitronix Technology Corporation

1. FEATURES

- Number of LCD drive outputs: 160
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

(Segment mode)
- Shift clock frequency

- 20 MHz (MAX.): V_{DD} = +5.0 ± 0.5 V
- 15 MHz (MAX.): V_{DD} = +3.0 to + 4.5 V
- 12 MHz (MAX.): V_{DD} = +2.5 to + 3.0 V

- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 160 bits of input data
- Line latch circuits are reset when /DISPOFF active

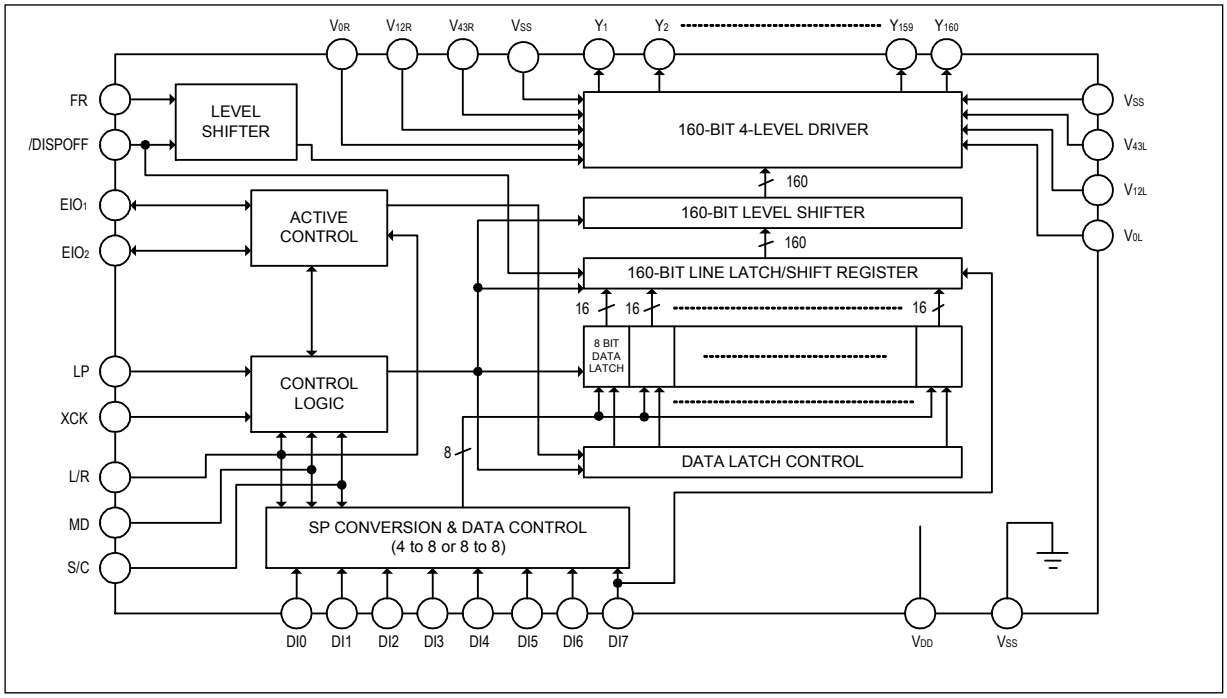
(Common mode)
- Shift clock frequency: 4 MHz (MAX.)
- Built-in 160-bit bi-directional shift register (divisible into 80 bits x 2)
- Available in a single mode (160-bit shift register) or in a dual mode (80-bit shift register x 2)
  - Y_1->Y_{160} Single mode
  - Y_{160}->Y_1 Single mode
  - Y_1->Y_{80}, Y_{81}->Y_{160} Dual mode
  - Y_{160}->Y_{81}, Y_{80}->Y_1 Dual mode

  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when /DISPOFF active

2. DESCRIPTION

The ST8016S is a 160-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. The ST8016S is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3. BLOCK DIAGRAM



4. FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 160 bits of data are read in 20 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 160 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12}, V_{43} or V_{SS}) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 160 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

5. INPUT/OUTPUT CIRCUITS

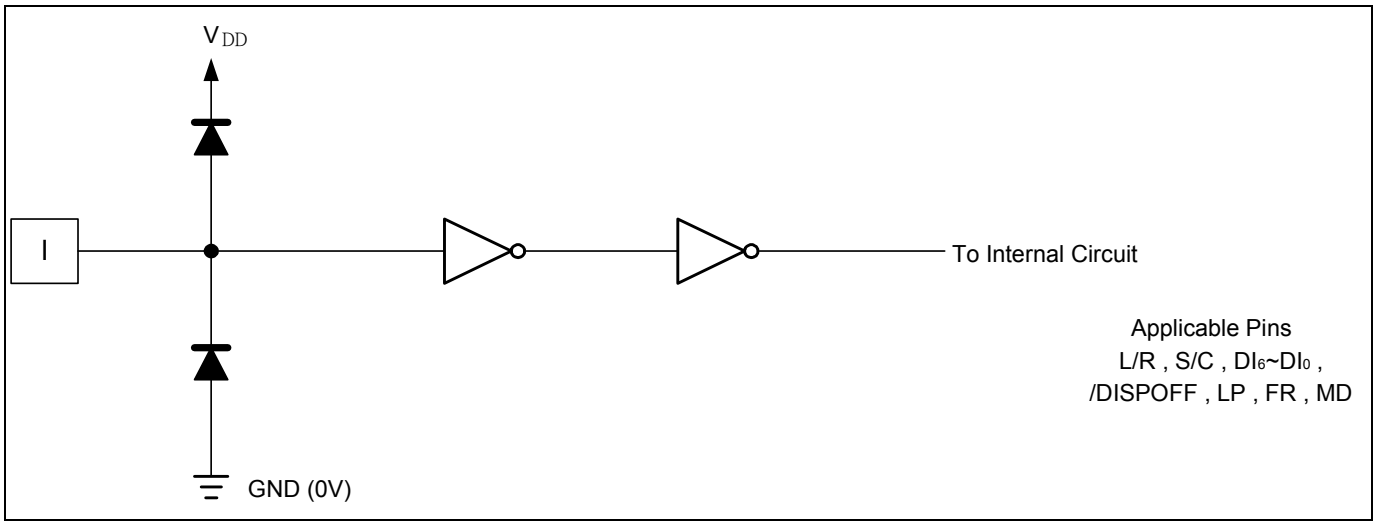


Figure 1 Input Circuit (1)

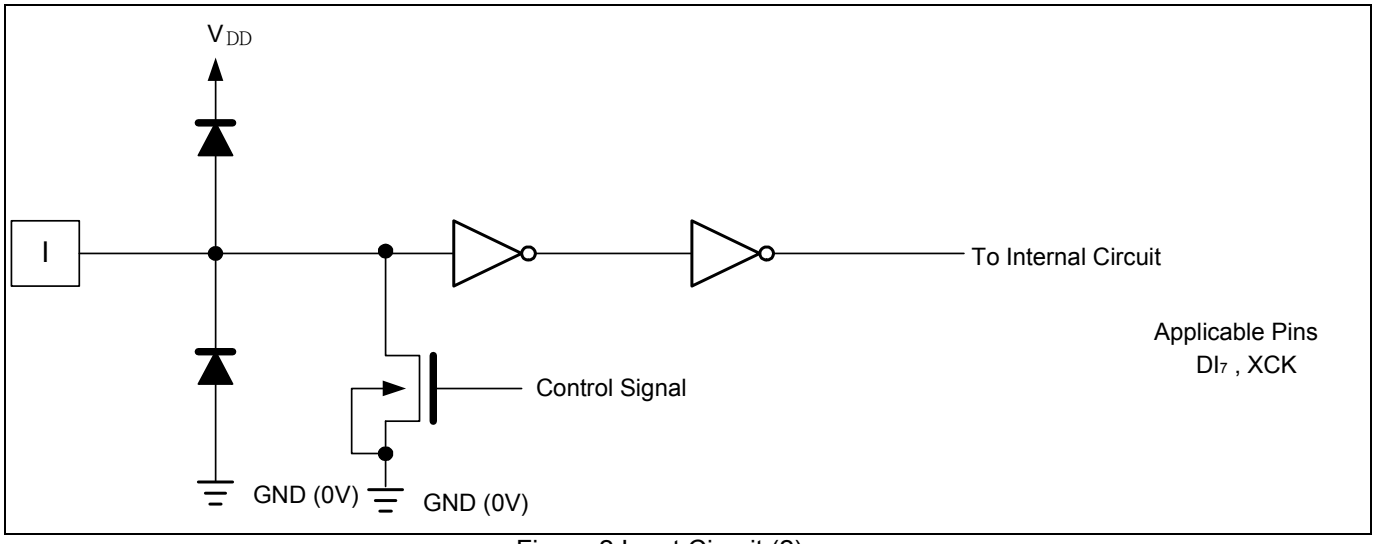


Figure 2 Input Circuit (2)

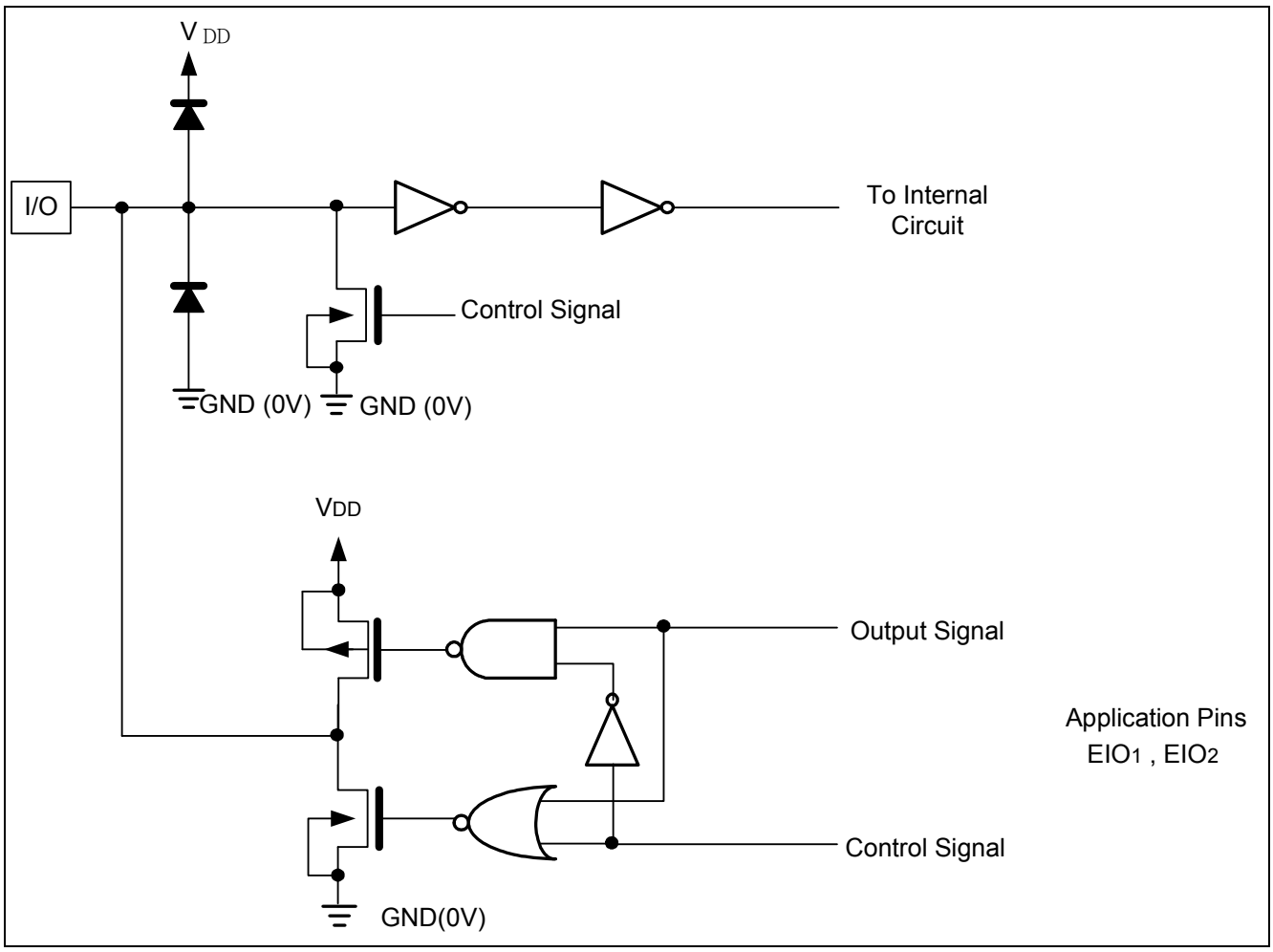


Figure 3 Input/Output Circuit

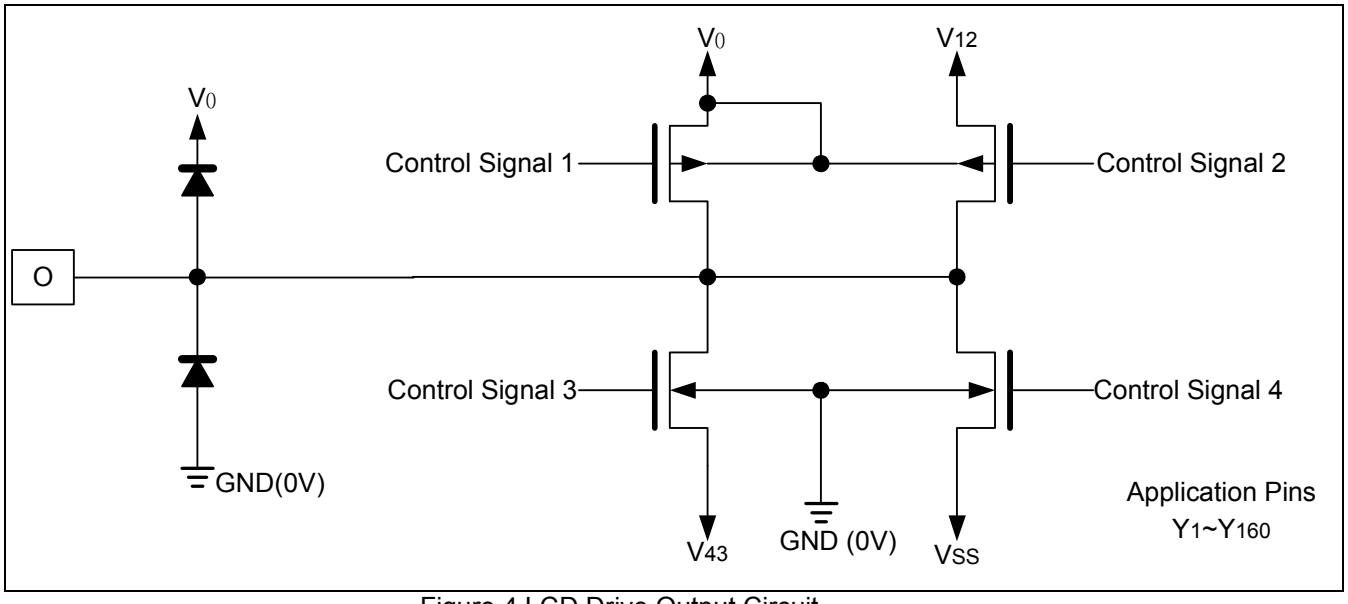


Figure 4 LCD Drive Output Circuit

6. FUNCTIONAL DESCRIPTION

6.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin • Connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic system power ground pin • Do not short LGND with GND and Vss by ITO on LCD panel • Connect it to GND on PCB or FPC.
V_{SS}	Connect to GND by ITO on LCD panel.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI_7-DI_0	Input pins for display data • In 4-bit parallel mode, DI_3-DI_0 are the display data input pins, and DI_7-DI_4 must be connected to LGND or V_{DD}. • In 8-bit parallel mode, All DI_7-DI_0 pins are the display data input pins. • Refer to section 6.2.2.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to LGND level "L", data is read sequentially from Y_{160} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{160}. • Refer to section 6.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it cannot output the reading data correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", 4-bit parallel input mode is set. • When set to V_{DD} level "H", 8-bit parallel input mode is set. • Refer to section 6.2.2.
S/C	Segment mode/common mode selection pin • When set to V_{DD} level "H", segment mode is set.
EIO_1, EIO_2	Input/output pins for chip selection • When L/R input is at LGND level "L", EIO_1 is set for output, and EIO_2 is set for input.

	• When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. • During output, set to "H" while LP • $\overline{XCK}$ is "H" and after 160 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 160 bits of data have been read.
Y_1 -Y_{160}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12} or V_{43}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin • Connected to +2.5 to +5.5 V.
GND	Ground pin
LGND	Logic system power ground pin • Do not short LGND with GND and Vss by ITO on LCD panel • Connect it to GND on PCB or FPC.
V_{SS}	Connect to GND by ITO on LCD panel.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage that is assigned by specification for each power pin.
EIO_1	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at LGND level "L', input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to section 6.2.2.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at LGND level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to section 6.2.2.
LP	Shift clock pulse input pin for bi-directional shift register • * Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{160} to Y_1 when set to LGND level "L", and data is shifted from Y_1 to Y_{160} when set to V_{DD} level "H". • Refer to section 6.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y_1-Y_{160}) are set to level Vss. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

MD	Mode selection pin • When set to LGND level "L", single mode operation is selected; when set to V_{DD} level "H" dual mode operation is selected. • Refer to section 6.2.2.
DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 81st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down(Connect to LGND or V_{DD}, avoiding floating.). • Refer to section 6.2.2.
S/C	Segment mode/common mode selection pin • When set to LGND level "L", common mode is set.
DI_6-DI_0	Not used • Connect DI_6-DI_0 to LGND or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to LGND or open.
Y_1 -Y_{160}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_{SS}) is selected and output. • Table of truth-values is shown in "TRUTH TABLE" in Functional Operations.

6.2 Functional Operations

6.2.1 Truth table

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V_{43}
L	H	H	V_{SS}
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y160)
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_{SS}
X	X	L	V_{SS}

NOTES:

- $V_{SS} < V_{43} < V_{12} < V_0$
- L : LGND (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage that is assigned by specification for each power pin.

6.2.2 Relationship between the display data and LCD drive output Pins

(Segment Mode)

(a) 4-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					40 CLOCK	39 CLOCK	38 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_5	Y_9	…	Y_{149}	Y_{153}	Y_{157}
				DI_1	Y_2	Y_6	Y_{10}	…	Y_{150}	Y_{154}	Y_{158}
				DI_2	Y_3	Y_7	Y_{11}	…	Y_{151}	Y_{155}	Y_{159}
				DI_3	Y_4	Y_8	Y_{12}	…	Y_{152}	Y_{156}	Y_{160}
L	H	Input	Output	DI_0	Y_{160}	Y_{156}	Y_{152}	…	Y_{12}	Y_8	Y_4
				DI_1	Y_{159}	Y_{155}	Y_{151}	…	Y_{11}	Y_7	Y_3
				DI_2	Y_{158}	Y_{154}	Y_{150}	…	Y_{10}	Y_6	Y_2
				DI_3	Y_{157}	Y_{153}	Y_{149}	…	Y_9	Y_5	Y_1

(b) 8-bit Parallel Input Mode

MD	L/R	EIO_1	EIO_2	DATA INPUT	NUMBER OF CLOCKS						
					20 CLOCK	19 CLOCK	18 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	…	Y_{137}	Y_{145}	Y_{153}
				DI_1	Y_2	Y_{10}	Y_{18}	…	Y_{138}	Y_{146}	Y_{154}
				DI_2	Y_3	Y_{11}	Y_{19}	…	Y_{139}	Y_{147}	Y_{155}
				DI_3	Y_4	Y_{12}	Y_{20}	…	Y_{140}	Y_{148}	Y_{156}
				DI_4	Y_5	Y_{13}	Y_{21}		Y_{141}	Y_{149}	Y_{157}
				DI_5	Y_6	Y_{14}	Y_{22}		Y_{142}	Y_{150}	Y_{158}
				DI_6	Y_7	Y_{15}	Y_{23}		Y_{143}	Y_{151}	Y_{159}
				DI_7	Y_8	Y_{16}	Y_{24}		Y_{144}	Y_{152}	Y_{160}
H	H	Input	Output	DI_0	Y_{160}	Y_{152}	Y_{144}	…	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{159}	Y_{151}	Y_{143}	…	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{158}	Y_{150}	Y_{142}	…	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{157}	Y_{149}	Y_{141}	…	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{156}	Y_{148}	Y_{140}	…	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{155}	Y_{147}	Y_{139}	…	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{154}	Y_{146}	Y_{138}	…	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{153}	Y_{145}	Y_{137}	…	Y_{17}	Y_9	Y_1

(Common Mode)

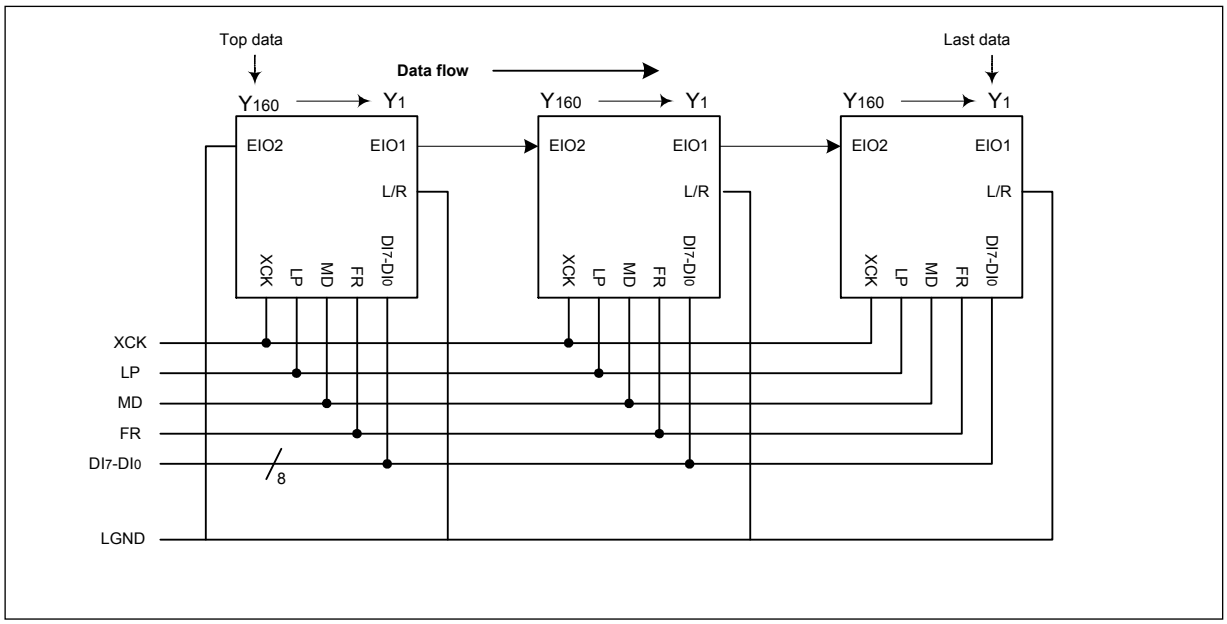
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	EIO_2	DI_7
L (Single)	L	$Y_{160} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{160}$	Input	Output	X
H (Dual)	L	$Y_{160} \rightarrow Y_{81}$ $Y_{80} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{80}$ $Y_{81} \rightarrow Y_{160}$	Input	Output	Input

NOTES:

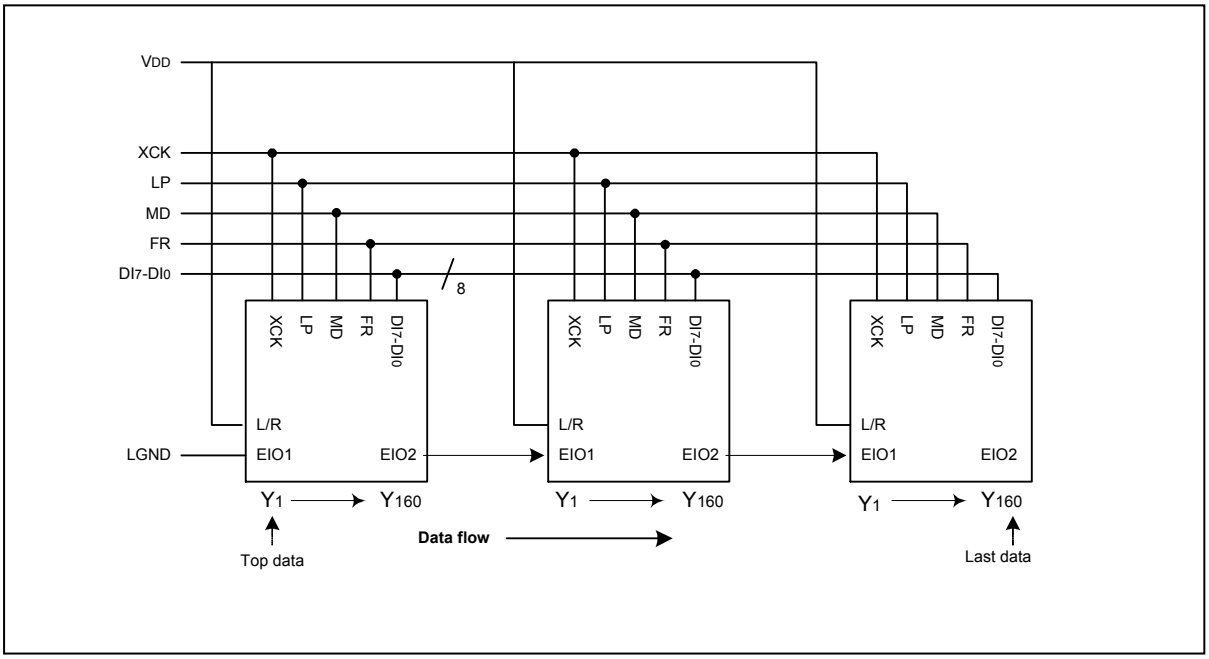
- L : LGND (0 V), H : V_{DD} (+2.5 to +5.5 V), X : Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

6.2.3 Connection examples of plural segment drivers

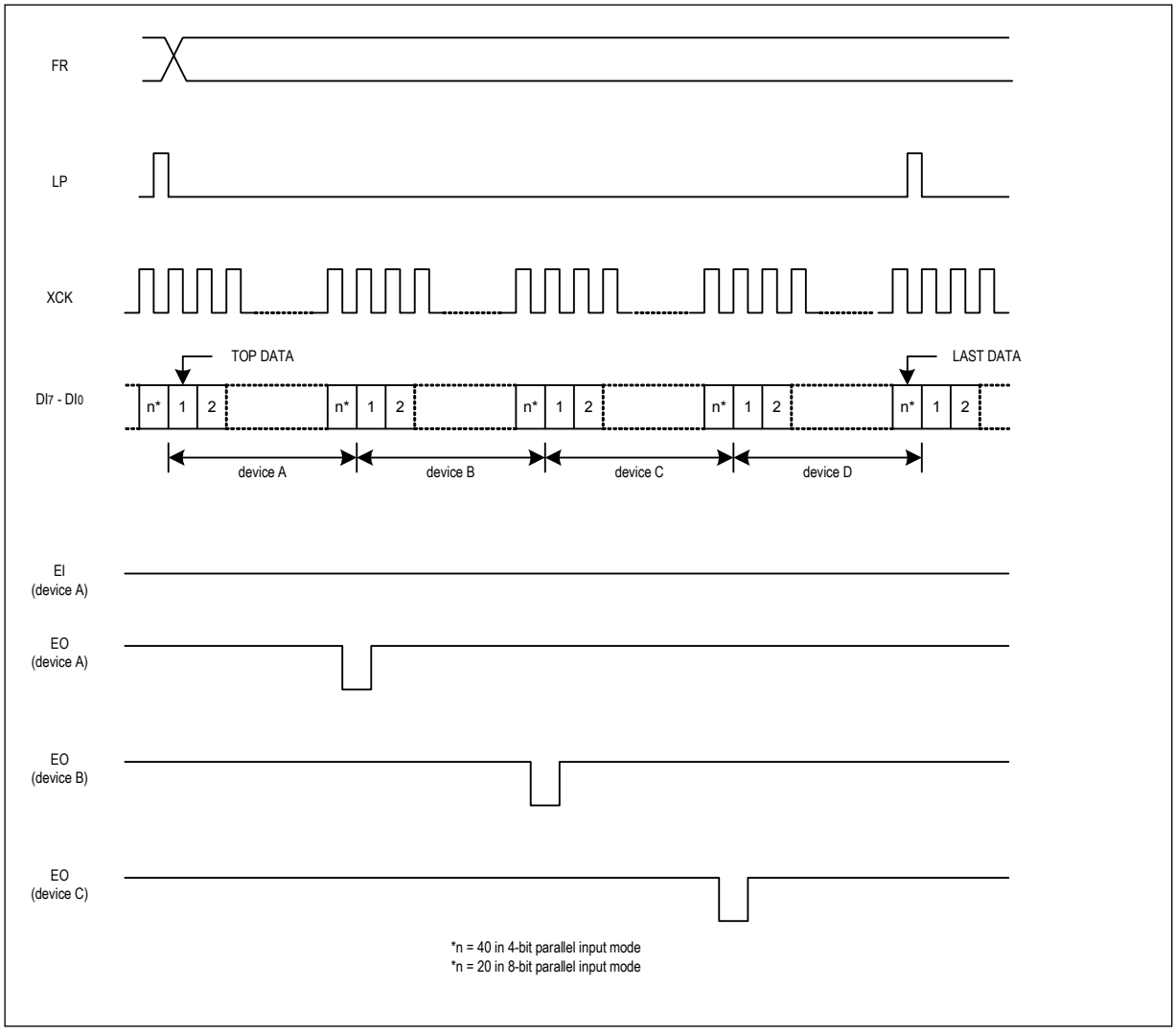
(a) When L/R = "L"



(b) When L/R = "H"

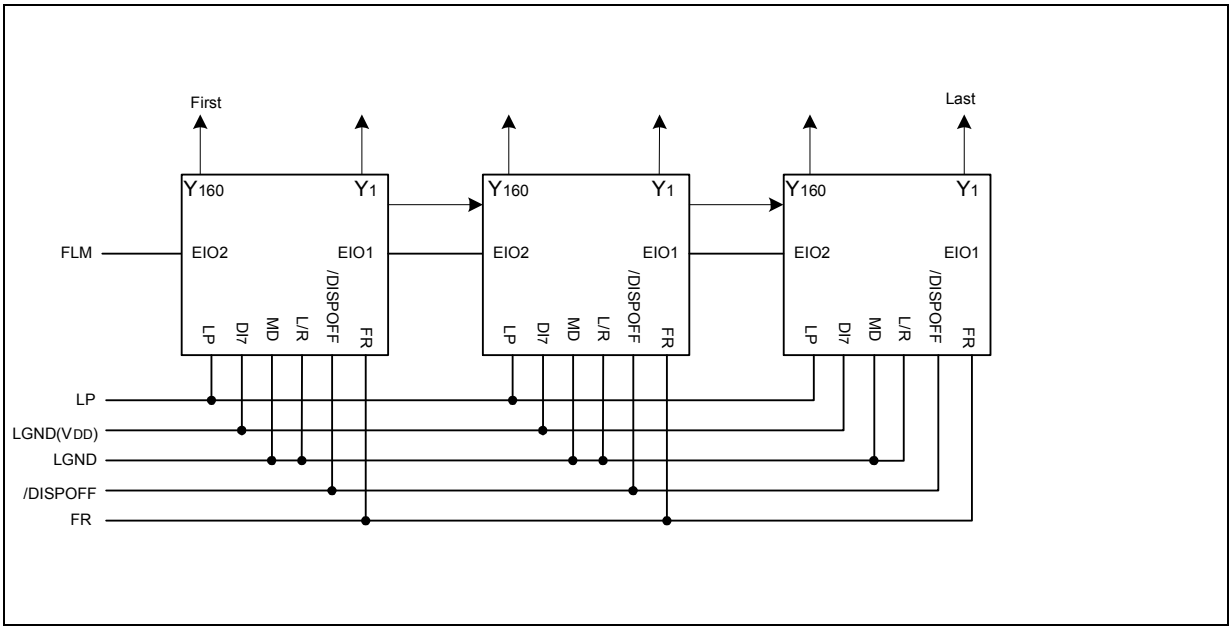


6.2.4 Timing chart of 4-device cascade connection of segment drivers

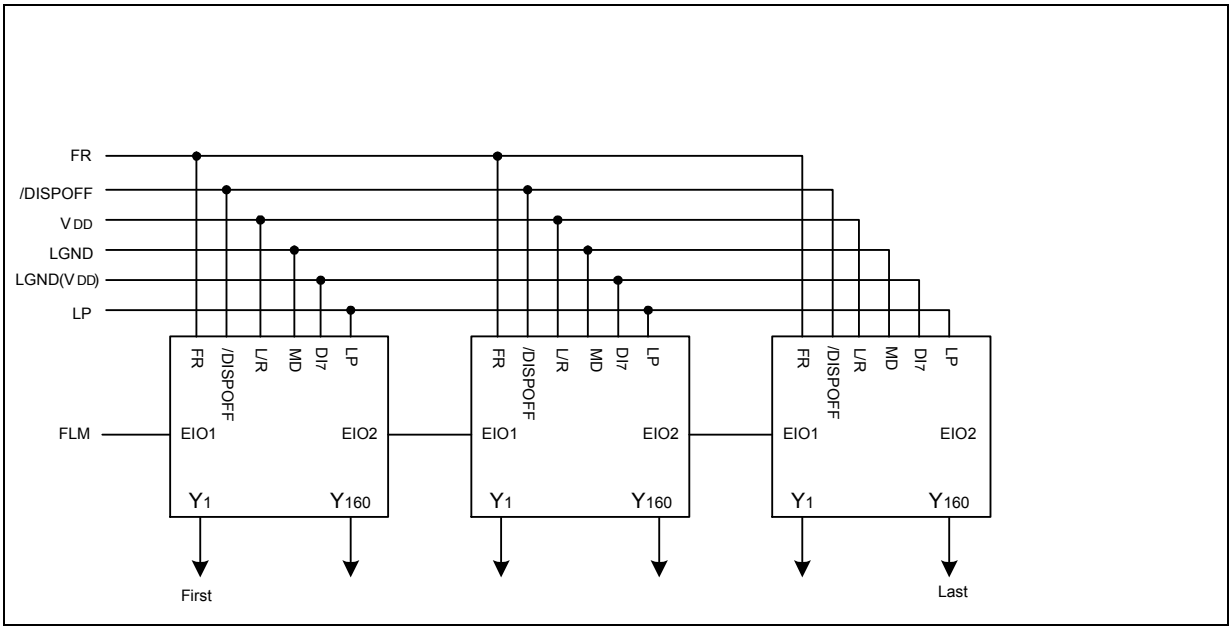


6.2.5 Connection examples for plural common drivers

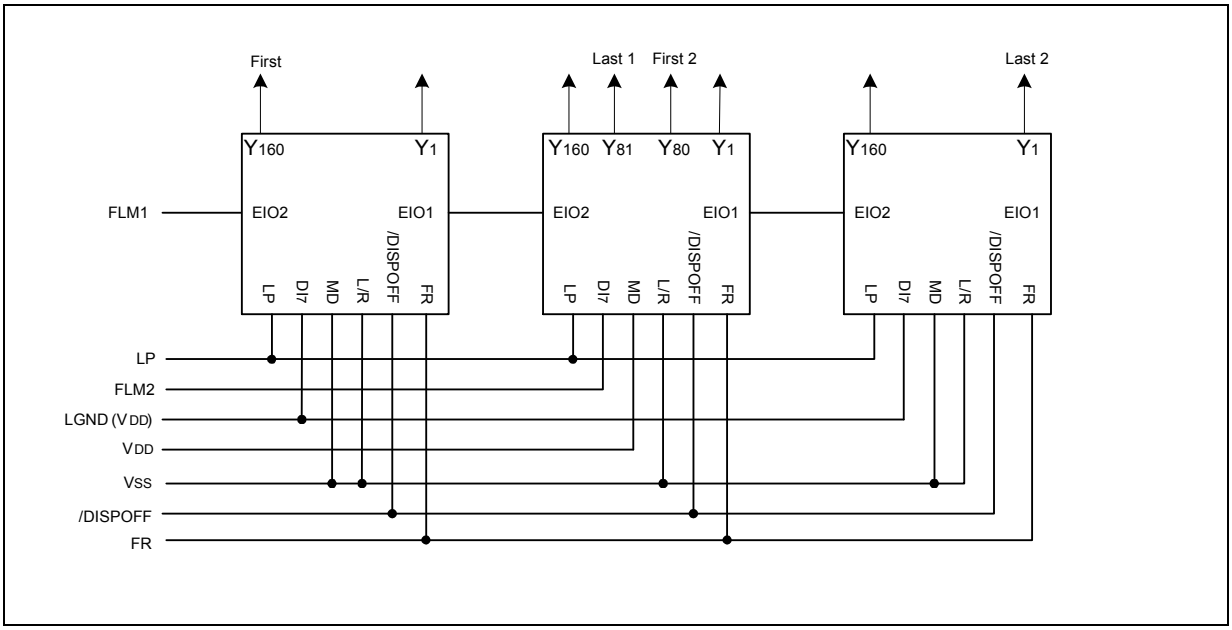
(a) Single Mode (L/R = "L")



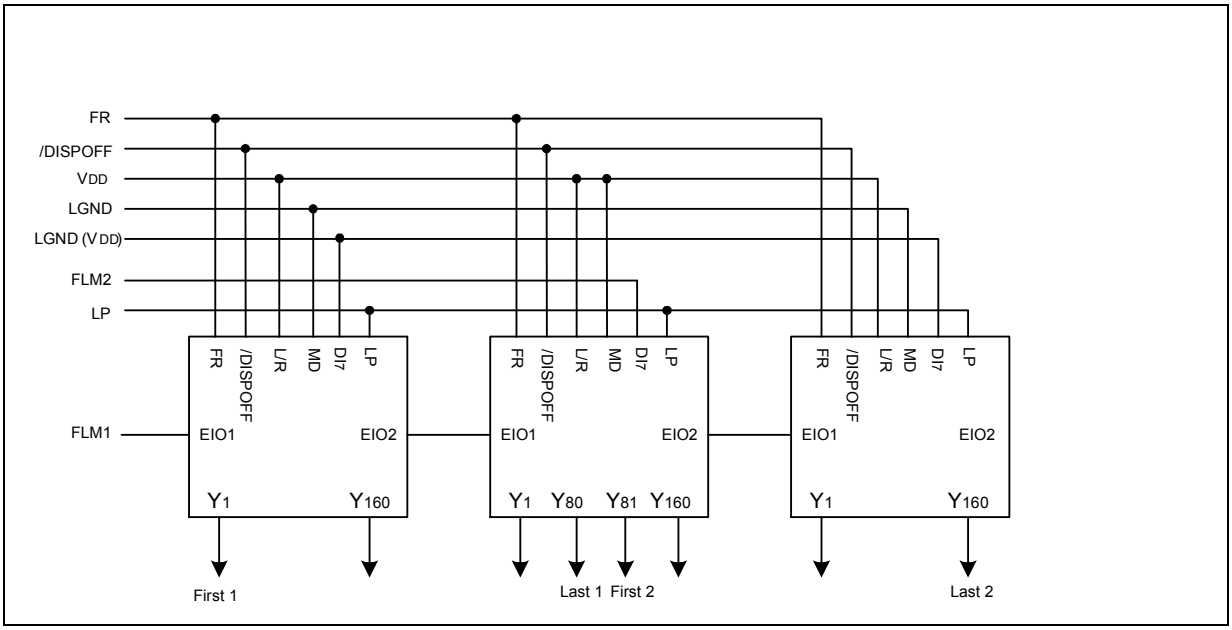
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual mode (L/R = "H")



7. PRECAUTIONS

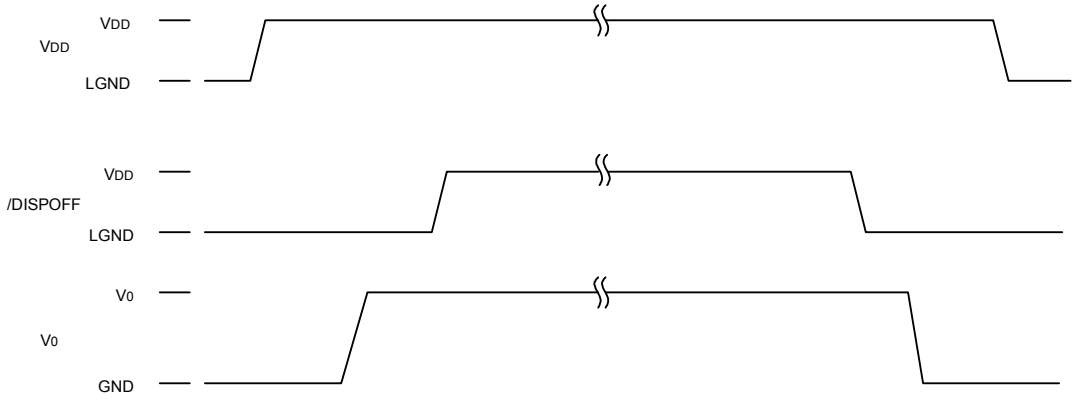
Precautions when connecting or disconnecting the power supply

This IC has a high-voltage LCD driver, so a high current that may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating may permanently damage it. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (4.7Ω to 50Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level LGND on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.

When connecting the power supply, follow the recommended sequence shown here



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8. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3~ +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 ~ +33.0	V	
	V_{12}	V_{12L}, V_{12R}	V_0 -10~ V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 ~ V_{SS} + 10	V	
Input voltage	V_I	$D1_7$-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF	-0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:
1. TA = +25 °C
2. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
3. Stress over the “Absolute Max. Ratings” conditions will damage the device permanently.

9. RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+30.0	V	
Operating temperature	T_{OPR}		-25		+85	°C	

NOTES:
1. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{I2} < V_0$.

10. ELECTRICAL CHARACTERISTICS

10.1 DC Characteristics

(Segment Mode) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{0L}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{0H}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = LGND	DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10	µA	
	I_{LIH}	V_I = V_{DD}				+10	µA	
Output resistance	R_{ON}	|ΔVON| =0.5V, V_0 = 30 V	Y_1-Y_{160}		1.0	1.5	kΩ	
Standby current	I_{STB}		LGND			50	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			7.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			0.9	mA	4

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, Vi = LGND.
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8 MHz, no-load, EI = LGND. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 8MHz, f_{LP} = 19.2 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABL E PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI7-DI0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}			V	
Output "Low" voltage	V_{0L}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{0H}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = LGND	DI7-DI0, XCK, LP, LIR, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	µA	
	I_{LIH}	V_I = V_{DD}	DI6-DI0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	µA	
Input pull-down current	I_{PD}	V_I = V_{DD}	DI7, XCK, EIO_1, EIO_2			100	µA	
Output resistance	R_{ON}	|ΔVON| =0.5V, V_0 = 30 V	Y_1-Y_{160}		1.0	1.5	kΩ	
Standby current	I_{SPD}		LGND			50	µA	1
Supply current (1)	I_{DD}		V_{DD}			80	µA	2
Supply current (2)	I_0		V_{0L}, V_{0R}			130	µA	2

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, V_I = LGND
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{LP} =19.2 kHz, f_{FR} = 80 Hz, 1/240 duty operation, no-load.

10.2 AC Characteristics

(Segment Mode 1) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +3.0 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 11ns	125			ns	1
Shift clock "H" pulse width	t_{WCKH}		51			ns	
Shift clock "L" pulse width	t_{WCKL}		51			ns	
Data setup time	t_{DS}		30			ns	
Data hold time	t_{DH}		40			ns	
Latch pulse "H" pulse width	t_{WLPH}		51			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		51			ns	
Latch pulse fall to shift clock fall time	t_{LH}		51			ns	
Enable setup time	t_S		36			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			78	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (LGND =V_{SS} = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (LGND =V_{SS} = 0 V, V_{DD} = +3.0 to +4.5 V, V_0 = + 15.0 to +30.0 V, T_{OPR} = -25 10+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		51			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
DISPOFF removal time	t_{SD}		100			ns	
DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

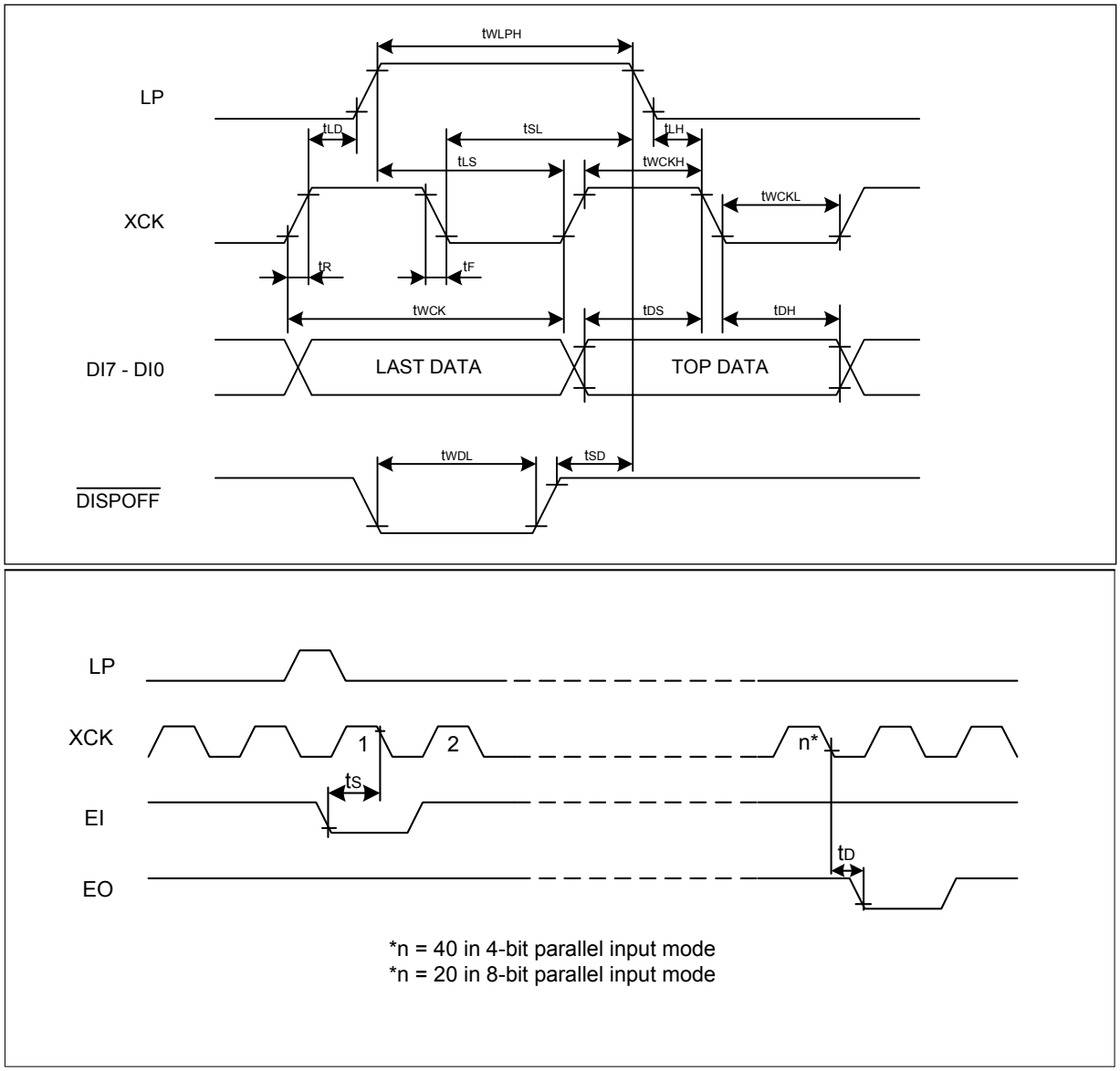
NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (LGND =V_{SS} = 0 V, V_{DD} = +2.5 to +5.5 V, V_0 = +15.0 to +30.0 V, T_{OPR} = -25 to +85° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
DISPOFF removal time	t_{SD}		100			ns
DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs

10.3 Timing Chart of Segment Mode



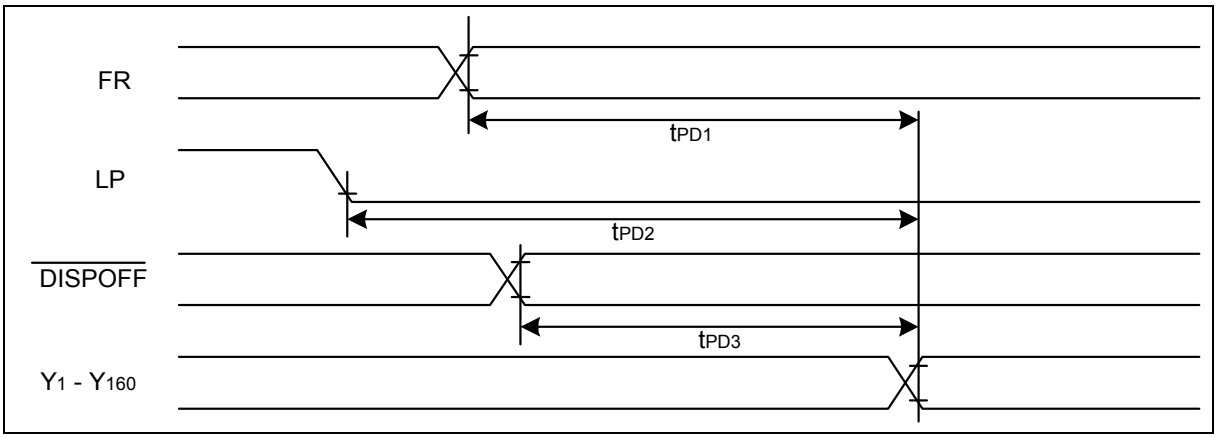
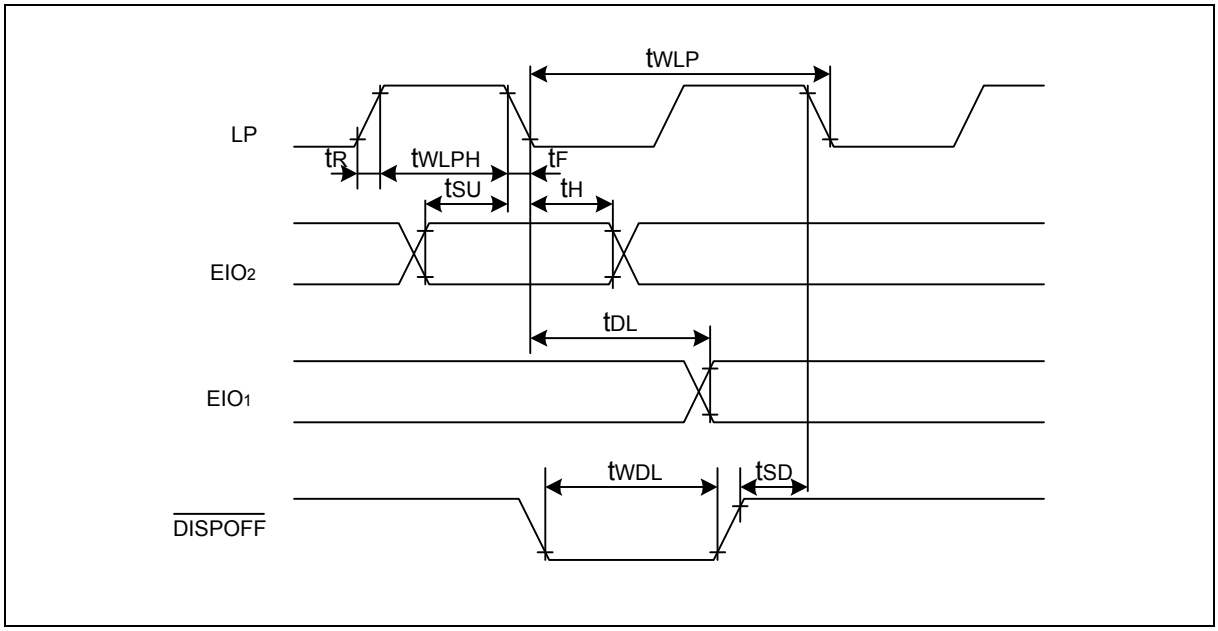
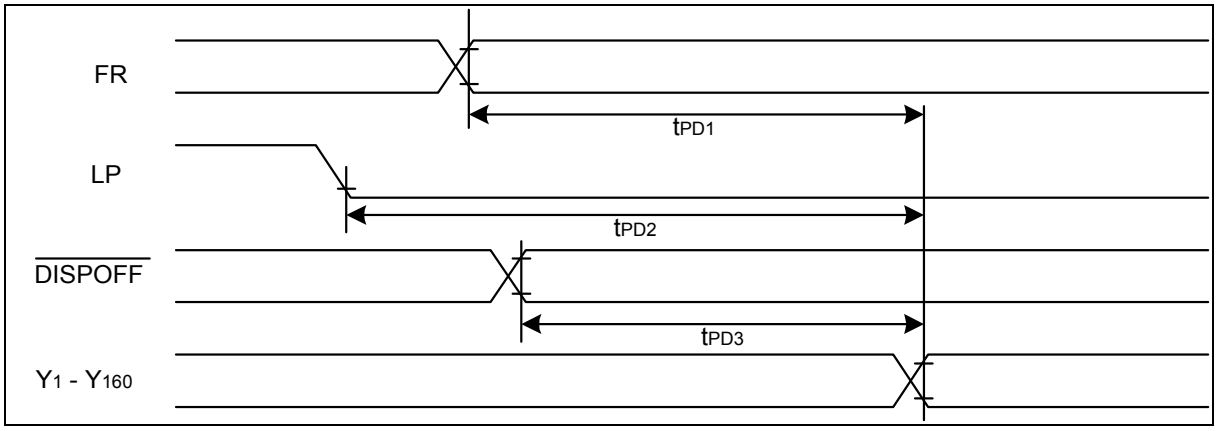


Fig. 8 Timing Characteristics (3)

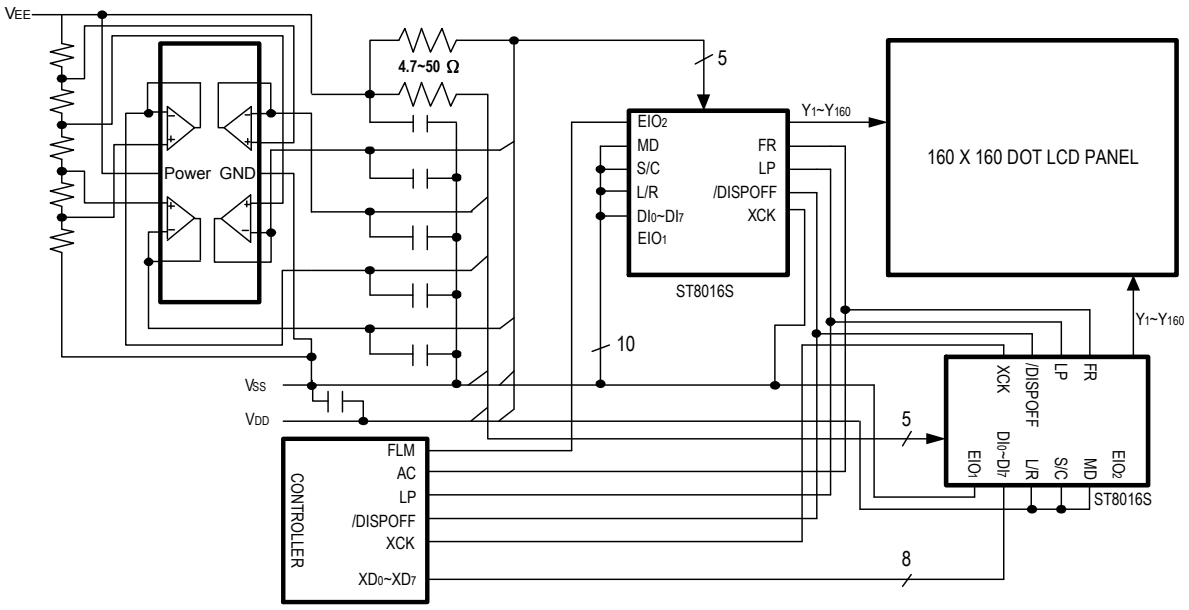
10.4 Timing Chart of Common Mode



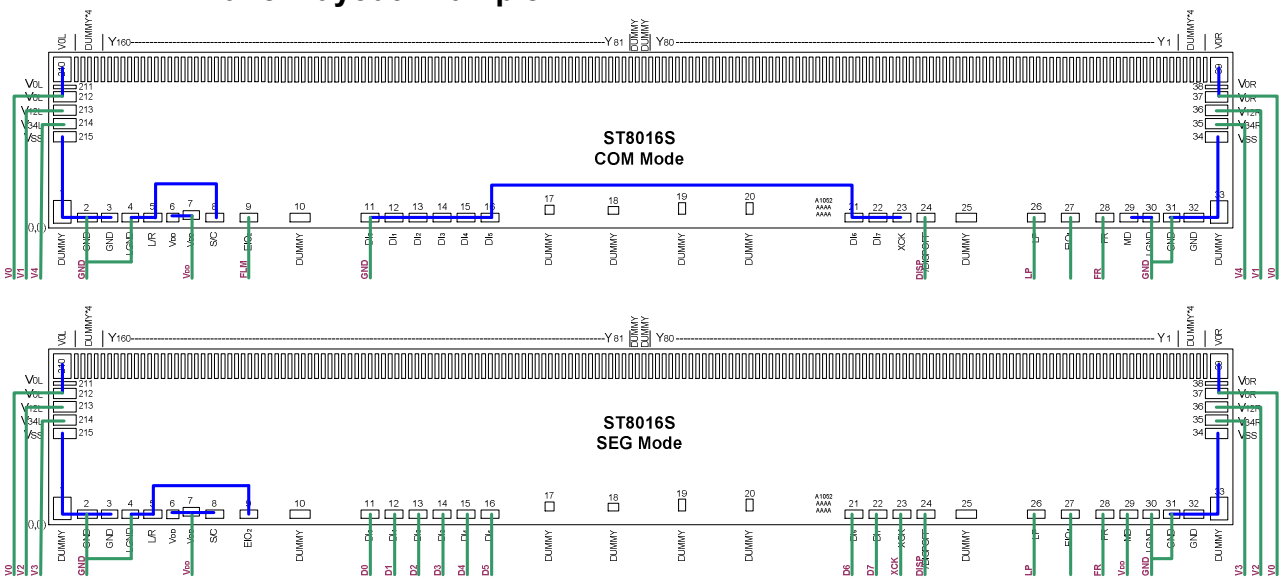


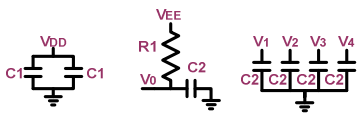
11. APPLICATION CIRCUIT

11.1 Application Circuit for Module



11.2 LCD Panel Layout Example





R1 : 4.7Ω ~ 50Ω
C1 : 0.1uF ~ 4.7uF
C2 : 0.1uF ~ 4.7uF
Circuit on PCB
Circuit on LCD

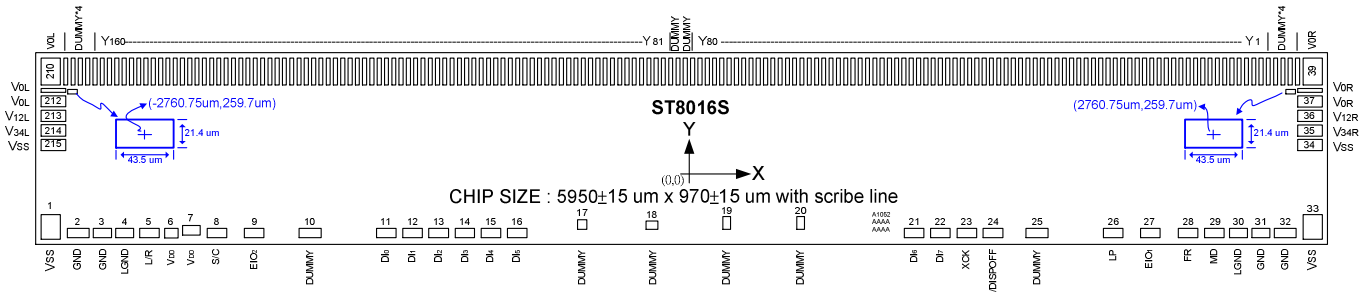
ITO layout Notices (for reference only)

1. We suggest the ITO resistor for LCD panel is about 15Ω/Square, and the resistor value is as smaller as better.
2. Among the interface pins, please to be sure the ITO resistor value of power pins are less than the following values that we suggest.

Pin Name	ITO Resistor Values Suggestion
LGND, GND, VDD, Vss	Less than 75Ω when VDD ≧ 3.0V, and the smaller the better
V0R, V0L	Less than 150Ω, and the smaller the better
V12R, V12L, V34R, V12L	Less than 250Ω, and the smaller the better

PS : Above resistor value test on 3” LCD panel.

12. PAD DIAGRAM



Note: Subtrate should be connected to GND.

Unit: um

PIN#	Name	X	Y	PIN#	Name	X	Y
1	V_{SS}	-2857.500	-355.000	34	V_{SS}	2845.000	16.500
2	GND	-2733.000	-383.100	35	V_{34R}	2845.000	82.500
3	GND	-2622.850	-383.150	36	V_{12R}	2845.000	148.500
4	LGND	-2521.550	-383.150	37	V_{0R}	2845.000	214.500
5	L/R	-2410.100	-383.100	38	V_{0R}	2845.000	264.000
6	V_{DD}	-2310.675	-383.350	39	V_{0R}	2857.500	350.000
7	V_{DD}	-2220.450	-370.650	40	DUMMY	2788.700	350.000
8	S/C	-2103.600	-383.100	41	DUMMY	2755.700	350.000
9	EIO_2	-1935.850	-383.100	42	DUMMY	2722.700	350.000
10	DUMMY	-1682.850	-383.100	43	DUMMY	2689.700	350.000
11	DI_0	-1337.575	-383.100	44	Y_1	2656.700	350.000
12	DI_1	-1218.950	-383.100	45	Y_2	2623.700	350.000
13	DI_2	-1100.250	-383.100	46	Y_3	2590.700	350.000
14	DI_3	-981.550	-383.100	47	Y_4	2557.700	350.000
15	DI_4	-862.850	-383.100	48	Y_5	2524.700	350.000
16	DI_5	-744.150	-383.100	49	Y_6	2491.700	350.000
17	DUMMY	-450.500	-344.400	50	Y_7	2458.700	350.000
18	DUMMY	-134.775	-347.675	51	Y_8	2425.700	350.000
19	DUMMY	204.125	-337.725	52	Y_9	2392.700	350.000
20	DUMMY	538.725	-337.725	53	Y_{10}	2359.700	350.000
21	DI_6	1053.350	-383.100	54	Y_{11}	2326.700	350.000
22	DI_7	1172.050	-383.100	55	Y_{12}	2293.700	350.000
23	XCK	1291.050	-383.100	56	Y_{13}	2260.700	350.000
24	/DISPOFF	1409.750	-383.100	57	Y_{14}	2227.700	350.000
25	DUMMY	1608.650	-383.100	58	Y_{15}	2194.700	350.000
26	LP	1953.925	-383.100	59	Y_{16}	2161.700	350.000
27	EIO_1	2121.600	-383.100	60	Y_{17}	2128.700	350.000
28	FR	2293.000	-383.100	61	Y_{18}	2095.700	350.000
29	MD	2411.700	-383.100	62	Y_{19}	2062.700	350.000
30	LGND	2521.550	-383.150	63	Y_{20}	2029.700	350.000
31	GND	2622.850	-383.150	64	Y_{21}	1996.700	350.000
32	GND	2733.000	-383.100	65	Y_{22}	1963.700	350.000
33	V_{SS}	2857.500	-355.000	66	Y_{23}	1930.700	350.000

67	Y24	1897.700	350.000	114	Y71	346.700	350.000
68	Y25	1864.700	350.000	115	Y72	313.700	350.000
69	Y26	1831.700	350.000	116	Y73	280.700	350.000
70	Y27	1798.700	350.000	117	Y74	247.700	350.000
71	Y28	1765.700	350.000	118	Y75	214.700	350.000
72	Y29	1732.700	350.000	119	Y76	181.700	350.000
73	Y30	1699.700	350.000	120	Y77	148.700	350.000
74	Y31	1666.700	350.000	121	Y78	115.700	350.000
75	Y32	1633.700	350.000	122	Y79	82.700	350.000
76	Y33	1600.700	350.000	123	Y80	49.700	350.000
77	Y34	1567.700	350.000	124	DUMMY	16.700	350.000
78	Y35	1534.700	350.000	125	DUMMY	-16.700	350.000
79	Y36	1501.700	350.000	126	Y81	-49.700	350.000
80	Y37	1468.700	350.000	127	Y82	-82.700	350.000
81	Y38	1435.700	350.000	128	Y83	-115.700	350.000
82	Y39	1402.700	350.000	129	Y84	-148.700	350.000
83	Y40	1369.700	350.000	130	Y85	-181.700	350.000
84	Y41	1336.700	350.000	131	Y86	-214.700	350.000
85	Y42	1303.700	350.000	132	Y87	-247.700	350.000
86	Y43	1270.700	350.000	133	Y88	-280.700	350.000
87	Y44	1237.700	350.000	134	Y89	-313.700	350.000
88	Y45	1204.700	350.000	135	Y90	-346.700	350.000
89	Y46	1171.700	350.000	136	Y91	-379.700	350.000
90	Y47	1138.700	350.000	137	Y92	-412.700	350.000
91	Y48	1105.700	350.000	138	Y93	-445.700	350.000
92	Y49	1072.700	350.000	139	Y94	-478.700	350.000
93	Y50	1039.700	350.000	140	Y95	-511.700	350.000
94	Y51	1006.700	350.000	141	Y96	-544.700	350.000
95	Y52	973.700	350.000	142	Y97	-577.700	350.000
96	Y53	940.700	350.000	143	Y98	-610.700	350.000
97	Y54	907.700	350.000	144	Y99	-643.700	350.000
98	Y55	874.700	350.000	145	Y100	-676.700	350.000
99	Y56	841.700	350.000	146	Y101	-709.700	350.000
100	Y57	808.700	350.000	147	Y102	-742.700	350.000
101	Y58	775.700	350.000	148	Y103	-775.700	350.000
102	Y59	742.700	350.000	149	Y104	-808.700	350.000
103	Y60	709.700	350.000	150	Y105	-841.700	350.000
104	Y61	676.700	350.000	151	Y106	-874.700	350.000
105	Y62	643.700	350.000	152	Y107	-907.700	350.000
106	Y63	610.700	350.000	153	Y108	-940.700	350.000
107	Y64	577.700	350.000	154	Y109	-973.700	350.000
108	Y65	544.700	350.000	155	Y110	-1006.700	350.000
109	Y66	511.700	350.000	156	Y111	-1039.700	350.000
110	Y67	478.700	350.000	157	Y112	-1072.700	350.000
111	Y68	445.700	350.000	158	Y113	-1105.700	350.000
112	Y69	412.700	350.000	159	Y114	-1138.700	350.000
113	Y70	379.700	350.000	160	Y115	-1171.700	350.000

161	Y_{116}	-1204.700	350.000	189	Y_{144}	-2128.700	350.000
162	Y_{117}	-1237.700	350.000	190	Y_{145}	-2161.700	350.000
163	Y_{118}	-1270.700	350.000	191	Y_{146}	-2194.700	350.000
164	Y_{119}	-1303.700	350.000	192	Y_{147}	-2227.700	350.000
165	Y_{120}	-1336.700	350.000	193	Y_{148}	-2260.700	350.000
166	Y_{121}	-1369.700	350.000	194	Y_{149}	-2293.700	350.000
167	Y_{122}	-1402.700	350.000	195	Y_{150}	-2326.700	350.000
168	Y_{123}	-1435.700	350.000	196	Y_{151}	-2359.700	350.000
169	Y_{124}	-1468.700	350.000	197	Y_{152}	-2392.700	350.000
170	Y_{125}	-1501.700	350.000	198	Y_{153}	-2425.700	350.000
171	Y_{126}	-1534.700	350.000	199	Y_{154}	-2458.700	350.000
172	Y_{127}	-1567.700	350.000	200	Y_{155}	-2491.700	350.000
173	Y_{128}	-1600.700	350.000	201	Y_{156}	-2524.700	350.000
174	Y_{129}	-1633.700	350.000	202	Y_{157}	-2557.700	350.000
175	Y_{130}	-1666.700	350.000	203	Y_{158}	-2590.700	350.000
176	Y_{131}	-1699.700	350.000	204	Y_{159}	-2623.700	350.000
177	Y_{132}	-1732.700	350.000	205	Y_{160}	-2656.700	350.000
178	Y_{133}	-1765.700	350.000	206	DUMMY	-2689.700	350.000
179	Y_{134}	-1798.700	350.000	207	DUMMY	-2722.700	350.000
180	Y_{135}	-1831.700	350.000	208	DUMMY	-2755.700	350.000
181	Y_{136}	-1864.700	350.000	209	DUMMY	-2788.700	350.000
182	Y_{137}	-1897.700	350.000	210	V_{0L}	-2857.500	350.000
183	Y_{138}	-1930.700	350.000	211	V_{0L}	-2845.000	264.000
184	Y_{139}	-1963.700	350.000	212	V_{0L}	-2845.000	214.500
185	Y_{140}	-1996.700	350.000	213	V_{12L}	-2845.000	148.500
186	Y_{141}	-2029.700	350.000	214	V_{34L}	-2845.000	82.500
187	Y_{142}	-2062.700	350.000	215	V_{SS}	-2845.000	16.500
188	Y_{143}	-2095.700	350.000				

12.1 Gold Bump size (unit: um)

Pad No.	X	Y	Area (um^2)
1,33	87.00	112.00	9744.0000
6	59.75	42.90	2563.2750
7	80.70	42.40	3421.6800
2,32	99.00	42.40	4197.6000
3,4,30,31	81.30	42.30	3438.9900
5,8,9,12~16,21~24,27~29	88.70	42.40	3760.8800
10,25	100.20	42.40	4248.4800
11,26	88.55	42.40	3754.5200
17	43.30	44.40	1922.5200
18	52.85	37.85	2000.3725
19,20	34.65	57.75	2001.0375
40~209	18.00	122.00	2196.0000
38,211	112.00	18.00	2016.0000
39,210	87.00	122.00	10614.0000
34~37,212~215	112.00	51.00	5712.0000

Wafer Thickness = 480.0±20um, Bump pad height (pad 1~215) = 15um, strength=30g

13. APPLICATION NOTE(REFERENCE ONLY)

13.1 Adjust V1 and V4 voltage to keep the V0-V1 = V4-VSS relation to get better display quality. The (V0-V1)-(V4-VSS) value had better less than 100mV.
13.2 Add 0.1uF high frequency by-pass capacitor to filter the noise on V0~V4 to VSS.
13.3 When OP follower circuit is used, please be sure the OP power is higher than V0 at least 1.5V.
13.4 EIO1 and EIO2 is enable pin for driver, please pay attention to the distance to avoid noise when cascade function is used. Two chip connecting distance is as shorter as better.

14. REVISION

REVISION	DESCRIPTION	PAGE	DATE
0.10	First release	1-25	2005/8/4
0.11	Delete TCP information	1-25	2005/9/8
0.12	Add LGND definition, and re-define the pin function	1-25	2005/11/22
0.13	Modify suggestion resistor value for V0 and bond pad height to 18um. Add alignment mark data and LCD Panel Layout Example.	21-22	2006/4/4
0.14	Modify LCD panel layout example S/C of COM to connect to LGND, and add the ITO resistor value suggestion.	21	2006/5/23
0.15	Modify the center of pad coordinate to the IC center.	22-24	2006/5/30
0.16	Modify the Bump pad height and add wafer thickness.	24	2006/6/7
0.17	Modify all Vss for logic setting pins to LGND	21-24	2006/7/21
0.18	Modify Description of LGND	1-25	2006/7/21
0.19	Change Sitronix Logo and Modify description of LGND for COM mode	1-25	2006/7/21
0.20	Modify arrangement	1-25	2006/8/3
0.21	Modify Chip size and thickness with scribe line Modify “ABSOLUTE MAXIMUM RATINGS” max value Modify “Output resistance” test condition	15,22,24	2006/10/26
0.22	Modify all the data about absolute max voltage and recommend max voltage	2,16-18	2007/5/25
0.23	Modify the ITO resistor value suggestion Add application note	21,26	2008/5/05
0.24	Modify LCD Panel Layout Example	21	2009/10/01