HIGH-VOLTAGE MIXED-SIGNAL IC

UC1509

128 x 128 4S STN LCD Controller-Driver

MP Specifications
Datasheet Revision: 1.1

IC Version: c_A
November 13, 2020

ULTRACHIP

The Coolest LCD Driver, Ever!!

TABLE OF CONTENT

UC1509

Single-Chip, Ultra-Low Power
128COM x 128SEG Matrix
Passive LCD Controller-Driver

INTRODUCTION

UC1509c is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture and FRM (Frame Rate Modulation) gray-shade modulation scheme to achieve near crosstalk free images, with well balanced gray shades.

In addition to low power COM and SEG drivers, UC1509c contains all necessary circuits for high-V LCD power supply, bias voltage generation, temperature compensation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver for 128x128 matrix STN LCD with 4 gray shades and B/W Mode.
- A software-readable ID pin and an MTP programmable ID bit to support configurable vender identification.
- Partial scroll function and programmable data update window to support flexible manipulation of screen data.
- Support both row ordered and page_c (page column) ordered display buffer RAM access.
- Support industry standard 2-wire, 3-wire, 4-wire serial buses (I^2C, S8, S9) and 8-bit parallel buses (8080 or 6800).
- Special driver structure and gray shade modulation scheme. Consistent low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display window, Bias Ratio and Line Rate allow many flexible power management options.
- Four software programmable frame rates up to 201Hz. Support the use of fast Liquid Crystal material for speedy LCD response.
- Software programmable 4 temperature compensation coefficients.
- On-chip Power-ON Reset and Software RESET command, make RST pin optional.
- Self-configuring 9x charge pump with on-chip pumping capacitors. Only 3 external capacitors are required to operate.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- Very low pin count (9~10 pins with S8, S9, or I^2C) allows exceptional image quality in COG format on conventional ITO glass.
- Many on-chip and I/O pad layout features to support optimized COG applications.
- V_{DD} (digital) range (Typ.) : 1.8V ~ 3.3V
  V_{DD} (analog) range (Typ.) : 2.7V ~ 3.3V
  LCD V_{OP} range: 6.0V ~ 15V
- Available MTP trimming support precise LCD contrast matching.
- Available in gold bump dies
  Bump pitch: 26.5 μM
  Bump gap: 12 μM
  Bump surface: 2,001 μM^2

Remark: The inspection standard of the product appearance is based on Ultrachip's inspection document.

ORDERING INFORMATION

Part Number	MTP	I²C	Description
UC1509cGAA	Yes	Yes	Gold bumped die, Bump Height 12uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their applications in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

MTP LIGHT SENSITIVITY

The MTP memory cell is sensitive to photon excitation. Under extended exposure to strong ambient light, the MTP cells can lose its content before the specified memory retention time span. The system designer is advised to provide proper light shields to realize full MTP content retention performance.

USE OF I²C

The implementation of I²C is already included and tested in all silicon.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

CONTENT DISCLAIMER

CONTACT INFORMATION

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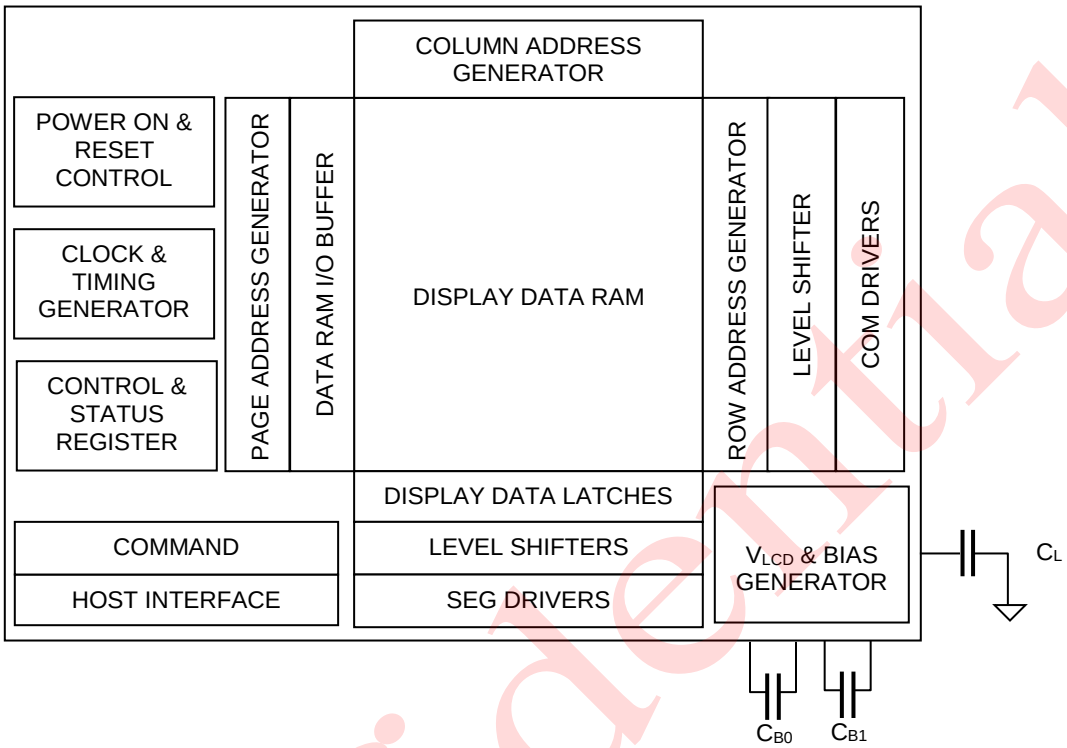
BLOCK DIAGRAM



PIN DESCRIPTION

Name	Type	Pins	Description
			MAIN POWER SUPPLY
V_{DD} V_{DD2} V_{DD3}	PWR	1 2 1	V_{DD} is the digital power supply and it should be connected to a voltage source that is no higher than V_{DD2}/V_{DD3}. V_{DD2}/V_{DD3} is the analog power supply and it should be connected to the same power source. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ Minimize the trace resistance for V_{DD} and V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	4 5	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. Minimize the trace resistance for this node.
			LCD POWER SUPPLY & VOLTAGE CONTROL
V_{B1+}, V_{B1-} V_{B0+}, V_{B0-}	PWR	2, 2 2, 2	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-} (2).  The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	1 1	High voltage LCD Power Supply. Connect these pins together. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the trace resistance under 50 Ω.

NOTE:

(1) Recommended capacitor values:
C_B: 150~250x LCD load capacitance or 2.2μF (5V), whichever is higher.
C_L: 330nF (25V) is appropriate for most applications.

(2) To avoid the correction of digital signals being affected by V_B charging / discharging, do not overlay C_B and the digital layout while FPC wiring.

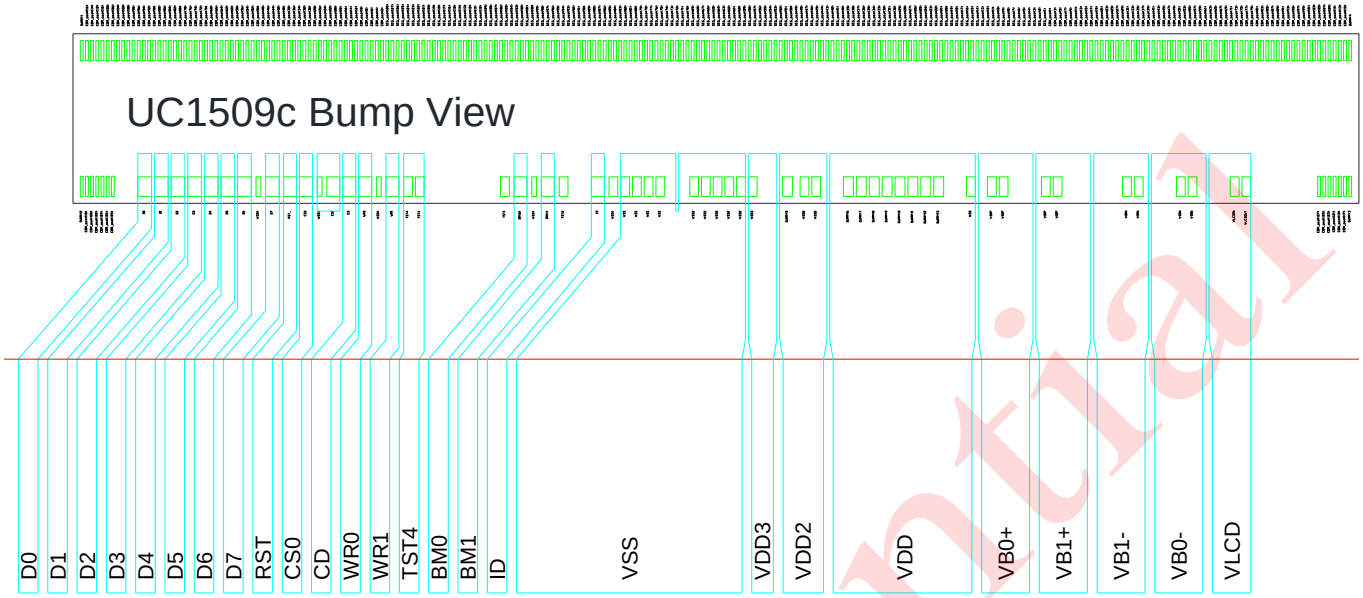
			HOST INTERFACE
BM0 BM1	I	1 1	Bus mode. The interface bus mode is determined by BM[1:0] and D[7:6] with the following relationship:

BM[1:0]	D[7:6]	Mode	Remark
11	Data	6800/8-bit	
10	Data	8080/8-bit	
01	11	2-wire I^2C	
00	10	4-wire SPI w/ 8-bit token	(S8: conventional)
01	10	3-wire SPI w/ 9-bit token	(S9: conventional)

CS0 / A2 CS1 / A3	I	1 1	Chip Select. Chip is selected when CS1="H" and CS0 = "L". When the chip is not selected, D[7:0] will be high impedance. In I^2C mode, these two pins indicate the I^2C bus address' bit 2 and bit 3.

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td>RST</td><td>I</td><td>1</td><td>When RST=”L”, all control registers are re-initialized by their default states. Since UC1509c has built-in Power-ON Reset and Software Reset command, RST pin is not required for proper chip operation.
An RC Filter has been included on-chip. There is no need for external RC noise filter. Connect the RST pin to MCU for reset control.</td></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation. In I^{2}C mode, CD pin is not used. Connect CD to V_{SS} when not used.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>ID</td><td>I</td><td>1</td><td>ID pin is for production control.
The connection will affect the content of PID when using the <code>Get Status</code> command. Connect to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR[1:0] controls the read/write operation of the host interface. See section Host Interface for more detail.
In parallel mode, WR[1:0] meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA,
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>BM=1x (Parallel)</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>BM=00 (S8)</td><td>1</td><td>0</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
<tr><td>BM=01 (S9)</td><td>1</td><td>0</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
<tr><td>BM=01 (I^{2}C)</td><td>1</td><td>1</td><td>–</td><td>–</td><td>SDA</td><td>–</td><td>–</td><td>SCK</td></tr>
</table>
Connect unused pins to V_{SS}.</td></tr>
<tr><th colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</th></tr>
<tr><td>SEG1 ~ SEG128</td><td>HV</td><td>128</td><td>SEG (page_c) driver outputs. Support up to 128 pixels.
Leave unused drivers open-circuit.</td></tr>
<tr><td>COM1 ~ COM128</td><td>HV</td><td>128</td><td>COM (row) driver outputs. Support up to 128 rows. Leave unused COM drivers open-circuit.</td></tr>
<tr><td colspan="4">Note: Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COMx or SEGx will correspond to index x-1, and the value ranges for those index registers will be 0~127 for COM and 0~127 for SEG.</td></tr>
<tr><th colspan="4">MISC. PINS</th></tr>
<tr><td>V_{DDX}</td><td></td><td>5</td><td>Auxiliary V_{DD}. These pins are connected to the main V_{DD} bus on chip. They are provided to facilitate chip configurations in COG application.
These pins should not be used to provide V_{DD} power to the chip. It is not necessary to connect V_{DDX} to main V_{DD} externally.</td></tr>
<tr><td>TST4</td><td>I/HV</td><td>2</td><td>Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation.
TST4 is also used as one of the high voltage programming power supply for MTP operation. For COG design with MTP options, please wire out TST4 with an ITO trace resistance 30 ~ 70 Ω.</td></tr>
<tr><td>TST1
TST2</td><td>I/O</td><td>1
1</td><td>Test I/O pin. Leave these pins open during normal use.</td></tr>
<tr><td>Dummy</td><td></td><td>13</td><td>Dummy pins are NOT connected inside the IC.</td></tr>
</table>

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The typical operation condition of UC1509c, V_{DD}=1.8V, should be met under all operating conditions. Unless V_{DD} and $V_{DD2/3}$ ITO trances can each be controlled to be 20 Ω or lower; otherwise V_{DD}-$V_{DD2/3}$ separation can cause the actual on-chip V_{DD} to drop below 1.65V during high speed data-write condition. Therefore, for COG, V_{DD}-$V_{DD2/3}$ separation requires very careful ITO layout and very stringent testing before MP.

CONTROL REGISTERS

UC1509c contains registers which control the chip operation. These registers can be modified by commands. The following table is a summary of the control registers, their meanings and their default values. Commands supported by UC1509c will be described in the next two sections. First, a summary table, followed by a detailed instruction-by-instruction description.

Name: The Symbolic reference of the register. Note that some symbol names refer to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after `Power-Up-Reset` and `System-Reset`.

Name	Bits	Default	Description
SL	7	00H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (no scrolling) and (127– 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT FLB	4 4	0H 0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN) of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections, 2xFLT on one side non-scrollable, 2XFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CR	5	00H	Return Page_C Address. Useful for cursor implementation.
CA	5	00H	Display Data RAM Page_C Address (Used in Host to Display Data RAM access)
RA	7	00H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 6 01b: 9 10b: 10 **11b: 11**
TC	2	0H	Temperature Compensation (per °C) **00b: -0.00%** 01b: -0.10% 10b: -0.15% 11b: -0.05%
PM	8	4EH	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	6	--	PM offset. PMO[5] = 1: The effective PM value, PMV = PM – PMO[4:0] PMO[5] = 0: The effective PM value, PMV = PM + PMO[4:0]
PC	4	EH	Power Control. PC[1:0]: 00b: LCD: ⩽ 6nF 01b: LCD: 6~9nF **10b: LCD: 9~13nF** 11b: LCD: 13~18nF PC[3:2]: 00b: External V_{LCD} **11b: Internal V_{LCD} (9X pump, standard)**
DC	4	8H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray Shade and B/W mode 0b: B/W Mode **1b: 4-Shade Mode**
AC	4	01H	Address Control: AC[0]: WA: Automatic page_c/row Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0: Page_C (CA) first** 1: Row (RA) first AC[2]: RID: RA (Row Address) auto increment direction (**L:+1** H:-1) AC[3]: Window Program Enable **0 : Disable** 1 : Enable

Name	Bits	Default	Description
LC	11	008H	LCD Control: LC[0]: Enable the first FLx2 lines in partial display mode (Default **OFF**). LC[1]: MX, Mirror X. SEG/Page_C sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **OFF**) LC[4:3]: Line Rate (Klps: Kilo-line-per-second) **00b: 14.2 Klps** 01b: 17.3 Klps 10b: 21.1 Klps 11b: 25.7 Klps Line Rate for On/Off mode: **00b: 5.7 Klps** 01b: 7.0 Klps 10b: 8.5 Klps 11b: 10.4 Klps (Line-Rate = Frame-Rate * Mux-Rate) LC[8:5]: Gray-Shade control. LC[6:5] / Gray-shade Level: 00 → 1; 01 → 2; 10 → 3; 11 → 4 LC[8:7] / Gray-shade Level: 00 → 3; 01 → 4; 10 → 5; 11 → 6 LC[10:9]: Partial Display Control **0xb: Disable.** Mux-Rate = CEN+1 (DST, DEN not used) 11b: Enabled. Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2
NIV	4	6H	N-line Inversion: NIV[1:0]: 00b: 9 lines 01b: 13 lines **10b: 17 lines** 11b: 23 lines NIV[2]: 0b: no-XOR **1b: XOR** NIV[3]: **0b: NIV Disabled** 1b: NIV Enabled
CEN DST DEN	7 7 7	7FH 00H 7FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN ⩾ DEN ⩾ DST+ 9
WPC0	5	00H	Window program starting page_c address. Value range: 0 ~31.
WPP0	7	00H	Window program starting row Address. Value range: 0~127.
WPC1	5	1FH	Window program ending page_c address. Value range: 0~31.
WPP1	7	7FH	Window program ending row Address. Value range: 0~127.
MTPC	6	10H	MTP Programming Control: MTPC[2:0] : MTP command **000** : Idle 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip use only. MTPC[3] : MTP Enable (auto clear after MTP command action done) MTPC[4] : Use/Ignore MTP value. 0: Ignore **1: Use** MTPC[5] : For testing only. Set to 0 for normal operation.
MTP	8	–	Multiple-Time Programming. MTP[5:0] for V_{LCD} fine tune MTP[7:6] for LCM manufacturer's configuration.
MTPM	6	00H	MTP Write Mask. 01H: program, **00H: no action**.
APC[2:0]	–	N/A	Advanced Product Configuration. For UltraChip only. Do *NOT* use.

Status Register			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag : 1 - MTP version, 0 - non-MTP version
MS	1	–	MTP programming in-progress
WS	1	–	MTP Command Succeeded
ID	1	PIN	Access the connected status of ID pin.
MX, MY, WA, DE, WS, MD, MS	1 1 1 1 1 1 1	1st	MX : Mirror X, LC[1] MY : Mirror Y, LC[2] WA : Wrap Around, AC[0] DE : Display Enable WS : MTP Succeeded MD : MTP Option. 1 - MTP version, 0 - non-MTP version MS : MTP Status
Ver, PMO	2 6	2nd	Ver : IC Version, range 00~-01, default : 0 PMO : PM Offset, PMO[5:0]
Prod, PID	4, 1	3rd	Prod[3:0], default = 7H, PID : connection status of accessing to ID pin.

COMMAND SUMMARY

The following is a list of host commands supported by UC1509c

C/D : 0: Control, 1: Data

W/R : 0: Write Cycle, 1: Read Cycle

D7-D0 : # Useful Data bits – Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	-	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Prod, PID}	N/A
				Ver[1:0]		PMO[5:0]							
				Prod[3:0]				0	PID	0	0		
4.	Set Page_C Address	0	0	0	0	0	#	#	#	#	#	Set CA[4:0]	00H
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7.	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8.	Set Adv. Program Control	0	0	0	0	1	1	0	0	R	R	Set R, R = 0~2	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#	Set APC[R][7:0]	
9.	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10.	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0H
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	0H
11.	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	4EH
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
12.	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[10:9]	00b: Disable
13.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14.	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	00H
		0	0	#	#	#	#	#	#	#	#		
15.	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18.	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
19.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20.	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[3:0]	6H
		0	0	-	-	-	-	#	#	#	#		
21.	Set LCD Gray Shade 1	0	0	1	1	0	1	0	0	#	#	Set LC[6:5]	01b
22.	Set LCD Gray Shade 2	0	0	1	1	0	1	0	1	#	#	Set LC[8:7]	10b
23.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25.	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
26.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
27.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
28.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
29.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
30.	Set Window Program Starting Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	0 #	0 #	Note (3)	Set WPC0	0
31.	Set Window Programming Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
32.	Set Window Programming Ending Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	1 #	0 #		Set WPC1	31
33.	Set Window Programming Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
34.	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Disable
35.	Set MTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]		10H
36.	Set MTP Write Mask	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[5:0]		0
37.	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Note (3)	Set MTP1	N/A
38.	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	
39.	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	
40.	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	
SERIAL READ COMMAND (ENABLED ONLY IN S8/S9 MODE)														
41.	Get Status	0	0	1	1	1	1	1	1	1	0	Get status until chip disabled		N/A
		0	1	-	MX	MY	WA	DE	WS	MD	MS			
		0	1	Ver[1:0]				PMO[5:0]						
		0	1	Prod[3:0]				0	PID	0	0			

Notes:

(1) Any bit patterns other than the commands listed above may result in undefined behavior.

(2) The interpretation of commands (36)~(40) depends on register MTPC[3].

(3) Commands (37)~(40) are shared with commands (30)~(33) and have exactly the same code.
When MTPC[3]=0, commands (37)~(40) are interpreted as `Window Programming` commands.
When MTPC[3]=1, they are the `MTP Control` commands.

(4) MTPM and PM are actually the same register. Only one of the commands (36 or 11) is valid at any time, and it is determined by MTPC[3].

(5) After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always
a) Remove TST4 power source,
b) Do a full V_{DD} ON-OFF-ON cycle.

COMMAND DESCRIPTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1, 2) operation uses internal Row Address register (RA) and Page_C Address register (CA). Four rows of LCD pixel image are defined as one row in SRAM. Each page_c of pixel corresponds to one page_c of SRAM data. RA and CA registers can be programmed by issuing `Set row Address` and `Set Page_C Address` commands. If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of page_c address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (PID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 31), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	-	MX	MY	WA	DE	WS	MD	MS
			Ver[1:0]		PMO[5:0]					
			Prod [3:0]				**0**	PID	**0**	**0**

Status 1 definitions:
- MX: Status of register LC[1], mirror X.
- MY: Status of register LC[2], mirror Y.
- WA: Status of register AC[0]. Automatic page_c/row wrap around.
- DE: Display enable flag. DE=1 when display is enabled
- WS: MTP Command Succeeded
- MD: MTP Option (1 - MTP version, 0 - non-MTP version)
- MS: MTP action status

Status 2 definitions:
- Ver[1:0]: IC Version Code, 00 ~ 11. Default: 00
- PMO[5:0]: PM offset value

Status 3 definitions:
- Prod[3:0]: Production Code. Value: 0111b (7h)
- PID: Provide connection status of accessing to ID pin.

If multiple `Get Status` commands are issued consecutively within one single CD 1⇨0⇨1 transaction, the `Get Status` command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page_C Address LSB CA[4:0]	0	0	**0**	**0**	**0**	CA4	CA3	CA2	CA1	CA0

Set SRAM page_c address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~31

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
00b= -0.00%/ºC 01b= -0.10%/ºC 10b= -0.15%/ºC 11b= -0.05%/ºC

(6) SET PANEL LOADING

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	**0**	**0**	**1**	**0**	**1**	**0**	PC1	PC0

Set PC[1:0] according to the capacitance loading of LCD panel.

Panel loading definition: 00b≤6nF 01b=6~9nF **10b=9~13nF** 11b=13~18nF

(7) SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External V_{LCD} **11b= Internal V_{LCD}** (9X pump, standard)

(8) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	R	R
(Double-byte command)	0	0	APC register parameter							

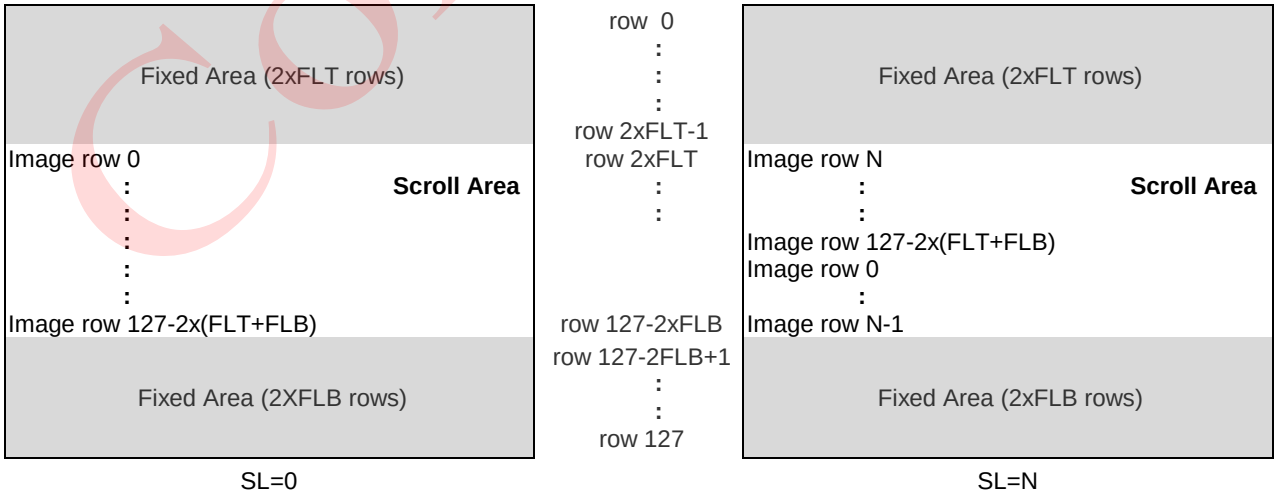
For UltraChip only. Please do NOT use.

(9) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	**0**	**1**	**0**	**0**	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[6:4]	0	0	**0**	**1**	**0**	**1**	**-**	SL6	SL5	SL4

Set the number of line to scroll up/down.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 127-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by `Set Fixed Lines` command.



(10) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address RA [6:4]	0	0	**0**	**1**	**1**	**1**	**-**	RA6	RA5	RA4

Set SRAM row Address for read/write access.

Possible value = **0**~127

(11) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0] (Double-byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 193**

(12) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [10:9]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	LC10	LC9

This command is used to enable partial display function.

LC[10:9] : **0xb: Disable Partial Display**, Mux-Rate = CEN+1 (DST, DEN not used.)
11b: Enable Partial Display, Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2

(13) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic page_c/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increase by one.

AC[1]: Auto-Increment order
0 : page_c (CA) increase (+1) first until CA reaches CA boundary, then RA will increase by (+/-1).
1 : row (RA) increase (+/-1) first until RA reach RA boundary, then CA will increase by (+1).

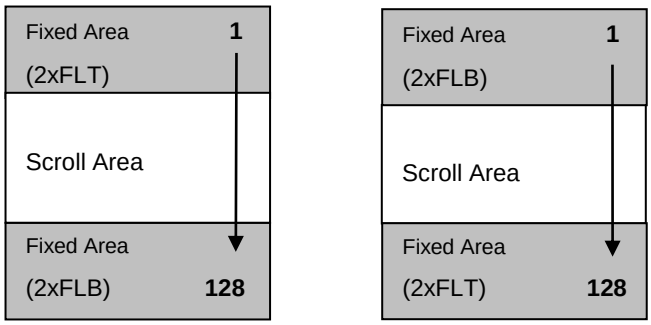
AC[2]: RID, Row Address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether row Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[3]=ON), see Command Description (31) ~ (35) for more details. When Window Program is disabled (AC[3]=OFF), the behavior of CA, RA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[3]=ON.

(14) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB}	0	0	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into Scroll and Fixed areas. The `Set Fixed Lines` command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], please make sure

MY=0 DST ⩾ FLTx2
DEN ⩽ (CEN-FLBx2).

MY=1 DST ⩾ FLBx2
DEN ⩽ (CEN-FLTx2)

(15) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Line-Rate = Frame-Rate * Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 85, 64, 43, and 32.

The followings are line rates at Mux Rate = 86~128:

00b: 14.2 Klps 01b: 17.3 Klps 10b: 21.1 Klps 11b: 25.7 Klps

(Klps: Kilo-Line-per-second)

while the followings are line rates in On/Off mode:

00b: 5.7 Klps 01b: 7.0 Klps 10b: 8.5 Klps 11b: 10.4 Klps

(16) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(17) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

(18) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [3:2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	DC3	DC2

This command is for programming register DC[3:2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit, and timing circuit will be halted to conserve power. When any of the DC[2] bits is set to 1, UC1509c will first exit from Sleep Mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3]: Gray Shade and B/W mode
0b: B/W Mode **1b: 4-Shade Mode**

For B/W mode, use data format for 4-shade-mode and UC1509c will convert them for B/W mode automatically.

Note : When the internal DC-DC converter starts to operate and pump out current to V_{LCD}, there will be an in-rush pulse current between V_{DD2} and V_{SS2} initially. To avoid this current pulse from causing potential harmful noise, do *NOT* issue any command or write any data to UC1509c for 5~10mS after setting DC[2] to 1.

(19) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] for COM (row) mirror (MY), SEG (page_c) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 31-CA as write/read (from host interface) display RAM page_c address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

(20) SET N-LINE INVERSION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-Line Inversion NIV [3:0]	0	0	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**
(Double-byte command)	0	0	**-**	**-**	**-**	**-**	NIV3	NIV2	NIV1	NIV0

This command is used for programming NIV[5:0] for N-Line Inversion:
NIV[1:0]: 00b: 9 lines 01b: 13 lines
10b: 17 lines 11b: 23 lines
NIV[2]: 0b: no-XOR **1b: XOR**
NIV[3]: **0b: Disable NIV** 1b: Enable NIV

(21) SET LCD GRAY SHADE 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[6:5]	0	0	**1**	**1**	**0**	**1**	**0**	**0**	LC6	LC5

This command sets gray scale register (LC[6:5]) to control the voltage RMS separation between the two gray shade levels (data "01" and data "10").

LC[6:5]: Select Gray-shade
00b: 1 **01b: 2** 10b: 3 11b: 4

LC[6:5]	Gray-shade Level	Gray-shade Intensity Mapped (0~36)
00b	1	9
01b	2	12
10b	3	15
11b	4	21

(22) SET LCD GRAY SHADE 2

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Gray Shade LC[8:7]	0	0	**1**	**1**	**0**	**1**	**0**	**1**	LC8	LC7

This command sets gray scale register (LC[8:7]) to control the voltage RMS separation between the two gray shade levels (data "01" and data "10").

LC[8:7]: Select Gray-shade
00b: 3 01b: 4 **10b: 5** 11b: 6

LC[8:7]	Gray-shade Level	Gray-shade Intensity Mapped (0~36)
00b	3	15
01b	4	21
10b	5	24
11b	6	27

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for "no operation".

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do not use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:
00b = 6 01b = 9 10b = 10 **11b = 11**

- The following commands (27~29) are for Partial Display:

(27) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**
(double-byte command)	0	0	**-**	*CEN [6:0]* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD.

(28) SET PARTIAL DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0**
(double-byte command)	0	0	**-**	*DST [6:0]* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

(29) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**
(double-byte command)	0	0	**-**	*DEN [6:0]* register parameter						

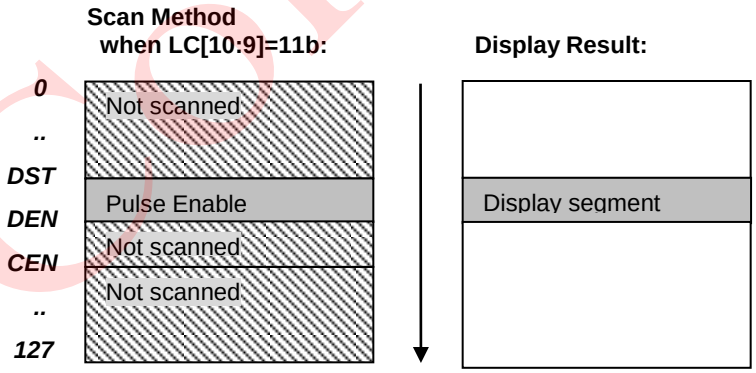
This command programs the ending COM electrode, which has been assigned a full scanning period, and which will output an active COM scanning pulse.

CEN, DST DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[10:9]=11b, the Mux-Rate is narrowed down to DEN - DST +1 + LC[0]x(FLT+FLB)x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also requires BR and V_{LCD} to be readjusted. When Mux-Rate is under 33, it is recommend to set BR=6.

For minimum power consumption, set LC[10:9]=11b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use B/W mode, set PC[1:0]=00b, and use lowest BR and lowest V_{LCD} which satisfies the contrast requirement.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(30) SET WINDOW PROGRAM STARTING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	**-**	**-**	**-**	*WPC0[4:0]* register parameter				

This command is to program the starting page_c address of RAM program window.

(31) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	**-**	*WPP0[6:0]* register parameter						

This command is to program the starting row Address of RAM program window.

(32) SET WINDOW PROGRAM ENDING PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	**-**	**-**	**-**	*WPC1[4:0]* register parameter				

This command is to program the ending page_c address of RAM program window.

(33) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	**-**	*WPP1[6:0]* register parameter						

This command is to program the ending row Address of RAM program window.

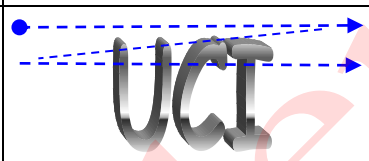
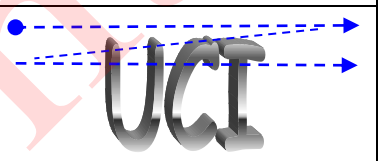
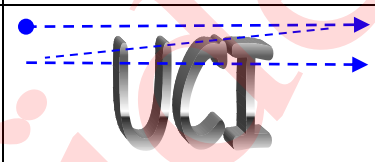
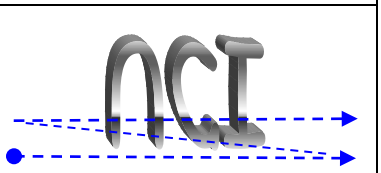
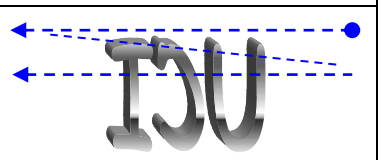
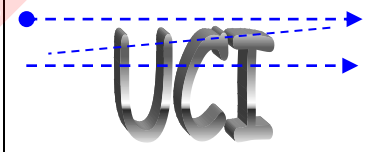
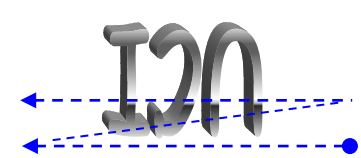
(34) SET WINDOW PROGRAM ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**0**	AC3

This command is to enable the Window Program Function. Window Program Enable should always be reset when changing the window program boundary and then set right before starting the new boundary program.

Window Program Function can be used to refresh the RAM data in a specified window of SRAM address. When window programming is enabled, the CA and RA increment and wrap around will be automatically adjusted, and therefore allow effective data update within the window.

The direction of Window Program will depend on the WA (AC[0]), PID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting. WA decides whether the program RAM address advances to next row / page_c after reaching the specified window page_c / row boundary. PID controls the RAM address increasing from WPP0 toward WPP1 (PID=0) or reverse the direction (PID=1). Auto-increment order directs the RAM address increment vertically (AC[1]=1) or horizontally (AC[1]=0). MX results the RAM page_c address increasing from 127-WPC0 to 127-WPC1 (MX=1) or WPC0 to WPC1 (MX=0).

Display Data Direction	Function Setting			Image in the Host (MPU) (Start : ●)	Image in Display Data Ram (Physical origin: upper left corner)
	AIO AC[1]	MX LC[1]	RID AC[2]		
Normal	0	0	0		
Y-mirror	0	0	1		
X-mirror	0	1	0		
X-mirror Y-mirror	0	1	1		

(35) SET MTP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPC (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**0**
	0	0	**-**	**-**	*MTPC* register parameter					

This command is for MTP operation control:

MTPC[2:0] : MTP command

000 : Idle 001 : MTP Read 010 : MTP Erase 011 : MTP Program
1xx : For UltraChip use only.

MTPC[3] : MTP Enable (automatically cleared each time after MTP command is done)
MTPC[4] : MTP value valid (ignore MTP value when L)
MTPC[5] : For testing only. Set to 0 for normal operation.

■ The following commands (36~40) are only valid when MTPC[3] =1:

DC[2] and MTPC[3] are mutually exclusive. Only one of these two control flags can be set to ON at any time. In other words, when DC[2] is ON, all MTP operations will be blocked, and, when MTP operation is active, set DC[2] to 1 will be blocked.

(36) SET MTP WRITE MASK

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTPM (double-byte command)	0	0	**1**	**0**	**1**	**1**	**1**	**0**	**0**	**1**
	0	0	**-**	**-**	*MTPM[5:0]* register parameter					

This command enables Write to each of the 7 individual MTP bits.

When MTPM[x]=1, the x-th bit of the MTP memory will be programmed to "1". MTPM[x]=0 means no write action for x-th bit. And the content of this bit will not change.

The amount of "programming current" increases with the number of 1's in MTPM. If the "programming current" appears to be too high for the LCM design (e.g. TST4 ITO trace is not wide enough to supply the current), use multiple write cycles and distribute the 1's evenly into these cycles.

MTPM[5:0]: Set PMO value

This command is only valid when MTPC[3]=1.

(37) SET V_{MTP1} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP1 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**
	0	0	Shared register parameter							

This command is for fine tuning V_{MPT1} (use with BR=00) and is only valid when MTPC[3]=1.

(38) SET V_{MTP2} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP2 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**1**
	0	0	Shared register parameter							

This command is for fine tuning V_{MTP2} (use with BR=10) and is only valid when MTPC[3]=1.

(39) SET MTP WRITE TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP3 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

(40) SET MTP READ TIMER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set MTP4 (double-byte command)	0	0	**1**	**1**	**1**	**1**	**0**	**1**	**1**	**1**
	0	0	Shared register parameter							

This command is only valid when MTPC[3]=1.

■ Serial Read Command (Enable only in S8/S9 mode):

(41) GET STATUS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	1	1	1	1	1	1	1	0
		1	**-**	MX	MY	WA	DE	WS	MD	MS
			Ver[1:0]		PMO[5:0]					
			Prod[3:0]				**0**	PID	**0**	**0**

Please refer to command (3).

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1509c via registers CEN, DST, DEN, and partial display control LC[10:9].

Combined with low power partial display mode and a low bias ratio of 6, UC1509c can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD} / V_{BIAS}$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

Due to the nature of STN operation, an LCD designed for good gray-shade performance at high Mux Rate (e.g. MR=128), can generally perform very well as a black and white display, at lower Mux Rate. However, it is also true that such technique generally cannot maintain LCD's quality of gray shade performance, since the contrast of the LCD will increase as the Mux Rate decreases, and the shades near the two ends of the spectrum will start to loose visibility.

UC1509c supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	9	10	11

Table 1: Bias Ratio

TEMPERATURE COMPENSATION

Four (4) different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	-0.00	-0.10	-0.15	-0.05

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[3:2].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

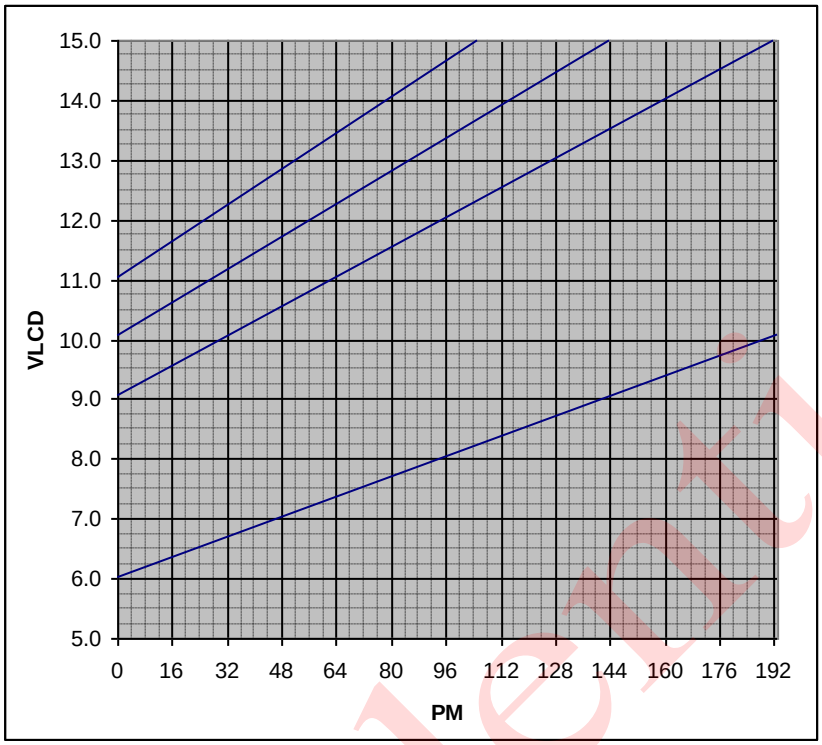
Gray shade LCD is sensitive to even a 1.5% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best results, software or MTP based V_{LCD} adjustment is the recommended method for V_{LCD} fine tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LCM design.

LOAD DRIVING STRENGTH

The power supply circuit of UC1509c is designed to handle LCD panels with load capacitance up to ~15nF when V_{DD2} = 2.7V. 15nF is also the recommended limit for LCD panel size for COG applications. For larger LCD panels, use higher V_{DD}.

VLCD QUICK REFERENCE



V_{LCD} Relationship to BR and PM at 25 °C

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} (V)
6	6.027	21.00	0	6.03
			193	10.08
9	9.083	30.82	0	9.08
			192	15.00
10	10.079	34.14	0	10.08
			144	15.00
11	11.070	37.41	0	11.07
			105	15.00

Note:

1. For good product reliability, keep $V_{LCD\ (max)}$ under **15.0V** under all operating temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR REFERENCE CIRCUIT

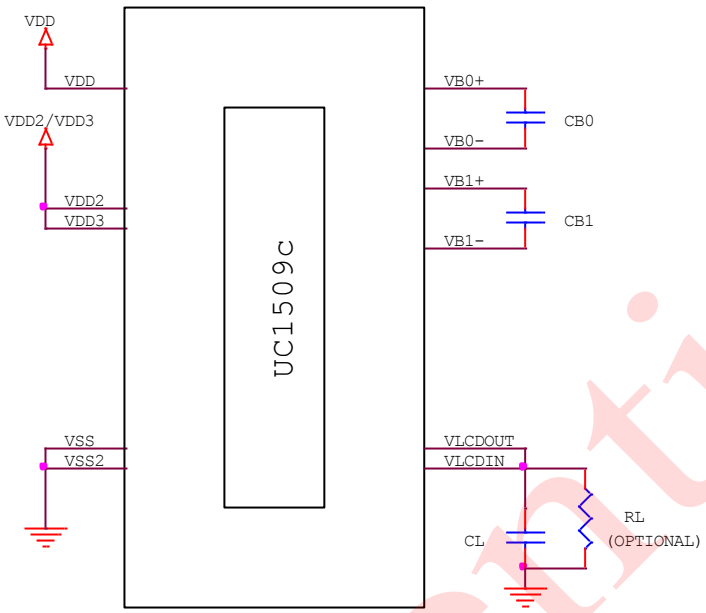


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

- Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)
  C_B: 150 ~ 250x LCD load capacitance or 2.2μF (5V), whichever is higher.
  C_L: 330 nF (25V) is appropriate for most applications.
  R_L: 3.3M Ω ~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1509c contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Four different line rates are provided for system design flexibility. The line rate is controlled by register LC[4:3]. When Mux-Rate is above 86, frame rate is calculated as:

Frame Rate = Line-Rate / Mux-Rate

When Mux-Rate is lowered to 85, 64, 43 and 32, line rate will be scaled down by 1.5, 2, 3 and 4 times automatically reduce power consumption.

Flicker-free frame rate is dependent on LC material and gray-shade modulation scheme. Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

When fast LC material with ($t_r + t_f$) < 160mS is used, faster line rate may be required under 4-shade mode to maintain good contrast ratio at operating temperature >50°C.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When COM drivers are in idle mode, their outputs are high-impedance (open circuit). When SEG drivers are in idle mode, their outputs are shorted to V_{SS}.

DRIVER ARRANGEMENTS

The naming conventions are: COM(x), where x=1~128, refers to the COM driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows fixed and it is not affected by SL, CST, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via `Set Display Enable` command. When DC[2] is set to OFF (logic “0”), both COM and SEG drivers will become idle and UC1509c will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become “1”, and UC1509c will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag is set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL SCROLL

Control register FL specifies a region of rows which are not affected by the SL register. Since SL register can be used to implement scroll function. The FL register can be used to implement fixed region when the other part of the display is scrolled by SL.

PARTIAL DISPLAY

UC1509c provides flexible control of Mux Rate and active display area. Please refer to Command Description (27) ~ (29) for more detail.

GRAY-SHADE MODULATION

UC1509c uses a proprietary line rate modulation scheme to generate 8 levels of gray shade. The relative levels of the gray shades can be programmed by setting register bit LC[8:5]. It controls the relative position of the light gray and dark gray shades. For detailed value, please refer to the register definition table.

ITO LAYOUT CONSIDERATIONS

Since the COM scanning pulses of UC1509c can be as short as 30μS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

For COG applications, low resistance ITO glass will help reduce SEG signal RC decay, minimize V_{DD}, V_{SS} noise, and ensure sufficient V_{DD2}, V_{SS2} supply for on-chip DC-DC converter.

COM TRACE

Excessive RC decay of COM scanning pulse can cause fluctuation of contrast and increase the crosstalk of COM direction.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 1.8\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

(Use worst case values for all calculations)

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 0.44\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

SEG TRACE

Excessive RC decay of SEG signal can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

To minimize crosstalk, please limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 0.5\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel page_c. It can be calculated by C_{LCD}/#_page_c, where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one page_c of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, visibility of shades will suffer, and crosstalk may increase sharply for medium shades.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	$(V_{ON}-V_{OFF})/V_{OFF}$	x0.80	x0.72
1/128	1/11	8.98%	7.2%	6.5%
1/128	1/10	8.79%	7.0%	6.3%

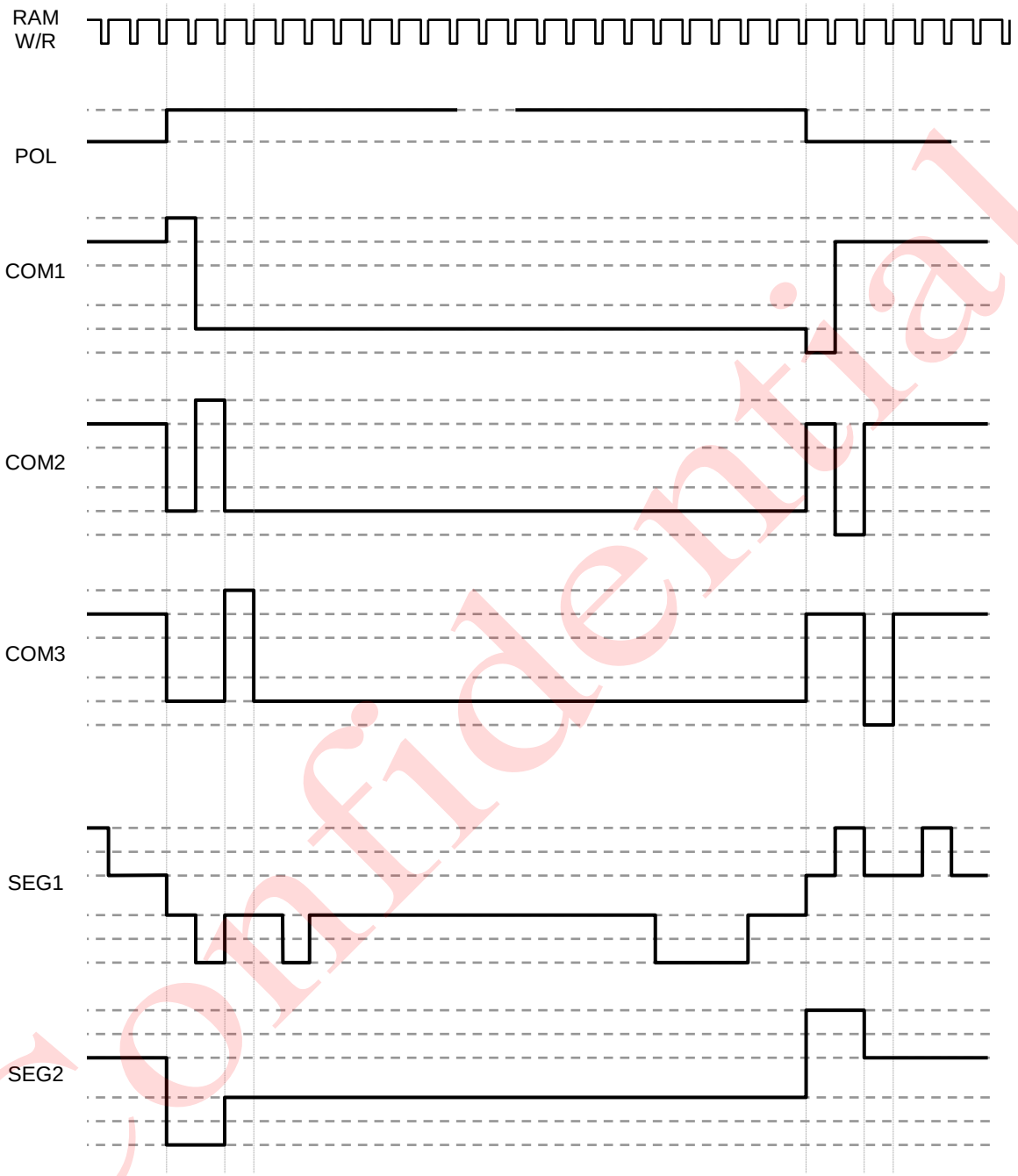


FIGURE 2: COM and SEG Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1509c supports two parallel bus protocols in 8-bit bus width, and three serial bus protocols. Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules.

		Bus Type				
		8080	**6800**	**S8 (4-wire)**	**S9 (3-wire)**	**I²C (2-wire)**
Width		8-bit	8-bit	Serial		
Access		Read / Write		Read (status) / Write		Read / Write
Control & Data Pins	BM[1:0]	10	11	00	01	01
	D[7:6]	Data	Data	10	10	11
	CS[1:0]	Chip Select				A[3:2]
	CD	Control/Data				–
	WR0	$\overline{WR}$	R/$\overline{W}$	0	0	0
	WR1	$\overline{RD}$	EN	0	0	0
	D[5:4]	Data	Data	–		
	D[3:0]	Data	Data	D0=SCK, D3=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}.

Table 3: Host interfaces Choices

PARALLEL INTERFACE

The timing relationship between UC1509c internal control signals, RD and WR, and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipe-line. This architecture requires that, every time memory address is modified, by either `Set CA`, or `Set RA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipe-line and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

8-BIT BUS OPERATION

UC1509c supports both 8-bit bus width.

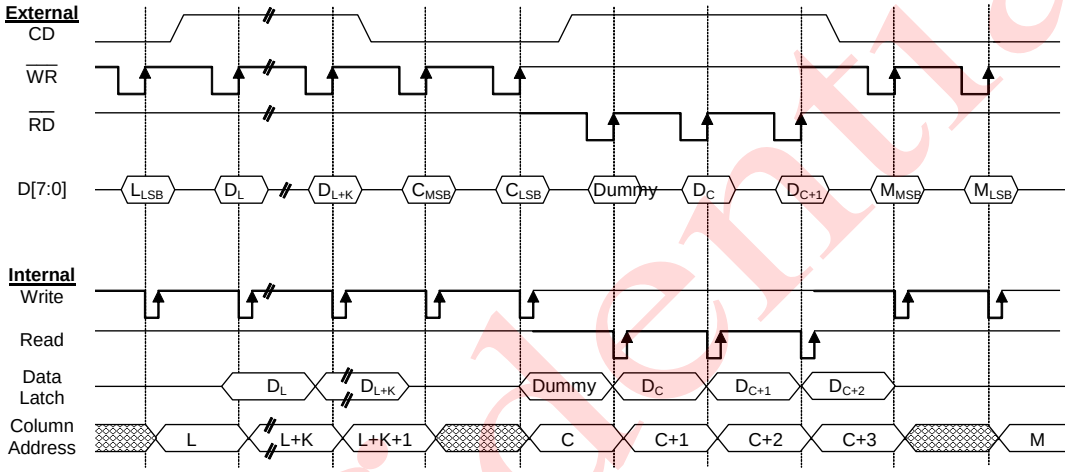


FIGURE 3: 8 bit Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1509c supports three serial modes, one 4-wire SPI mode (S8), one compact 3-wire mode (S9) and one 2-wire mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and D[7:6]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, these 8 bits will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

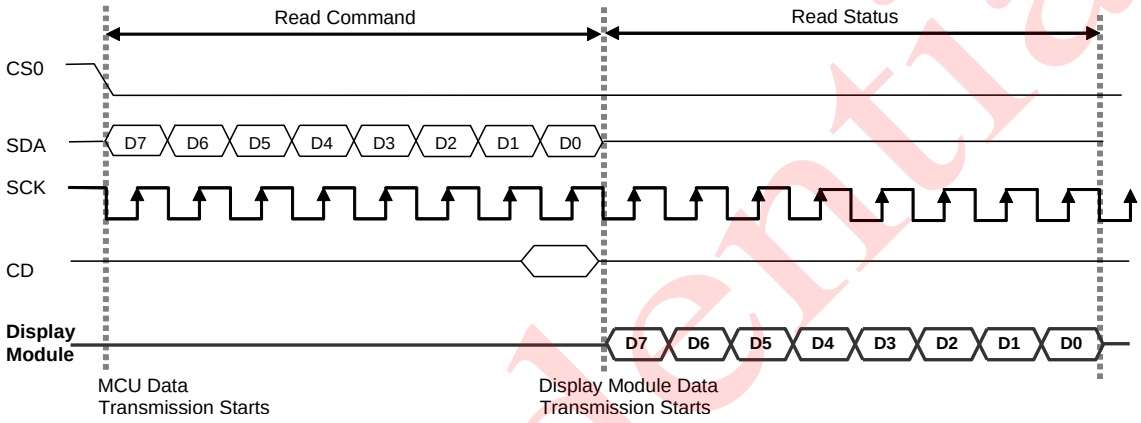


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

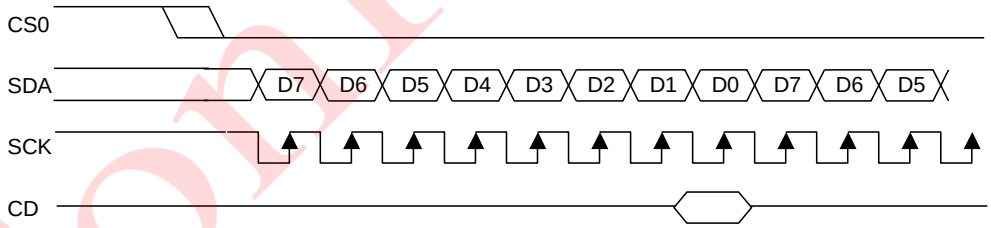


FIGURE 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIRE) INTERFACE

Pins CS[1-0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command/data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 or CS1 for each byte of data/command is recommended but optional.

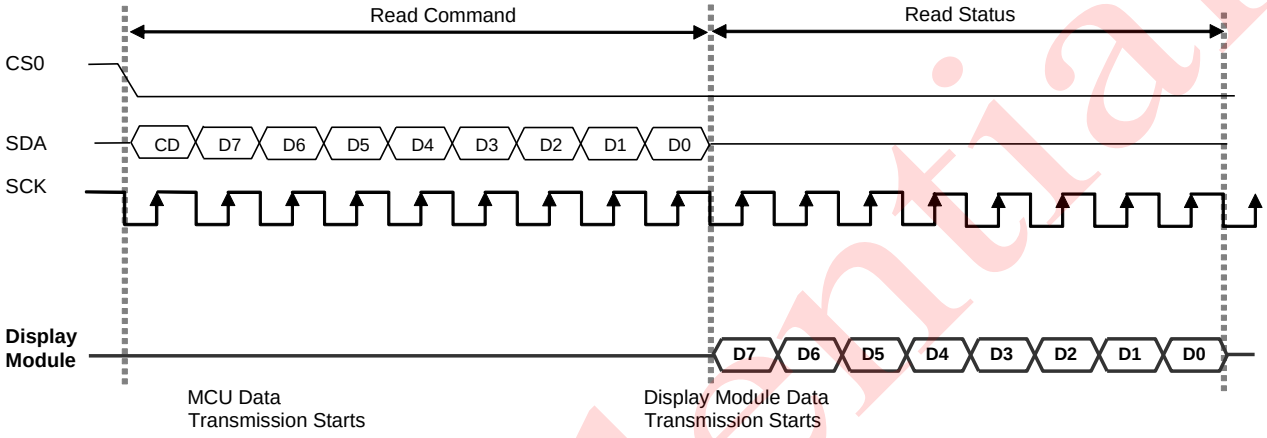


FIGURE 5.a: 3-wire Serial Interface (S9) – Read

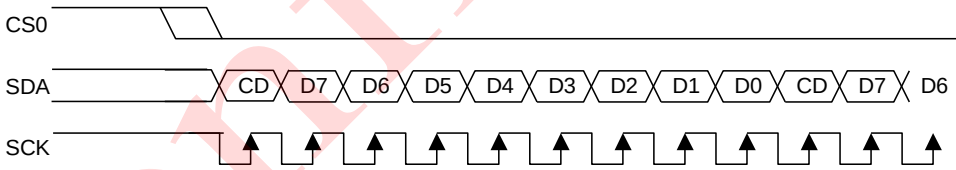
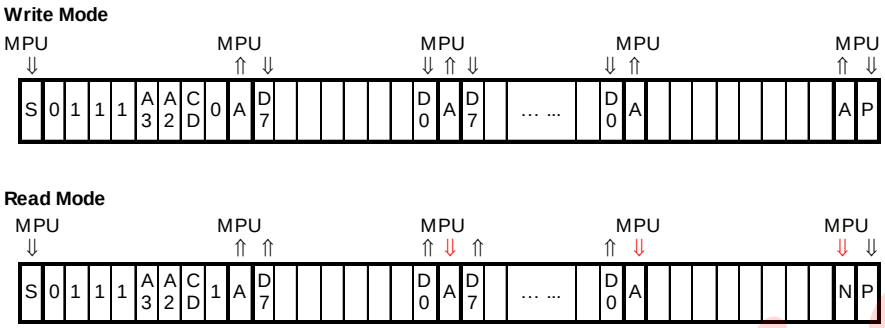


FIGURE 5.b: 3-wire Serial Interface (S9) – Write

2-WIRE SERIAL INTERFACE (I²C)



When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1509c is configured as an I²C bus signaling protocol compliant slave device. Please refer to I²C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1509c' device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I²C mode.

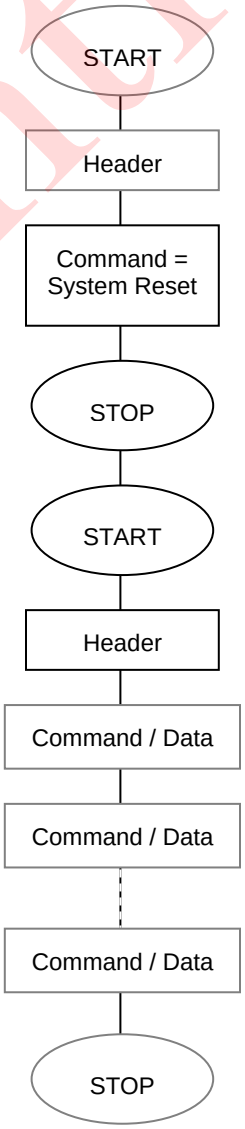
Each UC1509c I²C interface sequence starts with a START condition (S) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I²C mode and should be connected to V_{SS}. The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1509c will send out an acknowledge signal (A). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1509c) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE), or a Not Acknowledge (N, in READ mode) is sent by the bus master.

When using I²C serial mode, if the command of System Reset is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

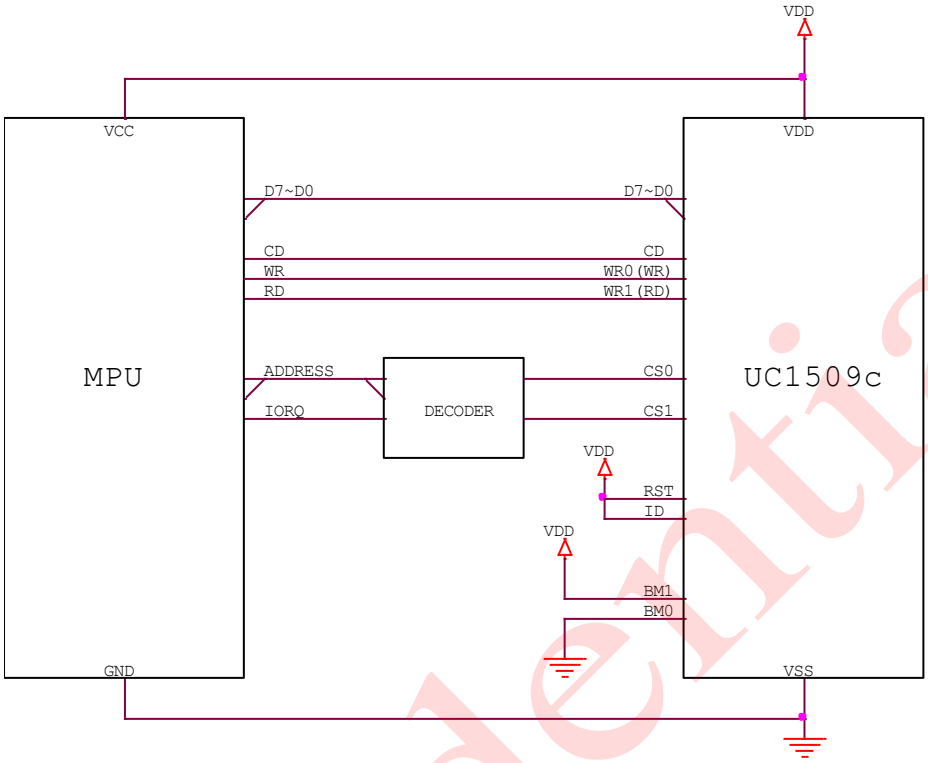


FIGURE 6: 8080/8bit parallel mode reference circuit

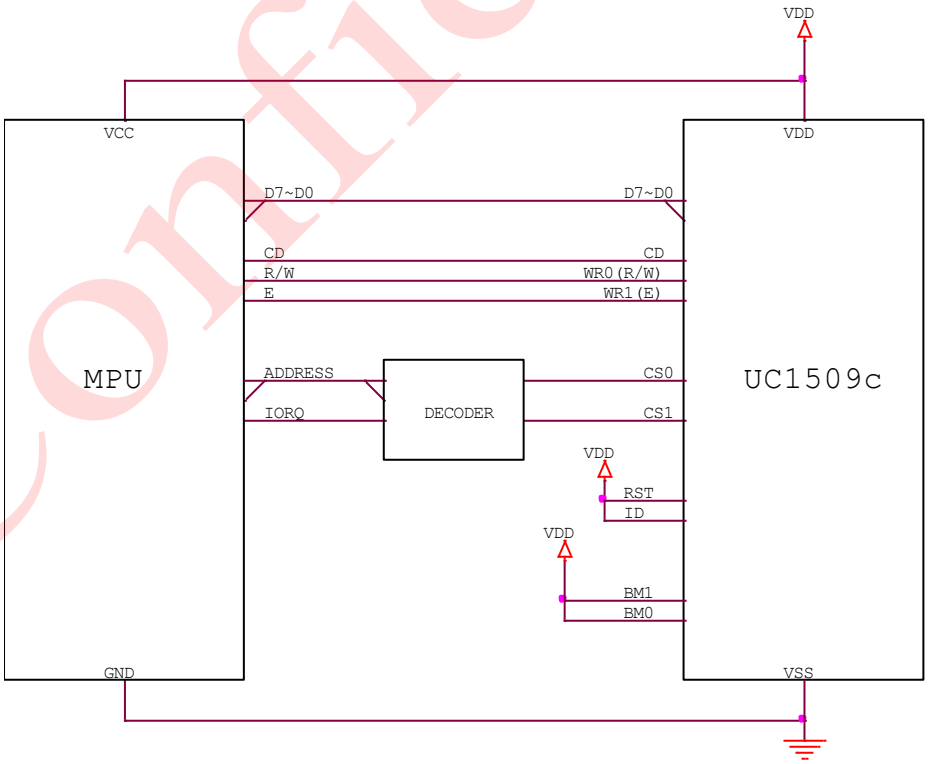


FIGURE 7: 6800/8bit parallel mode reference circuit

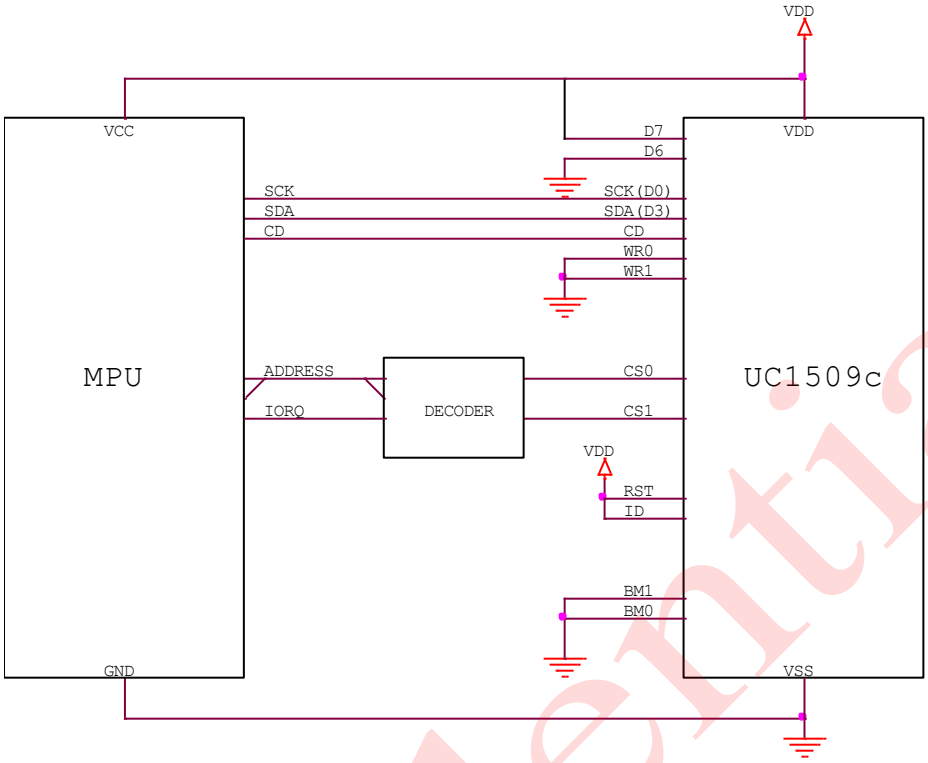


FIGURE 8: 4-Wires SPI (S8) serial mode reference circuit

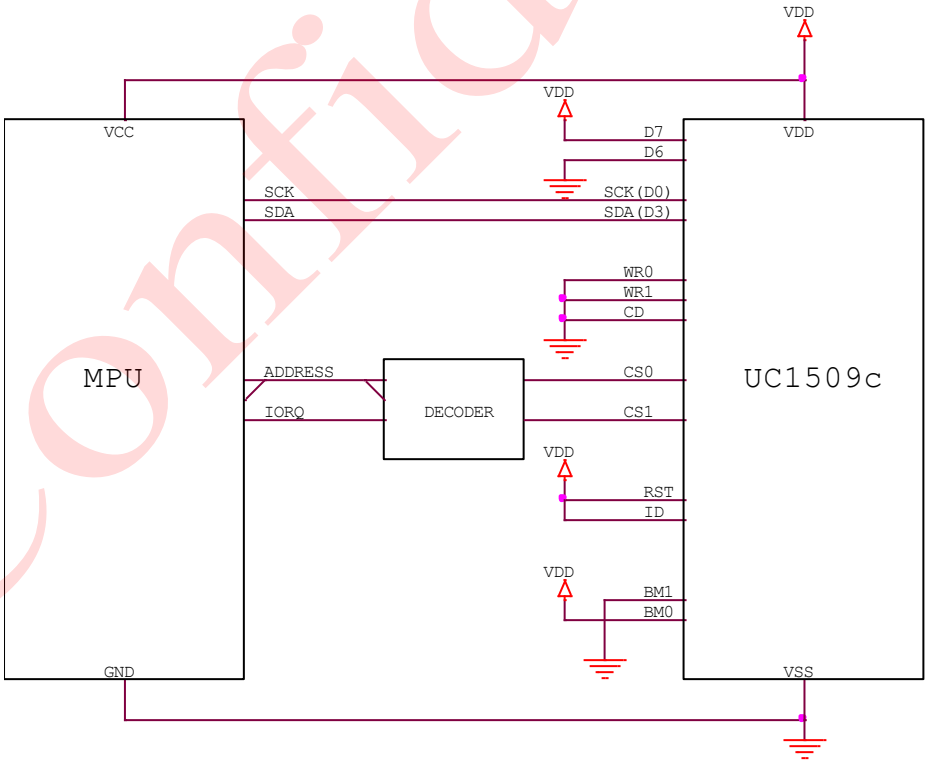


FIGURE 9: 3/4-Wires SPI (S9) serial mode reference circuit

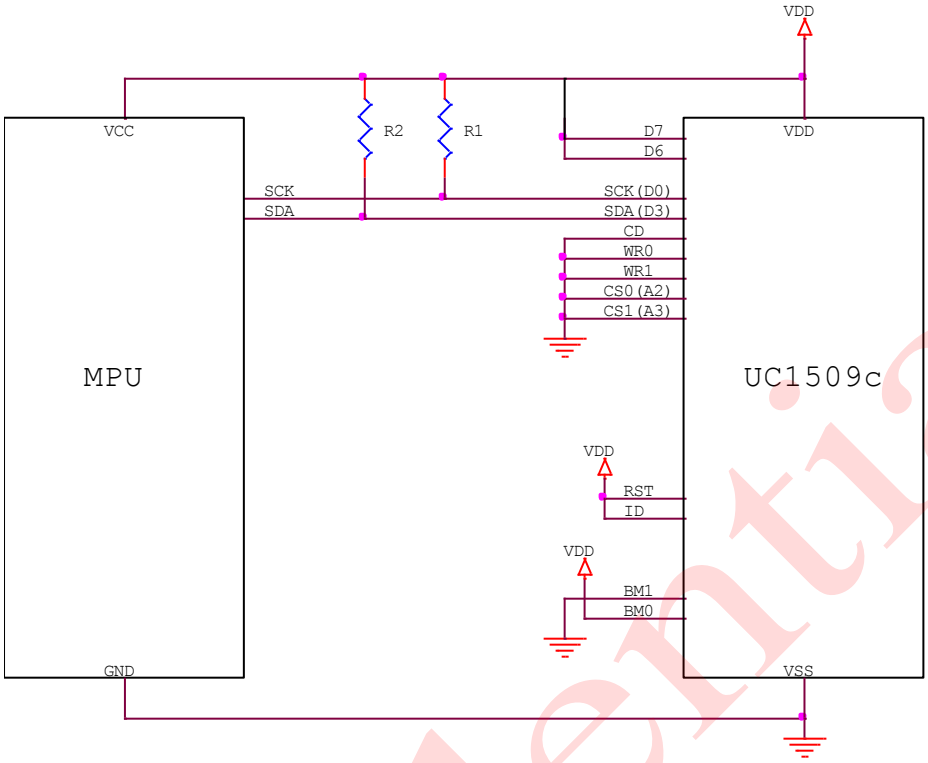


FIGURE 10: I²C serial mode reference circuit

Note

- The ID pin is for production control. The connection will affect the content of PID of the 3rd byte of `Get Status` command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. Connect the RST pin to MCU for reset control.
- When using I²C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

DISPLAY DATA RAM

DATA ORGANIZATION

The input display data is stored to a dual port static RAM (RAM, for Display Data RAM) organized as 128x128x2.

After setting CA and RA, the subsequent data write cycles will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its page_c and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Page_C Address (CA) by issuing `Set Row Address` and `Set Page_C Address` commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (127), and system programmers need to set the values of RA and CA explicitly.

If WA is ON (1), when CA reaches end of row, CA will be reset to 0 and RA will increase or decrease, depending on the setting of row Increment Direction (PID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Page_C Mirroring (MX) is implemented by selecting either (CA) or (31–CA) as the RAM page_c address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[2]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning COM electrodes can be obtained by combining the fixed COM scanning sequence and the following RAM address generation formula.

When FLT & FLB=0, during the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*

Otherwise
Line = Mod(*Line*+1, 128)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to SEG drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produces the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *128*. Effects such as row scrolling, row swapping can be emulated by changing SL dynamically.

MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between COM electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MUX-1*, *128*)
where MUX = CEN + 1

Otherwise
Line = Mod(*Line-1* , *128*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

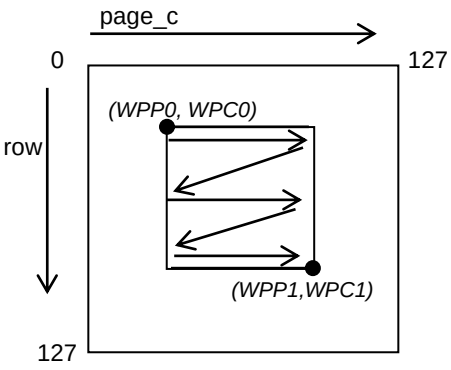
WINDOW PROGRAM

Window program is designed for data write in a specified window range of SRAM address. The procedure should start with window boundary registers setting (*WPP0*, *WPP1*, *WPC0* and *WPC1*) and then enable AC[3]. After AC[3] sets, data can be written to SRAM within the window address range which is specified by (*WPP0, WPC0*) and (*WPP1, WPC1*). AC[3] should be cleared after any modification of window boundary registers and then set again in order to initialize another window program.

The data write direction will be determined by AC[2:0] and MX settings. When AC[0]=1, the data write can be consecutive within the range of the specified window. AC[1] will control the data write in either page_c or row direction. AC[2] will result the data write starting either from row *WPP0* or WPP1. MX is for the initial page_c address either from *WPC0* to *WPC1* or from (*MC-WPC0* to *MC-WPC1*).

Example1:

AC[2:0] = 001, MX=0



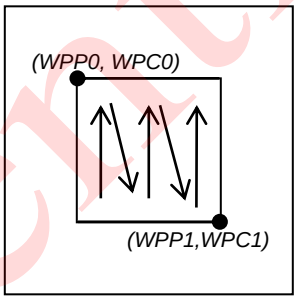
AC[0]=1: Automatically wrap around

AC[1]=0: Page_c increases first

AC[2]=0: increment direction is “+1”

Example 2:

AC[2:0] = 111, MX=0



AC[0]=1: Automatically wrap around

AC[1]=1: Row increases first

AC[2]=1: increment direction is “-1”

RAM

Line Adderss	Data	D1 / 0	D3 / 2	D5 / 4	D7 / 6	D1 / 0	D3 / 2	D5 / 4	D7 / 6		D1 / 0	D3 / 2	D5 / 4	D7 / 6
00H		11	10	01	00									
01H		00	11	10	01									
02H														
03H														
04H														
05H														
06H														
07H														
08H														
09H														
0AH														
0BH														
0CH														
0DH														
0EH														
0FH														
10H														
11H														
12H														
13H														
14H														
15H														
16H														
17H														
		Page_C0				Page_C1					Page_C31			
6CH														
6DH														
6EH														
6FH														
70H														
71H														
72H														
73H														
74H														
75H														
76H														
77H														
78H														
79H														
7AH														
7BH														
7CH														
7DH														
7EH														
7FH														
MX	0	C1	C2	C3	C4	C5	C6	C7	C8		C125	C126	C127	C128
	1	C128	C127	C126	C125	C124	C123	C122	C121		C4	C3	C2	C1

MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
R1	R113	R128	R16
R2	R114	R127	R15
R3	R115	R126	R14
R4	R116	R125	R13
R5	R117	R124	R12
R6	R118	R123	R11
R7	R19	R122	R10
R8	R120	R121	R9
R9	R121	R120	R8
R10	R122	R119	R7
R11	R123	R118	R6
R12	R124	R117	R5
R13	R125	R116	R4
R14	R126	R115	R3
R15	R127	R114	R2
R16	R128	R113	R1
R17	R1	R112	R128
R18	R2	R111	R127
R19	R3	R110	R126
R20	R4	R109	R125
R21	R5	R108	R124
R22	R6	R107	R123
R23	R7	R106	R122
R24	R8	R105	R121
R109	R93	R20	R36
R110	R94	R19	R35
R111	R95	R18	R34
R112	R96	R17	R33
R113	R97	R16	R32
R114	R98	R15	R31
R115	R99	R14	R30
R116	R100	R13	R29
R117	R101	R12	R28
R118	R102	R11	R27
R119	R103	R10	R26
R120	R104	R9	R25
R121	R105	R8	R24
R122	R106	R7	R23
R123	R107	R6	R22
R124	R108	R5	R21
R125	R109	R4	R20
R126	R110	R3	R19
R127	R111	R2	R18
R128	R112	R1	R17
		128	128
		MUX	

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

Row1 Page_C0 ⇨ D[7:0] : 00011011b
Row2 Page_C0 ⇨ D[7:0] : 01101100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1509c has two different types of Reset:
Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1509c enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1509c has three operating modes (OM):
Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep Mode.

OM changes are synchronized with the edges of UC1509c internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` *or* `System Reset` commands.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1509c consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1509c contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1509c internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

UC1509c power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of `System-Reset` command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1509c. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands.

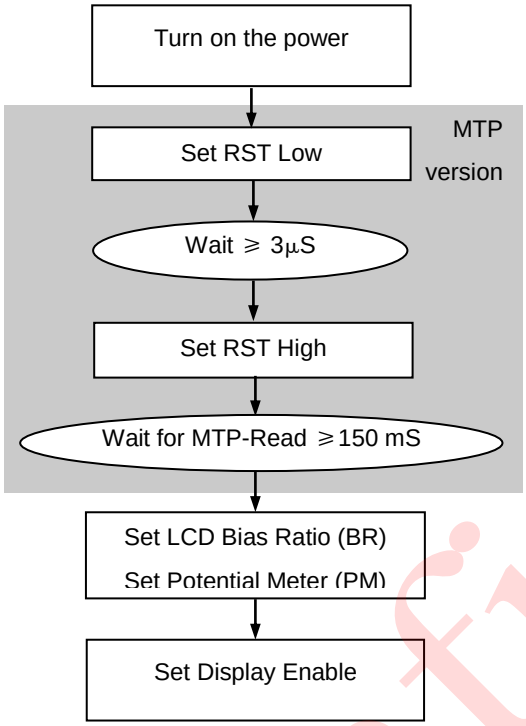


Figure 11: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L from causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge the external capacitor.

When internal V_{LCD} is not used, UC1509c will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

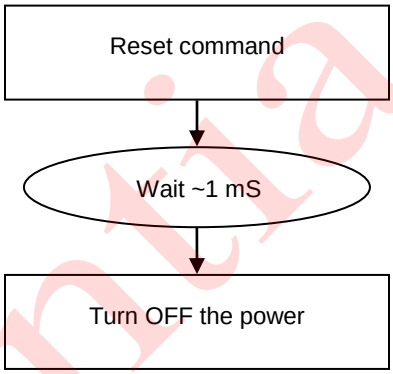


Figure 12: Reference Power-Down Sequence

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

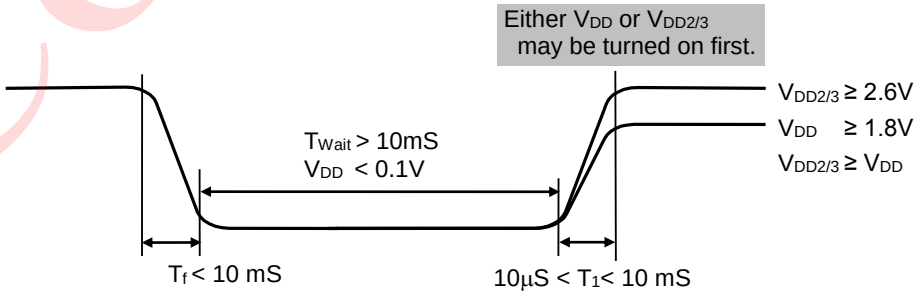


Figure 13: Delay allowance between V_{DD} and V_{DD23}

SAMPLE POWER MANAGEMENT COMMAND SEQUENCES

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type
Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1).

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn on V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 3μS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait 150mS after V_{DD} is ON
R	0 0	0 0	0 0	0 0	1 0	1 0	0 0	0 0	0 0	1 0	Set APC Command	Turn ON low voltage detector function.
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping	
A	0	0	1	0	1	0	0	0	#	#	Set Line Rate	Fine tune for power, flicker, contrast, and shading.
C	0	0	1	1	0	1	0	1	#	#	Set Gray Shade	
C	0	0	1	1	1	0	1	0	#	#	Set Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~1mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

MULTIPLE-TIME PROGRAM (MTP) NV MEMORY

OVERVIEW

MTP feature is available for UC1509c such that LCM maker can record an PM offset value in non-volatile memory cells, which can then be used to adjust the effective V_{LCD} value, in order to achieve high level of consistency for LCM contrast across all shipments.

To accomplish this purpose, three operations are supported by UC1509c:

MTP-Erase, MTP-Program, MTP-Read.

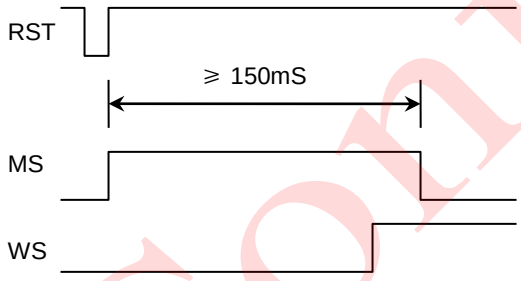
MTP-Program requires an external power source supplied to the TST4 pin. MTP allows program at least 10 times and should be performed only by the LCM makers.

MTP-Read is facilitated by the internal DC-DC converter built-in on UC1509c, no external power source is required, and it is performed automatically after hardware RESET (power-ON or pin RESET).

OPERATION FOR THE SYSTEM USERS

For the MTP version of UC1509c, the content of the NV memory will be read automatically after the power-on and hardware pin RESET. There is no user intervention or external power source required. When set up properly, the V_{LCD} will be fine tuned to achieve high level of consistency for the LCM contrast.

The MTP-READ is a relatively slow process and the time required can vary quite a bit. For a successful MTP-READ operation, the MS and WS bits in the Read Status commands will exhibit the following waveforms.



As illustrated above, the {MS, WS} will go through a {0,0}⇨{1,0}⇨{1,1}⇨{0,1} transition. When the {MS, WS}={0,1} state is reached, it means the LCM is ready to be turned on.

Although user can use `Read Status` command in a polling loop to make sure {MS,WS}={0,1} before proceeding with the normal operation, however, it may be simpler to just issue `Set Display Enable` command every 0.5~2 second, repeatedly, together with other LCM optimization settings, such as BR, CEN, TC, etc.

The above "Periodical re-initializing" approach is also an effective safeguard against accidental display off events such as

- ESD strikes
- Mechanical shocks causing LCM connector to malfunction temporarily

HARDWARE VS. SOFTWARE RESET

The auto-MTP-READ is only performed for hardware RESET (power-ON and RST pin), but not for software `RESET` command. This enables the ICs to turn on display faster without the delay caused by MTP-Read.

It is recommended to use the software *RESET* for such operation control purpose and use hardware RESET only during the event of power up and power down.

OPERATION FOR THE LCM MAKERS

Always ERASE the MTP NV memory cells, before starting the Write process.

MTP OPERATION FOR LCM MAKERS

1. High voltage supply and timer setting

In MTP Program operation, two different high voltages are needed. In chip design, one high voltage is generated by internal charge pump (V_{LCD}), the other high voltage must be input from TST4 by external voltage source.

V_{LCD} value is controlled by register MTP3 and MTP2. The default values of these two registers are appropriate for most applications.

External TST4 power source is required for MTP Program operation. MTP Programming speed depends on the TST4 voltage. Considering the ITO trace resistance in COG modules, it is recommended to program the MTP cells one at a time, so that the required 10V at TST4 can be maintained with proper consistency.

No external power source is required for MTP Erase and Read operation. For these MTP operation, TST4 should be open, or connected to V_{DD3}.

	V_{LCD}	**TST4 (external input)**
Program	MTP3 : 39h (12V)	10V (1mA per bit)
Erase	MTP3 : 39h (12V)	Floating or V_{DD3}
Read	MTP2 : 00h (6V)	Floating or V_{DD3}

Note:

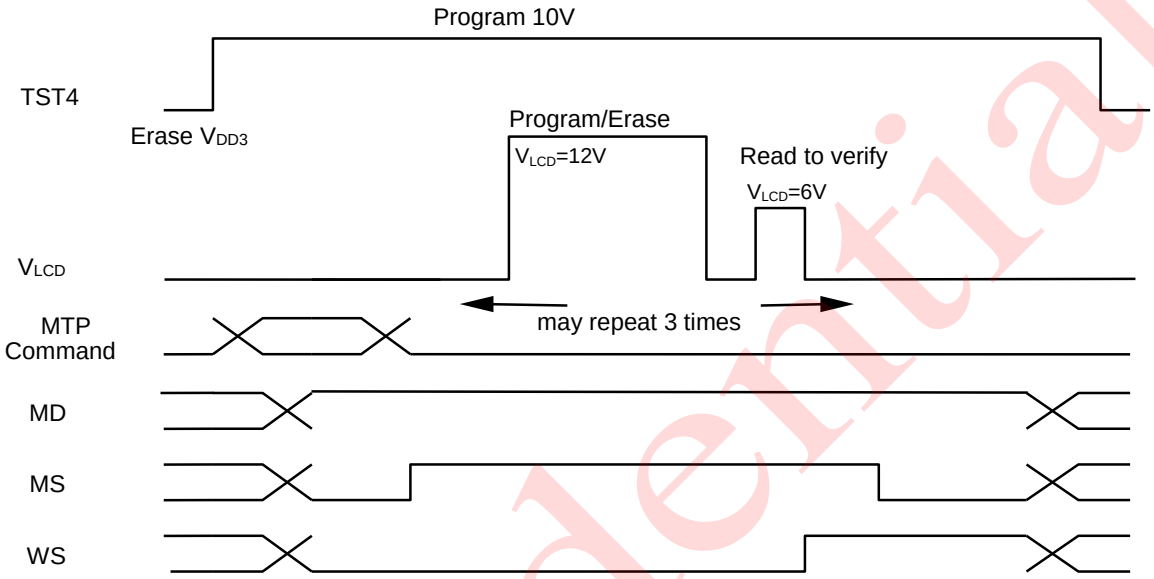
1. Do Erase before Program and Program one bit at a time.
2. When doing MTP Program or Erase, it's required to use $V_{DD2/3} \geqq 3.0V$.

2. Read MTP status bits

With normal Get Status method (CD=0, W/R=1), MTP operation status can be monitored in the real time. There are 3 status bits (WS, MD, MS) in status register. MTP control circuit will read to verify if the operation (program, erase) success or not.

WS : If the operation succeeded, and current operation will be ended with WS=1.
If it failed, last operation will be automatically retried two more times. If it fails 3 times, WS will be set to 0 and the operation is aborted.

MD is MTP ID, which is either 1 for MTP IC. No transition.



MTP status bits, TST4 & V_{LCD} Waveform

3. MTP Cell Value Usage

There are 8 MTP cell bits. They are divided into two groups for different trimming purpose.

(1) MTP[5:0] : V_{LCD} Trim

When PMO[5]=1: PM with trim = PM - PMO[4:0]
When PMO[5]=0: PM with trim = PM + PMO[4:0]

(2) MTP[7:6] : For LCM manufacturer's configuration.

MTP COMMAND SEQUENCE SAMPLE CODES

The following tables are examples of command sequence for MTP Program and Erase operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

MTP operations (Erase, Program, Read) and Set Display ON is mutual exclusive. There is no harm done to the IC or the LCM if this is violated. However, the violating commands will be ignored.

Type
Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of dataflow of the cycle. It can be either Write (0) or Read (1).

(1) MTP Program Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip Action	Comments
R	-	-	-	-	-	-	-	-	-	-	Set RST pin LOW	Wait 1mS after RST is LOW
R	-	-	-	-	-	-	-	-	-	-	Set RST pin HIGH	
R	-	-	-	-	-	-	-	-	-	-	Automatic Power-ON-Reset	Wait ~150mS
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP-Read V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP-Write V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP3: 39h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	1	1		MTP4: 27h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	0		MTP5: 04h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	-	-	0	0	0	0	0	1	MTPM	Ex: To program D0 to be 1, set MTPM to 000001b*
R	-	-	-	-	-	-	-	-	-	-	Apply TST4 voltage	Program: 10V
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	1		Set MTPC[2:0]=011
R	0	1	-	-	-	-	-	WS	-	MS	Get Status & PM	Check MTP Status until MS=0 and WS=1
R												Remove TST4 voltage
R											V_{DD}=0V	Power OFF

* It is recommended that users program one bit at a time.

(2) MTP Erase Sample Code

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	0	0	1	1	Set Line Rate	Set LC[4:3]=11b
R	0	0	1	1	1	1	0	1	0	0	Set V_{MTP1} Potentiometer	Set MTP-Read V_{LCD}
R	0	0	0	0	0	0	0	0	0	0		MTP2: 00h(6V)
R	0	0	1	1	1	1	0	1	0	1	Set V_{MTP2} Potentiometer	Set MTP-Write V_{LCD}
R	0	0	0	0	1	1	1	0	0	1		MTP3: 39h(12V)
R	0	0	1	1	1	1	0	1	1	0	Set MTP Write Timer	Set MTP Timer
R	0	0	0	0	1	0	0	1	1	1		MTP4: 27h(100mS)
R	0	0	1	1	1	1	0	1	1	1	Set MTP Read Timer	Set MTP Timer
R	0	0	0	0	0	0	0	1	0	0		MTP5: 04h(10mS)
R	0	0	1	0	1	1	1	0	0	1	Set MTP Write Mask	Set MTP Bit Mask
C	0	0	-	-	1	1	1	1	1	1	MTPM	Ex: To erase D[7:0], set MTPM to 111111b*
R	0	0	1	0	1	1	1	0	0	0	Set MTP Control	Set MTPC[3]=1
R	0	0	-	-	0	0	1	0	1	0		Set MTPC[2:0]=010
R	0	1	-	-	-	-	-	ws	-	MS	Get Status & PM	Check MTP Status until MS=0, WS=1
R											V_{DD}=0V	Power OFF

* It is recommended that users clear all the bits to be programmed.

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is therefore highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1509c require special "ESD Sensitivity" consideration in particular:

Test Mode (normal samples – MTP:00)		Machine Mode		Human Body Mode	
		V_{DD} mode	V_{SS} mode	V_{DD} mode	V_{SS} mode
LCD Driver		200V	200V	2.5KV	2.5KV
LCM Digital Interface		300V	300V	3.0KV	3.0KV
LCM HV pin / Test pin	TST1/2/4	250V	250V	3.0KV	2.5KV
	V_B pins	300V	300V	3.0KV	3.0KV
	V_{LCDIN}	300V	300V	3.0KV	3.0KV
	V_{LCDOUT}	300V	300V	3.0KV	3.0KV
PWR / GND			300V		3.0KV

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134, note 1 and 2.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.6	V
V_{LCD}	LCD Generated voltage (-30^{o}C ~ +80^{o}C)	-0.3	+19.8	V
V_{IN}	Digital input signal	-0.4	V_{DD} + 0.5	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:

1. V_{DD} is based on V_{SS} = 0V
2. Stress beyond ranges listed above may cause permanent damage to the device. These are stress rating only. This device should be operated under DC/AC characteristics condition for normal operation. Exposure to over the DC/AC characteristics conditions for extended periods may affect device reliability and function operation.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.6		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.6V, 25^{O}C		14	15	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.6V, 25^{O}C	0.89		1.78	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	μA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3}$ = 3.3V, Temp = 85 °C			50	μA
C_{IN}	Input capacitance			5	10	pF
C_{OUT}	Output capacitance			5	10	pF
$R_{ON(SEG)}$	SEG output impedance	V_{LCD} = 15V		1.6	2.1	kΩ
$R_{ON(COM)}$	Upward COM output impedance	V_{LCD} = 15V		1.6	2.1	kΩ
$R_{ONS(COM)}$	Downward COM output impedance			1.85	2.5	kΩ
f_{LINE}	Average Line rate	LC[4:3] = 10b	-10%	21.1	+10%	kHz

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 14 V,
Mux Rate = 128,
C_B = 2.2 μF,
All HV outputs are open circuit.

Bias Ratio = 11,
Line Rate = 00 b,
Bus mode = 6800,
Temperature = 25°C,

PM = 78,
Panel Loading (PC[1:0]) = 10b,
C_L = 330 nF,
MTP = 00 H,

Display Pattern	Conditions	Typical	Maximum	Unit
All-OFF	Bus = idle	435	653	μA
2-pixel checker	Bus = idle	462	693	μA
-	Reset (standby current)	< 1	5	μA

AC CHARACTERISTICS

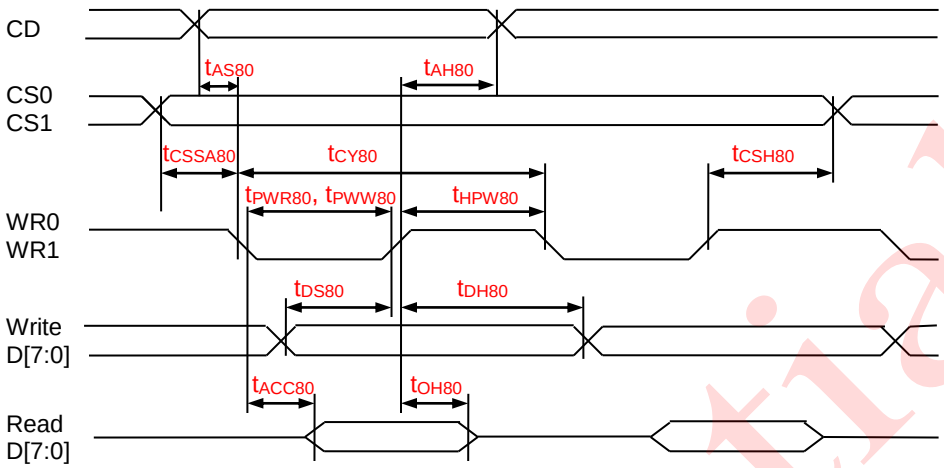


FIGURE 14: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
$t_{AS}80$ $t_{AH}80$	CD	Address setup time Address hold time		0 0	–	nS
$t_{CSSA}80$ $t_{CSH}80$	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
$t_{CY}80$ $t_{PWR}80$ / $t_{PWW}80$ $t_{HPW}80$	WR0, WR1	System cycle time Pulse width High pulse width		200 / 160 85 / 65 85 / 65	–	nS
$t_{DS}80$ $t_{DH}80$	D7~D0 (Write)	Data setup time Data hold time		– / 30 – / 0	–	nS
$t_{ACC}80$ $t_{OH}80$	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / – – / –	65 / – 30 / –	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
$t_{AS}80$ $t_{AH}80$	CD	Address setup time Address hold time		0 0	–	nS
$t_{CSSA}80$ $t_{CSH}80$	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS
$t_{CY}80$ $t_{PWR}80$ / $t_{PWW}80$ $t_{HPW}80$	WR0, WR1	System cycle time Pulse width High pulse width		350 / 300 160 / 135 160 / 135	–	nS
$t_{DS}80$ $t_{DH}80$	D7~D0 (Write)	Data setup time Data hold time		– / 60 – / 0	–	nS
$t_{ACC}80$ $t_{OH}80$	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / – – / –	120 / – 60 / –	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

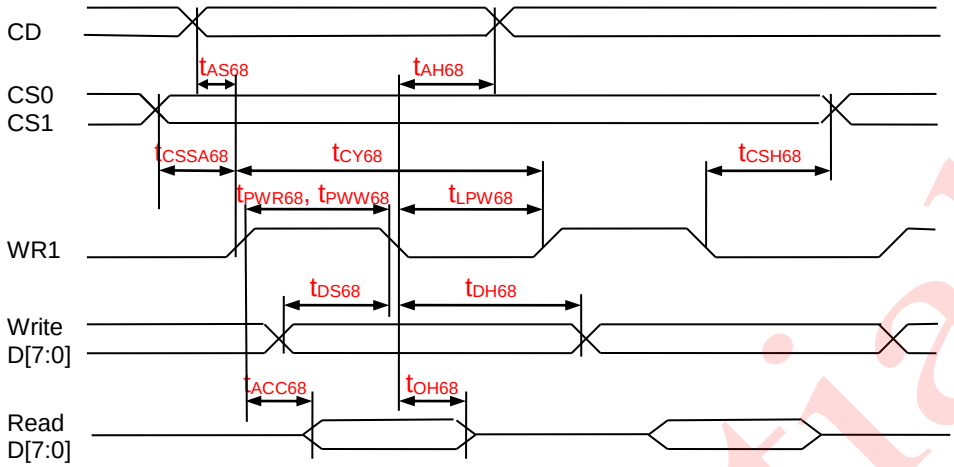


FIGURE 15: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY68} t_{PWR68} / t_{PWW68} t_{LPW68}	WR1	System cycle time Pulse width Low pulse width		200 / 160 85 / 65 85 / 65	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		– / 30 – / 0	–	nS
t_{ACC68} t_{OH68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / – – / –	70 / – 30 / –	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		10 10	–	nS
t_{CY68} t_{PWR68} / t_{PWW68} t_{LPW68}	WR1	System cycle time Pulse width Low pulse width		350 / 300 160 / 135 160 / 135	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		– / 60 – / 0	–	nS
t_{ACC68} t_{OH68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / – – / –	120 / – 60 / –	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

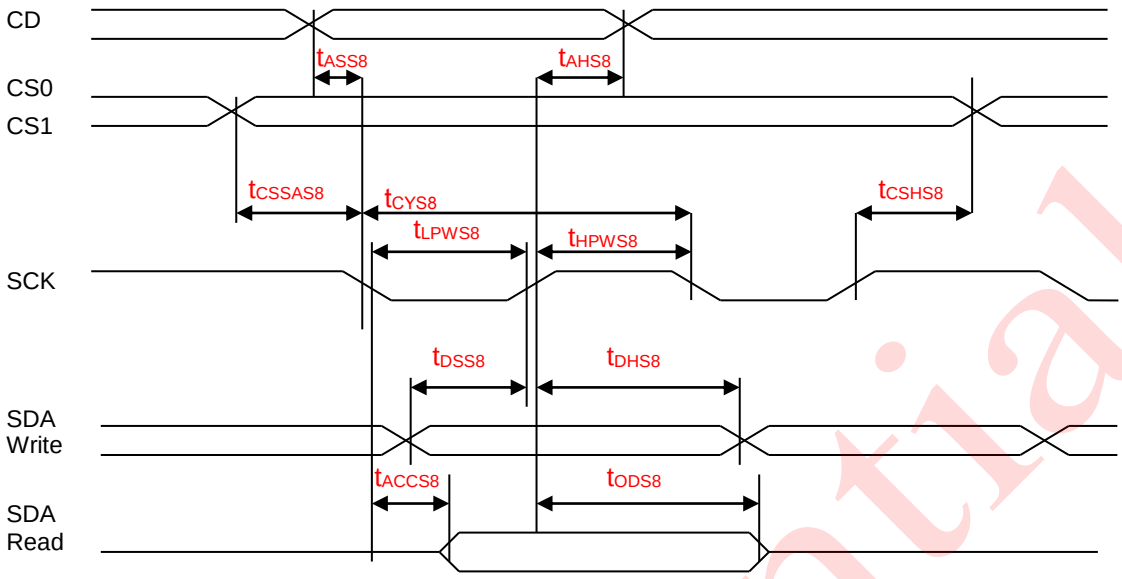


FIGURE 16: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)	(Read / Write)	
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		– / 0 – / 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 / 5 5 / 5	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System cycle time Low pulse width High pulse width		140 / 65 55 / 17 55 / 17	–	nS
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		– / 15 – / 5	–	nS
t_{ACCS8} t_{ODS8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / -- N/A / --	50 / -- N/A / --	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)	(Read / Write)	
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		– / 0 – / 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 / 10 10 / 10	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	System cycle time Low pulse width High pulse width		215 / 90 92 / 30 92 / 30	–	nS
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		– / 24 – / 5	–	nS
t_{ACCS8} t_{ODS8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / -- N/A / --	90 / – N/A / –	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

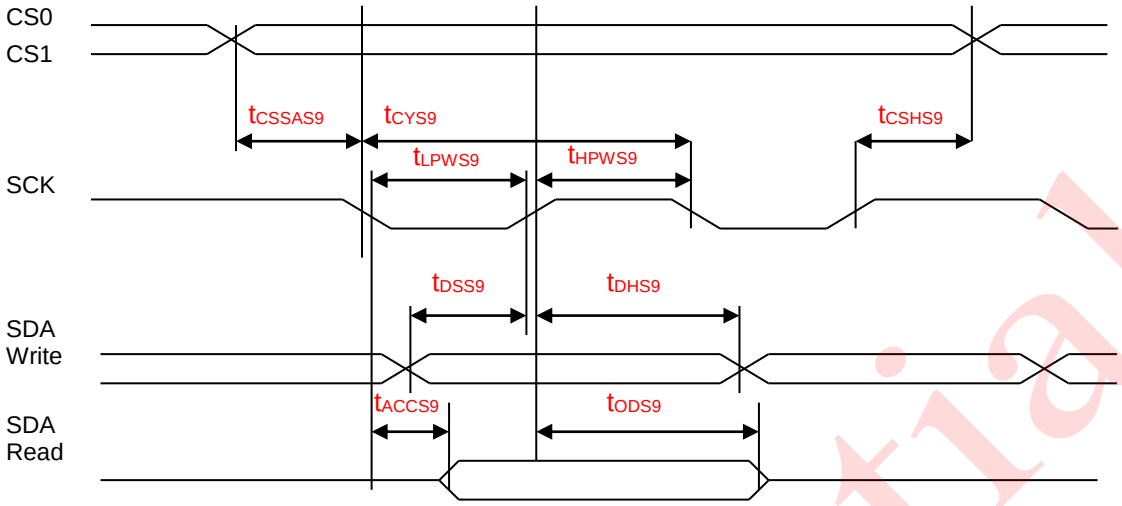


FIGURE 17: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		5 / 5 5 / 5	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		140 / 65 55 / 17 55 / 17	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		– / 15 – / 5	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / – N/A / –	50 / – N/A / –	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 / 10 10 / 10	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	System cycle time Low pulse width High pulse width		215 / 90 92 / 30 92 / 30	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		– / 24 – / 5	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / – N/A / –	90 / – N/A / –	nS

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

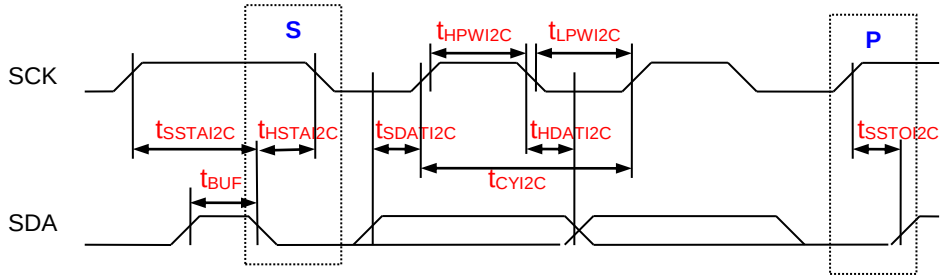


FIGURE 18: Serial bus timing characteristics (for I^2C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ⩽ V_{DD} < 3.465V, Ta= –30 to +85°C)				(Read / Write)		
tCYI2C	SCK	SCK cycle time		610 / 305	–	nS
tLPWI2C		Low pulse width		290 / 137		
tHPWI2C		High pulse width		290 / 137		
t_r, t_f	SCK SDA	Rise time and fall time		–	–	nS
tSSDAI2C		Data setup time		28		
tHDAI2C		Data hold time		11		
tSSTAI2C		START Setup time		28		
tHSTAI2C		START Hold time		28		
tSSTOI2C		STOP setup time		28		
tBUF		Bus free time between stop and start condition		165		
(1.65V ⩽ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
tCYI2C	SCK	SCK cycle time		780 / 360	–	nS
tLPWI2C		Low pulse width		375 / 165		
tHPWI2C		High pulse width		375 / 165		
t_r, t_f	SCK SDA	Rise time and fall time		–	–	nS
tSSDAI2C		Data setup time		55		
tHDAI2C		Data hold time		11		
tSSTAI2C		START Setup time		28		
tHSTAI2C		START Hold time		60		
tSSTOI2C		STOP setup time		28		
tBUF		Bus free time between stop and start condition		220		

Note: The rising time (tr) and the falling time (tf) are stipulated to be equal to or less than 15nS each.

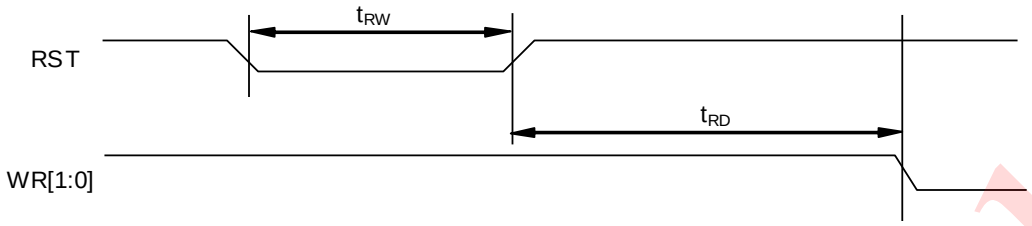


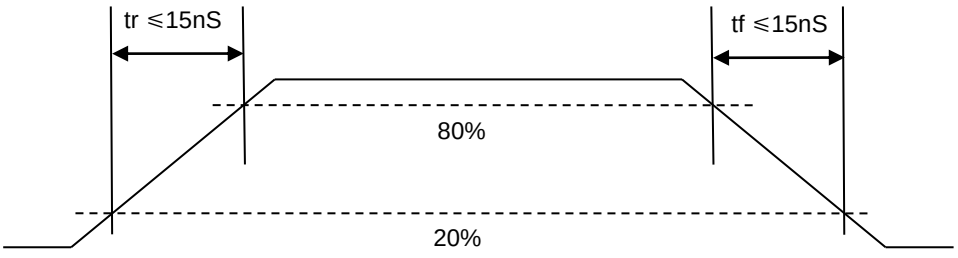
FIGURE 19: Reset Characteristics

(1.65V ≤ V_{DD} < 3.465V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
tRW	RST	Reset low pulse width		3	–	µS
tRD	RST, WR	Reset to WR pulse delay		10	–	mS

Note:

For each mode, the signal's rising time (tr) and falling time (tf) are stipulated to be equal to or less than 15nS each.



PHYSICAL DIMENSIONS

PAD COORDINATES

DIE SIZE:
6582 x 870 ± 40 μM²

DIE THICKNESS:
400 ± 20 μM

BUMP HEIGHT:
12μM ± 3μM
(H_{MAX} - H_{MIN}) within die ⩽ 2 μM

BUMP SIZE:
104 x 14.5 μM² (Typ.)

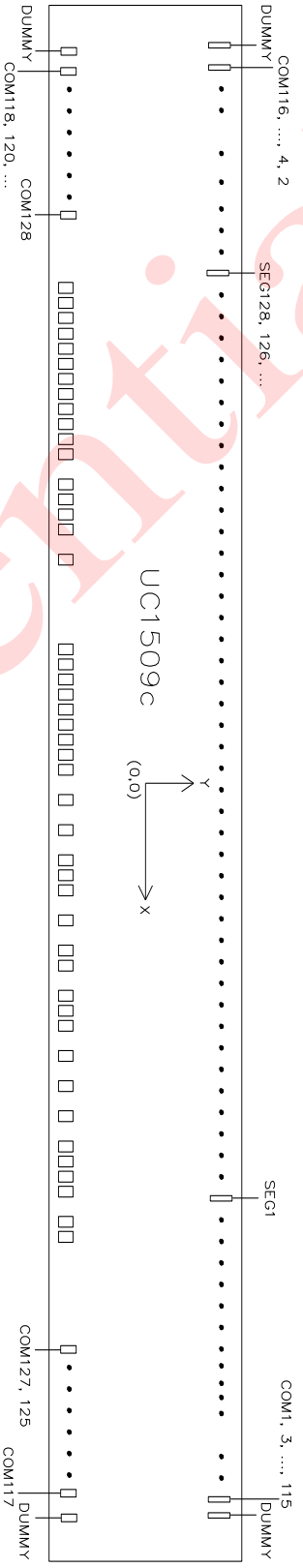
BUMP PITCH:
26.5 μM

BUMP GAP:
12 μM (Typ.)

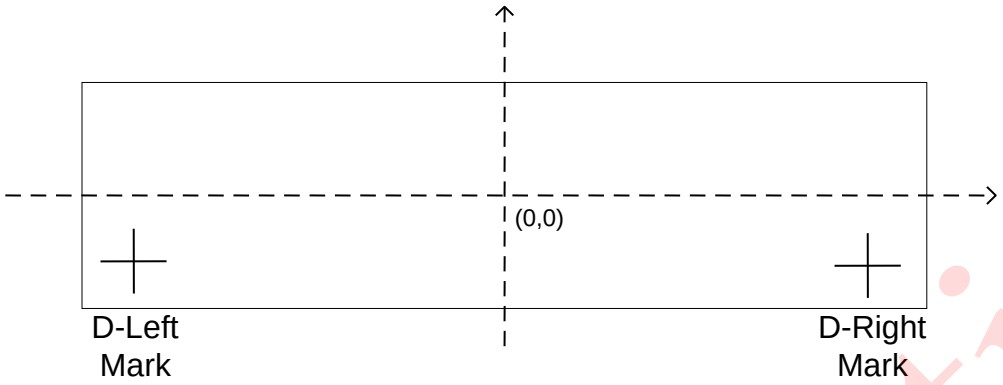
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

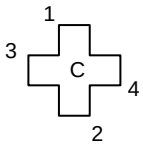
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

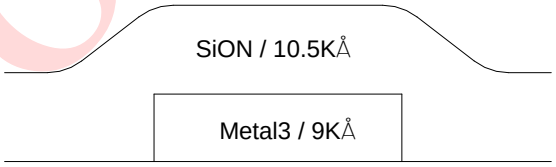
Alignment mark is on Metal3 under Passivation.

The “x” and “+” marks are symmetric both horizontally and vertically.

COORDINATES:

	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-3024	-332.5	3004	-332.5
2	-3004	-392.5	3024	-392.5
3	-3044	-352.5	2984	-352.5
4	-2984	-372.5	3044	-372.5
C	-3014	-362.5	3014	-362.5

TOP METAL AND PASSIVATION:



FOR MTP PROCESS CROSS-SECTION

PAD COORDINATES

#	Pad	X	Y	W	H
1	DUMMY2	-3246.25	-348.5	14.5	104
2	COM_pad<118>	-3219.75	-348.5	14.5	104
3	COM_pad<120>	-3193.25	-348.5	14.5	104
4	COM_pad<122>	-3166.75	-348.5	14.5	104
5	COM_pad<124>	-3140.25	-348.5	14.5	104
6	COM_pad<126>	-3113.75	-348.5	14.5	104
7	COM_pad<128>	-3087.25	-348.5	14.5	104
8	D0	-2923.95	-349.5	70	100
9	D1	-2838.85	-349.5	70	100
10	D2	-2753.75	-349.5	70	100
11	D3	-2668.65	-349.5	70	100
12	D4	-2583.55	-349.5	70	100
13	D5	-2498.45	-349.5	70	100
14	D6	-2413.35	-349.5	70	100
15	VDDX	-2341.8	-349.5	25	100
16	D7	-2270.25	-349.5	70	100
17	RST_	-2179.9	-349.5	66.5	100
18	CS0	-2098.3	-349.5	66.5	100
19	VDDX	-2028.5	-349.5	25	100
20	CS1	-1958.7	-349.5	66.5	100
21	CD	-1877.1	-349.5	66.5	100
22	WR0	-1795.5	-349.5	66.5	100
23	VDDX	-1725.7	-349.5	25	100
24	WR1	-1655.9	-349.5	66.5	100
25	TST4	-1576.1	-349.5	45	100
26	TST4	-1516.1	-349.5	45	100
27	TST1	-1080.225	-349.5	45	100
28	BM<0>	-1000.3	-349.5	66.5	100
29	VDDX	-930.5	-349.5	25	100
30	BM<1>	-860.7	-349.5	66.5	100
31	TST2	-780.025	-349.5	45	100
32	ID	-604.575	-349.5	66.5	100
33	VDDX	-524.775	-349.5	45	100
34	VSS	-464.775	-349.5	45	100
35	VSS	-404.775	-349.5	45	100
36	VSS	-344.775	-349.5	45	100
37	VSS	-284.775	-349.5	45	100
38	VSS2	-111.775	-349.5	45	100
39	VSS2	-51.775	-349.5	45	100
40	VSS2	8.225	-349.5	45	100
41	VSS2	68.225	-349.5	45	100
42	VSS2	128.225	-349.5	45	100
43	VDD3	188.225	-349.5	45	100
44	DUMMY5	366.575	-349.5	51	100
45	VDD2	453.075	-349.5	45	100
46	VDD2	513.075	-349.5	45	100
47	DUMMY6	678	-349.5	51	100
48	DUMMY7	744	-349.5	51	100
49	DUMMY8	810	-349.5	51	100
50	DUMMY9	876	-349.5	51	100
51	DUMMY10	942	-349.5	51	100
52	DUMMY11	1008	-349.5	51	100
53	DUMMY12	1074	-349.5	51	100
54	DUMMY13	1140	-349.5	51	100
55	VDD	1304.925	-349.5	45	100
56	VB0P	1412.1	-349.5	45	100
57	VB0P	1472.1	-349.5	45	100

#	Pad	X	Y	W	H
58	VB1P	1688.6	-349.5	45	100
59	VB1P	1748.6	-349.5	45	100
60	VB1N	2103.6	-349.5	45	100
61	VB1N	2163.6	-349.5	45	100
62	VB0N	2379.3	-349.5	45	100
63	VB0N	2439.3	-349.5	45	100
64	VLCDIN	2655	-349.5	45	100
65	VLCDOUT	2715	-349.5	45	100
66	COM_pad<127>	3087.25	-348.5	14.5	104
67	COM_pad<125>	3113.75	-348.5	14.5	104
68	COM_pad<123>	3140.25	-348.5	14.5	104
69	COM_pad<121>	3166.75	-348.5	14.5	104
70	COM_pad<119>	3193.25	-348.5	14.5	104
71	COM_pad<117>	3219.75	-348.5	14.5	104
72	DUMMY3	3246.25	-348.5	14.5	104
73	DUMMY4	3246.25	348.5	14.5	104
74	COM_pad<115>	3219.75	348.5	14.5	104
75	COM_pad<113>	3193.25	348.5	14.5	104
76	COM_pad<111>	3166.75	348.5	14.5	104
77	COM_pad<109>	3140.25	348.5	14.5	104
78	COM_pad<107>	3113.75	348.5	14.5	104
79	COM_pad<105>	3087.25	348.5	14.5	104
80	COM_pad<103>	3060.75	348.5	14.5	104
81	COM_pad<101>	3034.25	348.5	14.5	104
82	COM_pad<99>	3007.75	348.5	14.5	104
83	COM_pad<97>	2981.25	348.5	14.5	104
84	COM_pad<95>	2954.75	348.5	14.5	104
85	COM_pad<93>	2928.25	348.5	14.5	104
86	COM_pad<91>	2901.75	348.5	14.5	104
87	COM_pad<89>	2875.25	348.5	14.5	104
88	COM_pad<87>	2848.75	348.5	14.5	104
89	COM_pad<85>	2822.25	348.5	14.5	104
90	COM_pad<83>	2795.75	348.5	14.5	104
91	COM_pad<81>	2769.25	348.5	14.5	104
92	COM_pad<79>	2742.75	348.5	14.5	104
93	COM_pad<77>	2716.25	348.5	14.5	104
94	COM_pad<75>	2689.75	348.5	14.5	104
95	COM_pad<73>	2663.25	348.5	14.5	104
96	COM_pad<71>	2636.75	348.5	14.5	104
97	COM_pad<69>	2610.25	348.5	14.5	104
98	COM_pad<67>	2583.75	348.5	14.5	104
99	COM_pad<65>	2557.25	348.5	14.5	104
100	COM_pad<63>	2530.75	348.5	14.5	104
101	COM_pad<61>	2504.25	348.5	14.5	104
102	COM_pad<59>	2477.75	348.5	14.5	104
103	COM_pad<57>	2451.25	348.5	14.5	104
104	COM_pad<55>	2424.75	348.5	14.5	104
105	COM_pad<53>	2398.25	348.5	14.5	104
106	COM_pad<51>	2371.75	348.5	14.5	104
107	COM_pad<49>	2345.25	348.5	14.5	104
108	COM_pad<47>	2318.75	348.5	14.5	104
109	COM_pad<45>	2292.25	348.5	14.5	104
110	COM_pad<43>	2265.75	348.5	14.5	104
111	COM_pad<41>	2239.25	348.5	14.5	104
112	COM_pad<39>	2212.75	348.5	14.5	104
113	COM_pad<37>	2186.25	348.5	14.5	104
114	COM_pad<35>	2159.75	348.5	14.5	104

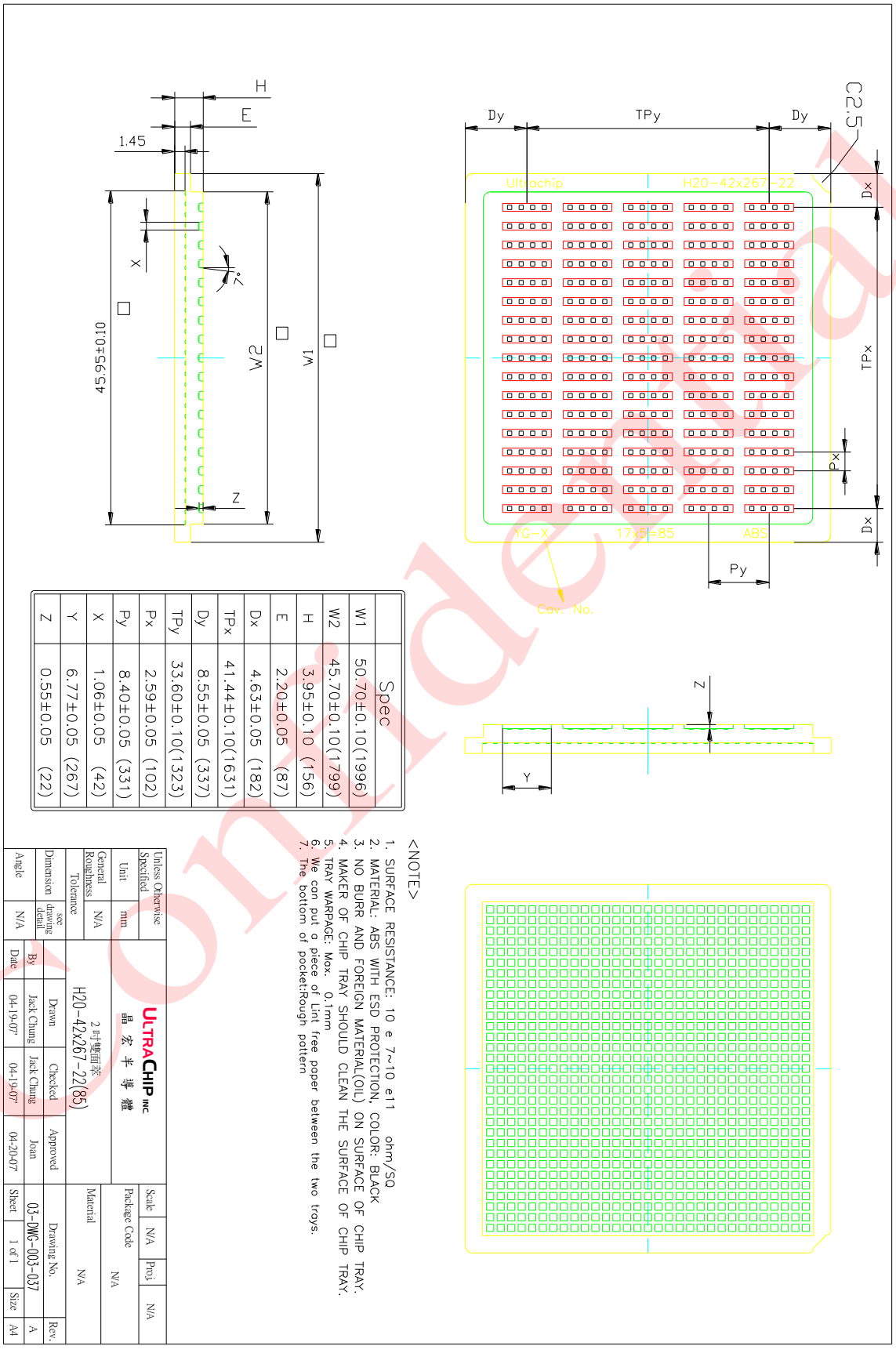
#	Pad	X	Y	W	H
115	COM_pad<33>	2133.25	348.5	14.5	104
116	COM_pad<31>	2106.75	348.5	14.5	104
117	COM_pad<29>	2080.25	348.5	14.5	104
118	COM_pad<27>	2053.75	348.5	14.5	104
119	COM_pad<25>	2027.25	348.5	14.5	104
120	COM_pad<23>	2000.75	348.5	14.5	104
121	COM_pad<21>	1974.25	348.5	14.5	104
122	COM_pad<19>	1947.75	348.5	14.5	104
123	COM_pad<17>	1921.25	348.5	14.5	104
124	COM_pad<15>	1894.75	348.5	14.5	104
125	COM_pad<13>	1868.25	348.5	14.5	104
126	COM_pad<11>	1841.75	348.5	14.5	104
127	COM_pad<9>	1815.25	348.5	14.5	104
128	COM_pad<7>	1788.75	348.5	14.5	104
129	COM_pad<5>	1762.25	348.5	14.5	104
130	COM_pad<3>	1735.75	348.5	14.5	104
131	COM_pad<1>	1709.25	348.5	14.5	104
132	SEG_pad<1>	1682.75	348.5	14.5	104
133	SEG_pad<2>	1656.25	348.5	14.5	104
134	SEG_pad<3>	1629.75	348.5	14.5	104
135	SEG_pad<4>	1603.25	348.5	14.5	104
136	SEG_pad<5>	1576.75	348.5	14.5	104
137	SEG_pad<6>	1550.25	348.5	14.5	104
138	SEG_pad<7>	1523.75	348.5	14.5	104
139	SEG_pad<8>	1497.25	348.5	14.5	104
140	SEG_pad<9>	1470.75	348.5	14.5	104
141	SEG_pad<10>	1444.25	348.5	14.5	104
142	SEG_pad<11>	1417.75	348.5	14.5	104
143	SEG_pad<12>	1391.25	348.5	14.5	104
144	SEG_pad<13>	1364.75	348.5	14.5	104
145	SEG_pad<14>	1338.25	348.5	14.5	104
146	SEG_pad<15>	1311.75	348.5	14.5	104
147	SEG_pad<16>	1285.25	348.5	14.5	104
148	SEG_pad<17>	1258.75	348.5	14.5	104
149	SEG_pad<18>	1232.25	348.5	14.5	104
150	SEG_pad<19>	1205.75	348.5	14.5	104
151	SEG_pad<20>	1179.25	348.5	14.5	104
152	SEG_pad<21>	1152.75	348.5	14.5	104
153	SEG_pad<22>	1126.25	348.5	14.5	104
154	SEG_pad<23>	1099.75	348.5	14.5	104
155	SEG_pad<24>	1073.25	348.5	14.5	104
156	SEG_pad<25>	1046.75	348.5	14.5	104
157	SEG_pad<26>	1020.25	348.5	14.5	104
158	SEG_pad<27>	993.75	348.5	14.5	104
159	SEG_pad<28>	967.25	348.5	14.5	104
160	SEG_pad<29>	940.75	348.5	14.5	104
161	SEG_pad<30>	914.25	348.5	14.5	104
162	SEG_pad<31>	887.75	348.5	14.5	104
163	SEG_pad<32>	861.25	348.5	14.5	104
164	SEG_pad<33>	834.75	348.5	14.5	104
165	SEG_pad<34>	808.25	348.5	14.5	104
166	SEG_pad<35>	781.75	348.5	14.5	104
167	SEG_pad<36>	755.25	348.5	14.5	104
168	SEG_pad<37>	728.75	348.5	14.5	104
169	SEG_pad<38>	702.25	348.5	14.5	104
170	SEG_pad<39>	675.75	348.5	14.5	104
171	SEG_pad<40>	649.25	348.5	14.5	104
172	SEG_pad<41>	622.75	348.5	14.5	104
173	SEG_pad<42>	596.25	348.5	14.5	104

#	Pad	X	Y	W	H
174	SEG_pad<43>	569.75	348.5	14.5	104
175	SEG_pad<44>	543.25	348.5	14.5	104
176	SEG_pad<45>	516.75	348.5	14.5	104
177	SEG_pad<46>	490.25	348.5	14.5	104
178	SEG_pad<47>	463.75	348.5	14.5	104
179	SEG_pad<48>	437.25	348.5	14.5	104
180	SEG_pad<49>	410.75	348.5	14.5	104
181	SEG_pad<50>	384.25	348.5	14.5	104
182	SEG_pad<51>	357.75	348.5	14.5	104
183	SEG_pad<52>	331.25	348.5	14.5	104
184	SEG_pad<53>	304.75	348.5	14.5	104
185	SEG_pad<54>	278.25	348.5	14.5	104
186	SEG_pad<55>	251.75	348.5	14.5	104
187	SEG_pad<56>	225.25	348.5	14.5	104
188	SEG_pad<57>	198.75	348.5	14.5	104
189	SEG_pad<58>	172.25	348.5	14.5	104
190	SEG_pad<59>	145.75	348.5	14.5	104
191	SEG_pad<60>	119.25	348.5	14.5	104
192	SEG_pad<61>	92.75	348.5	14.5	104
193	SEG_pad<62>	66.25	348.5	14.5	104
194	SEG_pad<63>	39.75	348.5	14.5	104
195	SEG_pad<64>	13.25	348.5	14.5	104
196	SEG_pad<65>	-13.25	348.5	14.5	104
197	SEG_pad<66>	-39.75	348.5	14.5	104
198	SEG_pad<67>	-66.25	348.5	14.5	104
199	SEG_pad<68>	-92.75	348.5	14.5	104
200	SEG_pad<69>	-119.25	348.5	14.5	104
201	SEG_pad<70>	-145.75	348.5	14.5	104
202	SEG_pad<71>	-172.25	348.5	14.5	104
203	SEG_pad<72>	-198.75	348.5	14.5	104
204	SEG_pad<73>	-225.25	348.5	14.5	104
205	SEG_pad<74>	-251.75	348.5	14.5	104
206	SEG_pad<75>	-278.25	348.5	14.5	104
207	SEG_pad<76>	-304.75	348.5	14.5	104
208	SEG_pad<77>	-331.25	348.5	14.5	104
209	SEG_pad<78>	-357.75	348.5	14.5	104
210	SEG_pad<79>	-384.25	348.5	14.5	104
211	SEG_pad<80>	-410.75	348.5	14.5	104
212	SEG_pad<81>	-437.25	348.5	14.5	104
213	SEG_pad<82>	-463.75	348.5	14.5	104
214	SEG_pad<83>	-490.25	348.5	14.5	104
215	SEG_pad<84>	-516.75	348.5	14.5	104
216	SEG_pad<85>	-543.25	348.5	14.5	104
217	SEG_pad<86>	-569.75	348.5	14.5	104
218	SEG_pad<87>	-596.25	348.5	14.5	104
219	SEG_pad<88>	-622.75	348.5	14.5	104
220	SEG_pad<89>	-649.25	348.5	14.5	104
221	SEG_pad<90>	-675.75	348.5	14.5	104
222	SEG_pad<91>	-702.25	348.5	14.5	104
223	SEG_pad<92>	-728.75	348.5	14.5	104
224	SEG_pad<93>	-755.25	348.5	14.5	104
225	SEG_pad<94>	-781.75	348.5	14.5	104
226	SEG_pad<95>	-808.25	348.5	14.5	104
227	SEG_pad<96>	-834.75	348.5	14.5	104
228	SEG_pad<97>	-861.25	348.5	14.5	104
229	SEG_pad<98>	-887.75	348.5	14.5	104
230	SEG_pad<99>	-914.25	348.5	14.5	104
231	SEG_pad<100>	-940.75	348.5	14.5	104
232	SEG_pad<101>	-967.25	348.5	14.5	104

#	Pad	X	Y	W	H
233	SEG_pad<102>	-993.75	348.5	14.5	104
234	SEG_pad<103>	-1020.25	348.5	14.5	104
235	SEG_pad<104>	-1046.75	348.5	14.5	104
236	SEG_pad<105>	-1073.25	348.5	14.5	104
237	SEG_pad<106>	-1099.75	348.5	14.5	104
238	SEG_pad<107>	-1126.25	348.5	14.5	104
239	SEG_pad<108>	-1152.75	348.5	14.5	104
240	SEG_pad<109>	-1179.25	348.5	14.5	104
241	SEG_pad<110>	-1205.75	348.5	14.5	104
242	SEG_pad<111>	-1232.25	348.5	14.5	104
243	SEG_pad<112>	-1258.75	348.5	14.5	104
244	SEG_pad<113>	-1285.25	348.5	14.5	104
245	SEG_pad<114>	-1311.75	348.5	14.5	104
246	SEG_pad<115>	-1338.25	348.5	14.5	104
247	SEG_pad<116>	-1364.75	348.5	14.5	104
248	SEG_pad<117>	-1391.25	348.5	14.5	104
249	SEG_pad<118>	-1417.75	348.5	14.5	104
250	SEG_pad<119>	-1444.25	348.5	14.5	104
251	SEG_pad<120>	-1470.75	348.5	14.5	104
252	SEG_pad<121>	-1497.25	348.5	14.5	104
253	SEG_pad<122>	-1523.75	348.5	14.5	104
254	SEG_pad<123>	-1550.25	348.5	14.5	104
255	SEG_pad<124>	-1576.75	348.5	14.5	104
256	SEG_pad<125>	-1603.25	348.5	14.5	104
257	SEG_pad<126>	-1629.75	348.5	14.5	104
258	SEG_pad<127>	-1656.25	348.5	14.5	104
259	SEG_pad<128>	-1682.75	348.5	14.5	104
260	COM_pad<2>	-1709.25	348.5	14.5	104
261	COM_pad<4>	-1735.75	348.5	14.5	104
262	COM_pad<6>	-1762.25	348.5	14.5	104
263	COM_pad<8>	-1788.75	348.5	14.5	104
264	COM_pad<10>	-1815.25	348.5	14.5	104
265	COM_pad<12>	-1841.75	348.5	14.5	104
266	COM_pad<14>	-1868.25	348.5	14.5	104
267	COM_pad<16>	-1894.75	348.5	14.5	104
268	COM_pad<18>	-1921.25	348.5	14.5	104
269	COM_pad<20>	-1947.75	348.5	14.5	104
270	COM_pad<22>	-1974.25	348.5	14.5	104
271	COM_pad<24>	-2000.75	348.5	14.5	104
272	COM_pad<26>	-2027.25	348.5	14.5	104
273	COM_pad<28>	-2053.75	348.5	14.5	104
274	COM_pad<30>	-2080.25	348.5	14.5	104
275	COM_pad<32>	-2106.75	348.5	14.5	104
276	COM_pad<34>	-2133.25	348.5	14.5	104
277	COM_pad<36>	-2159.75	348.5	14.5	104
278	COM_pad<38>	-2186.25	348.5	14.5	104
279	COM_pad<40>	-2212.75	348.5	14.5	104
280	COM_pad<42>	-2239.25	348.5	14.5	104
281	COM_pad<44>	-2265.75	348.5	14.5	104
282	COM_pad<46>	-2292.25	348.5	14.5	104
283	COM_pad<48>	-2318.75	348.5	14.5	104
284	COM_pad<50>	-2345.25	348.5	14.5	104
285	COM_pad<52>	-2371.75	348.5	14.5	104
286	COM_pad<54>	-2398.25	348.5	14.5	104
287	COM_pad<56>	-2424.75	348.5	14.5	104
288	COM_pad<58>	-2451.25	348.5	14.5	104

#	Pad	X	Y	W	H
289	COM_pad<60>	-2477.75	348.5	14.5	104
290	COM_pad<62>	-2504.25	348.5	14.5	104
291	COM_pad<64>	-2530.75	348.5	14.5	104
292	COM_pad<66>	-2557.25	348.5	14.5	104
293	COM_pad<68>	-2583.75	348.5	14.5	104
294	COM_pad<70>	-2610.25	348.5	14.5	104
295	COM_pad<72>	-2636.75	348.5	14.5	104
296	COM_pad<74>	-2663.25	348.5	14.5	104
297	COM_pad<76>	-2689.75	348.5	14.5	104
298	COM_pad<78>	-2716.25	348.5	14.5	104
299	COM_pad<80>	-2742.75	348.5	14.5	104
300	COM_pad<82>	-2769.25	348.5	14.5	104
301	COM_pad<84>	-2795.75	348.5	14.5	104
302	COM_pad<86>	-2822.25	348.5	14.5	104
303	COM_pad<88>	-2848.75	348.5	14.5	104
304	COM_pad<90>	-2875.25	348.5	14.5	104
305	COM_pad<92>	-2901.75	348.5	14.5	104
306	COM_pad<94>	-2928.25	348.5	14.5	104
307	COM_pad<96>	-2954.75	348.5	14.5	104
308	COM_pad<98>	-2981.25	348.5	14.5	104
309	COM_pad<100>	-3007.75	348.5	14.5	104
310	COM_pad<102>	-3034.25	348.5	14.5	104
311	COM_pad<104>	-3060.75	348.5	14.5	104
312	COM_pad<106>	-3087.25	348.5	14.5	104
313	COM_pad<108>	-3113.75	348.5	14.5	104
314	COM_pad<110>	-3140.25	348.5	14.5	104
315	COM_pad<112>	-3166.75	348.5	14.5	104
316	COM_pad<114>	-3193.25	348.5	14.5	104
317	COM_pad<116>	-3219.75	348.5	14.5	104
318	DUMMY1	-3246.25	348.5	14.5	104

TRAY INFORMATION



	Spec
W1	50.70±0.10(1996)
W2	45.70±0.10(1799)
H	3.95±0.10 (156)
E	2.20±0.05 (87)
Dx	4.63±0.05 (182)
TPx	41.44±0.10(1631)
Dy	8.55±0.05 (337)
TPy	33.60±0.10(1323)
Px	2.59±0.05 (102)
Py	8.40±0.05 (331)
X	1.06±0.05 (42)
Y	6.77±0.05 (267)
Z	0.55±0.05 (22)

<NOTE>

1. SURFACE RESISTANCE: 10 e 7~10 e11 ohm/SQ
2. MATERIAL: ABS WITH ESD PROTECTION, COLOR: BLACK
3. NO BURR AND FOREIGN MATERIAL(OIL) ON SURFACE OF CHIP TRAY.
4. MAKER OF CHIP TRAY SHOULD CLEAN THE SURFACE OF CHIP TRAY.
5. TRAY WARPAGE: Max. 0.1mm
6. We can put a piece of Lint free paper between the two trays.
7. The bottom of pocketRough pattern

Unless Otherwise Specified		ULTRACHIP INC 晶宏半導體		Scale	N/A
Unit	mm	2吋雙面袋 H20-42x267-22(85)		Package Code	N/A
General Roughness	N/A			Material	N/A
Tolerance					
Dimension	see drawing detail			Drawing No.	03-DWG-003-037
Angle	N/A			Sheet	1 of 1
	By	Drawn	Checked	Approved	
Date		Jack Chung	Jack Chung	Joan	
		04-19-07'	04-19-07'	04-20-07	

Proj.	N/A
Rev.	A
Size	A4

REVISION HISTORY

Revision	Contents	Date
1.0	(First release)	Sep. 28, 2017
1.1	Added 4 Grey shade display mode	Nov. 13, 2020