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**NT7065B****40-Channel Segment / Common  
Driver For Dot Matrix LCD****Introduction**

The NT7065B is a LCD driver IC which is fabricated by low power CMOS technology. Basically this IC consists of 20 x 2 bit bi-directional shift register, 20 x 2 bit data latch and 20 x 2 bit driver. This IC can be used as common or segment driver.

**Function**

- Dot matrix LCD driver with 40 channel output.
  - Selects function to use common/segment drivers simultaneously.
  - Input / Output signal.
    - Output: 20 x 2 channel waveform for LCD driving
    - Input: Serial display date and control signal from the controller LSI.
- Bias voltage (V1-V6)

**Features**

- Display driving bias: static~1/5
- Power supply voltage: 2.7~5.5V
- Supply voltage for display: 3~10V ( $V_{LCD}=V_{DD}-V_{EE}$ )
- Interface: (Controller NT7066U, NT7070B, NT7076U)
- CMOS Process
- Bare chip available



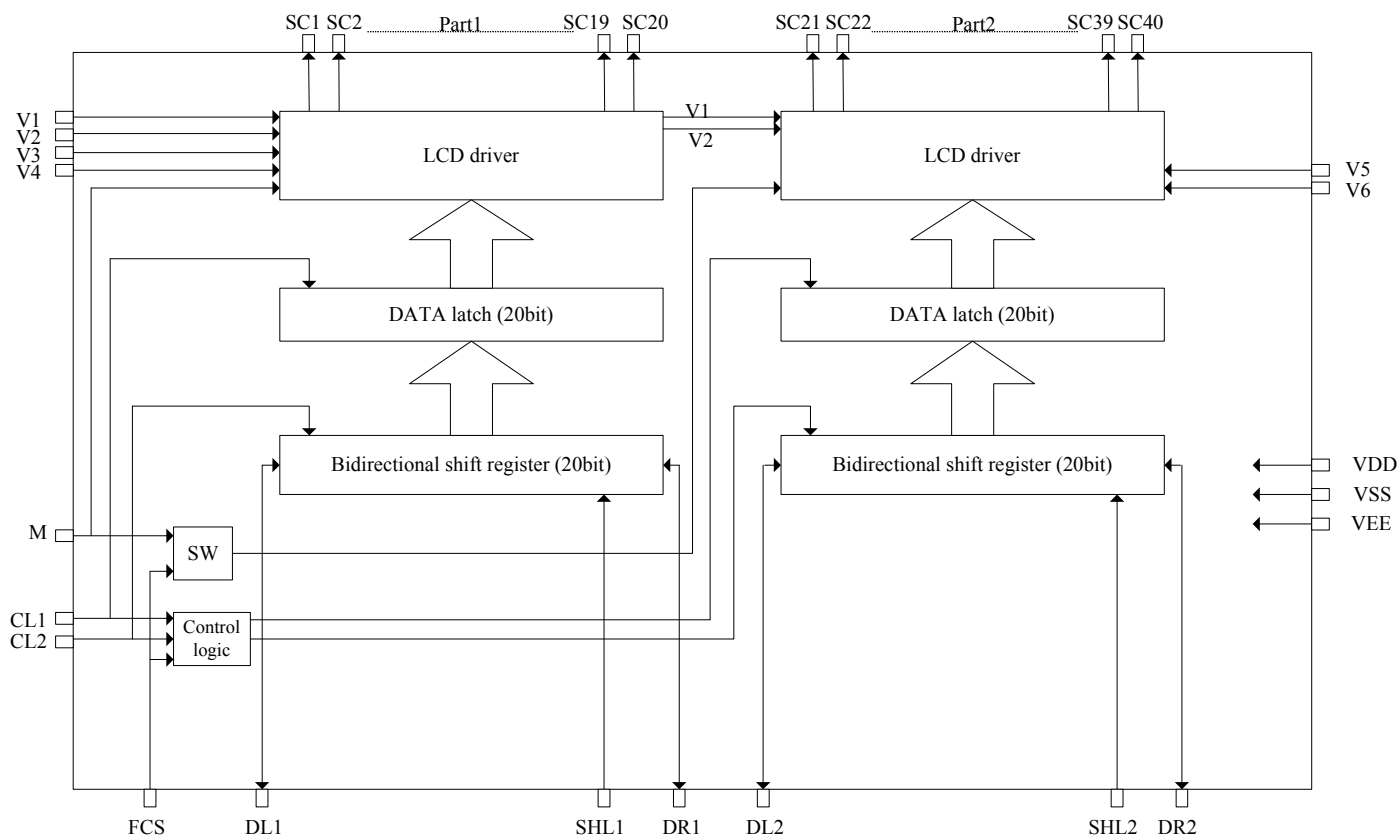
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**NT7065B**





## Block Diagram



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**NT7065B****Pin Description**

PIN	INPUT/ OUTPUT	NAME		DESCRIPTION				INTERFACE									
V <sub>DD</sub>	Power	Operating Voltage		For logical circuit (2.7~5.5V)				Power Supply									
GND				0V(GND)													
V <sub>EE</sub>		Negative Supply Voltage		For LCD driver circuit													
V1,V2	Input	Bias Voltage		Bias voltage level for LCD driver (select level)				Power									
SC1~SC20	Output	Part1	LCD Driver	LCD driver output				LCD									
V3,V4	Input		Bias Voltage	Bias voltage level for LCD drive (non-select level)				Power									
SHL1	Input		Data Interface	Selection of the shift direction of part1 shift register				V <sub>DD</sub> or GND									
				<table><tr><td>SHL1</td><td>DL1</td><td>DR1</td></tr><tr><td>V<sub>DD</sub></td><td>out</td><td>in</td></tr><tr><td>GND</td><td>in</td><td>out</td></tr></table>					SHL1	DL1	DR1	V <sub>DD</sub>	out	in	GND	in	out
				SHL1	DL1	DR1											
V <sub>DD</sub>	out	in															
GND	in	out															
Data input/output of part1 shift register																	
DL1,DR1	Input/ Output					Controller or NT7065B											
SC21~SC40	Output	Part2	LCD Driver	LCD driver output				LCD									
V5,V6	Input		Bias Voltage	Bias voltage level for LCD drive (non-select level)				Power									
SHL2	Input		Data Interface	Selection of the shift direction of part2 shift register				V <sub>DD</sub> or GND									
				<table><tr><td>SHL2</td><td>DL2</td><td>DR2</td></tr><tr><td>V<sub>DD</sub></td><td>out</td><td>in</td></tr><tr><td>GND</td><td>in</td><td>out</td></tr></table>					SHL2	DL2	DR2	V <sub>DD</sub>	out	in	GND	in	out
				SHL2	DL2	DR2											
V <sub>DD</sub>	out	in															
GND	in	out															
Data input/output of part2 shift register																	
DL2,DL2	Input/ Output					Controller or NT7065B											
M	Input	Alternated signal for LCD drive output						Controller									
CL1,CL2	Input	Data shift/latch clock															
FCS	Input	Mode selection	PART	FCS	CL1	CL2	M polarity										
				GND			M										
				V <sub>DD</sub>													
				GND			M										
V <sub>DD</sub>																	
				Shift/latch clock of display data and polarity of M signal are changed by FCS signal. By setting FCS to V <sub>DD</sub> level, user can select the function that use part1 as segment driver and part2 as common driver simultaneously.													

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**NT7065B****Maximum Absolute Limit** (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V <sub>DD</sub>	-0.3~+7.0	V
Driver supply voltage	V <sub>LCD</sub>	V <sub>DD</sub> -10.5~V <sub>DD</sub> +0.3	V
Input voltage 1	V <sub>IN1</sub>	-0.3~V <sub>DD</sub> +0.3	V
Input voltage 2 (V1~V6)	V <sub>IN2</sub>	V <sub>DD</sub> +0.3~V <sub>EE</sub> -0.3	V
Operating temperature	Topr	-30~+85	°C
Storage temperature	Tstg	-55~+125	°C

- Voltage greater than above may damage to the circuit
- VEE connect a protection resistor (220Ω±5%)

**Electrical Characteristics****DC characteristics** (V<sub>DD</sub>=2.7~5.5V, V<sub>DD</sub>-V<sub>EE</sub>=3~10V, Ta=+25°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating current*	I <sub>DD</sub>	f <sub>CL2</sub> =400KHz	-	1	mA	-
Supply current*	I <sub>EE</sub>	f <sub>CL1</sub> =1KHz	-	10	μA	
Input high voltage	V <sub>IH</sub>	-	0.7V <sub>DD</sub>	V <sub>DD</sub>	V	CL1,CL2,DL1, DL2,DR1,DR2, SHL1,SHL2,M, FCS
Input low voltage	V <sub>IL</sub>		0	0.3V <sub>DD</sub>		
Input leakage current	I <sub>LKG</sub>	V <sub>IN</sub> =0~V <sub>DD</sub>	-5	5	μA	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.4mA	V <sub>DD</sub> -0.4	-	V	DL1,DL2,DR1, DR2
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =+0.4mA	-	0.4		
Voltage descending	V <sub>D1</sub>	I <sub>ON</sub> =0.1mA for one of SC1~SC40	-	1.1		V(V1~V6)-SC( SC1~SC40)
	V <sub>D2</sub>	I <sub>ON</sub> =0.05mA for one of SC1~SC40	-	1.5		
Leakage current	I <sub>V</sub>	V <sub>IN</sub> =V <sub>DD</sub> ~V <sub>EE</sub> (output SC1~SC40 : floating)	-10	10	μA	V1~V6

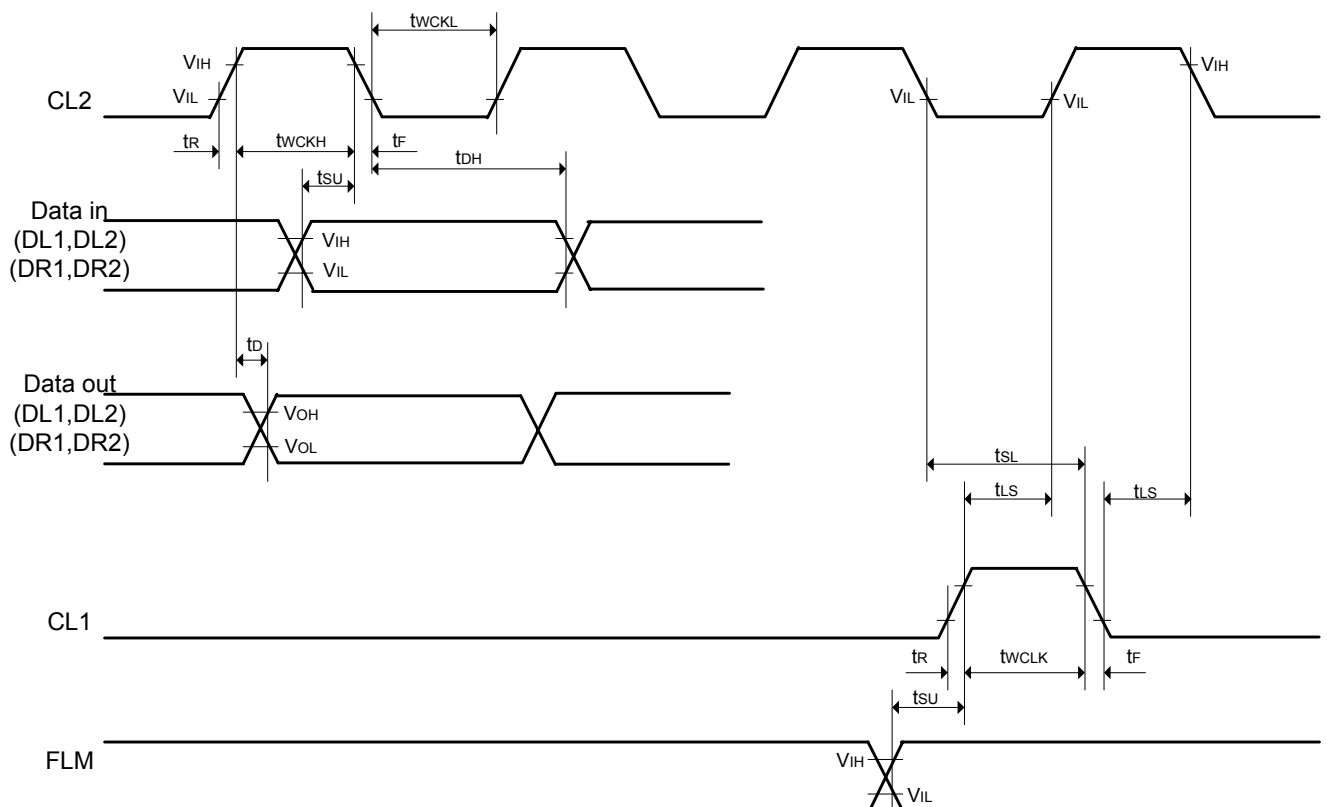
\*Input/Output current is excluded; When input at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at “H” or “L”.

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**NT7065B****AC characteristics ( $V_{DD}=2.7\sim 5.5V$ ,  $V_{DD}-V_{EE}=3\sim 10V$ ,  $T_a=+25^{\circ}C$ )**

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data shift frequency	$f_{CL}$	-	-	400	KHz	CL2
Clock high level width	$t_{WCKH}$	-	800	-	nS	CL1, CL2
Clock low level width	$t_{WCKL}$	-	800	-		CL2
Clock set-up time	$t_{SL}$	From CL2 to CL1	500	-		CL1, CL2
	$t_{LS}$	From CL1 to CL2	500	-		
Clock rise/fall time	$t_R/t_F$	-	-	200		DL1,DL2,DR1, DR2,FLM
Data set-up time	$t_{SU}$	-	300	-		
Data hold time	$t_{DH}$	-	300	-		
Data delay time	$t_D$	CL=15pF	-	500		DL1,DL2,DR1, DR2

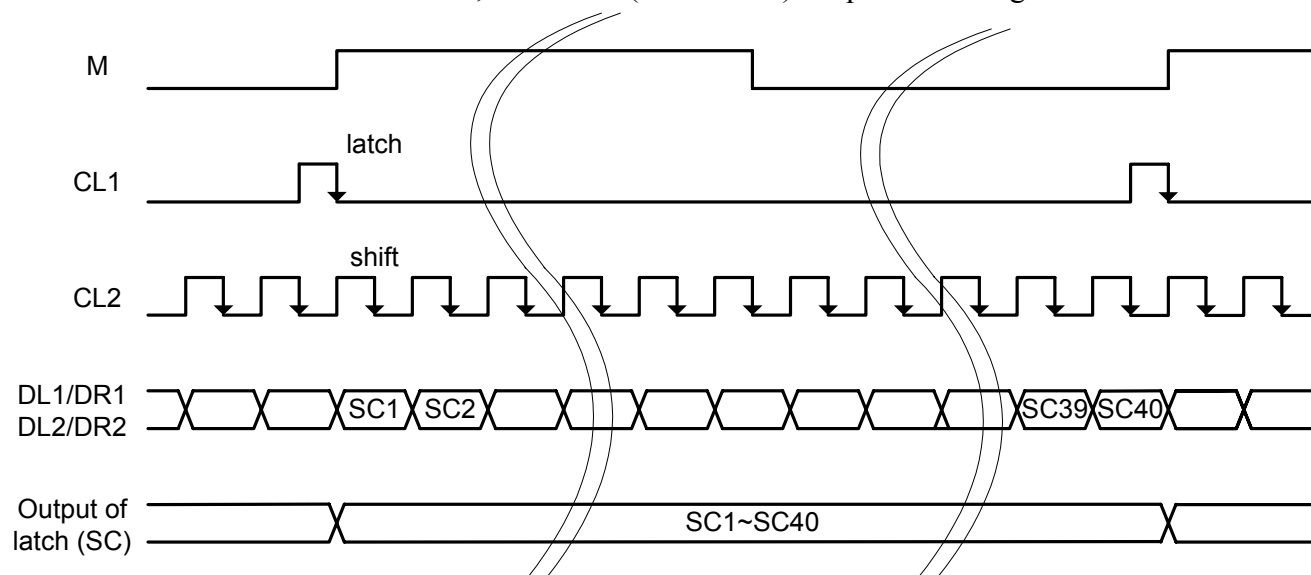
**Timing Characteristics**

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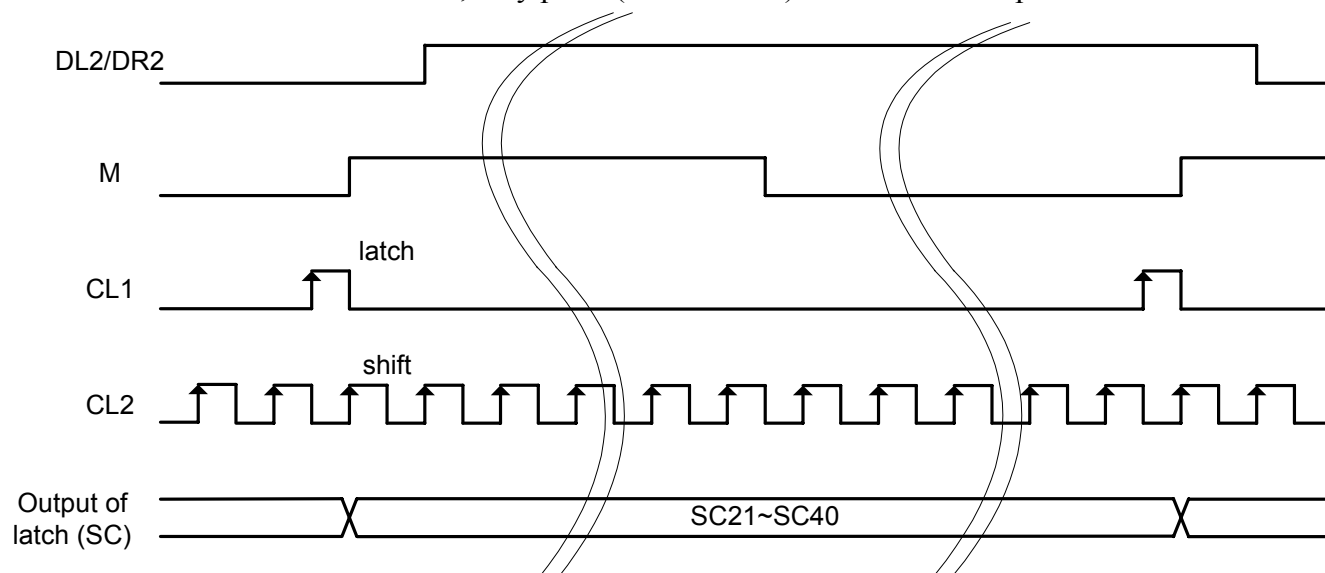
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**NT7065B****Functional Description****1) To drive segment type**

When the FCS is connected to GND, NT7065B (SC1~SC40) is operated as segment driver.

**2) To drive common type**

When the FCS is connected to  $V_{DD}$ , only part2 (SC21~SC40) of NT7065S is operated as common driver.



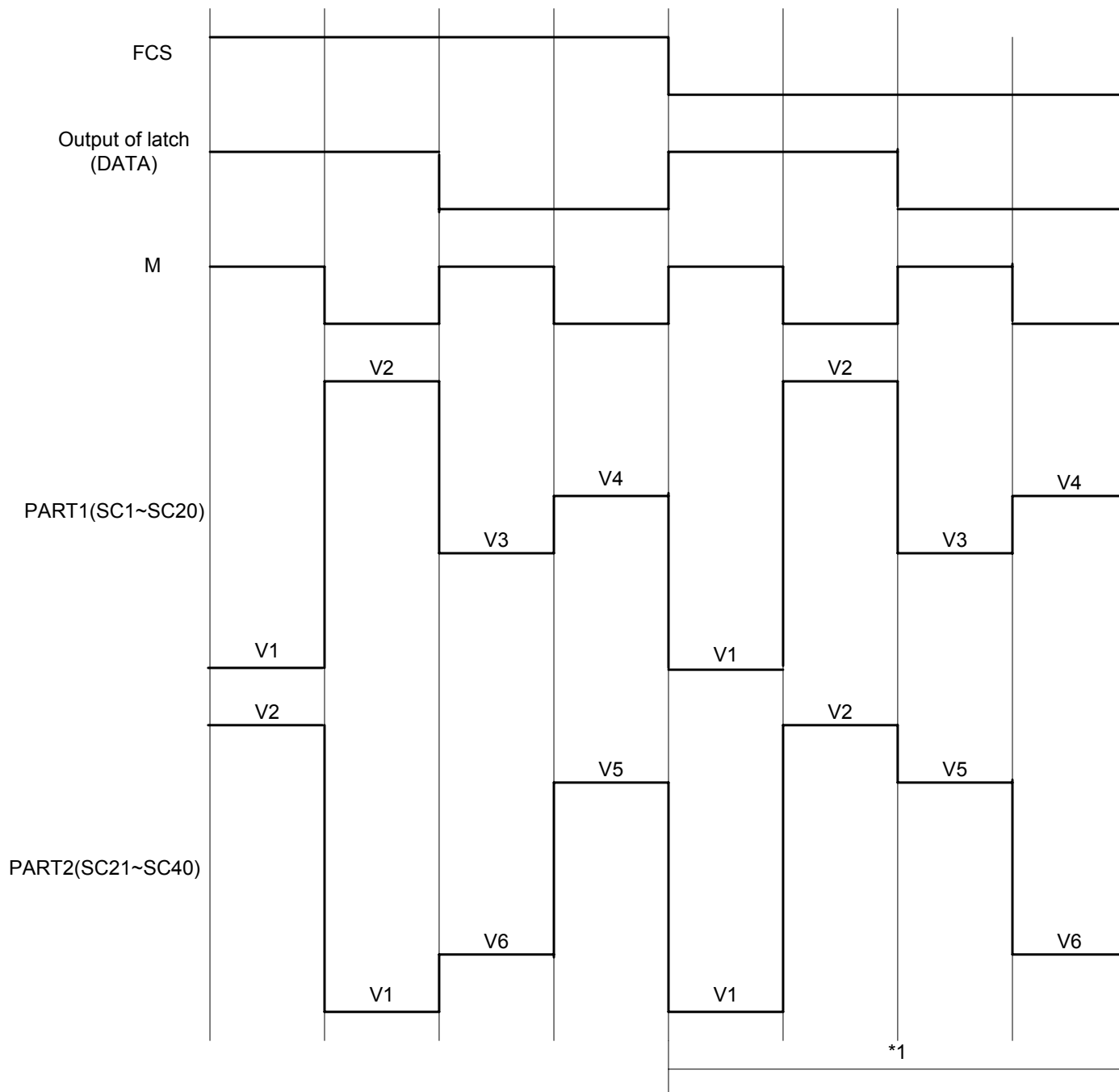
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# NT7065B

## LCD Output Waveforms



\*1: To use for same function of part1 and part2, V3 and V5, V4 and V6 of power supply for LCD driver are short circuited respectively.

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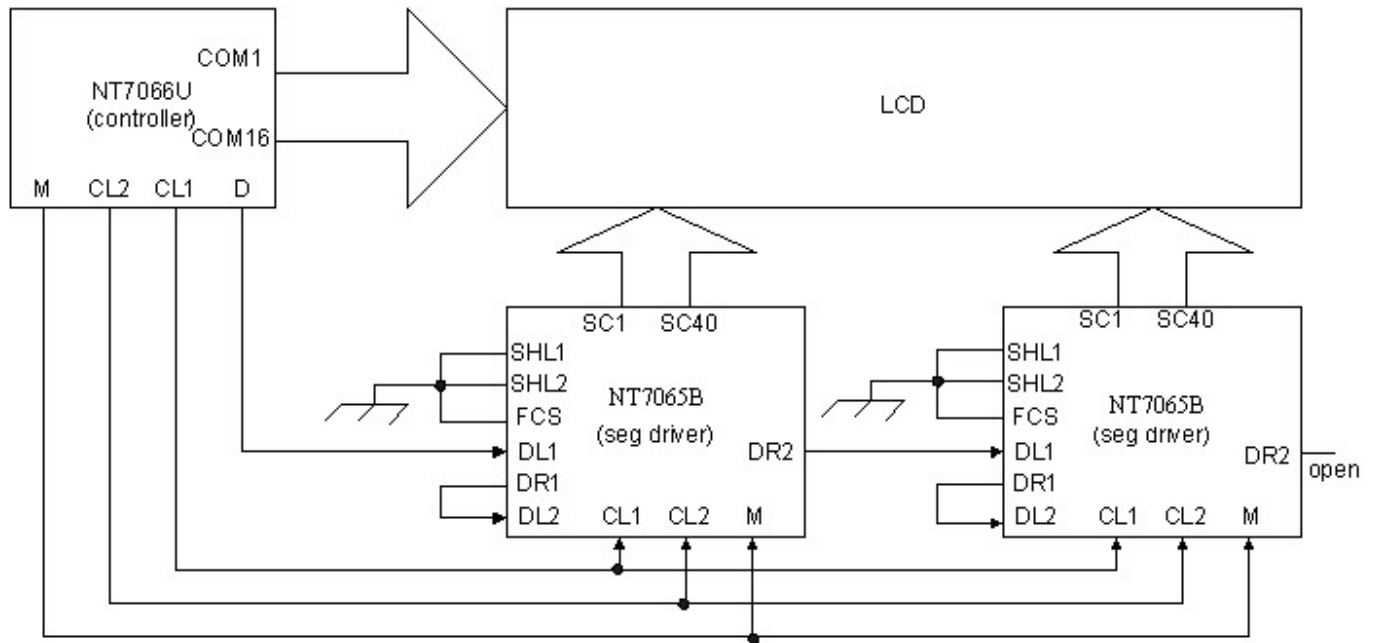
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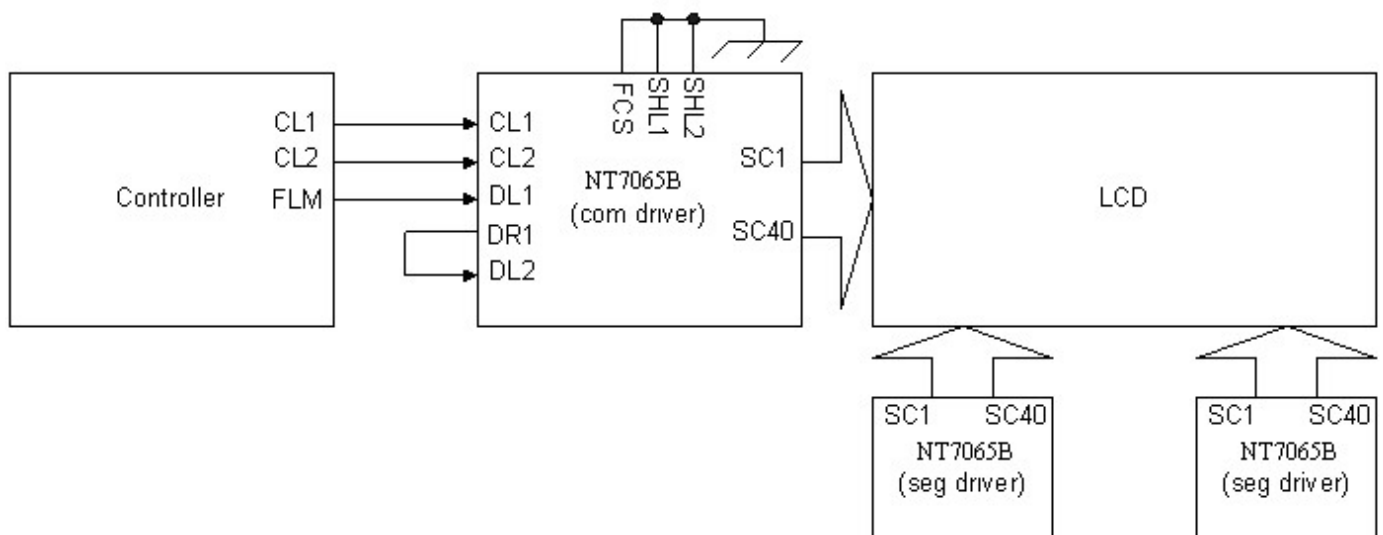
NT7065B

## Application circuit

### 1) Segment driver



## 2) Common driver





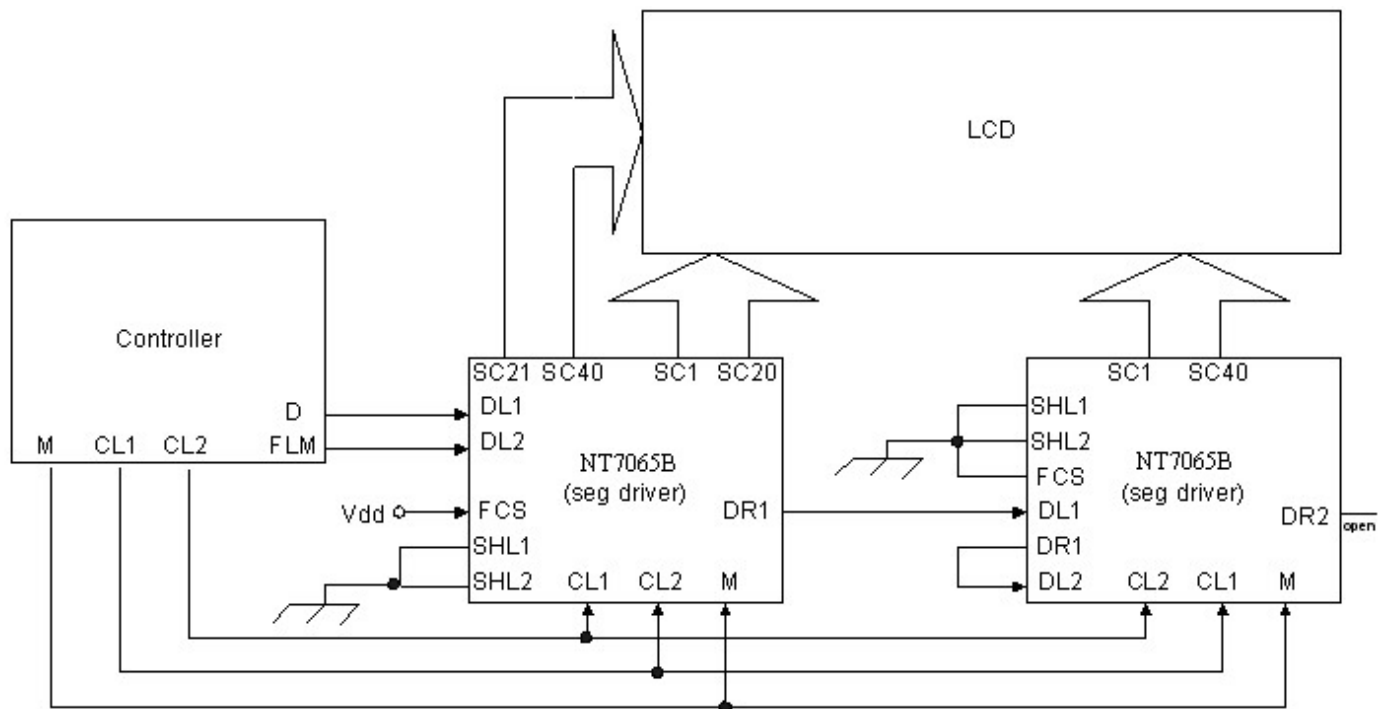
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NT7065B

### 3) Segment/Common driver





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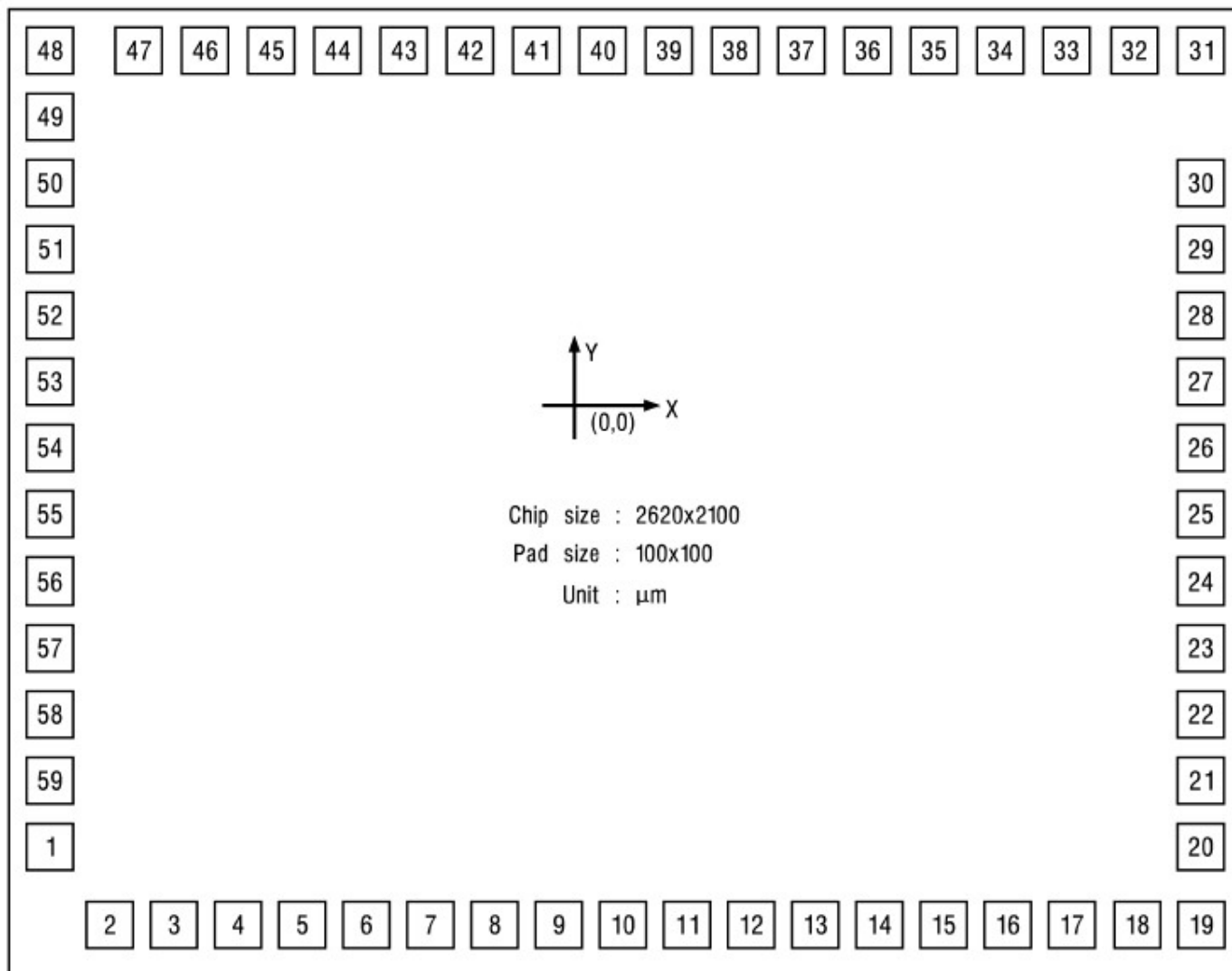
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# NT7065B

### Pad Diagram

**Note:** Please connects the substrate to  $V_{DD}$  or floating



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**NT7065B****Pad Location****Note:** (0,0) is center in the chip

Pad		Coordinates		Pad		Coordinates	
NO.	Name	X	Y	NO.	Name	X	Y
1	VEE	-1120.20	-642.50	31	SC28	1117.50	865.20
2	CL1	-1062.50	-865.20	32	SC27	992.50	865.20
3	CL2	-937.50	-865.20	33	SC26	867.50	865.20
4	GND	-812.50	-865.20	34	SC25	742.50	865.20
5	DL1	-687.50	-865.20	35	SC24	617.50	865.20
6	DR1	-562.50	-865.20	36	SC23	492.50	865.20
7	DL2	-437.50	-865.20	37	SC22	367.50	865.20
8	DR2	-312.50	-865.20	38	SC21	242.50	865.20
9	M	-187.50	-865.20	39	SC20	117.50	865.20
10	SHL1	-62.50	-865.20	40	SC19	-7.50	865.20
11	SHL2	62.50	-865.20	41	SC18	-132.50	865.20
12	FCS	187.50	-865.20	42	SC17	-257.50	865.20
13	V1	332.50	-865.20	43	SC16	-382.50	865.20
14	V2	457.50	-865.20	44	SC15	-507.50	865.20
15	V3	582.50	-865.20	45	SC14	-632.50	865.20
16	V4	707.50	-865.20	46	SC13	-757.50	865.20
17	V5	832.50	-865.20	47	SC12	-882.50	865.20
18	V6	957.50	-865.20	48	SC9	-1120.20	857.20
19	SC40	1082.50	-865.20	49	SC10	-1120.20	732.50
20	SC39	1120.20	-627.50	50	SC11	-1120.20	607.50
21	SC38	1120.20	-502.50	51	SC8	-1120.20	482.50
22	SC37	1120.20	-377.50	52	SC7	-1120.20	357.50
23	SC36	1120.20	-252.50	53	VDD	-1120.20	232.50
24	SC35	1120.20	-127.50	54	SC6	-1120.20	107.50
25	SC30	1120.20	-2.50	55	SC5	-1120.20	-17.50
26	SC31	1120.20	122.50	56	SC4	-1120.20	-142.50
27	SC32	1120.20	247.50	57	SC3	-1120.20	-267.50
28	SC33	1120.20	372.50	58	SC2	-1120.20	-392.50
29	SC34	1120.20	479.50	59	SC1	-1120.20	-517.50
30	SC29	1120.20	622.50				