MF1493-03

S1D15G10D08B000

Rev. 1.0a

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Rev. 1.0a

Contents

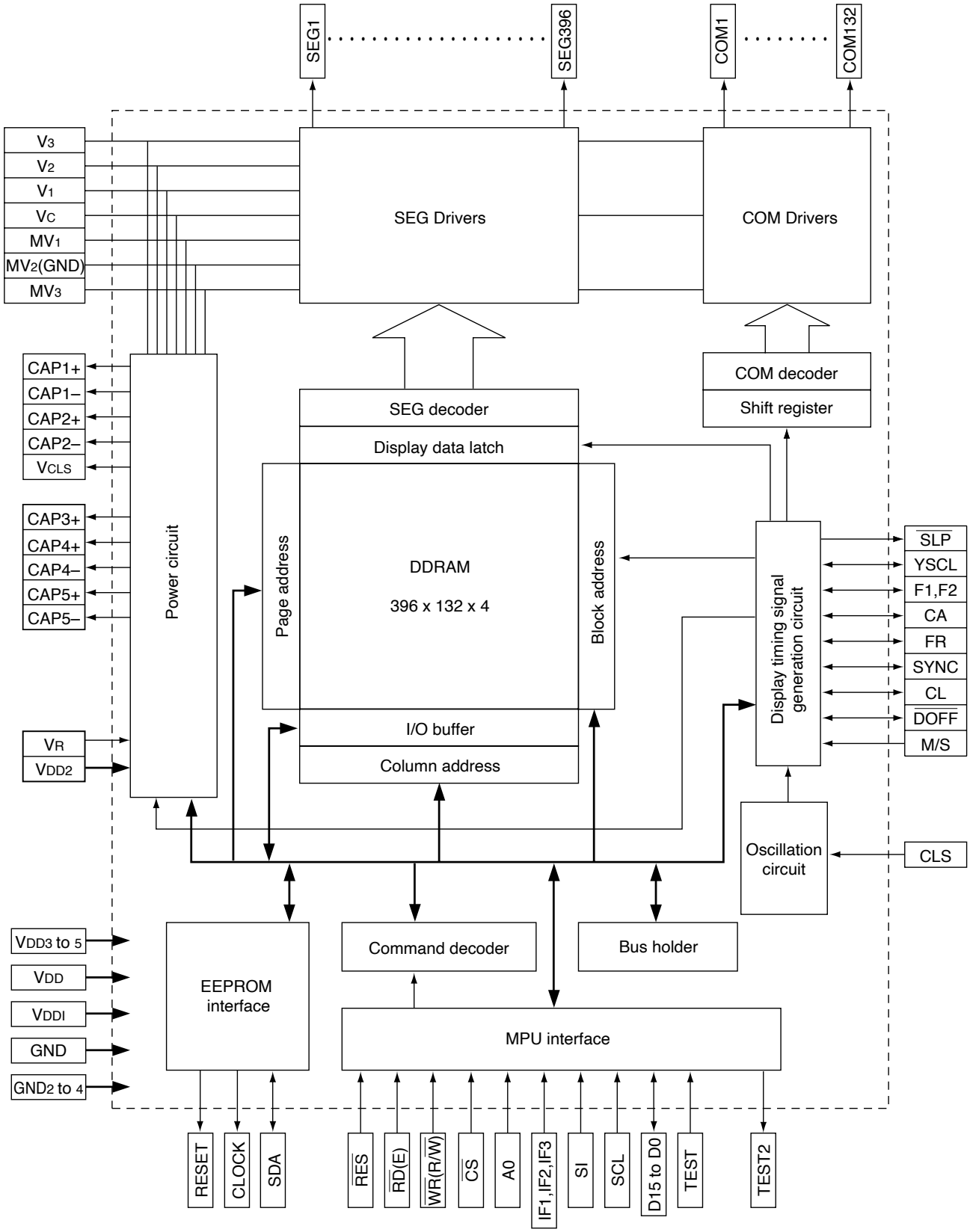
1. DESCRIPTION

S1D15G10 series are the LCD drivers equipped with the liquid crystal drive power circuit to realize color display with one chip.
S1D15G10 can be directly connected to the MPU bus to store parallel or serial gray-scale display data from MPU on the built-in RAM and to generate liquid crystal drive signals independent from MPU. S1D15G10 generates 396 segment outputs and 132 common outputs for driving liquid crystal. It incorporates the display RAM with capacity of 396 × 132 × 4 (16 gray-scale). A single dot of pixel on the liquid crystal panel corresponds to 4 bits of the built-in RAM, enabling to display 132 (RGB) × 132 pixels with one chip.
Read or write operations from MPU to the display RAM can be performed without resorting to external actuating clock signals. S1D15G10 allows you to run the display system of high performance and handy equipment at the minimum power consumption thanks to its low-power liquid crystal drive power circuit and oscillation circuit.

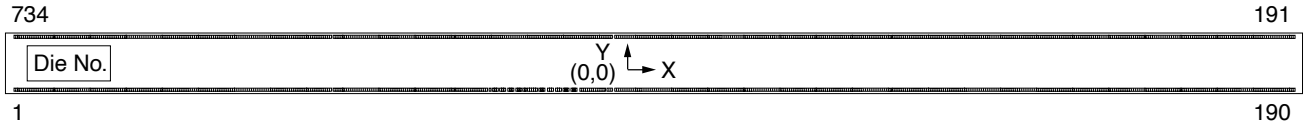
2. FEATURES

- Number of liquid crystal-drive outputs:
  396 segment outputs and 132 common outputs.
- Low cross talk by frame rate modulation.
- 256 color from 4096-color display or full 4096-color display.
  When 256 color from 4096-color display is selected: 8 gray-scale for red and green and 4 gray-scale for blue (intermediate tone is selected with the command).
  When 4096-color display is selected: 16 gray-scale for red, green and blue.
- Direct data display with display RAM
  (When the LCD is set to normally black)
  RAM bit Data "0000" ... OFF (Black)
  "1111" ...ON (Maximum RGB display)
  (Normally black LCD, using "inverse display" command)
- Partial display function: You can save power by limiting the display space. This function is most suited for handy equipment in the standby mode.
- Display RAM : 396 × 132 × 4 = 209,088 bits.
- MPU interface: S1D15G10 can be directly connected to both of the 8/16-bit parallel 80 and 68 series MPU. Two type serial interface are also available.
  • 3 pins serial : $\overline{CS}$, SCL and SI (D/C + 8-bit data)
  • 4 pins serial : $\overline{CS}$, SCL, SI and A0
- Abundant command functions: Area scroll function, automatic page & column increment function, display direction switching function and power circuit control function.
- Built-in liquid crystal drive power circuit: S1D15G10 is equipped the charge pump booster circuit, voltage follower circuit and electric volume control circuit.
- Oscillation circuit with built-in high precision CR (external clock signals acceptable)
- EEPROM interface functions
- Supply voltage
  Power for input/output system power:
  V_{DDI}–GND=1.7V to 3.6V
  Power for internal circuit operation:
  V_{DD}–GND=2.6V to 3.6V
  Reference power for booster circuit:
  V_{DD2}–GND=2.6V to 3.6V
  Power for liquid crystal drive:
  V_3–MV_3=12.0V to 21.0V
- Wider operational range: –40°C to +85°C.
- Shipping from: Chip with gold bump. COF.
- Note that the radiation resistant design or light resistance design in strict sense is not employed for S1D15G10.

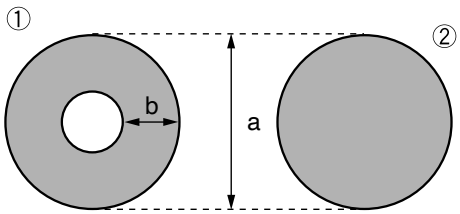
3. BLOCK DIAGRAM



4. PIN LAYOUT



Chip size	23.58 mm × 2.70 mm
Chip thickness	725 μm±25 μm (for reference)
Die No.	See Section 5 "List of Device Models."
Potential on board	GND
Bump size	Tolerance: ±4 μm (reference)
	Driver output side: (SEG1 to 396) 41.5 μm
	(COM1 to 33, 101 to 132) 48μm
	(COM34 to 100) 45μm
	Driver input side: 82 μm × 109 μm
Bump pitch	Driver output side: 42 μm
	I/O signal line side:100 μm min.
Bump height	22.5 μm±4 μm (for reference) : The tolerance is specified in delivery specification.
Alignment coordinate	
	① (–11449.8, –454.35)
	② (11424.0, –729.35)
Mark size	a = 80 μm
	b = 20 μm



5. LIST OF DEVICE MODELS

Model name	Die No.	Frame frequency /built-in oscillation frequency
S1D15G10D08B000	D15GAD8B0	180 Hz/47.52 kHz

6. PIN COORDINATE

Unit: μm

PAD No.	Pin Name	X	Y	Xsize	Ysize
1	NC	–11607.0	–1187.0	82	109
2	NC	–11487.0			
3	V_{3L}	–11367.0			
4	V_{3L}	–11247.0			
5	V_{3L}	–11127.0			
6	V_{3L}	–11007.0			
7	V_{2L}	–10887.0			
8	V_{2L}	–10767.0			
9	V_{2L}	–10647.0			
10	V_{1L}	–10527.0			
11	V_{1L}	–10407.0			
12	V_{1L}	–10287.0			
13	V_{CL}	–10167.0			
14	V_{CL}	–10047.0			
15	V_{CL}	–9927.0			
16	V_{CLSL}	–9807.0			
17	V_{CLSL}	–9687.0			
18	V_{CLSL}	–9567.0			
19	MV_{1L}	–9447.0			
20	MV_{1L}	–9327.0			
21	MV_{1L}	–9207.0			
22	MV_{3L}	–9087.0			
23	MV_{3L}	–8967.0			
24	MV_{3L}	–8847.0			
25	NC	–8714.0			
26	NC	–8614.0			
27	NC	–8514.0			
28	NC	–8414.0			
29	NC	–8314.0			
30	TESTA	–8169.0			
31	TESTA	–8054.0			
32	TESTA	–7939.0			
33	TESTA	–7824.0			
34	TESTA	–7709.0			
35	CAP2+	–7589.0			
36	CAP2+	–7474.0			
37	CAP2+	–7359.0			
38	CAP2+	–7244.0			
39	CAP2+	–7129.0			
40	CAP2–	–7009.0			
41	CAP2–	–6889.0			
42	CAP2–	–6769.0			
43	CAP2–	–6649.0			
44	CAP1+	–6529.0			
45	CAP1+	–6414.0			
46	CAP1+	–6299.0			
47	CAP1+	–6184.0			
48	CAP1+	–6069.0			
49	CAP1–	–5949.0			
50	CAP1–	–5829.0			
51	CAP1–	–5709.0			
52	CAP1–	–5589.0			
53	GND2	–5446.0			
54	GND2	–5341.0			
55	GND2	–5236.1			
56	GND2	–5131.1			
57	GND3	–5026.1	▼	▼	▼

PAD No.	Pin Name	X	Y	Xsize	Ysize
58	GND3	–4921.0	–1187.0	82	109
59	GND3	–4816.0			
60	GND	–4711.0			
61	GND	–4606.0			
62	GND	–4501.0			
63	V_{DD3}	–4396.0			
64	V_{DD3}	–4291.0			
65	V_{DD4}	–4186.0			
66	V_{DD4}	–4081.0			
67	TESTB	–3976.0			
68	V_{DD}	–3871.0			
69	V_{DD}	–3766.0			
70	V_{DDI}	–3661.0			
71	V_{DDI}	–3556.0			
72	V_{DDI}	–3451.0			
73	V_{DDI}	–3346.0			
74	FR	–3235.0			
75	YSCL	–3081.0			
76	F1	–2927.0			
77	F2	–2773.0			
78	$\overline{DOFF}$	–2619.0			
79	CA	–2465.0			
80	SYNC	–2311.0			
81	$\overline{SLP}$	–2157.0			
82	SDA	–2003.0			
83	RESET	–1849.0			
84	CLOCK	–1695.0			
85	TEST1	–1541.0			
86	GND *6	–1387.0		▼	
87	V_{DDI} *6	–1287.0		72	
88	CL	–1187.0		82	
89	CLS	–1033.0		▼	
90	GND *6	–879.0		▼	
91	V_{DDI} *6	–779.0		72	
92	MS	–679.0		82	
93	A0	–525.0		▼	
94	GND *6	–371.0		▼	
95	V_{DDI} *6	–271.0		72	
96	TEST2	–171.0		82	
97	$\overline{WR}$	–17.0		▼	
98	GND	137.0		▼	
99	V_{DDI}	237.0		72	
100	D0	337.0		82	
101	D1	491.0			
102	D2	645.0			
103	D3	799.0			
104	D4	953.0			
105	D5	1107.0			
106	D6	1261.0			
107	D7	1415.0			
108	GND	1569.0		▼	
109	V_{DDI}	1669.0		72	
110	D8	1769.0		82	
111	D9	1923.0			
112	D10	2077.0			
113	D11	2231.0			
114	D12	2385.0	▼	▼	▼

Unit: μm

PAD No.	Pin Name	X	Y	Xsize	Ysize
115	D13	2539.0	–1187.0	82	109
116	D14	2693.0			
117	D15	2847.0			
118	GND	3001.0			
119	V_{DDI}	3101.0		72	
120	$\overline{RD}$	3201.0		82	
121	$\overline{RES}$	3355.0			
122	GND *6	3509.0			
123	V_{DDI} *6	3609.0		72	
124	IF1	3709.0		82	
125	IF2	3863.0			
126	IF3	4017.0			
127	GND *6	4171.0			
128	V_{DDI} *6	4271.0		72	
129	SI	4371.0		82	
130	SCL	4525.0			
131	$\overline{CS}$	4679.0			
132	V_{DDI}	4861.0			
133	V_{DDI}	4966.0			
134	GND	5071.0			
135	GND	5176.0			
136	GND	5281.0			
137	GND	5386.0			
138	GND4	5491.0			
139	GND4	5596.0			
140	GND4	5701.0			
141	GND4	5806.0			
142	V_{DD}	5911.0			
143	V_{DD}	6016.0			
144	V_{DD5}	6121.0			
145	V_{DD5}	6226.0			
146	V_{DD2}	6372.0			
147	V_{DD2}	6477.0			
148	V_{DD2}	6582.0			
149	V_{DD2}	6687.0			
150	CAP4+	6807.0			
151	CAP4+	6927.0			
152	CAP4+	7047.0			
153	CAP4–	7167.0			
154	CAP4–	7287.0			
155	CAP4–	7407.0			
156	CAP5+	7527.0			
157	CAP5+	7647.0			
158	CAP5+	7767.0			
159	CAP5–	7887.0			
160	CAP5–	8007.0			
161	CAP5–	8127.0			
162	MV_{3R}	8247.0			
163	MV_{3R}	8367.0			
164	MV_{3R}	8487.0			
165	TESTC	8607.0			
166	TESTC	8727.0			
167	TESTC	8847.0			
168	TESTD	8967.0			
169	TESTD	9087.0			
170	TESTD	9207.0			
171	MV_{1R}	9327.0			

PAD No.	Pin Name	X	Y	Xsize	Ysize
172	MV_{1R}	9447.0	–1187.0	82	109
173	MV_{1R}	9567.0			
174	V_R	9686.9			
175	V_R	9807.0			
176	V_{CR}	9927.0			
177	V_{CR}	10047.0			
178	V_{CR}	10167.0			
179	V_{1R}	10287.0			
180	V_{1R}	10407.0			
181	V_{1R}	10527.0			
182	V_{2R}	10647.0			
183	V_{2R}	10767.0			
184	V_{2R}	10887.0			
185	V_{3R}	11007.0			
186	V_{3R}	11127.0			
187	V_{3R}	11247.0			
188	V_{3R}	11367.0			
189	NC	11487.0			
190	NC	11607.0			
191	NC	11661.0	1175.5	30	137
192	NC	11605.0			
193	NC	11549.0			
194	NC	11493.0			
195	NC	11445.0			
196	COM1	11397.0			
197	COM2	11349.0			
198	COM3	11301.0			
199	COM4	11253.0			
200	COM5	11205.0			
201	COM6	*1			
to	to				
227	COM32				
228	COM33	9861.0			
229	COM34	9815.0		28	
230	COM35	9770.0			
231	COM36	9725.0			
232	COM37	*2			
to	to				
261	COM66				
262	COM67	8330.0			
263	COM68	8285.0			
264	NC	8240.0			
265	NC	8195.0			
266	NC	8152.5		26	
267	SEG396	8111.0			
268	SEG395	8069.5			
269	SEG394	*3			
to	to				
660	SEG3				
661	SEG2	–8240.0			
662	SEG1	–8281.5			
663	NC	–8325.5		28	
664	NC	–8371.0			
665	NC	–8416.0			
666	COM69	–8461.0			
667	COM70	–8506.0			

Unit: μm

PAD No.	Pin Name	X	Y	Xsize	Ysize
668	COM71	*4	1175.5	28	137
to	to				
694	COM97				
695	COM98	–9766.0			
696	COM99	–9813.0		30	
697	COM100	–9861.0			
698	COM101	*5			
to	to				
727	COM130				

PAD No.	Pin Name	X	Y	Xsize	Ysize
728	COM131	–11349.0	1175.5	30	137
729	COM132	–11397.0			
730	NC	–11445.0			
731	NC	–11493.0			
732	NC	–11549.0			
733	NC	–11605.0			
734	NC	–11661.0			

1: You can determine the position on X coordinate from the formula “11157.0–48 (n–201)”, where the BUMP No. is “n”.
2: You can determine the position on X coordinate from the formula “9680.0–45 (n–232)”, where the BUMP No. is “n”.
3: You can determine the position on X coordinate from the formula “8028.0–41.5 (n–269)”, where the BUMP No. is “n”.
4: You can determine the position on X coordinate from the formula “–8551.0–45 (n–668)”, where the BUMP No. is “n”.
5: You can determine the position on X coordinate from the formula “–9909.0–48 (n–698)”, where the BUMP No. is “n”.
*6: This pin is used to pull up or pull down nearby pins. Thus, it can’t be used for feeding power.

7. PIN DESCRIPTION

7.1 Power Supply Pins

Pin name	I/O	Description	Number of pins
V_{DDI}	Input power	They are used to connect the power for input signals.	14
V_{DD}	Power supply	They are connected to V_{CC} - the system power. When the system power is smaller than 2.6V, they must be connected another 2.6V or greater power supply.	4
V_{DD2}	Step-up power	They are used to connect the power supply for the primary step-up. The relative magnitude of potential among the pins, namely $V_{DD2} \geq V_{DD} \geq V_{DD1}$, must be observed.	6
V_{DD3},V_{DD5}	Power supply	They are power supply pins on the power circuit *1.	4
V_{DD4}	Power supply	They are power supply pins on the oscillation circuit *1.	2
GND	Power supply	They are connected to the system ground.	15
GND2, GND4	Power supply	They are grounding pins on the power circuit *2.	8
GND3	Power supply	They are grounding pins on the oscillation circuit *2.	3
V_{3L}, V_{3R} V_{2L}, V_{2R} V_{1L}, V_{1R} V_{CL}, V_{CR} MV_{1L}, MV_{1R} MV_{3L}, MV_{3R}	Power supply	These pins are provided on the multi-level power supply for liquid crystal drive. Relative magnitude of potential among the pins, namely $V_{3L}(R) \geq V_{2L}(R) \geq V_{1L}(R) \geq V_{CL}(R) \geq MV_{1L}(R) \geq GND \geq MV_{3L}(R)$, must be observed. When or the internal power supply is turned on, predetermined voltage is output at respective pins. L and R of each power supply are connected inside the IC.	38
V_{CLSL} (V_{OUT})	Power supply	They are provided on the common driver operating power supply.	3
V_R	Input power	Regulator input pins.	2

*1: Since V_{DD}, V_{DD3}, V_{DD4} and V_{DD5} are not internally connected, they must be externally connected to V_{CC} - the system power.

*2: Since GND, GND2, GND3 and GND4 are not internally connected, they must be externally connected to the system GND (ground).

7.2 Pins on Liquid Crystal Drive Power Circuit

Pin name	I/O	Description	Number of pins
CAP1+	O	They connect the positive going side of the primary step-up capacitor.	5
CAP1–	O	They connect the negative going side of the primary step-up capacitor.	4
CAP2+	O	They connect the positive going side of the secondary step-up capacitor.	5
CAP2–	O	They connect the negative going side of the secondary step-up capacitor.	4
CAP3+	—	They are unused pins. Their pins must be fixed at OPEN.	5
CAP4+	O	They connect the positive going side of the tertiary step-up capacitor.	3
CAP4–	O	They connect the negative going side of the tertiary step-up capacitor.	3
CAP5+	O	They connect the positive going side of the tertiary step-up capacitor.	3
CAP5–	O	They connect the positive going side of the tertiary step-up capacitor.	3

7.3 MPU Interface Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D15 to D0</td><td>I/O</td><td>They connect to the standard 8-bit or 16-bit MPU bus via the 8/16-bit bi-directional bus.
When the following interface is selected and the CS pin is high, the following pins become high impedance.
① 8-bit parallel: D15-D18 are in the state of high impedance
② Serial interface: D15-D0 are in the state of high impedance</td><td>16</td></tr>
<tr><td>SI</td><td>I</td><td>This pin is used to input serial data when the serial interface is selected.</td><td>1</td></tr>
<tr><td>SCL</td><td>I</td><td>This pin is used to input serial clock when the serial interface is selected. The data is converted in the rising edge.</td><td>1</td></tr>
<tr><td>IF1, IF2
IF3</td><td>I</td><td>These pins are used to select either of the MPU interfaces.
Depending on status of IF1, IF2 and IF3, following selection is made.
<table>
<tr><th>IF1</th><th>IF2</th><th>IF3</th><th>MPU interface type</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>HIGH</td><td>80 series 16-bit parallel</td></tr>
<tr><td>HIGH</td><td>HIGH</td><td>LOW</td><td>80 series 8-bit parallel</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>LOW</td><td>68 series 16-bit parallel</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>HIGH</td><td>68 series 8-bit parallel</td></tr>
<tr><td>LOW</td><td>LOW</td><td>HIGH</td><td>9-bit serial</td></tr>
<tr><td>LOW</td><td>LOW</td><td>LOW</td><td>8-bit serial</td></tr>
</table></td><td>3</td></tr>
<tr><td>A0</td><td>I</td><td>Normally, the least significant bit of the MPU's address bus is connected to identify a parameter or display data from a command.
HIGH: Indicates that data entered to D15 to D0 or SI is a parameter or display data.
LOW: Indicates that data entered to D15 to D0 or SI is a command.
This function is disabled when the 9-bit serial interface is selected.</td><td>1</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td>This pin is used to enter chip select signal. It is activated when $\overline{CS}$ = LOW, enabling interface with MPU.</td><td>1</td></tr>
<tr><td>$\overline{RD}$ (E)</td><td>I</td><td>• It goes active LOW when connected to the 80 series MPU.
This pin is used to connect $\overline{RD}$ signal from the 80 series MPU. The data bus is maintained in the output status as long as this signal is LOW.
• It goes active HIGH when connected to the 68 series MPU.
In this case, this pin is used to enter the enable clock from 68 series MPU.</td><td>1</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>I</td><td>• It goes active LOW when connected to the 80 series MPU.
This pin connects $\overline{WR}$ signal from the 80 series MPU. Signal on the data bus is latched at the positive going edge of $\overline{WR}$ signal.
• This pin enters the read/write signal when connected to the 68 series MPU.
R/$\overline{W}$ = HIGH: Read
R/$\overline{W}$ = LOW: Write</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>Causing $\overline{RES}$ to LOW performs initialization.
Reset operation is performed according the level of $\overline{RES}$ signal.</td><td>1</td></tr>
</table>

7.4 Liquid Crystal Drive Circuit Signals

Pin name	I/O	Description	Number of pins
M/S	I	This pin is used to select either the master or slave operation. M/S = HIGH: Master operation	1
CLS	I	It is used to select the display clock. CLS = HIGH: Built-in CR oscillation is used. CLS = LOW: External clock is used. When the external clock is used (CLS = LOW), the signal is entered to CL pin.	1
CL	I/O	This pin inputs or outputs the display clock. It outputs the display clock only when M/S = HIGH and CLS = HIGH. Other than the above: External clock input	1
FR	I/O	This pin inputs or outputs the liquid crystal frame signal. M/S = HIGH: Outputs the signal M/S = LOW: Inputs the signal	1
SYNC	I/O	This pin inputs or outputs the liquid crystal synchronization signal. M/S = HIGH: Outputs the signal M/S = LOW: Inputs the signal	1
CA	I/O	This pin inputs or outputs the field start signal. M/S = HIGH: Outputs the signal M/S = LOW: Inputs the signal	1
F1, F2	I/O	This pin inputs or outputs the drive pattern signal. M/S = HIGH: Outputs the signal M/S = LOW: Inputs the signal	1
$\overline{DOFF}$	I/O	This pin is used to control blanking of liquid crystal display. M/S = HIGH: Outputs the signal M/S = LOW: Inputs the signal	1
YSCL	I/O	This pin inputs or outputs the line clock. M/S = HIGH: Outputs the signal M/S = LOW: Inputs the signal	1
SEGn	O	They output the signal for the segment drive of liquid crystal.	396
COMn	O	They output the signal for common drive of liquid crystal.	132

7.5 EEPROM Interface Pins

Pin name	I/O	Description	Number of pins
SDA	O	Connected to the SDA pin of S1F17A10. *1	1
RESET	O	Connected to the XRST pin of S1F17A10. *1	1
CLOCK	O	Connected to the SCK pin of S1F17A10. *1	1

* Always open if the S1F17A10 is not used.

7.6 Control Signals

Pin name	I/O	Description	Number of pins
$\overline{SLP}$	O	It is the sleep control pin. It outputs LOW level when the sleep-in command is executed.	1

7.7 Test Signals

Pin name	I/O	Description	Number of pins
TEST1	I	The pin for testing IC chips. Fix this pin to LOW.	1
TEST2	O	The output pin for testing IC chips. Make this pin open.	1
TESTA TESTB TESTC TESTD	O	The output pin for testing IC chips. Make this pin open.	12

8. FUNCTIONAL DESCRIPTION

8.1 MPU Interfaces

8.1.1 Selecting an MPU Interface Type

S1D15G10 transfers data via the 8/16-bit bi-directional data bus or serial data input.
You can select a desired interface face through the combinations of settings of IF1, IF2 and IF2 as shown in Table 8.1.1.

Table 8.1.1

IF1	IF2	IF3	Interface type	$\overline{CS}$	A0	$\overline{RD}$ E	$\overline{WR}$ R/$\overline{W}$	D15 to D8	D7 to D0	SI	SCL
HIGH	HIGH	HIGH	80 series 16-bit parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	D15 to D8	D7 to D0	—	—
HIGH	HIGH	LOW	80 series 8-bit parallel	$\overline{CS}$	A0	$\overline{RD}$	$\overline{WR}$	—	D7 to D0	—	—
HIGH	LOW	LOW	68 series 16-bit parallel	$\overline{CS}$	A0	E	R/$\overline{W}$	D15 to D8	D7 to D0	—	—
LOW	HIGH	HIGH	68 series 8-bit parallel	$\overline{CS}$	A0	E	R/$\overline{W}$	—	D7 to D0	—	—
LOW	LOW	HIGH	9-bit serial	$\overline{CS}$	—	—	—	—	—	SI	SCL
LOW	LOW	LOW	8-bit serial	$\overline{CS}$	A0	—	—	—	—	SI	SCL

— : Must be fixed to either HIGH or LOW.

8.1.2 8- or 16-bit Parallel Interface

S1D15G10 identifies type of the data bus signals according to combinations of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$) signals as shown in Table 8.1.2.

Table 8.1.2

A0	68 series		80 series		Function
	R/$\overline{W}$	E	$\overline{RD}$	$\overline{WR}$	
1	0	1	1	0	Parameters or display data write.
1	1	1	0	1	Display data read.
0	1	1	0	1	Status read.
0	0	1	1	0	Control data write (command).

Except when the $\overline{CS}$=LOW is taking place, D15 to D0 on S1D15G10 are caused to high impedance, disabling input of A0, $\overline{RD}$ (E) and $\overline{WR}$ (R/$\overline{W}$).

Relation between Data Bus and Gradation Data

S1D15G10 offers the 256-color display (8 gray-scale) out of 4096 colors as well as the 4096-color display (16 gray-scale). When using 256-color display out of 4096 colors, you can specify color for each of R, G and B using the palette function.
When using 4096 colors for display, you can select the type A or type B display mode depending on the data bus and RGB you use. Use the data control command for switcing between these modes.

(1) 256-color display out of 4096 colors

Using RGBSET8 command enables you to set color for each of R, G and B by turning on the palette function prepared to convert 3- or 2-bit data to 4-bit data.

① 8-bit mode

D7, D6, D5, D4, D3, D2, D1, D0: RRRGGGBB (8 bits) data is converted to RRRRGGGGBBBB (12 bits) and then stored on the display RAM.

② 16-bit mode

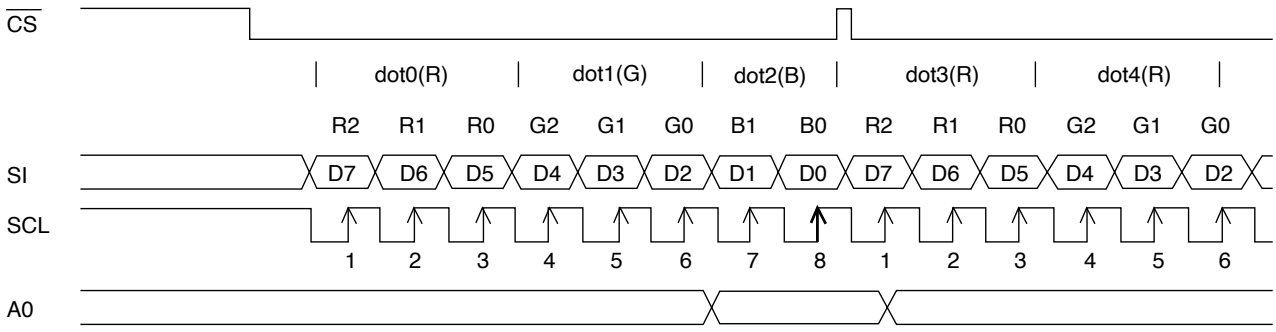
D15, D14, D13, D12, D11, D10, D9, D8: RRRGGGBB (8 bits)
D7, D6, D5, D4, D3, D2, D1, D0: RRRGGGBB (8 bits)
Data of two pixels is respectively converted to RRRRGGGGBBBB (12 bits) data and then simultaneously written to two addresses on the display RAM.

(2) 4096 color display
(2-1) Type 4096 color display
① 8-bit mode
D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGG (8 bits) 1st write
D7, D6, D5, D4, D3, D2, D1, D0: BBBBRRRR (8 bits) 2nd write
D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB (8 bits) 3rd write
Data is acquired through write operations as shown above and then that of two pixels is written to the display RAM.
② 16-bit mode
D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: RRRRGGGGBBBBXXXX (12 bits)
Data is acquired through single write operation and then written to the display RAM.
"XXXX" are dummy bits, and they are ignored for display.
(2-2) Type B 4096 color display
① 8-bit mode
D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRR (4 bits) 1st write
D7, D6, D5, D4, D3, D2, D1, D0: GGGGBBBB (8 bits) 2nd write
A single pixel of data is read after the second write operation as shown, and it is written in the display RAM.
"XXXX" are dummy bits, and they are ignored for display.
② 16-bit mode
D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0: XXXXRRRRGGGGBBBB (12 bits)
A single pixel of data is read and written in the display RAM in a single write operation.
"XXXX" are dummy bits, and they are ignored for display.

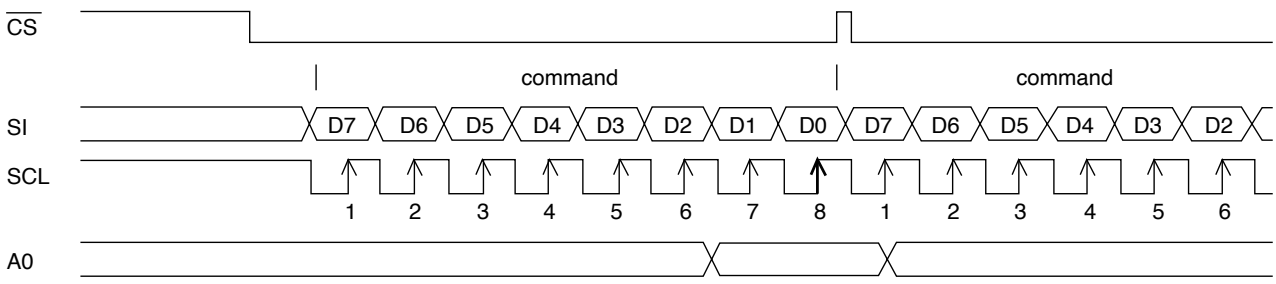
8.1.3 8- and 9-bit Serial Interface

The 8-bit serial interface uses four pins - $\overline{CS}$, SI, SCL and A0 - to enter commands and data. Meanwhile, the 9-bit serial interface uses three pins - $\overline{CS}$, SI and SCL - for the same purpose.
Data read is not available with the serial interface. Data entered must be 8 bits. Refer to the following chart for entering commands, parameters or gray-scale data.
The relation between gray-scale data and data bus in the serial input is the same as that in the 8-bit parallel interface mode (described in the preceding section) at every gradation.

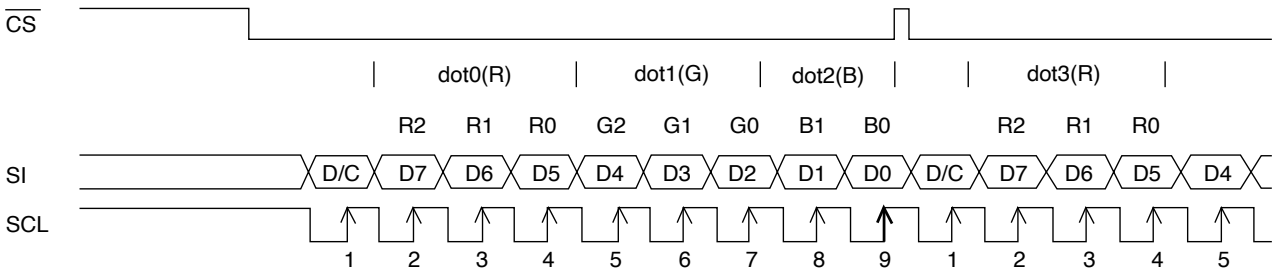
(1) 8-bit serial interface
When entering data (parameters): A0 = HIGH at the rising edge of the 8th SCL.



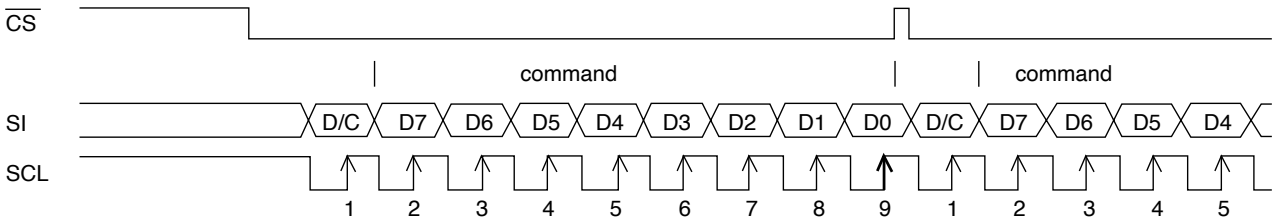
When entering command: A0 = LOW at the rising edge of the 8th SCL.



(2) 9-bit serial interface
When entering data (parameters): SI = HIGH at the rising edge of the 1st SCL.

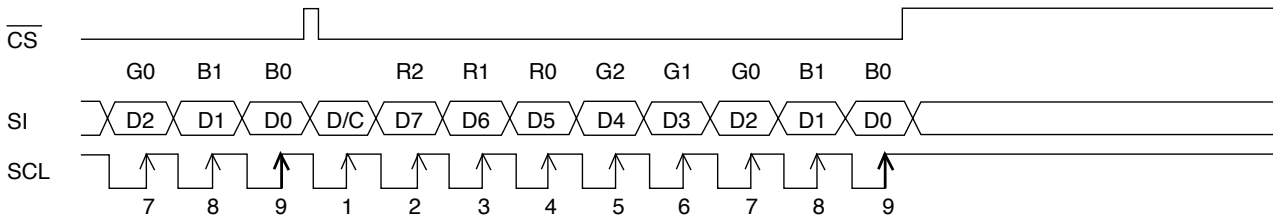


When entering commands: SI = LOW at the rising edge of the 1st SCL.



* If $\overline{CS}$ is caused to HIGH before 8 bits from D7 to D0 are entered, the data concerned is invalidated. Before entering succeeding sets of data, you must correctly input the data concerned again.
* In order to avoid data transfer error due to incoming noise, it is recommended to set $\overline{CS}$ at HIGH on byte basis to initialize the serial-to-parallel conversion counter and the register.
* When executing the command RAMWR, set $\overline{CS}$ to HIGH after writing the last address (after starting the 9th pulse in case of 9-bit serial input or after starting the 8th pulse in case of 8-bit serial input).

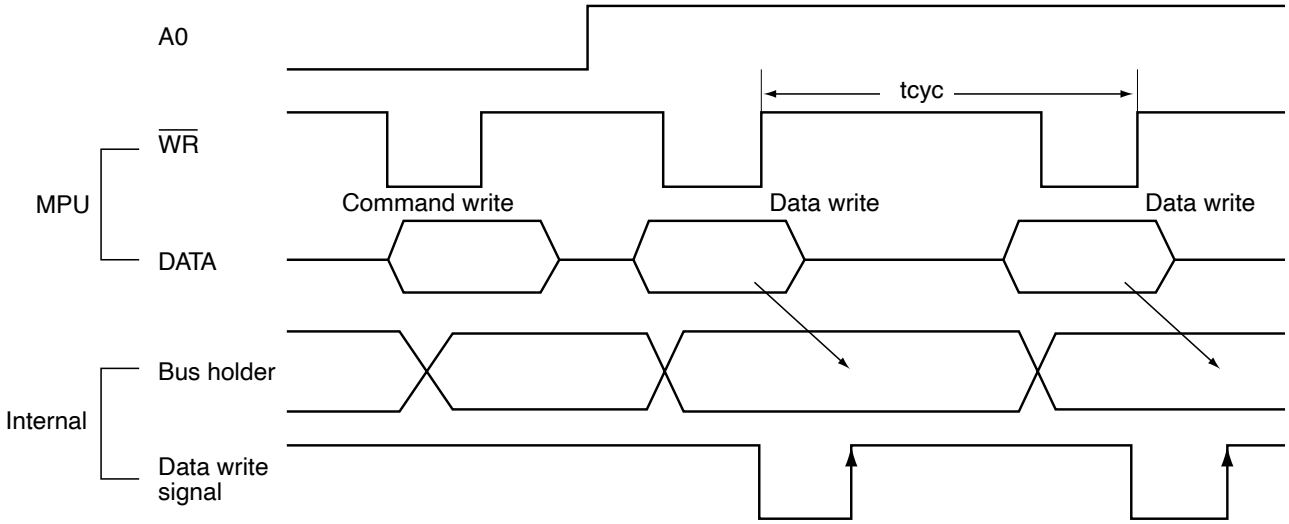
Example : In case of 9-bit serial input,



8.2 Access to DDRAM and Internal Registers

S1D15G10 realizes high-speed data transfer because the access from MPU is a sort of pipeline processing done via the bus holder attached to the internal, requiring the cycle time alone without needing the wait time.
For example, when MPU writes data to the DDRAM, the data is once held by the bus holder and then written to the DDRAM before the succeeding write cycle is started. When MPU reads data from the DDRAM, the first read cycle is dummy and the data read in the dummy cycle is held by the bus holder, and then it is read from the bus holder to the system bus in the succeeding read cycle. Fig. 8.2.1 illustrates these relations.

* Write operation



* Read operation

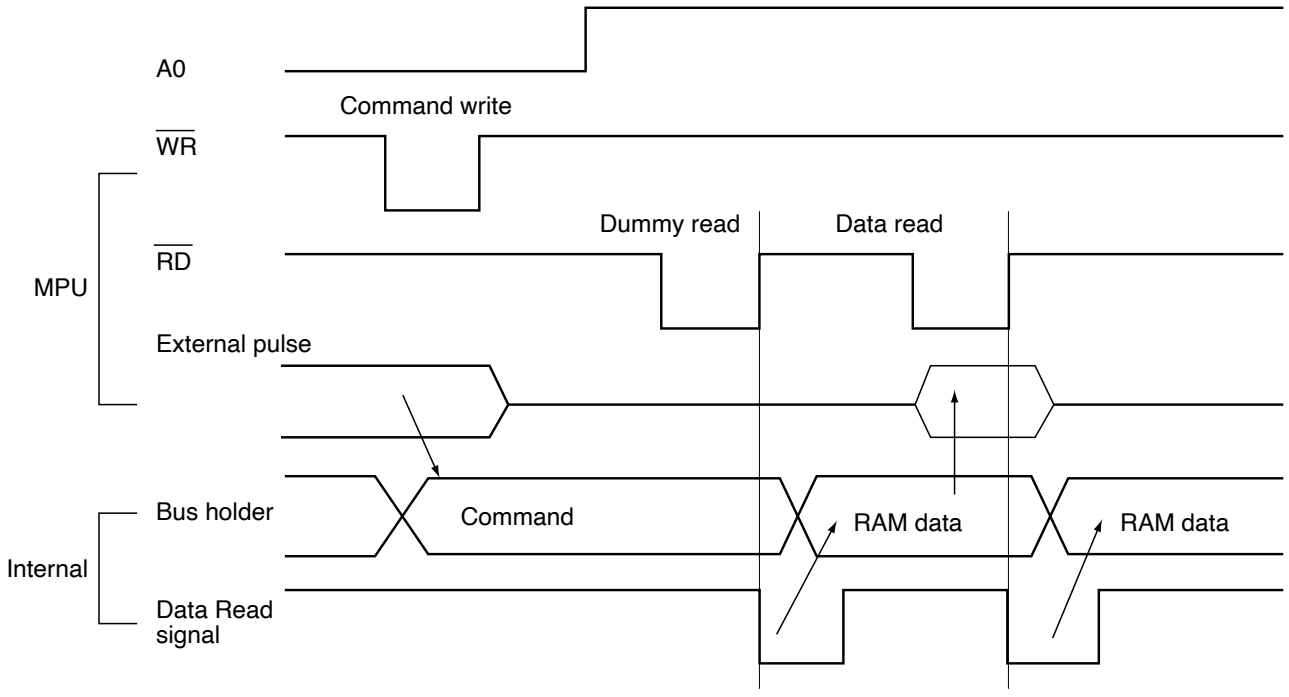


Fig. 8.2.1

* There is a restriction in the read sequence of the DDRAM. Namely, the data at the specified address is not output in the first data read conducted immediately after the memory read command (dummy read). It is read in the second data read.

8.3 DDRAM

8.3.1 DDRAM

It is 396 × 132 × 4 bits capacity RAM prepared for storing dot data. You can access a desired bit by specifying the page address and column address.
Since display data from MPU - D7 to D0 and D16 to D8 - correspond to one or two pixels of RGB, data transfer-related restrictions are reduced, realizing the display flexibly.
The RAM on S1D15G10 is separated to a block per 4 line to allow the display system to process data on the block basis.
MPU's read and write operations to and from the RAM are performed via the I/O buffer circuit. Reading of the RAM for the liquid crystal drive is controlled from another separate circuit.
Refer to the following memory map for the RAM configuration.

Memory Map (When using the 8 gray-scale. 8-bit mode)

RGB alignment (Command of data control parameter2=000)														
			Column											
LCD read direction	P11:0		0			1						131		
	P11:1		131			130						0		
	Color		R	G	B	R	G	B				R	G	B
	Page \ Data		D7 D6 D5	D4 D3 D2	D1 D0	D7 D6 D5	D4 D3 D2	D1 D0				D7 D6 D5	D4 D3 D2	D1 D0
Block	P10:0	P10:1												
0	0	131												
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
2	8	123												
	9	122												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			1	2	3	4	5	6				394	395	396

Each of RGB data entered to D7 to D0 (3 or 2 bits) is converted to 4 bits before written to the RAM. You can change position of R and B with DATCTL command.

Memory Map (When using the 8 gray-scale, 16-bit mode)

RGB alignment (Command of data control parameter2=000)																								
			Column																					
LCD read direction	P11:0		0			1			2			3					130			131				
	Color		R1	G1	B1	R2	G2	B2	R1	G1	B1	R2	G2	B2			R1	G1	B1	R2	G2	B2		
	Page \ Data		D15	D12	D9	D7	D4	D1	D15	D12	D9	D7	D4	D1			D15	D12	D9	D7	D4	D1		
			D14	D11	D8	D6	D3	D0	D14	D11	D8	D6	D3	D0			D14	D11	D8	D6	D3	D0		
			D13	D10		D5	D2		D13	D10		D5	D2				D13	D10		D5	D2			
	P11:1		131			130			129			128					1			0				
	Color		R2	G2	B2	R1	G1	B1	R2	G2	B2	R1	G1	B1			R2	G2	B2	R1	G1	B1		
	Page \ Data		D7	D4	D1	D15	D12	D9	D7	D4	D1	D15	D12	D9			D7	D4	D1	D15	D12	D9		
			D6	D3	D0	D14	D11	D8	D6	D3	D0	D14	D11	D8			D6	D3	D0	D14	D11	D8		
Block	P10:0	P10:1	D5	D2		D13	D10		D5	D2		D13	D10				D5	D2		D13	D10			
0	0	131																						
	1	130																						
	2	129																						
	3	128																						
1	4	127																						
	5	126																						
	6	125																						
	7	124																						
2	8	123																						
	9	122																						
31	124	7																						
	125	6																						
	126	5																						
	127	4																						
32	128	3																						
	129	2																						
	130	1																						
	131	0																						
SEGout			1	2	3	4	5	6	7	8	9	10	11	12			391	392	393	394	395	396		

Each of RGB data entered to D7 to D0 (3 or 2 bits) is converted to 4 bits before written to the RAM. You can change position of R and B with DATCTL command.

Memory Map (When using the 16 gray-scale Type A, 8-bit mode)

RGB alignment (Command of data control parameter2=000)																								
			Column																					
LCD read direction	P11: 0		0			1			2			3					130			131				
	Color		R1	G1	B1	R2	G2	B2	R1	G1	B1	R2	G2	B2			R1	G1	B1	R2	G2	B2		
	Data / Page		D7	D3	D7	D3	D7	D3	D7	D3	D7	D3	D7	D3			D7	D3	D7	D3	D7	D3		
			D6	D2	D6	D2	D6	D2	D6	D2	D6	D2	D6	D2			D6	D2	D6	D2	D6	D2		
			D5	D1	D5	D1	D5	D1	D5	D1	D5	D1	D5	D1			D5	D1	D5	D1	D5	D1		
			D4	D0	D4	D0	D4	D0	D4	D0	D4	D0	D4	D0			D4	D0	D4	D0	D4	D0		
	P11: 1		131			130			129			128					1			0				
	Color		R2	G2	B2	R1	G1	B1	R2	G2	B2	R1	G1	B1			R2	G2	B2	R1	G1	B1		
	Data / Page		D3	D7	D3	D7	D3	D7	D3	D7	D3	D7	D3	D7			D3	D7	D3	D7	D3	D7		
			D2	D6	D2	D6	D2	D6	D2	D6	D2	D6	D2	D6			D2	D6	D2	D6	D2	D6		
			D1	D5	D1	D5	D1	D5	D1	D5	D1	D5	D1	D5			D1	D5	D1	D5	D1	D5		
Block	P10:0	P10:1	D0	D4	D0	D4	D0	D4	D0	D4	D0	D4	D0	D4			D0	D4	D0	D4	D0	D4		
0	0	131																						
	1	130																						
	2	129																						
	3	128																						
1	4	127																						
	5	126																						
	6	125																						
	7	124																						
2	8	123																						
	9	122																						
31	124	7																						
	125	6																						
	126	5																						
	127	4																						
32	128	3																						
	129	2																						
	130	1																						
	131	0																						
SEGout			1	2	3	4	5	6	7	8	9	10	11	12			391	392	393	394	395	396		

You can change position of R and B with DATCTL command.

Memory Map (When using the 16 gray-scale Type A, 16-bit mode)

RGB alignment (Command of data control parameter2=000)														
			Column											
LCD read direction	P11:0		0			1						131		
	P11:1		131			130						0		
	Color		R	G	B	R	G	B				R	G	B
	Page \ Data		D15 D14 D13 D12	D11 D10 D9 D8	D7 D6 D5 D4	D15 D14 D13 D12	D11 D10 D9 D8	D7 D6 D5 D4				D15 D14 D13 D12	D11 D10 D9 D8	D7 D6 D5 D4
Block	P10:0	P10:1												
0	0	131												
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
2	8	123												
	9	122												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			1	2	3	4	5	6				394	395	396

You can change position of R and B with DATCTL command

Memory map (when using the 16 gray-scale Type B, 8-bit mode)

RGB alignment (Command of data control parameter2=000)														
			Column											
LCD read direction	P11:0		0			1						131		
	P11:1		131			130						0		
	Color		R	G	B	R	G	B				R	G	B
	Page \ Data		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0				D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0
Block	P10:0	P10:1												
0	0	131												
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
2	8	123												
	9	122												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			1	2	3	4	5	6				394	395	396

Positions of R and B can be changed using the DATCTL command.

Memory map (when using the 16 gray-scale Type B, 16-bit mode)

RGB alignment (Command of data control parameter2=000)														
			Column											
LCD read direction	P11:0		0			1						131		
	P11:1		131			130						0		
	Color		R	G	B	R	G	B				R	G	B
	Page \ Data		D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0	D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0				D11 D10 D9 D8	D7 D6 D5 D4	D3 D2 D1 D0
Block	P10:0	P10:1												
0	0	131												
	1	130												
	2	129												
	3	128												
1	4	127												
	5	126												
	6	125												
	7	124												
2	8	123												
	9	122												
31	124	7												
	125	6												
	126	5												
	127	4												
32	128	3												
	129	2												
	130	1												
	131	0												
SEGout			1	2	3	4	5	6				394	395	396

Positions of R and B can be changed using the DATCTL command.

8.3.2 Page Address Control Circuit

This circuit is used to control the address in the page direction when MPU accesses the DDRAM or when reading the DDRAM to display image on the LCD.
You can specify a scope of the page address (start and end page) with PASET (page address set) command. When the page-direction scan is specified with DATCTL (data control) command and the addresses are incremented from the start up to the end page, the column address is incremented by 1 and the page address returns to the start page.
The DDRAM supports up to 132 lines, and thus the total page becomes 132.
In the read operation, as the end page is reached, the column address is automatically incremented by 1 and the page address is returned to the start page.
Using the address normal/inverse parameter of DATCTL command allows you to inverse the correspondence between the DDRAM address and common output.

8.3.3 Column Address Control Circuit

This circuit is used to control the address in the column direction when MPU accesses the DDRAM. You can specify a scope of the column address (start and end column) using CASET (column address set). When the column-direction scan is specified with DATCTL command and the addresses are incremented from the start to the end up to the end column, the page address is incremented by 1 and the column address returns to the start column.
In the read operation, too, the column address is automatically incremented by 1 and returns to the start page as the end column is reached.
Just like the page address control circuit, using the column address normal/inverse parameter of DATCTL command enables to inverse the correspondence between the DDRAM column address and segment output. This arrangement relaxes restrictions in the chip layout on the LCD module.

8.3.4 I/O Buffer Circuit

It is the bi-directional buffer used when MPU reads or writes the DDRAM. Since MPU's read or write of the DDRAM is performed independently from data output to the display data latch circuit, asynchronous access to the DDRAM while the LCD is turned on does not cause troubles such as flicking of the display images.

8.3.5 Block Address Circuit

This circuit associates pages on the DDRAM with COM output. S1D15G10 processes signals for the liquid crystal display on 4-page basis (block basis). Thus, when specifying a specific area in the area scroll display or partial display, you must designate it in block.

8.3.6 Display Data Latch Circuit

This circuit is used to temporarily hold display data to be output from the DDRAM to the SEG decoder circuit. Since DISNOR/DISINV (display normal/inverse) and DISON/DISOFF (display on/display off) commands are used to control data in the latch circuit alone, they do not modify data in the DDRAM.

8.4 Area Scroll Display

Using ASCSET (area scroll set) and SCSTART (scroll start set) commands allows you to scroll the display screen partially. You can select any one of the following four scroll patterns.

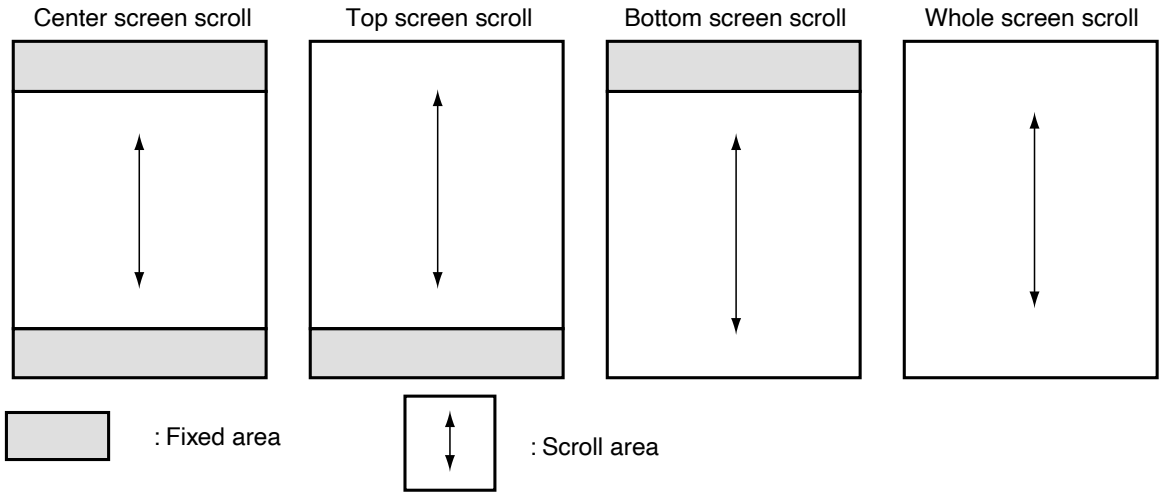
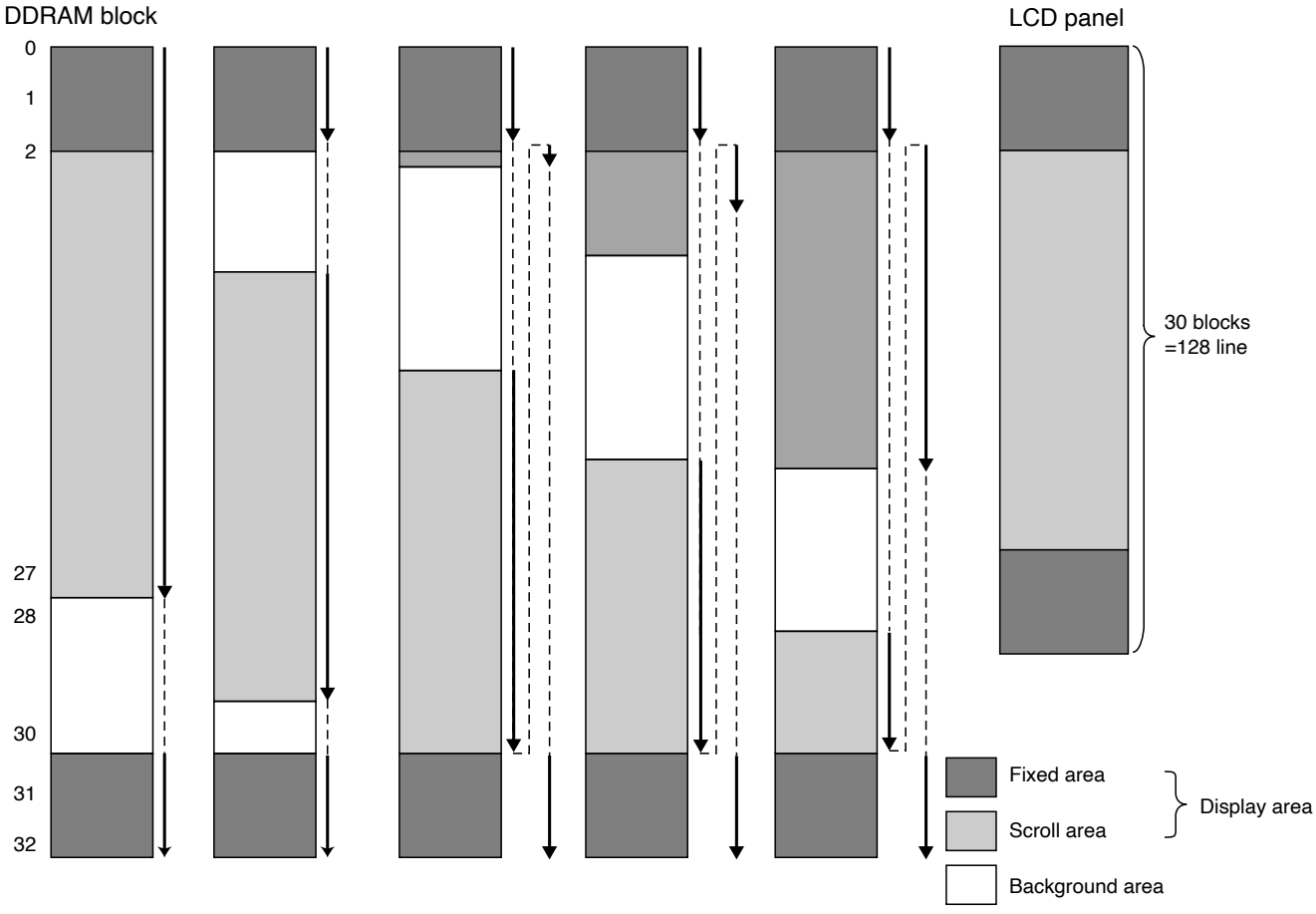


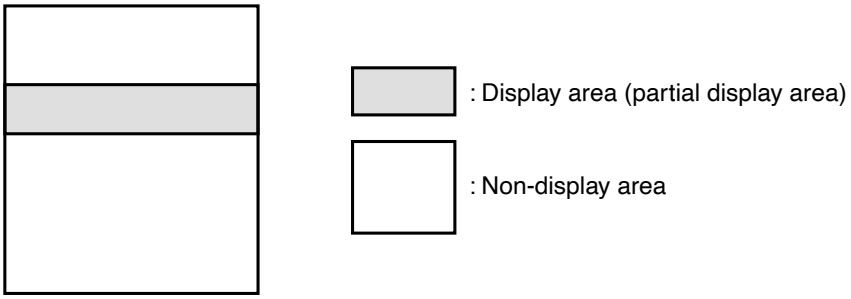
Fig. 8.4.1

When, for example, 1/120 duty (Display area: 30 blocks = 120 lines) is selected, and the top 2 blocks = 8 lines and bottom 2 blocks = 8 lines are specified as the fixed areas and the remaining 26 blocks = 104 lines as the scroll area, 3 blocks = 12 lines on the DDRAM can be used as the background area.



8.5 Partial Display

Using PTLIN (partial in) command allows you to turn on the partial display (division by line) of the screen. This mode requires less current consumption than the whole screen display, making it suitable for the mobile equipment in the standby state.



8.6 Gray-Scale Display

This function represents gray-scale by frame modulating the gray-scale date written on the display data RAM. In the 256-out-of-4096 colors (8 gray-scale) display, you can specify display colors using the command.

Normally black liquid crystal in the reverse display mode - 8 gray scale display

	Black	– –							Red
R (D7,D6,D5)	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)	
	Black	– –							Green
G (D4,D3,D2)	(0,0,0)	(0,0,1)	(0,1,0)	(0,1,1)	(1,0,0)	(1,0,1)	(1,1,0)	(1,1,1)	
	Black	– –							Blue
B (D1,D0)	(0,0)	(0,1)	(0,1)	(0,1)	(1,0)	(1,0)	(1,0)	(1,1)	
		Any one of above			Any one of above				

Respective data on red, green and blue are converted to the display data to be specified by the parameters of RGBSET8 command, and then written to the DDRAM. Blue is displayed in 4 gray-scale.

8.7 Oscillation Circuit

S1G15G10 contains the oscillation circuit whose operation does not require any external part. The oscillation circuit is enabled only when M/S = HIGH and CLS = HIGH. When the external clock signal is (CLS = LOW or M/S = LOW), the clock is entered from CL pin.

8.8 Display Timing Generation Circuit

This circuit generates the timing signal for display (CL, FR, SYNC, CA, F1, F2, $\overline{DOFF}$) using the clock from the built-in oscillation circuit or the external clock.
It is also used to generate the clock to turn on the liquid crystal-drive power circuit.
When using S1D15G10 in multi-chip array, the display timing signal (CL, FR, SYNC, CA, F1, F2, $\overline{DOFF}$) must be sent from the master to the slave.

8.9 SEG Decoder Circuit

This circuit outputs the segment driver control signal based on display data for 4-page and the timing signal.

8.10 Liquid Crystal Drive Circuit

It outputs liquid crystal drive voltage. Responding to the decoder output signal and the display-timing signal, the segment output pin outputs one of potentials V_2, V_1, V_C, MV_1 or MV_2 and the common output pin outputs one of potentials V_3, V_C or MV_3.

8.11 Liquid Crystal-Drive Power Circuit

The power circuit contained in S1D15G10 generates voltage required to drive liquid crystal. This low power consumption type power circuit is consisted the voltage regulator, booster circuits (primary, secondary) and voltage follower. The power circuit is enabled only when the master operation mode is turned on.
The power control circuit turns on or off the voltage regulator, booster circuits, Reference voltage generation circuit and voltage follower responding to PWRCTR (power control set) command. Thus, function of the external and internal power supplies can be partly used in parallel.
Table 8.11.1 lists the functions controlled by the 4-bit data - parameter of PWRCTR. Table 8.11.2 shows combinations of 4 bits (combinations shown in Table 8.11.2 alone are valid).

Table 8.11.1

Item	State "1"	State "0"
D3 Primary booster circuits control bit	ON	OFF
D2 Secondary booster circuit control bit	ON	OFF
D1 Reference voltage generation circuit control bit	ON	OFF
D0 Voltage adjusting circuit/Voltage follower control bit	ON	OFF

Table 8.11.2

Function turned on	D3	D2	D1	D0	External power input pins
1. Entire built-in power circuit is turned on	1	1	1	1	–
2. Other than the secondary booster and step-down circuits	1	0	1	1	V_3, MV_3
3. External power supply alone	0	0	0	0	V_3, V_2, V_C, MV_1, MV_3

8.11.2 Voltage Transform Circuit

The charge pump booster circuit and the operational amplifier's voltage follower generate each potential required to drive the liquid crystal based on the reference voltage generated by the voltage regulator.
Ground potentials (abbreviated as GND in the following description) of the power circuit in the IC are GND2 and GND4.
Fig. 8.11.1 illustrates mutual relationship between potentials.

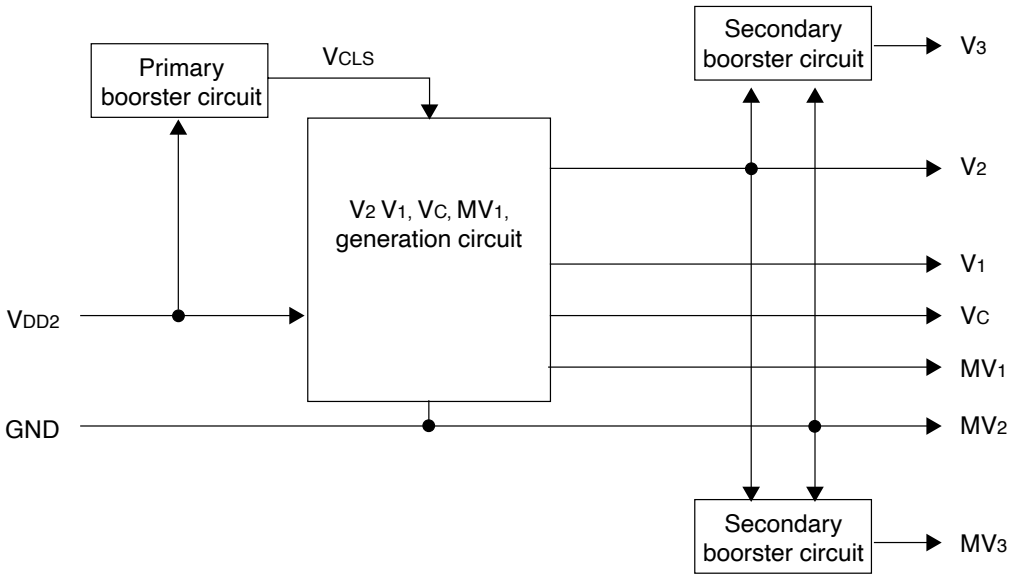


Fig. 8.11.1 Mutual Relationship between Voltage Transform Circuits

Table 8.11.3 shows the theoretical expression of respective potentials. Since these are theoretical values, they can differ from actual voltages depending on load on the liquid crystal.

Table 8.11.3 Theoretical Expression of Potentials

Signal name	Theoretical expression (relative to GND = 0V)	Theoretical expression (relative to Vc = 0V)
V_3	2×(V_2–GND)	2×(V_C–GND)
V_2	4/3×(V_1–GND)	V_C–GND
V_1	Output from voltage regulator	1/2×(V_C–GND)
V_C	2/3×(V_1–GND)	0V
MV_1	1/3×(V_1–GND)	–1/2×(V_C–GND)
GND(MV_2)	0V	–(V_C–GND)
MV_3	–(V_1–GND)	–2×(V_C–GND)

8.11.3 Primary Booster Circuit

The built-in booster circuit double the voltage of V_{DD2}-GND.
V_{DD2}-GND voltage is double by capacitor C connected across CAP1+ and CAP1 as well as V_{CSL} and GND (or V_{DD2}), and then output at V_{CSL} pin.
Fig. 8.11.2 shows how the voltage is stepped up by the capacitors connected.

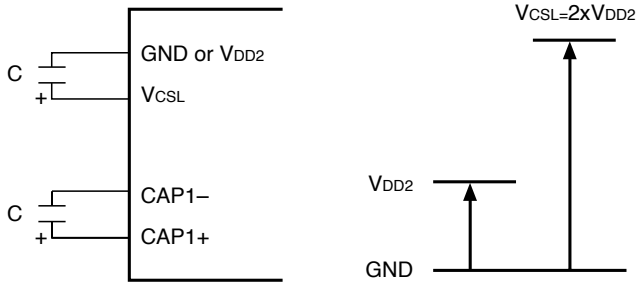


Fig. 8.11.2 Relation between Capacitors and Voltage Step-up

8.11.4 Voltage Regulator Circuit

The voltage regulator circuit generates the liquid crystal drive voltage V_1 using V_{CSL} from the primary booster circuit. S1D15G10 incorporates the high-precision constant voltage source, 64-step electronic volume control function and resistor to regulate V_1 voltage. The voltage regulator circuit covers a wider temperature range with fewer numbers of parts thanks to the temperature gradient control function as well as the temperature sensing function.
However, capacitors may be required for voltage regulation between V_1 and GND pins due to the load of LCD panel. Insert the capacitors, if necessary, by observing the voltage waveforms and current consumption.

(A) Built-in Resistor for V_1 Voltage Regulation
Using this resistor and the electronic volume control function allows you to control the liquid crystal drive voltage V_1 to an optimum level for the LCD panel with the command alone, without resorting to external resistors.
V_1 output voltage can be determined from Equation A-1 as long as the relation $V_1 < V_{CSL}$ is met.
However, set the voltage of V_1 by allowing for a drop in the voltage due to load, so that it becomes at or below 80 % of V_{CSL}.

$$V_1 = \left(1 + \frac{Rb}{Ra}\right) \bullet V_{EV} = \left(1 + \frac{Rb}{Ra}\right) \bullet \left(1 - \frac{\alpha + 2}{218}\right) \bullet V_{REG} \quad \text{(Equation A-1)}$$

Note: V_{REG} is the constant voltage source inside the IC. It is 1.2V (Typ.) at Ta = 25°C.

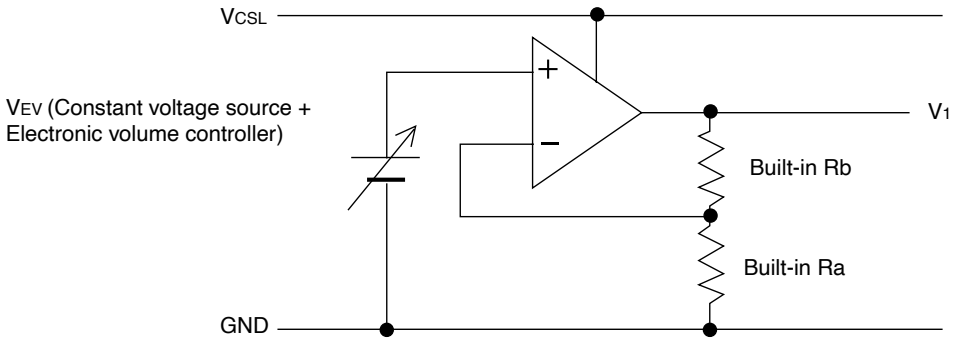


Fig. 8.11.3 Voltage Regulator Circuit

Rb/Ra in Equation A-1 is the resistance ratio of the built-in V1 voltage-regulating resistance. This ratio can be varied in 8 levels by changing parameters 2(P2) of electronic volum control command. Reference ratios of "1 + Rb/Ra" are shown in Table 8.11.4.

Table 8.11.4 Resistance Ratio of Built-in V2 Voltage-Regulating Resistance: Parameters and "1+ R/Ra" Ratio (For reference)

Parameter			1+Rb/Ra ratio	V1 voltage value
P22	P21	P20		
0	0	0	2.9032	Small
0	0	1	3.1914	
0	1	0	3.4090	•
0	1	1	3.6585	•
1	0	0	3.8793	•
1	0	1	4.0909	•
1	1	0	4.3269	
1	1	1	4.5454	Large

(B) V1 voltage control external resistor
If you use an external resistance control model, you can set the V1 voltage using an external resistor. Use a semi-fixed resistor for V1 voltage regulation.

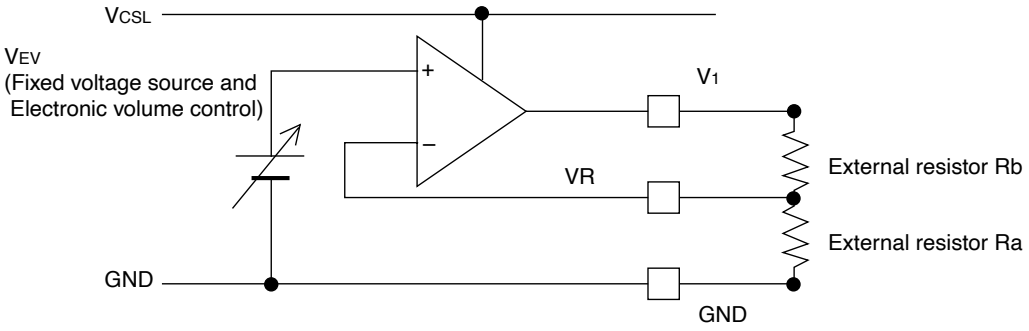


Fig. 8.11.4 Voltage Regulator Circuit

Select the external Ra and Rb values to allow stable voltage supply by observing the V2 voltage waveforms.
As the VR pin has a high input impedance and it is susceptible to ambient noise, the resistors and their leads must be placed in a short distance and they must be away from the clock source.

(C) Constant Voltage Source and Electronic Volume Control Circuit
The constant voltage source generates VREG - the reference voltage inside the IC. You can specify one of four types of temperature gradients with parameters of electronic volum control command. See Fig. 8.11.5.

Table 8.11.5 Parameters and VREG Temperature Gradient

Parameter		Temperature gradient (%/°C)
0	0	–0.05
0	1	–0.1
1	0	–0.15
1	1	–0.2

The electronic volume control circuit varies α in Equation A-1 according to parameters 1(P1) of electronic volum control command. Table 8.11.6 lists relation between the parameters and α.

Table 8.11.6 Parameters and Electronic Volume

Parameter						α	V1 voltage value
P15	P14	P13	P12	P11	P10		
0	0	0	0	0	0	63	Small
0	0	0	0	0	1	62	
0	0	0	0	1	0	61	
			•			•	•
			•			•	•
			•			•	•
1	1	1	1	0	1	2	
1	1	1	1	1	0	1	
1	1	1	1	1	1	0	Large

8.11.5 Voltage Divider/Voltage Follower Circuit

The voltage divider/voltage follower circuit V_1 output from the voltage regulator circuit and then generates liquid crystal drive voltages V_C using the operational amplifier-featured voltage follower.
Capacitors may be required for voltage regulation between the GND and each of V_C pin due to the load of LCD panel. Insert the capacitors, if necessary, by observing the voltage waveforms and current consumption.
The following theoretical equation is the potential relationship.
When the capacitor C is connected between CAP2+ and CAP2– and between V_2 and GND, the primary booster boosts the voltage from V_1 and MV_1 and generates V_2.

$V_C = 2/3 \times V_1$
$MV_1 = 1/3 \times V_1$
$V_2 = 4/3 \times V_1$

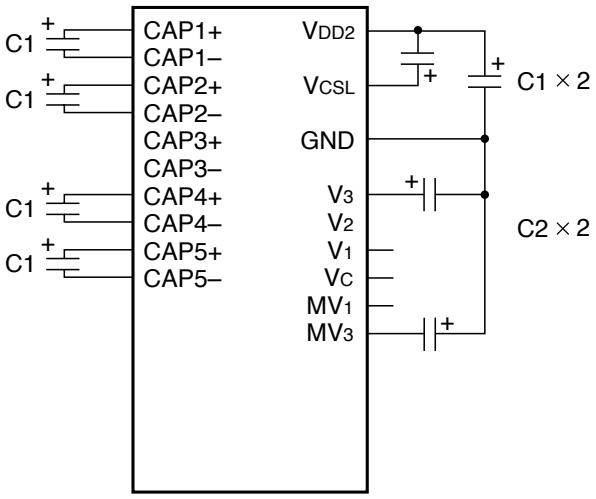
8.11.6 Secondary Booster Circuit / Step-Down Circuit

The secondary booster/step-down circuit boosts or steps down based on V_2, GND and produces V_3 and MV_3.
Their potential relationship is expressed with the following theoretical equation:

$V_3 = 2 \times V_2$
$MV_3 = -V_2$

8.11.7 Samples of Connections Peripheral to Power Circuit (For your information)

Following illustrates the connections when the entire power circuit is used.



Sample of common setting

Item	Setting	Unit
C1	1.0 to 4.7	μF
C2	0.47 to 1.0	

Optimum values of C1 and C2 above vary depending on the LCD panel to be driven. Above values should be referenced as information only. It is recommended to check how patterns with high load are displayed before finalizing the values.
C between V_{DD2} and GND signifies a bias capacitor.

9. COMMANDS

9.1 Command List

Following table lists the control signals and commands using the 80 series interface as the example.

Command		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function	Hex	Parameter
1	DISON	0	1	0	1	0	1	0	1	1	1	1	Display on	AF	None
2	DISOFF	0	1	0	1	0	1	0	1	1	1	0	Display off	AE	None
3	DISNOR	0	1	0	1	0	1	0	0	1	1	0	Normal display	A6	None
4	DISINV	0	1	0	1	0	1	0	0	1	1	1	Inverse display	A7	None
5	COMSCN	0	1	0	1	0	1	1	1	0	1	1	Common scan direction	BB	1byte
6	DISCTL	0	1	0	1	1	0	0	1	0	1	0	Display control	CA	3byte
7	SLPIN	0	1	0	1	0	0	1	0	1	0	1	Sleep in	95	None
8	SLPOUT	0	1	0	1	0	0	1	0	1	0	0	Sleep out	94	None
9	PASET	0	1	0	0	1	1	1	0	1	0	1	Page address set	75	2byte
10	CASET	0	1	0	0	0	0	1	0	1	0	1	Column address set	15	2byte
11	DATCTL	0	1	0	1	0	1	1	1	1	0	0	Data scan direction, etc.	BC	3byte
12	RGBSET8	0	1	0	1	1	0	0	1	1	1	0	256-color position set	CE	20byte
13	RAMWR	0	1	0	0	1	0	1	1	1	0	0	Writing to memory	5C	Data
14	RAMRD	0	1	0	0	1	0	1	1	1	0	1	Reading from memory	5D	Data
15	PTLIN	0	1	0	1	0	1	0	1	0	0	0	Partial display in	A8	2byte
16	PTLOUT	0	1	0	1	0	1	0	1	0	0	1	Partial display out	A9	None
17	RMWIN	0	1	0	1	1	1	0	0	0	0	0	Read and modify write	E0	None
18	RMWOUT	0	1	0	1	1	1	0	1	1	1	0	End	EE	None
19	ASCSET	0	1	0	1	0	1	0	1	0	1	0	Area scroll set	AA	4byte
20	SCSTART	0	1	0	1	0	1	0	1	0	1	1	Scroll start set	AB	1byte
21	OSCON	0	1	0	1	1	0	1	0	0	0	1	Internal oscillation on	D1	None
22	OSCOFF	0	1	0	1	1	0	1	0	0	1	0	Internal oscillation off	D2	None
23	PWRCTR	0	1	0	0	0	1	0	0	0	0	0	Power control	20	1byte
24	VOLCTR	0	1	0	1	0	0	0	0	0	0	1	Electronic volume control	81	2byte
25	VOLUP	0	1	0	1	1	0	1	0	1	1	0	Increment electronic control by 1	D6	None
26	VOLDOWN	0	1	0	1	1	0	1	0	1	1	1	Decrement electronic control by 1	D7	None
27	TMPGRD	0	1	0	1	0	0	0	0	0	1	0	Temperature gradient set	82	14byte
28	EPCTIN	0	1	0	1	1	0	0	1	1	0	1	Control EEPROM	CD	1byte
29	EPCOUT	0	1	0	1	1	0	0	1	1	0	0	Cancel EEPROM control	CC	None
30	EPMWR	0	1	0	1	1	1	1	1	1	0	0	Write into EEPROM	FC	None
31	EPMRD	0	1	0	1	1	1	1	1	1	0	1	Read from EEPROM	FD	None
32	EPSRRD1	0	1	0	0	1	1	1	1	1	0	0	Read register 1	7C	None
33	EPSRRD2	0	1	0	0	1	1	1	1	1	0	1	Read register 2	7D	None
34	NOP	0	1	0	0	0	1	0	0	1	0	1	NOP instruction	25	None
35	STREAD	0	0	1	Status								Status read		

(1) Display ON (DISON) Command: 1 Parameter: None
It is used to turn the display on. When the display is turned on, segment outputs and common outputs are generated at the level corresponding to the display data and display timing. You can't turn on the display as long as the sleep mode is selected. Thus, whenever using this command, you must cancel the sleep mode first.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	1

(2) Display OFF (DISOFF) Command: 1 Parameter: 0
It is used to forcibly turn the display off. As long as the display is turned off, every segment and common outputs are forced to VC level and $\overline{DOFF}$ pin is caused to LOW.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	1	1	0

(3) Normal display (DISNOR) Command: 1 Parameter: 0
It is used to normally highlight the display area without modifying contents of the display data RAM.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	0

(4) Inverse display (DISINV) Command: 1 Parameter: 0
It is used to inversely highlight the display area without modifying contents of the display data RAM. This command does not invert non-display areas in case of using partial display.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	0	1	1	1

(5) Common scan (COMSCAN) Command: 1 Parameter: 1
It is used to specify the common output scan direction. This command helps increasing degrees of freedom of wiring on the LCD panel.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	0	1	1	—
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Common scan direction

When 1/132 is selected for the display duty, pins and common output are scanned in the order shown below.

P12	P11	P10	Common scan direction					
			COM1 pin		COM68 pin	COM69 pin		COM132 pin
0	0	0	1	→	68	69	→	132
0	0	1	1	→	68	132	←	69
0	1	0	68	←	1	69	→	132
0	1	1	68	←	1	132	←	69

(6) Display control (DISCTL) Command: 1 Parameter: 3
This command and succeeding parameters are used to perform the display timing-related setups. This command must be selected before using SLPOUT. Don't change this command while the display is turned on.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	0	1	0	—
Parameter1 (P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	CL dividing ratio, F1 and F2 drive pattern.
Parameter2 (P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Drive duty
Parameter3 (P3)	1	1	0	*	*	*	P34	P33	P32	P31	P30	FR inverse-set value
Parameter4 (P4)	1	1	0	*	*	*	*	*	*	*	P40	Dispersion/non-dispersion

*: Invalid bits irrelevant to the operation.

P1: It is used to specify the CL dividing ratio, F1 and F2 drive-pattern switching period.
P14, P13, P12: CL dividing ratio. They are used to change number of dividing stages of external or internal clock.

P14	P13	P12	CL dividing ratio
0	0	0	2 divisions (default)
0	0	1	4 divisions
0	1	0	8 divisions
0	1	1	Not divide

P11, P10: They are used to change F1 and F2 drive-pattern switching period.

P11	P10	F1, F2 switching period
0	0	8H (default)
0	1	4H
1	0	16H
1	1	Field

P2: It is used to specify the duty of the module on block basis.

Duty	*	*	P25	P24	P23	P22	P21	P20	(Numbers of display lines)/4-1
Example: 1/128 duty	0	0	0	1	1	1	1	1	128/4–1=31

P3: It is used to specify number of lines to be inversely highlighted on LCD panel from P33 to P30 (lines can be inversely highlighted in the range of 2 to 16)

Inversely highlighted lines	*	*	*	P34	P33	P32	P31	P30	Inversely highlighted lines –1
Example: 11H	0	0	0	0	1	0	1	0	11–1=10
Example: 13H	0	0	0	0	1	1	0	0	13–1=12

In the default, 11H inverse highlight is selected.
P34= "0": Inversion occurs every frame. P34= "0": Independent from frames
P4: It is used to set dispersion or non-dispersion for the LCD driving method.

P40= "0": Dispersion P40= "1": Non-dispersion

(7) Seep in (SLPIN) Command: 1 Parameter: 0
Entering this command generates LOW at $\overline{SLP}$ pin.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	1

$\overline{DOFF}$ (LCD panel blanking control pin) on S1D15G10 is caused to LOW when the sleep in mode is turned on.

(8) Sleep out (SLPOUT) Command: 1 Parameter: 0
Entering this command generates HIGH at $\overline{SLP}$ pin.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	0	1	0	1	0	0

(9) Page address set (PASET) Command: 1 Parameter: 2
When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the page address area. As the addresses are incremented from the start to the end page in the page-direction scan, the column address is incremented by 1 and the page address is returned to the start page. Note that the start and end page must be specified as a pair. Also, the relation "start page < end page" must be maintained.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	1	1	0	1	0	1	—
Parameter1 (P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start page
Parameter2 (P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End page

(10) Column address set (CASET) Command: 1 Parameter: 2
When MPU makes access to the display data RAM, this command and succeeding parameters are used to specify the column address area. As the addresses are incremented from the start to the end column in the column-direction scan, the page address is incremented by 1 and the column address is returned to the start column. Note that the start and end page must be specified as a pair. Also, the relation "start column < end column" must be maintained.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	0	1	0	1	0	1	—
Parameter1 (P1)	1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Start address
Parameter2 (P2)	1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	End address

(11) Data control (DATCTL) Command: 1 Parameters: 2
This command and succeeding parameters are used to perform various setups needed when MPU operates display data stored on the built-in RAM.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	1	1	1	0	0	—
Parameter1 (P1)	1	1	0	*	*	*	*	*	P12	P11	P10	Normal/inverse display of page address and page-address scan direction.
Parameter2 (P2)	1	1	0	*	*	*	*	*	*	*	P20	RGB arrangement
Parameter3 (P3)	1	1	0	*	*	*	*	*	P32	P31	P30	Gray-scale setup

P1: It is used to specify the normal or inverse display of the page address and also to specify the page address scanning direction.
P10: Normal/inverse display of the page address. P10 = 0: Normal and P10 = "1": Inverse.
P11: Normal/reverse turn of column address. P11 = "0": Normal rotation and P11 = "1": Reverse rotation
P12: Address-scan direction. P12 = "0": In the column direction and P12 = "1": In the page direction.

P2: RGB arrangement. This parameter allows you to change RGB arrangement of the segment output according to RGB arrangement on the LCD panel. In this case, writing position of data {R = (D7, D6, D5), G = (D4, D3, D2), B = (D1, D0)} on the display memory is changed.

P20	line	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	•••	SEG395
0	Even page	R	G	B	R	G	B	R	G	•••	B
	Odd page	R	G	B	R	G	B	R	G	•••	B
1	1	B	G	R	B	G	R	B	G	•••	R
	2	B	G	R	B	G	R	B	G	•••	R

In the default, (P20) = (0) is selected.

P3: Gray-scale setup. Using this parameter, you can a select desired display colors between the 256 colors (8 gray-scale) or 4096 colors (16 gray-scale) for the display color. For 16 gray-scale display, you can select the Type A or Type B display mode depending on the difference in RGB data arrangement you use.

P32	P31	P30	Numbers of gray-scale
0	0	1	8 gray-scale
0	1	0	16 gray-scale display Type A
1	0	0	16 gray-scale display Type B

(12) 256-color position set (RGBSET8) Command: 1 Parameter: 0
When turning on 256-color display (8 gray-scale), this command allows you to choose colors to represent each of red, green and blue from 4096 colors.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	1	1	0	—
Parameter1 (P1)	1	1	0	*	*	*	*	P13	P12	P11	P10	Intermediate red tone 000
Parameter4 (P8)	1	1	0	*	*	*	*	P83	P82	P81	P80	Intermediate red tone 111
Parameter9 (P9)	1	1	0	*	*	*	*	P93	P92	P91	P90	Intermediate green tone 000
Parameter16 (P16)	1	1	0	*	*	*	*	P163	P162	P161	P160	Intermediate green tone 111
Parameter17 (P17)	1	1	0	*	*	*	*	P173	P172	P171	P170	Intermediate blue tone 00
Parameter20 (P20)	1	1	0	*	*	*	*	P203	P202	P201	P200	Intermediate blue tone 11

Data (Red and Green: 3 bits and Blue: 2 bits) to be written from the MPU to the DDRAM are converted to 4-bit data before the write operation takes place. When reading data from the DDRAM, data on red and green are converted to 3 bits and that on blue are converted to 2 bits before the output.

(13) Memory write (RAMWR) Command: 1 Parameter: Numbers of data written
When MPU writes data to the display memory, this command turns on the data entry mode. Entering this command always sets the page and column addresses at the start address. You can rewrite contents of the display data RAM by entering data succeeding to this command. At the same time, this operation increments the page or column address as applicable. The write mode is automatically cancelled if any other command is entered.
① 8-bit bus

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	0	—
Parameter	1	1	0	Data to be written								Data to be written

② 16-bit bus

Command name	A0	$\overline{RD}$	$\overline{WR}$	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	*	*	*	0	1	0	1	1	1	0	0	Memory write
Data to be written	1	1	0	Data to be written																Write data

(14) Memory read (RAMRD) Command: 1 Parameter: Numbers of data read
When MPU reads data from the display memory, this command turns on the data read mode. Entering this command always sets the page and column addresses at the start address. After entering this command, you can read contents of the display data RAM. At the same time, this operation increments the page or column address as applicable. The data read mode is automatically cancelled if any other command is entered.
① 8-bit bus

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	1	0	1	1	1	0	1	—
Parameter	1	0	1	Data to be read								Data to be read

② 16-bit bus

Command name	A0	$\overline{RD}$	$\overline{WR}$	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	*	*	*	*	*	*	*	*	0	1	0	1	1	1	0	1	Memory read
Data to be read	1	0	1	Data to be read																Read data

(15) Partial in (PTLIN) Command: 1 Parameter: 2
This command and succeeding parameters specify the partial display area. This command is used to turn on partial display of the screen (dividing screen by lines) in order to save power. Since S1D15G10 processes the liquid crystal display signals on 4-line basis (block basis), the display and non-display areas are also specified on 4-bit line (block basis).

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	0	0	—
Parameter1 (P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address
Parameter2 (P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	End block address

*: Invalid bits irrelevant with the operation.

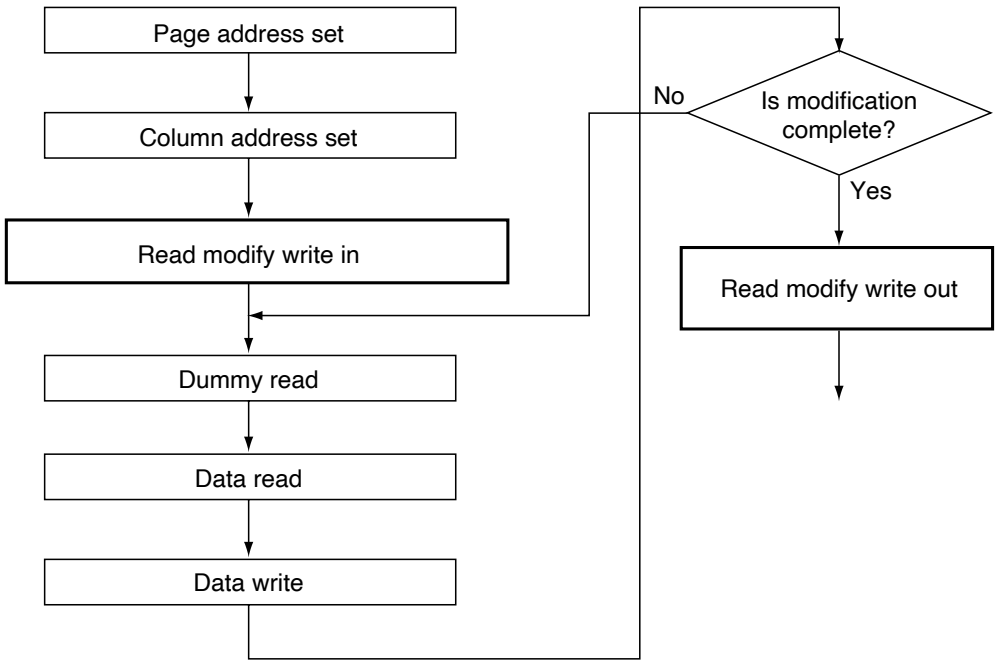
A block address that can be specified for the partial display must be the displayed one (don't try to specify an address not to be displayed when scrolled).
When the partial display mode is turned on, following state is introduced to S1D15G10 in the non-display area:
* LOW is output to $\overline{DOFF}$ pin.
* All COM pins output V_C.
* All SEG pins output V_1 or MV_1.
SEG output is forced to V_1 or MV_1 depending on state of FR in the last display line. When FR is HIGH, V_1 is output and when FR is LOW, MV_1 is output. Phase of FR is constantly reversed at start of a frame.

(16) Partial out (PTLOUT) Command: 1 Parameter: 0
This command is used to exit from the partial display mode.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	0	1	0	1	0	0	1

(17) Read modify write in (RMWIN) Command: 1 Parameter: 0
This command is used along with the column address set command, page address set command and read modify write out command. This function is used when frequently modifying data to specify a specific display area such as blinking cursor. First set a specific display area using the column and page address commands. Then, enter this command to set the column and page addresses at the start address of the specific area. When this operation is complete, the column (page) address won't be modified by the display data read command. It is incremented only when the display data write command is used. You can cancel this mode by entering the read modify write out or any other command.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	0	0	0	0



(18) Read modify write out (RMWOUT) Command: 1 Parameter: 0
Entering this command cancels the read modify write mode.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	0	1	1	1	0

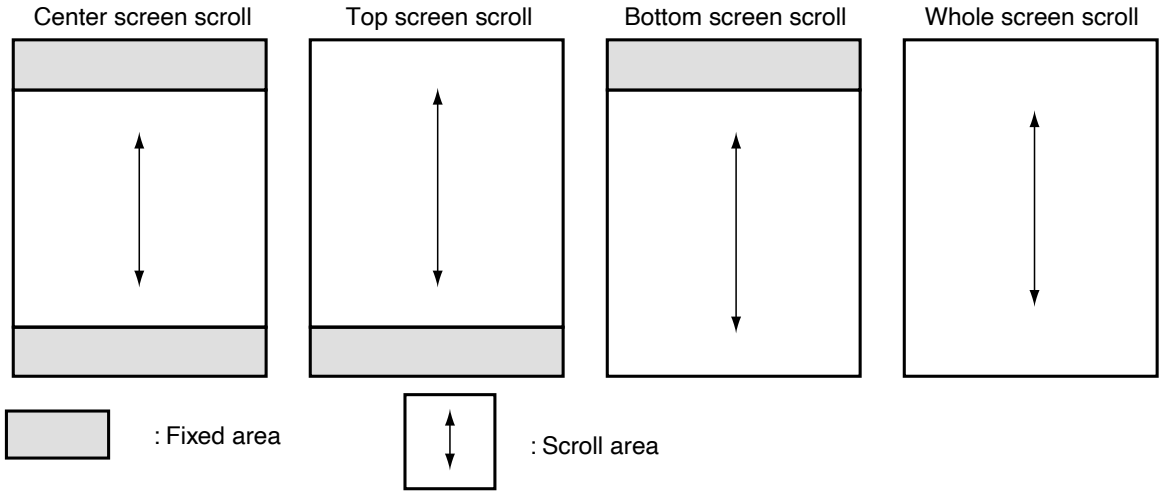
(19) Area scroll set (ASCSET) Command: 1 Parameter: 4
It is used when scrolling only the specified portion of the screen (dividing the screen by lines). This command and succeeding parameters specify the type of area scroll, FIX area and scroll area.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	0	—
Parameter1 (P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Top block address
Parameter2 (P2)	1	1	0	*	*	P25	P24	P23	P22	P21	P20	Bottom block address
Parameter3 (P3)	1	1	0	*	*	P35	P34	P33	P32	P31	P30	Number of specified blocks
Parameter4 (P4)	1	1	0	*	*	*	*	*	*	P41	P40	Area scroll mode

*: Invalid bits irrelevant with the operation.

P4: It is used to specify an area scroll mode.

P41	P40	Types of area scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll



Since S1D15G10 processes the liquid crystal display signals on the four-line basis (block basis), FIX and scroll areas are also specified on the four-line basis (block basis).
DDRAM address corresponding to the top FIX area is set in the block address incrementing direction starting with 0 block. DDRAM address corresponding to the bottom FIX area is set in the block address decreasing direction starting with 41st block. Other DDRAM blocks excluding the top and bottom FIX areas are assigned to the scroll + background areas.

P1: It is used to specify the top block address of the scroll + background areas. Specify the 0th block for the top screen scroll or whole screen scroll.
The scroll start block address is also set at this top block address until the scroll-start block set command specifies the address.
P2: It specifies the bottom address of the scroll + background areas. Specify the 32th block for the bottom or whole screen scroll.
Required relation between the start and end blocks (top block address < bottom block address) must be maintained.
P3: It specifies a specific number of blocks {Numbers of (Top FIX area + Scroll area) blocks - 1}. When the bottom scroll or whole screen scroll, the value is identical with P2.

You can turn on the area scroll function by executing the area scroll set command first and then specifying the display start block of the scroll area with the scroll start set command.

[Area Scroll Setup Example]
In the center screen scroll of 1/120 duty (display range: 120 lines = 30 blocks), if 8 lines = 2 blocks and 8 lines = 2 blocks are specified for the top and bottom FIX areas, 104 lines = 26 blocks is specified for the scroll areas, respectively, 12 lines = 3 blocks on the DDRAM are usable as the background area. Value of each parameter at this time is as shown below.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
P1	1	1	0	*	*	0	0	0	0	1	0	Top block address = 2
P2	1	1	0	*	*	0	1	1	1	1	0	Bottom block address = 30
P3	1	1	0	*	*	0	1	1	0	1	1	Number of specific blocks = 27
P4	1	1	0	*	*	*	*	*	*	0	0	Area scroll mode = Center

*: Invalid bits irrelevant to the operations.

(20) Scroll start address set (SCSTART) Command: 1 Parameter: 1
This command and succeeding parameter are used to specify the start block address of the scroll area. Note that you must execute this command after executing the area scroll set command. Scroll becomes available by dynamically changing the start block address.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	1	0	1	0	1	1	—
Parameter1 (P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	Start block address

*: Invalid bits irrelevant to the operations.

(21) Internal oscillation on (OSCON) Command: 1 Parameter: 0
This command turns on the internal oscillation circuit. It is valid only when the internal oscillation circuit of CLS = HIGH is used.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	0	1

(22) Internal oscillation off (OSOFF) Command: 1 Parameter: 0
It turns off the internal oscillation circuit. This circuit is turned off in the reset mode.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	0	1	0

(23) Power control set (PWRCTR) Command: 1 Parameter: 1
This command is used to turn on or off the liquid crystal driving power circuit, booster/step-down circuits and voltage follower circuit.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	0	0	1	0	0	0	0	0	—
Parameter1 (P1)	1	1	0	*	*	*	P14	P13	P12	P11	P10	LCD drive power

*: Invalid bits irrelevant to the operations.

P10: It turns on or off the Reference voltage generation circuit.
P10 = "1": ON. P10 = "0": OFF.
P11: It turns on or off the voltage regulator and circuit voltage follower.
P11 = "1": ON. P11 = "0": OFF.
Note: 2 bits of P10 and P11 must be turned on or off simultaneously.
P12: It turns on or off the secondary booster/step-down circuit.
P12 = "1": ON. P12 = "0": OFF.
P13: It turns on the primary booster circuit.
P13 = "1": ON. P13 = "0": OFF.
P14: It is used to select either external resistance using the V_R terminal or control via EEPROM access to adjust V_1 voltage.
P14 = "1": External resistance P14 = "0": EEPROM

(24) Electronic volume control (VOLCTR) Command: 1 Parameter: 2
This command is used to specify the voltage regulator circuit's electronic volume value α and resistance ratio of built-in voltage regulating resistor.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	0	1	
Parameter1 (P1)	1	1	0	*	*	P15	P14	P13	P12	P11	P10	V_1 volume value α
Parameter2 (P2)	1	1	0	*	*	*	*	*	P22	P21	P20	1 + Rb/Ra

*: Invalid bits irrelevant to the operations.
P1: It is used to specify V_1 electronic volume value.
P2: It specifies resistance ratio of the internal resistor.

(25) Increment Electronic Control (VOLUP) Command: 1 Parameter: No
This command increments Electronic Control value α of voltage regulator circuit by 1.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	0

If you set the Electronic Control value to 111111, the control value is set to 000000 after this command has been executed.

(26) Decrement Electronic Control (VOLDOWN) Command: 1 Parameter: No
This command decrements Electronic Control value α of voltage regulator circuit by 1.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	1	0	1	1	1

If you set the Electronic Control value to 000000, the control value is set to 111111 after this command has been executed.

(27) Temperature Gradient Setting (TMPGRD) Command : 1, Parameter : 14

The average temperature gradient of the voltage for a liquid crystal drive voltage is set up with this command.
Set parameters P2 to P14 as in a table below.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	0	0	0	0	0	1	0	
Parameter1 (P1)	1	1	0	*	*	*	*	*	*	P11	P10	Average temperature gradient
Parameter2 (P2)	1	1	0	0	0	0	0	0	0	0	0	
Parameter3 (P3)	1	1	0	0	0	0	0	0	0	0	0	
Parameter4 (P4)	1	1	0	0	0	0	0	0	0	0	0	
Parameter5 (P5)	1	1	0	0	0	0	0	0	0	0	0	
Parameter6 (P6)	1	1	0	*	*	0	0	0	0	0	0	
Parameter7 (P7)	1	1	0	*	*	0	0	0	0	0	0	
Parameter8 (P8)	1	1	0	*	*	0	0	0	0	0	0	
Parameter9 (P9)	1	1	0	*	*	0	0	0	0	0	0	
Parameter10 (P10)	1	1	0	*	*	0	0	0	0	0	0	
Parameter11 (P11)	1	1	0	*	*	0	0	0	0	0	0	
Parameter12 (P12)	1	1	0	*	*	0	0	0	0	0	0	
Parameter13 (P13)	1	1	0	*	*	*	*	*	*	*	0	
Parameter14 (P14)	1	1	0	*	*	0	0	0	0	0	0	

P1: It specifies average temperature gradient.

P11	P10	Average temperature gradient [%/°C]
0	0	–0.05
0	1	–0.1
1	0	–0.15
1	1	–0.2

P2 to P14: Set the parameter as the table shown previously.

(28) Control EEPROM (EPCTIN) Command: 1 Parameter: 1
This command with its parameter selects the EEPROM (S1F17A10) Control mode. The parameter can be set to either Write or Read.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Function
Command	0	1	0	1	1	0	0	1	1	0	1	—
Parameter1 (P1)	1	1	0	*	*	P5	*	*	*	*	*	Selects Write or Read.

* Invalid bit; it is ignored during operation.

P5: Specifies data writing into or reading from the EEPROM (S1F17A10) as follows.
If P5=0: Read; if P5=1: Write

(29) Cancel EEPROM Control (EPCOUT) Command: 1 Parameter: 0
This command cancels the EEPROM (S1F17A10) Control mode. If data is read from the EEPROM, both of Electronic Control value and built-in resistance ratio are updated by the read data.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	0	0	1	1	0	0

(30) Write Into EEPROM (EPMWR) Command: 1 Parameter: 0
This command writes the Electronic Control value and built-in resistance ratio into the EEPROM (S1F17A10).

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	0

(31) Read From EEPROM (EPMRD) Command: 1 Parameter: 0
This command reads the Electronic Control value and built-in resistance ratio from the EEPROM (S1F17A10), and temporarily stores them in S1D15G10 registers.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	1	1	1	1	1	1	0	1

(32) Read Register 1 (EPSRRD1) Command: 1 Parameter: 0
Issue the EPSRRD1 and STREAD (Status Read) commands in succession to read the Electronic Control value.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	0

Issue the Status Read command immediately after this command. Also, always issue the NOP command after the STREAD (Status Read) command.

(33) Read Register 1 (EPSRRD2) Command: 1 Parameter: 0
Issue the EPSRRD1 and STREAD (Status Read) commands in succession to read the built-in resistance ratio.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	1	1	1	1	1	0	1

Issue the Status Read command immediately after this command. Also, always issue the NOP command after the STREAD (Status Read) command.

(34) Non-operating (NOP) Command: 1 Parameter: 0
This command does not affect the operation.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	1	0	0	0	1	0	0	1	0	1

This command, however, has the function of canceling the IC test mode. Thus, it is recommended to enter it periodically to prevent malfunctioning due to noise and such.

(35) Status read (STREAD)
It is the command for reading the internal condition of the IC. Three statuses can be displayed depending on the setting.

	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
Command	0	0	1	Status data							

① Status after reset or after NOP operation

D7: Area scroll mode	Refer to P41 (ASCSET).	
D6: Area scroll mode	Refer to P40 (ASCSET).	
D5: Read modify write	0: Out	1: In
D4: Scan direction	0: Page	1: Column
D3: Display ON/OFF	0: OFF	1: ON
D2: EEPROM access	0: Out of access	1: In access
D1: Display normal/inverse	0: Inverse	1: Normal
D0: Partial display	0: OFF	1: ON

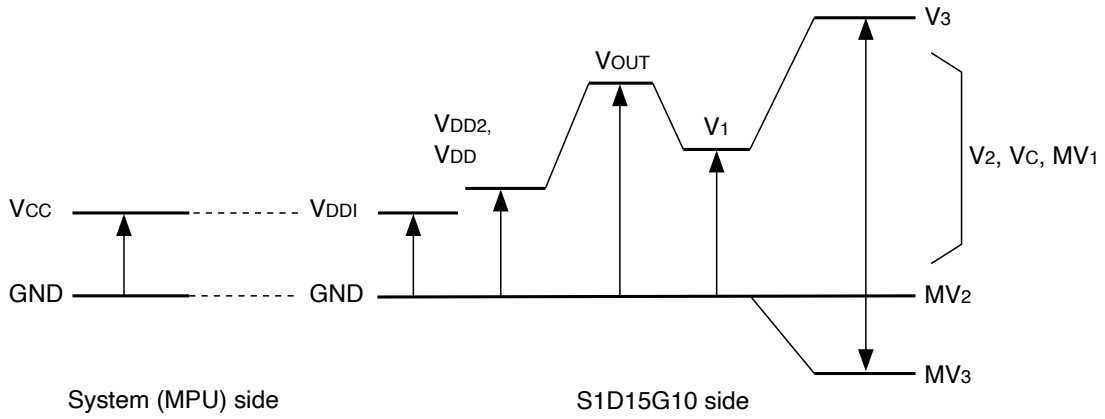
② Status after EPSRRD1 operation
D7, D6: Undefined (1 or 0)
D5 to D0: Electronic volume control values

③ Status after EPSRRD2 operation
D7 to D3: Undefined (1 or 0)
D2 to D0: Built-in resistance ratio

10. ABSOLUTE MAXIMUM RATING

Item		Symbol	Rating	Unit
Source voltage (1)		V_{DD},V_{DD2}	–0.3 to 4.0	V
Input source voltage		V_{DDI}	–0.3 to 4.0	V
Source voltage (2)		V_3,V_{OUT}	–0.3 to 25.0	V
Source voltage (3)		V_2,V_1,V_C	–0.3 to V_3	V
		MV_1	–0.3 to V_{DD2}	
		MV_3	–10.0 to +0.5	
Input voltage		V_{IN}	–0.3 to V_{DDI}+0.5	V
Output voltage		V_O	–0.3 to V_{DDI}+0.5	V
Operating temperature		Topr	–40 to +85	°C
Storage temperature	Bare chip	Tstr	–65 to +150	°C

Potential Relation



Notes: 1. Voltages are all indicated relevant to GND = 0V.
2. Voltage of V_3, V_2, V_1, V_C, MV_1, MV_2 (GND) and MV_3 must constantly meets the requirement $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2$ (GND) $\geq MV_3$.
3. V_{DD} and V_{OUT} voltages must constantly meets the requirement $V_{OUT} \geq V_{DD}$.
4. If LSI is operated beyond the absolute maximum rating, it can be damaged permanently. Normal operating conditions should conform to the electric characteristics of LSI, otherwise malfunctioning of LSI can result in addition to deterioration of its reliability.
5. Definition of V_{DD} is applicable to V_{DD3}, V_{DD4} and V_{DD5} pins.
6. Definition of GND is applicable to GND2, GND3 and GND4 pins.

11. ELECTRIC CHARACTERISTICS

11.1 DC Characteristics

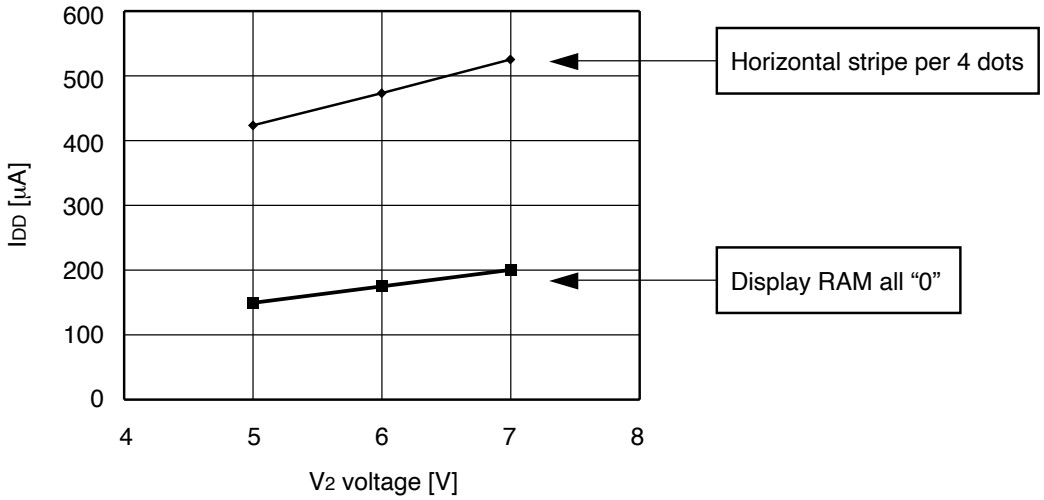
Except where otherwise specified, GND = 0V, V_{DD} = 2.75V, V_{DDI} = 1.8V and Ta = 20°C to 85°C.

Table 11.1

Item		Symbol	Condition	Standard value			Unit	Applicable pin
				Min.	Typ.	Max.		
Operating voltage (1)	Operable	V_{DD}	—	2.6	2.75	3.6	V	V_{DD} *1
Operating voltage (2)	Operable	V_{DDI}	—	1.7	1.8	V_{DD}	V	V_{DDI}
Operating voltage (3)	Operable	V_3	V_3 to MV_3	12.0	—	21.0	V	V_3
	Operable	V_3	—	8.0	—	14.0	V	V_3
	Operable	V_2	—	4.0	—	7.0	V	V_2
	Operable	V_1	—	3.0	—	5.3	V	V_1
	Operable	V_C	—	2.0	—	3.5	V	V_C
	Operable	MV_1	—	1.0	—	1.8	V	MV_1
	Operable	MV_2	—	GND	—	GND	V	MV_2
	Operable	MV_3	—	–7.0	—	–4.0	V	MV_3
High level input voltage		V_{IHC}	—	0.8×V_{DDI}	—	V_{DDI}	V	*2
				0.7×V_{DDI}	—	V_{DDI}	V	*3
Low level input voltage		V_{ILC}	—	0.0	—	0.2×V_{DDI}	V	*2
				0.0	—	0.3×V_{DDI}	V	*3
High level output voltage		V_{OH}	IOH=–0.6mA	V_{DDI}–0.4	—	V_{DDI}	V	*4
Low level output voltage		V_{OL}	IOL=+0.6mA	0.0	—	0.4	V	*4
Input leak current		ILI	V_{IN}=V_{DDI} or GND	—	—	1.0	μA	*3
Output leak current		ILO		—	—	1.0	μA	*4
Liquid crystal drive ON resistance		RONseg	V_2=5.0V, ΔV=0.5V	—	3.5	10	kΩ	SEGn *5
		RONcom	V_3=16.0V, ΔV=0.5V	—	0.4	1.0	kΩ	COMn *5
Static current consumption		IDDQ	V_{DD}=V_{DDI}=3.6V,Ta=25°C	—	2	10	μA	V_{DD}
		I3Q	V_3–MV_3=18.0V,Ta=25°C	—	—	1.5	μA	V_3
		I2Q	V_2=6.0V,Ta=25°C	—	—	3.0	μA	V_2
Dynamic current consumption		IDD	During RAM access 3MHz	—	500	750	μA	V_{DD}+V_{DDI}
			During display Frame frequency 180Hz	—	180	400	μA	V_{DD} *8
		V_{DDI}	During display on	—	5	20	μA	V_{DDI}
Input terminal capacity		CI	Freq.=1MHz	—	—	15	pF	*3
Output terminal capacity		CO	Ta=25°C, Elemental chip	—	—	15	pF	*4
Oscillated frequency	Internal oscillation	fOSC	180Hz device, Ta=25°C	45.2	47.6	50.0	kHz	*6
	External input	fCL	180Hz device, 1/132duty	—	47.6	—	kHz	CL *6

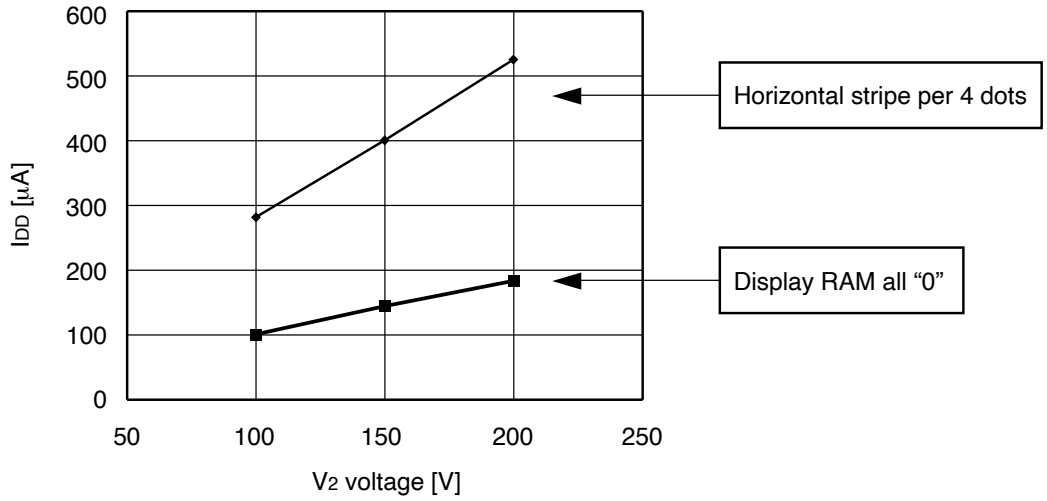
Table 11.2

	Item	Symbol	Condition	Standard value			Unit	Applicable pin
				Min.	Typ.	Max.		
Built-in power supply circuit	Input voltage to primary booster circuit	V_{DD2}	—	2.6	—	3.6	V	V_{DD}
	Output voltage from primary booster circuit	V_{OUT}	Double boosting, no load	5.2	—	7.2	V	V_{OUT}
	Primary booster circuit output impedance	Rout	Double boosting, V_{DD}=2.7V, C=2.2µF	—	400	—	Ω	V_{OUT}
	Reference voltage	V_{REG}	Ta=25°C	1.16	1.20	1.24	V	*7
	Voltage adjusting circuit output voltage	V_1	no load	3.0	—	5.25	V	V_2
	Secondary boosting output voltage	V_3		8.0	—	14.0	V	V_3
	Secondary step-down output voltage	MV_3		–7.0	—	–4.0	V	MV_3



Condition: V_{DD} = 2.75V, V_{DDI} = 1.8V, frame frequency 180Hz
During display, built-in power supply and external oscillation.
Typical value when Ta = 25°C

Fig. 11.1 Dynamic current consumption (During display, liquid crystal drive voltage dependent)

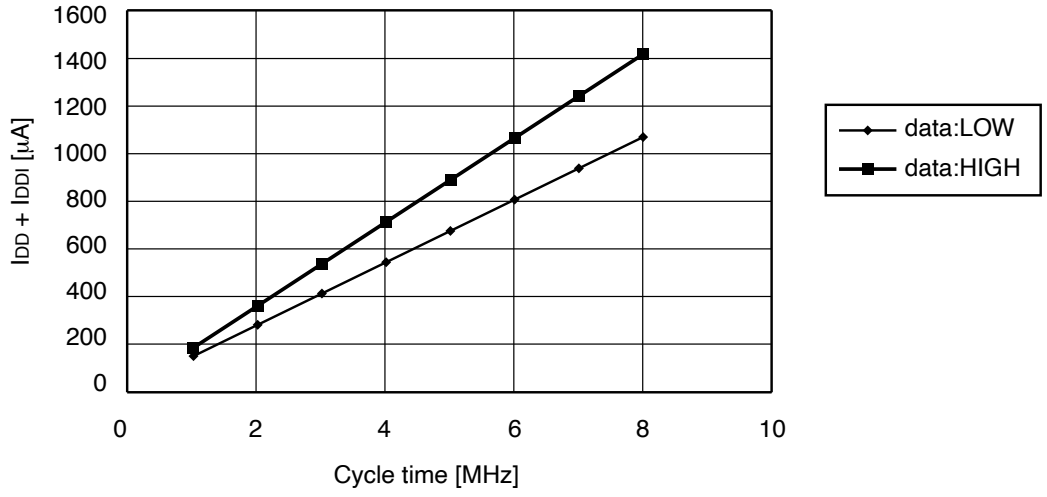


Condition: V_{DD} = 2.75V, V_{DDI} = 1.8V, V_2 = 6.0V
During display, built-in power supply and built-in oscillation circuit on.
Typical value when Ta = 25°C

Fig. 11.2 Dynamic current consumption (During display, frame frequency dependent)

Table 11.3 Current Consumption in Power Save Mode GND = 0V, V_{DD} = V_{DDI} = 1.8V, V_{DD} = 2.75V and Ta = 25°C.

Item	Symbol	Condition	Standard value			Unit	Applicable pin
			Min.	Typ.	Max.		
Sleep mode	I_{DDS}	—	—	1.0	10.0	μA	V_{DD}, V_{DDI}



Condition: V_{DD} = V_{DDI} = 3.0V, built-in power supply and built-in oscillation circuit off .
The interface is 8-bit parallel 80 system and the data is 16gray-scale Type A.
Typical value when Ta = 25°C.

Fig. 11.3 Dynamic current consumption (During display RAM access)

Table 11.4 Relation between Oscillated Frequency fosc, Display Clock Frequency fCL and Frame Frequency of Liquid Crystal

Item	fCL	fFR
When built-in oscillation circuit is used	43.2kHz (Typ.) *1	$\frac{f_{CL}/\text{Dividing ratio}}{2 \times \text{Display duty}}$
When built-in oscillation circuit is not used	External input (fCL)	$\frac{f_{CL}/\text{Dividing ratio}}{2 \times \text{Display duty}}$

*1: When 180Hz frame frequency device is used. (Display duty : 120, without dividing ratio)
fFR represents cycle of framing, not cycle of FR signal.
Dividing ratio and display duty are set with the display control command.

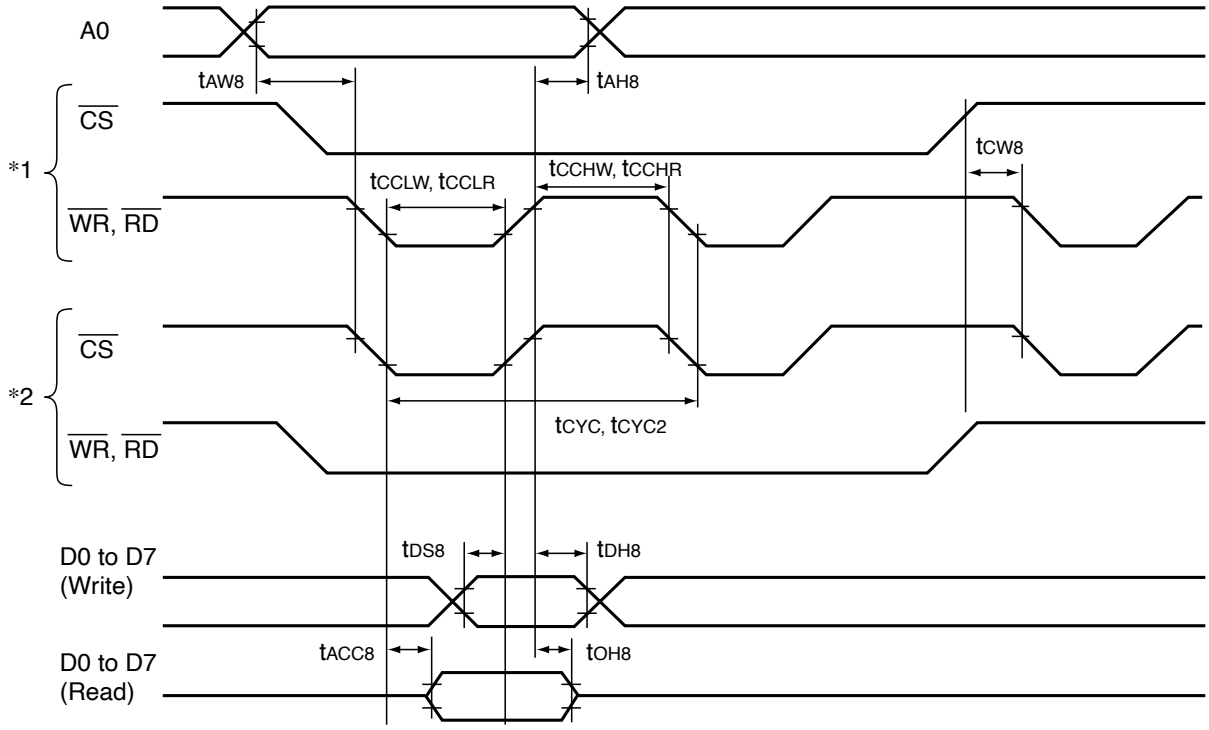
DC Characteristics - Supplementary Description

*1: Operation is warranted if radical voltage fluctuations occur while MPU is in the process of access.
*2: This applies only to $\overline{RES}$.
*3: D15 to D0 (Input mode)
SI, SCL IF1 to IF3, A0, CS, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{RES}$, M/S and CLS.
*4: D15 to D0 (Input and Output mode)
CL, FR SYNC, CA, F1, F2 and $\overline{DOFF}$.
*5: It represents the resistance value when 0.5V is applied across the output pin SEGn or COMn and respective power terminals (V_3, V_2, V_1, V_C, MV_1 and MV_2). It is specified within the range of the operating voltage (3).
RON = 0.5V/ΔI (ΔI is the current conducted when 0.5V is applied across the power supply and output pin).
*6: For the relation between oscillated frequency and frame frequency, refer to Table 11.4. The standard value listed in relation to the external input is a recommended value.
*7: This is the reference voltage source built into the IC. It is not output to the pin.
*8: It indicates the current consumed by the IC alone when the built-in oscillation circuit is in operation and the display is turned on. It does not include current consumed by the LCD panel capacity and wiring capacity. The value is applicable only when access is not being made by MPU.

11.2 AC Characteristics

System Bus

Read/write characteristics I (80 series MPU)



*1 is when access is made with $\overline{WR}$ and $\overline{RD}$ when $\overline{CS}$ is LOW.
*2 is when access is made with $\overline{CS}$ when $\overline{WR}$ and $\overline{RD}$ are LOW.

Ta=–40 to +85°C, V_{DD}=2.6 to 3.6V, V_{DDI}=2.6 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
A0	t_{AH8}	Address hold time	10	—	ns	—
	t_{AW8}	Address setup time	0	—	ns	
$\overline{WR}$, $\overline{RD}$,$\overline{CS}$	t_{CYC}	Write cycle	190	—	ns	—
	t_{CYC2}	Read cycle	250	—	ns	
	t_{CCHW}	Control pulse HIGH width (write)	140	—	ns	
	t_{CCHR}	Control pulse HIGH width (read)	70	—	ns	
	t_{CCLW}	Control pulse LOW width (write)	40	—	ns	
	t_{CCLR}	Control pulse LOW width (read)	170	—	ns	
	t_{CW8}	$\overline{CS}$–$\overline{WR}$, $\overline{RD}$ time	45	—	ns	
D0 to D7	t_{DS8}	Data setup time	10	—	ns	—
	t_{DH8}	Data hold time	20	—	ns	
	t_{ACC8}	Read access time	—	170	ns	C_L=10 to 100pF
	t_{OH8}	Output disable time	5	60	ns	

* Rise and fall time of input signal (t_r, t_f) must be 15 ns maximum.
* All timings must be specified using 30% and 70% of V_{DD}-GND as the reference.
* t_{CCLW} and t_{CCLR} are specified by the duration during which $\overline{CS}$ as well as $\overline{WR}$ and $\overline{RD}$ are LOW.
* A0 timing is specified by the duration during which $\overline{CS}$ as well as $\overline{WR}$ and $\overline{RD}$ are LOW.

Ta=–40 to +85°C, V_{DD}=2.6 to 3.6V, V_{DDI}=1.7 to 2.6V

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
A0	t_{AH8}	Address hold time	10	—	ns	—
	t_{AW8}	Address setup time	0	—	ns	
$\overline{WR}$, $\overline{RD}$,$\overline{CS}$	t_{CYC}	Write cycle	190	—	ns	—
	t_{CYC2}	Read cycle	250	—	ns	
	t_{CCHW}	Control pulse HIGH width (write)	140	—	ns	
	t_{CCHR}	Control pulse HIGH width (read)	70	—	ns	
	t_{CCLW}	Control pulse LOW width (write)	40	—	ns	
	t_{CCLR}	Control pulse LOW width (read)	170	—	ns	
	t_{CW8}	$\overline{CS}$–$\overline{WR}$, $\overline{RD}$ time	40	—	ns	
D0 to D7	t_{DS8}	Data setup time	10	—	ns	—
	t_{DH8}	Data hold time	20	—	ns	
	t_{ACC8}	Read access time	—	200	ns	C_L=10 to 100pF
	t_{OH8}	Output disable time	5	60	ns	

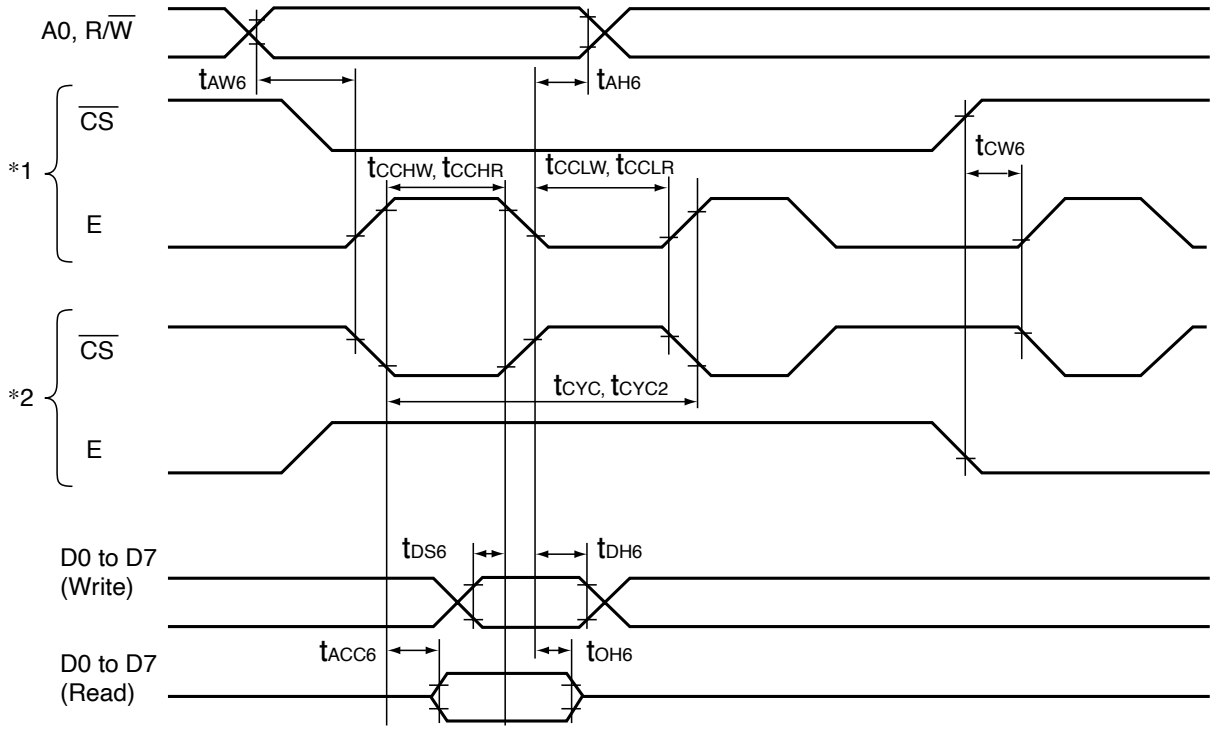
* Rise and fall time of input signal (t_r, t_f) must be 15 ns maximum.
* All timings must be specified using 30% and 70% of V_{DD}-GND as the reference.
* t_{CCLW} and t_{CCLR} are specified by the duration during which $\overline{CS}$ as well as $\overline{WR}$ and $\overline{RD}$ are LOW.
* A0 timing is specified by the duration during which $\overline{CS}$ as well as $\overline{WR}$ and $\overline{RD}$ are LOW.

Ta=–40 to +70°C, V_{DD}=V_{DDI}=2.9V±3%

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
A0	t_{AH8}	Address hold time	10	—	ns	—
	t_{AW8}	Address setup time	0	—	ns	
$\overline{WR}$, $\overline{RD}$,$\overline{CS}$	t_{CYC}	Write cycle	150	—	ns	*1
	t_{CYC2}	Read cycle	250	—	ns	
	t_{CCHW}	Control pulse HIGH width (write)	110	—	ns	
	t_{CCHR}	Control pulse HIGH width (read)	70	—	ns	
	t_{CCLW}	Control pulse LOW width (write)	35	—	ns	
	t_{CCLR}	Control pulse LOW width (read)	170	—	ns	
	t_{CW8}	$\overline{CS}$–$\overline{WR}$, $\overline{RD}$ time	35	—	ns	
D0 to D7	t_{DS8}	Data setup time	10	—	ns	—
	t_{DH8}	Data hold time	20	—	ns	
	t_{ACC8}	Read access time	—	200	ns	C_L=10 to 100pF
	t_{OH8}	Output disable time	5	60	ns	

*1 t_{CYC} is specified by t_{CCHW} + t_{CCLW} + t_r + t_f.
*2 All timings must be specified using 30% and 70% of V_{DD}-GND as the reference.
*3 t_{CCLW} and t_{CCLR} are specified by the duration during which $\overline{CS}$ as well as $\overline{WR}$ and $\overline{RD}$ are LOW.
*4 A0 timing is specified by the duration during which $\overline{CS}$ as well as $\overline{WR}$ and $\overline{RD}$ are LOW.
*5 Rise and fall time of input signal (t_r, t_f) must be 15 ns maximum.

* Read/write characteristics II (68 series MPU)



* 1 is when access is made with E when $\overline{CS}$ is LOW.
* 2 is when access is made with $\overline{CS}$ when E is LOW.

Ta =–40 to +85°C, V_{DD}=2.6 to 3.6V, V_{DDI}=2.6 to V_{DD}

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
A0, R/$\overline{W}$	t_{AH6}	Address hold time	10	—	ns	—
	t_{AW6}	Address setup time	0	—	ns	
E, $\overline{CS}$	t_{CYC}	Write cycle	190	—	ns	—
	t_{CYC2}	Read cycle	250	—	ns	
	t_{CCLW}	Control pulse LOW width (write)	140	—	ns	
	t_{CCLR}	Control pulse LOW width (read)	70	—	ns	
	t_{CCHW}	Control pulse HIGH width (write)	40	—	ns	
	t_{CCHR}	Control pulse HIGH width (read)	170	—	ns	
	t_{CW6}	$\overline{CS}$–E time	40	—	ns	
D0 to D7	t_{DS6}	Data setup time	10	—	ns	—
	t_{DH6}	Data hold time	20	—	ns	
	t_{ACC6}	Read access time	—	170	ns	C_L=10 to 100pF
	t_{OH6}	Output disable time	5	60	ns	

* Rise and fall time of input signal (tr, tf) must be 15 ns maximum.
* All timings must be specified using 30% and 70% of V_{DD}–V_{SS} as the reference.
* t_{CCHW} and t_{CCHR} are specified by the duration during which $\overline{CS}$ is LOW and E is HIGH.
* A0 and R/$\overline{W}$ timings are specified by the duration during which $\overline{CS}$ is LOW and E is HIGH.

Ta =–40 to +85°C, V_{DD}=2.6 to 3.6V, V_{DDI}=1.7 to 2.6V

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
A0, R/$\overline{W}$	t_{AH6}	Address hold time	10	—	ns	—
	t_{AW6}	Address setup time	0	—	ns	
E, $\overline{CS}$	t_{CYC}	Write cycle	190	—	ns	—
	t_{CYC2}	Read cycle	280	—	ns	
	t_{CCLW}	Control pulse LOW width (write)	140	—	ns	
	t_{CCLR}	Control pulse LOW width (read)	70	—	ns	
	t_{CCHW}	Control pulse HIGH width (write)	40	—	ns	
	t_{CCHR}	Control pulse HIGH width (read)	200	—	ns	
	t_{CW6}	$\overline{CS}$–E time	40	—	ns	
D0 to D7	t_{DS6}	Data setup time	10	—	ns	—
	t_{DH6}	Data hold time	20	—	ns	
	t_{ACC6}	Read access time	—	200	ns	C_L=10 to 100pF
	t_{OH6}	Output disable time	5	60	ns	

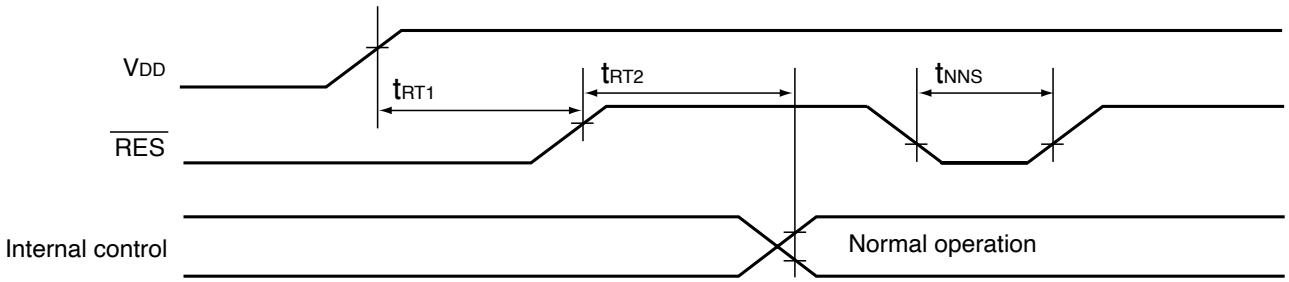
* Rise and fall time of input signal (t_r, t_f) must be 15 ns maximum.
* All timings must be specified using 30% and 70% of V_{DD}–V_{SS} as the reference.
* t_{CCHW} and t_{CCHR} are specified by the duration during which $\overline{CS}$ is LOW and E is HIGH.
* A0 and R/$\overline{W}$ timings are specified by the duration during which $\overline{CS}$ is LOW and E is HIGH.

Ta =–40 to +70°C, V_{DD}=V_{DDI}=2.9V±3%

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
A0, R/$\overline{W}$	t_{AH6}	Address hold time	10	—	ns	—
	t_{AW6}	Address setup time	0	—	ns	
E, $\overline{CS}$	t_{CYC}	Write cycle	150	—	ns	*1
	t_{CYC2}	Read cycle	280	—	ns	
	t_{CCLW}	Control pulse LOW width (write)	110	—	ns	
	t_{CCLR}	Control pulse LOW width (read)	70	—	ns	
	t_{CCHW}	Control pulse HIGH width (write)	35	—	ns	
	t_{CCHR}	Control pulse HIGH width (read)	200	—	ns	
	t_{CW6}	$\overline{CS}$–E time	35	—	ns	
D0 to D7	t_{DS6}	Data setup time	10	—	ns	—
	t_{DH6}	Data hold time	20	—	ns	
	t_{ACC6}	Read access time	—	200	ns	C_L=10 to 100pF
	t_{OH6}	Output disable time	5	60	ns	

*1 t_{CYC} is specified by t_{CCHW} + t_{CCLW} + t_r + t_f.
*2 All timings must be specified using 30% and 70% of V_{DD}–V_{SS} as the reference.
*3 t_{CCHW} and t_{CCHR} are specified by the duration during which $\overline{CS}$ is LOW and E is HIGH.
*4 A0 and R/$\overline{W}$ timings are specified by the duration during which $\overline{CS}$ is LOW and E is HIGH.
*5 Rise and fall time of input signal (t_r, t_f) must be 15 ns maximum.

* Reset timing

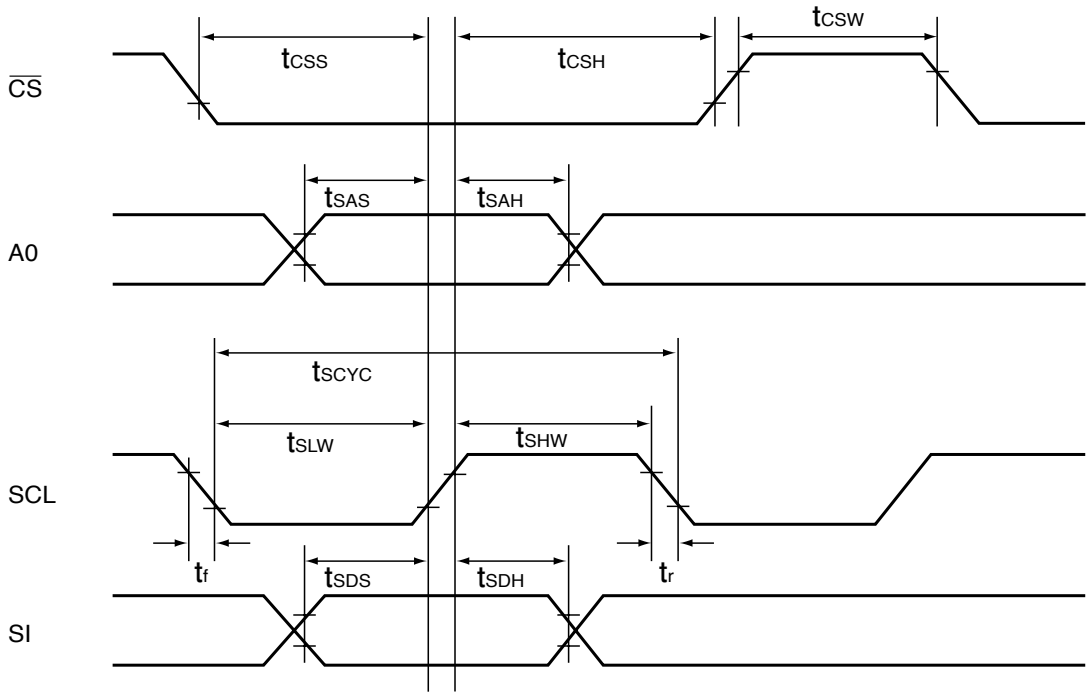


Ta =–40 to +85°C, VDD=2.6 to 3.6V, VDDI=1.7 to VDD

Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
$\overline{RES}$	tRT1	Reset cancel (when the power is turned on.)	350	—	ns	*1
	tRT2	Reset cancel (during normal operation)	350	—	ns	
	tNNS	Non-Sensitive noize *3	—	100	ns	

*1 Rise and fall time of input signal (tr, tf) must be 15ns maximum.
*2 All timings must be specified using 20% and 80% of VDD–VSS as the reference.
*3 Non-Sensitive noise width means that S1D15G10 can usually maintain a state of normal operation, even if the 100ns LOW level noise at maximum mixes into a $\overline{RES}$ terminal.

* Serial input characteristics



Ta =–40 to +85°C, V_{DD}=2.6 to 3.6V, V_{DDI}=1.7 to V_{DD}

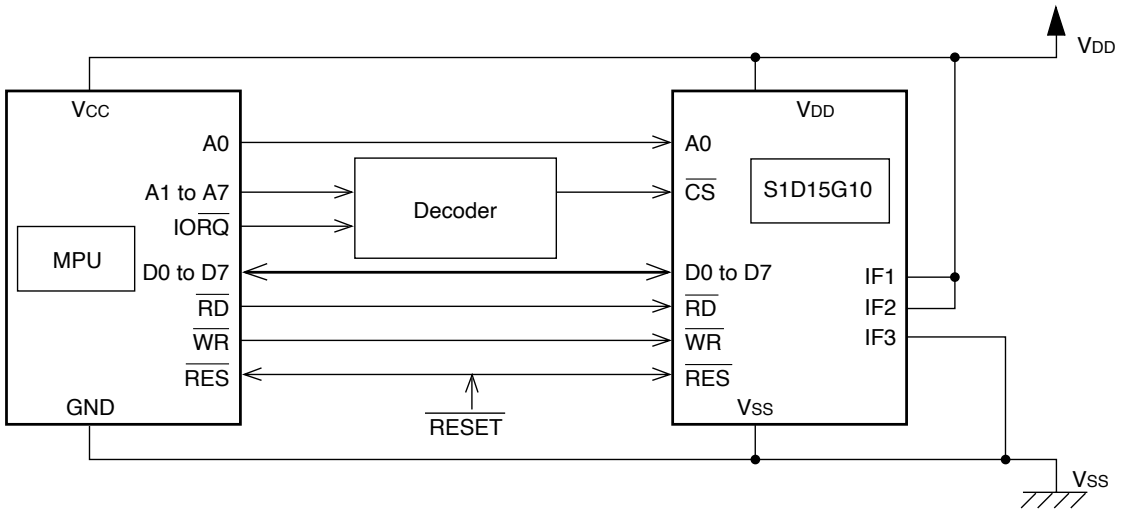
Signal	Symbol	Parameter	Min.	Max.	Unit	Measuring conditions and others
$\overline{CS}$	t_{CSS}	$\overline{CS}$ setup time	10	—	ns	*1, *2
	t_{CSH}	$\overline{CS}$ hold time	30	—	ns	
	t_{CSW}	$\overline{CS}$ HIGH width	110	—	ns	
A0	t_{SAS}	Address setup time	90	—	ns	
*3	t_{SAH}	Address hold time	20	—	ns	
SCL	t_{SCYC}	Clock cycle	50	—	ns	
	t_{SLW}	LOW width	15	—	ns	
	t_{SHW}	HIGH width	15	—	ns	
SI	t_{SDS}	Data setup time	10	—	ns	
	t_{SDH}	Data hold time	10	—	ns	

* 1: Rise and fall time of every input signal (t_r, t_f) must be 15 ns maximum.
* 2: All timings must be specified using 30% and 70% of V_{DDI} as the reference.
* 3: t_{SAS} and t_{SAH} are applicable to the 8-bit serial interface alone.

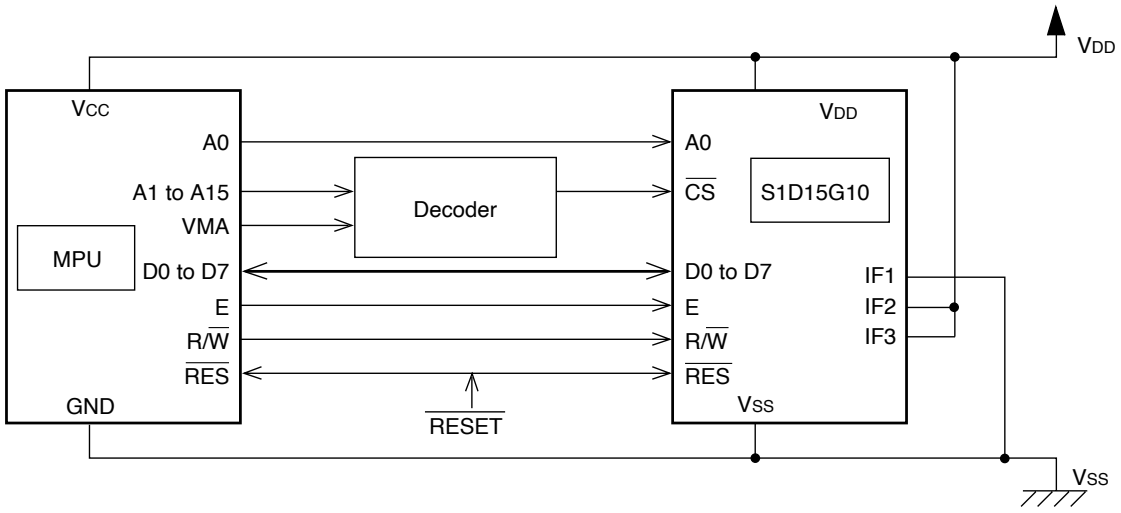
12. MPU INTERFACES (EXAMPLES FOR YOUR REFERENCE)

S1D15G10 series can be directly connected to 80 series and 68 series MPU. Using a serial interface allows you to operate S1D15G10 series with fewer signal lines. In addition to interfaces (1) to (3) given below, using IF1 to IF3 pins enables to employ the 16-bit interface and 9-bit serial interface.
When initialization with $\overline{RES}$ is complete, make sure that input pins of S1D15G00 series are correctly controlled.

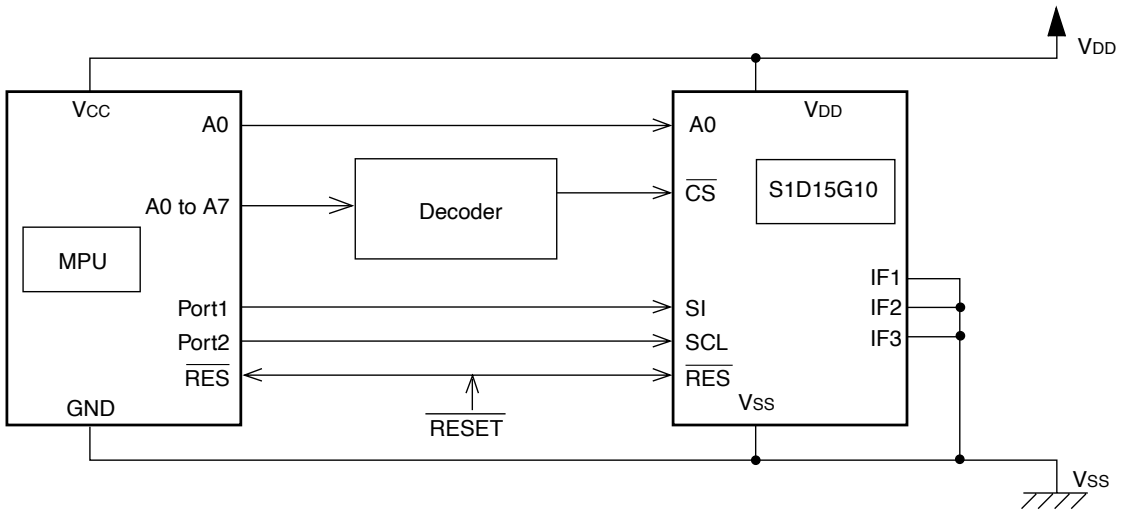
(1) 80 series MPU – 8-bit interface



(2) 68 series MPU – 8-bit interface



(3) 8-bit serial interface



12.1 Software Setup Examples

12.1.1 When Power is Turned On

Input power (V_{DDI}, V_{DD}).

↓

Be sure to apply POWER-ON RESET ($\overline{RES}$ = LOW)

↓

<Display Setting>	**<<State after resetting>>**
Display control (DISCTL)	
Setting clock dividing ratio and F1/F2 drive selection:	2 dividing, 8 h
Duty setting:	1/4
Setting reverse rotation number of line:	11h reverse rotations
Common scan direction (COMSCN)	
Setting scan direction:	COM1 -> COM68, COM69 -> COM132
Temperature Gradient Setting (TMPGRD)	

↓

Oscillation ON (OSCON)	Oscillation OFF

↓

Sleep-out (SLIPOUT)	Sleep-in

↓

<Power Supply Setting>	**<<State after resetting>>**
Electronic volume control (VOLCTR)	
Setting volume value α :	0
Setting built-in resistance value :	0 (3.95)
Power control (PWRCTR)	
Setting operation of power supply circuit:	All OFF

↓

<Display Setting 2>	**<<State after resetting>>**
Normal rotation of display (DISNOR)/Inversion of display (DISINV):	Normal rotation of display
Partial-in (PTLIN)/Partial-out (PTLOUT)	Partial-out
Setting fix area:	0
Area scroll set (ASSET)	
Setting area scroll region:	0
Setting area scroll type:	Full-screen scroll
Scroll start set (SCSTART)	
Setting scroll start address:	0

↓

<Display Setting 3>	**<<State after resetting>>**
Data control (DATCTL)	
Setting normal rotation/inversion of page address:	Normal rotation
Setting normal rotation/inversion of column address:	Normal rotation
Setting direction of address scanner:	Column direction
Setting RGB arrangement:	RGB
Setting gradation:	8 gradations
256-color position set (RGBSET8)	
Setting color position at 256-color	All 0

↓

<RAM Setting> **<<State after resetting>>**

Page address set (PASET)
Setting start page address: 0
Setting end page address: 0
Column address set (CASET)
Setting start column address: 0
Setting end column address: 0

↓

<RAM Write> **<<State after resetting>>**

Memory write command (RAMWR)
Writing displayed data : Repeat as many as the number needed and exit by entering other command.

↓

<Waiting (approximately 100ms)>

Wait until the power supply voltage has stabilized.
Enter the power supply control command first, then wait at least 100ms before entering the display ON command when the built-in power supply circuit operates.
If you do not wait, an unwanted display may appear on the liquid crystal panel.

↓

Display ON (DISON): Display OFF

*1: When the IC is in Sleep In state, the liquid crystal drive power supply and the boosting power output and GND pin are jumpered, therefore, the Sleep Out command must be entered to cancel the Sleep state prior to turning on the built-in circuit.

(Note) If changes are unnecessary after resetting, command input is unnecessary.

12.2.2 Command Input Procedure During Power Off

•When power-on reset is not used

<< IC status>>

Display off (DISOFF): display is turned off, and all of the common and segment pins become VC potential.

↓

Liquid crystal drive power supply circuit off (PWRCTR): built-in power supply circuit stops.

↓

Oscillation off (OSCOFF): built-in oscillation circuit stops and all the circuits inside the IC also stop.

↓

Sleep In (SLPIN) *2

↓

Stop the power supply (VDDI, VDD).

*2: In order to discharge the capacitor connected to the liquid crystal drive power supply circuit, execute the Sleep In command to put the IC in Sleep state prior to stopping the power supply. Stop VDDI and VDD when the output of the liquid crystal drive power supply circuit has dropped sufficiently.

•When power-on reset is used

Turn on the power-on reset ($\overline{RES}$ = LOW) *3

↓

Stop the power supply (VDDI, VDD).

*3: Stop VDDI and VDD when the output of the liquid crystal drive power supply circuit has dropped sufficiently.

(Note:1)
This IC is the logic circuit of the VDD-GND and VDDI-GND power supplies, and it controls the liquid crystal output driver. If the VDDI-GND and VDD-GND power supplies are stopped with residual voltage in the liquid crystal drive power supply circuit, the liquid crystal output driver (COM, SEG) may output uncontrolled voltage. Stop VDDI and VDD when the output of the liquid crystal drive power supply circuit has dropped sufficiently.
(Note:2)
Avoid writing in the display RAM during sleep-in since it may cause too much current to be generated.

12.2.3 Sleep state

This IC goes into Sleep state when the Sleep In command and several other commands are executed. When in the Sleep state, IC power consumption will be kept to a minimum. Also, internal status including the display RAM will be maintained, the Sleep Out and several commands will resume the display state.

•Setting the Sleep state

<< IC status>>

① **Display off (DISOFF):** display is turned off, and all the common segment and pins become VC potential.

↓

② **Liquid crystal drive power supply circuit off (PWRCTR):** built-in power supply circuit stops.

↓

③ **Oscillation off (OSCOFF):** built-in oscillation circuit stops and all the circuits inside the IC also stop.

↓

Sleep In (SLPIN): commands other than ① to ③ and display RAM content are maintained. Commands can be entered.
(Note) Avoid writing in the display RAM during sleep-in since it may cause too much current to be generated.

•Releasing the Sleep state

<<IC status>>

Sleep Out (SLPOUT)

↓

Oscillation on (OSCON): built-in power supply circuit operates and liquid crystal drive potential is supplied.

↓

Wait (approx. 100ms): wait until liquid crystal drive power supply boots and stabilizes. Wait until the power supply voltage stabilizes.

↓

Display on (DISON): display comes on and the display RAM content is output.

12.2.4 Refresh Sequence

Refreshing of the state setup is recommended by reentering the command, parameters and the display data in order to recover from improper IC operations due to such reasons as noise.
Reconfigure the following commands and parameters.

Common scan direction (COMSCN)
Temperature gradient (TMPGRD)
Oscillation on (OSCON)
Sleep Out (SLPOUT)
Electronic volume control (VOLCTR)
Power supply control (PWRCTR)
Normal (DISNOR)/Inverted display (DISINV)
Partial in (PTLIN)/Partial out (PTLOUT)
Area scroll set (ASCSET)
Scroll start set (SCSTART)
Data control (DATCTL)
256-color position set (RGBSET8)
NOP instruction (NOP) *1
Page address set (PASET)
Column address set (CASET)
Memory write command (RAMWR): display data write
Display on (DISON)

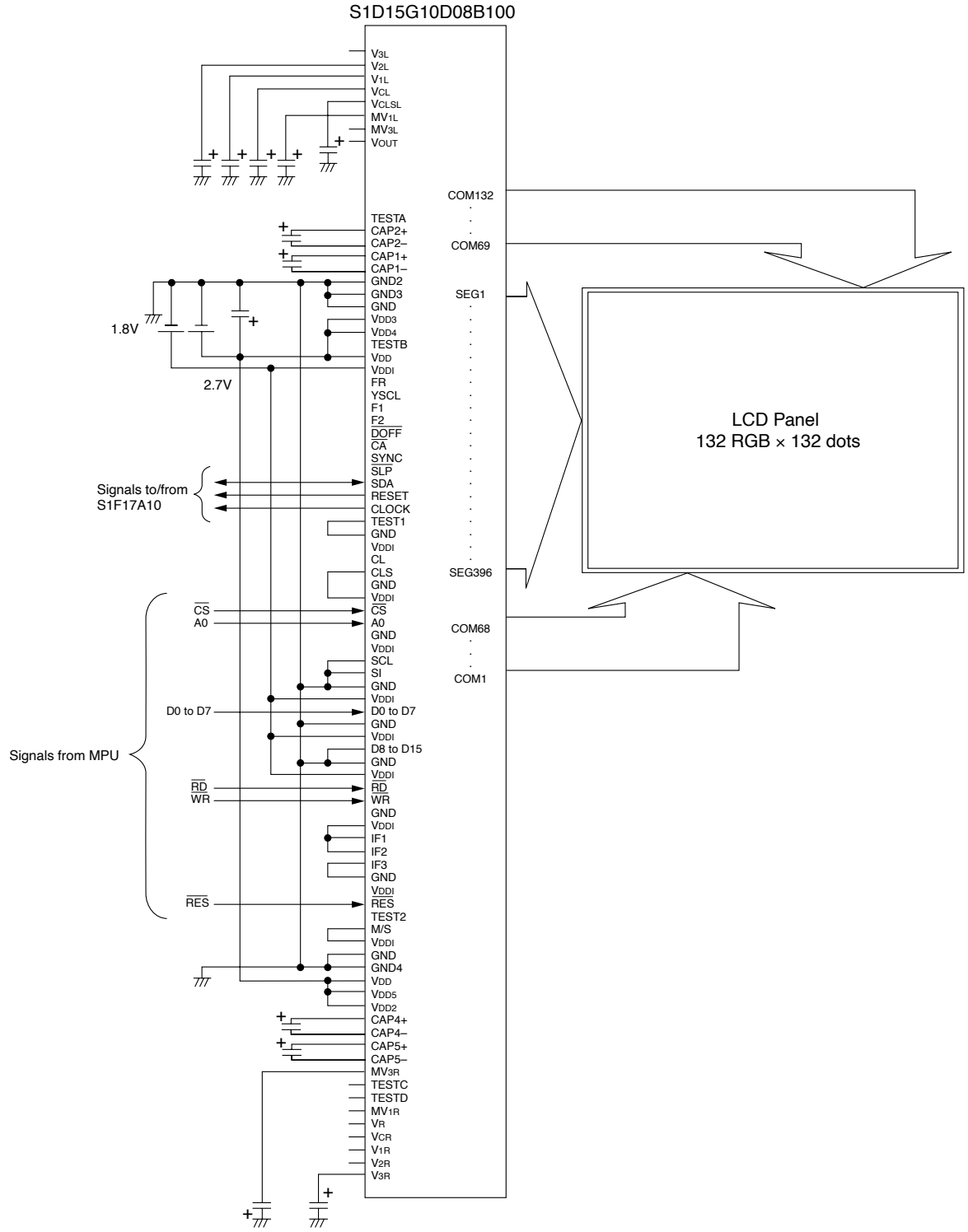
*1: IC shipment inspection test state can be escaped with NOP instruction. Add this to the refresh sequence.

If display control (DISCTL) is reconfigured during display, noise may occur on the display, so omit this from the refresh sequence. Reconfigure with the display off.

13. PERIPHERAL CONNECTION EXAMPLES

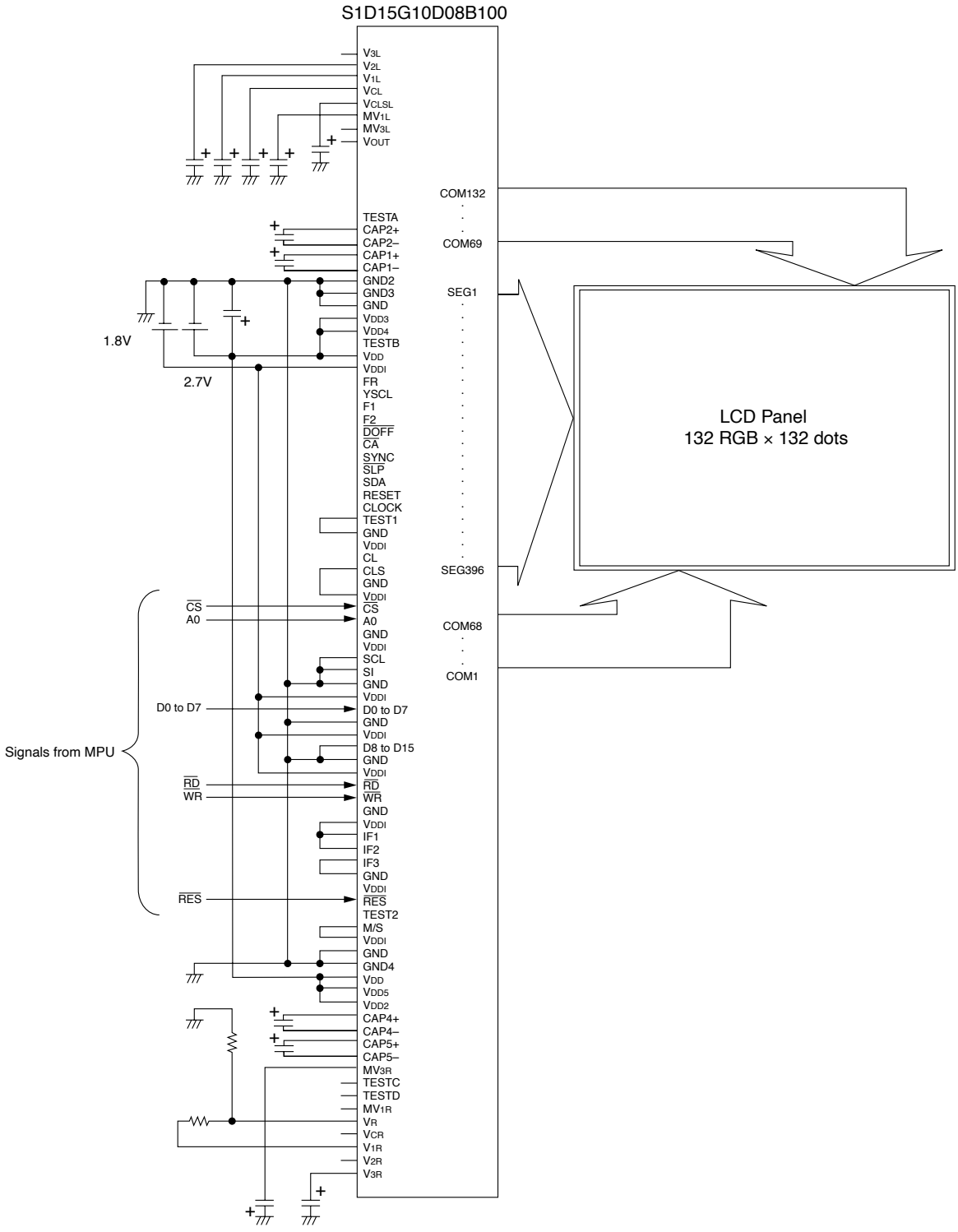
13.1 When EEPROM is used

Power voltages: V_{DDI}=1.8 V, V_{DD}=2.7 V
Interface: 8-bit parallel interface
Primary boosting: Triple
Clock: The built-in oscillator circuit is used.
V_1 voltages: Set by the peripheral EEPROM . PWRCTR: P14= “0”
Capacitors: A bypass capacitor is used between V_{DD} and GND pins. A voltage regulator capacitor is used between GND and each of V_2, V_1, V_C and MV_1 pins.
Connect them by observing the current consumption and voltage waveforms.



13.2 When peripheral split resistor is used

Power voltages: V_{DDI}=1.8 V, V_{DD}=2.7 V
Interface: 8-bit parallel interface
Primary boosting: Triple
Clock: The built-in oscillator circuit is used.
V_1 voltages: Set by external split resistors. PWRCTR: P14= "1"
Capacitors: A bypass capacitor is used between V_{DD} and GND pins. A voltage regulator capacitor is used between GND and each of V_2, V_1, V_C and MV_1 pins.
Connect them by observing the current consumption and voltage waveforms.



14. EEPROM INTERFACE

The S1D15G10D00B chips provide the Write and Read functions to write the Electronic Control value and built-in resistance ratio into and read them from the peripheral EEPROM (S1F17A10). Using the Write and Read functions, you can store these values appropriate to each LCP panel.

14.1 Conditions when EEPROM read/write is performed

① The built-in oscillator circuit is already operating.
② The CL division by 2 and 132 display lines have been set by the Display Control command.

14.2 EEPROM writing instructions

1. Issue the VOLCTR command to set the appropriate Electronic Control value and built-in resistance ratio.
2. Issue the EPCTIN command to select the Control EEPROM mode (for data writing).
3. Issue the EPMWR command to write data into the EEPROM.
4. Issue the EPCTOUT command to cancel the EEPROM Control mode.

14.3 EEPROM data reading instructions

1. Issue the EPCTIN command to select the EEPROM Control mode (for data reading).
2. Issue the EPMRD command to read data from the EEPROM.
3. Issue the EPCTOUT command to cancel the EEPROM Control mode and updates the Electronic Control value and built-in resistance ratio using the read data.

Miscellaneous:
The MPU can read the Electronic Control value and built-in resistance ratio by issuing a combination of EPSRRD1 or EPSRRD2 and STREAD (Status Read) commands.

Notes: As the EPCTIN, EPCWR and EPCRD commands require the following processing times, use a software timer or insert a process to loop the operation by monitoring the status read value of D2 (Access to EEPROM). If these times are insufficient, the Read or Write operation may fail.

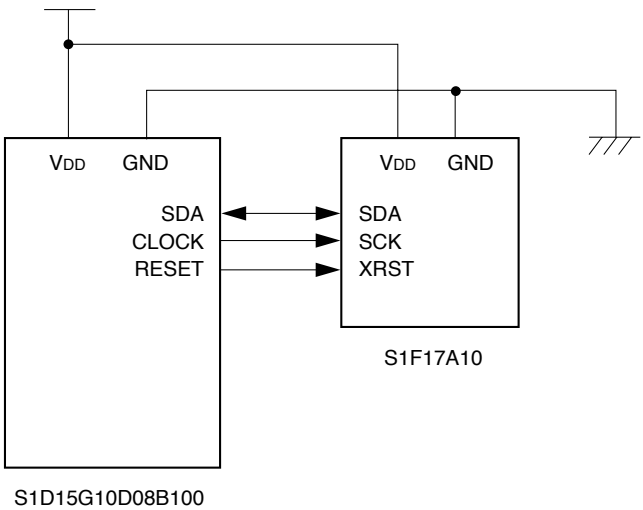
① EPCTIN $\frac{5}{fosc/4}(\text{sec})$

② EPCWR $\frac{10}{fosc/320}(\text{sec})$

③ EPCRD $\frac{10}{fosc/4}(\text{sec})$

14.4 Connection example

S1D15G10 and S1F17A10 connection example.
VDD for both chips is connected to the same potential.



15. CAUTIONS

Concerning this development specification, users are advised to pay attention to the following precautions.

1. This development specification is subject to modifications without previous notice.
2. This development specification does not grant the industrial property right or any other right, or exercising such rights.

Application examples contained in this document are intended only to help users to understand the product better. SEIKO EPSON shall not be liable to any circuit-related problem resulted from using these examples.

Users are requested to pay attention to the following points when using S1D15G10 series.

Precautions on Light

Characteristics of semiconductor devices can be changed when exposed to light as described in the operational principles of solar batteries. Exposing this IC to light, therefore, can potentially lead to its malfunctioning.

① Care must be exercised in designing the operation system and mounting the IC so that it may not be exposed light during operation

② Care must be exercised in designing the inspection process and handling the IC so that it may not be exposed to light during the process.

③ The IC must be shielded from light in the front, back and side faces.

Precautions on External Noises

① Internal state of S1D15G10 can be changed when exposed to adversely affecting external factors such as excessive noises though it can maintain the command-instructed operational status and display data. Thus, you must make sure when mounting the IC and designing the operation system that measures for eliminating noises or measures protecting the IC from noises are prepared.

② In order to be prepared against sudden noise, it is recommended to prepare the software to perform periodic refreshing of operational state (re-setting of commands and re-transfer of display data).

Precautions on Mounting COG

When mounting COG, you must take into consideration of resistance component generated across the driver chip and externally connected parts (capacitor and resistor) resulting from ITO wiring. This resistance component can interfere with high-speed operation of liquid crystal display or MPU.

When mounting COG, you must take into consideration of the following three points in the module design:

1. To minimize resistance between the driver chip pin to the external part.
2. To minimize resistance at the power terminal of the driver chip.
3. To develop sample COG modules with varying degrees of ITO sheet resistance in order to select one with the sheet resistance allowing sufficient operational margins.