HIGH-VOLTAGE MIXED-SIGNAL IC

UC1701

65x132 STN Controller-Driver

MP Specifications
Datasheet Revision: 1.0

IC Version: c_B
September 29, 2014

ULTRACHIP

The Coolest LCD Driver, Ever!

Table of Content

UC1701

Single-Chip, Ultra-Low Power
65COM by 132SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1701c is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver supports 65x132 graphics STN LCD panels.
- Support both row ordered and column ordered display buffer RAM access.
- Support industry standard 8-bit parallel bus (8080 or 6800 mode), 4-wire serial bus (S8), and 2-wire I^2C serial interfaces.
- Ultra-low power consumption under all display patterns.
- Selectable Mux Rate and Bias Ratio allow flexible power management options.
- Internal charge pump with on-chip pumping capacitor requires only 1 external capacitor to operate.
- Very low pin count (7~9-pin) allows exceptional image quality in COG format on conventional ITO glass.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} range (Typ.): 2.7V ~ 3.3V
  $V_{DD2/3}$ range(Typ.): 2.7V ~ 3.3V
  LCD V_{OP} range: 3.85V ~ 10.0V
- Available in gold bump dies
- COM/SEG bump information
  Bump pitch: 27 μM
  Bump gap: 12 μM ± 3 μM
  Bump surface: 1500 μM^2

ORDERING INFORMATION

Part Number	I^2C	Description
UC1701cGAB	Yes	Gold Bumped Die, Bump Height: 10uM
UC1701cGBB	Yes	Gold Bumped Die, Bump Height: 15uM

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of wafer sawing. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

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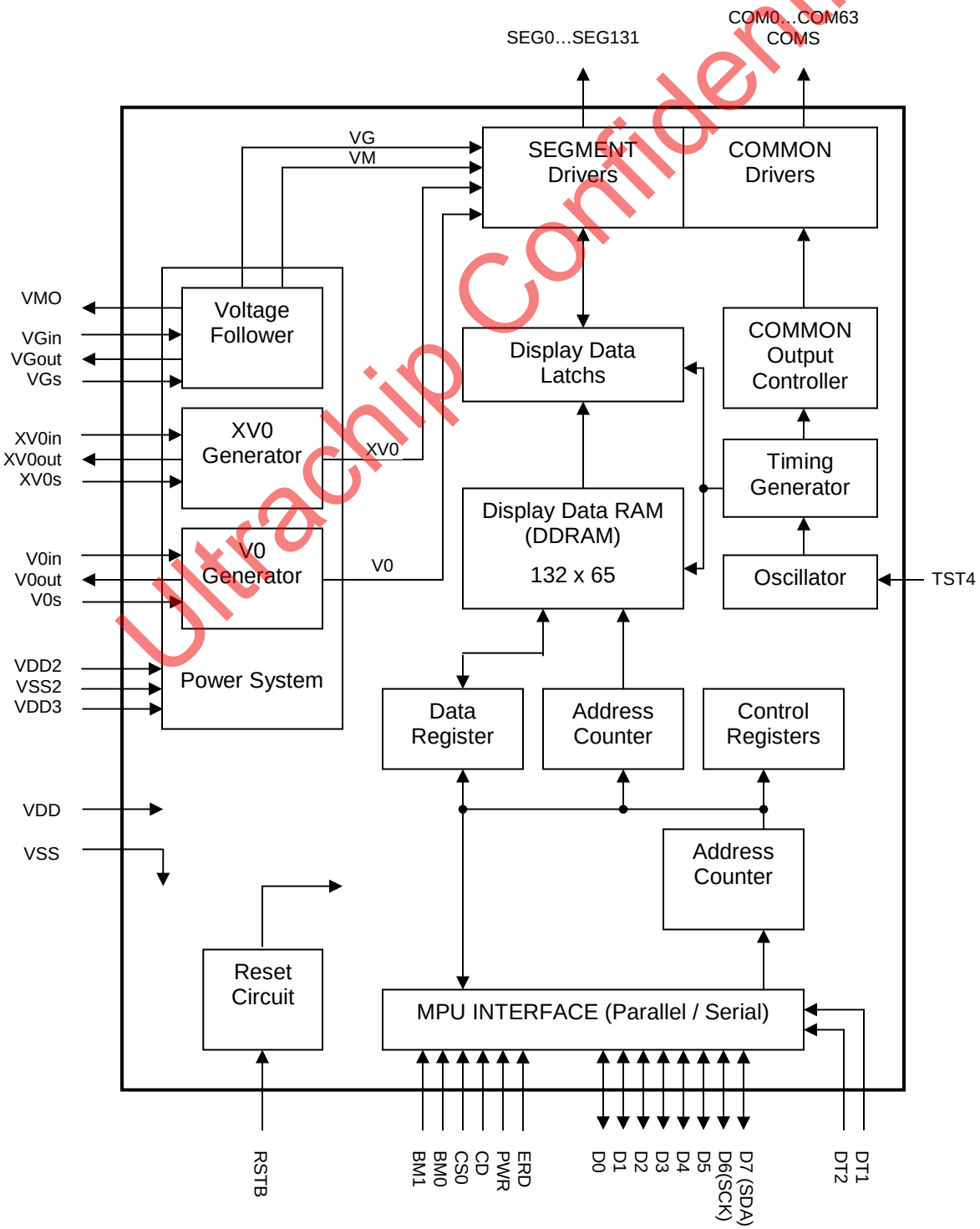
BLOCK DIAGRAM

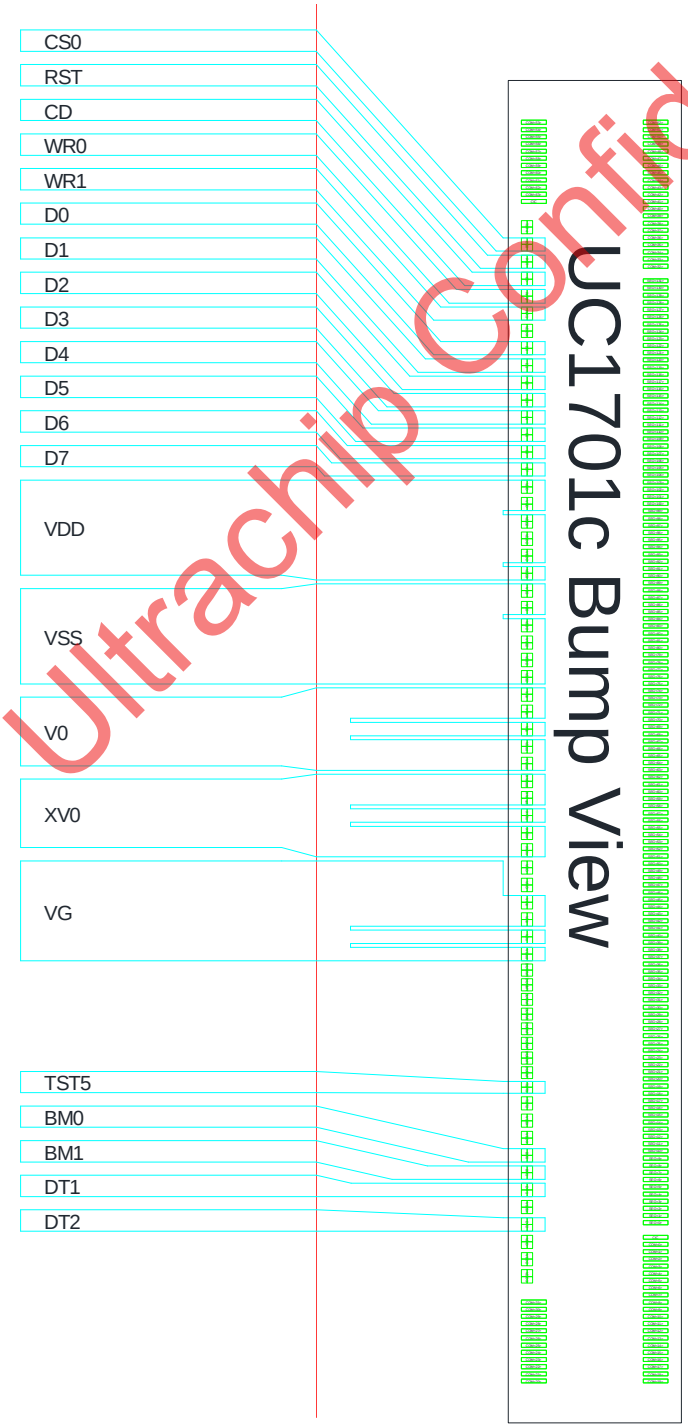


PIN DESCRIPTION

Pin (Pad) Name	Type	Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	3 4 2	V_{DD} supplies for Display Data RAM and digital logic, V_{DD2} supplies for analog circuit, V_{DD3} supplies for reference voltage circuits. V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}. ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	2 4	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V0in V0out V0s	PWR	2 2 1	V0 is the LCD driving voltage for COM circuit at negative frame. V0in is the V0 input of common circuits. V0out is the output of V0 regulator. V0s is the feedback of V0 regulator. Be sure that V0 ≥ VG > VM > V_{SS} ≥ XV0, under operation. These pins should be separated in ITO layout; while they should be connected together in FPC layout.
VGin VGout VGs	PWR	2 1 1	VG is the LCD driving voltage for segment circuit. VGout is the output of VG regulator. VGs is the feedback of VG regulator. VGin is the VG input of segment circuits. 1.6V ≤ VG < V_{DD2}. These pins should be separated in ITO layout; while they should be connected together in FPC layout.
XV0in XV0out XV0s	PWR	2 2 1	XV0 is the LCD driving voltage for common circuit at positive frame. XV0out is the output of XV0 regulator. XV0s is the feedback of XV0 regulator. XV0in is the XV0 input of common circuits. These pins should be separated in ITO layout; while they should be connected together in FPC layout.
VMO	PWR	2	VM is the LCD driving voltage for common circuits. 0.8V ≤ VM < V_{DD2}.
NOTE • Recommended capacitor values: C_{V0}: Optional. 0.1uF/16V. Connect the capacitor of C_{V0} value between XV0 and V0.			
HOST INTERFACE			
BM0 BM1 TST5	I	1 1 1	Bus mode: The interface bus mode is determined by BM[1:0] and TST5 by the following relationship: BM[1:0] / TST5 / Mode 11 / Open / 6800/8-bit 10 / Open / 8080/8-bit 0x / Open / 4-wire SPI w/ 8-bit token (S8: conventional) 0x / 1 / 2-wire serial (I^2C) Always connect unused pins to either Vss or V_{DD}.
CS0	I	1	Chip Select. Chip is selected when CS0 = "L". When the chip is not selected, D[7:0] will be of high impedance.
RST	I	1	It's necessary to set pin-reset in 3 mS after $V_{DD2/3}$ stable. When RST="L", all control registers are re-initialized by their default states. An RC Filter has been included on-chip. There is no need for external RC noise filter.

<table>
<tr><th>Pin (Pad) Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td>CD</td><td>I</td><td>1</td><td>Select Control data or Display data for read/write operation.
”L”: Control data ”H”: Display data</td></tr>
<tr><td>WR0 / A3
WR1 / A2</td><td>I</td><td>1
1</td><td>WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details.
In parallel mode, the meaning of WR[1:0] depends on which interface it is in, 6800 or 8080 mode. In serial interface modes, these two pins are not used. Connect them to V_{SS} or V_{DD}.
In I^2C mode, these two pins specifies bits 3~2 of device address (A[3:2]).</td></tr>
<tr><td>DT1
DT2</td><td>I</td><td>1
1</td><td>Duty selection.
<table>
<tr><th>DT2</th><th>DT1</th><th>Duty</th></tr>
<tr><td>0</td><td>0</td><td>1/65</td></tr>
<tr><td>0</td><td>1</td><td>1/49</td></tr>
<tr><td>1</td><td>0</td><td>1/33</td></tr>
<tr><td>1</td><td>1</td><td>1/55</td></tr>
</table></td></tr>
<tr><td>D7~D0</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[7] to SDA, D[6] to SCK.
<table>
<tr><th></th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>Parallel (8-bit)</td><td>DB7</td><td>DB6</td><td>DB5</td><td>DB4</td><td>DB3</td><td>DB2</td><td>DB1</td><td>DB0</td></tr>
<tr><td>Serial (S8, I^2C)</td><td>SDA</td><td>SCK</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
<tr><td colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</td></tr>
<tr><td>SEG0 ~
SEG131</td><td>HV</td><td>132</td><td>SEG (column) driver outputs. Support up to 132 pixels.
Leave unused SEG drivers open-circuit.</td></tr>
<tr><td>COM0 ~
COM63</td><td>HV</td><td>64</td><td>COM (row) driver outputs. Support up to 64 rows.
Leave unused COM drivers open-circuit.</td></tr>
<tr><td>CIC</td><td>HV</td><td>2</td><td>Icon driver outputs. Leave it open if not used.</td></tr>
<tr><td colspan="4">MISC. PINS</td></tr>
<tr><td>V_{DDX}</td><td></td><td>2</td><td>Auxiliary V_{DD}. This pin is connected to the main V_{DD} bus within the IC. It’s provided to facilitate chip configurations in COG application.
There’s no need to connect V_{DDX} to main V_{DD} externally and it should <u>NOT</u> be used to provide V_{DD} power to the chip.</td></tr>
<tr><td>V_{SSX}</td><td></td><td>2</td><td>Auxiliary V_{ss}. These pins are connected to the main Vss bus within the IC, to facilitate chip configurations in COG application.
There’s no need to connect VssX to main Vss externally and they should <u>NOT</u> be used to provide Vss power to the chip.</td></tr>
<tr><td>TST4</td><td>I</td><td>1</td><td>Test control. There’s an on-chip pull-up resistor for TST4. Leave it open during normal use.</td></tr>
<tr><td>TST2</td><td>I/O</td><td>1</td><td>Test I/O pins. Leave these pins open during normal use.</td></tr>
<tr><td>Dummy</td><td></td><td>8</td><td>Dummy pins are NOT connected inside the IC.</td></tr>
</table>

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The operation condition, V_{DD}=2.7V (typical), should be satisfied under all operating conditions. UC1701c's peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1701c's on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 2.6V and cause the IC to malfunction.

CONTROL REGISTERS

UC1701c contains registers, which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, Command Table and Command Description.

Name: The Symbolic reference of the register. Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after hardware reset.

Name	Bits	Default	Description
SL	6	00H	Scroll Line. Scroll the displayed image up by *SL* rows. The valid SL value is between 0 (for no scrolling) and 63. Setting SL outside of this range causes undefined effects on the displayed image. This register does not affect icon output CIC.
CA	8	00H	Column Address of DDRAM (Display Data RAM). Value range is 0~131. (Used in Host to access DDRAM)
PA	4	0H	Page Address of DDRAM. Value range 0~8. (Used in Host to access DDRAM)
BR	1	0H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS} varies according to Duty selected: **BR=0** / BR=1 Duty=1/65: 1/9 / 1/7 Duty=1/49: 1/8 / 1/6 Duty=1/33: 1/6 / 1/5 Duty=1/55: 1/8 / 1/6
PM	6	20H	Adjust contrast of LCD panel display.
PC	6	20H	Power Control. PC [0]: VG pump control. (Default **0: Disable**) PC [1]: V0 pump control. (Default **0: Disable**) PC [2]: XV0 pump control. (Default **0: Disable**) PC [5:3]: Resistor Ratio for V_{LCD}. (Default **100b**) 000b~111b : Rb/Ra ratio setting
CR	8	0H	Return Column Address. Useful for cursor implementation.
AC3	1	0H	Address Control. AC3: CUM: Cursor update mode, (Default **0: OFF**) When CUM=1, CA increment on write only, wrap around suspended
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse (bit-wise data inversion. Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) When DC[2] is set to 0, the IC will enter Sleep Mode
LC	2	0H	LCD Control: LC[0]: MX, Mirror X SEG/Column sequence inversion (Default: **0: OFF**) LC[1]: MY, Mirror Y COM/Row sequence inversion (Default: **0: OFF**)
APC0 APC1	8 8	90H --	Advanced Program Control. APC0 [7] : TC, V_{BIAS} temperature compensation coefficient (%-per-^{o}C) 0b : TC curve definition = -0.05% / ^{o}C **1b : TC curve definition = -0.11% / ^{o}C** APC0 [6] is fixed. APC0 [5:4] : FR, Frame Rate: (Unit: Hz) Frame Rate / FR[1:0]: 00b / FR[1:0]: 01b / FR[1:0]: 10b / FR[1:0]: 11b Duty:1/65: 58 / **77** / 96 / 115 Duty:1/55: 102 / **136** / 170 / 203 Duty:1/49: 115 / **153** / 191 / 229 Duty:1/33: 57 / **76** / 94 / 113 APC0 [3:2] are fixed. APC0 [1:0] : WA, automatic column/row Wrap Around. WA[0] : **0: PA wrap around disable** 1: PA wrap around enable. WA[1] : **0: CA wrap around disable** 1: CA wrap around enable. APC1[7:0] : For UltraChip's use only. Do *NOT* use.

Name	Bits	Default	Description
			Status Registers
BZ, MX, DE, RST	1 1 1 1	0	BZ : Set to 1 when system is busy. Commands can only be accepted when BZ=0. MX : Mirror X-axle (i.e. SEG or column) DE : Set to 1 when display enabled. RST : Reset flag. RST=1 when reset is in progress.

COMMAND TABLE

The following is a list of host commands supported by UC1701c

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # Useful Data bits, – Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	BZ	MX	DE	RST	0	0	0	0	Get Status	--
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB			0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	000b
6.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
7.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
8.	Set V_{LCD} Resistor Ratio	0	0	0	0	1	0	0	#	#	#	Set PC[5:3]	100b
9.	Set Electronic Volume (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[5:0]	20H
				0	0	#	#	#	#	#	#		
10.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
11.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
12.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
13.	Set SEG Direction	0	0	1	0	1	0	0	0	0	#	Set LC[0]	0b
14.	Set COM Direction	0	0	1	1	0	0	#	-	-	-	Set LC[1]	0b
15.	System Reset	0	0	1	1	1	0	0	0	1	0	Software Reset	N/A
16.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
17.	Set LCD Bias Ratio	0	0	1	0	1	0	0	0	1	#	Set BR	0b
18.	Set Cursor Update Mode	0	0	1	1	1	0	0	0	0	0	AC3=1, CR=CA	N/A
19.	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC3=0, CA=CR.	N/A
20.	Set Static Indicator OFF	0	0	1	0	1	0	1	1	0	0	NOP	N/A
21.	Set Static Indicator ON	0	0	1	0	1	0	1	1	0	1	NOP	N/A
	Set Static Indicator			-	-	-	-	-	-	-	-		
22.	Set Booster Ratio (double-byte command)	0	0	1	1	1	1	1	0	0	0	NOP	0b
				0	0	0	0	0	0	0	#		
23.	Set Power Save (compound command)	0	0	#	#	#	#	#	#	#	#	Display OFF & All Pixel ON	N/A
24.	Set Test Control (double-byte command)	0	0	1	1	1	1	1	1	TT		For UCI only Do NOT use	N/A
				-	#	#	#	#	#	#	#		
25.	Set Adv. Program Control 0 (double-byte command)	0	0	1	1	1	1	1	0	1	0	Set TC, FR, WA	90H
				#	0	#	#	0	0	#	#		
26.	Set Adv. Program Control 1 (double-byte command)	0	0	1	1	1	1	1	0	1	1	For UCI only Set APC1	N/A
				#	#	#	#	#	#	#	#		

* Any bit patterns other than the commands listed above, may result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Write/Read Data Byte (Command 1,2) access Display Data RAM based on Page Address (PA) register and Column Address (CA) register. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	BZ	MX	DE	RST	**0**	**0**	**0**	**0**

BZ: BZ=1 when busy. The system accepts commands only when BZ=0.
MX: Mirror X. Status of register LC[0]
DE: Display Enable flag. DE=1 when display is enabled.
RST: RST flag. RST=1 when reset is in progress.

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB, CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB, CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: 0~131

5. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control, PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

Set PC[2:0] to enable the built-in charge pump.

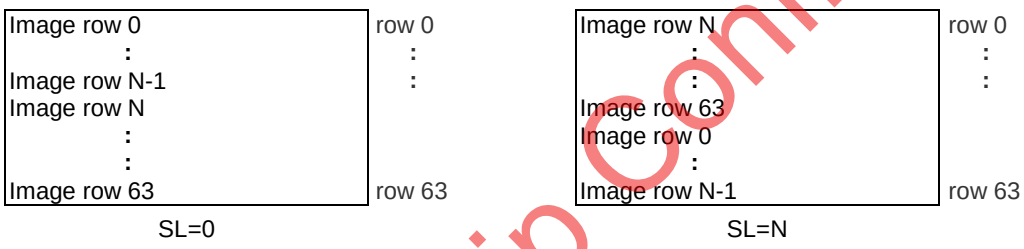
PC[2] : XV0 pump control. **0: Disable** (Default)
PC[1] : V0 pump control. **0: Disable** (Default)
PC[0] : VG pump control. **0: Disable** (Default)

6. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line, SL[5:0]	0	0	**0**	**1**	SL5	SL4	SL3	SL2	SL1	SL0

Set the scroll line number. Range : 0~63

Scroll line setting will scroll the displayed image up by *SL* rows. Icon output CIC will not be affected by `Set Scroll Line` command.



7. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address, PA[3:0]	0	0	**1**	**0**	**1**	**1**	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = 0~8.

8. Set V_{LCD} Resistor Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{LCD} Resistor Ratio, PC[5:3]	0	0	**0**	**0**	**1**	**0**	**0**	PC5	PC4	PC3

Configure PC[5:3] to set internal Resistor Ratio, Rb/Ra, for the V_{LCD} Voltage regulator to adjust the contrast of the display panel:

PC[5:3] : 000b~111b – 1+Rb/Ra ratio. **Default : 100b**. Refer to V_{LCD} Quick Reference for "1+Rb/Ra" ratio.

$V_{LCD}=((1+Rb/Ra) \times Vev) \times (1+(T-25)\times C_T\%)$ $\quad Vev=(1-(63-PM)/162)\times V_{REF}$

where Rb and Ra are internal resistors,
V_{REF} is on-chip contrast voltage, and
PM is a value of electronic volume

9. Set Electronic Volume

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Electronic Volume, PM[5:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
			0	**0**	PM5	PM4	PM3	PM2	PM1	PM0

Set PM[5:0] for electronic volume "PM" for VLCD voltage regulator to adjust contrast of LCD panel display

Effective range: 0~63. **Default: 32 (20h)**

10. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON, DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.
Default : 0

11. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display, DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

12. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable, DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1701c will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers.

13. Set SEG Direction

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Segment Direction, LC[0]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	LC0 / MX

Set LC[0] for SEG (column) mirror (MX). **Default : 0**

MX is implemented by reversing the mapping order between RAM and SEG (column) electrodes. The data stored in RAM is not affected by MX command. Yet, MX has immediate effect on the display image.

14. Set COM Direction

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Common Direction, LC[1]	0	0	**1**	**1**	**0**	**0**	LC1 / MY	**-**	**-**	**-**

Set LC[1] for COM (row) mirror (MY). **Default : 0b**

MY is implemented by reversing the mapping between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. Yet, MY has immediate effect on the display image.

15. System Reset (Software Reset)

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Software Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset.

Some control register values will be reset to their default values. Yet, data stored in RAM will not be affected. See the “Reset and Power Management” section for more details.

16. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

17. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio, BR	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**1**	BR

Select voltage bias ratio required for LCD. **Default : 0**

The setting of Bias ratio varies according to Duty:

DUTY	BR = 0	BR = 1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

18. Set Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Cursor Update Mode	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**

This command is used for set cursor update mode function. When cursor update mode sets, UC1701c will update register CR with the value of register CA. The column address CA will increment with write RAM data operation but the address wraps around will be suspended no matter what WA setting is. However, the column address will not increment in read RAM data operation. The set cursor update mode can be used to implement “write after read RAM” function. The column address (CA) will be restored to the value, which is before the set cursor update mode command, when reset cursor update mode.

The purpose of this pair commands and their feature is to support “write after read” function for cursor implementation.

19. Reset Cursor Update Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Reset Cursor Update Mode	0	0	**1**	**1**	**1**	**0**	**1**	**1**	**1**	**0**

Set AC3=0 and CA=CR.

20. Set Static Indicator OFF

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Turn OFF Static Indicator	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**0**

No Operation.

21. Set Static Indicator ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Turn ON Static Indicator	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**0**	**1**
	0	0	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**

No Operation.

22. Set Booster Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Booster Ratio (Double-byte command)	0	1	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**0**
			0	**0**	**0**	**0**	**0**	**0**	**0**	**-**

This command is used for “No Operation”.

23. Set Power Save

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Power Save (Compound Command)	0	0	#	#	#	#	#	#	#	#

24. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double-byte command)	0	1	**1**	**1**	**1**	**1**	**1**	**1**	TT	
			-	#	#	#	#	#	#	#

This command is for UltraChip’s Test only. Do NOT use.

25. Set Advanced Program Control 0

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control, APC0 [7:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**0**
			TC, APC0 [7]	**0**	FR1, APC0 [5]	FR0, APC0 [4]	**0**	**0**	WA1, APC0 [1]	WA0, APC0 [0]

TC : APC0 [7], V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:
TC : 0b = -0.05%/^{o}C, **1b = -0.11%/^{o}C**

APC0 [6] is fixed.
APC0 [5:4] : FR, Frame Rate: (Unit: Hz)

FR[1:0] :	Duty:1/65	00b: 58	**01b: 77**	10b: 96	11b: 115
FR[1:0] :	Duty:1/55	00b: 102	**01b: 136**	10b: 170	11b: 203
FR[1:0] :	Duty:1/49	00b: 115	**01b: 153**	10b: 191	11b: 229
FR[1:0] :	Duty:1/33	00b: 57	**01b: 76**	10b: 94	11b: 113

APC0 [3:2] are fixed.

WA : APC0 [1:0], Automatic column/row wrap around.
WA[0] : **0: PA WA disable** 1: PA WA enable.
WA[1] : **0: CA WA disable** 1: CA WA enable.

26. Set Advanced Program Control 1

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control, APC1 [7:0] (Double-byte command)	0	0	**1**	**1**	**1**	**1**	**1**	**0**	**1**	**1**
			APC1 register parameter							

For UltraChip only. Please Do *NOT* use.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is set by DT[2:1] :

DT2	DT1	Duty
0	0	1/65
0	1	1/49
1	0	1/33
1	1	1/55

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_G - V_{MO-} = V_{MO}$

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1701c supports four *BR* as listed below. BR can be selected by software program.

Duty	Bias Ratio	
	BR=0	BR=1
1/65	1/9	1/7
1/49	1/8	1/6
1/33	1/6	1/5
1/55	1/8	1/6

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

The temperature compensation coefficient is **–0.11% / °C (default)** or –0.05% / °C.

V_{LCD} GENERATION

V_{LCD} is supplied by internal charge pump. The source of V_{LCD} is controlled by PC[2:0]. For good product reliability, it is recommended to keep V_{LCD} under 10.0V for all temperature conditions.

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *PC[5:3]* (V_{LCD} Resistor Ratio) with the following relationship:

$$V_{LCD}=((1+Rb/Ra) \times Vev) \times (1+(T-25)\times C_T\%)$$

$$Vev=(1-(63-PM)/162)\times V_{REF}$$

where

Ra and Rb are two design constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is value of electronic volume,

V_{REG} is on-chip contrast voltage,

T is the ambient temperature in °C, and

C_T is temperature compensation coefficient.

V_{LCD} FINE TUNING

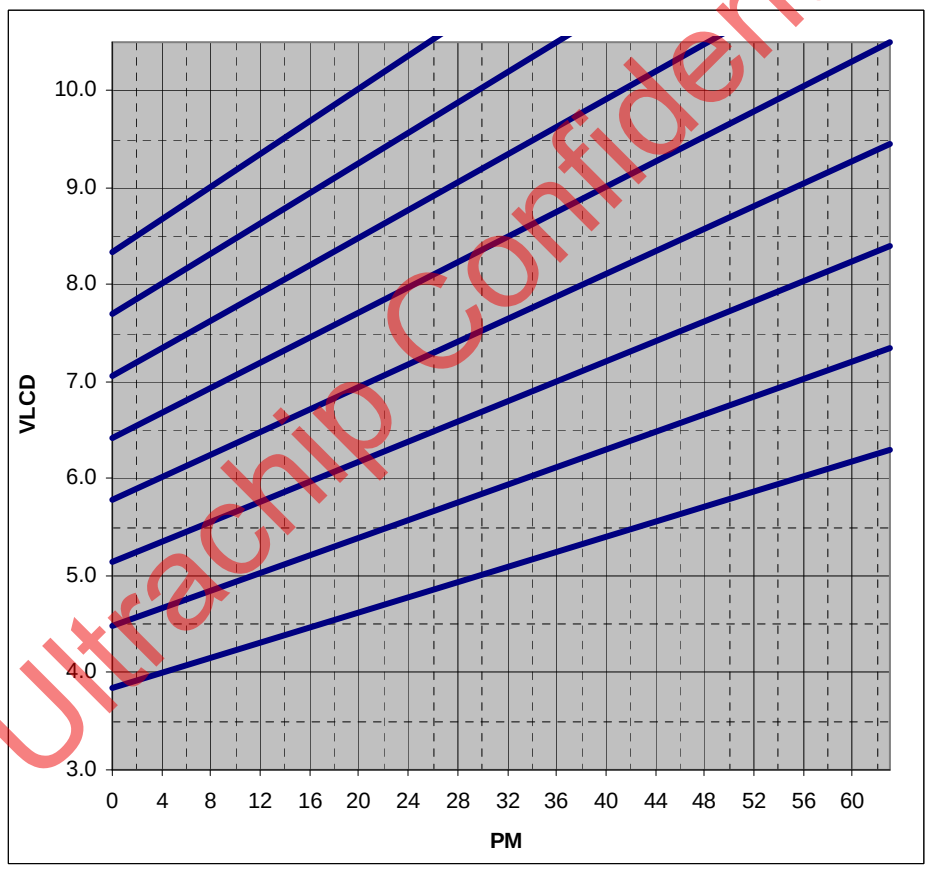
Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LEM design

LOAD DRIVING STRENGTH

The power supply circuit of UC1701c is designed to handle LCD panels with loading up to ~24nF using 20-Ω/Sq ITO glass with $V_{DD2/3} \geqslant 2.6V$. For larger LCD panels, use lower resistance ITO glass packaging.

V_{LCD} QUICK REFERENCE



V_{LCD} Programming Curve.

PC[5:3]	1+Rb/Ra	V_{REF}	PM	V_{LCD} Range (V)
000b	3.0	2.1	0	3.85
			63	6.30
001b	3.5	2.1	0	4.49
			63	7.35
010b	4.0	2.1	0	5.13
			63	8.40
011b	4.5	2.1	0	5.78
			63	9.45
100b	5.0	2.1	0	6.42
			56	10.05
101b	5.5	2.1	0	7.06
			42	10.05
110b	6.0	2.1	0	7.70
			30	10.03
111b	6.5	2.1	0	8.34
			20	10.03

Note: For good product reliability, keep V_{LCD} under **10.0V** over all temperature.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

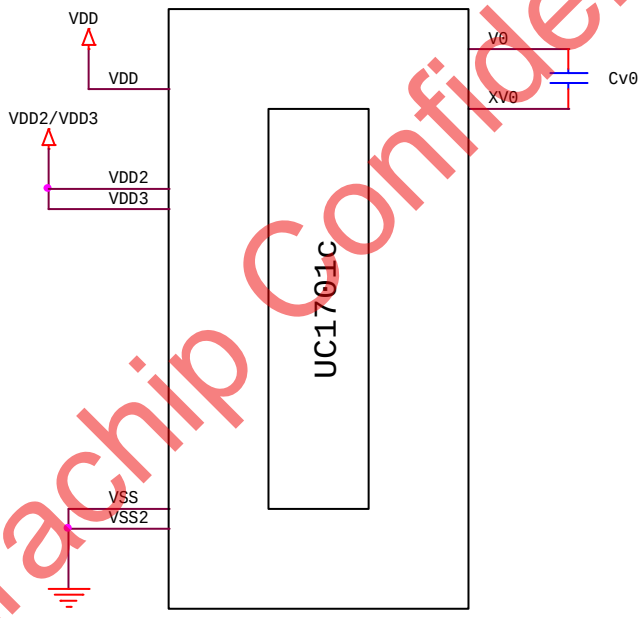


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_{V0} : Optional. 0.1 µF/16V Connect the capacitor of C_{V0} value between XV0 and V0.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1701c contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

4 different frame rates are provided based on different Mux-Rate for system design flexibility.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM*x*, where x = 0~63, refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1701c will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1", and UC1701c will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn ON COM and SEG drivers.

That is the display is turned ON after setting PC[2:0]=111b and DC[2]=1.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1701c can be as short as 153µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 9.23\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 2.76\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 6.30\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / (# of column), where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, and crosstalk will increase.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Example:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/65	1/9	10.6%	9.6%	7.5%

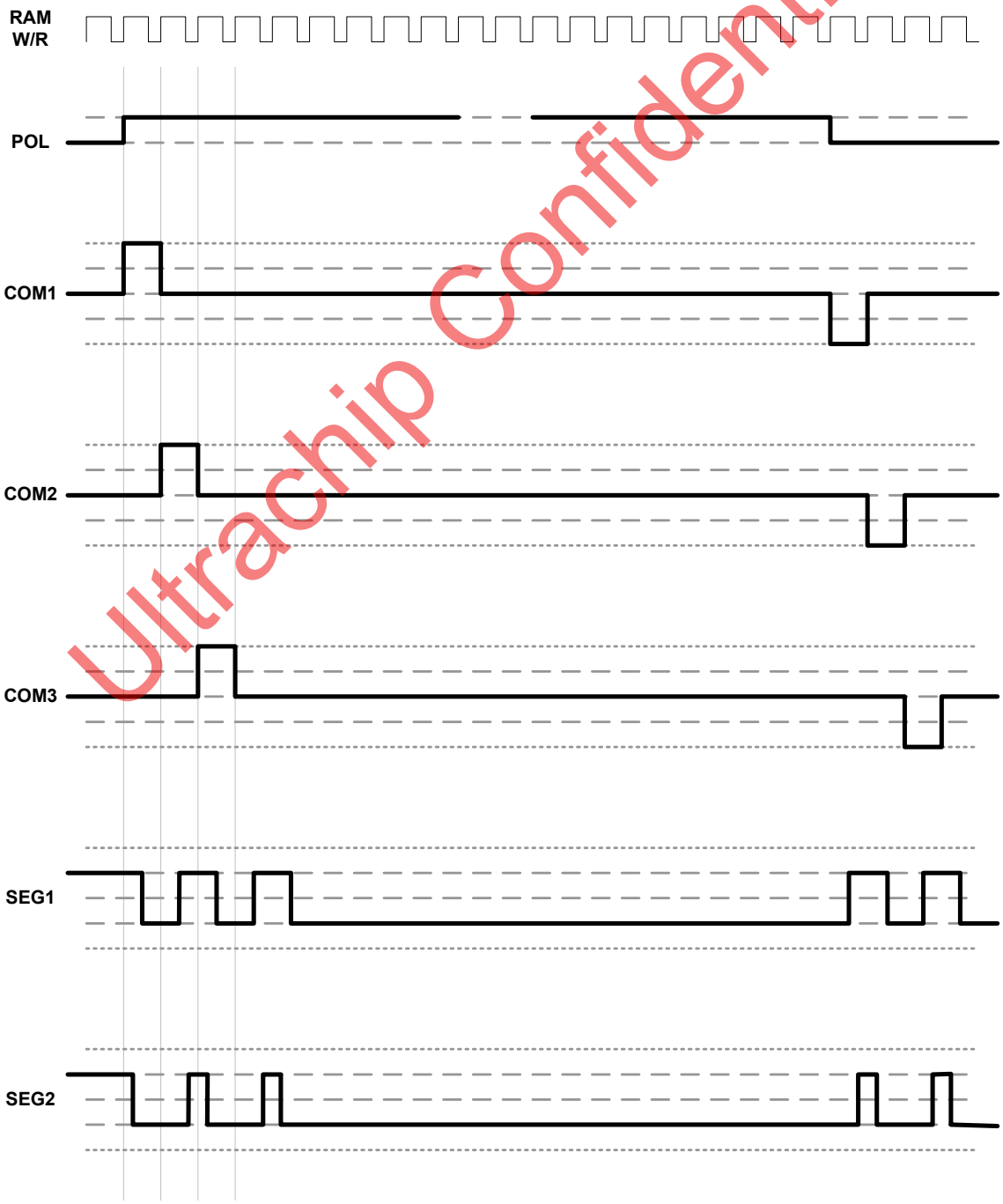


FIGURE 2: COM and SEG Electrode Driving Waveform

THE COMMON OUTPUT STATUS SELECT CIRCUIT

In the UC1701c chips, the COM output scan direction can be selected by the common output status select command. (See the table below for details.) Consequently, the constraints in IC layout at the time of LCD module assembly can be minimized.

Duty	Direction	COM[0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM[48:63]	CIC
1/65	0	COM [0:63]							CIC
	1	COM [63:0]							
1/49	0	COM[0:23]		NC			COM [24:47]		CIC
	1	COM[47:24]		NC			COM [23:0]		
1/33	0	COM[0:15]	NC					COM[16:31]	CIC
	1	COM[31:16]	NC					COM[15:0]	
1/55	0	COM [0:26]			NC	COM [27:53]			CIC
	1	COM [53:27]			NC	COM [26:0]			

Table 2: Duty Layout

HOST INTERFACE

As summarized in the table below, UC1701c supports 2 8-bit parallel bus protocols and 2 serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use serial bus to create compact LCD modules and minimize connector pins.

		Bus Type			
		8080	**6800**	**S8 (4-wire)**	**I²C (2-wire)**
Width		8-bit	8-bit	Serial	
Access		Read / Write		Write only	
Control & Data Pins	BM[1:0]	10	11	0x	
	TST5	Open			1
	CS0	Chip select			--
	CD	Control/Data	0	–	
	WR0	$\overline{WR}$	R/$\overline{W}$	–	A3
	WR1	$\overline{RD}$	EN	–	A2
	DB[5:0]	Data		–	
	DB[7:6]	Data		DB[6]=SCK, DB[7]=SDA	

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Bus Interface	CS Init. Bus State	RESET Init. Bus State
8-bit	✓	–	✓
S8	✓	✓	✓
I²C	–	–	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- RESET can be pin reset / soft reset.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1701c internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that every time memory address is modified, either in parallel mode or serial mode, by either `Set CA` or `Set PA` command, a dummy read cycle needs to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data is transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

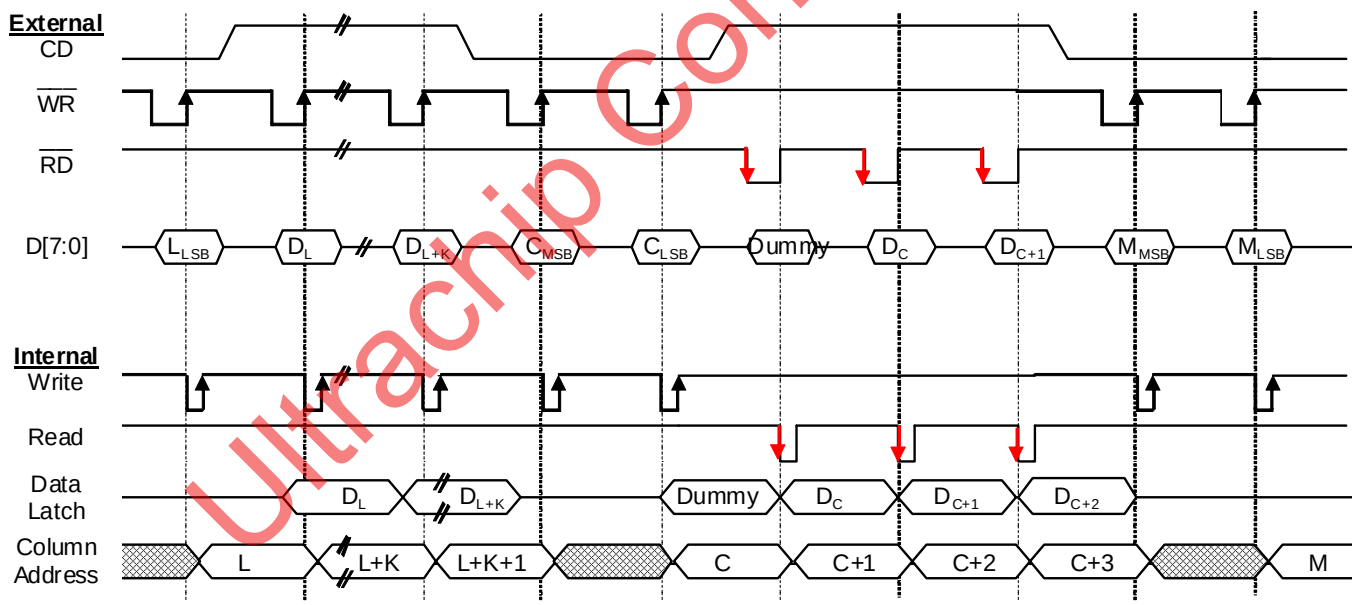


Figure 3: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1701c supports 2 serial modes: 4-wire SPI mode (S8). Bus interface mode is determined by the wiring of the BM[1:0] and TST5. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Only write operations are supported in 4-wire serial mode. Pins WR[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse.

Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

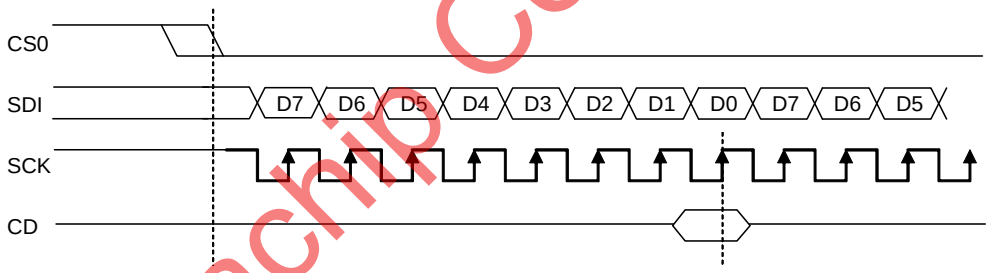
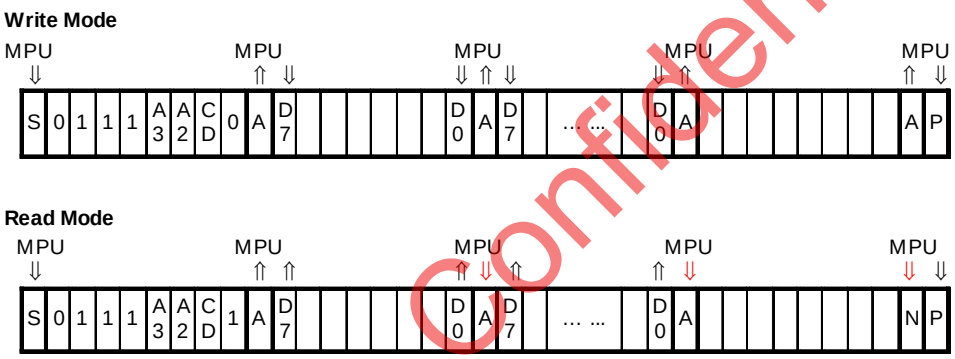


Figure 4: 4-wire Serial Interface (S8)

I²C (2-WIRE) INTERFACE



When BM[1:0] is set to "LH" and TST5 is set to "H", UC1701c is configured as an I²C bus signaling protocol compliant slave device. Please refer to I²C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins WR0~WR1 (WR[0] becomes A[3], WR[1] becomes A[2]) are used to configure UC1701c' device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I²C mode.

Each UC1701c I²C interface sequence starts with a "S" (Start) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

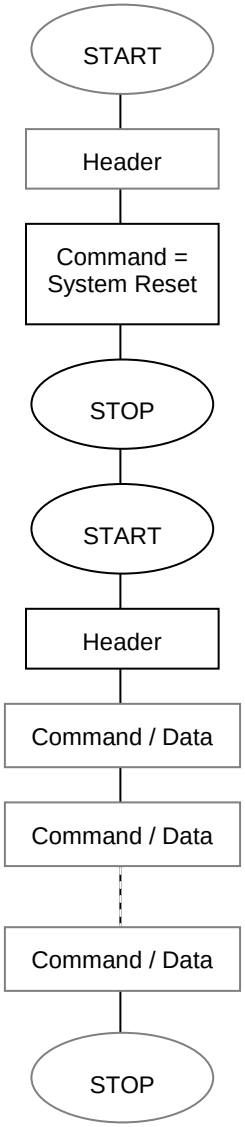
Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I²C mode and should be connected to V_{SS}.

The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1701c will send out an "A" (Acknowledge signal, pull to "L"). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1701c) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE mode), or an N (Not Acknowledged, in READ mode) is sent by the bus master.

When using I²C serial mode, if command `System Reset` is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

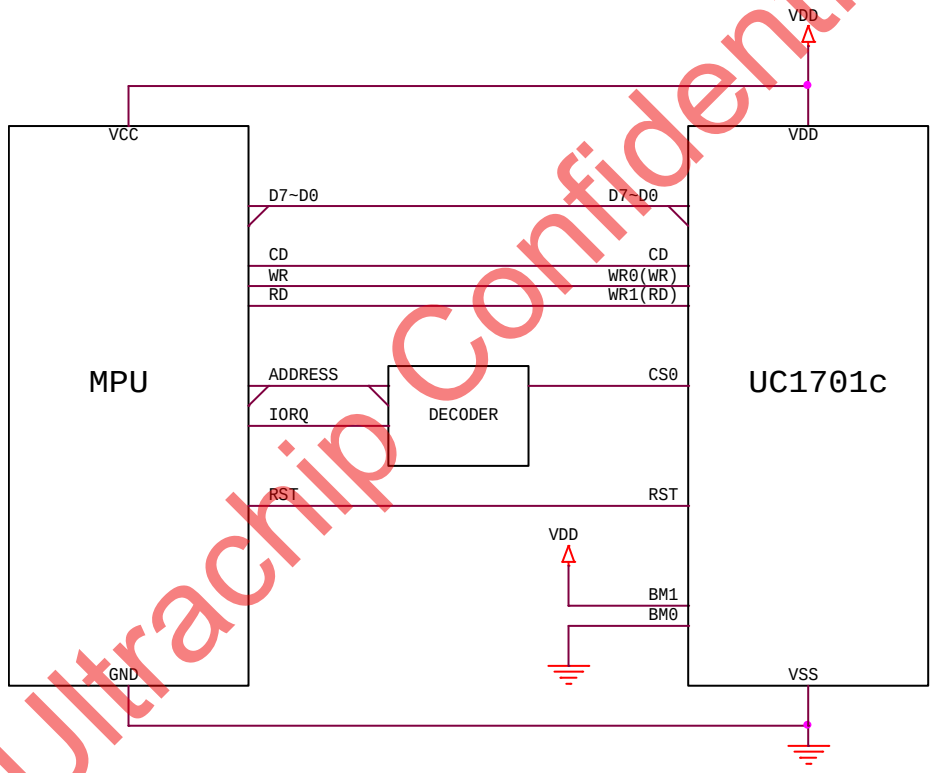


FIGURE 5: 8080/8bit parallel mode reference circuit

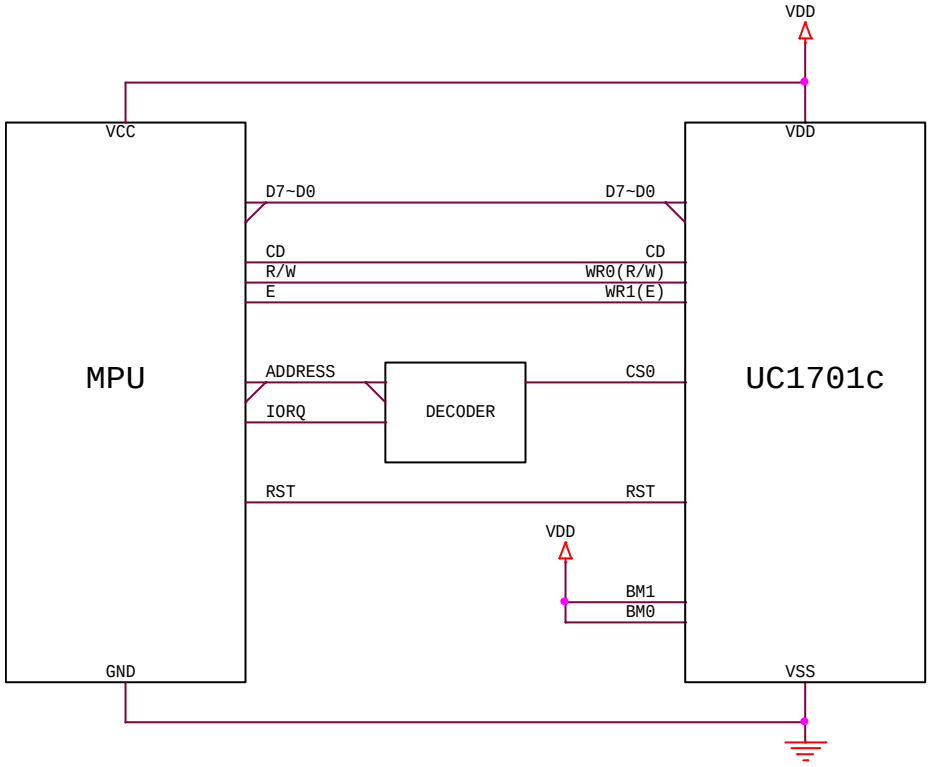


FIGURE 6: 6800/8bit parallel mode reference circuit

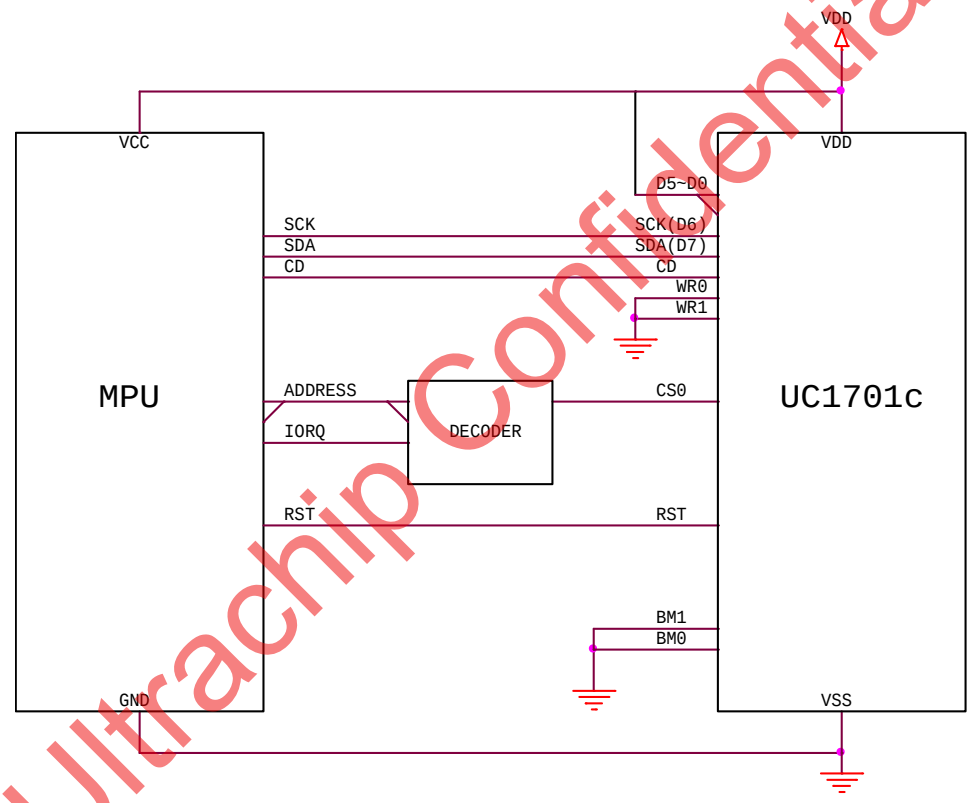


FIGURE 7: Serial-8 serial mode reference circuit

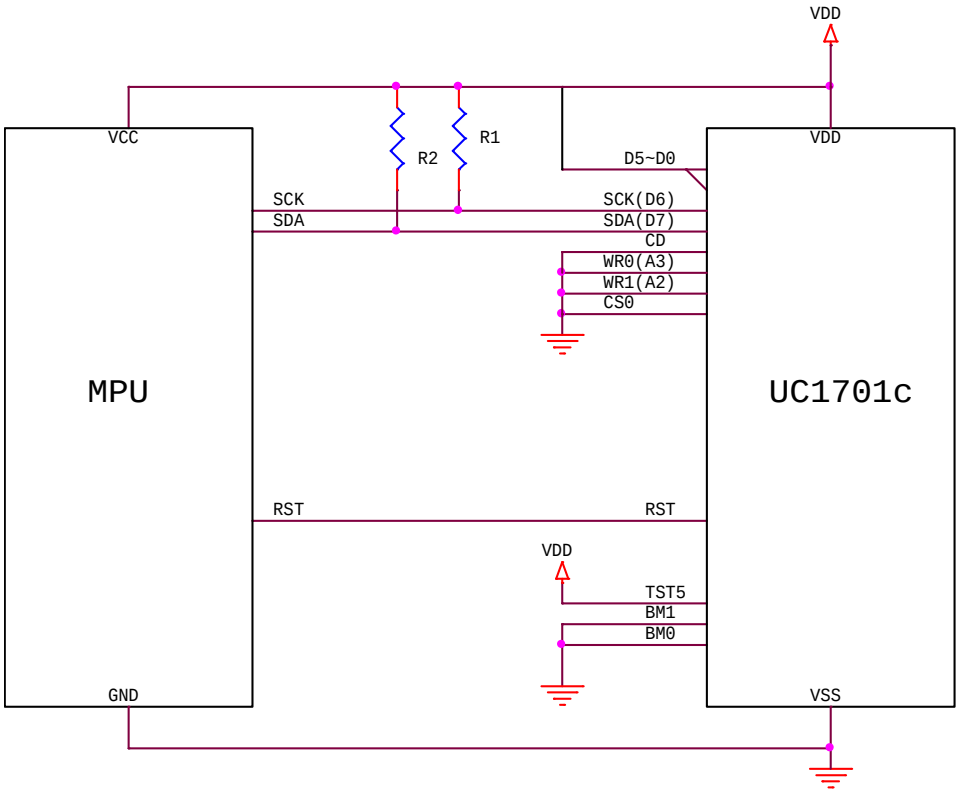


FIGURE 8: I²C serial mode reference circuit

Note

- The ID pins are for production control. The connection will affect the content of D[7] of the 1-st byte of the `Get Status` command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When the RST pin is not used, connect it to V_{DD}.
- When using I^2C serial mode, WR1/0 are user configurable and affect A[3:2] of device address.
- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.
- When using Read function:

(8080) Set WR1=0 (6800) Set WR1=1 → data output will be enabled. (Serial) Set SCK=0	(8080) Set WR1=1 (6800) Set WR1=0 → data output will be disabled. (Serial) Set SCK=1

- It is REQUIRED to set MPU's data port to 1 before Data Read or Status Read actions.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data is stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 65x132.

After setting CA and PA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Page Address (PA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (131–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), or Mirror Y (MY, LC[1]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*
Otherwise
Line = Mod (*Line*+1, 64)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

MY IMPLEMENTATION

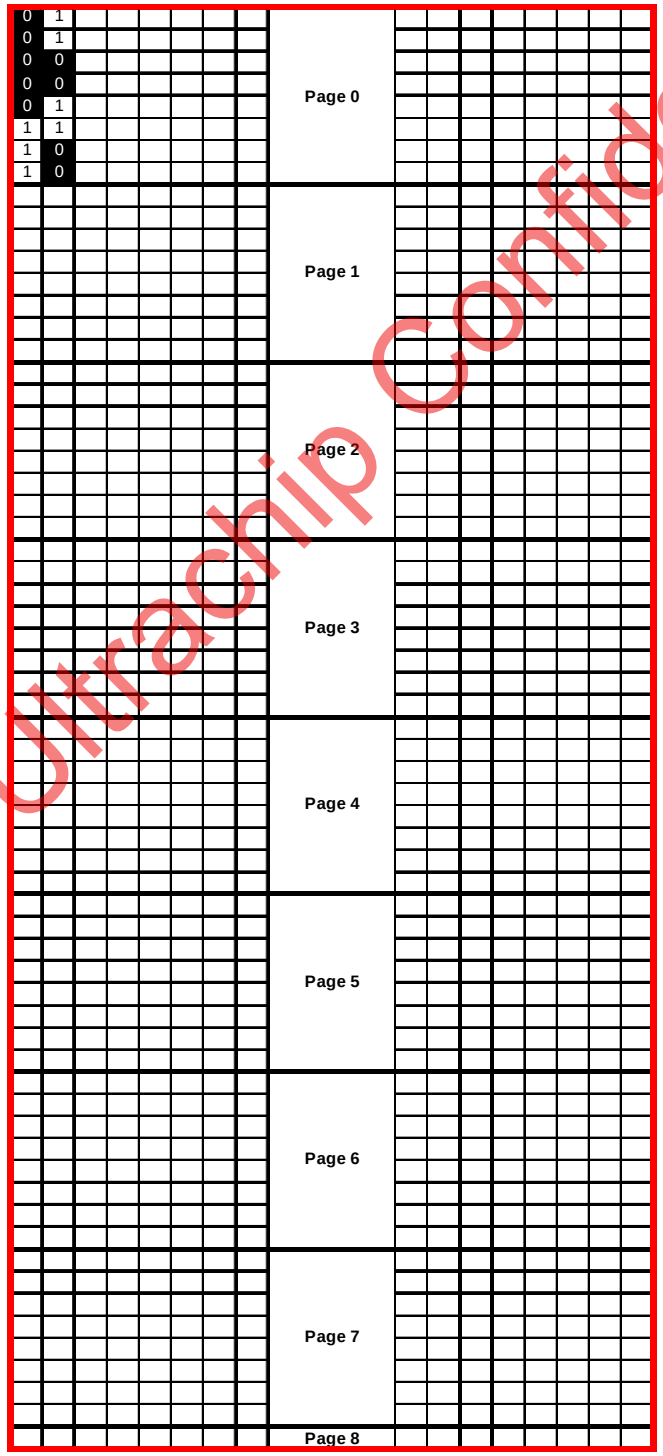
Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod (*SL + MR -1*, *64*)
Otherwise
Line = Mod (*Line-1*, *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

PA[3:0]	0	Line AddeCss
0000	D0	00H
	D1	01H
	D2	02H
	D3	03H
	D4	04H
	D5	05H
	D6	06H
	D7	07H
0001	D0	08H
	D1	09H
	D2	0AH
	D3	0BH
	D4	0CH
	D5	0DH
	D6	0EH
	D7	0FH
0010	D0	10H
	D1	11H
	D2	12H
	D3	13H
	D4	14H
	D5	15H
	D6	16H
	D7	17H
0011	D0	18H
	D1	19H
	D2	1AH
	D3	1BH
	D4	1CH
	D5	1DH
	D6	1EH
	D7	1FH
0100	D0	20H
	D1	21H
	D2	22H
	D3	23H
	D4	24H
	D5	25H
	D6	26H
	D7	27H
0101	D0	28H
	D1	29H
	D2	2AH
	D3	2BH
	D4	2CH
	D5	2DH
	D6	2EH
	D7	2FH
0110	D0	30H
	D1	31H
	D2	32H
	D3	33H
	D4	34H
	D5	35H
	D6	36H
	D7	37H
0111	D0	38H
	D1	39H
	D2	3AH
	D3	3BH
	D4	3CH
	D5	3DH
	D6	3EH
	D7	3FH
1000	D0	40H

RAM



MX=0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8					SEG128	SEG129	SEG130	SEG131	SEG132
MX=1	SEG132	SEG131	SEG130	SEG129	SEG128	SEG127	SEG126	SEG125					SEG5	SEG4	SEG3	SEG2	SEG1

Panel Location	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=25	MY=1 SL=25
COM1	C1	C49	C64	C48	C25	C9
COM2	C2	C50	C63	C47	C24	C8
COM3	C3	C51	C62	C46	C23	C7
COM4	C4	C52	C61	C45	C22	C6
COM5	C5	C53	C60	C44	C21	C5
COM6	C6	C54	C59	C43	C20	C4
COM7	C7	C55	C58	C42	C19	C3
COM8	C8	C56	C57	C41	C18	C2
COM9	C9	C57	C56	C40	C17	C1
COM10	C10	C58	C55	C39	C16	---
COM11	C11	C59	C54	C38	C15	---
COM12	C12	C60	C53	C37	C14	---
COM13	C13	C61	C52	C36	C13	---
COM14	C14	C62	C51	C35	C12	---
COM15	C15	C63	C50	C34	C11	---
COM16	C16	C64	C49	C33	C10	---
COM17	C17	C1	C48	C32	C9	---
COM18	C18	C2	C47	C31	C8	---
COM19	C19	C3	C46	C30	C7	---
COM20	C20	C4	C45	C29	C6	---
COM21	C21	C5	C44	C28	C5	---
COM22	C22	C6	C43	C27	C4	---
COM23	C23	C7	C42	C26	C3	---
COM24	C24	C8	C41	C25	C2	---
COM25	C25	C9	C40	C24	C1	---
COM26	C26	C10	C39	C23	C64	C48*
COM27	C27	C11	C38	C22	C63	C47
COM28	C28	C12	C37	C21	C62	C46
COM29	C29	C13	C36	C20	C61	C45
COM30	C30	C14	C35	C19	C60	C44
COM31	C31	C15	C34	C18	C59	C43
COM32	C32	C16	C33	C17	C58	C42
COM33	C33	C17	C32	C16	C57	C41
COM34	C34	C18	C31	C15	C56	C40
COM35	C35	C19	C30	C14	C55	C39
COM36	C36	C20	C29	C13	C54	C38
COM37	C37	C21	C28	C12	C53	C37
COM38	C38	C22	C27	C11	C52	C36
COM39	C39	C23	C26	C10	C51	C35
COM40	C40	C24	C25	C9	C50	C34
COM41	C41	C25	C24	C8	C49	C33
COM42	C42	C26	C23	C7	C48	C32
COM43	C43	C27	C22	C6	C47	C31
COM44	C44	C28	C21	C5	C46	C30
COM45	C45	C29	C20	C4	C45	C29
COM46	C46	C30	C19	C3	C44	C28
COM47	C47	C31	C18	C2	C43	C27
COM48	C48	C32	C17	C1	C42	C26
COM49	C49	C33	C16	---	C41	C25
COM50	C50	C34	C15	---	C40	C24
COM51	C51	C35	C14	---	C39	C23
COM52	C52	C36	C13	---	C38	C22
COM53	C53	C37	C12	---	C37	C21
COM54	C54	C38	C11	---	C36	C20
COM55	C55	C39	C10	---	C35	C19
COM56	C56	C40	C9	---	C34	C18
COM57	C57	C41	C8	---	C33	C17
COM58	C58	C42	C7	---	C32	C16
COM59	C59	C43	C6	---	C31	C15
COM60	C60	C44	C5	---	C30	C14
COM61	C61	C45	C4	---	C29	C13
COM62	C62	C46	C3	---	C28	C12
COM63	C63	C47	C2	---	C27	C11
COM64	C64	C48	C1	---	C26	C10
CIC	CIC	CIC	CIC	CIC	CIC	CIC
			65	49	65	49
			MUX			

Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

- Page 0 SEG 1 (D7-D0) : 11100000b
- Page 0 SEG 2 (D7-D0) : 00110011b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1701c has 2 different types of reset: Pin Reset (hardware reset) and System Reset (Software reset). Pin Reset is activated by connecting the RST pin to ground; while System Reset is performed by software commands. After each power-up, a Pin Reset, which is in 3mS, is required. In the following discussions, reset means Pin Reset.

The differences between pin reset (hardware reset) and system reset (software reset) :

Procedure	Pin Reset (hardware reset)	System Reset (software reset)
Display OFF: DC[2]=0, all SEGs/COMs output at V_{SS}	V	X
Normal Display: DC[0]=0, DC[1]=0	V	X
SEG Normal Direction: MX=0	V	X
Clear Serial Counter and Shift Register (if using Serial Interface)	V	X
Bias Selection: BR=0	V	X
Booster Level BL[1:0]=0	V	X
Exit Power Saving Mode	V	X
Power Control OFF: PC[2:0]=000b	V	X
Exit Cursor Update mode	V	V
Scroll Line SL[5:0]=0	V	V
Column Address CA[7:0]=0	V	V
Page Address PA[3:0]=0	V	V
COM Normal Direction: MY=0	V	V
V_{LCD} Regulation Ratio PC[5:3]=100b	V	V
PM[5:0]=10 0000b	V	V
Exit Test Mode	V	V

RESET STATUS

When UC1701c enters RESET sequence:

- Operation mode will be “Reset”
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1701c has three operating modes (OM):
Reset, Sleep, and Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

There are 2 commands that will initiate OM transitions:
Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter sleep mode.

OM changes are synchronized with the edges of UC1701c internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
RST_ pin pulled “L”	Reset	00
Set Driver Enable to “0”	Sleep	10
Set Driver Enable to “1”	Normal	11

Table 5: OM changes

When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1701c consumes very little energy in Sleep mode (typically under 5µA).

EXITING SLEEP MODE

UC1701c contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1701c internal voltage sources are restored to their proper values.

POWER-UP SEQUENCE

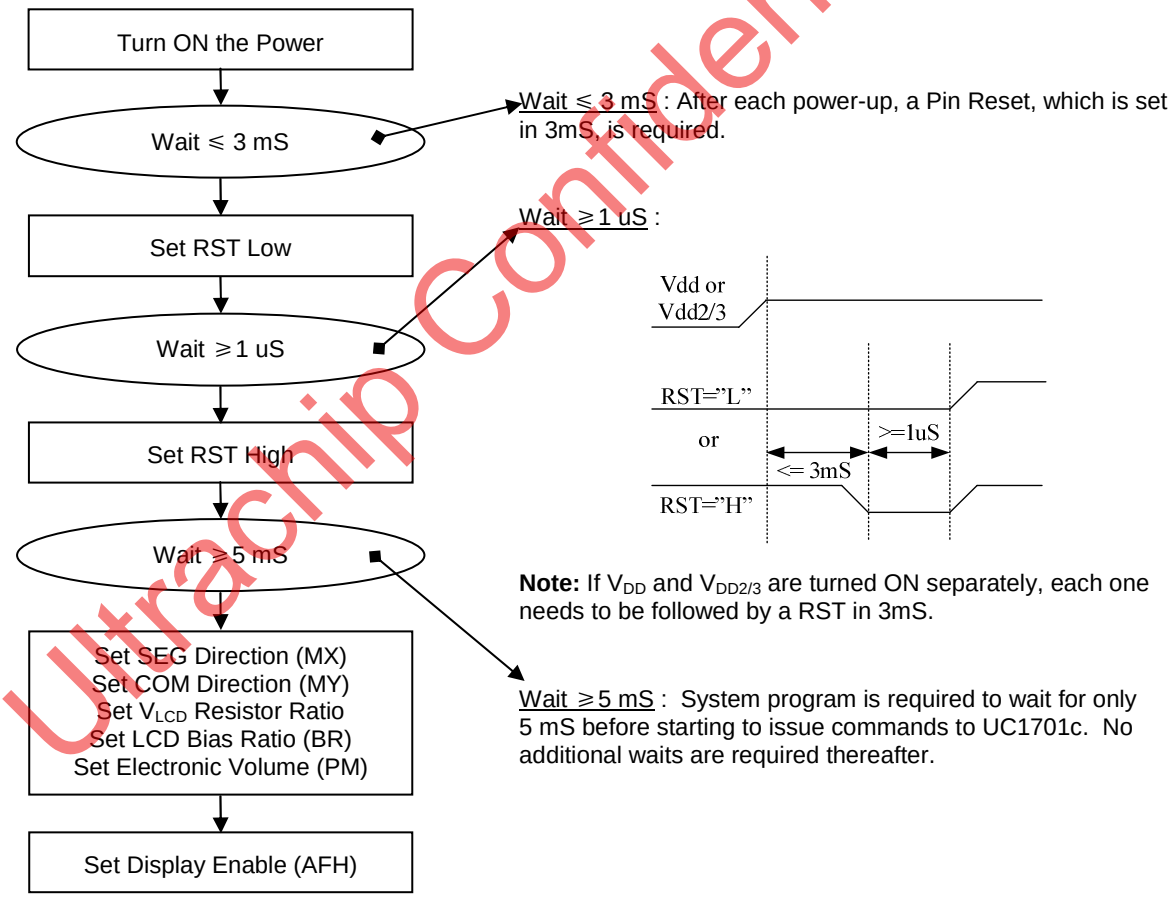


Figure 9: REFERENCE POWER-UP SEQUENCE

There's no delay needed while turning ON V_{DD} and $V_{DD2/3}$, and either one can be turned on first:

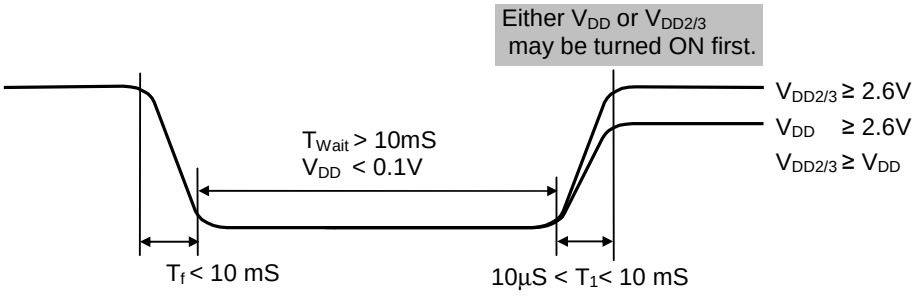


Figure 10: Power Off-On Sequence

ENTER/EXIT SLEEP MODE SEQUENCE

UC1701c enters Sleep mode from Display mode by issuing Set Display Disable command and setting all-pixel-ON.

To exit Sleep mode, set All-pixel-OFF.

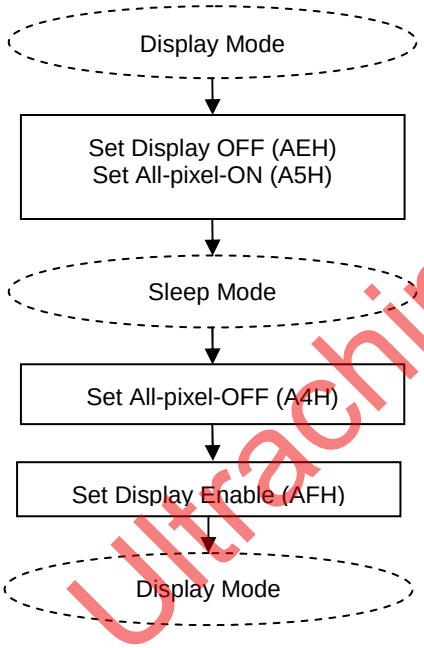


FIGURE 11: Reference Enter/Exit Sleep Mode Sequence

Power-Down Sequence

To prevent the charge stored in capacitor Cv0 causing abnormal residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

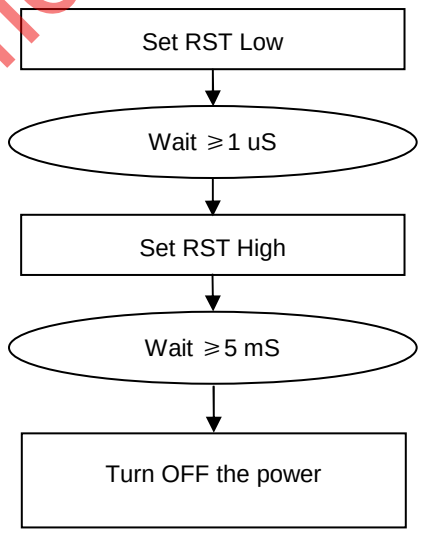


FIGURE 12: Reference Power-Down Sequence

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

C/D The type of the interface cycle. It can be either Command (0) or Data (1).

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

Type
Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Turn ON V_{DD} and $V_{DD2/3}$	Wait until V_{DD}, $V_{DD2/3}$ are stable
R	–	–	–	–	–	–	–	–	–	–	Wait ⩽ 3 mS	
R	–	–	–	–	–	–	–	–	–	–	Set RST pin Low	Wait 1 uS after RST is Low
R	–	–	–	–	–	–	–	–	–	–	Set RST pin High	Wait 5 mS after RST is High
O	0	0	1	1	1	1	1	0	1	0	Set Adv. Program Control 0	
			1	0	0	1	0	0	1	1		Set Wrap Around Enable
R	0	0	1	0	1	0	0	0	0	#	Set SEG Direction	Set up LCD format specific parameters, MX, MY, etc.
R	0	0	1	1	0	0	#	–	–	–	Set COM Direction	
R	0	0	0	0	1	0	0	#	#	#	Set V_{LCD} Resistor Ratio	LCD specific operating voltage setting
R	0	0	1	0	1	0	0	0	1	#	Set LCD Bias Ratio	
R	0 0	0 0	1 0	0 0	0 #	0 #	0 #	0 #	0 #	1 #	Set Electronic Volume	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	0	0	1	0	1	1	1	1	Set Power Control	
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~5mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 - notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$ -V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+11.0	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	^{o}C
T_{STR}	Storage temperature	-55	+125	^{o}C

Note:

1. All voltages are based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		2.6	2.7~3.3	3.6	V
$V_{DD2/3}$	Supply for bias & pump		2.6	2.7~3.3	3.6	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geq$ 2.6V, 25°C	3.85		10.0	V
V_D	LCD data voltage	$V_{DD2/3} \geq$ 2.6V, 25°C	0.80		1.32	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{OL}	Output logic LOW	I_{OH} = -0.5mA			$0.2V_{DD}$	V
V_{OH}	Output logic HIGH	I_{OL} = 0.5mA	$0.8V_{DD}$			V
I_{IL}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-50	1.5	50	uA
I_{SB}	Standby current	V_{DD} = $V_{DD2/3}$ = 3.3V, Temp = 85°C			50	uA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 10V		2000	3000	Ω
$R_{0(COM)}$	COM output impedance	V_{LCD} = 10V		2000	3000	Ω
F_{FR}	Average Frame Rate	Duty=1/65	-15%	77	+20%	Hz
		Duty=1/49		153		
		Duty=1/33		76		
		Duty=1/55		136		

POWER CONSUMPTION

V_{DD} = 2.7 V,
V_{LCD} = 8.49 V
Mux Rate = 65,
Temperature = 25°C

Bias Ratio = 0b,
Frame Rate = 77Hz,
Bus mode = 6800,

PM = 32,
C_{v0} = 0.1 uF,
All outputs are open circuit.

Display Pattern	Conditions	Typical	Maximum	Unit
All-OFF	Bus = idle	203	325	μA
2-pixel checker	Bus = idle	205	328	μA
1-pixel checker	Bus = idle	218	349	μA
-	Bus = idle (standby current)	-	5	μA

AC CHARACTERISTICS

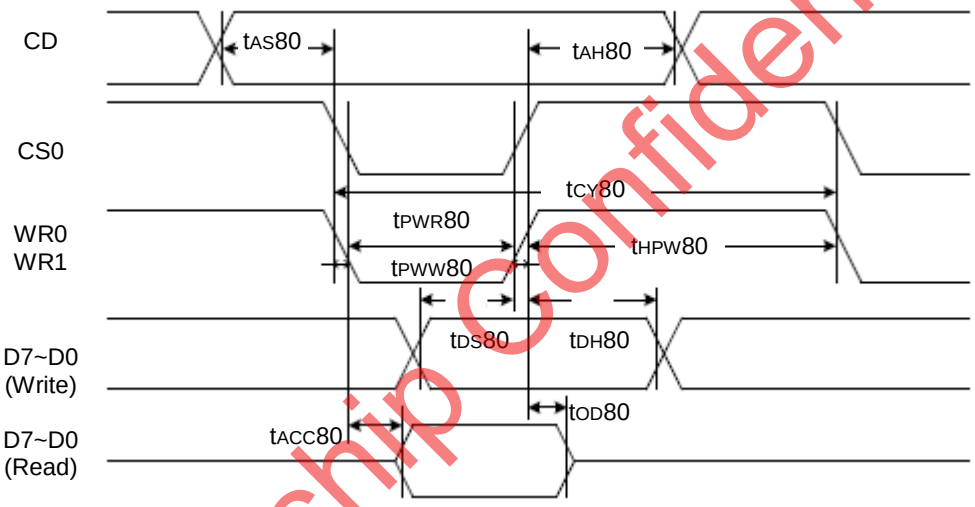


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.6V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	–	nS
t_{CY80} t_{PWR80}, t_{PWW80} t_{HPW80}	WR0, WR1	Cycle time Low Pulse width High pulse width		250 / 250 140 / 140 80 / 80	–	nS
t_{DS80} t_{DH80}	D7~D0 (Write)	Data setup time Data hold time		-- / 40 -- / 20	–	nS
t_{ACC80} t_{OD80}	D7~D0 (Read)	Read access time Output disable time	C_L= 16pF	– / -- 5 / --	70 50	nS

Note: tr (rising time), tf (falling time): ≤ 15nS

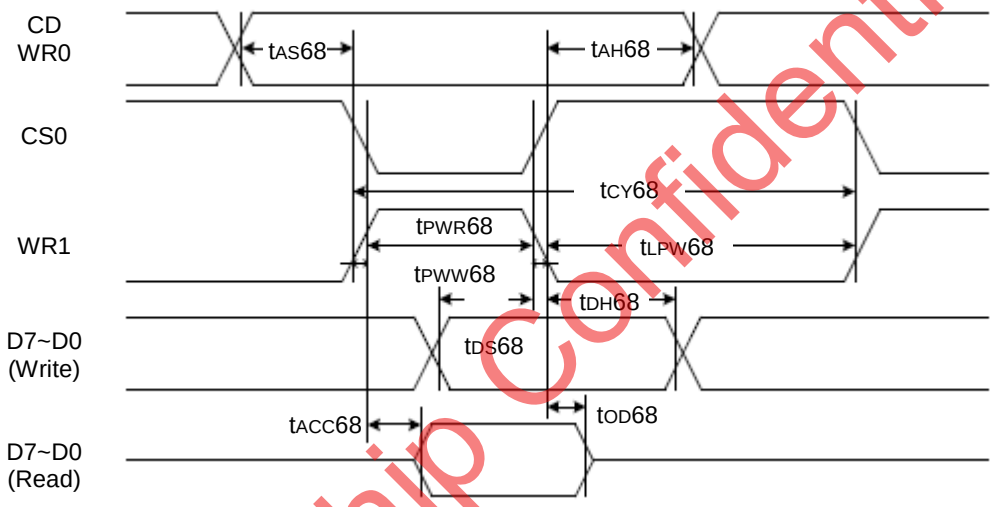


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.6V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	–	nS
t_{CY68} t_{PWR68}, t_{PWW68} t_{LPW68}	WR1	System cycle time High Pulse width Low pulse width		250 / 250 140 / 140 80 / 80	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		-- / 40 -- / 10	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L= 16pF	– / -- 5 / --	70 50	nS

Note: tr (rising time), tf (falling time) : ≤ 15nS

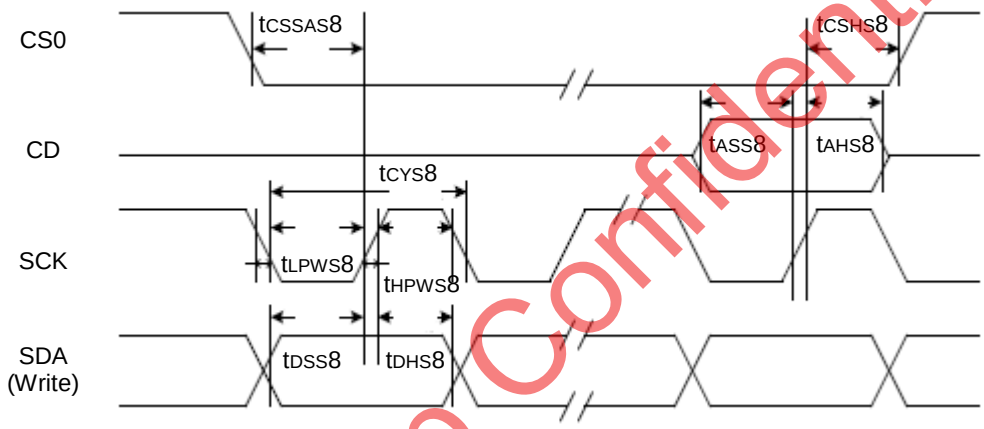


FIGURE 15: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.6V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)						
t_{ASS8}	CD	Address setup time		20	–	nS
t_{AHS8}		Address hold time		10		
t_{CSSAS8}	CS0	Chip select setup time		20	–	nS
t_{CSHS8}		Chip select hold time		40		
t_{CYS8}	SCK	Cycle time		80	–	nS
t_{LPWS8}		Low pulse width		25		
t_{HPWS8}		High pulse width		25		
t_{DSS8}	SDA (Write)	Data setup time		20	–	nS
t_{DHS8}		Data hold time		10		

Note: tr (rising time), tf (falling time) : ≤ 15nS

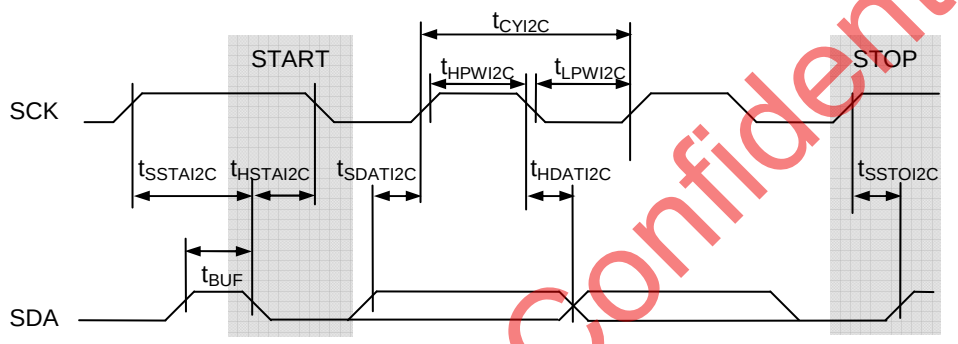


FIGURE 16: Serial bus timing characteristics (for I^2C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.6V ⩽ V_{DD} ⩽ 3.6V, Ta= –30 to +85°C)						
t_{CYI2C}	SCK	SCK cycle time		305	–	nS
t_{HPWI2C}		High pulse width		110		
t_{LPWI2C}		Low pulse width		165		
$t_{SSTAI2C}$	SCK SDA	Setup time – START		28	–	nS
$t_{HSTAI2C}$		Hold time – START		55		
t_{SDAI2C}		Setup time – Data		40		
t_{HDAI2C}		Hold time – Data		11		
$t_{SSTOI2C}$		Setup time – STOP		28		
t_{BUF}	SDA	Bus Free time between STOP and START		165	–	nS

Note: tr (Rising time), tf (falling time): ⩽ 15nS

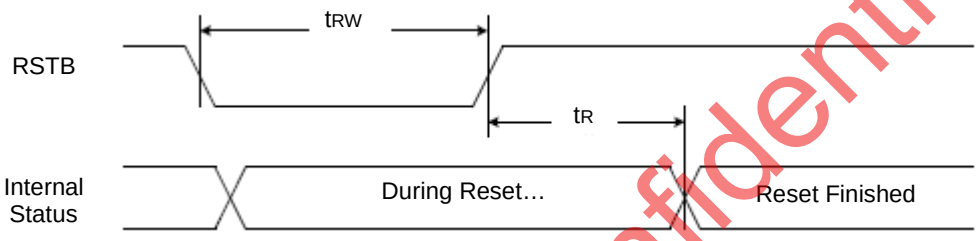
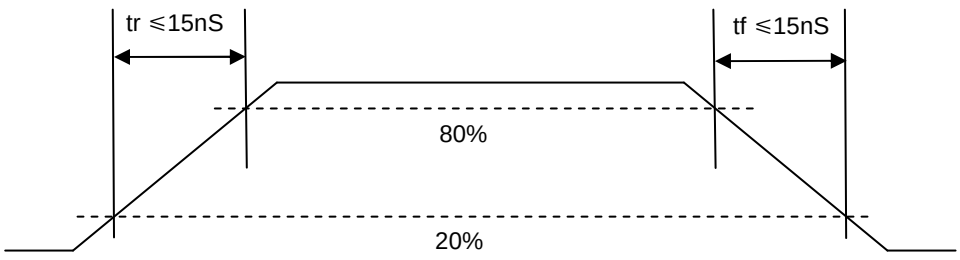


FIGURE 17: Reset Characteristics

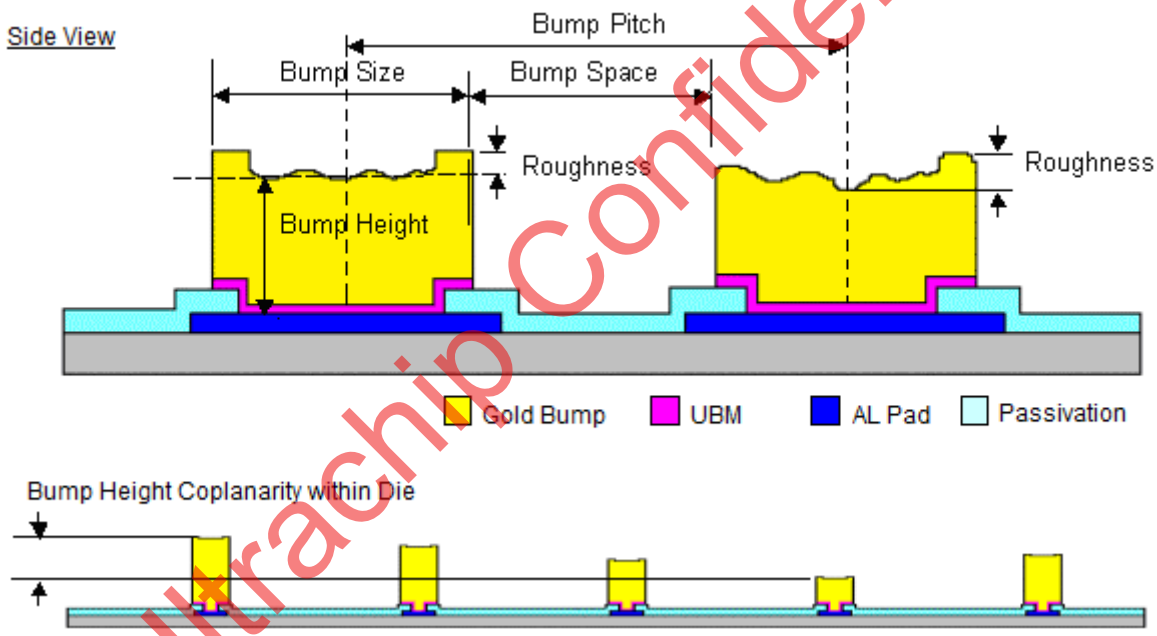
(2.6V ≤ V_{DD} < 3.6V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
t_{RW}	RST	Reset low pulse width		1	–	µS
t_R	RST, Internal Status	Reset to Internal Status pulse delay		--	1	mS

Note: For each mode, the signal's rising time (tr) and falling time (tf) are stipulated to be equal to or less than 15nS each.



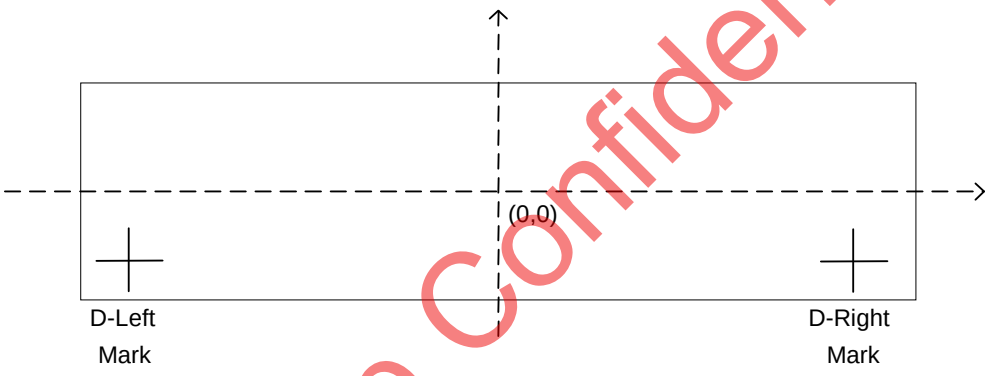
PHYSICAL DIMENSIONS



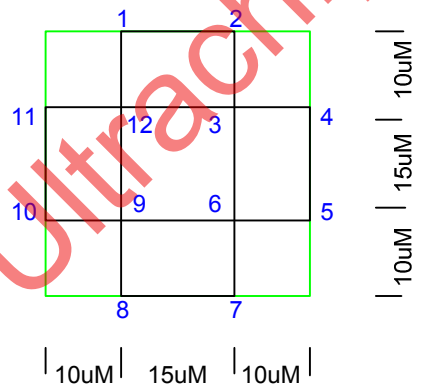
Die / Bump Information:

Die Size:	(5040 µM ± 40 µM) x (703 µM ± 40 µM)
Die Thickness:	300 µM ± 20 µM
	D_{MAX} - D_{MIN} ≤ 2 µM
Bump Height:	10 µM ± 3 µM (Part Number: UC1701cGAB)
	15 µM ± 3 µM (Part Number: UC1701cGBB)
	$H_{MAX} – H_{MIN}$ ≤ 2 µM
Hardness:	90Hv ± 25Hv
Bump Size:	(15µM ± 2 µM) x (100µM ± 2 µM)
Bump Pitch:	27 µM
Bump Gap:	12 µM ± 3 µM
Bump Area:	1500uM^2
Coordinate origin:	Chip center
Pad reference:	Pad center

ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

The "+" mark is symmetric both horizontally and vertically.

COORDINATES:

Point	D-Left Mark		D-Right Mark	
	X	Y	X	Y
1	-1984.5	-149.5	1969.5	-149.5
2	-1969.5	-149.5	1984.5	-149.5
3	-1969.5	-159.5	1984.5	-159.5
4	-1959.5	-159.5	1994.5	-159.5
5	-1959.5	-174.5	1994.5	-174.5
6	-1969.5	-174.5	1984.5	-174.5
7	-1969.5	-184.5	1984.5	-184.5
8	-1984.5	-184.5	1969.5	-184.5
9	-1984.5	-174.5	1969.5	-174.5
10	-1994.5	-174.5	1959.5	-174.5
11	-1994.5	-159.5	1959.5	-159.5
12	-1984.5	-159.5	1969.5	-159.5

PAD COORDINATES

#	Pad	X	Y	W	H
1	COM<53>	-2363	-247	15	100
2	COM<54>	-2336	-247	15	100
3	COM<55>	-2309	-247	15	100
4	COM<56>	-2282	-247	15	100
5	COM<57>	-2255	-247	15	100
6	COM<58>	-2228	-247	15	100
7	COM<59>	-2201	-247	15	100
8	COM<60>	-2174	-247	15	100
9	COM<61>	-2147	-247	15	100
10	COM<62>	-2120	-247	15	100
11	COM<63>	-2093	-247	15	100
12	CIC	-2066	-247	15	100
13	TST4	-1970	-274.5	50	45
14	CS0	-1905	-274.5	50	45
15	RST	-1840	-274.5	50	45
16	CD	-1775	-274.5	50	45
17	WR0	-1710	-274.5	50	45
18	WR1	-1645	-274.5	50	45
19	VDDX	-1580	-274.5	50	45
20	D0	-1515	-274.5	50	45
21	D1	-1450	-274.5	50	45
22	D2	-1385	-274.5	50	45
23	D3	-1320	-274.5	50	45
24	D4	-1255	-274.5	50	45
25	D5	-1190	-274.5	50	45
26	D6	-1125	-274.5	50	45
27	D7	-1060	-274.5	50	45
28	VDD	-995	-274.5	50	45
29	VDD	-930	-274.5	50	45
30	VDD2	-865	-274.5	50	45
31	VDD2	-800	-274.5	50	45
32	VDD2	-735	-274.5	50	45
33	VDD3	-670	-274.5	50	45
34	VSS	-605	-274.5	50	45
35	VSS	-540	-274.5	50	45
36	VSS2	-475	-274.5	50	45
37	VSS2	-410	-274.5	50	45
38	VSS2	-345	-274.5	50	45
39	VSS2	-280	-274.5	50	45
40	V0in	-215	-274.5	50	45
41	V0in	-150	-274.5	50	45
42	V0s	-85	-274.5	50	45
43	V0out	-20	-274.5	50	45
44	V0out	45	-274.5	50	45
45	XV0out	110	-274.5	50	45
46	XV0out	175	-274.5	50	45
47	XV0s	240	-274.5	50	45
48	XV0in	305	-274.5	50	45
49	XV0in	370	-274.5	50	45
50	VMO	435	-274.5	50	45
51	VMO	500	-274.5	50	45
52	VGin	565	-274.5	50	45
53	VGin	630	-274.5	50	45
54	VGs	695	-274.5	50	45
55	VGout	760	-274.5	50	45
56	DUMMY	820	-274.5	45	45
57	DUMMY	875	-274.5	45	45
58	DUMMY	930	-274.5	45	45

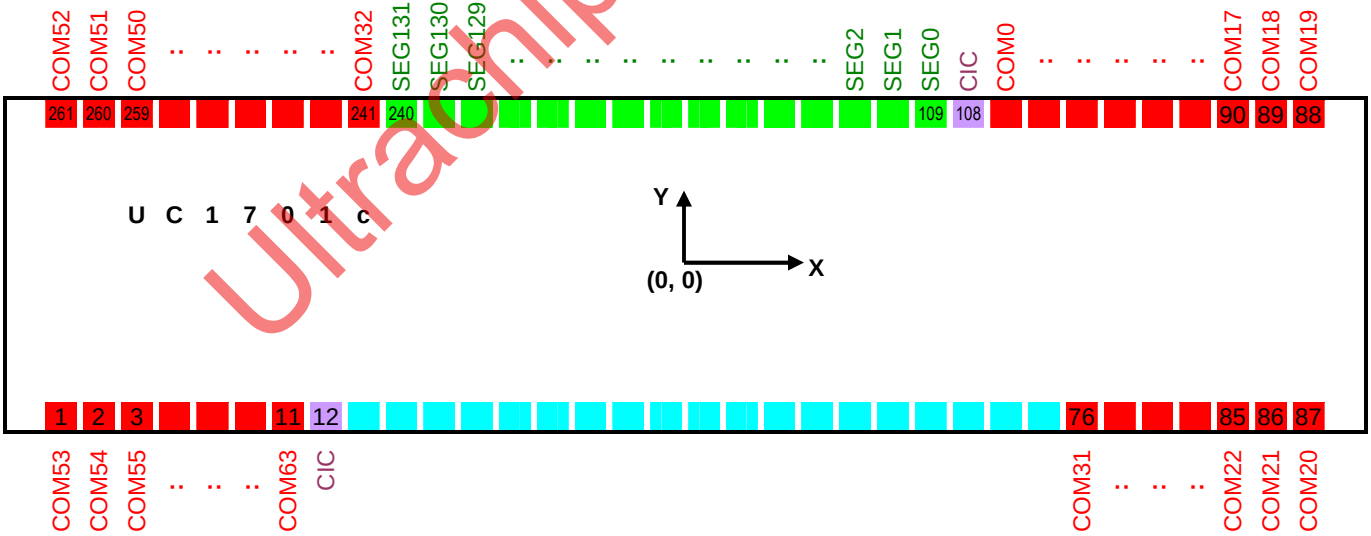
#	Pad	X	Y	W	H
59	DUMMY	985	-274.5	45	45
60	DUMMY	1040	-274.5	45	45
61	DUMMY	1095	-274.5	45	45
62	DUMMY	1150	-274.5	45	45
63	DUMMY	1205	-274.5	45	45
64	TST5	1260	-274.5	45	45
65	TST2	1320	-274.5	50	45
66	VSSX	1385	-274.5	50	45
67	VDDX	1450	-274.5	50	45
68	BM0	1515	-274.5	50	45
69	BM1	1580	-274.5	50	45
70	DT1	1645	-274.5	50	45
71	VSSX	1710	-274.5	50	45
72	DT2	1775	-274.5	50	45
73	VDD	1840	-274.5	50	45
74	VDD2	1905	-274.5	50	45
75	VDD3	1970	-274.5	50	45
76	COM<31>	2066	-247	15	100
77	COM<30>	2093	-247	15	100
78	COM<29>	2120	-247	15	100
79	COM<28>	2147	-247	15	100
80	COM<27>	2174	-247	15	100
81	COM<26>	2201	-247	15	100
82	COM<25>	2228	-247	15	100
83	COM<24>	2255	-247	15	100
84	COM<23>	2282	-247	15	100
85	COM<22>	2309	-247	15	100
86	COM<21>	2336	-247	15	100
87	COM<20>	2363	-247	15	100
88	COM<19>	2363	247	15	100
89	COM<18>	2336	247	15	100
90	COM<17>	2309	247	15	100
91	COM<16>	2282	247	15	100
92	COM<15>	2255	247	15	100
93	COM<14>	2228	247	15	100
94	COM<13>	2201	247	15	100
95	COM<12>	2174	247	15	100
96	COM<11>	2147	247	15	100
97	COM<10>	2120	247	15	100
98	COM<9>	2093	247	15	100
99	COM<8>	2066	247	15	100
100	COM<7>	2039	247	15	100
101	COM<6>	2012	247	15	100
102	COM<5>	1985	247	15	100
103	COM<4>	1958	247	15	100
104	COM<3>	1931	247	15	100
105	COM<2>	1904	247	15	100
106	COM<1>	1877	247	15	100
107	COM<0>	1850	247	15	100
108	CIC	1823	247	15	100
109	SEG<0>	1768.5	247	15	100
110	SEG<1>	1741.5	247	15	100
111	SEG<2>	1714.5	247	15	100
112	SEG<3>	1687.5	247	15	100
113	SEG<4>	1660.5	247	15	100
114	SEG<5>	1633.5	247	15	100
115	SEG<6>	1606.5	247	15	100
116	SEG<7>	1579.5	247	15	100

#	Pad	X	Y	W	H
117	SEG<8>	1552.5	247	15	100
118	SEG<9>	1525.5	247	15	100
119	SEG<10>	1498.5	247	15	100
120	SEG<11>	1471.5	247	15	100
121	SEG<12>	1444.5	247	15	100
122	SEG<13>	1417.5	247	15	100
123	SEG<14>	1390.5	247	15	100
124	SEG<15>	1363.5	247	15	100
125	SEG<16>	1336.5	247	15	100
126	SEG<17>	1309.5	247	15	100
127	SEG<18>	1282.5	247	15	100
128	SEG<19>	1255.5	247	15	100
129	SEG<20>	1228.5	247	15	100
130	SEG<21>	1201.5	247	15	100
131	SEG<22>	1174.5	247	15	100
132	SEG<23>	1147.5	247	15	100
133	SEG<24>	1120.5	247	15	100
134	SEG<25>	1093.5	247	15	100
135	SEG<26>	1066.5	247	15	100
136	SEG<27>	1039.5	247	15	100
137	SEG<28>	1012.5	247	15	100
138	SEG<29>	985.5	247	15	100
139	SEG<30>	958.5	247	15	100
140	SEG<31>	931.5	247	15	100
141	SEG<32>	904.5	247	15	100
142	SEG<33>	877.5	247	15	100
143	SEG<34>	850.5	247	15	100
144	SEG<35>	823.5	247	15	100
145	SEG<36>	796.5	247	15	100
146	SEG<37>	769.5	247	15	100
147	SEG<38>	742.5	247	15	100
148	SEG<39>	715.5	247	15	100
149	SEG<40>	688.5	247	15	100
150	SEG<41>	661.5	247	15	100
151	SEG<42>	634.5	247	15	100
152	SEG<43>	607.5	247	15	100
153	SEG<44>	580.5	247	15	100
154	SEG<45>	553.5	247	15	100
155	SEG<46>	526.5	247	15	100
156	SEG<47>	499.5	247	15	100
157	SEG<48>	472.5	247	15	100
158	SEG<49>	445.5	247	15	100
159	SEG<50>	418.5	247	15	100
160	SEG<51>	391.5	247	15	100
161	SEG<52>	364.5	247	15	100
162	SEG<53>	337.5	247	15	100
163	SEG<54>	310.5	247	15	100
164	SEG<55>	283.5	247	15	100
165	SEG<56>	256.5	247	15	100
166	SEG<57>	229.5	247	15	100
167	SEG<58>	202.5	247	15	100
168	SEG<59>	175.5	247	15	100
169	SEG<60>	148.5	247	15	100
170	SEG<61>	121.5	247	15	100
171	SEG<62>	94.5	247	15	100
172	SEG<63>	67.5	247	15	100
173	SEG<64>	40.5	247	15	100
174	SEG<65>	13.5	247	15	100
175	SEG<66>	-13.5	247	15	100
176	SEG<67>	-40.5	247	15	100

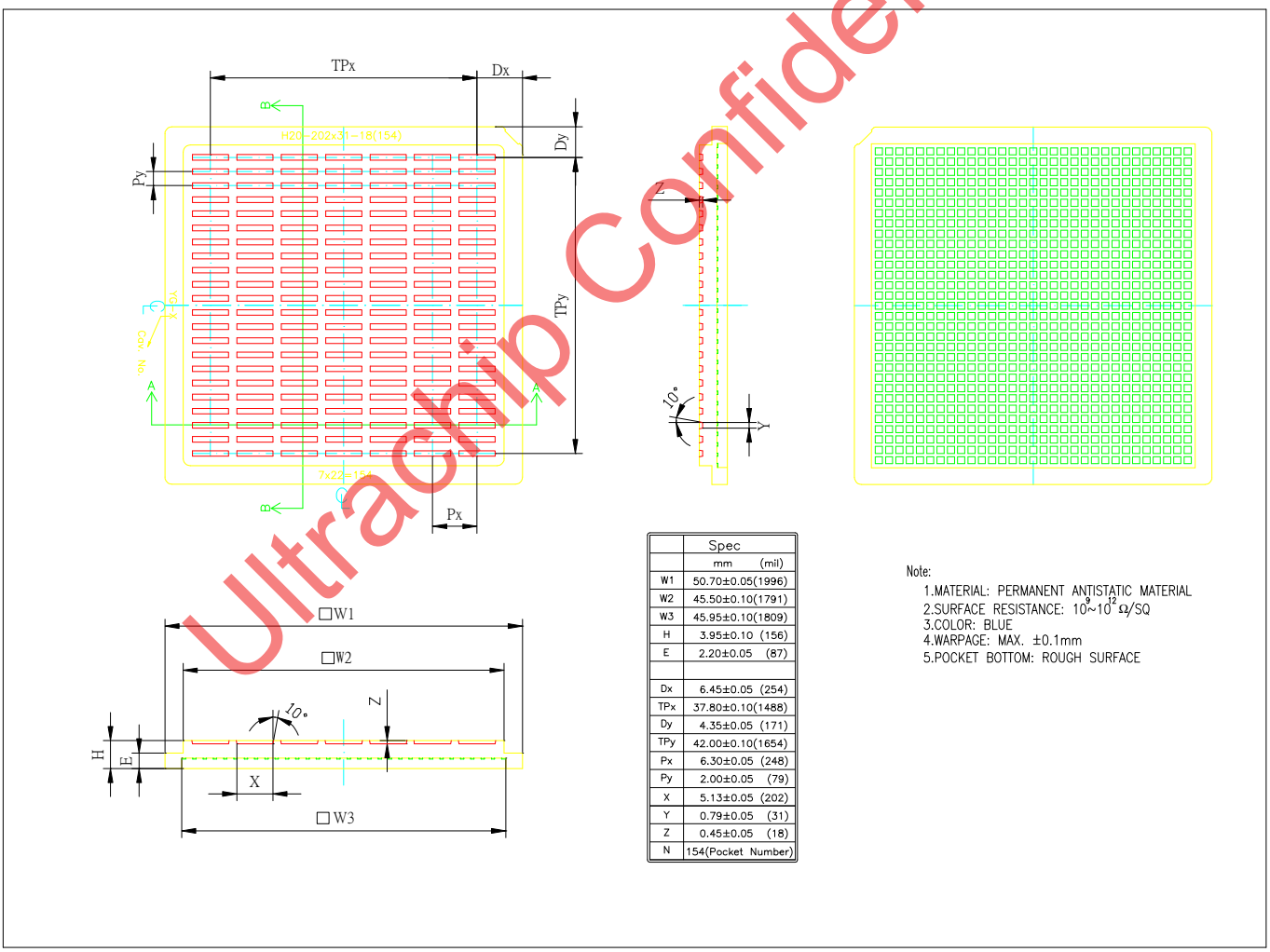
#	Pad	X	Y	W	H
177	SEG<68>	-67.5	247	15	100
178	SEG<69>	-94.5	247	15	100
179	SEG<70>	-121.5	247	15	100
180	SEG<71>	-148.5	247	15	100
181	SEG<72>	-175.5	247	15	100
182	SEG<73>	-202.5	247	15	100
183	SEG<74>	-229.5	247	15	100
184	SEG<75>	-256.5	247	15	100
185	SEG<76>	-283.5	247	15	100
186	SEG<77>	-310.5	247	15	100
187	SEG<78>	-337.5	247	15	100
188	SEG<79>	-364.5	247	15	100
189	SEG<80>	-391.5	247	15	100
190	SEG<81>	-418.5	247	15	100
191	SEG<82>	-445.5	247	15	100
192	SEG<83>	-472.5	247	15	100
193	SEG<84>	-499.5	247	15	100
194	SEG<85>	-526.5	247	15	100
195	SEG<86>	-553.5	247	15	100
196	SEG<87>	-580.5	247	15	100
197	SEG<88>	-607.5	247	15	100
198	SEG<89>	-634.5	247	15	100
199	SEG<90>	-661.5	247	15	100
200	SEG<91>	-688.5	247	15	100
201	SEG<92>	-715.5	247	15	100
202	SEG<93>	-742.5	247	15	100
203	SEG<94>	-769.5	247	15	100
204	SEG<95>	-796.5	247	15	100
205	SEG<96>	-823.5	247	15	100
206	SEG<97>	-850.5	247	15	100
207	SEG<98>	-877.5	247	15	100
208	SEG<99>	-904.5	247	15	100
209	SEG<100>	-931.5	247	15	100
210	SEG<101>	-958.5	247	15	100
211	SEG<102>	-985.5	247	15	100
212	SEG<103>	-1012.5	247	15	100
213	SEG<104>	-1039.5	247	15	100
214	SEG<105>	-1066.5	247	15	100
215	SEG<106>	-1093.5	247	15	100
216	SEG<107>	-1120.5	247	15	100
217	SEG<108>	-1147.5	247	15	100
218	SEG<109>	-1174.5	247	15	100
219	SEG<110>	-1201.5	247	15	100
220	SEG<111>	-1228.5	247	15	100
221	SEG<112>	-1255.5	247	15	100
222	SEG<113>	-1282.5	247	15	100
223	SEG<114>	-1309.5	247	15	100
224	SEG<115>	-1336.5	247	15	100
225	SEG<116>	-1363.5	247	15	100
226	SEG<117>	-1390.5	247	15	100
227	SEG<118>	-1417.5	247	15	100
228	SEG<119>	-1444.5	247	15	100
229	SEG<120>	-1471.5	247	15	100
230	SEG<121>	-1498.5	247	15	100
231	SEG<122>	-1525.5	247	15	100
232	SEG<123>	-1552.5	247	15	100
233	SEG<124>	-1579.5	247	15	100
234	SEG<125>	-1606.5	247	15	100
235	SEG<126>	-1633.5	247	15	100
236	SEG<127>	-1660.5	247	15	100

#	Pad	X	Y	W	H
237	SEG<128>	-1687.5	247	15	100
238	SEG<129>	-1714.5	247	15	100
239	SEG<130>	-1741.5	247	15	100
240	SEG<131>	-1768.5	247	15	100
241	COM<32>	-1823	247	15	100
242	COM<33>	-1850	247	15	100
243	COM<34>	-1877	247	15	100
244	COM<35>	-1904	247	15	100
245	COM<36>	-1931	247	15	100
246	COM<37>	-1958	247	15	100
247	COM<38>	-1985	247	15	100
248	COM<39>	-2012	247	15	100
249	COM<40>	-2039	247	15	100

#	Pad	X	Y	W	H
250	COM<41>	-2066	247	15	100
251	COM<42>	-2093	247	15	100
252	COM<43>	-2120	247	15	100
253	COM<44>	-2147	247	15	100
254	COM<45>	-2174	247	15	100
255	COM<46>	-2201	247	15	100
256	COM<47>	-2228	247	15	100
257	COM<48>	-2255	247	15	100
258	COM<49>	-2282	247	15	100
259	COM<50>	-2309	247	15	100
260	COM<51>	-2336	247	15	100
261	COM<52>	-2363	247	15	100



TRAY INFORMATION



	Spec
	mm (mil)
W1	50.70±0.05(1996)
W2	45.50±0.10(1791)
W3	45.95±0.10(1809)
H	3.95±0.10 (156)
E	2.20±0.05 (87)
Dx	6.45±0.05 (254)
TPx	37.80±0.10(1488)
Dy	4.35±0.05 (171)
TPy	42.00±0.10(1654)
Px	6.30±0.05 (248)
Py	2.00±0.05 (79)
X	5.13±0.05 (202)
Y	0.79±0.05 (31)
Z	0.45±0.05 (18)
N	154(Pocket Number)

Note:
1.MATERIAL: PERMANENT ANTISTATIC MATERIAL
2.SURFACE RESISTANCE: 10^{9}~10^{12} Ω/SQ
3.COLOR: BLUE
4.WARPAGE: MAX. ±0.1mm
5.POCKET BOTTOM: ROUGH SURFACE

REVISION HISTORY

Revision	Contents	Date
0.6	First Release	Jun. 17, 2014
1.0	Average Frame Rate (Min.): –10% → –15% Average Frame Rate (Max.): +10% → +20%	Sep. 29, 2014
	Power Consumption data are provided.	