第四次实验报告

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一、 实现 CSR 寄存器

1. CSR 的整体架构参考了老师给出的代码和 regfile 的相关操作
2. CSR 的功能主要我分成了四块，第一是检测异常，第二是检测中断，第三是检测指令中的 CSR 指令并对之进行处理，第四就是对 MRET 的处理
3. 对于 CSR 指令的读操作，几乎和 regfile 完全一致，直接使用组合逻辑读出即可，对于写操作，我为了保证 ALU 模块可以正常的计算需要写入 rd 的值，我将对于 CSR 中写入值的计算直接写在了 CSR 寄存器模块内。先计算结果，然后也是类似于 regfile 写指令的操作更改 CSR 的对应值
4. 使用组合逻辑对上述的四种情况按顺序一一进行考虑(其实这四种情况是互斥的，不会出现一条指令兼具几种情况的问题)，这里对于 CSR 寄存器的修改完全参照文档即可。

二、 对于流水线的修改

1. 对于 CSR 类型指令的处理：在 decoder 中加入对于 CSR、MRET、ECALL 指令的识别。在 decode 阶段通过向外传递 csrra，通过 csrrd 读取 CSR 对应的值，并通过 immediate 模块对 dataD 的 srca 和 srcb 进行布局，方便后续的处理。将 x[rs1]或 zmm[4:0]存储在 dataD.csr 中，CSR 的对应值会在后续的 ALU 运算中自动被存入 result 中不必担心。ECALL 和 MRET 指令对流水线不需要太多的改动，只需要识别即可。由于 CSR 指令或者是任何会改变 CSR 寄存器的操作都会导致整个流水线的刷新，所以其实我们不必考虑 CSR 寄存器的数据冲突问题，因为就算冲突了，后面出现的指令也会被刷新不会被执行。
2. 识别异常：在 FETCH 阶段可能导致的异常是 pc[1:0]!=2’b00 将 dataF.error=FETCHERROR，同时将 ireq.valid 和 stopf 等进行相应的修改，后续的异常还有在 decode 阶段未找到相应指令的解析方式，在 memery 阶段根据所取数据的 msize 发现地址未对齐。对这些异常指令的处理方式类似于 FETCH 阶段的处理，当发现你获得的 data 中已经是一条错误指令，将他看做费指令不予理会即可。
3. 流水线的刷新：由于 cbus 的合理性要求，dreq 和 ireq 不能在中途改变。因此在处理异常的时候我分成三个步骤进行处理。当出现异常但是 stopm 为 1 的时候，给出一个 stallcsr 信号说明这时候 memory 阶段的 dreq 还在取指令不能变化，所以所有的寄存器保持原样不变，除了 memery 阶段这是 stopm 自己就可以完成的，只需要对 memery 阶段做一个 store 的操作即可所以不需要额外操作。当 stopm 为 1 的时候，将 decode 和 execute 的指令 flush，但是 ireq 的情况还未知，继续让他取指令，memory 中由于 execute 的指令被刷新，dreq 不再工作，但是 dataM 还要保持不变以维持 csr 的信息来源。指导 stopf 也为 0 表示所有的流水线的取内存操作全部完成，这时候将所有流水线寄存器全部刷新即可。这时我再对 csr 寄存器进行一些列操作，同时按照要求取出新的 PC，在 fetch 阶段更新 pc_next 即可。同时为了防止在处理异常的时候传入的一条访存指令更改内存，需要保证 dreq 的 valid 只能在没有异常或中断的时候才会有效。

三、 通过截图

1. Test-lab4 TEST=all 通过截图

```
TEST=all ./build/emu --no-diff -i ./ready-to-run/lab4/all-test-priv.bin --dump-wave || true
Emu compiled at Jun 11 2022, 08:51:40
The image is ./ready-to-run/lab4/all-test-priv.bin
Using simulated 256MB RAM
dump wave 0-999999 to /mnt/c/Users/Administrator/Desktop/2022Spring_final/Arch-2022Spring-FDU/build/1654908704.fst...
Single test passed.
Run paint
Aptenodytes patagonicus
Picture generated.
Compressed size=2140
Done! Result:

QAppeDAMu8qQDO4c4A9ebTAAYAAmsQuwjMAmIEIgJhIxECYBcAAAAGAAJrErsGzAJiBCICYSIRAmYYAAAABgACaxO7BcwCYgQiAmEiEQJgGAAAAAYAAmoHqg67A8wCZgQiAmEiEQJgGAAAAAYAAmoLqgu7A8
wCYgMiAmEhEQJgGQAAAAYAAmoNqgq7AswCYgMiAmEhEQJgGQAAAAYAAmoPqgm7AsYFIgJhHxECYBoAAAAHAAJqD6oJuwLGBCICYR8RAmAaAAAABwACahGqCLsCYgMiAmEeEQJmGwAAAAcAAmkGmQyqB7sCYg
MiAmEeEQJgGwAAAAcAAmkJmQqqB7sCYgMiAmEdEQJgGwAAAAcAAmkLmQmqBrsCYgMiAmEcEQJgHAAAAAcAAmkNmQiqBrsCYgMiAmYcEQJgHAAAAAcAAmkOmQiqBrsCYgMiAmEaEQJmHQAAAAcAAmkOmQiqBr
sCYgIiAmYaEQJgHQAAAAcAAmgGiAmZB6oGuwJiAyICYRgRAmAeAAAABwACaAiICJkHqga7AmIDIgJhFxECYB4AAAAHAAJoCYgImQaqBrsCxgMiAmEWEQJmHwAAAAcAAmgKiAeZB6oGuwJiAyICYRURAmAfAA
AABwACaAuIB5kGqga7AsYEIgJhFBECYB8AAAAIAAJoC4gGmQaqBrsCzAJiAiICZhMRAmAgAAAACAACZwR3B4gGmQaqBrsDzAJiAiICZhIRAmAgAAAACAACZwV3B4gGmQaqBbsEzAJiAiICZhARAmYhAAAACA
ACZwZ3BogGmQaqBrsEzAJiAiICZg8RAmAhAAAACAACZwZ3BogGmQaqBrsFzAJiAyICZg0RAmAhAAAABwACZgd3BogGmQaqBrsFzALWAmICIgJmCxECYCIAAAAHAAJmB3cGiAaZBqoGuwXMA90CZgIiAmYKEQ
JgIgAAAAgAAmcGdwaIBpkGqga7BcwE3QNmAgADZgYRAmAjAAAACAACZwZ3BogGmQaqBrsFzAXdAuYCZgIAA2YEEQJgIwAAAAgAAmcGdwaIBpkGqga7BcwF3QPuA2YDAAVmJAAAAAgAAmYFdweIBpkGqgW7Bs
wF3QXuAvYGZiUAAAAJAAJnA3cHiAaZBqoGuwbMBd0F7gT/BGYlAAAACQACaAqIBpkGqga7BswF3QXuA/8CZgJEAmAkAAAACQACaAmIB5kGqga7BcwG3QXuAvYCZANEAmAkAAAACgACaAeIB5kHqga7BcwG3Q
TuAmYGRAJgJAAAAAoAAmgGiAiZBqoGuwbMBd0E7gJmB0QCYCQAAAAKAAJmBYgImQeqBrsGzAXdAuYCZglEAmAkAAAACwACaAKICZkHqge7BcwG3QJkC0QCYCQAAAALAAJpCpkIqga7BswE3QJmDUQCYCQAAA
AMAAJpCJkIqge7BswC3QJmAjYNRAJgJAAAAAwAAmkHmQiqB7sGzALdAmMCMwJkDEQCYCQAAAAMAAJmBpkJqge7BswCZgQzAmQMRAJgJAAAA0AAmkDmQqqB7sEzANmBjMCZAxEAmAkAAAADQACZgyqB7sEzA
JjCDMCZAxEAmAkAAADgACagqqCLsCzAJmCjMCZAxEAmAkAAADgACZgiqCbsCxgNmCjMCZgtEAmAlAAAADwACagaqCbsCxgJEAmMLMwJkCkQCYCUAAAAQAAJqA6oJuwNmAkQCZgwzAmQKRAJgJQAAABAAAm
YCqwi7AmYERAJmDTMCZApEAmAlAAAAEQACawi7AmYFRAJjDTMCZApEAmAlAAAAEgACawW7AmYGRAJmDjMCZApEAmAlAAAAEgACZgO7AmYIRAJjDjMCZApEAmAlAAAEwACawK2AmQIRAJjDjMCZApEAmAlAA
AAEwADZgpEAmYOMwJmC0QCYCUAAAAUAAJkCkQCYw4zAmQLRAJgJQAAABQAAmYKRANmDDMCZgxEAmAlAAAAFQACZAxEBWYFMwNmDUQCYCUAAAAWAAJkEEQGZg9EAmAlAAAAFwACZCREAmAlAAAAGAACZCNEAm
AlAAAAGAACZiJEAmYmAAAAGQACZiFEA2YlAAAAGgACZiBEA2UlAAAAHAACZB5EA2UCYCMAAAAdAAJmHUQCZQJWAmAiAAAAHgACZhxEAmUCVQJgIgAAACAAAmYbRAJlAlYCYCEAAAAhAANmGUQCZQJVAmAhAA
AAIwADZhdEAmUCVQJmIQAAACUABGYURAJmA1UCYCAAAAAoAAVmEUQCZQJVAmYgAAAALQAHZgtEAmUCVQJgHwAAADMAAmYKRAJmAlUCZh8AAAA0AAJmCkQCZQJVAmYeAAAANQADZghEAmYDVQJgHQAAADcAAm
YIRAJmAlUCZh0AAAA4AANmB0QCZgJVAmAcAAAAOgACZghEA2UCYBsAAAA7AAJmCEQDZhwAAAA8AANmB0QDZhsAAAA+AAJmCEQCZhoAAAA/AAJmCEQCYBkAAABAAANmBkQCZhkAAABCAAJmBkQCYBgAAABDAA
NmBEQCZhgAAABFAAJmBEQCYBcAAABGAAJmA0QCZhcAAABHAANmAkQCYBYAAABJAAJmAkYCYBUAAABKAAVmFQAAAEwAA2YVAAAABwADYAJmAwADYAJmOQADZhQAAAAHAAZgAgAGYDkAAmYUAAAABwADYAJmAg
YCZgIGAmZQAAAABwAOYE8AAAAHAANgAmYGBgJmUAAAAGQAAABkAAAAZAAAAGQAAAAAQ==
Run coremark
Running CoreMark for 10 iterations
2K performance run parameters for coremark.
CoreMark Size    : 666
Total time (ms)  : 852
Iterations       : 10
Compiler version : GCC11.1.0
seedcrc          : 0xe9f5
[0]crclist       : 0xe714
[0]crcmatrix     : 0x1fd7
[0]crcstate      : 0x8e3a
[0]crcfinal      : 0xfcaf
Finised in 852 ms.
```

```
CoreMark Iterations/Sec 11
Run dhrystone
Dhrystone Benchmark, Version C, Version 2.2
Trying 10000 runs through Dhrystone.
Finished in 1437 ms
==================================================
Dhrystone PASS          12 Marks
                vs. 100000 Marks (i7-7700K @ 4.20GHz)
Run stream
-------------------------------------------------------------
STREAM version $Revision: 5.10 $
-------------------------------------------------------------
This system uses 8 bytes per array element.
-------------------------------------------------------------
Array size = 2048 (elements), Offset = 0 (elements)
Memory per array = 0.0 MiB (= 0.0 GiB).
Total memory required = 0.0 MiB (= 0.0 GiB).
Each kernel will be executed 10 times.
 The *best* time for each kernel (excluding the first iteration)
 will be used to compute the reported bandwidth.
-------------------------------------------------------------
* checktick: start=1.491390
* checktick: start=1.492970
* checktick: start=1.494363
* checktick: start=1.495840
* checktick: start=1.497211
* checktick: start=1.498599
* checktick: start=1.499975
* checktick: start=1.501402
* checktick: start=1.502971
* checktick: start=1.504442
* checktick: start=1.505750
* checktick: start=1.507207
* checktick: start=1.508613
* checktick: start=1.510050
* checktick: start=1.511538
* checktick: start=1.512964
* checktick: start=1.514389
* checktick: start=1.515837
* checktick: start=1.517288
* checktick: start=1.518638
Your clock granularity/precision appears to be 99 microseconds.
Each test below will take on the order of 18485 microseconds.
   (= 186 clock ticks)
Increase the size of the arrays if this shows that
```

```
WARNING -- The above is only a rough guideline.
For best results, please be sure you know the
precision of your system timer.
-------------------------------------------------------------
Function    Best Rate MB/s  Avg time     Min time     Max time
Copy:               8.3     0.004078     0.003953     0.004203
Scale:              0.5     0.062579     0.062403     0.062871
Add:                0.8     0.062189     0.061003     0.064027
Triad:              0.3     0.145032     0.143751     0.147013
-------------------------------------------------------------
Solution Validates: avg error less than 1.000000e-13 on all three arrays
-------------------------------------------------------------
Run conwaygame
Play Conway's life game for 200 rounds.
seed=4786


                        *     **
                        *     **
                        *

                    ***   ***

 **
 **
Run sys-test
trap here, epc 8000600c, cause 8
Test ecall_u [OK]
trap here, epc 8000608c, cause 8
trap here, epc 8000602e, cause 0
Test instr_misalign [OK]
trap here, epc 8000608c, cause 8
trap here, epc 80006040, cause 4
Test load_misalign [OK]
trap here, epc 8000608c, cause 8
trap here, epc 80006050, cause 6
Test store_misalign [OK]
trap here, epc 8000608c, cause 8
trap here, epc 800060b0, cause 8000000000000007
Test timer_intr [OK]
trap here, epc 8000608c, cause 8
trap here, epc 80006090, cause 8000000000000003
Test software_intr [OK]
trap here, epc 8000607c, cause 8
Timer interrupt in test_trap, this should happen 50 times.
```

```
Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
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Timer interrupt in test_trap, this should happen 50 times.
Timer interrupt in test_trap, this should happen 50 times.
Test m_trap [OK]
Privileged test finished.
Exit with code = 0
^CCore 0: SOME SIGNAL STOPS THE PROGRAM at pc = 0x0
total guest instructions = 0
instrCnt = 0, cycleCnt = 0, IPC = -nan
Seed=0 Guest cycle spent: 478734528 (this will be different from cycleCnt if emu loads a snapshot)
Host time spent: 1094357ms
This emulator compiled with JTAG Remote Bitbang client. To enable, use +jtag_rbb_enable=1.
Listening on port 23334
make: *** [Makefile:60: test-lab4] Interrupt
```