Flexim Simulator User Guide

(Pre-release, Work-in-Progress)

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Part I. Introduction

1 About Flexim

Flexim is an open-source, modular and highly configurable architectural simulator for evaluating emerging multicore processors. It can run statically compiled MIPS32 Little-Endian (LE) programs.

For the latest Flexim code, please visit the project's website on Github: http://github.com/mcai/flexim.

2 Key Features

1. Architectural
   - Simulation of a classic five-stage superscalar pipeline with out-of-order execution.
   - Multi-level memory hierarchy with the directory-based MESI cache coherence protocol.
   - Support for Syscall-emulation mode simulation (i.e., application only, no need to boot an OS).
   - Correct execution of several state-of-the-art benchmark suites, e.g., wcet_bench, Olden and CPU2006.
2. Non-architectural
   - Developed from scratch in the object-oriented system programming language D 2.0. Great efforts are made to advocate software engineering practices in the simulator construction.
   - A powerful infrastructure that provides common functionalities such as eventing, logging and XML I/O.
   - Pervasive use of XML-based I/O for architectural, workload and experiment configurations and statistics.
   - Easy to use. No scripting. Only required are a statically compiled simulator executable and a few XML files.

3 System Requirements

1. Make sure that you have a Ubuntu 10.04 Linux machine. Other popular Linux distributions may work as well if you are lucky enough.
2. Make sure that you have the latest DMD 2.0 compiler installed. If not, go to this page and download "dmd D 2.0 compiler 1-click install for Ubuntu": http://www.digitalmars.com/d/download.html.

4 How to Build and Run Flexim

1. Unpack the zip or tar file containing the Flexim source.
2. In the main directory of the distribution, you can
   - build Flexim using the command: '`make`';
   - remove all the built files using the command: '`make clean`'.

   By default, the flexim binary is placed in the bin/ folder.
3. Download and unpack cross-compiler-mipsel.tar.bz2 from http://github.com/mcai/flexim/downloads/. Use it to compile MIPS32 LE programs to be simulated by Flexim.
4. In the subdirectory build/, you can start simulation with the default simulation configuration using the command: "`./flexim`" or "`./flexim --experiment=<experiment-name>`". Benchmarks and experiments are specified in the subdirectory configs/benchmarks/ and configs/experiments/, respectively.
5. You can find configuration and statistics files in the configs/ and stats/ subdirectories, respectively. Some sample XML files are provided for your reference.
6. Useful tip: As with all other open source projects, you can learn more by digging into the Flexim source code.

5 Contact Information

If you have any questions, please feel free to contact: Min Cai <itecgo@163.com>.

Part II. Design Documentation

6 Overview

The whole development of the Flexim simulator encompasses three main categories of functionalities: functional simulation, performance simulation and supporting infrastructure.

7 Development Progress

Main Category	Current Progress	
Functional Simulation	Int. Inst. Decoding & Execution	OK for wcet-bench, mst, em3d, etc.
	Fp. Inst. Decoding & Execution	OK for wcet-bench, mst, em3d, etc.
	System Call Emulation	OK for wcet-bench, mst, em3d, etc.
	MIPS LE ELF Exe. Loader	Can run statically compiled programs
Performance Simulation	Five-stage OoO pipelining	RUU-based; to be written
	Set-associative cache structure	OK
	Cache coherence	Being rewritten; in good progress
	On-chip interconnect	Planned
	Interface to external DRAM simulators	To be planned
Supporting Infrastructure	Eventing and callback mechanisms	OK, pervasive use in existing code
	Categorized logging mechanism	OK, limited use in existing code
	XML-based I/O for configs and stats	OK
	Plotting and table generation for experiments	Planned

8 Functional Simulation

8.1 Instruction Decoding and Execution

In Flexim, there are two kinds of instructions, i.e., static instructions and dynamic instructions.

8.1.1 Basic Instructions

1. syscall.

```
thread.syscall(thread.intRegs[2]);
```

2. sll.

```
thread.intRegs[this[RD]] = thread.intRegs[this[RT]] << this[SA];
```

3. sllv.

```
thread.intRegs[this[RD]] = thread.intRegs[this[RT]] << bits(thread.intRegs[this[RS]], 4, 0);
```

4. sra.

```
thread.intRegs[this[RD]] = cast(int) thread.intRegs[this[RT]] >> this[SA];
```

5. srav.

```
thread.intRegs[this[RD]] = cast(int) thread.intRegs[this[RT]]
                                  >> bits(thread.intRegs[this[RS]], 4, 0);
```

6. srl.

```
thread.intRegs[this[RD]] = cast(uint) thread.intRegs[this[RT]] >> this[SA];
```

7. srlv.

```
thread.intRegs[this[RD]] = cast(uint) thread.intRegs[this[RT]]
                                >> bits(thread.intRegs[this[RS]], 4, 0);
```

8.1.2 Branching Instructions

1. Common operations found in the implementation of branching operations.
   Displacement calculation:

```
this.displacement = sext(this[OFFSET] << 2, 16);
```

   Branching function:

```
void branch(Thread thread) {
        thread.nnpc = thread.npc + this.displacement;
}
```

2. b.

```
this.branch(thread);
```

3. bal.

```
thread.intRegs[ReturnAddressReg] = thread.nnpc;
this.branch(thread);
```

4. beq.

```
if(cast(int) thread.intRegs[this[RS]] == cast(int) thread.intRegs[this[RT]]) {
        this.branch(thread);
}
```

5. beqz.

```
if(cast(int) thread.intRegs[this[RS]] == 0) {
        this.branch(thread);
}
```

6. bgez.

```
if(cast(int) thread.intRegs[this[RS]] >= 0) {
        this.branch(thread);
}
```

7. bgezal.

```
thread.intRegs[ReturnAddressReg] = thread.nnpc;
if(cast(int) thread.intRegs[this[RS]] >= 0) {
        this.branch(thread);
}
```

8. bgtz.

```
if(cast(int) thread.intRegs[this[RS]] > 0) {
        this.branch(thread);
}
```

9. blez.

```
if(cast(int) thread.intRegs[this[RS]] <= 0) {
        this.branch(thread);
}
```

10. bltz.

```
if(cast(int) thread.intRegs[this[RS]] < 0) {
        this.branch(thread);
}
```

11. bltzal.
12. bne.
13. bnez.
14. bc1f.
15. bc1t.
16. bc1fl.
17. bc1tl.

8.1.3 Jumping Instructions

1. Common operations found in the implementation of jumping operations.
   Abstract definition of target PC calculation:

```
abstract uint targetPc(Thread thread);
```

   Jumping function:

```
void jump(Thread thread, uint addr) {
        thread.nnpc = addr;
}
```

2. j.
3. jal.
4. jalr.
5. jr.

8.1.4 Floating Point Arithmetic Instructions

8.1.5 Integer Arithmetic Instructions

8.1.6 Memory Access Instructions

8.2 System Call Emulation

A few system calls are emulated for the correct execution of the whole wcet_bench benchmark suite, and mst and em3d from the Olden benchmark suite.

8.3 MIPS Little-Endian ELF Executable Loader

9 Performance Simulation

9.1 Five-Stage Out-of-Order Pipelining

A classic five-stage out-of-order issue processor core is modeled after the SimpleScalar implementation. Methods in class OoOThread implementing the pipeline stages are outlined below.

Method Name	Insts Transfer between Queues	Comments
commit()	RUU $\longrightarrow$ <committed>	Retiring insts, EAs $\dashrightarrow$ LSQ
writeback()	EventQ $\dashrightarrow$ ReadyQ	Resolving reg deps
refreshLsq()	LSQ $\longrightarrow$ ReadyQ	Resolving mem deps
issue()	ReadyQ $\longrightarrow$ EventQ	Accessing FUs and data caches
dispatch()	FetchQ $\longrightarrow$ RUU + LSQ + ReadyQ	Resolving reg deps
fetch()	ICache $\longrightarrow$ FetchQ	Fetching and decoding insts

9.2 Set-Associative Cache Structure

9.3 Cache Coherence

9.4 On-Chip Interconnect

9.5 Interface to External DRAM Simulators

10 Supporting Infrastructure

There are various supporting modules aside the aforementioned main components to advocate the reusability of the simulator, in which the ELF program loader component is used to load statically compiled MIPS32 little-endian executable into the simulator, the event queue component is used extensively to event driven the simulator per cycle, and the logging component supports configurable logging functionalities that can facilitate development and even be useful after release.

10.1 Eventing and Callback Mechanisms

10.2 Categorized Logging Mechanism

10.3 XML-Based Input/Output for Configurations and Statistics

10.4 Plotting and Table Generation for Experiments

Part III. Evaluation and Comparisons to Other Simulators

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12.1 Results