Flexim Integrated Simulation Environment (ISE)

File Edit View Tools Help

Architectures

L1L1 L2

Processor Cores

Simple CPU OoO CPU

Caches

L1I Cache L1D Cache L2 Cache

Interconnects

Fixed P2P

Main Memories

Fixed DRAM

Simulated Architecture

Component	Specification
core#0	ooOProcessorCore0
core#1	ooOProcessorCore1
l2	l2Cache5
interconnect	fixedLatencyP2PInterconnec
mainMemory	fixedLatencyDRAM7

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