Flexim: Facilitating User-Friendly Cycle-Accurate Simulation of Multicore Processors

Min Cai, Zhimin Gu

Beijing Institute of Technology, Beijing 100081, P.R.China

Abstract

Good cycle-accurate simulators are critical for conducting successful multicore processor architecture research nowadays. However, most of the existing simulators are written in C or C++ for speed considerations and the modeled computer structures and functionalities are too complicated to be implemented in a clear yet efficient way. The resulting unreadable code makes the simulator hard to use and extend. As a niche market, other not-so-realistic simulators are mostly used for educational and visualization purposes that they are written in traditional object-oriented languages such as Java or C#, which omit many machine details that are necessary for architectural study. There is a permanent need of balancing speed and elegance while simulating multicore architectures.

In this paper, we present Flexim, a user-friendly cycle-accurate multicore architectural simulator, which consists of the simulator core and the GUI based Integrated Simulation Environment (ISE) . Within the core, Flexim remodels the core functionalities of the classic SimpleScalar simulator and extends it to enable configurable timing simulation of out-of-order cores and multi-level cache hierarchies of multicore processors. It exploits interface-based hierarchical modularity and cycle-accurate callback-based eventing to improve the modularity and extensibility of the simulator core. For the GUI-based ISE, Flexim uses XML files and setup wizards to ease the configuration of the simulator, and utilizes graph visualization to provide static and dynamic views of the multicore architecture under simulation. Simulations of a few popular benchmark suites such as Olden and CPU2006 are shown for illustrative purposes.

Keywords: Cycle-accurate simulator, multicore processor architecture, integrated simulation environment