MF105 – Multiple Resonance Filter (MuRF)

Performance Specification
March 10, 2004 Version

GENERAL

The MF105 Multiple Resonance Filter is an analog audio signal processor with one audio input and two audio outs. It includes a microprocessor section to read the panel controls and switches, read the pedal/control jacks, generate patterns, produce control signals for the analog circuitry, and drive the indicator LEDs.

The audio signal chain consists of the following sections:

- An input amplifier,
- Eight resonant filters, each of which is followed by a dedicated VCA,
- A VCA for the direct, unfiltered signal,
- Two output amplifiers, and
- The usual on/bypass switching.

The outputs of filters 1, 3, 5, and 7 go to the LEFT/MONO audio output, while the outputs of filters 2, 4, 6 and 8 go to the RIGHT audio output.

Each of the filter VCAs has a separate control input to which an envelope control voltage is applied. In addition, all of the filter VCAs have a common control input for setting the overall gain. The direct VCA has a separate control input for controlling its overall gain.

All of the filters have a common control input for shifting their resonant frequencies. This control signal is a high frequency rectangular wave, the duty cycle of which determines the amount of frequency shift.

Analog control signal generation and processing consists of the following functions:

- A high frequency oscillator, a variable-threshold comparator, and a driver, for generating the frequency shifting control signal,
- A level-shifting amplifier for the filter overall gain control signal,
- A level-shifting amplifier for the direct overall gain control signal, and
- A voltage-to-current converter for controlling the gain of the audio input amplifier

The panel controls and switches, control and timing signal jacks, the stomp switch, and the peak voltage are scanned by a C8051F005 microprocessor. The microprocessor and the associated digital circuitry generate the following signals in response to the settings of the panel controls and the signals applied to the jacks:

- A separate envelope control voltage for each of the filter VCAs,
- Control voltage for the filter VCA overall gain,
- Control voltage for the direct overall gain,
- Control voltage for the gain of the audio input amplifier,
- Control voltage for determining the duty cycle of the frequency shift control signal,
- Switch signal for the on/bypass function, and
- Switch signals for the OVERLOAD, PATTERN RATE, and ON/BYPASS indicator LEDs.

The eight envelopes are produced sequentially, in a pattern that is determined by the PATTERN selector switch, and at a rate that is determined by the RATE rotary control.

The ENVELOPE rotary control changes the times of the envelope segments. All eight envelopes are the same shape.

The MIX rotary control determines the relative amounts of filtered and direct audio signals that appear at the outputs.

The DRIVE rotary control determines the gain of the input amplifier.

The OUTPUT rotary control changes the gains of both the filter VCAs and the direct VCA.

The function of the two-position panel switch currently labeled BANK has not yet been fully determined. It will probably be used to enable/defeat the LFO component of the frequency shift control signal.

The control and timing jacks perform the following functions:

The RATE, ENVELOPE, and MIX jack signals perform the same function as the RATE, ENVELOPE, and MIX panel controls.

The LFO jack signal changes the rate of the microprocessor-generated sine wave that is used for the frequency shift function.

The SWEEP jack signal is combined with the microprocessor-generated sine wave in a manner that will be described below.

The TAP jack, when used, disables the microprocessor-generated pattern rate. In its place, it substitutes the time between the last two transitions to LO at the TAP jack input.

The circuitry of the MF105 MuRF is on three circuit boards. They are called the ANALOG BOARD, the DIGITAL BOARD, and the JACK BOARD. The analog board contains the entire audio chain and nearly all of the analog control processing. The digital board contains the microprocessor, the associated digital circuitry, and most of the A/D input circuitry and D/A output circuitry. The digital board also holds all of the panel components except for the stomp switch. The jack board holds all the jacks, plus a few resistors. The analog and digital boards are interconnected via two dual row thru-board headers, one of which also connects via a short ribbon cable to the jack board. The digital board also contains headers for the stomp switch and for the JTAG programming connection. The circuitry on the analog board and the digital board is surface mounted, and all the jacks, panel components, and connectors are thru-hole mounted. The analog and digital boards are four-layer, while the jack board is two-layer.

The circuitry on each of the board will now be described in detail.

ANALOG BOARD CIRCUITRY

The following circuit description refers to the MURF ANALOG schematic diagram dated December 23, 2003. This schematic is current as of today, but will undergo minor tweaks and changes from now through February 16.

SHEET 1

AUDIO_IN is the audio signal at the AUDIO IN jack. The input network C5-R5-R6-C4 provides DC isolation, radio frequency filtering, and protection of input amplifier U3A. The output of U3A is the signal AUDIO, which is the amplified audio input signal

Negative feedback around U3A goes through U2. U2 is a VCA whose gain is controlled by the current through R11 and Q1. U3B is a sample-and-hold buffer, the output of which determines the voltage across R11.

U9A is a 70 kHz oscillator. The triangular waveform across C17 is applied to comparator U12A. The output of U12A is a 70kHz rectangular wave with a peak-to-peak voltage of about 15 volts. This signal is fed through R31 to the inputs of U9B – U9F. The output of U9B – U9F is a fast-switching 70 kHz waveform with a peak-to-peak voltage of 10 volts. This is the SHIFT control signal that is applied to all of the filters, and which changes the filters' resonant frequencies by about +/- 15% (Sheets 2 and 3).

U14B is a sample-and-hold buffer/level shifter/amplifier. The output of U14B is applied to the non-inverting input of U12A through R44 and R36. This voltage determines the duty cycle of the SHIFT waveform.

U12B is a sample-and-hold buffer/level shifter/amplifier. Its output is the D-CONTROL signal. It controls the overall gain of the direct VCA (Sheet 4).

U14A is a sample-and-hold buffer-level shifter/amplifier. Its output is the F_CONTROL signal. It controls the overall gain of all filter VCAs (Sheets 2 and 3). Note that the

F_CONTROL signal is a diode drop across Q16. The current through Q16 is determined by the voltage at the output of U14A and by R50. This is a current mirror configuration. There is a transistor in each of the filter VCA circuits that matches the properties of Q16.

U10 is a multiplexer that routes one of the microprocessor D/A outputs to the inputs of U3B, U12B, U14A, and U14B. The signals J1-11 and J1-12 select the output routing, while the signal J1-13 inhibits U10 when it is high.

SHEETS 2 AND 3

Sheets 2 and 3 show all eight filters and filter VCAs. The circuits are identical, except for the sizes of the two capacitors in the filter circuit. I'll describe FILT/VCA_1 in detail. The AUDIO signal is applied to the filter through R48. The actual filter circuit consists of U13A, C27, C35, R47 and R53. The output of the filter is at U13A-1. D8 conducts when the peak voltage at U13A-1 is higher than the RECT voltage. The RECT voltage is held by a capacitor on the digital board, where it is scanned by the microprocessor. The purpose of the RECT voltage is to determine what the highest peak voltage is at the outputs of the filter and the AUDIO signal. This enables the microprocessor to determine the status of the overload LED, and perhaps cut down the gain of the input amplifier to reduce overload distortion.

U15A and U15B switch on and off in response to the SHIFT waveform. When these switches are on, the filter resonant frequency is raised by about 30%, because R63 and R64 are placed in parallel with R47 and R53 respectively. When the switches are off, the filter resonant frequency is not raised. As the duty cycle of the SHIFT signal increases from 0% to 100%, the average resonant frequency increases from 0% to 30%.

The output of the filter is applied through C25 and R39 to the bases of Q7 and Q3. The transconductance of this transistor pair is proportional to the current through them, which is the the same as the current through Q8.

U11A, R33, and Q4 is a voltage-to-current converter. The input J1-1 is the envelope voltage for Filter 1. It goes from 0V to +2.4 volts. The voltage at U11A-1 is such that the current in milliamperes through Q4 is numerically equally to the voltage at J1-1.

The current through Q8 is a fraction of the current through Q4. This fraction is determined by the voltage across R30. If the voltage across R30 is zero, then the current through Q8 is equal to the voltage across Q4. This is very nearly the case when Q11 is shut off. However, when Q11 conducts, there is a voltage drop across R30, and the current through Q8 is reduced to a fraction of the current through Q4. This fraction depends only on F_CONTROL, which, in turn, depends on the voltage at the output of U14A (Sheet 1). This is how a single voltage at the output of U14A determines the overall gains of all filter VCAs, regardless of the status of the envelopes.

The collectors of Q7 and Q3 are bussed to the corresponding outputs of FILT 3, FILT 5, and FILT 7, and go to the summing inputs of the "ODD" output amplifier (Sheet 4).

Similarly, the collector outputs of FILT 2, FILT 4, FILT 6, and FILT 8 are bussed and go to the summing inputs of the "EVEN" amplifier.

Note D14 in the FILT/VCA_4 box. This enables the unfiltered audio (the AUDIO signal) to contribute to the RECT voltage on the digital board. Thus, the RECT voltage, and therefore the overload LED, will respond to the peak voltage of the AUDIO signal or to any of the filter outputs, and will therefore tell the musician if one or more of these signals isclose to clipping.

SHEET 4

The DIRECT VCA is shown in the upper left corner of the sheet. It is actually two VCAs. One VCA is for the "ODD" summing amplifier, while the other VCA is for the "EVEN" summing amplifier. Thus, the direct signal is fed equally to both audio outputs. The amount that is fed is determined by the D_CONTROL signal, which is derived from the settings of the MIX and the OUTPUT panel controls.

U8A and U8B are the two output amplifiers. They are differential amplifiers. Q2 supplies a smoothed voltage of about +7 volts that enable to collectors of the filter VCA's to be connected to the inputs of U8A and U8B.

U6 performs the bypass/on switching functions. The switch signal J1-19 comes from the digital board. The audio feeds to the LEFT/MONO OUT and RIGHT OUT jacks appear at J2-4 and J2-6 respectively. Note that when the MF105 is in bypass, the bypass output appears only at the LEFT/MONO jack.

The power inverter and regulators are shown in the lower right corner. Note that voltage inverters U4 and U5 are going to be replaced with a single higher current device.

DIGITAL BOARD

The following circuit description refers to the MURF DIGITAL schematic diagram dated December 28, 2003. This schematic is current as of today, but may undergo minor tweaks and changes from now through February 16.

The C8051F005 microprocessor has four eight-bit I/O ports, eight 12-bit A/D inputs, two 12-bit D/A outputs, a dedicated JTAG port for programming, and several other inputs and outputs, most of which are not used. The device runs on +3.3 volts. The manufacturer's data book states that all digital inputs and outputs are tolerant to +5V. The data book also states that "weak pullup" of the inputs and outputs can be enabled. In this circuit, input ports do not have external pullup resistors, but some outputs do have pullup resistors that are connected to +5V.

Ports P0 and P1 are inputs ports. SW1 is a 12-position rotary switch that selects the pattern. The switch wiper is connected to ground, and the twelve positions are connected to Port 0.0-7 and Port 1.0-3. Other panel and jack switch inputs are a) the two position slide switch, b) the stomp switch, c) the sleeve-bridging contact on the TAP jack,

and d) the tip contact on the TAP jack. Only the tip contact is protected with diodes to +5V and ground, since it is the only input that is accessible to the outside world.

Ports P2 and P3 are output ports. The hardware is set up for these ports to be open collector. P2.0-5 enables or shorts out the six indicator LEDs (two colors for each of the three LEDs). P2.6 determines the control terminal of U1 (NOTE: THE CURRENT SCHEMATIC IS WRONG. THE CONTROL TERMINALS OF U1 SHOULD BE CONNECTED TO P2.6, NOT P3.7.)

P3.0-3 determines the control and inhibit terminals of U4. P3.4-6 determines the control and inhibit terminals of U10 on the analog board. P3.7 determines the control terminal of U6 on the analog board.

Of the eight ADC inputs (AIN0 to AIN7), AIN0 – AIN2 are taken from the three outputs of U1. The inputs to U1 are the five control input jacks, while the sixth is the signal "E", which is the same signal as RECT on the analog board, but buffered by U5A. Thus, AIN0 – AIN2 convert a total of six analog signals.

AIN3 – AIN7 are connected directly to the five panel rotary potentiometers. There is a +2.4 V reference voltage across all of these pots. This voltage is buffered by U5B.

J4 is the JTAG interface. It is connected to the microprocessor in accordance with the information in the data book.

The DAC output DAC0 is multiplexed to eight sample-and-hold buffers U6A – U9B. The outputs of these buffers are the eight envelopes. Each envelope goes to a slide potentiometer. . The envelope voltage across a slide potentiometer goes from 0V to +2.4V. The wiper of the slide potentiometer goes through the board interconnect to the envelope input of the appropriate filter VCA

DAC1 is the other DAC output. It goes to U10 on the analog board.