



CBMIA User's Guide

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Abstract

This document describes the CBMIA board usage for firmware version 2.00 and older. The CBMIA is a MIL1553 bus controller in PCI form-factor.

| Revision | Date | Author | Comments |
|----------|------------|-----------------|------------------|
| 0.1 | 19.06.2012 | Matthieu CATTIN | Initial revision |

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1 Overview

At CERN MIL1553 is used to control several types of equipments (e.g. power converters). CERN implementation of MIL1553 is based on MIL-STD-1553-B, but is not fully compliant to it. Nevertheless, the encoding, the frames structure and the low level protocol are compliant.

The MIL1553 bus uses a command/response protocol. It is based on Manchester encoded 16-bit words. Each word starts with an additional 3-bit synchronisation pattern and ends with an odd parity bit ¹.

In this document, a command/response couple is called a transaction. There is two types of transactions; "BC to RT" and RT to BC". In any case, the transaction is initiated by the BC. Writing a command word to the TX_REG register will start a transaction. Then a response from a RT is expected. The end of a transaction is detected either when a RT finished sending a frame or upon response timeout. The response timeout t in seconds is set in hardware to:

$$t = \frac{2^{10} - 1}{40e6} = 25.575us$$

Note that according the the MIL-STD-1553 specification, a RT must reply to a BC request within the time period of 4 to 12us. A response time counter starts just after the end of the BC transmission. It will generate an error in case of timeout (no reply from RT). If enabled in the IRQ_EN register, an interrupt request is generated at the end of a transaction.

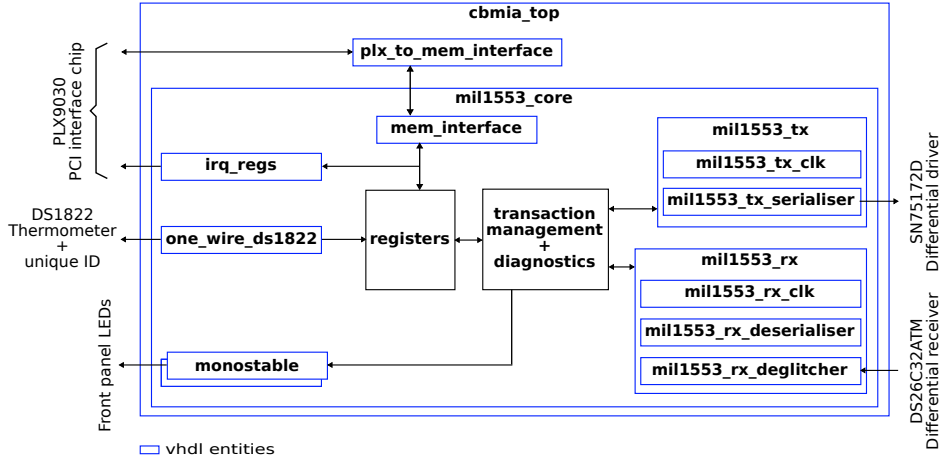


Figure 1: CBMIA firmware architecture, only main entities and blocks are shown.

¹See MIL-STD-1553B specification for further details.

2 Front panel LEDs

| LED nb | Description |
|--------|------------------------------|
| 0 | Tx in progress |
| 1 | Parity error |
| 2 | Rx in progress |
| 3 | Manchester error |
| 4 | Response timeout |
| 5 | Number of word error |
| 6 | PCI bus access |
| 7 | Overwrite error ² |

3 Glossary

BC : Bus Controller, this is a master on a MIL1553 bus.
RT : Remote Terminal, this is a slave on a MIL1553 bus.
Transaction : Command/response couple
Frame : One or more words send by either the BC or the RT.

²Transmission request during a transaction will generate an error.

4 Memory Map

The register width is 32 bits. Addresses in the following table represents an offset from the first address of the PCI window. The addresses are 32-bit words addresses.

Table 1: CBMIA memory map.

| Address | Access | Description |
|---------|--------|---|
| 00 | CR | Interrupt source |
| 01 | RW | Interrupt enable mask |
| 02 | RO | Temperature |
| 03 | RO | Status register |
| 04 | RW | Command register |
| 05 | RW | Reserved |
| 06 | RO | Unique ID (MSBs) |
| 07 | RO | Unique ID (LSBs) |
| 08 | RW | Transmit register |
| 09 | RO | Receive register |
| 10 - 26 | RO | Receive buffer |
| 27 - 42 | RW | Transmit buffer |
| 43 | RO | Transmitted frame counter |
| 44 | RO | Reveived frame counter |
| 45 | RO | Parity error counter |
| 46 | RO | Manchester error counter |
| 47 | RO | Number of word received error counter |
| 48 | RO | Sent request during transaction error counter |
| 49 | RO | Number of word transmitted, expected and received |
| 50 | RO | RT response time |
| 51 | RO | Reception error counter |
| 52 | RO | Response timeout counter |

5 Registers detailed description

5.1 Interrupt source

Name : IRQ_SRC

Offset : 0 (0x0)

Access : CR (Clear on read)

| Fields | Description |
|-------------|--|
| bit [0] | End of transaction IRQ. |
| bit [14:1] | Unused. Ignore on read. |
| bit [15] | Reception error (FSM watchdog). |
| bit [16] | Response timeout (no reply from RT). |
| bit [17] | Number of received word differs from number of expected word (in the frame causing this IRQ). |
| bit [18] | Manchester error (in the frame causing this IRQ). |
| bit [19] | Parity error (in the frame causing this IRQ). |
| bit [20] | T/R flag, 0 = BC-¿RT transaction, 1 = RT-¿BC transaction. |
| bit [26:21] | Word count. If T/R flag = 1, contains the number of word present in the receive buffer, including the status word. |
| bit [31:27] | RT number, 0 = response timeout or truncated/corrupted frame. |

5.2 Interrupt enable mask

Name : IRQ_EN

Offset : 1 (0x1)

Access : WR (Read/write)

| Fields | Description |
|------------|--|
| bit [0] | 0 = Disables end of transaction IRQ, 1 = Enables end of transaction IRQ. |
| bit [31:1] | Unused. Ignore on read, write with 0. |

5.3 Temperature

Name : TEMP

Offset : 2 (0x2)

Access : RO (Read only)

Temperature of the board in degree Celsius. The temperature value is refreshed every second.

| Fields | Description |
|---------------|-------------------------|
| bit [3:0] | Fractional part. |
| bit [10:4] | Integer part. |
| bit [15:11] | Sign. |
| bit [31:16] | Unused. Ignore on read. |

5.4 Status register

Name : STAT

Offset : 3 (0x3)

Access : RO (Read only)

| Fields | Description |
|---------------|--|
| bit [15:0] | BCD encoded HDL version (e.g. 0203 = v2.03). |
| bit [30:16] | Unused. Ignore on read. |
| bit [31] | Transaction flag. 0 = MIL1553 bus is idle, 1 = Transaction in progress on MIL1553 bus. |

5.5 Command register

Name : CMD

Offset : 4 (0x4)

Access : RW (Read/write)

| Fields | Description |
|---------------|---|
| bit [0] | Software reset command. Write 1 to reset (automatically cleared). |
| bit [15:1] | Unused. Ignore on read, write with 0. |
| bit [19:16] | Test point 0 mux (See mux correspondance table). |
| bit [23:20] | Test point 1 mux (See mux correspondance table). |
| bit [27:24] | Test point 2 mux (See mux correspondance table). |
| bit [31:28] | Test point 3 mux (See mux correspondance table). |

5.6 Reserved

Name : RFU

Offset : 5 (0x5)

Access : RO (Read only)

| Fields | Description |
|---------------|---------------------------------------|
| bit [31:0] | Unused. Ignore on read, write with 0. |

5.7 Unique ID (MSBs)

Name : ID_MSB

Offset : 6 (0x6)

Access : RO (Read only)

| Fields | Description |
|------------|---|
| bit [31:0] | Board's unique ID. MSBs of DS1822 64-bit unique ID. |

5.8 Unique ID (LSBs)

Name : ID_LSB

Offset : 7 (0x7)

Access : RO (Read only)

| Fields | Description |
|------------|---|
| bit [31:0] | Board's unique ID. LSBs of DS1822 64-bit unique ID. |

5.9 Transmit register

Name : TX_REG

Offset : 8 (0x8)

Access : RW (Read/write)

| Fields | Description |
|-------------|---------------------------------------|
| bit [4:0] | Word count. |
| bit [9:5] | Sub-module address. |
| bit [10] | T/R. |
| bit [15:11] | RT address. |
| bit [31:16] | Unused. Ignore on read, write with 0. |

Bits [15:0] corresponds to the command word to be sent on the MIL1553 bus. When this register is written, a transaction starts (if no other transaction are in progress). If a transaction is already in progress, the request is ignored.

5.10 Receive register

Name : RX_REG

Offset : 9 (0x9)

Access : RO (Read only)

| Fields | Description |
|-------------|---|
| bit [15:0] | RT status word of the last transaction. |
| bit [31:16] | First received data word of the last transaction (if any, otherwise 0). |

5.11 Receive buffer

Name : RX_BUF

Offset : 10-26 (0xA-0x1A)

Access : RO (Read only)

The receive buffer contains the last frame received from an RT. Every buffer address contains two 16-bit words. The first word is always the RT status, as defined in the MIL1553 protocol. The receive buffer is reset to zero at the beginning of a transaction. In a transaction, it is mandatory for the RT to transmit at least its status. Then in "RT to BC" transactions, the RT can send up to 32 words. The number of word in the receive buffer, including the status word, is stored in the IRQ_SRC register bit[26:21].

| Address | Upper 16-bit word | Lower 16-bit word |
|---------|-------------------|-------------------|
| 10 | Data word 0 | RT status word |
| 11 | Data word 2 | Data word 1 |
| ... | ... | ... |
| 25 | Data word 30 | Data word 29 |
| 26 | 0x0000 | Data word 31 |

5.12 Transmit buffer

Name : TX_BUF

Offset : 27-42 (0x1B-2A)

Access : RW (Read/write)

The transmit buffer contains the frame to be send to the RT. In a "BC to RT" transaction, the BC can send up to 32 words to a RT. The command word (first word in a frame) is taken from the TX_REG register.

| Address | Upper 16-bit word | Lower 16-bit word |
|---------|-------------------|-------------------|
| 27 | Data word 1 | Data word 0 |
| 28 | Data word 3 | Data word 2 |
| ... | ... | ... |
| 41 | Data word 29 | Data word 28 |
| 42 | Data word 31 | Data word 30 |

5.13 Transmitted frame counter

Name : TX_FRAME_CNT

Offset : 43 (0x2B)

Access : RO (Read only)

| Fields | Description |
|------------|--|
| bit [31:0] | Transmitted frame counter. Cleared on reset. |

5.14 Reveived frame counter

Name : RX_FRAME_CNT

Offset : 44 (0x2C)

Access : RO (Read only)

| Fields | Description |
|------------|---|
| bit [31:0] | Received frame counter. Cleared on reset. |

5.15 Parity error counter

Name : PARITY_ERR_CNT

Offset : 45 (0x2D)

Access : RO (Read only)

| Fields | Description |
|------------|--|
| bit [31:0] | Parity error counter. Incermented on parity error in the received frame. Cleared on reset. |

5.16 Manchester error counter

Name : MANCH_ERR_CNT

Offset : 46 (0x2E)

Access : RO (Read only)

| Fields | Description |
|------------|--|
| bit [31:0] | Manchester encoding error. Incermented on Manchester encoding error in the received frame. Cleared on reset. |

5.17 Number of word received error counter

Name : NB_WORD_ERR_CNT

Offset : 47 (0x2F)

Access : RO (Read only)

| Fields | Description |
|------------|---|
| bit [31:0] | Number of word error counter. Incremented when the number of received words is different from the expected number of words. Cleared on reset. |

5.18 Sent request during transaction error counter

Name : TX_ERR_CNT

Offset : 48 (0x30)

Access : RO (Read only)

| Fields | Description |
|------------|---|
| bit [31:0] | Transmission error counter. Incremented when a transmission request (write to TX_REG) arrives during a transaction. Cleared on reset. |

5.19 Number of word transmitted, expected and received

Name : NB_WORD

Offset : 49 (0x31)

Access : RO (Read only)

| Fields | Description |
|-------------|---|
| bit [5:0] | Word count transmitted (for BC- \rightarrow RT and RT- \rightarrow BC). |
| bit [11:6] | Word count received (for RT- \rightarrow BC only). |
| bit [17:12] | Expected number of word (for BC- \rightarrow RT and RT- \rightarrow BC). |
| bit [25:18] | Unused. Ignore on read. |
| bit [26] | Reception error (FSM watchdog). |
| bit [27] | Response timeout (no reply from RT). |
| bit [28] | Number of received word differs from number of expected word (in the frame causing this IRQ). |
| bit [29] | Manchester error (in the frame causing this IRQ). |
| bit [30] | Parity error (in the frame causing this IRQ). |
| bit [31] | T/R flag, 0 = BC- \rightarrow RT transaction, 1 = RT- \rightarrow BC transaction. |

5.20 RT response time

Name : RESP_TIME

Offset : 50 (0x32)

Access : RO (Read only)

Response time t in seconds is calculated as follow:

$$t = \frac{1023 - counter_value}{40e^6}$$

| Fields | Description |
|---------------|--|
| bit [9:0] | Response timeout counter value. Can be used to measure the RT response time. |
| bit [31:10] | Unused. Ignore on read. |

If Response timeout counter value is 1023, it means that a the RT didn't reply and a timeout occurred.

5.21 Reception error counter

Name : RX_ERROR_CNT

Offset : 51 (0x33)

Access : RO (Read only)

| Fields | Description |
|---------------|---|
| bit [31:0] | Reception error counter. Incremented if the bus is idle for more than 3.2us during a frame reception (-i FSM watchdog). Cleared on reset. |

5.22 Response timeout counter

Name : RESP_TIMEOUT_CNT

Offset : 52 (0x34)

Access : RO (Read only)

| Fields | Description |
|---------------|---|
| bit [31:0] | Response timeout counter. Incremented on RT response timeout. Cleared on reset. |