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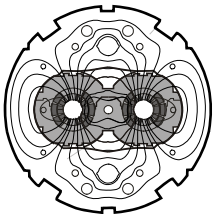

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User Manual

USER MANUAL FOR THE CVORA CARD

Abstract

This note contains the description of the CVORA (new DPRam) card for application programmers and system designers.

This card is a versatile module designed to store three kind of digital values that can be either parallel or serial transmitted data or else previously counted pulses.

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History of Changes

Rev. No.	*Date*	*Pages*	*Description of Changes*
0.1	2007-04-30		Start the draft
0.2	2008-02-04		Modification in abstract and parallel mode description
0.3	2008-02-05		New abstract by Jean Michel Nonglaton
0.4	2008-02-06		Some grammatical correction (thanks Pablo)
0.5	2008-02-08	7	Addition of the programmable analogue outputs descriptions

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Acknowledgments

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1. INTRODUCTION

The CVORA card is a VME module used to replace all the DPRam cards and sampler receiver cards.

The old dual Port Ram card is described in PS/CO/Note 94-49 (Tech.) and the CVORA card keeps all its functionalities.

The Sampler Transceiver card is described in AB/CO/Note 05-04 (Tech.). The CVORA includes 36 times the receiver part (32 in rear panel, 2 optical inputs and 2 copper inputs in front panel). The serial inputs protocol is the same and described in chapter 4.

The card holds seven modes of operation described in chapter 3.

The VME interface is 24 bits address and 32 bits data with interrupt possibility. The base address must be set by corresponding 5 bits switches which determine a 19 bits address space for a module.

A specific address is reserved to program from the VME bus the on board FPGA. Another corresponding eight switches might be also set (See SW1 on card view – chapter 6). This feature is reserved for specialists only.

Three jumpers determine the default mode of the card (see chapter 3). The mode is also programmable.

The last four jumpers on the card are for specialists only. When removed they permit a JTAG programming of the Prom of the onboard Xilinx FPGA.

The inputs/outputs of the module depend of the mode, so they will also be described in chapter 3.

See front view in chapter 5 to see all front panel inputs.

2. ADDRESS MAP

The address space covered by the module is limited to five (5) 32 bit registers + 512kBytes of on board memory. Base address (BA) can be set with SW2 (see card view – chapter 6). The addresses of the internal registers are given below, as byte offsets from the module VME base address:

Address	*R/W*	*Register Name*	*Register description (or Command)*
BA	R/W	SOURCEREG	control Register
+0x04	R	READADDREG	Memory Pointer Register

+0x08	R/W	MODEREG	Mode Register
+0x0C	R/W	CHANNELREG	Channel Register
+0x10	R	FREQREG	Frequency Meter Register
+0x14	R/W	DACREG	DAC outputs Register
+0x20 to +7FFC	R	External Memory	External Memory 512kBytes (minus 32 Bytes)

2.1 THE CONTROL REGISTER

The control register is a control register in write and a status register in read

- **Bit 0** is the pulse polarity of the inputs. This bit determines polarity of the inputs: a '0' means negative logic inputs. eg.: pulses from a TG8. A '1' means positive logic inputs used by new timing modules (CTRP, CTRV, CTRI etc…)

- **bit 1** enable (1) or disable (0) the module

- **Bit 2** enable (1) or disable (0) interrupt request

- **Bit 3** is used to trigger a **soft start** command

- **Bit 4** is used to trigger a **soft stop** command

- **Bit 5** is set during acquisition (between a start and a stop input) – If written with a '1' this bit resets the memory pointer address to empty state, it is the **soft re-arm** command.

- **Bit 6** is set if there is a Counter overflow (btrain mode). This bit is read only

- **Bit 7** is set if the RAM is overflowed. This bit is read only.

- **Bit 15 down to 8** is the IRQ vector whose default value is: 134 decimal, 86 hex – these bits could be read or written to set the new interrupt vector.

- **Bit 31 down to 16** is the version number (read only). eg.: 0142 means version 1.42.

The soft start command could be used as the front panel "**start**" input, this action or pulse starts the acquisition process.

The soft stop command could be used as the front panel "**stop**" input, this action or pulse stops the acquisition process.

The re-arm command could not be sent during the acquisition, so a disable module (0 on bit 1) must be done before this command. This command could replace the "**Reset**" front panel lemo00 input.

2.2 THE MEMORY POINTER REGISTER

In this register you read the memory pointer.

- If this register is filled with **00000020** the memory is **EMPTY**.

- If this register is filled with **0007FFFC** the memory is **FULL**.

- Other value means that the memory could be read from 0x20 to the value read in the register with significant value received by the card.

- The pointer gives a value in bytes so the increased factor is always four because of the 32 bits (four bytes) data bus of the CVORA card.

The organisation of the value received depends on the mode and will be described, mode by mode, in chapter 3.

2.3 THE MODE REGISTER

Only the three least significant bits give the mode. Seven modes are possible.

- Mode 000 --> reserved but parallel input for the moment
- Mode 100 --> parallel input
- Mode 001 --> one optical input 16 bits – Input 2 is ignored
- Mode 010 --> one copper Input 16 bits
- Mode 011 --> Btrain counters
- Mode 101 --> two optical inputs 16 bits
- Mode 110 --> two copper Inputs 16 bits
- Mode 111 --> 32 Serial Inputs on rear panel (P2 connector).

These three bits could be read or written to set the mode. There are tree jumpers on the card to set the default mode, but as soon as the mode is written the jumpers are ignored.

The rest of the register is permanently set with the letters “CVO” in ASCII as “**43564Fxx**”.

Eg.: **“43564707”** means mode **“CVORA 32 Serial Inputs”**.

The mode register can not be changed during acquisition. If the module is not disabled the command to change the mode will be ignored.

2.4 CHANNEL REGISTER

This register is used only in the **32 Serial inputs mode**.

Each bit corresponds to an input. So a ‘1’ in the bit 0 enables input 1, a ‘1’ in bit 1 enables input 2, etc…, ‘1’ in bit 31 enables input 32.

The more inputs are validated, the less acquisitions can be stored in memory (see memory organisation for this mode in chapter 3).

2.5 FREQUENCY METER REGISTER

This register holds the frequency of the external clock input in the front panel, it is just to control if the good clock is received. The value read is in Hertz. Usually the clock is the millisecond clock from a timing card, so the correct value read in this case is 3F8 hex (1000 in decimal). This register is read only.

2.6 DAC REGISTER

In the P2 Serial mode (mode 7), this register holds the integer value of the input reconstructed by the internal digital to analogue converter.

e.g.: if 5 is written in this register, the analogue output one must show the plot sent to the input number 5 of the rear panel and the analogue output two shows the plot of the input number 6 of the rear panel. (See front panel in chapter 5)

3. MODES DESCRIPTION

There are seven different modes to use the CVORA card.

There are tree jumpers on the card to set the default mode, but as soon as the mode register is written the jumpers are ignored.

3.1 PARALLEL MODE

The three LSB bits in the mode register must be set with “000” (0).

To stay compatible with old DP-Ram card there is two sub-modes, but in fact, due to the very fast logic in the CVORA, the strobe could be used as the external clock in the parallel mode.

Every clock or strobe pulse, the data are stored in the memory and the address pointer increased by four. When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set. If 16 bits mode is used the MSB two bytes stay at 0 if there is no data on the second flat cable connector. If the 32 bits are connected, the 32 bits are stored, so the 16 bit mode doesn’t really exist and is kept only for compatibility with the old DP-Ram card.

3.1.1 DIGITAL ACQUISITION WITH SYNCHRONIZATION PULSES ON STROBE

16 or 32 bit wide parallel data is acquired via the P2 VME connectors. A special board must be connected at the rear of the VME chassis to hold the two 34 pin flat cable connectors DATA HIGH and DATA LOW. The connector Inputs are balanced receivers with 110 Ohm impedance. Not connected inputs will give 0. The STROBE pulse indicates stable data. These inputs are fully compatible with the old DP-Ram card parallels inputs.

3.1.2 DIGITAL ACQUISITION WITHOUT SYNCHRONIZATION PULSES ON STROBE

This mode is like the one above except that it is assumed that the synchronization between data stable and acquisition CLOCK has already been done externally. This makes synchronization with the STROBE input not necessary, i. e. the STROBE is not connected but the external clock might be.

The parallel mode is kept for compatibility and to keep the possibility to replace an old DP-Ram card with a CVORA. As the parallel inputs come usually from a sampler receiver card, the serial input of the sampler card could be directly connected to one of the copper or optical inputs. Of course one of the following Serial modes might be used.

3.2 OPTICAL “ONE 16 BIT INPUT” MODE

Only the first optical input is used. (Input 1)

The CVORA is put in this mode if the three LSB bits in the mode register are set with 001 (1).

Only the first optical input is taken in account. The second is completely ignored even if data are received on the second input.

The serial data is stored and parallelised permanently in a buffer but stored in the memory only on a rising/falling (depending on polarity bit) edge of the External clock input. The memory pointer is increased by four. When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set.

In every long word (4 bytes) read the 16 MSB bits will be reset at 0.

3.3 OPTICAL “TWO 16 BIT INPUTS” MODE

Both two front panel optical inputs are used.

The CVORA is put in this mode if the three LSB bits in the mode register are set with 101 (5).

The two front panel optical inputs are taken in account.

The serial data is stored and parallelised permanently in a buffer but stored in the memory only on a rising/falling (depending on polarity bit) edge of the External clock input. The memory pointer is increased by four. When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set.

In every long word (4 bytes) read the 16 MSB bits will be the data from input 2 and 16 LSB bits from input 1.

3.4 COPPER “ONE 16 BIT INPUT” MODE

Only the first copper input is used. (Input 1)

The CVORA is put in this mode if the three LSB bits in the mode register are set with 010 (2).

Only the first copper front panel input is taken in account. The second is completely ignored even if data are received on the second input.

The serial data is stored and parallelised permanently in a buffer but stored in the memory only on a rising/falling (depending on polarity bit) edge of the External clock input. The memory pointer is increased by four. When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set.

In every long word (4 bytes) read the 16 MSB bits will be reset at 0.

3.5 COPPER “TWO 16 BIT INPUTS” MODE

Both two front panel copper inputs are used.

The CVORA is put in this mode if the three LSB bits in the mode register are set with 110 (6).

The two front panel copper inputs are taken in account.

The serial data is stored and parallelised permanently in a buffer but stored in the memory only on a rising/falling (depending on polarity bit) edge of the External clock input. The memory pointer is increased by four. When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set.

In every long word (4 bytes) read the 16 MSB bits will be the data from input 2 and 16 LSB bits from input 1.

3.6 32 SERIAL INPUTS MODE

The CVORA is put in this mode if the three LSB bits in the mode register are set with 111 (7).

The 32 rear panel copper inputs are taken in account according to the channel register.

The 16 bit inputs of each serial input are stored in memory if and only if the corresponding bit is set in the channel register and acquisition is started.

All odd inputs are stored in the two LSB bytes of the long word stored.

All even inputs are stored in the two MSB bytes of the long word stored.

Because inputs data contains only 16 bits, the total inputs must be considered as 16 x 2 serial inputs in place of 32 serial inputs. This is to avoid losing space in the 32 bits memory data bus instead.

The serial data is stored and parallelised permanently in a buffer but stored in the memory only on a rising/falling (depending on polarity bit) edge of the External clock input. The memory pointer is increased by four multiplied by the number of serial inputs validated (odd and/or even). When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set.

In every long word (4 bytes) read the 16 MSB bits will be the data from even input and 16 LSB bits from odd input.

The channel register permits to increase consequently the number of clock pulses the data stored in memory. For example if you use only one or two channel, you could store 131040 points of acquisition. If you use the 32 inputs, this number must be divided by 16, so the results is only 8190.

With a 1 MHz input clock, to fill the internal 4Mbits internal memory, this is respectively for one or two inputs 131 seconds of acquisition and 8192 milliseconds of acquisition if all 32 serial inputs are validated. It is enough for a PS cycle but not for a SPS super cycle.

3.7 BTRAIN MODE

The CVORA is put in this mode if the three LSB bits in the mode register are set with 011 (3).

In this mode there is only one up/down counter. When acquisition is started by a start pulse on the front panel input or by a “soft start” command, the counter counts up on edge of the “**bup**” input, and down on edge of the “**bdown**” input.

The edge is a rising or falling edge depending on which polarity is selected in the mode control register.

The instantaneous value resulting from these 32 bits up/down counting is stored in the memory and address pointer is increased by four. When the memory pointer reaches the maximum value (7FFFC) the Memory overflow bit in the control register is set.

If the internal counter reaches the maximum 32 bits value “**FFFFFFFF**” the bit 6 “**Counter Overflow**” is set in the control register.

4. SERIAL INPUT PROTOCOL

The protocol uses the SCI (Serial Communication Interface) data format. The SCI uses the standard non-return-to-zero mark/space data format illustrated in the figure under.

A frame is received every 250 microseconds.

The code 0x0000 is the lowest value measured.

The code 0xFFFF is the highest value measured.

Port configuration is: 128 kbaud, 1 stop, 1start, no parity.

- One first word of 9 bits is sent, bits b0 to b7 are the height most significant bits of the ADC conversion. The bit 8 is set to one.

- A second 9 bits word is sent, bits b0 to b7 are the eight least significant bits of the ADC conversion. The bit b8 is set to zero.

Figure 9-1. SCI Data Format

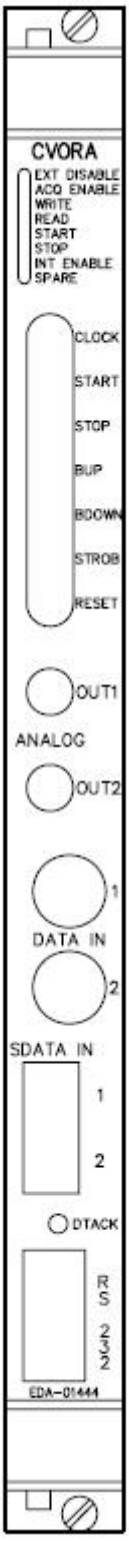
This protocol was historically used in the sampler transceiver card which uses a MC68HC05 microprocessor holding this SCI port. A detailed description of SCI can be read in chapter 9 of the microprocessor documentation:
http://www.freescale.com/files/microcontrollers/doc/data_sheet/MC68HC05C8A.pdf
.

5. FRONT VIEW

You can see, next page, a plot of the front panel and explanations about the led, the analogue outputs and RS232 communication and display port.

There is 9 led on this module, a group of eight at the top and the DTACK (Data acknowledge) led at the bottom.

- The seven led at the top are the same as the DP-Ram card, the spare led is actually lit when the counter is overflowed in the BTRAIN mode or the memory is full in others.



LED:

- **"Ext Disable"** led is yellow and lit when the module is disable (control register bit 1).
- **"Acq Enable"** led is green and lit when the acquisition is started between a start and a stop.
- **"Write"** led is green and lit when the data are written in the internal memory.
- **"Read"** led is green and lit when the internal memory is read from the VME bus.
- **"Start"** led is green and lit during 200 milliseconds when a start pulse or a "soft start" command occurs.
- **"stop"** led is green and lit during 200 milliseconds when a stop pulse or a "soft start" command occurs.
- **"Int Enable"** led is green and lit when the interrupt is enable.
- **"Spare"** led is green and lit when the memory is full or the counter is overflowed in BTRAIN mode.

Analogue output:

These outputs permit to check that the data received are correct and reflect the reality before the digital conversion. An oscilloscope connected on these output will show the analogue signal reconstructed with two internal digital analogue converters. In the "32 Serial mode" the rear inputs shown is indicated in the read/write register DACREG.

RS232 Port:

This port permits to read from a terminal or a "Timing DISPLAY" six lines of 16 characters containing the following data:

- 1st line: CVORA + version number.
- 2nd line: Base address of the module.
- 3rd line: Actual mode of the module.
- 4th line: Frequency of the External clock connected on the clock input.
- 5th line: Bits 15 to 0 of the Channel Register (only relevant in "32 Serial Inputs Mode").
- 6th line: Bits 31 to 16 of the Channel Register (only relevant in "32 Serial Inputs Mode").

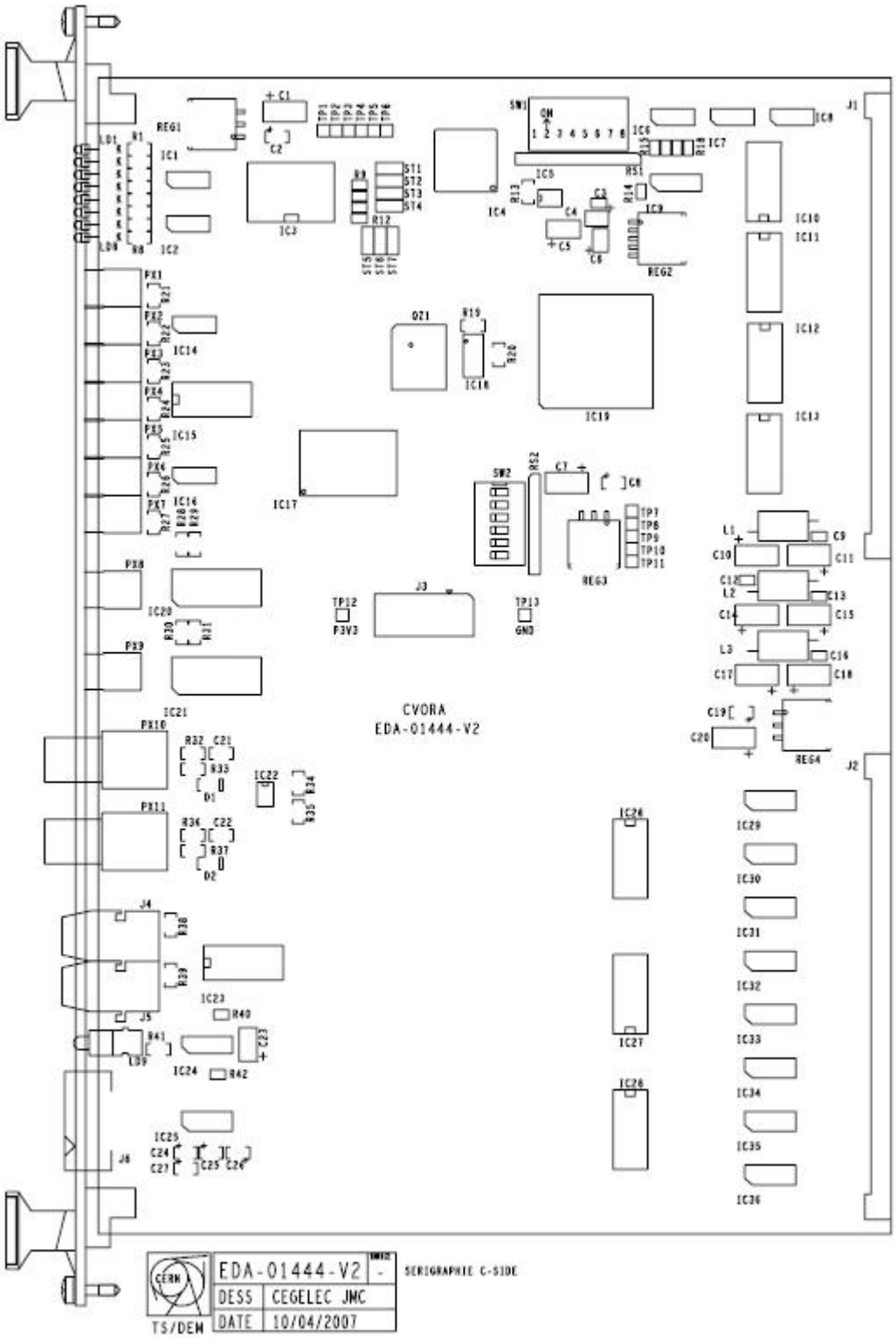
For future use this port is bidirectional, but for the moment only the above data are transmitted from this port.

6. CARD VIEW

Jumpers ST1, ST2, ST3 and ST4 must be closed during operation, these jumpers are used only during JTAG Boundary Scan test of the card after manufacturing.

Jumpers ST5, ST6 and ST7 is the mode by default (at power on), these jumpers are ignored if the mode register is written.

See next page for the drawing of the card.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