

# Report Generated by Test Manager

**Title:** Test  
**Author:** MCBTI  
**Date:** 30-Sep-2025 18:22:14

## Test Environment

Platform: GLNXA64  
MATLAB: (R2025a)

Summary

Name	Outcome	Duration (Seconds)
<a href="#">Results: 2025-Sep-30 18:20:49</a>	2	7.626
<a href="#">MOT_CTRL_CTRL_FUN</a>	2	7.048
<a href="#">MOT_CTRL_CTRL_FUN_003</a>		4.408
<a href="#">MOT_CTRL_CTRL_FUN_004</a>		2.476

## Results: 2025-Sep-30 18:20:49

Result Type: Result Set  
Parent: None  
Start Time: 30-Sep-2025 18:20:50  
End Time: 30-Sep-2025 18:20:58  
Outcome: Total: 2, Passed: 2

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## MOT\_CTRL\_CTRL\_FUN

### Test Result Information

Result Type: Test Suite Result  
Parent: [Results: 2025-Sep-30 18:20:49](#)  
Start Time: 30-Sep-2025 18:20:50  
End Time: 30-Sep-2025 18:20:57  
Outcome: Total: 2, Passed: 2

### Test Suite Information

Name: MOT\_CTRL\_CTRL\_FUN

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## MOT\_CTRL\_CTRL\_FUN\_003

### Test Result Information

Result Type: Test Case Result  
Parent: [MOT\\_CTRL\\_CTRL\\_FUN](#)  
Start Time: 30-Sep-2025 18:20:50  
End Time: 30-Sep-2025 18:20:55  
Outcome: Passed  
Description:

Este teste valida os limites da saída do controlador. Foi utilizado um degrau, que inicia no menor setpoint para testar o limite inferior, e termina em um setpoint maior que a velocidade do motor, validando se o controlador irá saturar no máximo.


## Test Case Information

Name: MOT\_CTRL\_CTRL\_FUN\_003  
Type: Baseline Test

## Test Case Requirements

Description: MOT\_CTRL-CRTL-FUN-003 Saturação na saída do controlador  
Document: MOT\_CTRL\_CTRL.slreqx

## Logical and Temporal Assessments

Name	Assessment
 CheckControlValu es	<p>At any point in time, whenever true is true then, with no delay, result must be true</p> <p><b>REQUIREMENTS</b></p> <p><b>Description:</b> MOT_CTRL-CRTL-FUN-003 Saturação na saída do controlador</p> <p><b>Document:</b> <a href="#">MOT_CTRL_CTRL.slreqx</a></p>

## Simulation

### System Under Test Information

Model: PIDAdj  
Harness: MOT\_CTRL\_CTRL\_FUN\_003  
Harness Owner: PIDAdj  
Release: Current  
Simulation Mode: normal  
Override SIL or PIL Mode: 0  
Configuration Set: Configuration1  
Start Time: 0  
Stop Time: 10  
Checksum: 2546493675 491098190 1403019958 1286505467  
Simulink Version: 25.1  
Model Version: 1.4  
Model Author: tecnicomcbti  
Date: Tue Sep 30 18:10:06 2025  
User ID: tecnicomcbti

Model Path:

Solver Name:

Solver Type:

Fixed Step Size:

Simulation Start Time:

Simulation Stop Time:

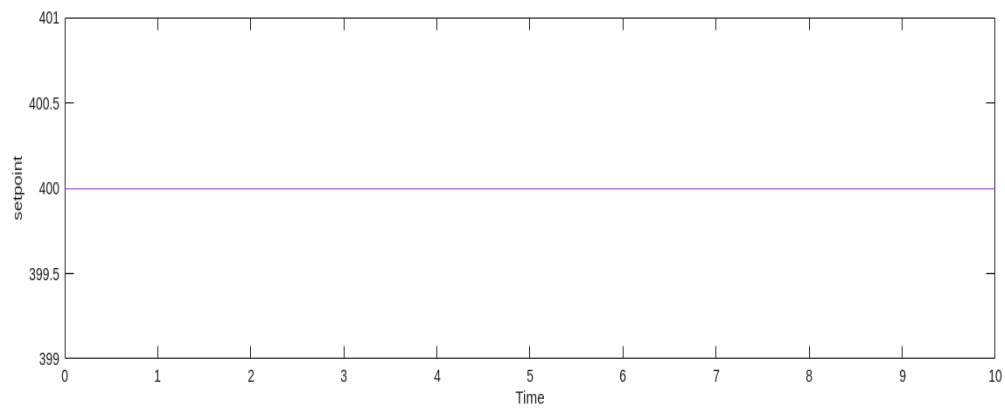
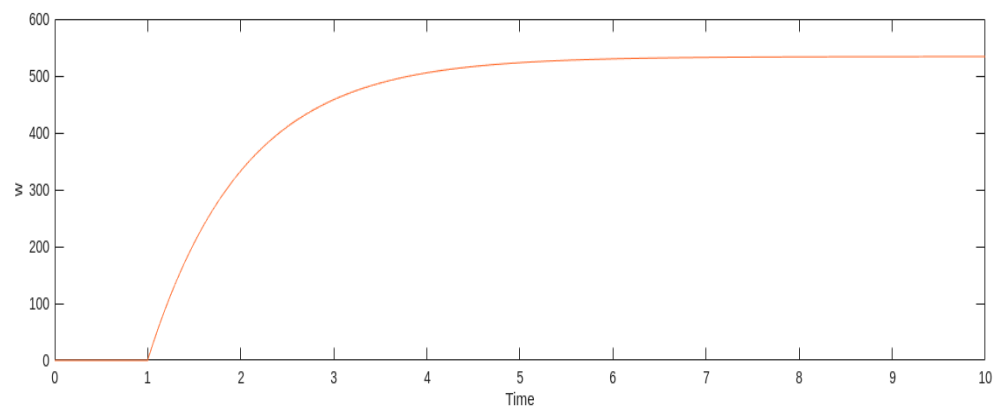
Platform:

/home/tecnicomcbti/cursoMBD/  
model\_based\_design\_with\_real\_time\_hardware\_t  
esting/Tests/PIDControl/  
MOT\_CTRL\_CTRL\_FUN\_003.slx  
ode3  
Fixed-Step  
0.0001  
2025-09-30 18:20:51  
2025-09-30 18:20:54  
GLNXA64

Simulation Output

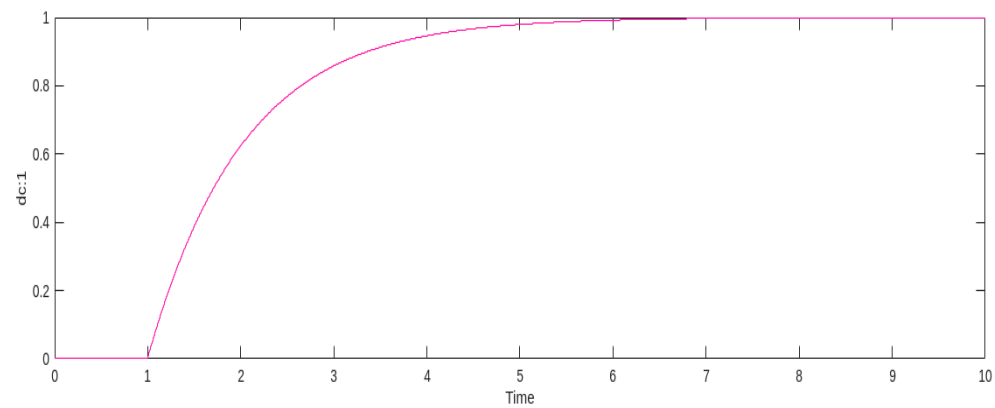
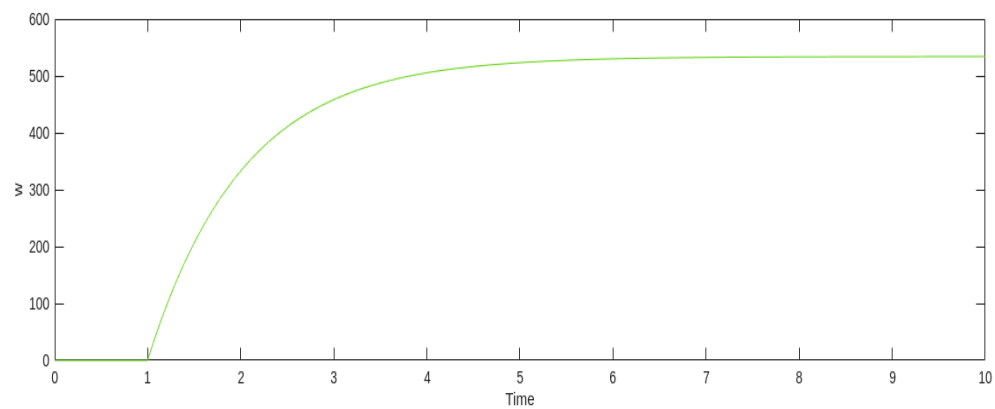
Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
w	double		Continuous	linear	union	<a href="#">Link</a>
setpoint	double		0.001	zoh	union	<a href="#">Link</a>
w	double		0.0001	linear	union	<a href="#">Link</a>
dc:1	double		0.001	zoh	union	<a href="#">Link</a>
result	boolean		0.001	zoh	union	<a href="#">Link</a>

Name	Data Type	Units	Sample Time	Interp	Sync
w	double		Continuous	linear	union
setpoint	double		0.001	zoh	union



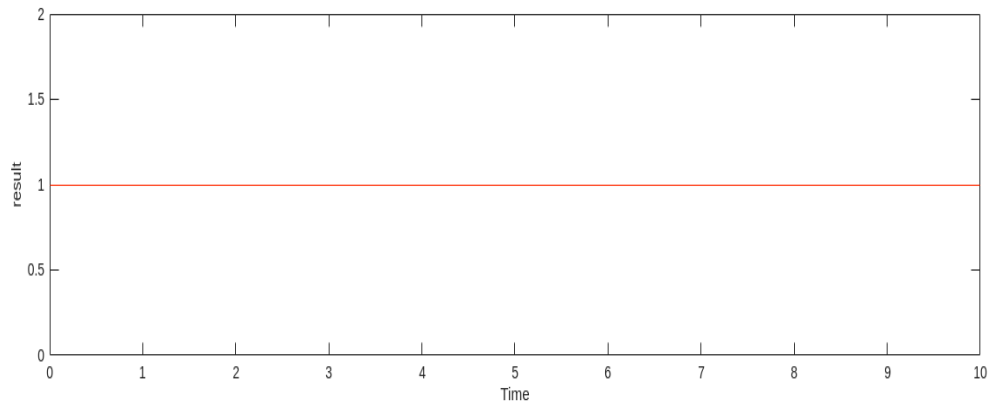
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Name	Data Type	Units	Sample Time	Interp	Sync
w	double		0.0001	linear	union
dc:1	double		0.001	zoh	union



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Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		0.001	zoh	union



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Simulation Logs:

Sample time of '[MOT\\_CTRL\\_CTRL\\_FUN\\_003/Step](#)' '[Output Port 1](#)' and the sample time specified for this signal by '[MOT\\_CTRL\\_CTRL\\_FUN\\_003/Input Conversion Subsystem/SigSpec\\_1](#)' must match.

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#### Test Logs:

No baseline criteria evaluation performed as no baseline data is available for this test.

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## MOT\_CTRL\_CTRL\_FUN\_004

### Test Result Information

Result Type:	Test Case Result
Parent:	<a href="#">MOT_CTRL_CTRL_FUN</a>
Start Time:	30-Sep-2025 18:20:55
End Time:	30-Sep-2025 18:20:57
Outcome:	Passed
Description:	

Este teste valida o tempo de estabilização da resposta a um degrau, utilizando o critério de 2% para o erro em regime permanente.


### Test Case Information

Name:	MOT_CTRL_CTRL_FUN_004
Type:	Baseline Test

### Test Case Requirements

Description:	MOT_CTRL-CRTL-FUN-004 Resposta ao degrau
Document:	MOT_CTRL_CTRL.slreqx

## Logical and Temporal Assessments

Name	Assessment
 CheckSettlingTime	At any point in time, whenever flag is true then, with no delay, result must be true
	<b>REQUIREMENTS</b>
	<b>Description:</b> MOT_CTRL-CRTL-FUN-004 Resposta ao degrau
	<b>Document:</b> <a href="#">MOT_CTRL_CTRL.slreqx</a>

## Simulation

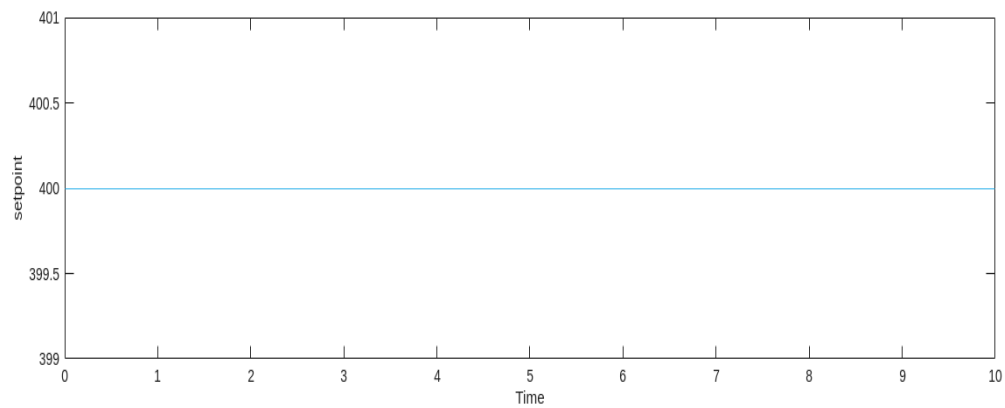
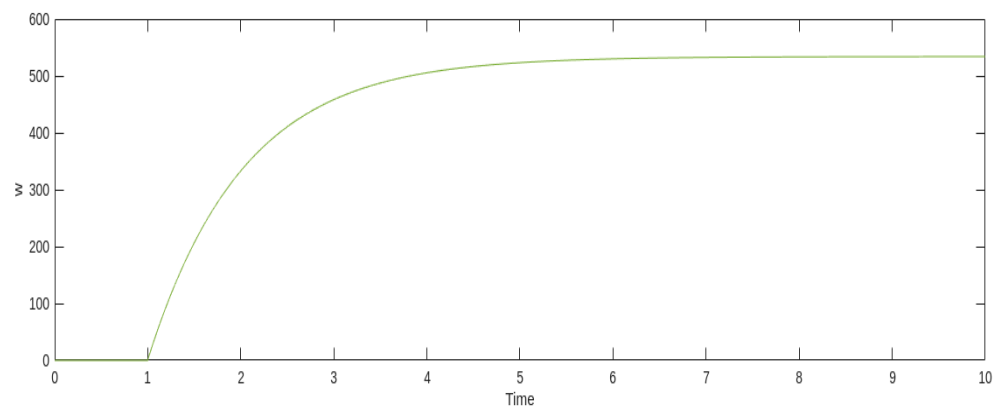
### System Under Test Information

Model:	PIDAdj
Harness:	MOT_CTRL_CTRL_FUN_004
Harness Owner:	PIDAdj
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	1933764614 3710173996 1777251044 721005618
Simulink Version:	25.1
Model Version:	1.6
Model Author:	tecnicomcbti
Date:	Tue Sep 30 18:06:18 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursomBD/ model_based_design_with_real_time_hardware_t esting/Tests/PIDControl/ MOT_CTRL_CTRL_FUN_004.slx
Solver Name:	ode3
Solver Type:	Fixed-Step
Fixed Step Size:	0.0001
Simulation Start Time:	2025-09-30 18:20:55
Simulation Stop Time:	2025-09-30 18:20:57
Platform:	GLNXA64

Simulation Output

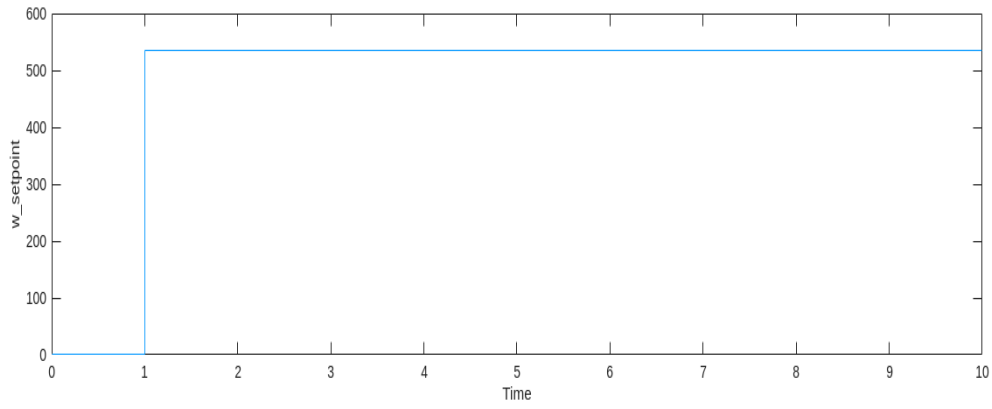
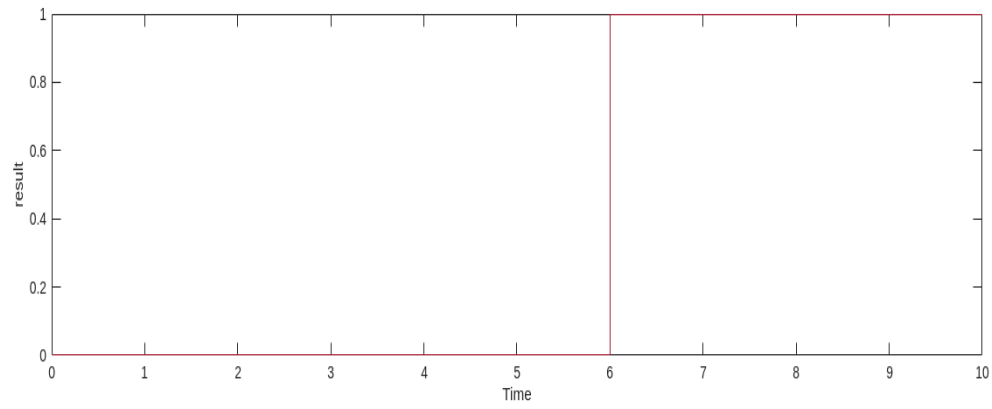
Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
w	double		Continuous	linear	union	<a href="#">Link</a>
setpoint	double		0.001	zoh	union	<a href="#">Link</a>
result	boolean		0.0001	zoh	union	<a href="#">Link</a>
w_setpoint	double		0.0001	zoh	union	<a href="#">Link</a>
flag	boolean		0.0001	zoh	union	<a href="#">Link</a>

Name	Data Type	Units	Sample Time	Interp	Sync
w	double		Continuous	linear	union
setpoint	double		0.001	zoh	union



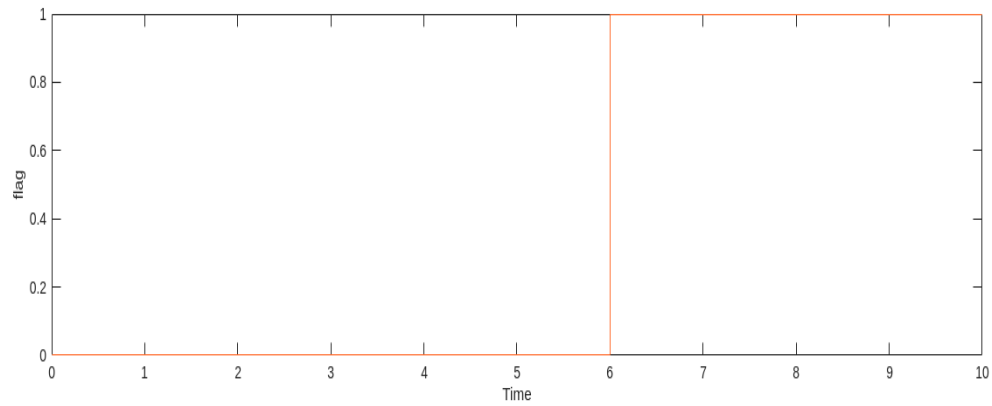
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Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		0.0001	zoh	union
w_setpoint	double		0.0001	zoh	union



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Name	Data Type	Units	Sample Time	Interp	Sync
flag	boolean		0.0001	zoh	union



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Simulation Logs:

Sample time of '[MOT\\_CTRL\\_CTRL\\_FUN\\_004/Test Sequence](#)' '[Output Port 2](#)' and the sample time specified for this signal by '[MOT\\_CTRL\\_CTRL\\_FUN\\_004/Input Conversion Subsystem/SigSpec\\_1](#)' must match.

Sample time of '[MOT\\_CTRL\\_CTRL\\_FUN\\_004/Test Assessment](#)' '[Input Port 2](#)' and the sample time specified for this signal by '[MOT\\_CTRL\\_CTRL\\_FUN\\_004/Input Conversion Subsystem/SigSpec\\_1](#)' must match.

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Test Logs:

No baseline criteria evaluation performed as no baseline data is available for this test.

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