Report Generated by Test Manager

Title: **Test**
Author: **MCBTI**
Date: **30-Sep-2025 09:04:30**

Test Environment

Platform: GLNXA64
MATLAB: (R2025a)

Summary

Name	Outcome	Duration (Seconds)
Results: 2025-Sep-30 08:55:50	3	9.218
MOT_CTRL_PWM_FUN	3	8.914
MOT_CTRL_PWM_FUN_001		1.602
MOT_CTRL_PWM_FUN_002		6.609
MOT_CTRL_PWM_FUN_003		0.481

Results: 2025-Sep-30 08:55:50

Result Type:	Result Set
Parent:	None
Start Time:	30-Sep-2025 08:55:51
End Time:	30-Sep-2025 08:56:00
Outcome:	Total: 3, Passed: 3

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MOT_CTRL_PWM_FUN

Test Result Information

Result Type:	Test Suite Result
Parent:	Results: 2025-Sep-30 08:55:50
Start Time:	30-Sep-2025 08:55:51
End Time:	30-Sep-2025 08:56:00
Outcome:	Total: 3, Passed: 3

Test Suite Information

Name:	MOT_CTRL_PWM_FUN

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MOT_CTRL_PWM_FUN_001

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PWM_FUN
Start Time:	30-Sep-2025 08:55:51
End Time:	30-Sep-2025 08:55:52
Outcome:	Passed
Description:	

Teste do gerador de sinal PWM, de acordo com os requisitos MOT_CTRL_PWM_FUN_001 . Este teste vaida a precisão do sinal PWM.

Test Case Information

Name: MOT_CTRL_PWM_FUN_001
Type: Baseline Test

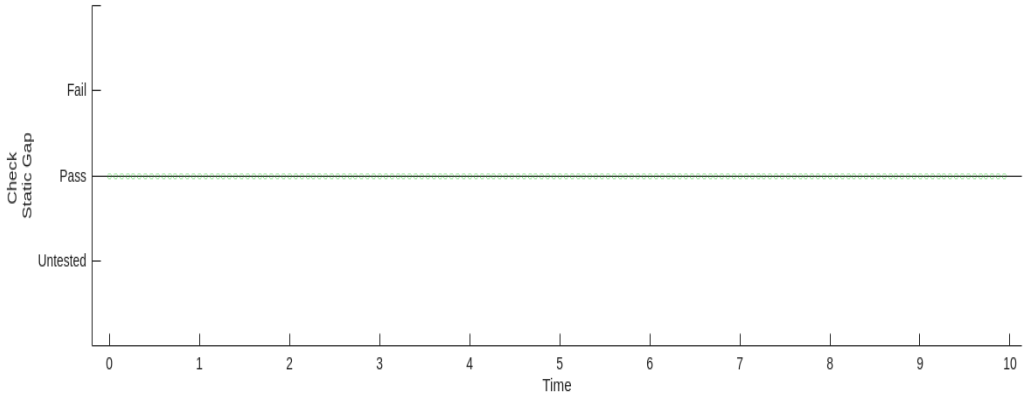
Test Case Requirements

Description: MOT_CTRL_PWM_FUN_001 Geração PWM
Document: MOT_CTRL_PWM.slreqx

Verify Result

Name	Link to Plot
Check Static Gap	Link

Name
Check Static Gap



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Logical and Temporal Assessments

Name	Assessment
DataTypeVerification	At any point in time, whenever true is true then, with a delay of at most 0.0001 seconds, (result_simulation == true) must be true **REQUIREMENTS** **Description:** MOT_CTRL_PWM_FUN_001 Geração PWM **Document:** MOT_CTRL_PWM.slreqx

Simulation

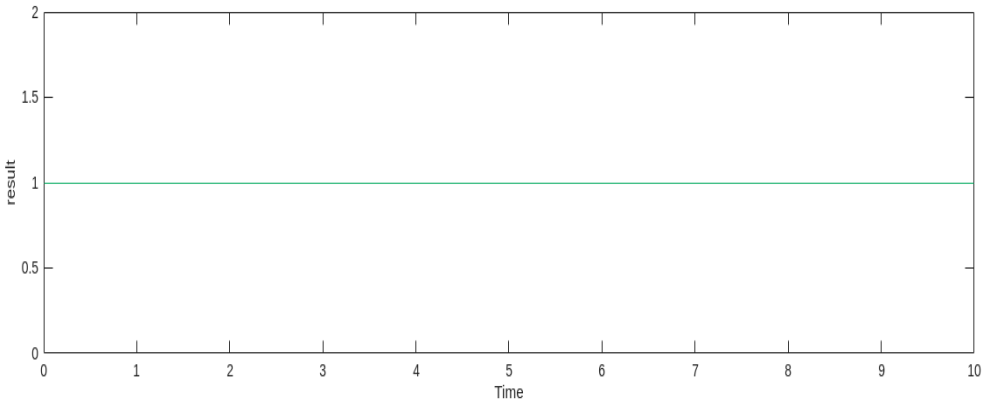
System Under Test Information

Model:	PwmGenerator
Harness:	MOT_CTRL_PWM_FUN_001
Harness Owner:	PwmGenerator
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	1378972331 3600151409 2748184173 2179167049
Simulink Version:	25.1
Model Version:	1.10
Model Author:	tecnicomcbti
Date:	Tue Sep 30 08:07:28 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/PwmGeneration/MOT_CTRL_PWM_FUN_001.slx
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.0001
Simulation Start Time:	2025-09-30 08:55:51
Simulation Stop Time:	2025-09-30 08:55:52
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		0.0001	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		0.0001	zoh	union



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Simulation Logs:
Sample time of 'MOT_CTRL_PWM_FUN_001/Repeating Sequence Stair/Out' 'Output Port 1' and the sample time specified for this signal by

'MOT_CTRL_PWM_FUN_001/Input Conversion Subsystem/SigSpec_1' must match.

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Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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MOT_CTRL_PWM_FUN_002

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PWM_FUN
Start Time:	30-Sep-2025 08:55:53
End Time:	30-Sep-2025 08:55:59
Outcome:	Passed
Description:	

Teste do gerador de sinal PWM de acordo com os requisitos MOT_CTRL_PWM_FUN_002. Este teste vaida a frequência do sinal de PWM, com tolerância de 2%. Escolheu-se um valor de ciclo de trabalho fixo em 50%, que é suficiente para validar a análise no espectro da frequência, pois a onda é de período fixo em 1 [ms]. Adiciou-se um delay de 1 segundo para que o processador de sinal responda.

Test Case Information

Name:	MOT_CTRL_PWM_FUN_002

Type: Baseline Test

Test Case Requirements

Description: MOT_CTRL_PWM_FUN_002 Frequência do sinal PWM
Document: MOT_CTRL_PWM.slreqx

Logical and Temporal Assessments

Name	Assessment
FrequencyAnalysis	At any point in time, whenever (flag == true) is true then, with no delay, (result_simulation == true) must be true **REQUIREMENTS** **Description:** MOT_CTRL_PWM_FUN_002 Frequência do sinal PWM **Document:** MOT_CTRL_PWM.slreqx

Simulation

System Under Test Information

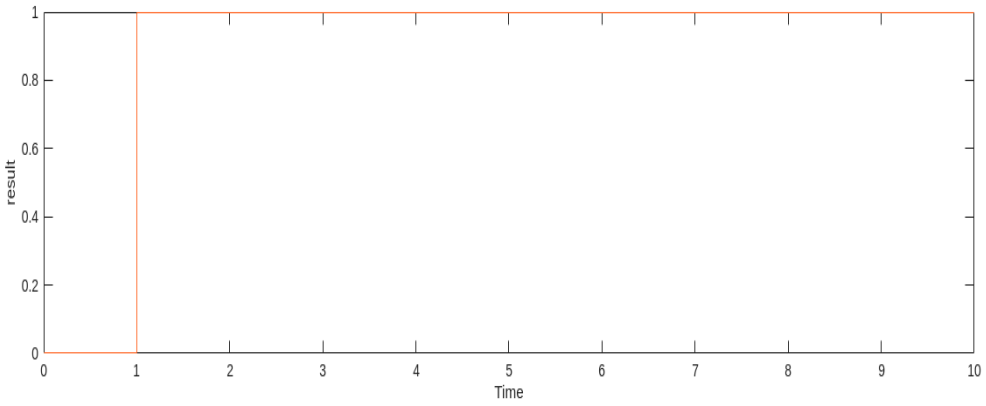
Model:	PwmGenerator
Harness:	MOT_CTRL_PWM_FUN_002
Harness Owner:	PwmGenerator
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	1712715897 2432939688 1546082188 3598526386
Simulink Version:	25.1
Model Version:	1.5
Model Author:	tecnicomcbti
Date:	Tue Sep 30 08:12:56 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/PwmGeneration/MOT_CTRL_PWM_FUN_002.slx

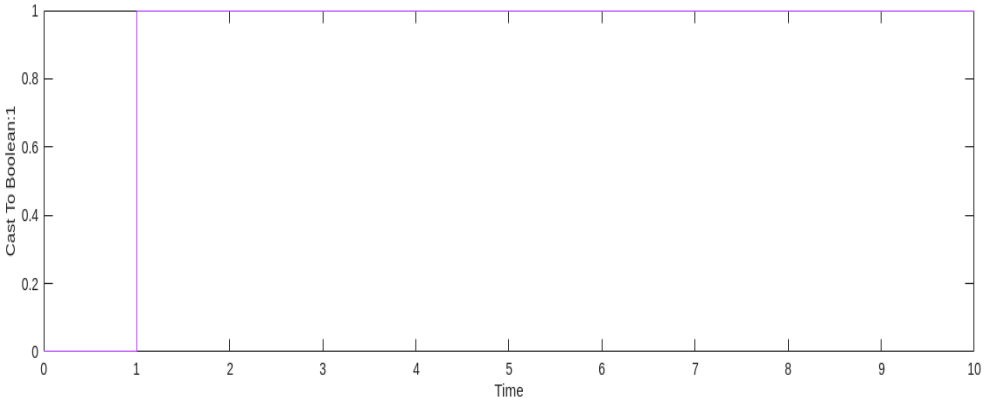
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.0001
Simulation Start Time:	2025-09-30 08:55:53
Simulation Stop Time:	2025-09-30 08:55:59
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		0.0001	zoh	union	Link
Cast To Boolean:1	boolean		0.0001	zoh	union	Link
freq	double		0.0001	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		0.0001	zoh	union
Cast To Boolean:1	boolean		0.0001	zoh	union





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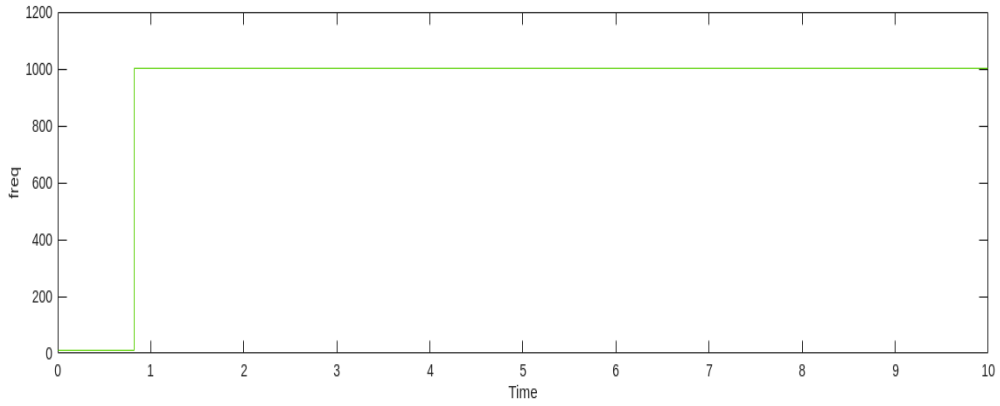
Name	Data Type	Units	Sample Time	Interp	Sync
freq	double		0.0001	zoh	union



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Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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MOT_CTRL_PWM_FUN_003

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PWM_FUN
Start Time:	30-Sep-2025 08:55:59
End Time:	30-Sep-2025 08:56:00
Outcome:	Passed
Description:	

Teste para verificar se o nível de tensão para a saída PWM está de acordo com o intervalo do nível de tensão TTL.

Test Case Information

Name:	MOT_CTRL_PWM_FUN_003
Type:	Baseline Test

Test Case Requirements

Description:	MOT_CTRL_PWM_FUN_003 SInal compatível com nível TTL
Document:	MOT_CTRL_PWM.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckTTLVoltage Level	At any point of time, (result_simulation == true) must be true **REQUIREMENTS** **Description:** MOT_CTRL_PWM_FUN_003 SInal compatível com nível TTL **Document:** MOT_CTRL_PWM.slreqx

Simulation

System Under Test Information

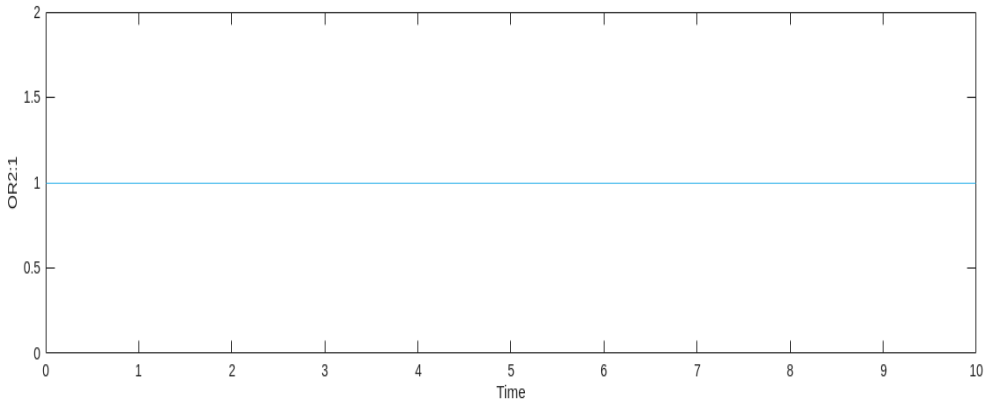
Model:	PwmGenerator
Harness:	MOT_CTRL_PWM_FUN_003

Harness Owner:	PwmGenerator
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	2179236991 4004264220 2984926077 480457920
Simulink Version:	25.1
Model Version:	1.3
Model Author:	tecnicomcbti
Date:	Tue Sep 30 08:16:59 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/PwmGeneration/MOT_CTRL_PWM_FUN_003.slx
Solver Name:	FixedStepDiscrete
Solver Type:	Fixed-Step
Fixed Step Size:	0.0001
Simulation Start Time:	2025-09-30 08:55:59
Simulation Stop Time:	2025-09-30 08:56:00
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
OR2:1	boolean		0.0001	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
OR2:1	boolean		0.0001	zoh	union



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Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

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