Report Generated by Test Manager

Title: **Test**
Author: **MCBTI**
Date: **30-Sep-2025 12:54:51**

Test Environment

Platform: GLNXA64
MATLAB: (R2025a)

Summary

Name	Outcome	Duration (Seconds)
Results: 2025-Sep-30 12:53:13	6	21.679
MOT_CTRL_PTH_FUN	6	17.061
MOT_CTRL_PTH_FUN_001_1		10.045
MOT_CTRL_PTH_FUN_001_2		1.592
MOT_CTRL_PTH_FUN_002_1		1.617
MOT_CTRL_PTH_FUN_002_2		1.059
MOT_CTRL_PTH_FUN_003_1		1.186
MOT_CTRL_PTH_FUN_003_2		0.774

Results: 2025-Sep-30 12:53:13

Result Type:	Result Set
Parent:	None
Start Time:	30-Sep-2025 12:53:14
End Time:	30-Sep-2025 12:53:36
Outcome:	Total: 6, Passed: 6

Back to Report Summary

MOT_CTRL_PTH_FUN

Test Result Information

Result Type:	Test Suite Result
Parent:	Results: 2025-Sep-30 12:53:13
Start Time:	30-Sep-2025 12:53:14
End Time:	30-Sep-2025 12:53:31
Outcome:	Total: 6, Passed: 6

Test Suite Information

Name: MOT_CTRL_PTH_FUN

Back to Report Summary

MOT_CTRL_PTH_FUN_001_1

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PTH_FUN
Start Time:	30-Sep-2025 12:53:14
End Time:	30-Sep-2025 12:53:24
Outcome:	Passed
Description:	

A tensão chaveada na saída deve ser positiva quando o sinal de controle for positivo (forward).

Test Case Information

Name: MOT_CTRL_PTH_FUN_001_1
Type: Baseline Test

Test Case Requirements
Description: MOT_CTRL_PTH_FUN_001_1 Comutação de polaridade positiva
Document: MOT_CTRL_PTH.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckPosVoltage	At any point in time, whenever flag is true then, with no delay, result must be true **REQUIREMENTS** **Description:** MOT_CTRL_PTH_FUN_001_1 Comutação de polaridade positiva **Document:** MOT_CTRL_PTH.slreqx

Simulation

System Under Test Information

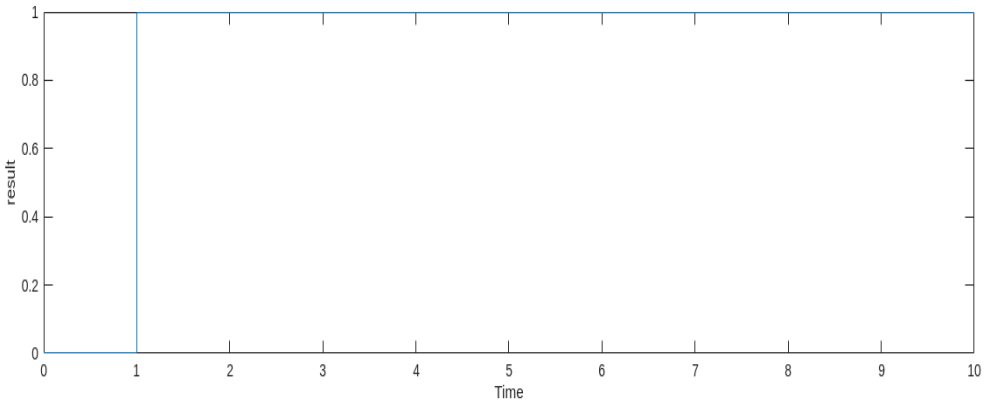
Model:	HBridgeLut
Harness:	MOT_CTRL_PTH_FUN_001_1
Harness Owner:	HBridgeLut
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	4126654337 1588566826 1636800467 2365284924
Simulink Version:	25.1
Model Version:	1.6
Model Author:	tecnicomcbti
Date:	Tue Sep 30 09:51:18 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/Hbridge/MOT_CTRL_PTH_FUN_001_1.slx

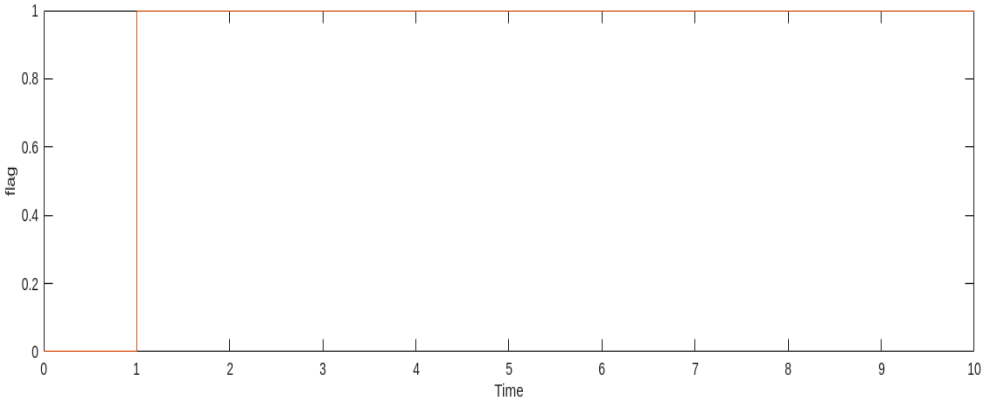
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2025-09-30 12:53:15
Simulation Stop Time:	2025-09-30 12:53:23
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		Continuous	zoh	union	Link
flag	boolean		Continuous	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		Continuous	zoh	union
flag	boolean		Continuous	zoh	union





Back to Report SummaryBack to Signal Summary

Simulation Logs:
Sample time of 'MOT_CTRL_PTH_FUN_001_1/Test Sequence' 'Output Port 2' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_001_1/Input Conversion Subsystem/SigSpec_1' must match.

Sample time of 'MOT_CTRL_PTH_FUN_001_1/Test Sequence' 'Output Port 3' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_001_1/Input Conversion Subsystem/SigSpec_2' must match.

Back to Report Summary

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

Back to Report Summary

MOT_CTRL_PTH_FUN_001_2

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PTH_FUN
Start Time:	30-Sep-2025 12:53:24
End Time:	30-Sep-2025 12:53:26
Outcome:	Passed
Description:	

A tensão chaveada na saída deve ser positiva quando o sinal de controle for negativo (backward).

Test Case Information

Name:	MOT_CTRL_PTH_FUN_001_2
Type:	Baseline Test

Test Case Requirements

Description: MOT_CTRL_PTH_FUN_001_2 Comutação de polaridade negativa
Document: MOT_CTRL_PTH.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckNegVoltage	At any point in time, whenever flag is true then, with no delay, result must be true **REQUIREMENTS** **Description:** MOT_CTRL_PTH_FUN_001_2 Comutação de polaridade negativa **Document:** MOT_CTRL_PTH.slreqx

Simulation

System Under Test Information

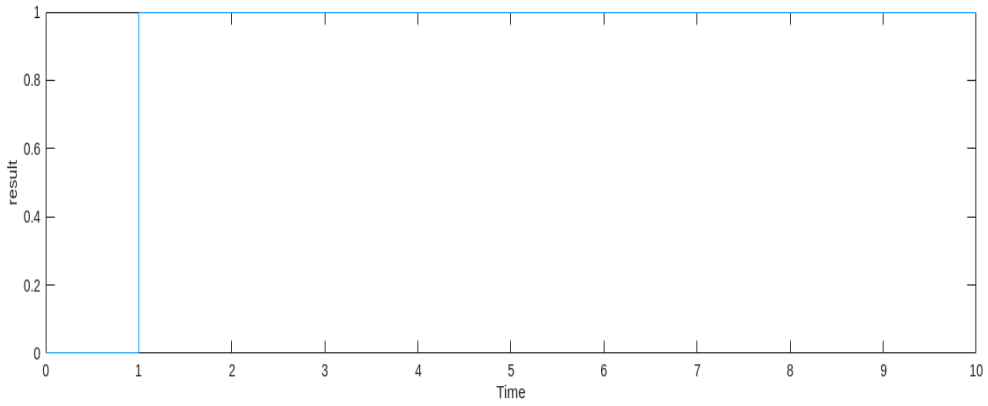
Model:	HBridgeLut
Harness:	MOT_CTRL_PTH_FUN_001_2
Harness Owner:	HBridgeLut
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	3212620800 4110130333 2791090609 3948193966
Simulink Version:	25.1
Model Version:	1.3
Model Author:	tecnicomcbti
Date:	Tue Sep 30 10:21:44 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/Hbridge/MOT_CTRL_PTH_FUN_001_2.slx
Solver Name:	VariableStepDiscrete
Solver Type:	Variable-Step

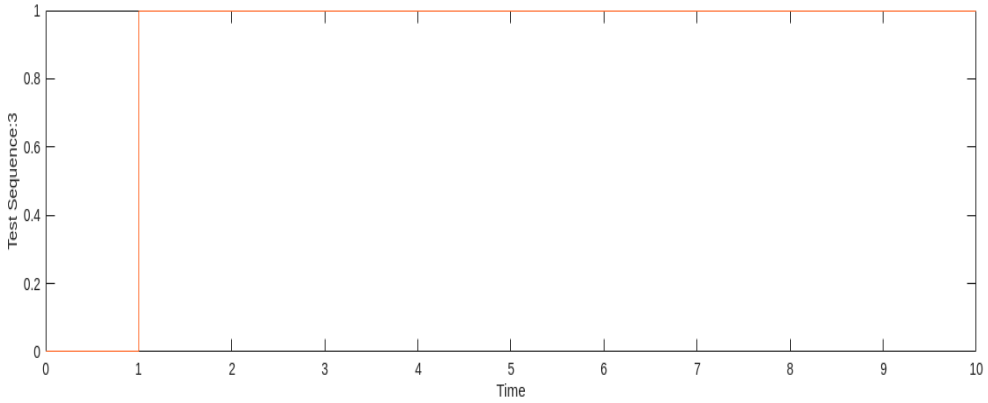
Max Step Size:	0.20000000000000001
Simulation Start Time:	2025-09-30 12:53:24
Simulation Stop Time:	2025-09-30 12:53:26
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		Continuous	zoh	union	Link
Test Sequence:3	boolean		Continuous	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		Continuous	zoh	union
Test Sequence:3	boolean		Continuous	zoh	union





Back to Report SummaryBack to Signal Summary

Simulation Logs:
Sample time of 'MOT_CTRL_PTH_FUN_001_2/Test Sequence' 'Output Port 2' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_001_2/Input Conversion Subsystem/SigSpec_1' must match.

Sample time of 'MOT_CTRL_PTH_FUN_001_2/Test Sequence' 'Output Port 3' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_001_2/Input Conversion Subsystem/SigSpec_2' must match.

Back to Report Summary

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

Back to Report Summary

MOT_CTRL_PTH_FUN_002_1

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PTH_FUN
Start Time:	30-Sep-2025 12:53:26
End Time:	30-Sep-2025 12:53:28
Outcome:	Passed
Description:	

A ponte H deve realizar a transição completa do estado desligado para o estado direto em até 250 ms.

Test Case Information

Name:	MOT_CTRL_PTH_FUN_002_1
Type:	Baseline Test

Test Case Requirements

Description:	MOT_CTRL_PTH_FUN_002_1 Tempo de comutação entre estados da ponte H
Document:	MOT_CTRL_PTH.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckSwitchingTime	At any point in time, whenever flag is true then, with a delay of at most 0.25 seconds, result must be true **REQUIREMENTS** **Description:** MOT_CTRL_PTH_FUN_002_1 Tempo de comutação entre estados da ponte H **Document:** MOT_CTRL_PTH.slreqx

Simulation

System Under Test Information

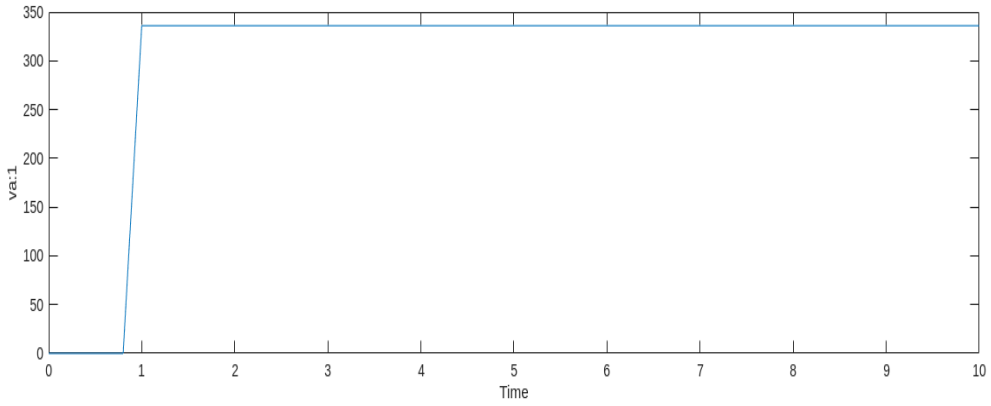
Model:	HBridgeLut
Harness:	MOT_CTRL_PTH_FUN_002_1
Harness Owner:	HBridgeLut
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	2304906878 67289101 2016243114 1814846521
Simulink Version:	25.1
Model Version:	1.4
Model Author:	tecnicomcbti
Date:	Tue Sep 30 10:07:20 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/Hbridge/MOT_CTRL_PTH_FUN_002_1.slx
Solver Name:	VariableStepDiscrete

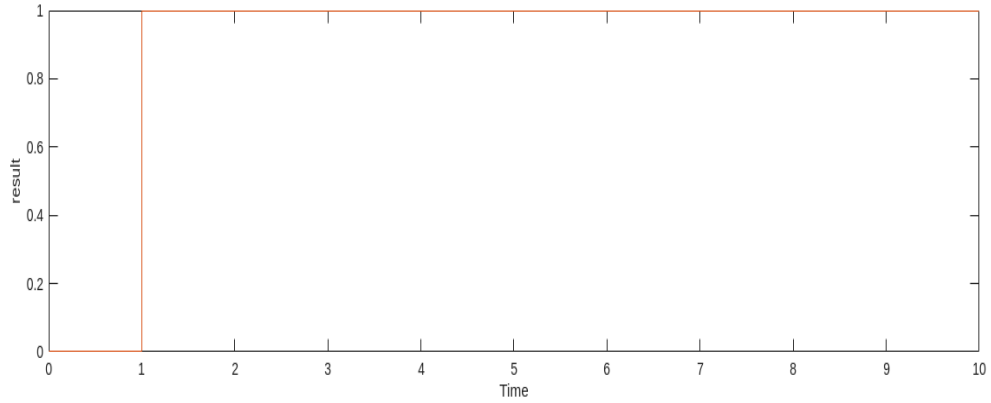
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2025-09-30 12:53:26
Simulation Stop Time:	2025-09-30 12:53:27
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
va:1	double		Continuous	linear	union	Link
result	boolean		Continuous	zoh	union	Link
flag	boolean		Continuous	zoh	union	Link

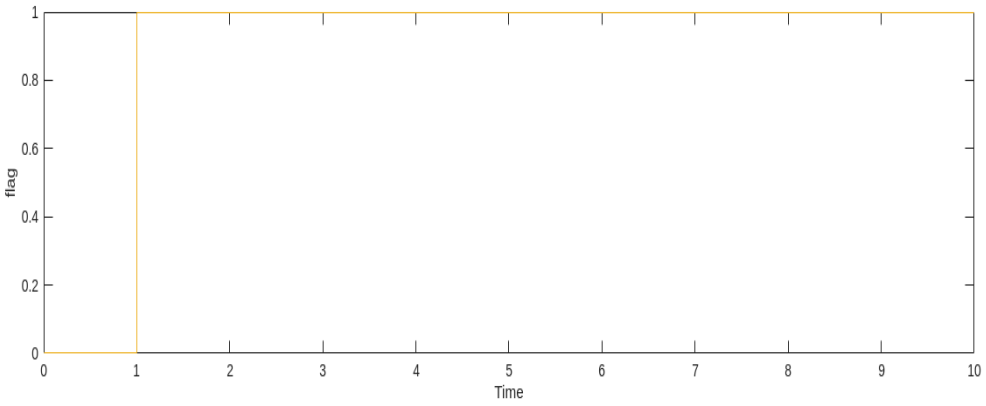
Name	Data Type	Units	Sample Time	Interp	Sync
va:1	double		Continuous	linear	union
result	boolean		Continuous	zoh	union





Back to Report SummaryBack to Signal Summary

Name	Data Type	Units	Sample Time	Interp	Sync
flag	boolean		Continuous	zoh	union



Back to Report SummaryBack to Signal Summary

Simulation Logs:
Sample time of 'MOT_CTRL_PTH_FUN_002_1/Test Sequence1' 'Output Port 2' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_002_1/Input Conversion Subsystem/SigSpec_1' must match.

Sample time of 'MOT_CTRL_PTH_FUN_002_1/Test Sequence1' 'Output Port 3' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_002_1/Input Conversion Subsystem/SigSpec_2' must match.

Back to Report Summary

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

Back to Report Summary

MOT_CTRL_PTH_FUN_002_2

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PTH_FUN
Start Time:	30-Sep-2025 12:53:28
End Time:	30-Sep-2025 12:53:29
Outcome:	Passed
Description:	

A ponte H deve realizar a transição completa do estado desligado para o estado reverso em até 250 ms.

Test Case Information

Name:	MOT_CTRL_PTH_FUN_002_2
Type:	Baseline Test

Test Case Requirements

Description: MOT_CTRL_PTH_FUN_002_2 Tempo de comutação entre estados da ponte H
Document: MOT_CTRL_PTH.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckSwitchingTime	At any point in time, whenever flag is true then, with a delay of at most 0.25 seconds, result must be true **REQUIREMENTS** **Description:** MOT_CTRL_PTH_FUN_002_2 Tempo de comutação entre estados da ponte H **Document:** MOT_CTRL_PTH.slreqx

Simulation

System Under Test Information

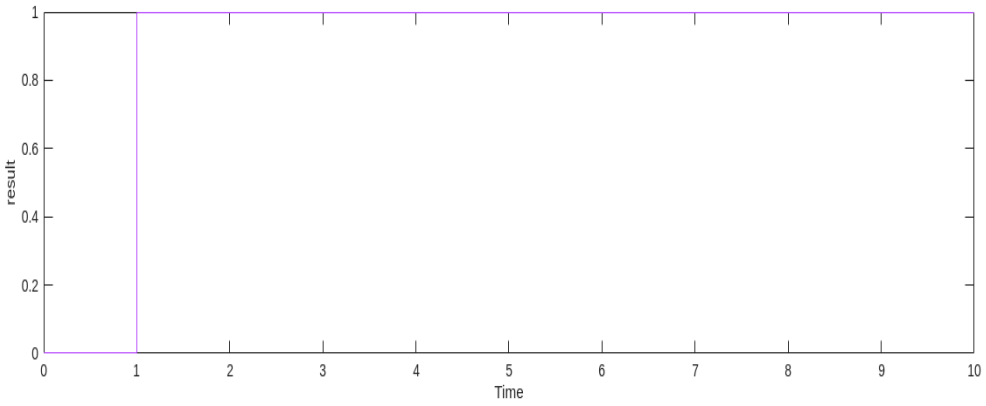
Model:	HBridgeLut
Harness:	MOT_CTRL_PTH_FUN_002_2
Harness Owner:	HBridgeLut
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	355570891 2300943967 43981522 376888449
Simulink Version:	25.1
Model Version:	1.8
Model Author:	tecnicomcbti
Date:	Tue Sep 30 10:09:11 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/Hbridge/MOT_CTRL_PTH_FUN_002_2.slx
Solver Name:	VariableStepDiscrete

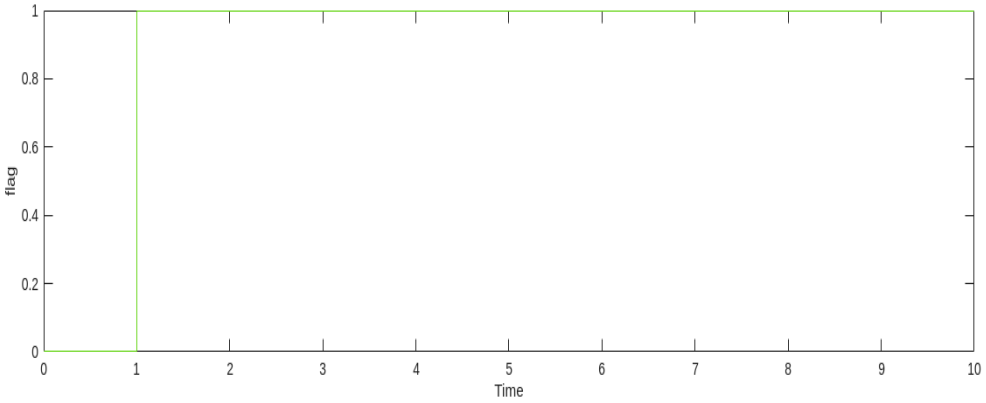
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2025-09-30 12:53:28
Simulation Stop Time:	2025-09-30 12:53:29
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		Continuous	zoh	union	Link
flag	boolean		Continuous	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		Continuous	zoh	union
flag	boolean		Continuous	zoh	union





Back to Report SummaryBack to Signal Summary

Simulation Logs:
Sample time of 'MOT_CTRL_PTH_FUN_002_2/Test Sequence' 'Output Port 2' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_002_2/Input Conversion Subsystem/SigSpec_1' must match.

Sample time of 'MOT_CTRL_PTH_FUN_002_2/Test Sequence' 'Output Port 3' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_002_2/Input Conversion Subsystem/SigSpec_2' must match.

Back to Report Summary

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

Back to Report Summary

MOT_CTRL_PTH_FUN_003_1

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PTH_FUN
Start Time:	30-Sep-2025 12:53:29
End Time:	30-Sep-2025 12:53:30
Outcome:	Passed
Description:	

A tensão de saída da ponte H aplicada ao motor deve próxima de 336 V no sentido direto, com toletância de 5%.

Test Case Information

Name:	MOT_CTRL_PTH_FUN_003_1
Type:	Baseline Test

Test Case Requirements

Description: MOT_CTRL_PTH_FUN_003_1 Faixa de operação da tensão de saída da ponte H
Document: MOT_CTRL_PTH.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckStaticGap	At any point in time, whenever flag is true then, with a delay of at most 0.25 seconds, result must be true **REQUIREMENTS** **Description:** MOT_CTRL_PTH_FUN_003_1 Faixa de operação da tensão de saída da ponte H **Document:** MOT_CTRL_PTH.slreqx

Simulation

System Under Test Information

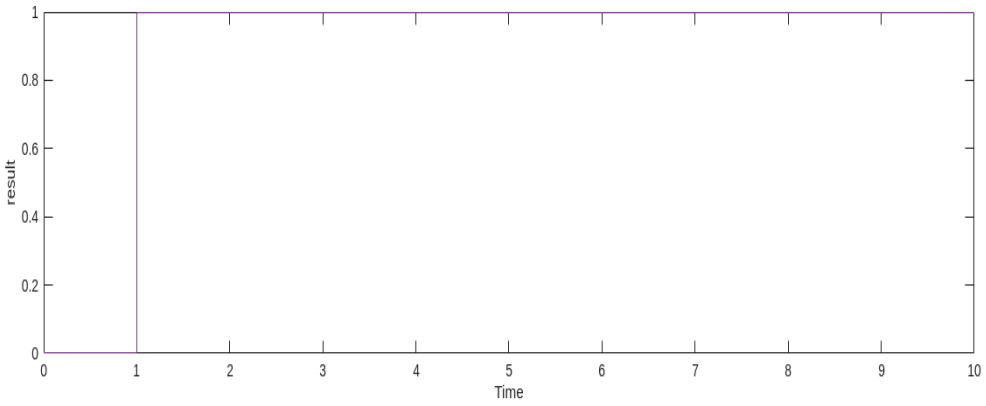
Model:	HBridgeLut
Harness:	MOT_CTRL_PTH_FUN_003_1
Harness Owner:	HBridgeLut
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	3152107088 605830788 2509720400 1449986112
Simulink Version:	25.1
Model Version:	1.6
Model Author:	tecnicomcbti
Date:	Tue Sep 30 10:17:55 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/Hbridge/MOT_CTRL_PTH_FUN_003_1.slx
Solver Name:	VariableStepDiscrete

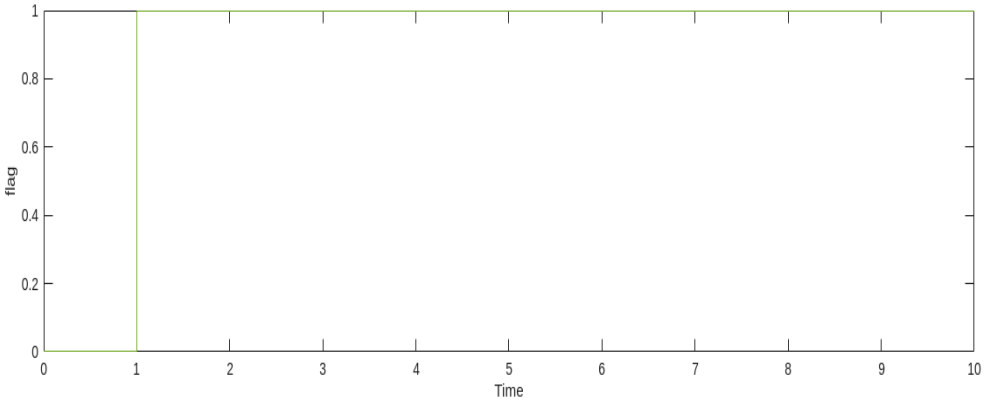
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2025-09-30 12:53:29
Simulation Stop Time:	2025-09-30 12:53:30
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		Continuous	zoh	union	Link
flag	boolean		Continuous	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		Continuous	zoh	union
flag	boolean		Continuous	zoh	union





Back to Report SummaryBack to Signal Summary

Simulation Logs:
Sample time of 'MOT_CTRL_PTH_FUN_003_1/Test Sequence' 'Output Port 2' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_003_1/Input Conversion Subsystem/SigSpec_1' must match.

Sample time of 'MOT_CTRL_PTH_FUN_003_1/Test Sequence' 'Output Port 3' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_003_1/Input Conversion Subsystem/SigSpec_2' must match.

Back to Report Summary

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

Back to Report Summary

MOT_CTRL_PTH_FUN_003_2

Test Result Information

Result Type:	Test Case Result
Parent:	MOT_CTRL_PTH_FUN
Start Time:	30-Sep-2025 12:53:30
End Time:	30-Sep-2025 12:53:31
Outcome:	Passed
Description:	

A tensão de saída da ponte H aplicada ao motor deve próxima de 336 V no sentido reverso, com toletância de 5%.

Test Case Information

Name:	MOT_CTRL_PTH_FUN_003_2
Type:	Baseline Test

Test Case Requirements

Description: MOT_CTRL_PTH_FUN_003_2 Faixa de operação da tensão de saída da ponte H
Document: MOT_CTRL_PTH.slreqx

Logical and Temporal Assessments

Name	Assessment
CheckStaticGap	At any point in time, whenever flag is true then, with a delay of at most 0.25 seconds, result must be true **REQUIREMENTS** **Description:** MOT_CTRL_PTH_FUN_003_2 Faixa de operação da tensão de saída da ponte H **Document:** MOT_CTRL_PTH.slreqx

Simulation

System Under Test Information

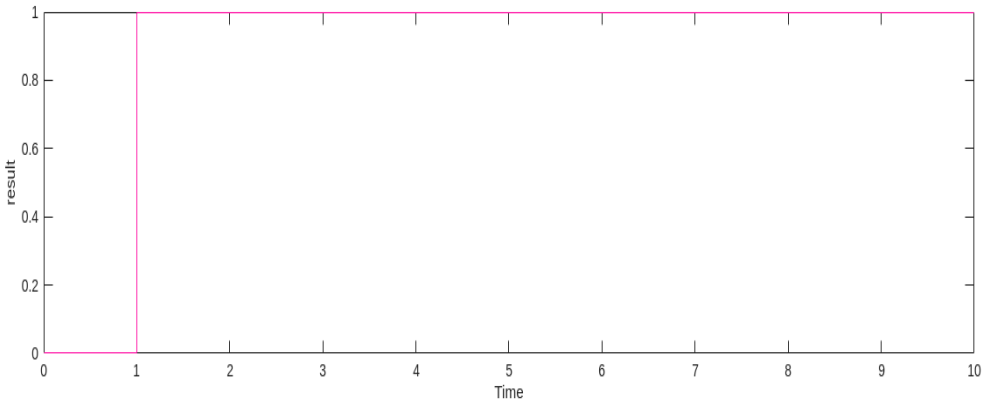
Model:	HBridgeLut
Harness:	MOT_CTRL_PTH_FUN_003_2
Harness Owner:	HBridgeLut
Release:	Current
Simulation Mode:	normal
Override SIL or PIL Mode:	0
Configuration Set:	Configuration1
Start Time:	0
Stop Time:	10
Checksum:	557191343 2264133680 2558056823 3958585701
Simulink Version:	25.1
Model Version:	1.5
Model Author:	tecnicomcbti
Date:	Tue Sep 30 10:20:52 2025
User ID:	tecnicomcbti
Model Path:	/home/tecnicomcbti/cursoMBD/model_based_design_with_real_time_hardware_testing/Tests/Hbridge/MOT_CTRL_PTH_FUN_003_2.slx
Solver Name:	VariableStepDiscrete

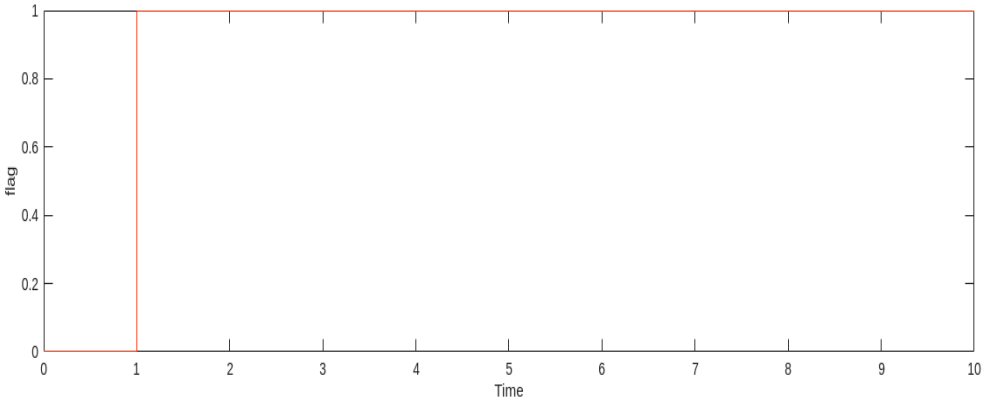
Solver Type:	Variable-Step
Max Step Size:	0.20000000000000001
Simulation Start Time:	2025-09-30 12:53:30
Simulation Stop Time:	2025-09-30 12:53:31
Platform:	GLNXA64

Simulation Output

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plot
result	boolean		Continuous	zoh	union	Link
flag	boolean		Continuous	zoh	union	Link

Name	Data Type	Units	Sample Time	Interp	Sync
result	boolean		Continuous	zoh	union
flag	boolean		Continuous	zoh	union





Back to Report SummaryBack to Signal Summary

Simulation Logs:
Sample time of 'MOT_CTRL_PTH_FUN_003_2/Test Sequence' 'Output Port 2' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_003_2/Input Conversion Subsystem/SigSpec_1' must match.

Sample time of 'MOT_CTRL_PTH_FUN_003_2/Test Sequence' 'Output Port 3' and the sample time specified for this signal by 'MOT_CTRL_PTH_FUN_003_2/Input Conversion Subsystem/SigSpec_2' must match.

Back to Report Summary

Test Logs:
No baseline criteria evaluation performed as no baseline data is available for this test.

Back to Report Summary