CprE 281 QUIZ 7

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Initial Stuff and Basics
Assigned Date: Week # 10

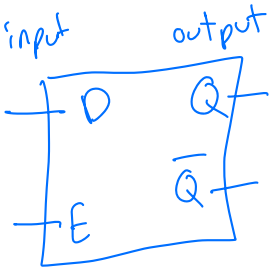
Instructions

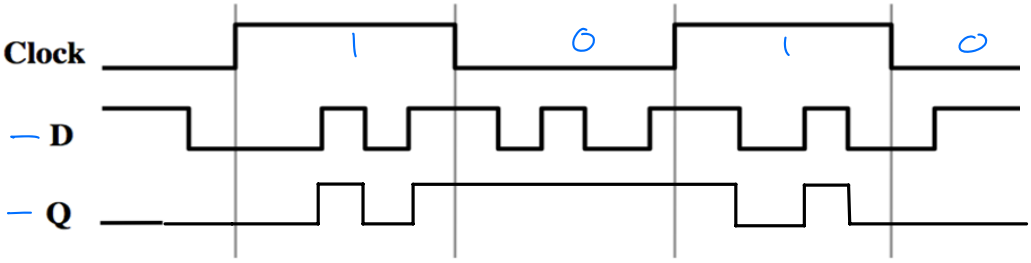
Complete the question below to the best of your ability. Once complete, upload a PDF of your work to canvas.

Questions

P1. Timing Diagram (1x 20p each = 30p)

Assume that Q is initially zero for this problem. Complete the timing diagram for a gated D Latch shown below:





P2. D flip-flop (1 x 10p each = 10p)

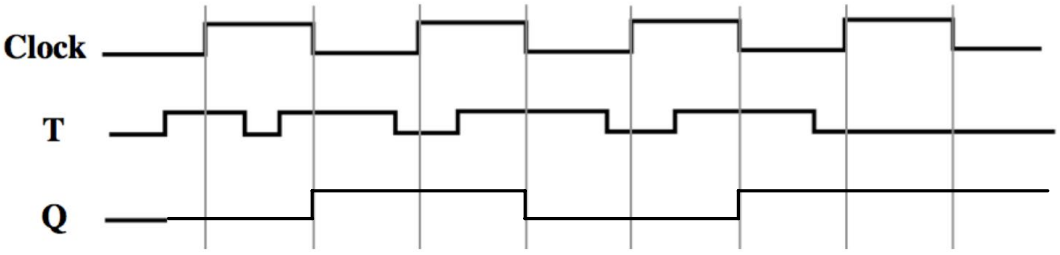
Draw a circuit diagram of the positive-edge-triggered D flip-flop with synchronous preset.

below

P3. Timing Diagram (1x 20p each = 30p)

Assume that Q is initially zero for this problem. Complete the timing diagram for a negative edge-triggered T flip-flop shown below:

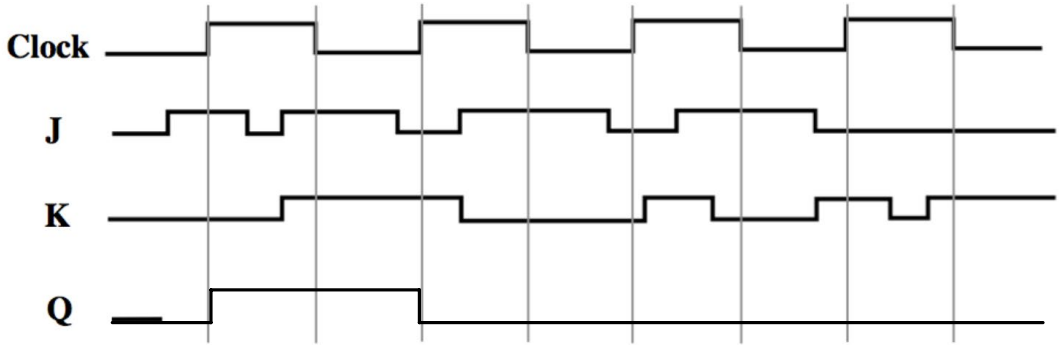
T flip flop



P4. Timing Diagram (1x 20p each = 30p)

Assume that Q is initially zero for this problem. Complete the timing diagram for a positive edge-triggered J-K flip-flop shown below:

J-K flip flop



P2) inputs