CprE 281 QUIZ 8

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Initial Stuff and Basics
Assigned Date: Week # 11

Instructions

Complete the question below to the best of your ability. Once complete, upload a PDF of your work to canvas.

Questions

P1. Register (40 points)

Below ↓

Design a four-bit register with both shift and parallel load features. The inputs of the register include a 2-bit input bus J as J_1J_0, a 4-bit input bus X as $X_3X_2X_1X_0$, and a clock signal. The register will have a 4-bit output bus Q that represents the value stored in the register. You are allowed to use any number and size of the following: DFFs, MUXes, decoders, encoders, AND gates, OR gates, and NOT gates (Notice that you do not need all of them). The operation of the registers are defined below:

- If J=0, then the output Q will take on the values in X.
  $Q_3^{new} = X_3, Q_2^{new} = X_2, Q_1^{new} = X_1, Q_0^{new} = X_0$
- If J=1, then the output Q remains unchanged.
  $Q_3^{new} = Q_3^{old}, Q_2^{new} = Q_2^{old}, Q_1^{new} = Q_1^{old}, Q_0^{new} = Q_0^{old}$
- If J=2, then the output Q is shifted to the left.
  $Q_3^{new} = Q_2^{old}, Q_2^{new} = Q_1^{old}, Q_1^{new} = Q_0^{old}, Q_0^{new} = X_0$
- If J=3, then the output Q is shifted to the right.
  $Q_3^{new} = X_0, Q_2^{new} = Q_3^{old}, Q_1^{new} = Q_2^{old}, Q_0^{new} = Q_1^{old}$

P2. Register File (40p)

Below ↓

Design a **register file** with **two 4-bit registers**, one write port, one read port, and one write enable line.

P3. Counter (2x 10p each = 20p)

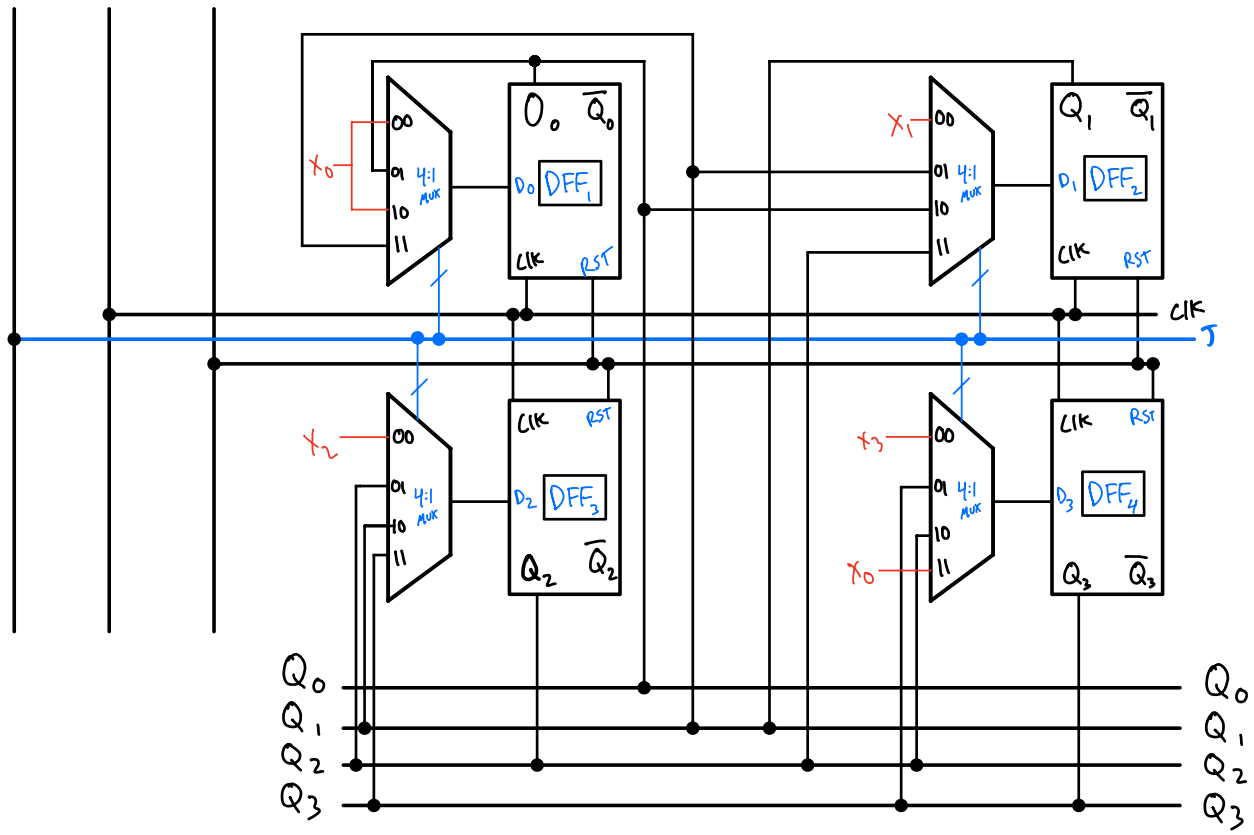
Below ↓

a) Design a four-bit asynchronous down-counter.
b) Design a three-bit synchronous down-counter

P1)

inputs

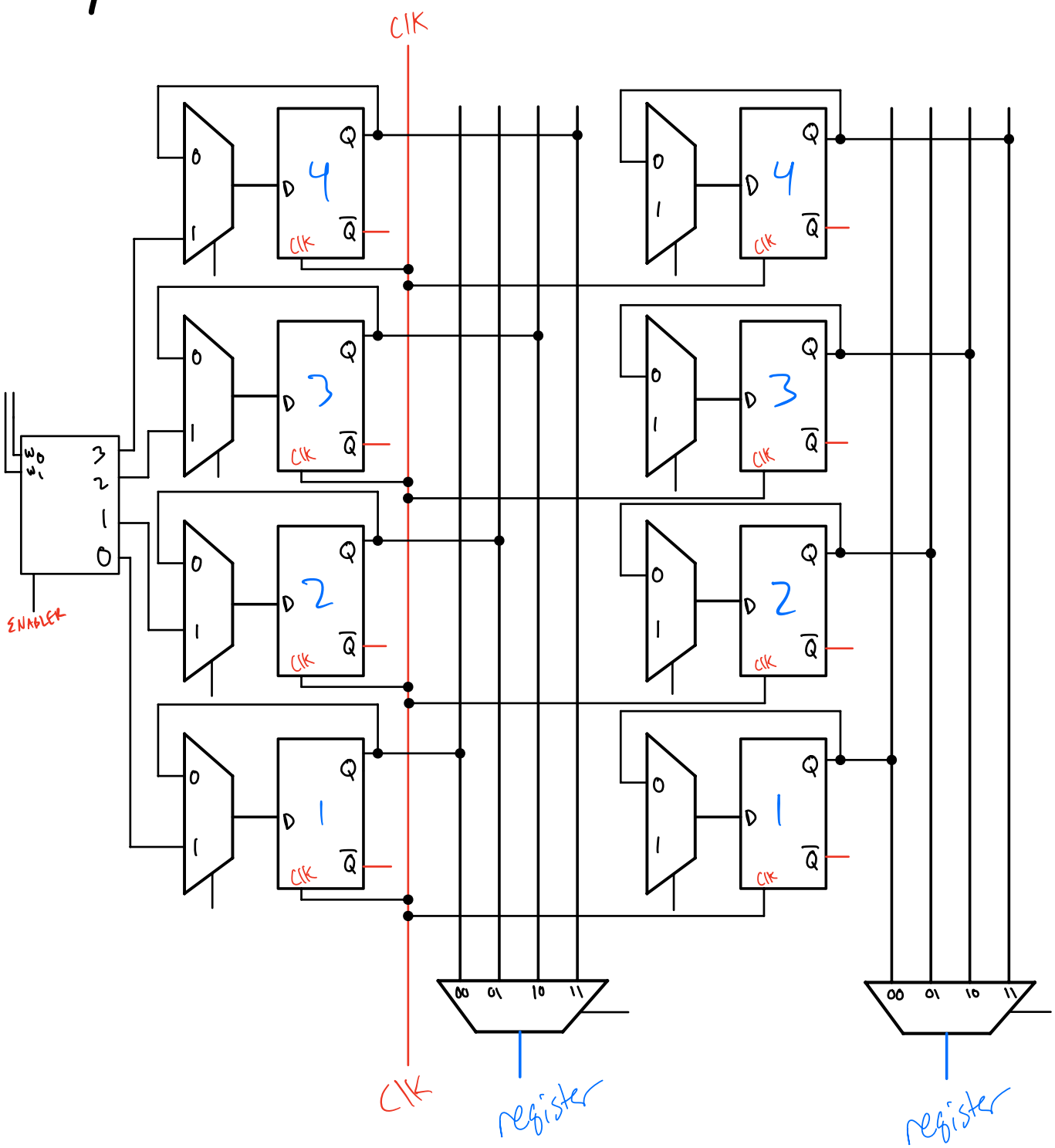
J CLK Reset



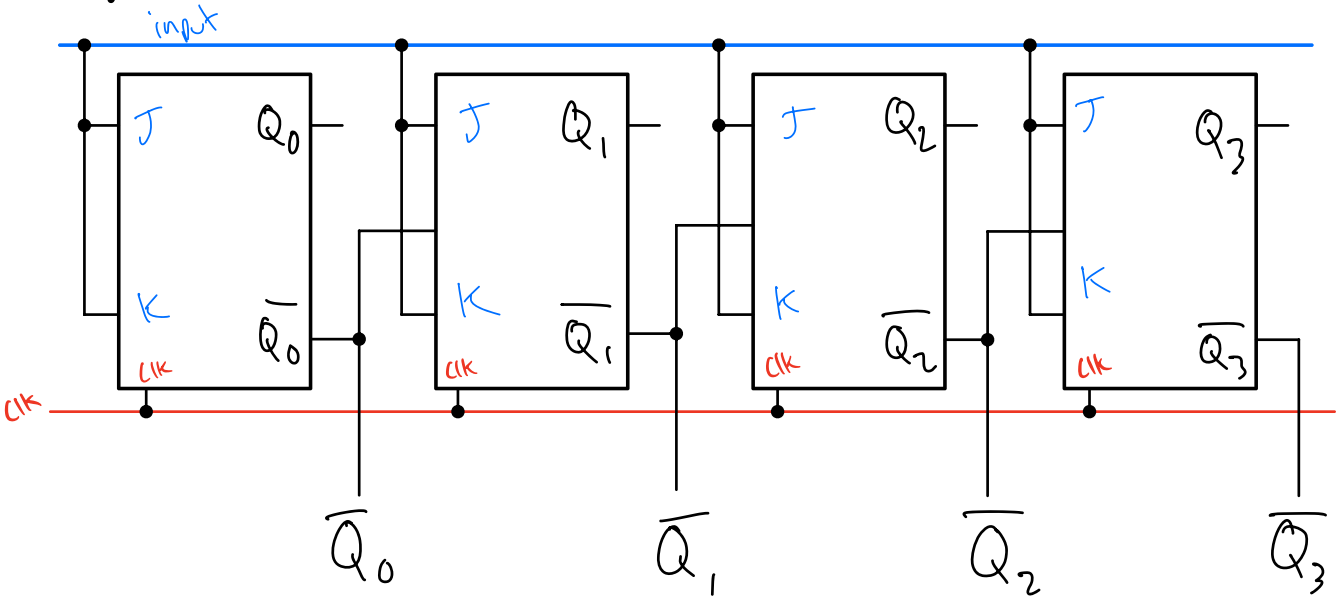
register Outputs

p2)

dual 4 bit registers



P3) a) 4 bit asynch down counter



b) 3 bit synch down counter