CprE 281 HW6
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Multiplexers, Decoders, Encoders, and Latches
Assigned Date: Week #08
Finish by Mar. 12, 2023

Questions

P 1. (16 points) Answer the following questions about decoders and MUXes:

a. How many 2-4 decoders are necessary to create a 4-to-16 decoder?
b. How many 3-8 decoders are necessary to create a 6-to-64 decoder?
c. How many 1-bit 2-to-1 MUXes are necessary to create a 1-bit 8-to-1 MUX?
d. How many 1-bit 2-to-1 MUXes are necessary to create an 8-bit 2-to-1 MUX?

below ↓

P 2. (10 points) Given a supply of 1-to-2 decoders, show how to get a 3-to-8 decoder circuit. Assume each of the 1-to-2 decoders has an ENABLE input (ENABLE = 1 enables the decoder), but you do not need to include enable capability on the 3-to-8 decoder circuit.

below ↓

P 3.(20 points) Consider the following truth table for the function $f(a, b, c, d)$.

below ↓

a	*b*	*c*	*d*	*f*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

a) Implement *f* using one 4-to-16 decoder and a minimal number of gates.

b) Implement *f* using two 2-to-4 decoders, one 4-to-1 multiplexer, and a minimal number of gates.

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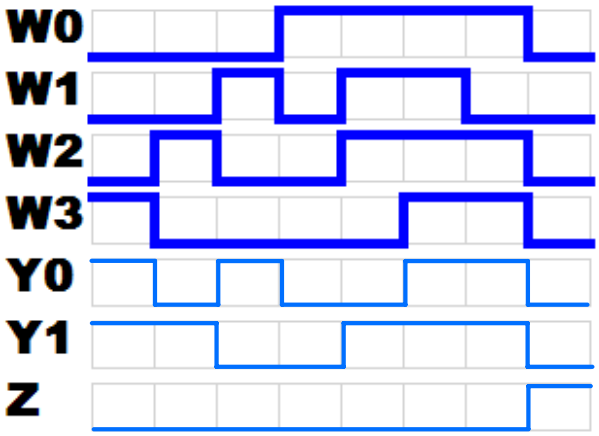
P 4. (28 points): Using the specified decoder(s), implement the following:

below ↓

A. One NOT gate using only one 1-2 decoder.
B. One **3**-input AND gate using only two 1-2 decoders.
C. One 2-input OR gate using only four 1-2 decoders.
D. One 2-input NOR gate using only one 2-4 decoder.

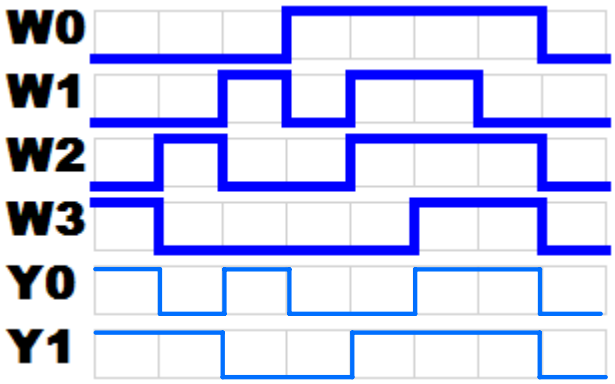
P 5. **(16 points)** Fill in the timing diagrams below:

A. For a 4-to-2 priority encoder.



priority

B. B: For a 4-to-2 binary encoder.



binary

C. Which encoder's inputs are contrary to its input assumptions? Why?

the binary encoder, there are multiple cycles in which both inputs are either high or low at the same time, which is not possible ex. cycles 5, 6, 7, 8

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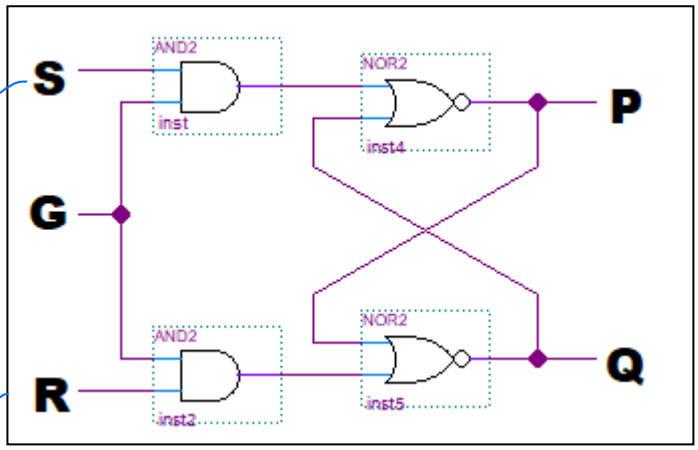
P 6.(10points) Consider the SR Latch shown below.

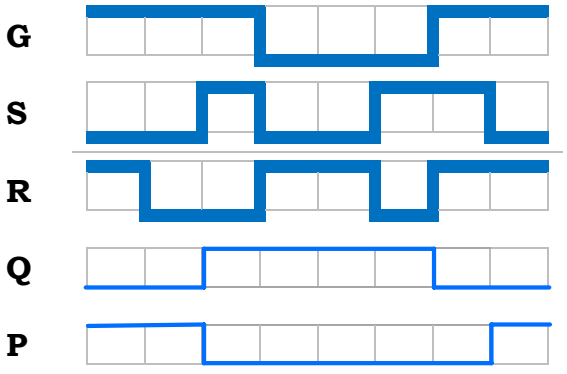


a) Complete the characteristic table.

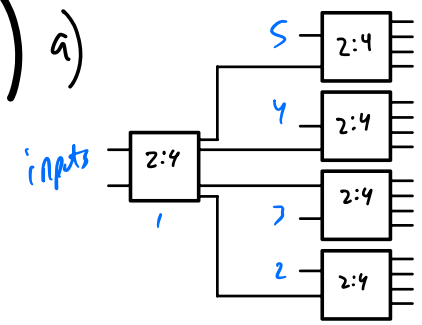
G	S	R	Q	P
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1	0	1
1	1	0	1	0
1	1	1	0	0

MEMORY

b) Complete the timing diagram shown below for outputs Q and P.



P1) a)



for 16 outputs
5 2:4 decoders needed.
16/4 = 4+1 = 5

b) 64/8 = 8+1 = 9

9 3:8 decoders needed for 6 to 64 decoder

c) 1bit 2to1 MUX from 8:1 MUX

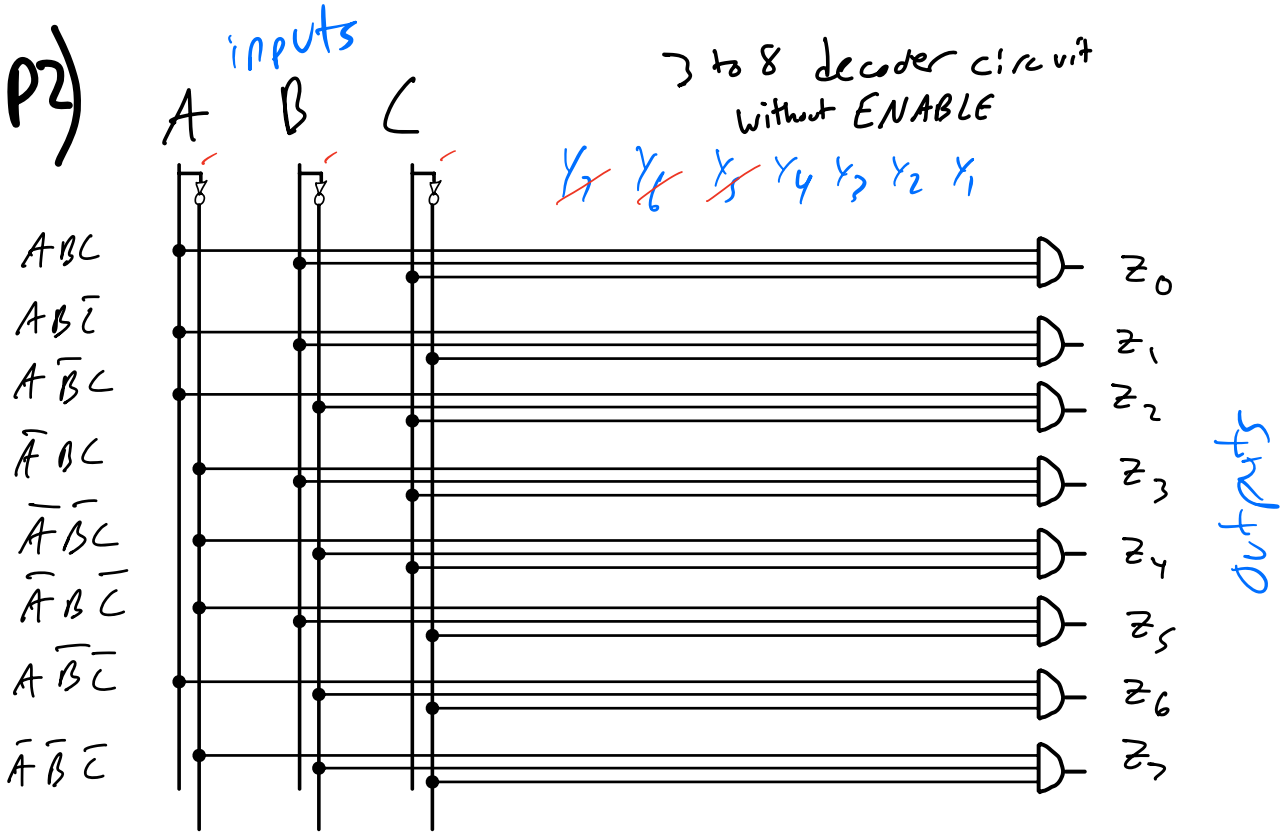
8/2 = 4 MUX
4/2 = 2 MUX
2/1 = 1 MUX

7 1bit 2to1 MUXs needed

d) 7 same

7 for 1bit 8:1 MUX
So 7 for 8 bit 2:1 MUX also

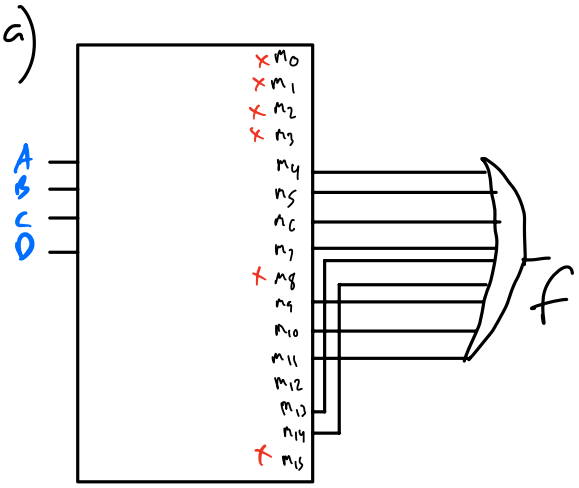
P2)



P3)

	a	b	c	d	f
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

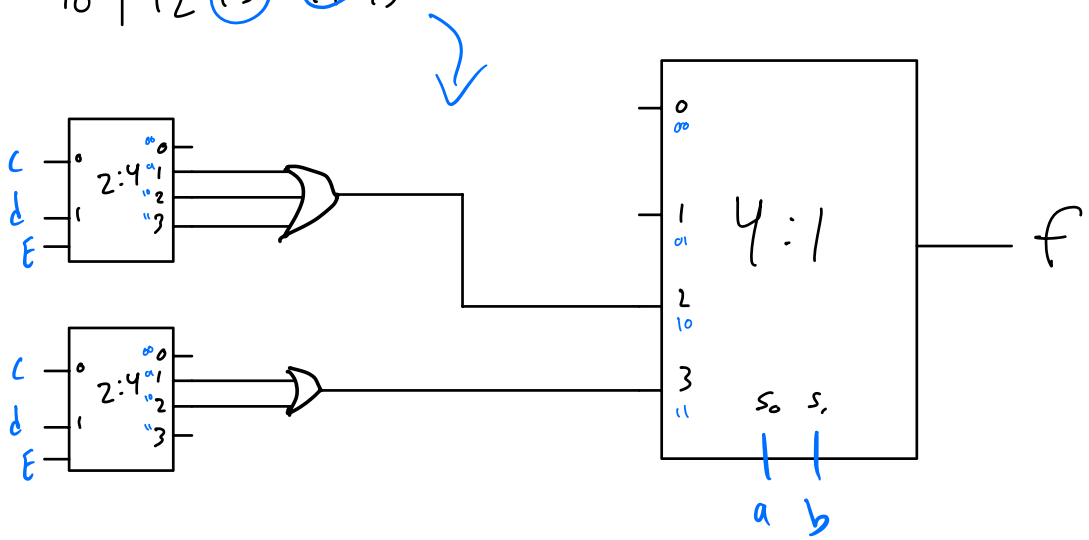
a)



$f(a,b,c,d) = \Sigma m(4,5,6,7,9,10,11,13,14)$

b) $f(a,b,c,d) = \Sigma m(4,5,6,7,9,10,11,13,14)$

ab \ cd	00	01	11	10
00	0	1	2	3
01	4	5	6	7
11	8	9	10	11
10	12	13	14	15



P4) a) One not gate using one 1-2 decoder

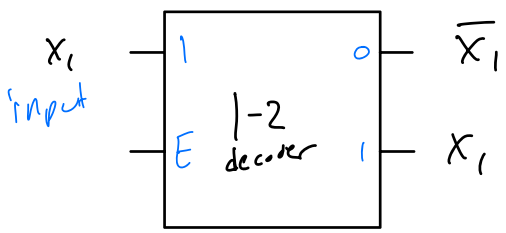
b) 3-input AND gate using two 1-2 decoders

c) One 2-input OR gate using four 1-2 decoders

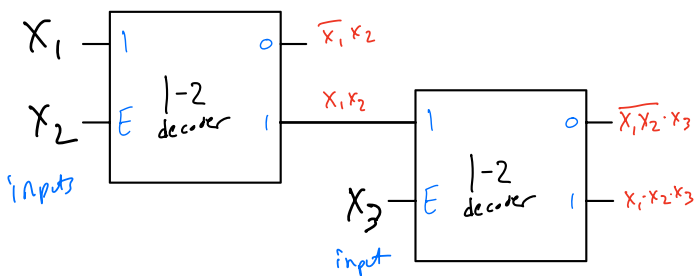
d) One 2-input NOR gate using one 2-4 decoder

instructions do not mention not being able to use ENABLERS

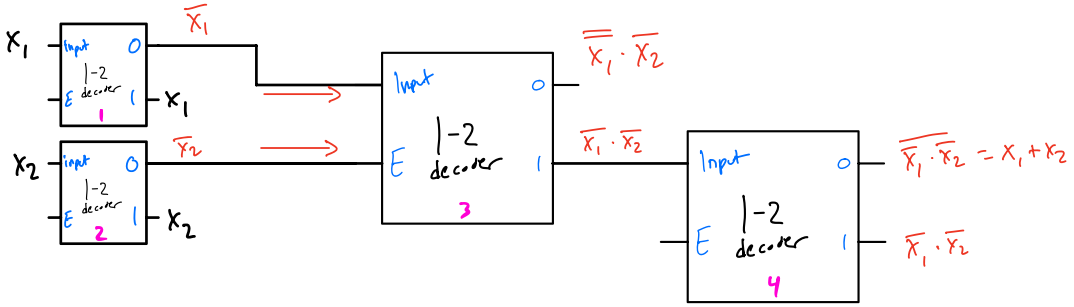
a)



b) three inputs



c) one 2-input OR gate and (4) 1-2 decoders



d) one 2-input NOR gate one 2-4 decoder