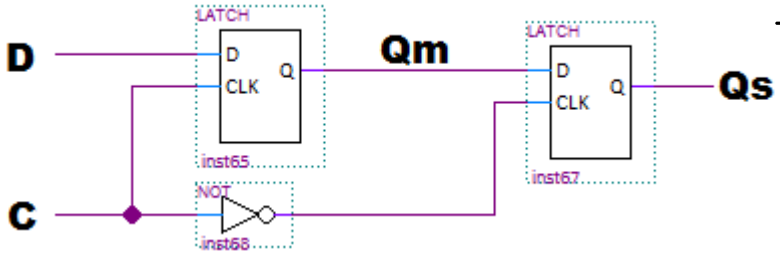
Cpr E 281 HW07
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Representation and Arithmetic
Assigned: Week 10

DONE

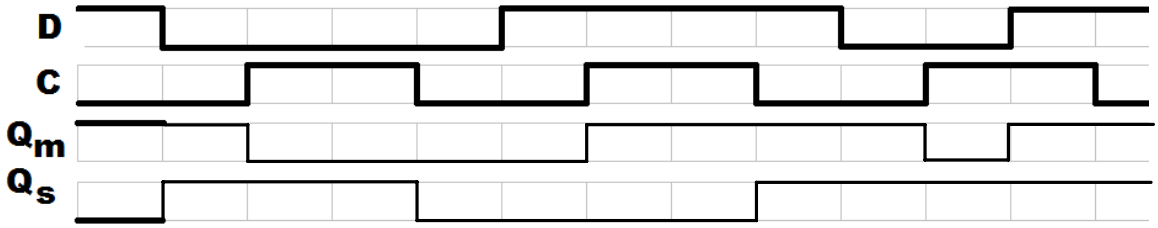
P1. (20 points): Answer the following questions based on the circuit shown below.



clk	D	Q
0	0	X
0	1	X
1	0	0
1	1	1

A. A: The latch that appears (twice) in the above circuit is a D Latch. Show the characteristic table for a D Latch.

B. B: Fill in the timing diagram for the values shown above.



below ↓

P2. (10 points): Show how a D Flip-Flop (DFF) can be made using a T Flip-Flop (TFF). Your circuit must contain all of the functionality of a DFF (PRESET and CLEAR implementations are not necessary), but must use only one TFF and one 2-1 MUX.

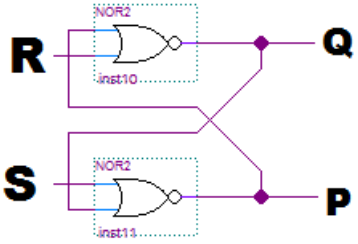
DONE

P3. (30 points): We want to create an LM-latch with the characteristic table shown below:

DONE

L	M	Q	P
0	0	0	1
0	1	No change	No change
1	0	No change	No change
1	1	1	0

A. Show the characteristic table for the SR Latch shown below.



S	R	Q	P
0	0	Memory	Memory
0	1	0	1
1	0	1	0
1	1	0	0

B. For each input combination to the LM-latch characteristic table shown above, write the values of S and R that will produce the output combinations. Then derive expressions for S and R in terms of L and M.

Below ↓

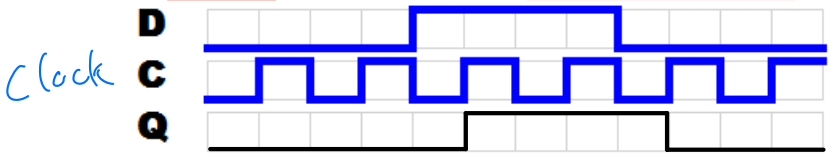
C. Draw the completed circuit for the LM-latch with the characteristic table based on the expressions derived in part B.

P4. (40 points): Complete the following timing diagrams for the specified components. The clock is C. You may assume that Q is initially at 0 unless specified otherwise.

DONE

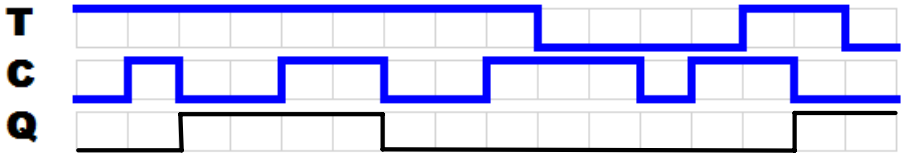
Q = 0

A. A positive-edge-triggered D Flip-Flop (DFF).

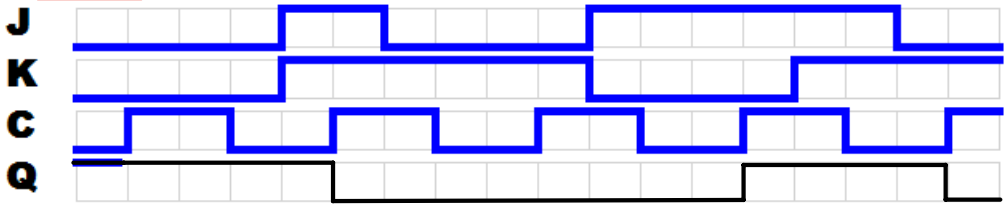


Clock

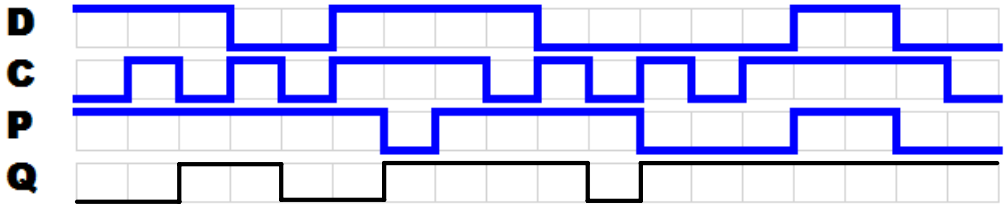
B. A negative-edge-triggered T Flip-Flop (TFF).



C. A positive-edge-triggered JK Flip-Flop (JKFF).



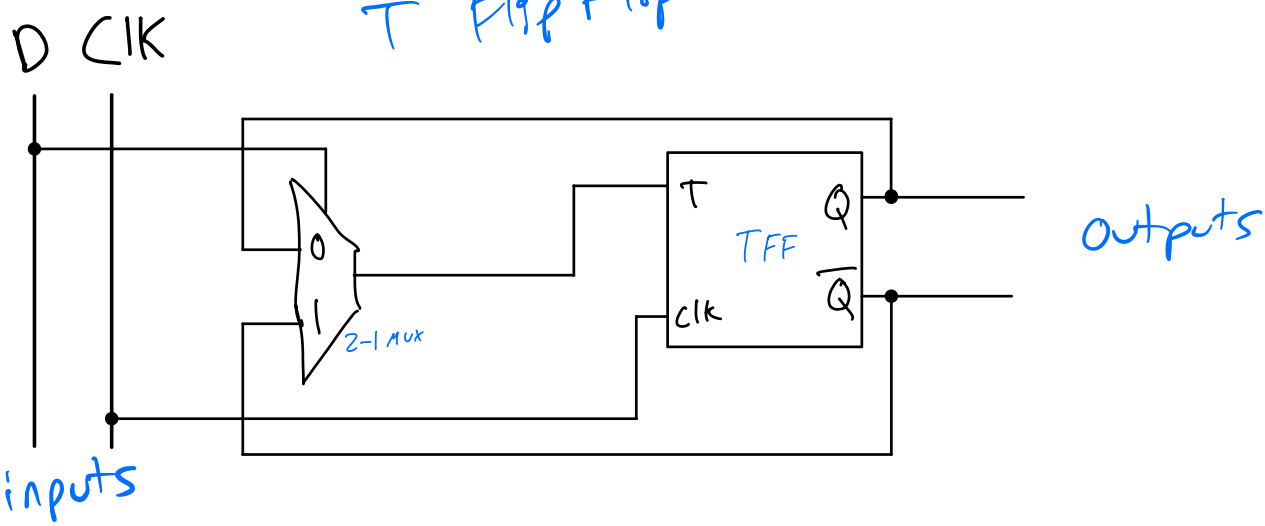
D. A negative-edge-triggered DFF with active-low Preset P (preset occurs when P=0).



p2)

0 0 0 0
0 1 0 1
1 0 1 1
1 1 1 0

T Flip flop



p3) Lm Latch

L	M	S	R	Q	P
0	0	0	1	0	1
0	1	0	0	X	X
1	0	0	0	X	X
1	1	1	0	1	0