Nick McCullough - ID: 950337388 - Lab Section 7

CprE 281 HW02

ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Design Examples, Intro to Verilog
Assigned Date: Third Week
Finish by Feb. 5, 2023

P1. (10 points) Write the corresponding Verilog symbol for the following terms:

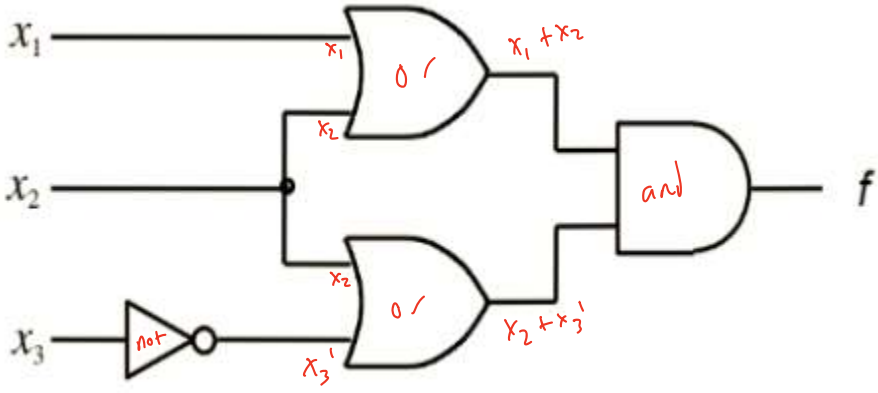
A. AND
B. OR
C. XOR
D. Complementation

a) &
b) |
c) ^
d) ~

P2. (10 points) Describe the difference between structural Verilog and behavioral Verilog

answers below

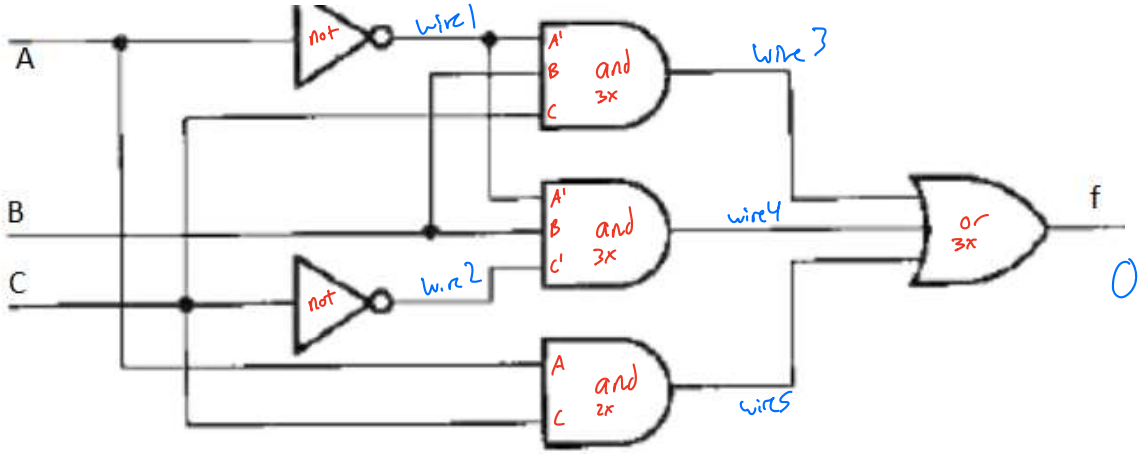
P3. (15 points) Write both the structural and behavioral Verilog code for the circuit shown below:



inputs

output

P4. (15 points) Write both the structural and behavioral Verilog code for the circuit shown below:



inputs

output

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P5. (15 points) Find the simplest SOP form of the following functions:

A. f(a) = Σ m(0,1)
B. f(a,b) = Σ m(1,2)
C. f(a,b,c) = Σ m(0,3,5,6)
D. f(a,b,c) = Σ m(1,3,4,5,6)
E. f(a,b,c,d) = Σ m(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13)

P6. (15 points) A four-variable logic function that is equal to 1 if any three or all four of its variables are equal to 1 is called a majority function. Design a minimum-cost SOP circuit that implements this majority function.

P7. (20 points) Derive a minimum-cost realization of the four-variable function that is equal to 1 if exactly two or three of its variables are equal to 1. Otherwise, it is equal to 0.

P2) – in structural Verilog, functions are designed using components, like logic gates, inverters, MUX. You will see "and" or "xor" for example to describe a process to carry out.

– Behavioral Verilog is like the name implies, it is used to describe the behavior of digital processes & circuits, it also has Continuous data flow & procedural data flow.

– Continuous uses terms such as "wire" and any input will affect the output immediately

– Procedural are not continuous & the data flow depends on specific order of events using blocks, such as "always" "sum" "carry" any variables defined as "reg" hold their value until it is assigned with a new value (unlike continuous)

p3)

Structural

```
module problem3s(x1,x2,x3,f);
input x1,x2,x3;
output f;
wire wire1,wire2,wire3;

not u1(wire1, x3);
or u2(wire2, x1, x2);
or u3(wire3, x2, wire1);
and u4(f, wire2, wire3);

endmodule
```

Behavioral

```
Module problem3b(x1,x2,x3,f);
input x1,x2,x3;
output reg f;

always @(*)
begin
f <= (x1|x2) & (x2|~x3);
end

endmodule
```

p4)

Structural

```
module problem4s (A, B, C, f)
input A, B, C;
output f;
wire wire1, wire2, wire3, wire4, wire5;

not u1 (wire1, A);
not u2 (wire2, B);
and u3 (wire3, wire1, B, C);
and u4 (wire4, wire1, B, wire2);
and u5 (wire5, A, C);
or u6 (f, wire3, wire4, wire5);

end module
```

Behavioral

```
module problem4b (A, B, C, f);
input A, B, C;
output f;

always @ (*)
begin

f <= ((~A & B & C) | (~A & B & ~C) | (A & C));

end

endmodule
```

P5)

A) f(a) = Σ m(0,1)

1

$f(a) = a' + a = 1$

B. f(a,b) = Σ m(1,2)

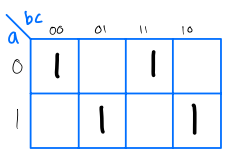
2

$f(a) = a'b + ab'$

Simplified: $a \oplus b$

C. f(a,b,c) = Σ m(0,3,5,6)

3



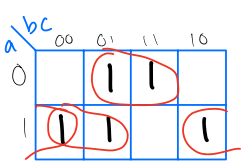
$f(a,b,c) = (a'b'c') + (a'bc) + (ab'c) + (abc')$

$b'(ac + a'c') + b(a'c + ac')$

$f(a,b,c) = b \oplus (a \odot c)$

D. f(a,b,c) = Σ m(1,3,4,5,6)

3

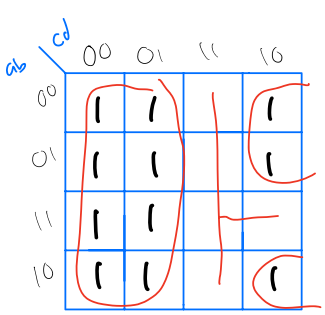


$f(a,b,c) = a'c + ab' + ac'$

$(a \oplus c) + ab'$

E. f(a,b,c,d) = Σ m(0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13)

4 3 7 11



$f(a,b,c,d) =$

$c' + b'd' + a'd'$

P6) 4 variable, any three or four are equal to 1

x1	x2	x3	x4	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

$\bar{x1}\,x2\,x3\,x4$

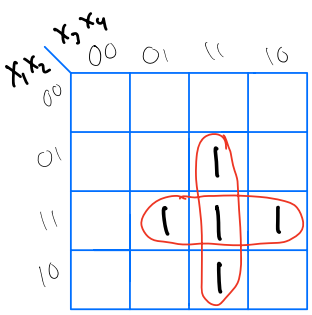
$x1\,\bar{x2}\,x3\,x4$

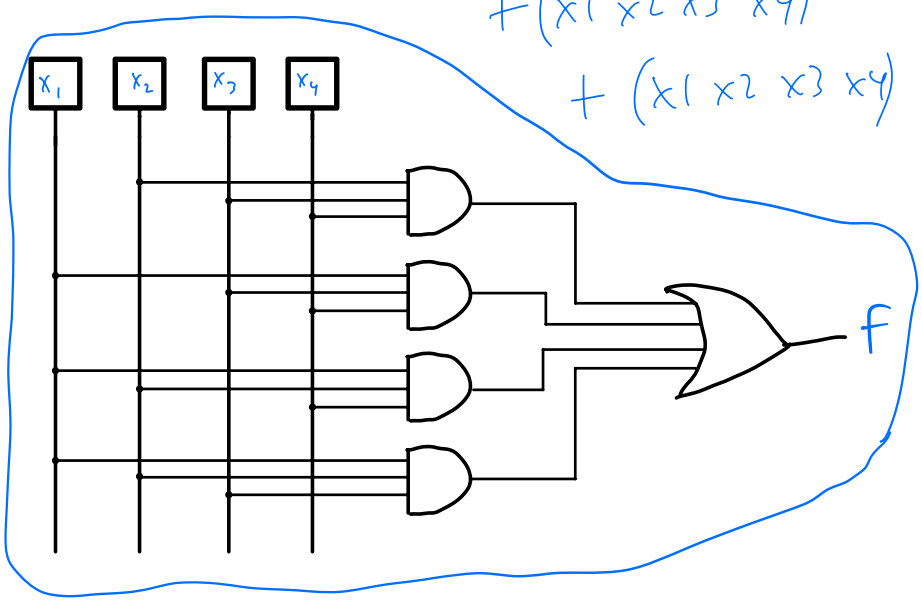
$x1\,x2\,\bar{x3}\,x4$

$x1\,x2\,x3\,\bar{x4}$

$x1\,x2\,x3\,x4$

$f = (\bar{x1}\,x2\,x3\,x4) + (x1\,\bar{x2}\,x3\,x4) + (x1\,x2\,\bar{x3}\,x4) + (x1\,x2\,x3\,\bar{x4}) + (x1\,x2\,x3\,x4)$



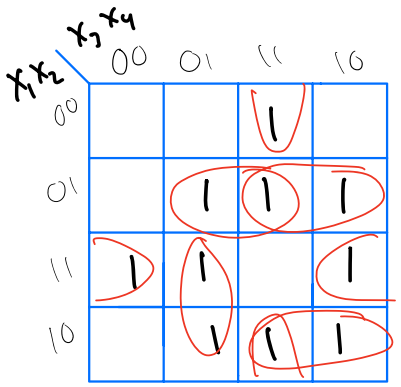


P7) 4 variables exactly 2 or 3 are equal to 1

x1	x2	x3	x4	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

$f(x1, x2, x3, x4) =$

$\Sigma m(3, 5, 6, 7, 9, 10, 11, 12, 13, 14)$



$f = (\overline{x1}\, x2\, x4) + (x1\, \overline{x3}\, x4) + (x1\, x2\, \overline{x4}) + (x1\, \overline{x2}\, x3) + (\overline{x1}\, x2\, x3) + (\overline{x2}\, x3\, x4)$

Question did not ask to draw circuit