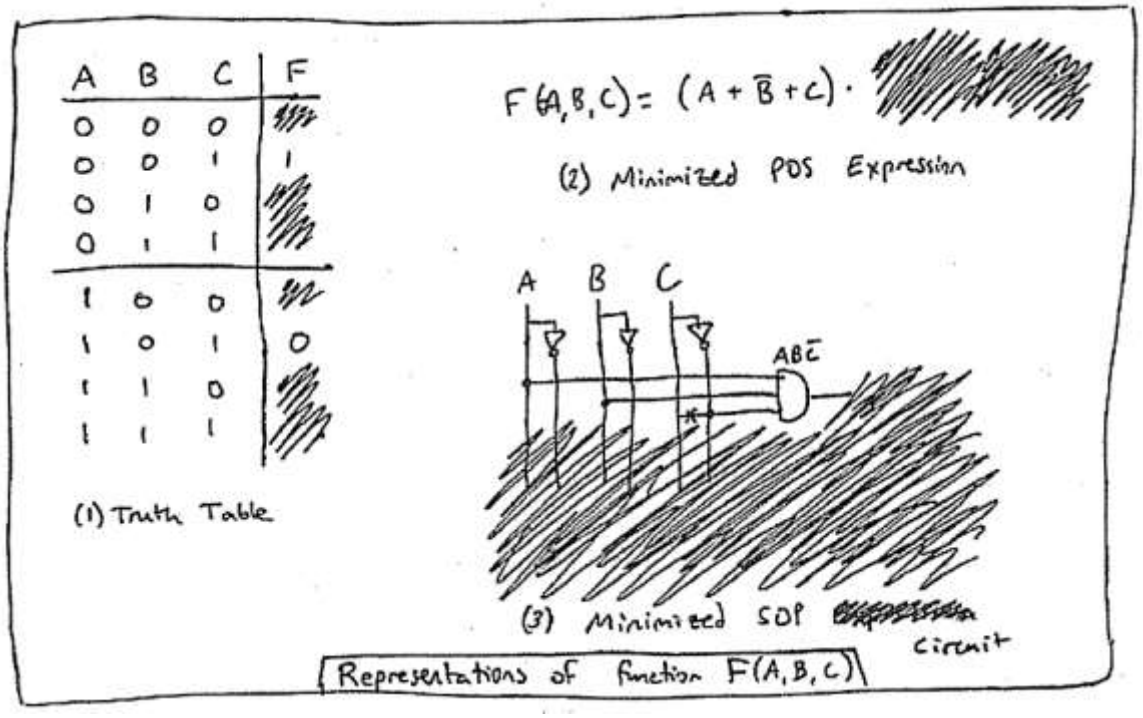
Cpr E 281 HW04
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Minimization and Karnaugh Maps
Assigned Date: Week 06
Due Date: Sunday, Feb. 26, 2023

P1. (4x4=16 points) You stumble across an old manuscript containing the following page, but some ink stains are obscuring part of the content. Deduce the function F(A,B,C) and write: a) the complete K-map; b) the complete truth table; c) the minimized POS expression; and d) the minimized SOP circuit diagram. Explain your reasoning.



Below

P2. (14 points) Design a circuit that accepts a 4-bit number X= $x_3x_2x_1x_0$ as input and generates a 1-bit output *P* that is equal to 1 if the input number is a prime. (0 and 1 are not prime; 2, 3, 5, etc., are prime.)

a) (7 points) Write down the truth table for the output *P*.
b) (7 points) Derive the simplest SOP expressions for the output *P*.

Below

P3. (20 points) Design a circuit that accepts a 3-bit number X= $x_2x_1x_0$ as input and generates a 6-bit number Y= $y_5y_4y_3y_2y_1y_0$ as output, which is equal to the square of the input number (i.e., $Y=X^2$).

a) (10 points) Write down the truth table for the six output lines $y_5y_4y_3y_2y_1y_0$ that jointly represent the number Y in binary.
b) (10 points) Derive the simplest SOP expressions for each bit of the output. That is, derive six expressions: one for y_5, another for y_4, and so on.

Below

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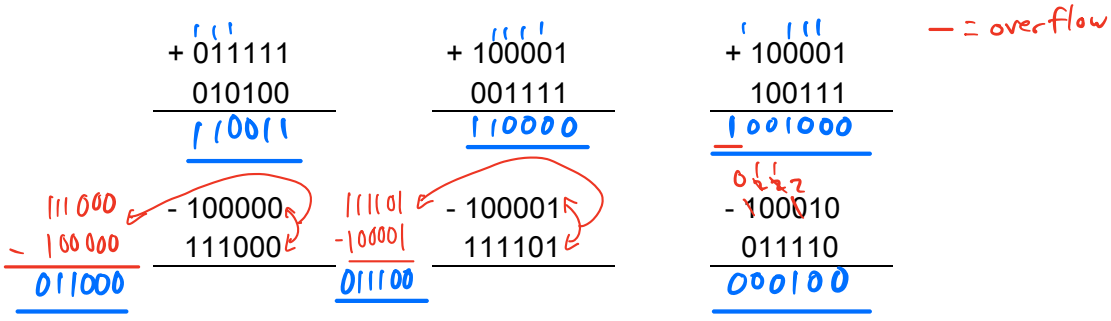
P4 (8 points): For the grid below, shade the boxes for each number in the column that can be represented with only 4-bits under the format for that particular row.

	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
Unsigned									■	■	■	■	■	■	■	■	
Sign & Magnitude						■	■	■	■	■	■	■					
1's Complement						■	■	■	■	■	■	■					
2's Complement					■	■	■	■	■	■	■	■					

P5 (12 points): Perform the following operations on the numbers and **indicate if overflow occurs** for each operation. All numbers are 6 bits wide (stored in 2's complement). Show your work and all carry bits.



P6 (16 points): Let A be a three-bit unsigned number. Use a seven-bit adder (and NOT gates, as necessary) to design a circuit that calculates the following operations. Note that the output may be assumed as unsigned, unless it is possible for the operation to produce a negative answer, in which case, the output must be correct in 2's complement:

a) **W = 3A + 1**
b) **X = 2A – 17**
c) **Y = 40A + 6**
d) **Z = 32 – 4A**

Below ↓

P7 (14 points): In the circuits below, find the algebraic expression for **B(X)** (B in terms of X) and **X(A)** (the expression for X in terms of A). Overflow is ignored, but all results that would produce overflow should not be accepted as an allowed value.
I: Here, A is a 5-bit unsigned integer, X is a 7-bit unsigned integer, and B is a 7-bit number in 2's complement.

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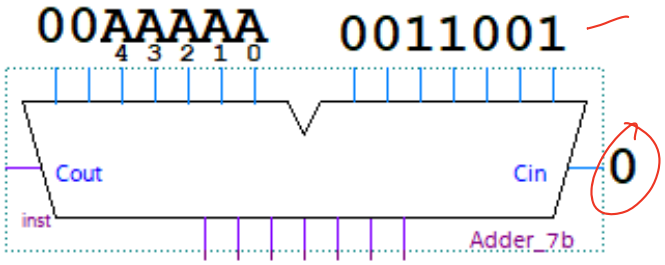
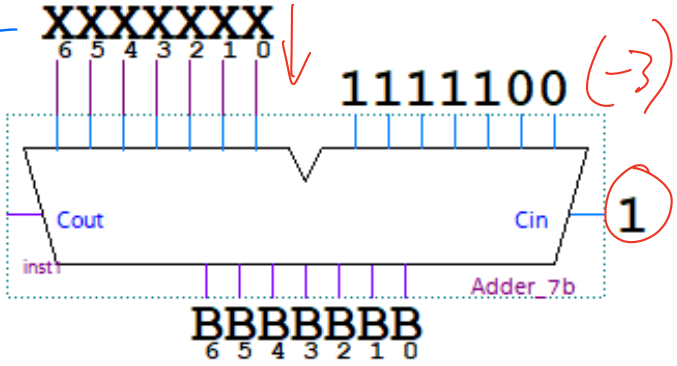
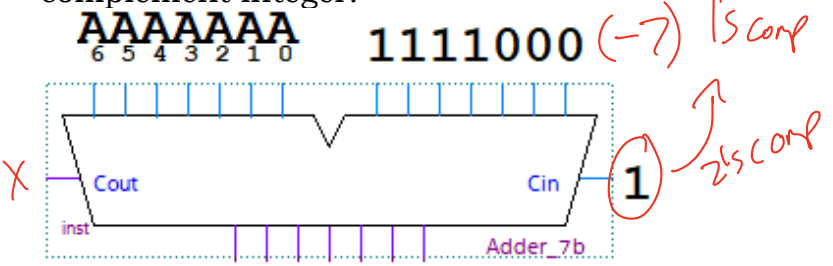


X=A+25

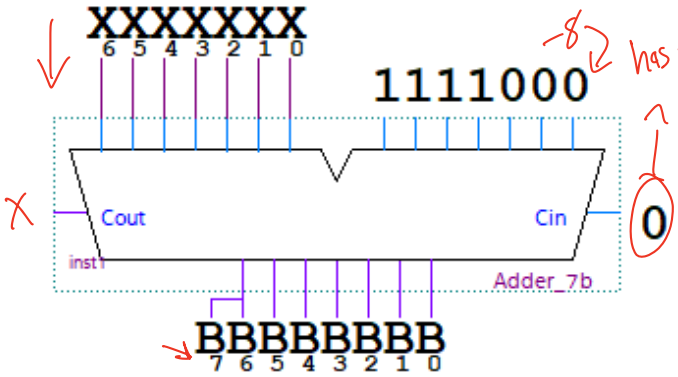


B = X-3

II: A and X are both 7-bit 2's complement integers, but B is an 8-bit 2's complement integer.



X = A-7



B = X-8

III: A is a 3-bit unsigned integer, X is an unsigned 7-bit integer, and B is an 8-bit unsigned number. Hint: identify the role of B_7 in the circuit.

B_7?

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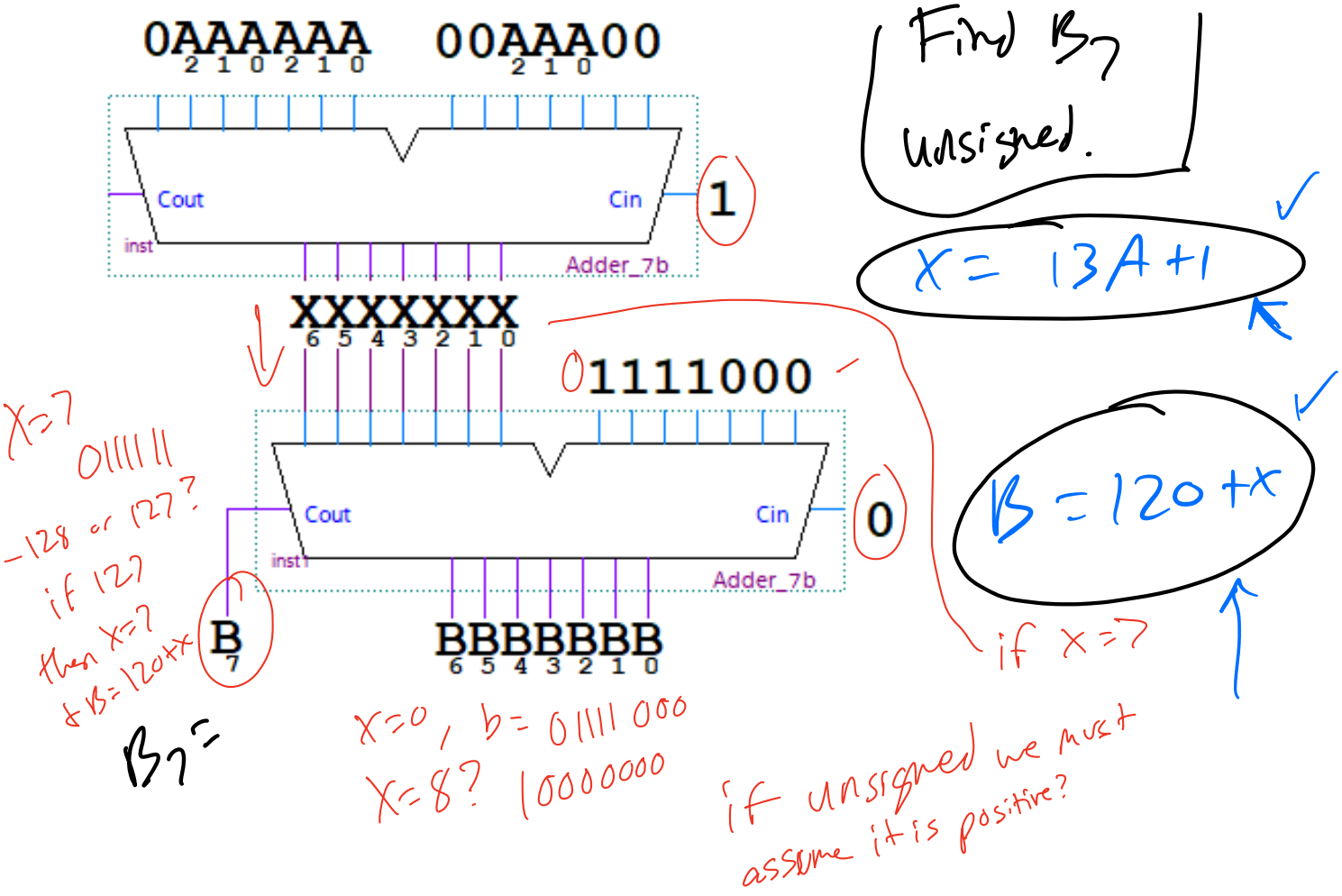
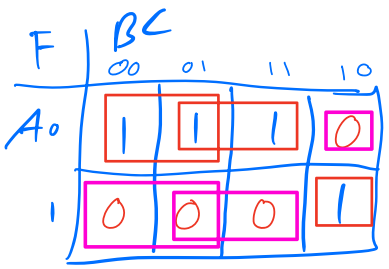


P1)

a)



b)

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

c) POS: $F(A,B,C) =$

$$(\bar{A}+B)(\bar{A}+\bar{C})(A+\bar{B}+C)$$

d) SOP: $F(A,B,C) =$

$$B\bar{C} + \bar{A}\bar{C} + A\bar{B}\bar{C}$$

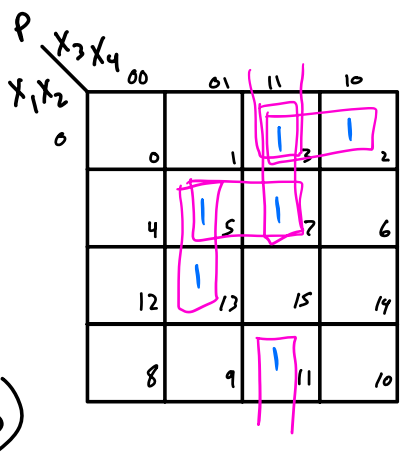
Based on the truth table, the POS express is based from graping the 0's together, SOP is graping the 1's together.

P2)

a)

	X_1	X_2	X_3	X_4	P
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	0

b)



$$\bar{A}\bar{B}C + \bar{A}CD + \bar{B}CD + B\bar{C}D$$

P3)

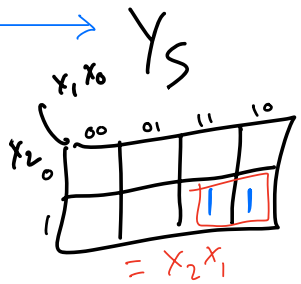
input three bit $X = X_2\ X_1\ X_0$

output six bit $Y = Y_5\ Y_4\ X_3\ Y_2\ Y_1\ Y_0$

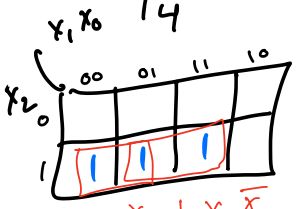
b) ↓

a)

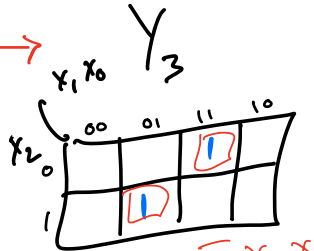
X_2	X_1	X_0	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1



$= X_2 X_1$



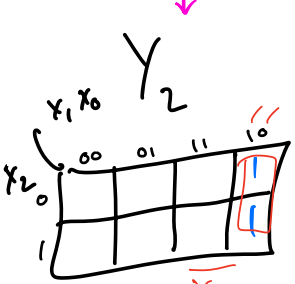
$= X_2 X_0 + X_2 \bar{X_1}$



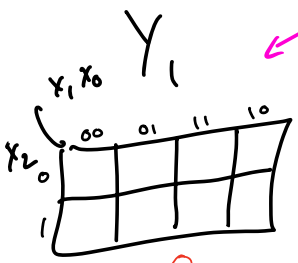
$X_2 \bar{X_1} X_0 + \bar{X_2} X_1 X_0$

or

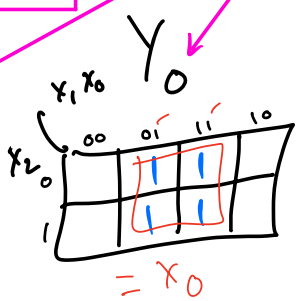
$X_0 (X_2 \oplus X_1)$



$= X_1 \bar{X_0}$



$= 0$



$= X_0$

P6)

7bit adder

$W = 3A + 1$ $\quad Y = 40A + 6$

$X = 2A - 17$ $\quad Z = 32 - 4A$

7bits

	6	5	4	3	2	1	0
A	0	0	0		A_2	A_1	A_0
2A	0	0		A_2	A_1	A_0	0
4A	0		A_2	A_1	A_0	0	0
8A		A_2	A_1	A_0	0	0	0
32A	A_2	A_1	A_0	0	0	0	0

A=3-bit #

V_1 V_2	F
00	Y
01	X
10	Z
11	W

using 4x1 MUX

7bit adder using 6 gates:

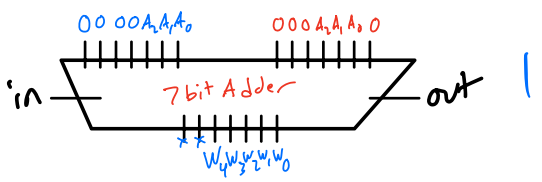
W: 2A + A + 1

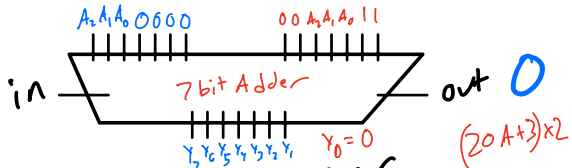
X: 2A - 17

Y: 32A + 8A + 6

Z: 32 - 4A

$W = 2A + A + 1$



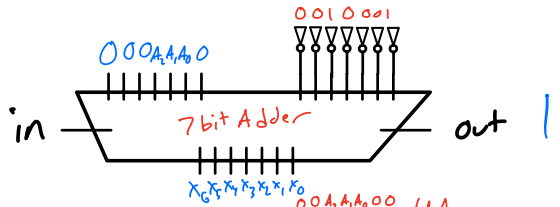


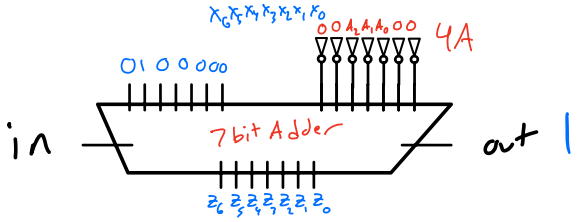
(20A+3)x2

$Y = 32A + 8A + 6$

Y is shifted due to carry.

$X = 2A - 17$





$Z = 32 - 4A$