Victor Croitoru

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EDUCATION

University of Illinois Chicago
Masters of Science in Electrical and Computer Engineering *August 2023 - Now*
Loyola University Chicago
Bachelors of Science in Computer Engineering *September 2019 – May 2023*

WORK EXPERIENCE

Intrinsic Quality LLC, Elk Grove Village, IL
Electronics Test Engineer *May 2023 - Now*

- Writing test specifications, statements of work, and procedures
- Designing schematics for test system hardware and wiring in Solidworks Electrical
- Creating of Custom PCB Boards for Instrument Control through Cadstar
- Developing software (C, C#, .net, XML, Python, SQL) to control instrumentation
- Composing documentation describing test design concepts and operator instructions
- Responsible for performing preliminary research resulting in a $300,000 project acquisition

Morton Arboretum, Lisle, IL
Communications Officer – *Technology Lead* *September 2022 - May 2023*

- Constructing a device within 2000$ budget capable of detecting movement and activity of Emerald Ash Bores larvae
- Ability to determine larvae death and difference in activity levels throughout test cycles
- Onboard processing to filter and distinguish larvae noise
- ESP32 microcontroller coded in C derivative Arduino IDE code with multiple sensors attached
- Created proxy to mimic EAB noise to test device
- Data is transferred over Wi-Fi to google sheets

Loyola University Chicago
Research Intern *May 2022 - August 2022*

- Designed force transducer holder for measuring muscle force
- Utilized Solidworks to create omnidirectional tower to hold force transducer

PROJECT EXPERIENCE

Final Project • MIPS Multi-Cycle CPU • UIC *April 2024 – May 2024*

- Designed and implemented a multicycle MIPS processor as a project, focusing on the controller and Datapath
- Utilized Quartus Prime Lite to implement SystemVerilog code a
- Developed control signals and FSM logic for the controller unit, ensuring accurate instruction execution
- Handled instructions such as add, sub, and, or, slt, lw, sw, beq, addi, and j
- Implemented the datapath unit, integrating key components like the register file, ALU, and memory
- Conducted thorough testing and debugging to verify the processor's functionality.

Lead • NN Digit Recognition with FPGA Displaying Output with ALU • UIC *September 2023 – December 2023*

- Developed TensorFlow model for live digit recognition using MNIST database
- Orchestrated Python-to-Arduino-to-FPGA communication for real-time data processing
- Implemented FPGA-based arithmetic operations with real-time display on DE1-SoC board
- Engineered live image capture and processing system with neural network classification display
- Github - https://github.com/Vcroitoru/NN-Digit-Recognition-with-FPGA-Displaying-Output

Intro to VLSI • MAC Datapath for Neural Networks • UIC *September 2023 – December 2023*

- Designed a MAC Datapath using 45nm CMOS for neural network applications in Cadence
- Implemented SRAM arrays, inverters, adders, multipliers, and registers for VLSI functionality
- Optimized for low power consumption while achieving 1 GHz clock frequency target
- Applied power-saving techniques to create an energy-efficient system meeting performance constraints

TECHNICAL SKILLS

Languages: C++; C#/.Net; Verilog/System Verilog; Python
Tools: Quartus; ModelSim; MATLAB/Simulink; Cadence; SolidWorks/SolidWorks Electrical; CADstar; LabVIEW; Microsoft Office