# Terence Zeng

980-505-4374 | terencezeng2004@gmail.com | linkedin.com/in/terence-zeng- | terencezeng6.github.io

### **EDUCATION**

## University of Illinois Urbana-Champaign

Expected Graduation Date: December 2025

Bachelor of Science in Computer Engineering, Minor in Mathematics

- GPA: 4.0 (Dean's List, James Scholar, Robert E. Lepic Electrical Engineering Scholarship)
- Relevant Coursework: Data Structures, Algorithms and Models of Computation, Operating Systems, Computer Systems and Programming, Artificial Intelligence, Digital Systems Laboratory (FPGA), Digital Signal Processing

## EXPERIENCE

### Course Assistant, ECE 374 (Algorithms and Models of Computation)

August 2024 – Present

ECE Department, University of Illinois Urbana-Champaign

- Facilitated weekly office hours to support students in developing a deeper, intuitive understanding of algorithms
- Offered personalized guidance and created original examples to help students build problem-solving skills
- Graded students' assignments and provided feedback on clarity and accuracy of solutions

# Embedded Software Engineering Intern

May 2024 – August 2024

Midea America Corporation (Fortune Global 500) - Louisville, KY

- Developed embedded software to interface temperature, humidity, and weight sensors with Arduinos using I2C protocol and custom DAC programming in C++, enhancing data accuracy by 25% and improving responsiveness
- Designed algorithms that reduced the magnitude of spin phase oscillations in washers, improving stability
- Prototyped circuit layouts and assisted in formulating patents in the research and development department

Intern July 2023

Guotai Junan Investments

- Automated parsing of options trading data to streamline decision-making and improve workflow efficiency
- Integrated tools such as Python, OpenPyXL, Pandas, and BeautifulSoup with internal email system

#### Projects

# Real-Time Speech Vocoder on FPGA | SystemVerilog, Vivado

- Designed a vocoder on a Spartan-7 FPGA, modifying and pitch-shifting speech with approximately a 100ms delay
- Calculated coefficients for band-pass FIR filters using FFT(Fast Fourier Transform), then modulated sine waves
- Converted mic input from 1-bit pulse-density modulation format to 8-bit pulse-code modulation, then to PWM
- Interfaced communication between various IP blocks with AXI protocol

## Website Portfolio | HTML, CSS, JavaScript

- Utilized HTML, CSS, and JavaScript to create website featuring projects and experience
- Includes resolution-adaptive image gallery with transitions, light/dark mode switch, popup boxes, etc.

## Machine Learning Facial Analysis Displayed on LED Matrix | TensorFlow, OpenCV, Google MediaPipe

- Consolidated microcontroller, LED system, and programs to develop project for Engineering Open House
- Detects facial features and emotional state of subjects and displays infographic on an embedded LED matrix, using tools such as TensorFlow, OpenCV, and Google MediaPipe computer vision framework

# Computerized Simulation of Binary Black Hole Trajectory | NumPy, Matplotlib

• Developed a Python (with NumPy, Matplotlib) program that simulated path of binary black hole system by calculating metrics such as energy and radii over time using data from LIGO observatory

# TECHNICAL SKILLS

Languages: Python, SystemVerilog, C, C++, Assembly (RISC-V), Java, JavaScript, HTML, CSS Tools: Git, Linux, Vivado, Vitis, Visual Studio, Google Cloud, PyCharm, IntelliJ, Eclipse, Quartus, Docker Libraries: PyTorch, TensorFlow, OpenCV, NumPy, SciPy, MatPlotLib, Pandas, BeautifulSoup, OpenPyXL

# ACTIVITIES

- UIUC Competitive Math ranked top 10 in UIUC undergraduate math contest, AIME qualifier x 5, HiMCM finalist
- Earthquake Engineering Research Institute AutoCAD specialist, committee member
- Open-Source @ Illinois Engineering Open House Project hardware subteam
- Association for Quantitative Trading Education