Erick Hillebrand

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EDUCATION

University of Chicago 2016 - 2018
MS, Computer Science

University of Illinois at Urbana-Champaign 2009 - 2012
BS, Electrical Engineering

EXPERIENCE

IMC Trading *(Leading Global Options Trading Firm)*
Software Engineer **May 2018 - Feb 2025**
Member of Execution Team for FICC/Index Options Desk

C++ Quoting Engine

- Quoting system implemented in C++ for ultra low latency and high throughput
- Worked with traders and devs to prioritize new features, identify bottlenecks, and monitor performance throughout the development and rollout
- Implemented core logic for tracking quotes in the market, including updating and canceling quotes and respecting exchange throttling constraints
- Designed and implemented end-to-end visibility for trade analysis, debugging, and performance monitoring. This visibility was used by traders and devs for investigations and to drive research for improvements and new features
- Created integration-level test framework and implemented tests
- Added support for SQF and ILink3 protocols

Cancel Engine Threshold Generation

- Owned, designed, and implemented system to dynamically update cancel thresholds based on quotes in the market
- Worked with traders to analyze and improve performance after rollout

Quoting Instruction Publisher

- Worked closely with traders to rapidly iterate on and refine quoting strategies
- Added additional visibility to allow traders to research new strategies

Protocol Compatibility Project

- Researched, designed and implemented forward compatibility support for IMC's proprietary protocol code generator, while evaluating potential open source alternatives
- Managed rollout of new features globally across all dev teams and offices

C++ Vol Adjustment Publisher

- Greenfield project to dramatically reduce amount of time required to adjust volatility based on market events
- Worked with quants to develop a new low latency algorithm for calculating and applying adjustments based on their research
- Worked with dev teams across the organization to design and build necessary support, configuration, and analysis components
- Provided continuing support locally after US rollout, as well as consulting with other offices on new features specific to other regions

Bazel Migration

- Migrated primary C++ repo to use Bazel, dramatically reducing build times and improving reliability and developer experience
- Designed and implemented buildfile generation tooling both to automate migration of new code and maintain buildfiles across the repo

Maxeler Technologies ***(High Performance Dataflow Computing)***
Software Engineer **July 2015 - March 2018**

DragonEye Project

- US Army project to create FPGA-accelerated framework for high throughput face detection and recognition system
- Developed custom H.264 video decoder in C to reduce load on face detection system for streaming video applications

Futures and Options Deployable Margin Library

Interest Rate Swap Deployable Margin Library

- Led joint project with the Chicago Mercantile Exchange to develop deployable financial risk analytic software applications in C++

Northrop Grumman ***(Aerospace and Defense)***
Embedded Software Engineer **June 2012 – July 2015**

Virtual Systems Integration Laboratory Software Team

EPAWSS/Commando II VSIL

- Created and developed new VSIL to support Eagle Passive/Active Warning & Survivability System (EPAWSS) project (DML)
- Prototyped new components and configurations of the EPAWSS system hardware for performance tests and software development purposes
- Secret Clearance

Professional Development Program

Rotation #4 – Systems Integration and Test Engineering
C-5/C-17 Large Aircraft Infrared Countermeasures (LAIRCM)

- Created unique Aircraft Characterization Modules for C-5B LAIRCM system

Rotation #3 – Engineering Project Management
Enhanced Missile Warning Sensor IO Card (EMWSIO)

- Worked with Extreme Engineering Solutions to debug EMWSIO PCIe connectivity issues (including travel to XES location)

Rotation #2 – Digital Hardware Engineering
APR-39D(V)2 Crystal Video Receiver Processor (CVRP)

- Created, synthesized, and simulated FPGA interface modules for Receivers and Low Band Array (VHDL)
- Integrated existing modules into PS FPGA and simulated full FPGA design

Rotation #1 – Software Engineering
LAIRCM System Processor Replacement (LSPR)

- Created software interface for low voltage power supply and microcontroller

SKILLS

Technical

- Performance analysis, benchmarking, processor architecture and cache-conscious programming, Solarflare kernel bypass, FPGA development

Finance

- Knowledge of market microstructure and exchange protocols
- Knowledge of options quoting and hitting systems
- FINRA Series 57 (Securities Trader)

Interpersonal

- Strong communication skills and problem solving skills, extensive experience working in interdisciplinary teams
- Works closely with traders and project stakeholders to plan and execute projects

Languages

- Extensive experience with modern C++, Java, C
- Moderate experience with Python, VHDL, x86 assembly, MIPS assembly