

ALINX FPGA BOARD

AX7010

User Manual



Revision History:

Revision	Description
1.0	First Release

Copyright Notice:

Copyright ©2018 by ALINX Technologies inc. All rights are reserved.

Development Environment:

Vivado 2015.4 is from Xilinx website

<https://www.xilinx.com>

Official website:

<Http://www.alinx.com.cn>

E-mail:

avic@alinx.com.cn

Tel:

+86-021-67676997

WeChat public number:

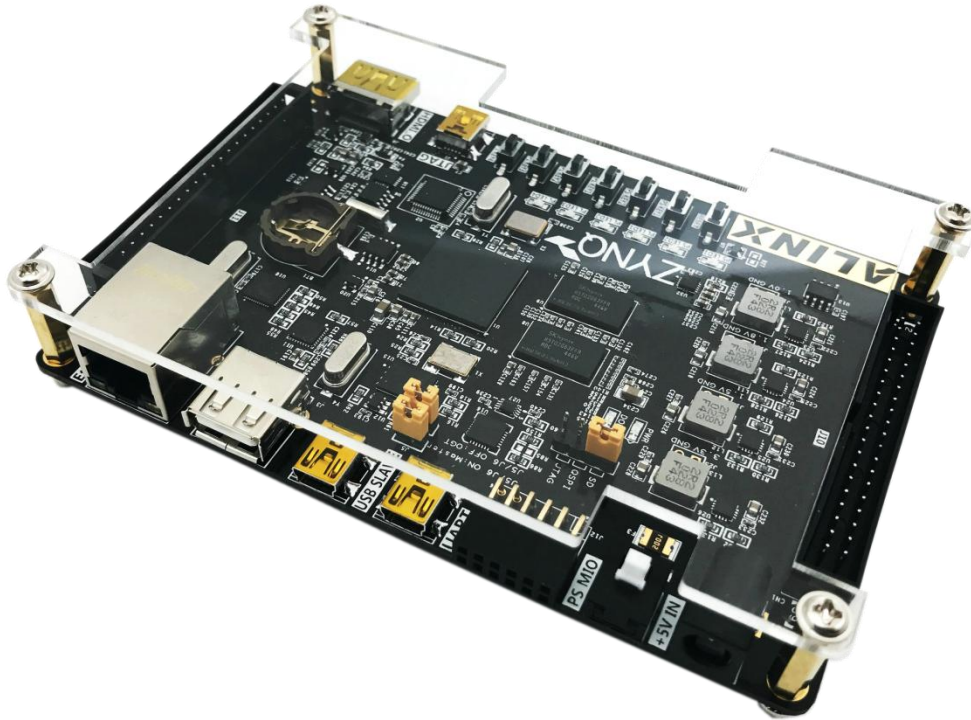
ALINX-HEIJIN



Contents

1. OVERVIEW	6
2. STRUCTURE SIZE	7
3. POWER.....	7
4. ZYNQ7000	9
4.1 JTAG	11
4.2 FPGA POWER SUPPLY SYSTEM	12
4.3 ZYNQ START CONFIGURATION	12
5. CLOCK CONFIGURATION.....	13
5.1 PS SYSTEM CLOCK SOURCE.....	13
5.2 PL SYSTEM CLOCK SOURCE.....	13
6. PS PERIPHERALS.....	14
6.1 QSPI FLASH.....	14
6.2 DDR3 DRAM	15
6.3 GIGABIT ETHERNET INTERFACE.....	17
6.4 USB2.0	18
6.5 USB TO UART	20
6.6 SD CARD SLOT.....	20
6.7 PS PMOD	21
6.8 USER LED	22
6.9 USER KEY	22
7. PL PERIPHERALS	23
7.1 HDMI	23
7.2 EEPROM	24
7.3 RTC	24
7.4 EXPANSION PORT J10	25
7.5 EXPANSION PORT J11	27
7.6 USER LED	28
7.7 USER KEY	29

This development platform is the solution of XILINX Zynq7000 SOC chip. It uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. It uses Xilinx's Zynq7000 series XC7Z010-1CLG400C as its core processor and has rich hardware resources and peripheral interfaces on ARM and FPGA, respectively. The design concept of “exquisite, practical and concise” is not only suitable for the software verification of the software staff, but also suitable for the hardware design of the hardware developer, that is, the system cooperation of software and hardware to speed up the development process of the project.



1. Overview

Here is a brief introduction to the Zynq7000 development platform AX7010.

This development board uses Xilinx's Zynq7000 series of chips, XC7Z010-1CLG400C, 400-pin FBGA package. The ZYNQ7000 chip can be divided into a processor system part Processor System (PS) and a programmable logic part Programmable Logic (PL). On the AX7010 development board, the PS and PL sections of the ZYNQ7000 are equipped with a wealth of external interfaces and devices to facilitate user use and functional verification. In addition, the Xilinx USB Cable Downloader circuit is integrated on the development board. Users can use a USB cable to download and debug the development board. Figure 1-2 shows the structure of the entire AX7010 system:

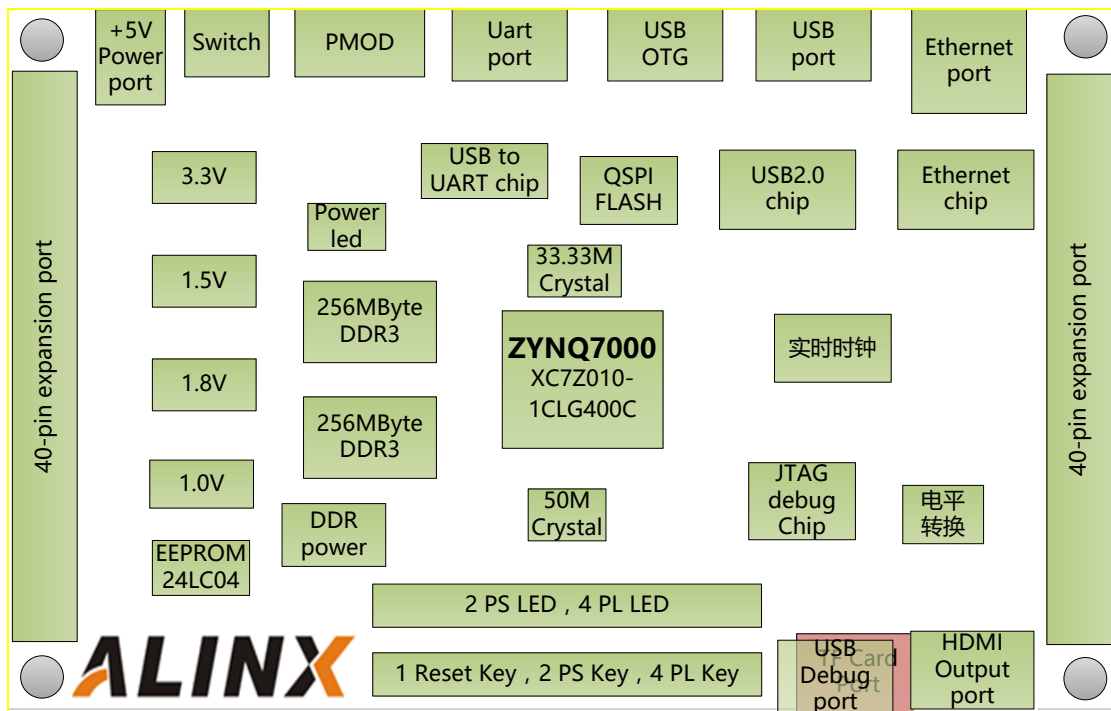


Figure1-1

Through Figure1-1 , we can see the interfaces and functions that our development platform can contain:

- +5V power input, maximum 2A current protection;
- Xilinx ARM+FPGA chip Zynq-7000 XC7Z010-1CLG400C
- Two high-capacity 2Gbit (4Gbit total) high-speed DDR3 SDRAMs, which can be used as cache for ZYNQ chip data or as operating system memory;
- 1 256Mbit QSPI FLASH, which can be used as ZYNQ chip system file and user data storage;
- 1 10/100M/1000M Ethernet RJ-45 interface, which can be used for Ethernet data exchange with computers or other network devices;
- 1 HDMI video input and output interface, can realize 1080P video image transmission;
- 1high-speed USB2.0 HOST interface, which can be used to connect USB peripherals such as mouse, keyboard, and USB flash drive to the development board;
- 1 high-speed USB2.0 OTG interface for OTG communication with PC or USB devices;
- 1y USB Uart interface for serial communication with PCs or external devices;
- 1RTC real-time clock with battery holder. The battery model is CR1220.

- 1 IIC interface EEPROM 24LC04;
- 6 users LED, 2 PS control, 4 PL control;
- 7 buttons, 1 CPU reset button, 2 PS control buttons, 4 PL control buttons;
- 1 on-board 33.333Mhz active crystal oscillator provides a stable clock source for the PS system. A 50MHz active crystal oscillator provides additional clocks for the PL logic.
- 2 40-pin expansion ports (2.54mm pitch) are used to expand the IO of the PL portion of the ZYNQ. Can be connected to 7-inch TFT module, camera module and AD/DA module and other expansion modules;
- 1 12-pin expansion port (2.54mm pitch) to extend the MIO of the ZYNQ PS system
- 1 USB JTAG port to debug and download the ZYNQ system through the USB cable and the onboard JTAG circuit
- 1 Micro SD card (back of the development board) is used to store the operating system image and file system.

2. Structure size

The size of the development board is 130mm x 90mm, and there are 4 screw positioning holes around the board, used to fix the development board, the hole diameter of the positioning hole is 3.5mm (diameter)

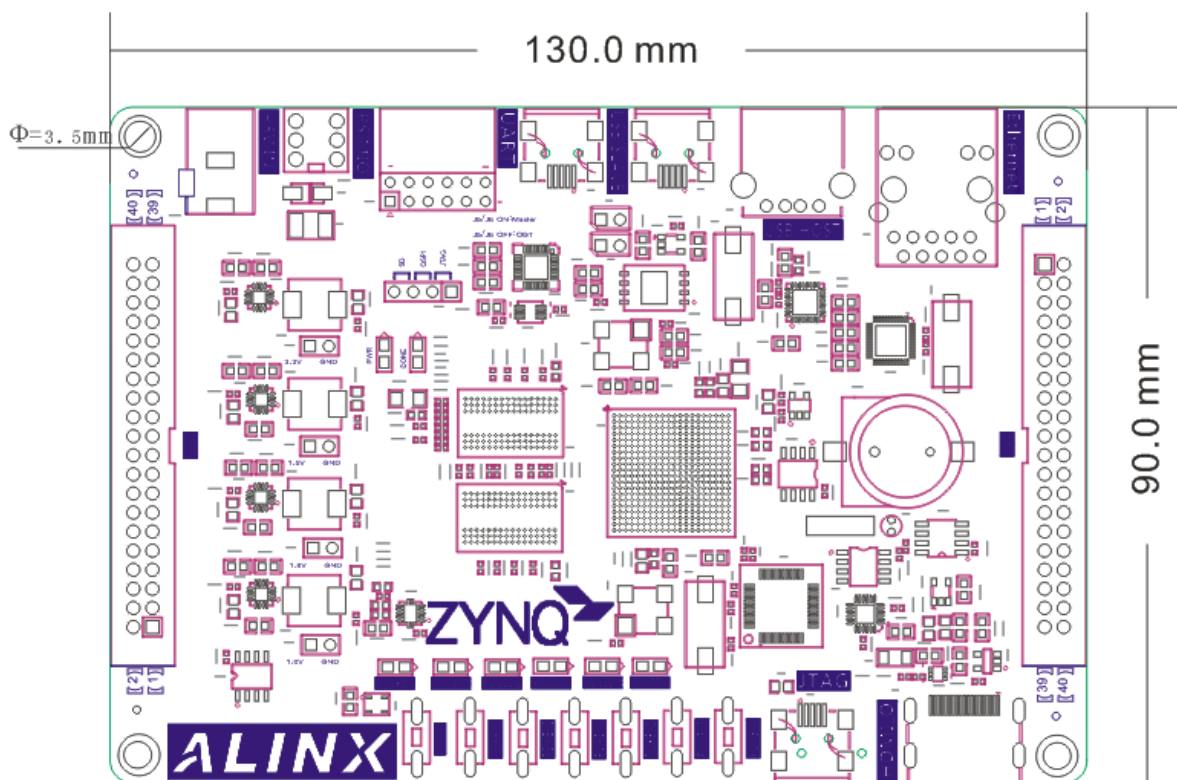


Figure2-1

3. Power

Power input: The power supply voltage of the development board is DC5V. Please use the power supply of the development board. Do not use other specifications of the power supply to avoid damaging the development board. The power supply design diagrams on the

development board are Figure 3-1:

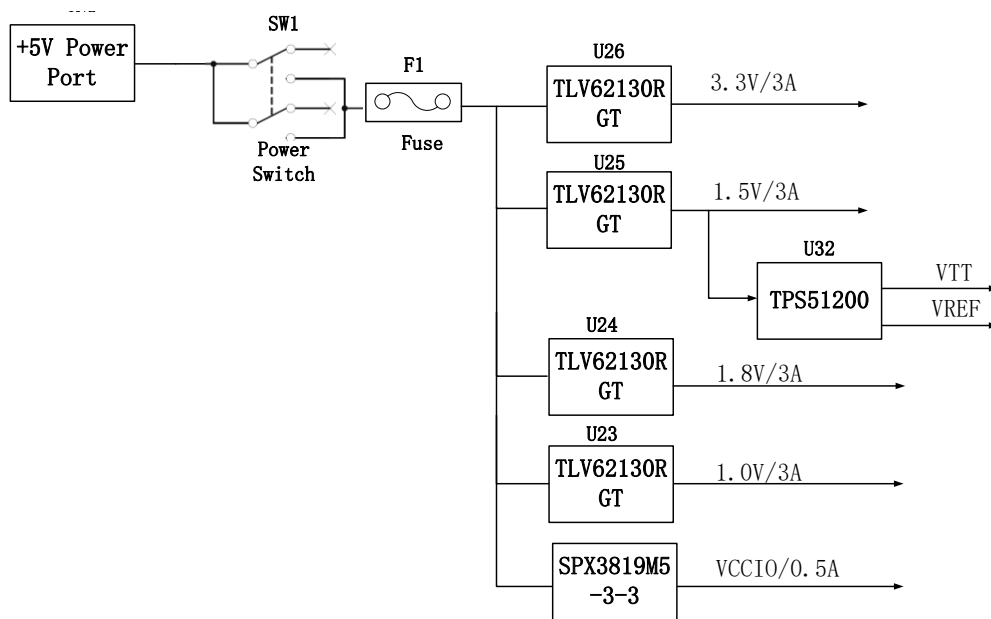


Figure 3-1

The development board is powered by +5V and is converted to +3.3V, +1.5V, +1.8V, +1.0V four-way power through four-way DC/DC power supply chip TLV62130RGT. Each output current can be as high as 3A. The VCCIO power is generated by all-way LDO SPX3819M5-3-3, VCCIO is the most power supply for BANK35 of ZYNQ. By replacing other LDO chips, the IO of BANK35 is adapted to different voltage standards. 1.5V generates the VTT and VREF voltages required for DDR3 through TI's TPS51200. The functions of each power distribution are shown in the following table:

Power	Function
+3.3V	ZYNQ VCCIO, Ethernet, Uart, HDMI, RTC, FLASH, EEPROM and SD card
+1.8V	ZYNQ Auxiliary voltage, ZYNQ PLL, ZYNQ Bank501 VCCIO, Ethernet, USB2.0
+1.0V	ZYNQ kernel voltage
+1.5V	DDR3, ZYNQ Bank502
VREF VTT	DDR3
VCCIO	ZYNQ Bank35

Table 3-1

Because the power supply of the PS and PL parts of ZYNQ has the power-on sequence requirements, we have designed according to the power requirements of ZYNQ in the circuit design. The order of power-up is 1.0V -> 1.8V -> 1.5V -> 3.3V -> VCCIO, Figure 3-2 shows the circuit design of the power supply:

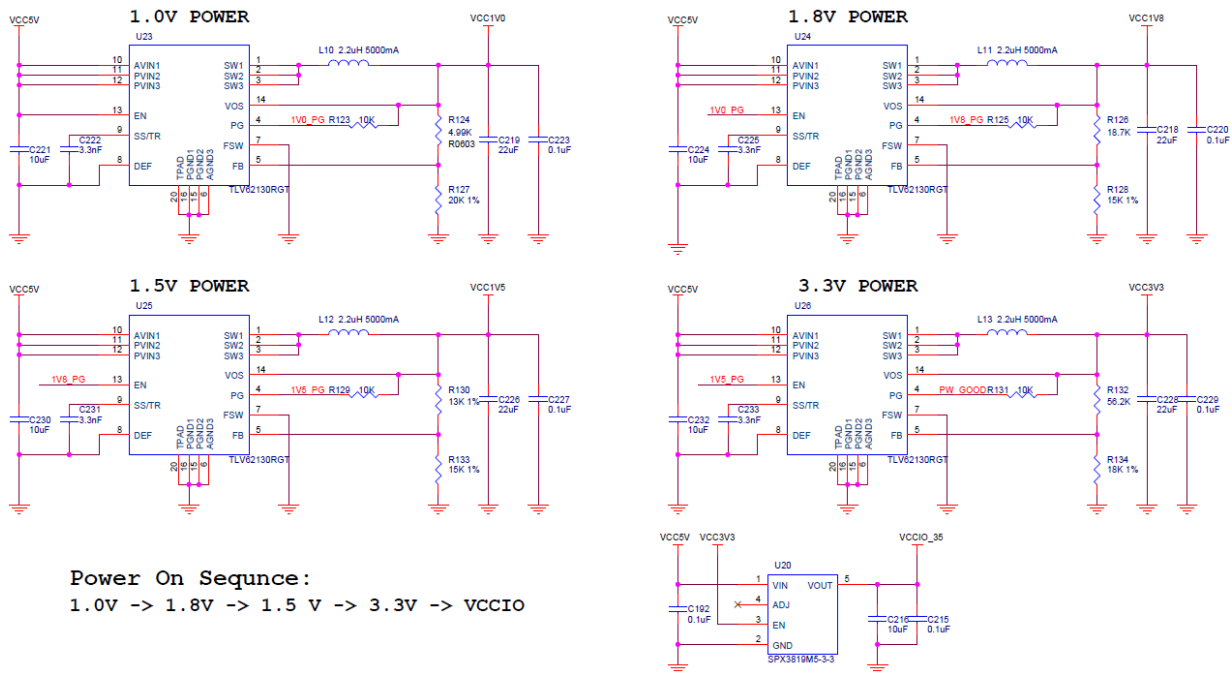


Figure 3-2

When designing the PCB, we use an 8-layer PCB, leaving an independent power plane and GND plane, making the power supply of the entire development board very stable. On the PCB, we set aside test points for each power supply so that the user can confirm the voltage on the board.

4. ZYNQ7000

The development board uses Xilinx's Zynq7000 series chip, XC7Z010-1CLG400C. The chip's PS system integrates two ARM Cortex™-A9 processors, AMBA® interconnects, internal memory, external memory interfaces, and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO and so on. The PS can operate independently and start on power-up or reset. The overall block diagram of the ZYNQ7000 chip is shown in Figure 4-1

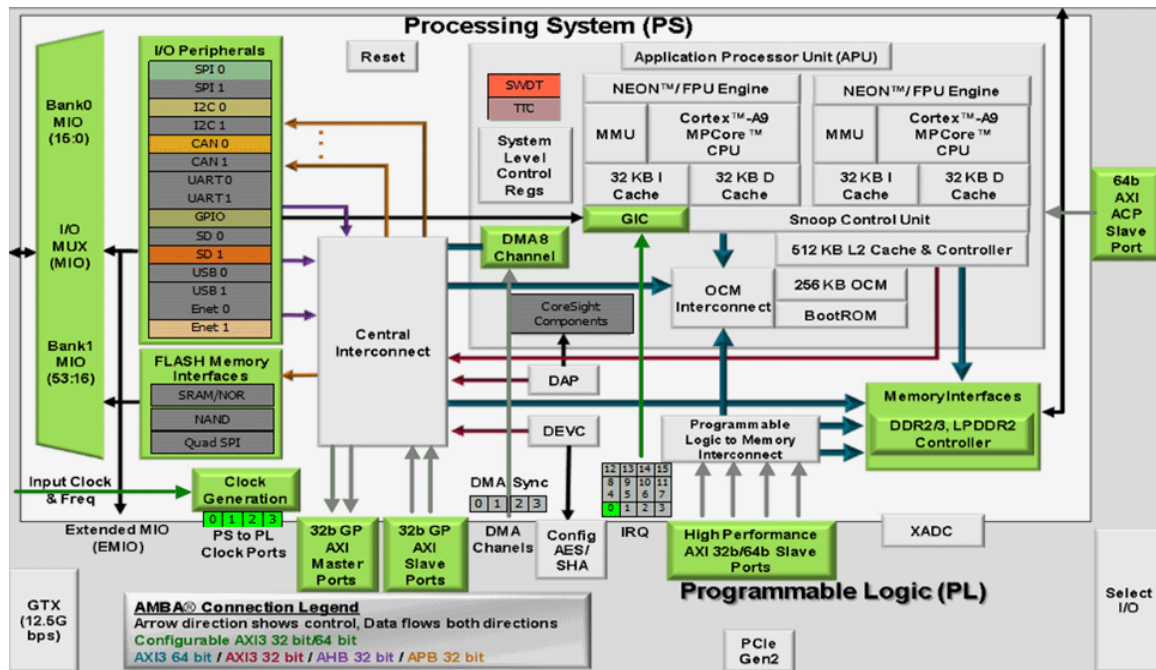


Figure 4-1

The main parameters of the PS system part are as follows:

- Application processor based on ARM dual core CortexA9
- 32KB Level 1 instruction and data cache per CPU, 512KB Level 2 cache shared by 2 CPUs
- On-chip boot ROM and 256KB on-chip RAM
- External memory interface supporting 16/32 bit DDR2 and DDR3 interfaces
- Two Gigabit LAN Support: Divergent-Aggregate DMA, GMII, RGMII, SGMII Interfaces
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers
- 2 SPIs, 2 UARTs, 2 I2C interfaces
- 4 sets of 32bit GPIO, 54 (32+22) as PS system IO, 64 connects to PL
- High-bandwidth connection within PS and PS to PL

The main parameters of the PL logic section are as follows:

- Logic Cells: 28K;
- Lookup table LUTs: 17600
- flip-flops: 35200
- Multiplier 18x25MACCs:80;
- Block RAM: 240KB;
- **Two AD converters** that can measure on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

The XC7Z010-1CLG400C is a BGA package with 400 pins and a pin pitch of 0.8mm. When we use the BGA packaged chip, the pin names are changed into letter + number, such as E3, G3, etc. Figure 4-2 shows the XC7Z010 chip physical map used for the development board.



Figure 4-2

4.1 JTAG

First of all, we talk about the JTAG debugging interface of AX7010 development board. JTAG download and debug circuit has been integrated on the circuit board, so users do not need to purchase additional Xilinx downloader. As long as a USB cable can be ZYNQ development and debugging. In the AX7010 development board through a FTDI USB bridge chip FT232HL PC USB and ZYNQ JTAG debug signals TCK, TDO, TMS, TDI for data communication. Figure 4-3 shows the schematic of the JTAG port on the development board:

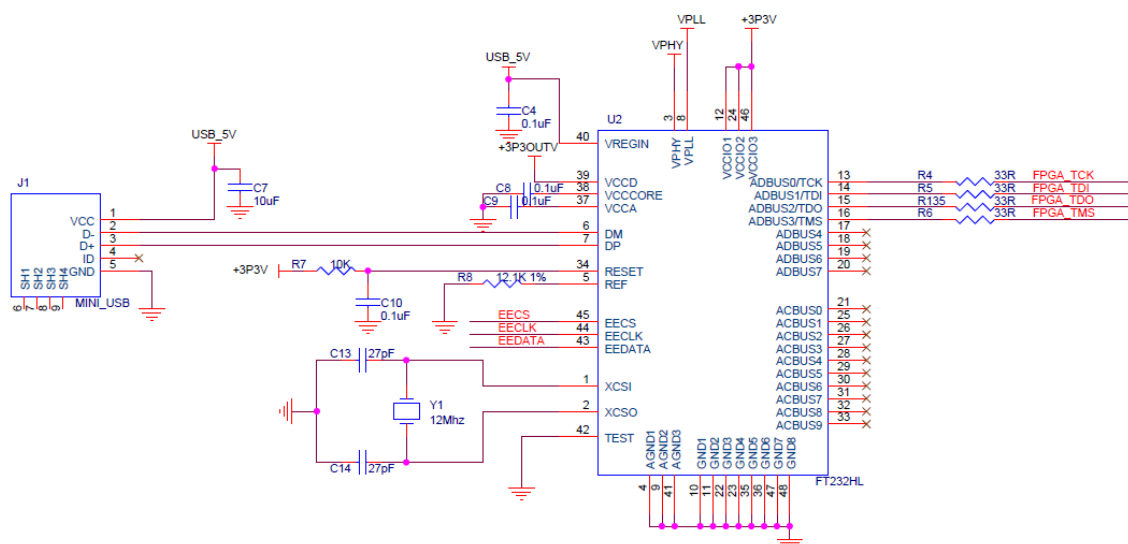


Figure 4-3

On the AX7010 development board, the JTAG interface is in the form of a USB interface. Users can use the USB cable provided to connect the PC and JTAG interfaces to perform ZYNQ system debugging.

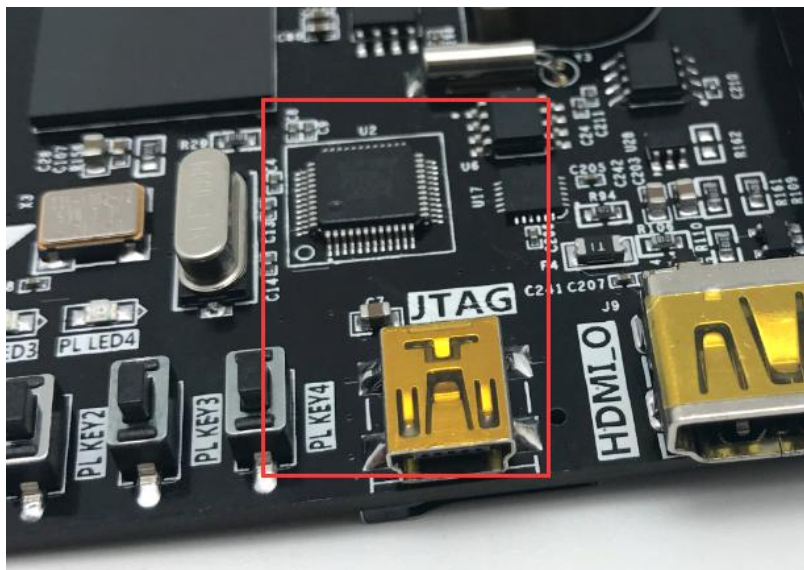


Figure 4-4

4.2 FPGA Power Supply System

Next, let's talk about the AX7010's power supply design section. The power supply of the ZYNQ chip is divided into a PS system part and a PL logic part, and the power of the two parts is independently operated. The power supply of the PS system part and the power supply of the PL logic part all have a power-up sequence. An abnormal power-up sequence may cause the ARM system and the FPGA system to fail to operate normally.

The power supplies for the PS section are VCCPINT, VCCPAUX, VCCPLL, and PS VCCO. VCCPINT is the power supply pin of PS core, and it is connected to 1.0V; VCCPAUX is the auxiliary power supply pin of PS system, which is connected to 1.8V; VCCPLL is the power supply pin of PS's internal clock PLL, which is also connected to 1.8V; PSVCCO is the voltage of BANK, including VCCO_MIO0, VCCO_MIO1, and VCCO_DDR, depending on the connected peripherals, the power supply connected will also be different. On the AX7010 development board, VCC_MIO0 is connected to 3.3V, VCCO_MIO1 is connected to 1.8V, and VCCO_DDR is connected to 1.5V. The PS system requires the power-on sequence to be VCCPINT power supply first, then VCCPAUX and VCCPLL, and finally PS VCCO. The order of power off is the opposite.

The power supply for the PL section is VCCINT, VCCBRAM, VCCAUX and VCCO. VCCPINT is the FPGA core power supply pin, connected to 1.0V; VCCBRAM is the FPGA block RAM power supply pin; 1.0V; VCCAUX is the FPGA auxiliary power supply pin, connected to 1.8V; VCCO is the voltage of each BANK PL, including BANK13, BANK34, BANK35, on the AX7010 development board, BANK voltage connection 3.3V. The PL system requires the power-on sequence to be VCCINT first, followed by VCCBRAM, then VCCAUX, and finally VCCO. If VCCINT and VCCBRAM have the same voltage, they can be powered on at the same time. The order of power off is the opposite.

4.3 ZYNQ Start configuration

The AX7010 development platform supports 3 boot modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the ZYNQ chip is powered on, it

will detect the level of the responding MIO port to determine which boot mode. Users can select different boot modes through the J13 jumper on the core board. The J13 startup mode is configured as shown in Table 4-1.

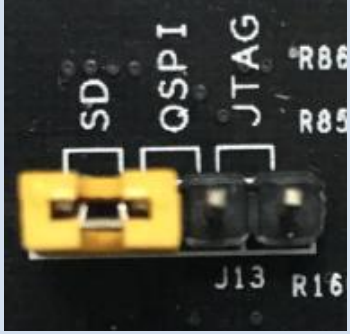
J13	Jump cap position	Startup mode
	Connect the two pins on the left side	SD Card
	Connect the two pins on the middle side	QSPI FLASH
	Connect the two pins on the right side	JTAG

Table 4-1

5. Clock configuration

The AX7010 development board provides active clocks for the PS system and the PL logic sections, respectively. It is the PS system and PL logic that can work independently.

5.1 PS System clock source

The ZYNQ chip provides a 33.333 MHz clock input to the PS section through the X1 crystal on the development board. The input of the clock is connected to the pins of PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 5-1:

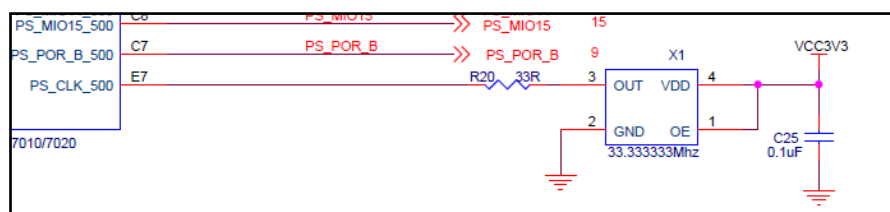


Figure 5-1

Clock pin assignment:

Signal Name	Pin
PS_CLK_500	E7

5.2 PL System clock source

The AX7010 development board provides a single-ended 50MHz PL system clock source with 3.3V supply. The crystal oscillator output is connected to the FPGA's global clock (MRCC), which can be used to drive the user logic within the FPGA. The schematic of this clock source is shown in Figure 5-2

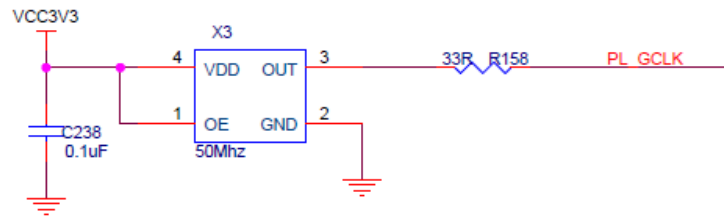


Figure 5-2

PL Clock pin assignment:

Signal Name	Pin
PL_GCLK	U18

6. PS Peripherals

Because ZYNQ is composed of the PS part of the ARM system and the PL part of the FPGA logic, some of the peripherals on the development board are connected to the IO of the PS, and some of the peripherals are connected to the IO of the PL of the development board. First of all, we introduce the peripherals connected to the PS section.

6.1 QSPI Flash

The development board has 1 256MBit Quad-SPI FLASH chip, W25Q256, which uses the 3.3V CMOS voltage standard. In use, it can be used as the boot device of the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific model and related parameters of QSPI FLASH are shown in Table 6-1.

Position	Model	Capacity	Factory
U6	W25Q256BV	32M Byte	Winbond

Table 6-1

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 6-1 shows the hardware connection diagram of QSPI Flash.

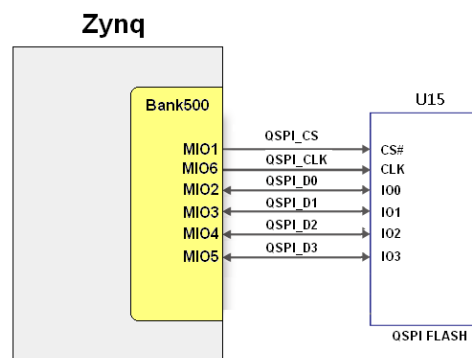


Figure 6-1

FLASH Pin Assignment:

Signal Name	Pin Name	Pin Number
QSPI_CLK	PS_MIO6_500	A5
QSPI_CS	PS_MIO1_500	A7
QSPI_D0	PS_MIO2_500	B8
QSPI_D1	PS_MIO3_500	D6
QSPI_D2	PS_MIO4_500	B7
QSPI_D3	PS_MIO5_500	A6

Table 6-2

6.2 DDR3 DRAM

The AX7010 development board is equipped with two SKHynix (Hynix) 2Gbit (512MB) DDR3 chips (4Gbit total), model number H5TQ2G63FFR (compatible with MT41J128M16RA-125). The DDR bus width is 32 bits in total. The maximum operating speed of DDR3 SDRAM is up to 533MHz (data rate 1066Mbps). The DDR3 memory system is directly connected to the memory interface of the BANK 502 of the ZYNQ processing system (PS). The specific configuration of DDR3 SDRAM is shown in Table 6-3.

Position	Model	Capacity	Factory
U8,U9	H5TQ2G63FFR-RDC	128M Byte*16bit	SKHynix

Table 6-3

The hardware design of DDR3 needs to strictly consider the signal integrity. We have fully considered the matching resistor/termination resistance, trace impedance control, and the length of the trace during the circuit design and PCB design to ensure the high-speed and stable operation of DDR3. The hardware connection of DDR3 DRAM is shown in Figure 6-2.

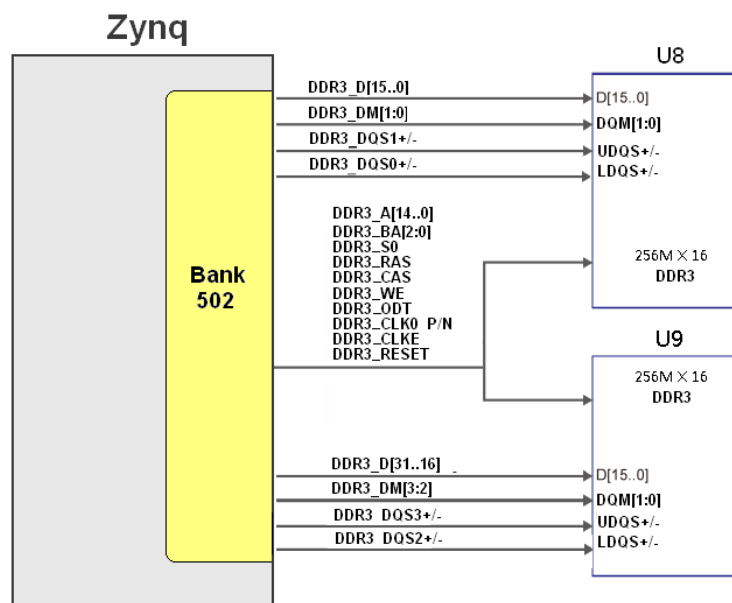


Figure 6-2

DDR3 DRAM Pin Assignment:

Signal Name	Pin Name	Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	B2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	G2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	F2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	R2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	T2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	W5
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W4
DDR3_DQ[0]	PS_DDR_DQ0_502	C3
DDR3_DQ [1]	PS_DDR_DQ1_502	B3
DDR3_DQ [2]	PS_DDR_DQ2_502	A2
DDR3_DQ [3]	PS_DDR_DQ3_502	A4
DDR3_DQ [4]	PS_DDR_DQ4_502	D3
DDR3_DQ [5]	PS_DDR_DQ5_502	D1
DDR3_DQ [6]	PS_DDR_DQ6_502	C1
DDR3_DQ [7]	PS_DDR_DQ7_502	E1
DDR3_DQ [8]	PS_DDR_DQ8_502	E2
DDR3_DQ [9]	PS_DDR_DQ9_502	E3
DDR3_DQ [10]	PS_DDR_DQ10_502	G3
DDR3_DQ [11]	PS_DDR_DQ11_502	H3
DDR3_DQ [12]	PS_DDR_DQ12_502	J3
DDR3_DQ [13]	PS_DDR_DQ13_502	H2
DDR3_DQ [14]	PS_DDR_DQ14_502	H1
DDR3_DQ [15]	PS_DDR_DQ15_502	J1
DDR3_DQ [16]	PS_DDR_DQ16_502	P1
DDR3_DQ [17]	PS_DDR_DQ17_502	P3
DDR3_DQ [18]	PS_DDR_DQ18_502	R3
DDR3_DQ [19]	PS_DDR_DQ19_502	R1
DDR3_DQ [20]	PS_DDR_DQ20_502	T4
DDR3_DQ [21]	PS_DDR_DQ21_502	U4
DDR3_DQ [22]	PS_DDR_DQ22_502	U2
DDR3_DQ [23]	PS_DDR_DQ23_502	U3
DDR3_DQ [24]	PS_DDR_DQ24_502	V1
DDR3_DQ [25]	PS_DDR_DQ25_502	Y3
DDR3_DQ [26]	PS_DDR_DQ26_502	W1
DDR3_DQ [27]	PS_DDR_DQ27_502	Y4
DDR3_DQ [28]	PS_DDR_DQ28_502	Y2
DDR3_DQ [29]	PS_DDR_DQ29_502	W3
DDR3_DQ [30]	PS_DDR_DQ30_502	V2
DDR3_DQ [31]	PS_DDR_DQ31_502	V3
DDR3_DM0	PS_DDR_DM0_502	A1
DDR3_DM1	PS_DDR_DM1_502	F1
DDR3_DM2	PS_DDR_DM2_502	T1
DDR3_DM3	PS_DDR_DM3_502	Y1
DDR3_A[0]	PS_DDR_A0_502	N2

DDR3_A[1]	PS_DDR_A1_502	K2
DDR3_A[2]	PS_DDR_A2_502	M3
DDR3_A[3]	PS_DDR_A3_502	K3
DDR3_A[4]	PS_DDR_A4_502	M4
DDR3_A[5]	PS_DDR_A5_502	L1
DDR3_A[6]	PS_DDR_A6_502	L4
DDR3_A[7]	PS_DDR_A7_502	K4
DDR3_A[8]	PS_DDR_A8_502	K1
DDR3_A[9]	PS_DDR_A9_502	J4
DDR3_A[10]	PS_DDR_A10_502	F5
DDR3_A[11]	PS_DDR_A11_502	G4
DDR3_A[12]	PS_DDR_A12_502	E4
DDR3_A[13]	PS_DDR_A13_502	D4
DDR3_A[14]	PS_DDR_A14_502	F4
DDR3_BA[0]	PS_DDR_BA0_502	L5
DDR3_BA[1]	PS_DDR_BA1_502	R4
DDR3_BA[2]	PS_DDR_BA2_502	J5
DDR3_S0	PS_DDR_CS_B_502	N1
DDR3_RAS	PS_DDR_RAS_B_502	P4
DDR3_CAS	PS_DDR_CAS_B_502	P5
DDR3_WE	PS_DDR_WE_B_502	M5
DDR3_ODT	PS_DDR_ODT_502	N5
DDR3_RESET	PS_DDR_DRST_B_502	B4
DDR3_CLK_P	PS_DDR_CKP_502	L2
DDR3_CLK_N	PS_DDR_CKN_502	M2
DDR3_CKE	PS_DDR_CKE_502	N3

6.3 Gigabit Ethernet interface

The AX7010 development board provides users with network communication services through the Realtek RTL8211E-VL Ethernet PHY chip. The Ethernet PHY chip is connected to the GPIO interface of the BANK501 on the PS side of ZYNQ. The RTL8211E-VL chip supports 10/100/1000 Mbps network transfer rate and communicates with the Zynq7000 PS system's MAC layer through the RGMII interface. The RTL8211E-VL supports MDI/MDX adaptation, various speed adaptations, Master/Slave adaptation, and MDIO bus support for PHY register management. The RTL8211E-VL power-on detects certain IO level conditions to determine its own operating mode. Table 6-4 describes the default settings after the GPHY chip is powered on.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 001
SELRGV	RGMII 1.8V or 1.5V level selection	1.8V
AN[1:0]	Auto-negotiation configuration	(10/100/1000M) Adaptive
RX Delay	RX clock 2ns delay	delay
TX Delay	TX clock 2ns delay	delay

Table 6-4

When the network is connected to Gigabit Ethernet, the data transmission of the FPGA and PHY chip RTL8211E-VL is through the RGMII bus communication, the transfer clock is 125Mhz, the data is sampled at the rising and falling clock samples.

When the network is connected to Fast Ethernet, the data transmission of the FPGA and PHY chip RTL8211E-VL is through the RMII bus communication, transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

Figure 6-3 shows the connection between the ZYNQ and the Ethernet PHY chip:

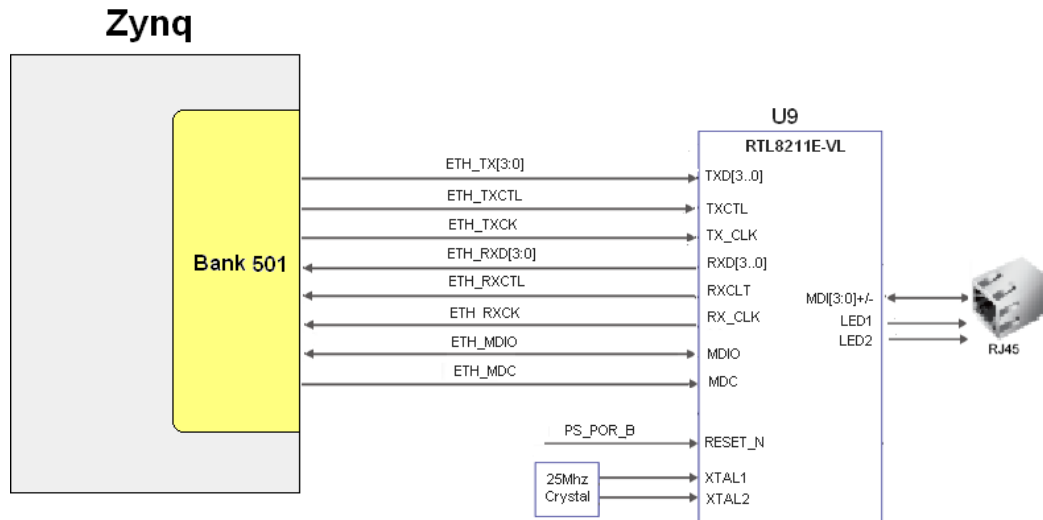


Figure 6-3

Ethernet Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
ETH_GCLK	PS_MIO16_501	A19	RGMII Send clock
ETH_TXD0	PS_MIO17_501	E14	Send data bit 0
ETH_TXD1	PS_MIO18_501	B18	Send data bit1
ETH_TXD2	PS_MIO19_501	D10	Send data bit2
ETH_TXD3	PS_MIO20_501	A17	Send data bit3
ETH_TXCTL	PS_MIO21_501	F14	Send enable signal
ETH_RXCK	PS_MIO22_501	B17	RGMII Receive clock
ETH_RXD0	PS_MIO23_501	D11	Receive data Bit0
ETH_RXD1	PS_MIO24_501	A16	Receive data Bit1
ETH_RXD2	PS_MIO25_501	F15	Receive data Bit2
ETH_RXD3	PS_MIO26_501	A15	Receive data Bit3
ETH_RXCTL	PS_MIO27_501	D13	Receive data valid signal
ETH_MDC	PS_MIO52_501	C10	MDIO Management clock
ETH_MDIO	PS_MIO53_501	C11	MDIO Management clock

6.4 USB2.0

The USB2.0 transceiver used by the AX7010 is a 1.8V, high-speed USB3320C-EZK that supports the ULPI standard interface. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver to enable high-speed USB2.0 Host and Slave mode data

communications. The data and control signals of the USB3320C USB are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. A 24 MHz crystal provides the system clock to the USB3320C.

The development board provides users with two USB ports, one is the Host USB port and the other is the Slave USB port. They are USB Type A and Micro USB, which allow users to connect different USB peripherals. Users can switch between Host and Slave through J5 and J6 jumpers on the development board. Table 6-5 shows the mode switching instructions:

J5, J6 state	USB mode	Explain
Installed	HOST	Development board as a master device, USB port to connect mouse, keyboard, USB, etc. slave peripherals
Not installed	OTG/Slave	Development board as a slave device, USB port to connect the computer

Table 6-5

Figure 6-4 shows the connection between the ZYNQ processor and the USB3320C-EZK chip.

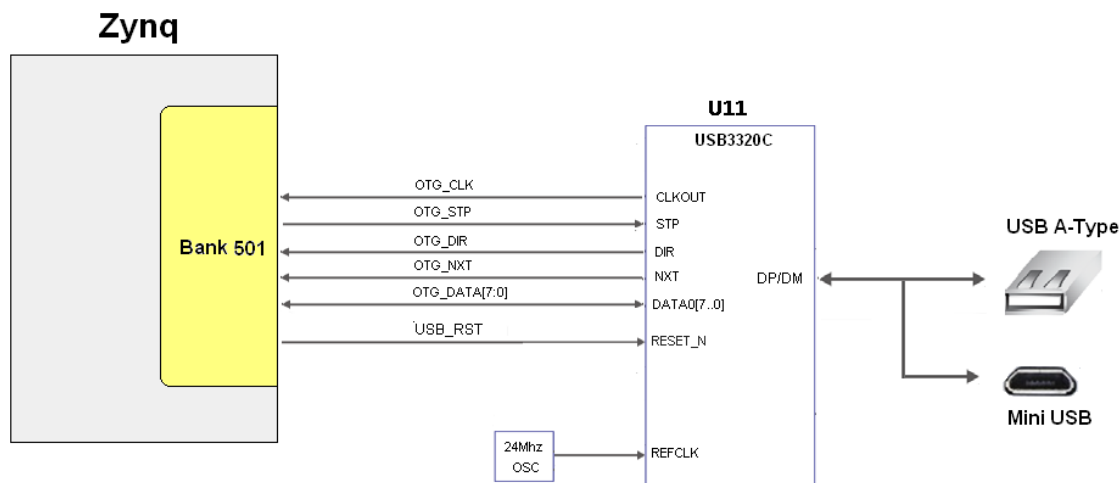


Figure 6-4

USB2.0 Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
OTG_DATA4	PS_MIO28_501	C16	USB data bit4
OTG_DIR	PS_MIO29_501	C13	USB data direction signal
OTG_STP	PS_MIO30_501	C15	USB stop signal
OTG_NXT	PS_MIO31_501	E16	USB next data signal
OTG_DATA0	PS_MIO32_501	A14	USB data bit0
OTG_DATA1	PS_MIO33_501	D15	USB data bit1
OTG_DATA2	PS_MIO34_501	A12	USB data bit2
OTG_DATA3	PS_MIO35_501	F12	USB data bit3
OTG_CLK	PS_MIO36_501	A11	USB clock signal

OTG_DATA5	PS_MIO37_501	A10	USB data bit5
OTG_DATA6	PS_MIO38_501	E13	USB data bit6
OTG_DATA7	PS_MIO39_501	C18	USB data bit7
OTG_RESETN	PS_MIO46_501	D16	USB reset signal

6.5 USB to Uart

The AX7010 development board uses the USB to UART chip of Silicon Labs CP2102GM. The USB interface uses the Mini USB interface. Users can use a Mini USB cable to connect to the PC for serial communication.

The TX/RX signal of the UART is connected to the signal of the PS BANK501 of the ZYNQ EPP. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the CP2102GM is 3.3V, we connect here through the TXS0102DCUR level conversion chip.

Figure 6-5 shows the connection between CP2102GM and ZYNQ:

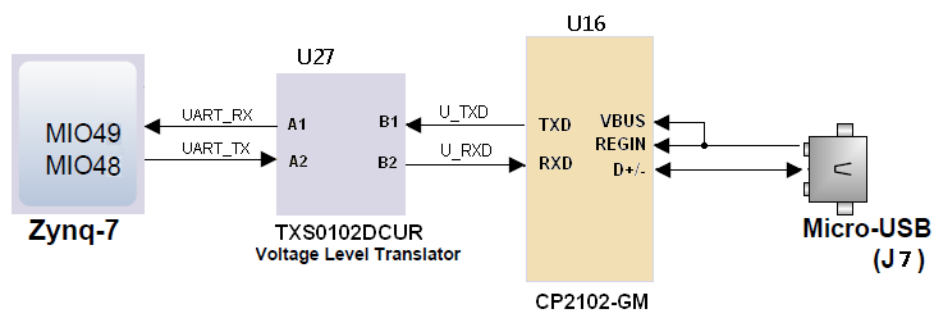


Figure 6-5

Uart Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
UART_TX	PS_MIO48_501	B12	Uart data output
UART_RX	PS_MIO49_501	C12	Uart data input

Silicon Labs provides virtual PC port (VCP) drivers for host PCs. These drivers allow the CP2102GM USB-UART bridge device to be displayed as a COM port in communication application software (eg, TeraTerm or HyperTerminal). The VCP device driver must be installed before the PC host establishes communication with the AX7010 development board.

6.6 SD Card slot

The AX7010 development board includes a Micro SD card interface to provide user access to SD card memory, BOOT programs for storing ZYNQ chips, Linux operating system kernels, file systems, and other user data files.

The SDIO signal is connected to the IO signal of the PSNKNK501 of the ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, the data level of the SD card is 3.3V, and we connect here through the TXS02612 level converter. The schematic of the Zynq7000 PS and SD card connectors is shown in Figure 6-6

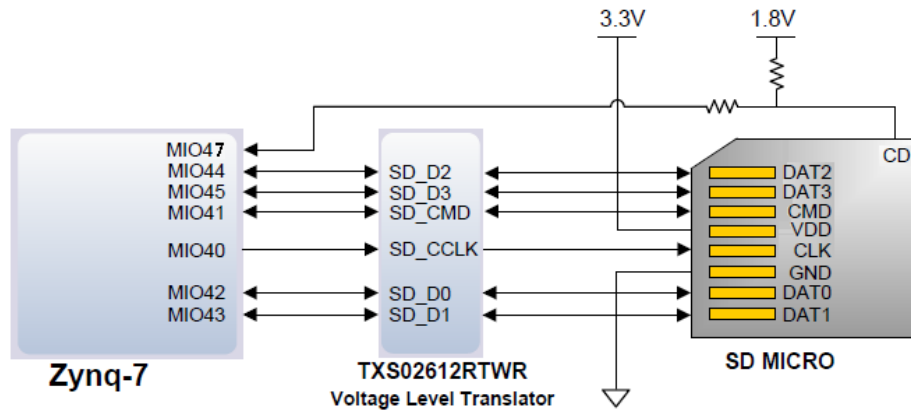


Figure 6-6

SD Card slot Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
SD_CLK	PS_MIO40	D14	SD clock signal
SD_CMD	PS_MIO41	C17	SD command signal
SD_D0	PS_MIO42	E12	SD data0
SD_D1	PS_MIO43	A9	SD data1
SD_D2	PS_MIO44	F13	SD data2
SD_D3	PS_MIO45	B15	SD data3
SD_CD	PS_MIO47	B14	SD card insert signal

6.7 PS PMOD

The AX7010 development board reserves a 12-pin 2.54mm PMOD interface (J12) for connecting the PS BANK500's IO and external modules or circuits. Because the IO of BANK500 is 3.3V standard, the signal of the connected external equipment and circuit also needs the 3.3V level standard. The schematic of the PMOD connector is shown in Figure 6-7.

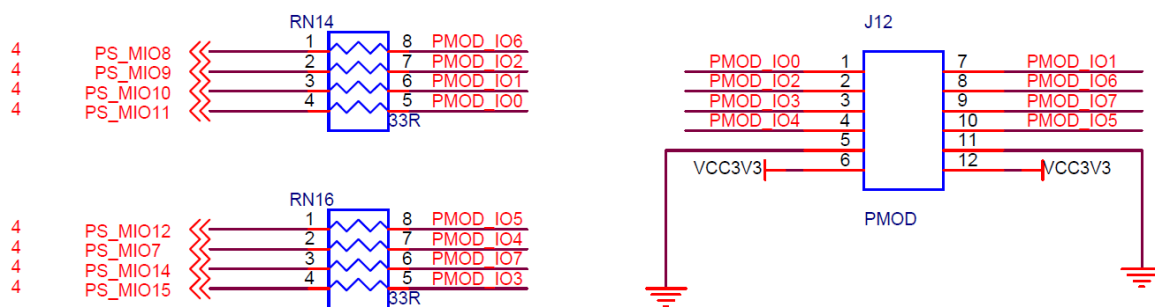


Figure 6-7

PS PMOD Pin Assignment:

PMOD Pin	Signal Name	Pin Name	Pin Number
PIN1	PMOD_IO0	PS_MIO11_500	C6
PIN2	PMOD_IO2	PS_MIO9_500	B5
PIN3	PMOD_IO3	PS_MIO15_500	C8
PIN4	PMOD_IO4	PS_MIO7_500	D8

PIN5	GND	-	-
PIN6	+3.3V	-	-
PIN7	PMOD_IO1	PS_MIO10_500	E9
PIN8	PMOD_IO6	PS_MIO8_500	D5
PIN9	PMOD_IO7	PS_MIO14_500	C5
PIN10	PMOD_IO5	PS_MIO12_500	D9
PIN11	GND	-	-
PIN12	+3.3V	-	-

6.8 User LED

On the AX7010 development board, two LED light-emitting diodes are connected to the BANK500 IO of the PS section. Users can use these two LEDs to debug the program. When the BANK500 IO voltage is high, the LED light goes out, and when the BANK500 IO voltage is low, the LED is lit. A schematic diagram of the connection between the ZYNQ BANK500 IO and the LED lamp is shown in Figure 6-8.

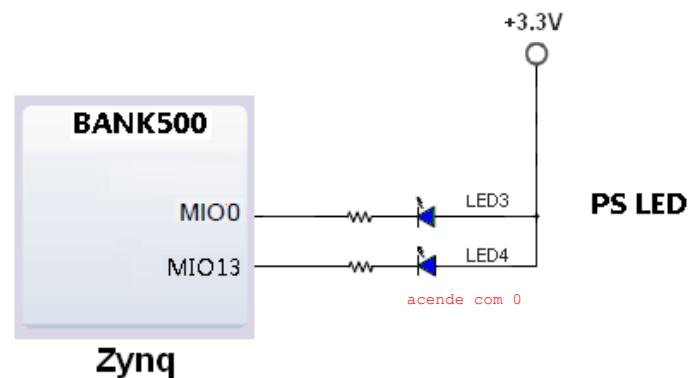


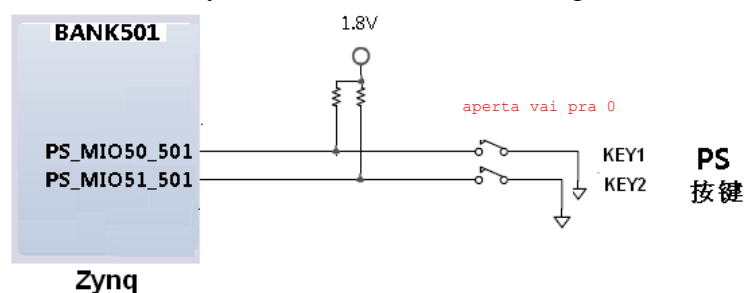
Figure 6-8

PS LED Pin Assignment:

Signal Name	Pin Name	Pin Number	
MIO0_LED	PS_MIO0_500	E6	PS LED1
MIO13_LED	PS_MIO13_500	E8	PS LED2

6.9 User Key

On the AX7010 development board, two user buttons are connected to the BANK501 IO of the PS section. The user can use these two user buttons to test the input signal and interrupt trigger. When the button is pressed in the design, the signal voltage input to the ZYNQ BANK501 IO is low, and when it is not pressed, the signal is high. A schematic diagram of the ZYNQ BANK501 IO and key connections is shown in Figure 6-9.



PS KEY Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
MIO_KEY1	PS_MIO50_501	B13	PS User KEY1
MIO_KEY2	PS_MIO51_501	B9	PS User KEY2

Next we will introduce the peripherals connected to the PL part (FPGA logic part).

The full name of HDMI is the high-definition multimedia video output interface. On the AX7010 development board, the differential IO of the FPGA is directly connected to the differential signal and clock of the HDMI interface. In the FPGA, the HDMI signal is converted to parallel. The HDMI digital video output transmission solution is supported. The maximum support is 1080P. @60Hz output functions. The HDMI signal is connected to the BANK34 of the PL portion of the ZYNQ. Figure 7-1 shows the schematic diagram of the HDMI design.



Signal Name	Pin Name	Pin Number	Explain
HDMI_CLK_P	IO_L13P_T2_MRCC_34	N18	HDMI clock+
HDMI_CLK_N	IO_L13N_T2_MRCC_34	P19	HDMI clock-
HDMI_D0_P	IO_L16P_T2_34	V20	HDMI data0+
HDMI_D0_N	IO_L16N_T2_34	W20	HDMI data0-
HDMI_D1_P	IO_L15P_T2_DQS_34	T20	HDMI data1+

HDMI_D1_N	IO_L15N_T2_DQS_34	U20	HDMI data1-
HDMI_D2_P	IO_L14P_T2_SRCC_34	N20	HDMI data2+
HDMI_D2_N	IO_L14N_T2_SRCC_34	P20	HDMI data2-
HDMI_SCL	IO_L20N_T3_34	R18	HDMI IIC clock
HDMI_SDA	IO_L19P_T2_34	R16	HDMI IIC data
HDMI_CEC	IO_L17P_T2_34	Y18	HDMI remote control signal
HDMI_HPD	IO_L17N_T2_34	Y19	HDMI Hot plug detection signal
HDMI_OUT_EN	IO_L18P_T2_34	V16	HDMI Power output control

7.2 EEPROM

The AX7010 development board has an EEPROM, 24LC04, with a capacity of 4Kbit (2*256*8bit) and consists of two 256-byte blocks that communicate through the IIC bus. On-board EEPROM is to learn IIC bus communication. The IIC signal of the EEPROM is connected to the ZNKQ PL port of the BANK34 IO port. Figure 7-2 is the schematic of EEPROM

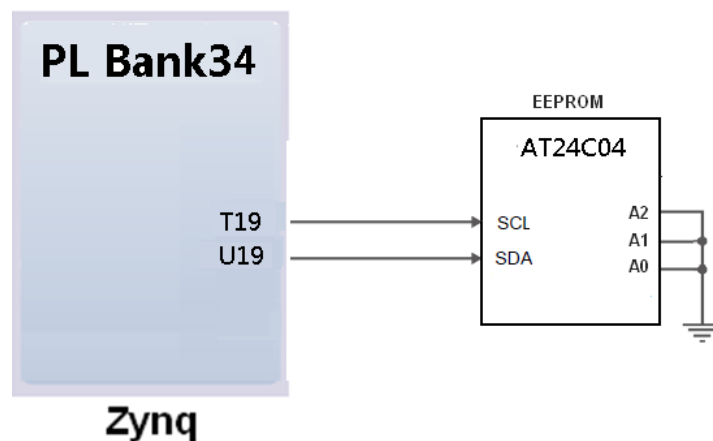


Figure 7-2

EEPROM Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
EEPROM_I2C_SCL	IO_25_34	T19	IIC 时钟信号
EEPROM_I2C_SDA	IO_L12N_T1_MRCC_34	U19	IIC 数据信号

7.3 RTC

The development board has a real-time clock RTC chip, DS1302, whose function is to provide calendar functions up to 2099, with days, minutes, seconds and weeks. If the system requires time, RTC needs to be involved in the product. He needs a 32.768KHz passive clock externally to provide an accurate clock source to the clock chip so that RTC can accurately provide clock information to the product. At the same time, in order to

power down the product, the real-time clock can still operate normally, generally, it is necessary to provide another battery to power the clock chip. BT1 is the battery holder, and we will use the button battery (CR1220, voltage 3V). After it is put in, when the system loses the battery, the coin cell battery can also supply power to the DS1302. In this way, regardless of whether the product is powered or not, the DS1302 will operate normally and will not be interrupted, providing continuous time information. The RTC interface signal is also connected to the BANK34 and BANK35 IO ports of the ZYNQ PL. Figure 7-3 shows the DS1302 schematic.

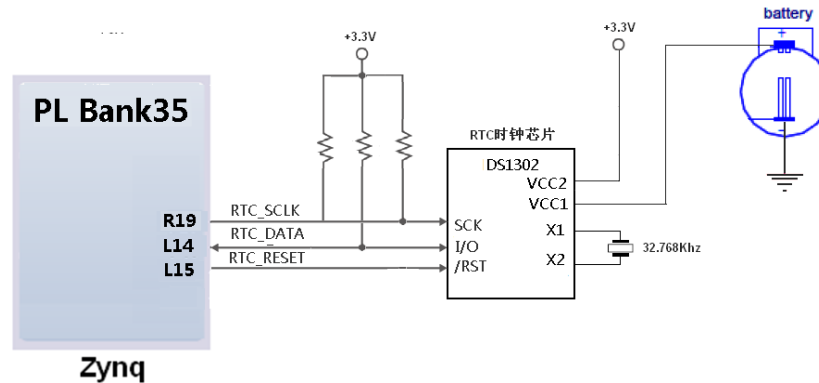


Figure 7-3

DS1302 Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
RTC_SCLK	IO_0_34	R19	RTC clock signal
RTC_RESET	IO_L22N_T3_AD7N_35	L15	RTC reset signal
RTC_DATA	IO_L22P_T3_AD7P_35	L14	RTC data signal

7.4 Expansion port J10

Expansion port J10 is a 40-pin 2.54mm double-row connector that expands more peripherals and interfaces for users.

The expansion port includes one 5-V power supply, two 3.3-V power supplies, three grounds, and 34 IO ports. The signal of IO port is connected to BANK35 and BANK35 of ZYNQ PL. The default level is 3.3V. Some IO of expansion port J10 can change the level of IO by replacing the power chip (SPX3819M5-3-3) on the development board. Do not directly connect directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect the level conversion chip.

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from damage caused by excessive external voltage or current. The P and N traces on the PCB design use differential traces to control the differential impedance to 100 ohms. Figure 7-4 shows the circuit of the expansion port (J10):

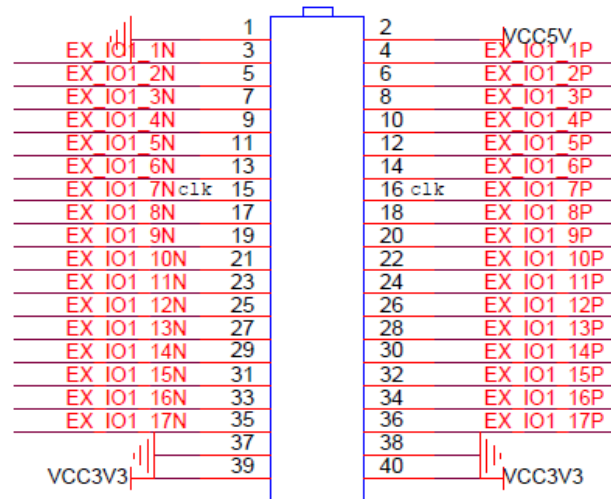


Figure 7-4

J10 Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
PIN1	GND	-	-
PIN2	+5V	-	-
PIN3	EX_IO1_1N	IO_L22N_T3_34	W19
PIN4	EX_IO1_1P	IO_L22P_T3_34	W18
PIN5	EX_IO1_2N	IO_L6N_T0_34	R14
PIN6	EX_IO1_2P	IO_L6P_T0_34	P14
PIN7	EX_IO1_3N	IO_L7N_T1_34	Y17
PIN8	EX_IO1_3P	IO_L7P_T1_34	Y16
PIN9	EX_IO1_4N	IO_L10N_T1_34	W15
PIN10	EX_IO1_4P	IO_L10P_T1_34	V15
PIN11	EX_IO1_5N	IO_L8N_T1_34	Y14
PIN12	EX_IO1_5P	IO_L8P_T1_34	W14
PIN13	EX_IO1_6N	IO_L23N_T3_34	P18
PIN14	EX_IO1_6P	IO_L23P_T3_34	N17
PIN15	EX_IO1_7N	IO_L11N_T1_34	U15
PIN16	EX_IO1_7P	IO_L11P_T1_34	U14
PIN17	EX_IO1_8N	IO_L24N_T3_34	P16
PIN18	EX_IO1_8P	IO_L24P_T3_34	P15
PIN19	EX_IO1_9N	IO_L9N_T1_34	U17
PIN20	EX_IO1_9P	IO_L9P_T1_34	T16
PIN21	EX_IO1_10N	IO_L21_N_T3_34	V18
PIN22	EX_IO1_10P	IO_L21_P_T3_34	V17
PIN23	EX_IO1_11N	IO_L5N_T0_34	T15
PIN24	EX_IO1_11P	IO_L5P_T0_34	T14
PIN25	EX_IO1_12N	IO_L3N_T0_34	V13
PIN26	EX_IO1_12P	IO_L3P_T0_34	U13
PIN27	EX_IO1_13N	IO_L4N_T0_34	W13
PIN28	EX_IO1_13P	IO_L4P_T0_34	V12
PIN29	EX_IO1_14N	IO_L2N_T0_34	U12

PIN30	EX_IO1_14P	IO_L2P_T0_34	T12
PIN31	EX_IO1_15N	IO_L1N_T0_34	T10
PIN32	EX_IO1_15P	IO_L1P_T0_34	T11
PIN33	EX_IO1_16N	IO_L2N_T0_35	A20
PIN34	EX_IO1_16P	IO_L2P_T0_35	B19
PIN35	EX_IO1_17N	IO_L1N_T0_35	B20
PIN36	EX_IO1_17P	IO_L1P_T0_35	C20
PIN37	GND	-	-
PIN38	GND	-	-
PIN39	+3.3V	-	-
PIN40	+3.3V	-	-

7.5 Expansion port J11

The expansion port J11 is also a 40-pin 2.54mm double row connector, which allows users to expand more peripherals and interfaces.

The expansion port includes one 5-V power supply, two 3.3-V power supplies, three grounds, and 34 IO ports. The signal of IO port is connected to BANK35 of ZYNQ PL. The default level is 3.3V. All IO of expansion port J11 can change the level of IO by replacing the power chip (SPX3819M5-3-3) on the development board. Do not directly connect directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect the level conversion chip.

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from damage caused by excessive external voltage or current. The P and N traces on the PCB design use differential traces to control the differential impedance to 100 ohms. . The circuit of the expansion port (J11) is shown in Figure 7-5.

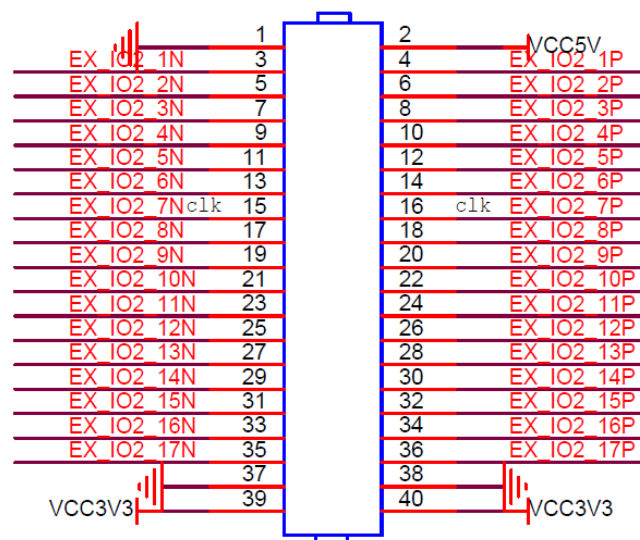


Figure 7-5

J11 Pin Assignment:

Pin	Signal Name	Pin Name	Pin Number
PIN1	GND	-	-
PIN2	+5V	-	-
PIN3	EX_IO2_1N	IO_L6N_T0_35	F17
PIN4	EX_IO2_1P	IO_L6P_T0_35	F16
PIN5	EX_IO2_2N	IO_L15N_T2_35	F20
PIN6	EX_IO2_2P	IO_L15P_T2_35	F19
PIN7	EX_IO2_3N	IO_L18N_T2_35	G20
PIN8	EX_IO2_3P	IO_L18P_T2_35	G19
PIN9	EX_IO2_4N	IO_L14N_T2_35	H18
PIN10	EX_IO2_4P	IO_L14P_T2_35	J18
PIN11	EX_IO2_5N	IO_L9N_T1_35	L20
PIN12	EX_IO2_5P	IO_L9P_T1_35	L19
PIN13	EX_IO2_6N	IO_L7N_T1_35	M20
PIN14	EX_IO2_6P	IO_L7P_T1_35	M19
PIN15	EX_IO2_7N	IO_L12N_T1_35	K18
PIN16	EX_IO2_7P	IO_L12P_T1_35	K17
PIN17	EX_IO2_8N	IO_L10N_T1_35	J19
PIN18	EX_IO2_8P	IO_L10P_T1_35	K19
PIN19	EX_IO2_9N	IO_L17N_T2_35	H20
PIN20	EX_IO2_9P	IO_L17P_T2_35	J20
PIN21	EX_IO2_10N	IO_L11N_T1_35	L17
PIN22	EX_IO2_10P	IO_L11P_T1_35	L16
PIN23	EX_IO2_11N	IO_L8N_T1_35	M18
PIN24	EX_IO2_11P	IO_L8P_T1_35	M17
PIN25	EX_IO2_12N	IO_L4N_T0_35	D20
PIN26	EX_IO2_12P	IO_L4P_T0_35	D19
PIN27	EX_IO2_13N	IO_L5N_T0_35	E19
PIN28	EX_IO2_13P	IO_L5P_T0_35	E18
PIN29	EX_IO2_14N	IO_L16N_T2_35	G18
PIN30	EX_IO2_14P	IO_L16P_T2_35	G17
PIN31	EX_IO2_15N	IO_L13N_T2_35	H17
PIN32	EX_IO2_15P	IO_L13P_T2_35	H16
PIN33	EX_IO2_16N	IO_L19N_T3_35	G15
PIN34	EX_IO2_16P	IO_L19P_T3_35	H15
PIN35	EX_IO2_17N	IO_L20N_T3_35	J14
PIN36	EX_IO2_17P	IO_L20P_T3_35	K14
PIN37	GND	-	-
PIN38	GND	-	-
PIN39	+3.3V	-	-
PIN40	+3.3V	-	-

7.6 User LED

The PL section of the AX7010 development board connects four LED light emitting diodes. The schematic diagram of the 4 user LED parts is shown in Figure 7-6. The LED lamp signal

is connected to the IO of the PL part BANK35. When the IO pin of the PL section BANK35 outputs a logic 0, the LED is lit, and when it is logic 1, the LED is extinguished.

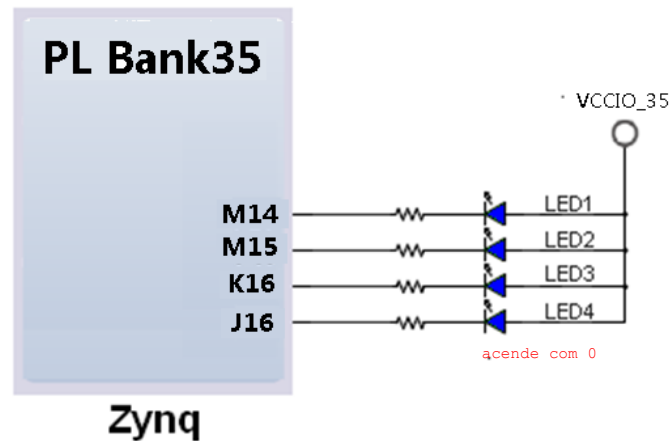


Figure 7-6

PL User LED Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
LED1	IO_L23P_T3_35	M14	PL LED1
LED2	IO_L23N_T3_35	M15	PL LED2
LED3	IO_L24P_T3_35	K16	PL LED3
LED4	IO_L24N_T3_35	J16	PL LED4

7.7 User Key

The PL section of the AX7010 development board contains four user buttons (KEY1~KEY4). The signals of the buttons are connected to the BINs of BANK34 and BANK35 of ZYNQ. The buttons are all active low. When they are not pressed, the signal is high; when the button is pressed, the signal is low. The schematic of the four user buttons is shown in Figure 7-7.

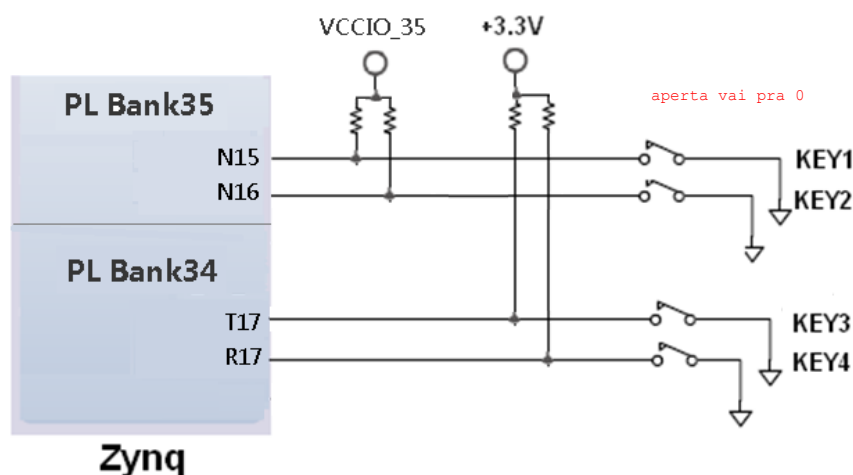


Figure 7-7

PL User Key Pin Assignment:

Signal Name	Pin Name	Pin Number	Explain
KEY1	IO_L21P_T3_35	N15	PL KEY1
KEY2	IO_L21P_T3_35	N16	PL KEY 2
KEY3	IO_L20P_T3_34	T17	PL KEY 3
KEY4	IO_L19N_T3_34	R17	PL KEY 4