ENGIN 366 Final Project:

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Objective: The purpose of this final project is to build a basic logic circuit using CMOS. This circuit is biased from a current mirror. We used CMOS logic to build 2 logic gates that will output the Sum or Carry of a half adder.

Equipment:

1. 6 ALD1103 CMOS chips
2. 1 ALD1107 PMOS chip
3. 1 ALD1106 NMOS chip
4. 3 1 kΩ Resistor
5. 1 4-DIP switch
6. 2 Green LEDs

Introduction:

Digital logic found in electronics uses MOSFETs for efficiency and size. Our electronic components have billions of FETs that perform digital logic operations. We chose to build a half adder as the half adder is the basis of different components. This half adder takes in 2 binary bits and adds them together, outputting a Sum and Carry bit. To bias our circuit we also used 2 current mirrors to keep the drain current low enough to propagate the signal across all the chips. This circuit should only turn on one LED at a time.

Description:

We chose a 1 kΩ resistor to get a reference current of 8 mA to bias our transistors. Using two current mirrors we can pull and push current to bias our MOSFETS. We do this because in class we learned that a NMOS current mirror is a current sink, and the PMOS is a current source. This allows us to connect the output of the PMOS source to bias the different MOSFETs that will compute the logic.

To build a half adder, we need to use AND and XOR gates. We built these gates using the CMOS matched pair MOSFETS. This is because we can use 4 FETs to build a NAND gate, and we use the NAND gate to build the AND and XOR gates. We use CMOS because it avoids using an inverter stage and allows the voltage to be high enough to keep proper logic between gates. A NAND gate always outputs a 1 unless both inputs are 1, then it outputs a 0. The AND gate requires two NAND gates and the XOR requires 4 NAND gates. We used the 1103 CMOS chip to have matched pairs and because each chip has 2 NMOS and 2 PMOS this allowed us to use one chip per NAND gate.

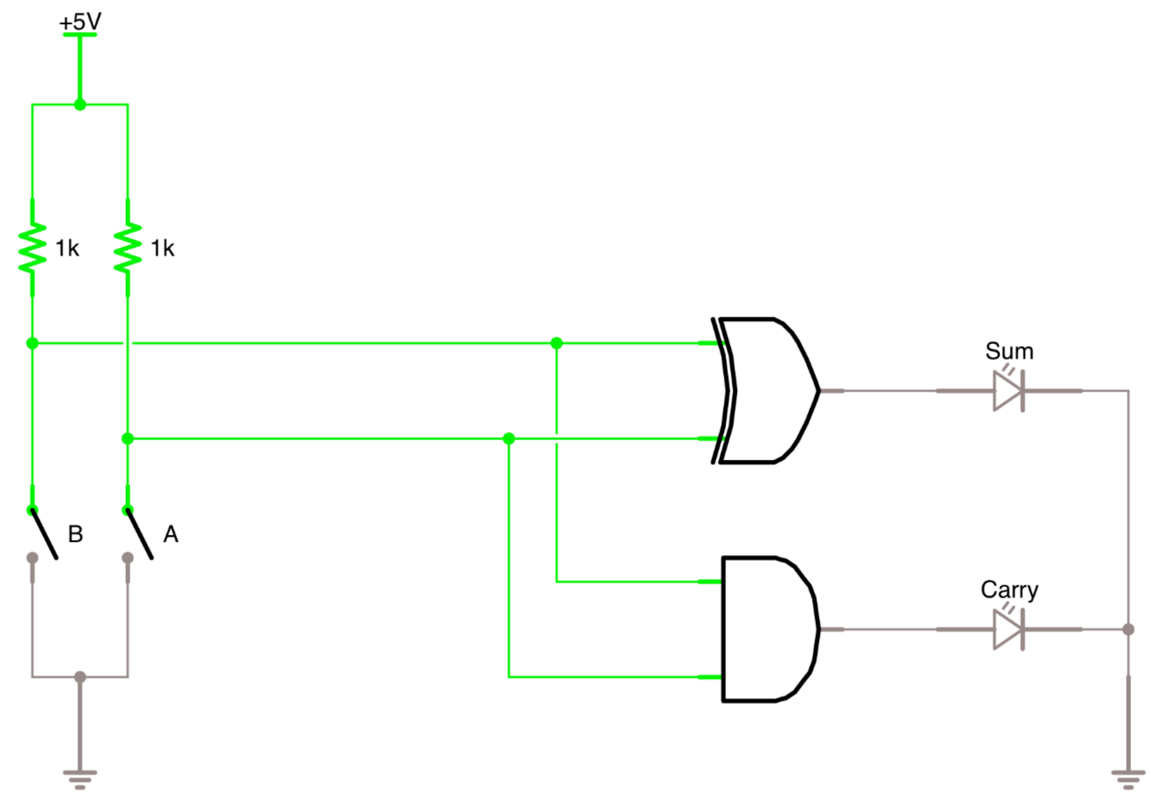

Figure 1: Circuit diagram with logic gates instead of MOSFETS.

The following images we sourced from the internet to see how we can wire the MOSFETs to make NAND gates to obtain the logic gates we need for our circuit.

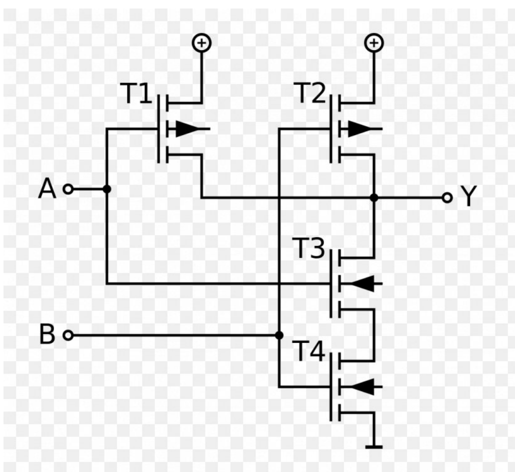

Figure 2: Using 4 MOSFETs we can build one NAND gate. We have 2 PMOS at the top of the circuit and 2 NMOS at the bottom. If both inputs are high, then the current flows through the series NMOS and drops the voltage at the output to 0. If only one is high, then the current is able to flow through the output.

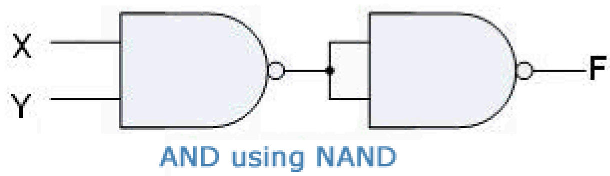

Figure 3: Using 2 NAND gates to build one AND gate.

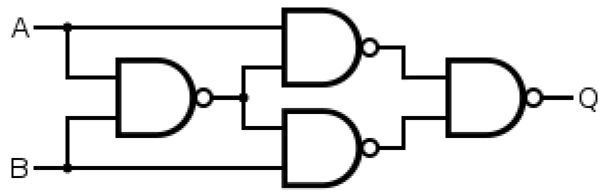

Figure 4: XOR gate using 4 NAND gates.

Lab Measurements:

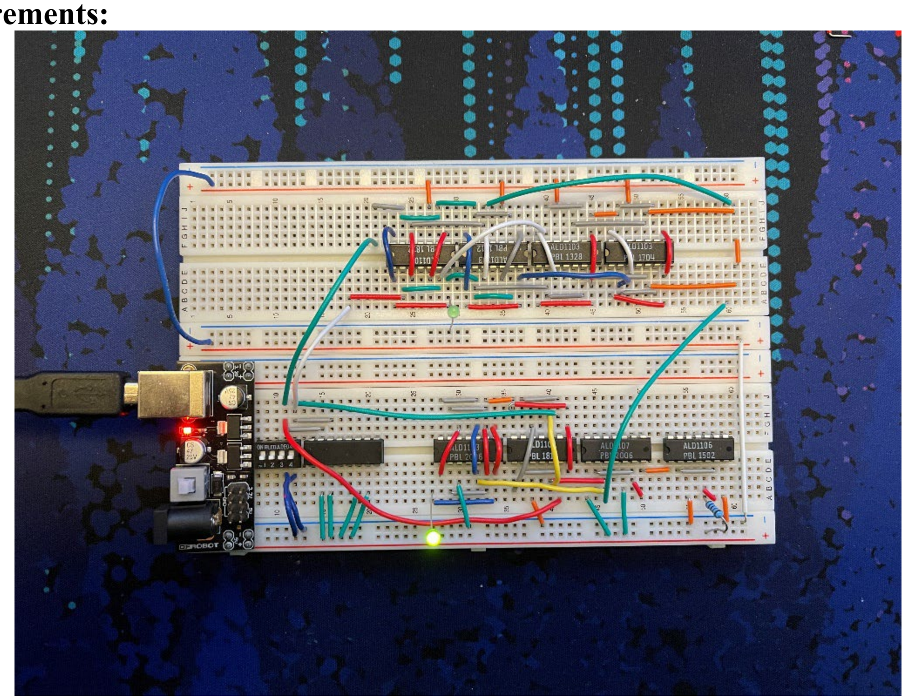

Figure 5: Built circuit with inputs A = 1 and B = 1. We can see that only the carry LED is on. The top breadboard contains the 4 CMOS chip that build the XOR gate, the lower breadboard has the inputs, AND gate, and current mirrors.

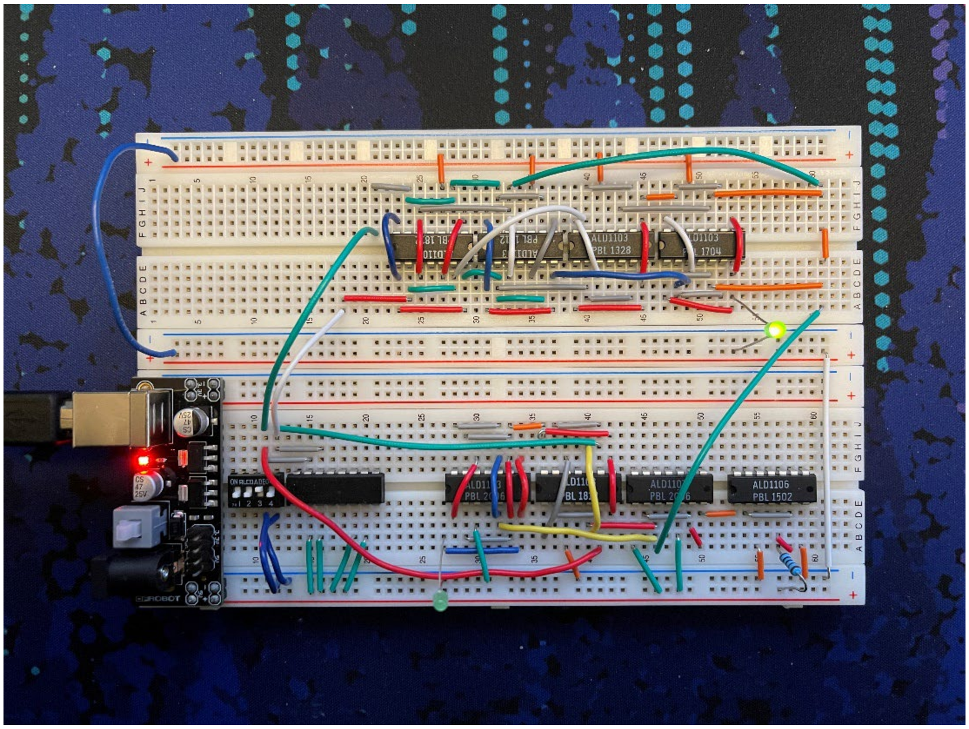

Figure 6: Circuit with input A = 1, where the Sum LED is on.

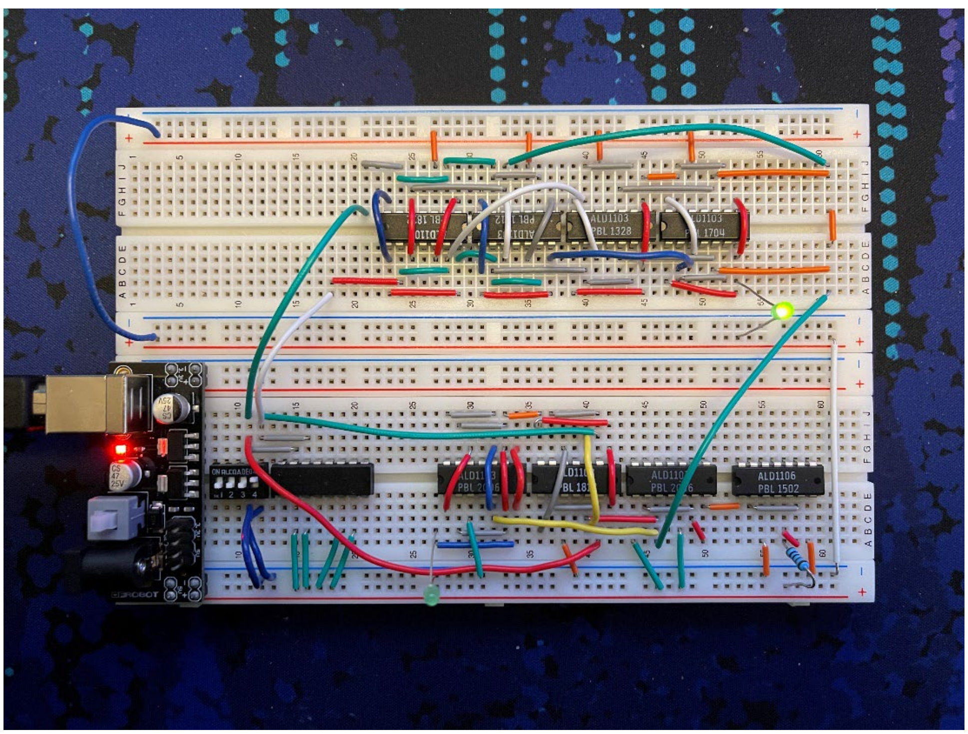

Figure 7: Circuit with input B = 1, where the Sum LED is on.

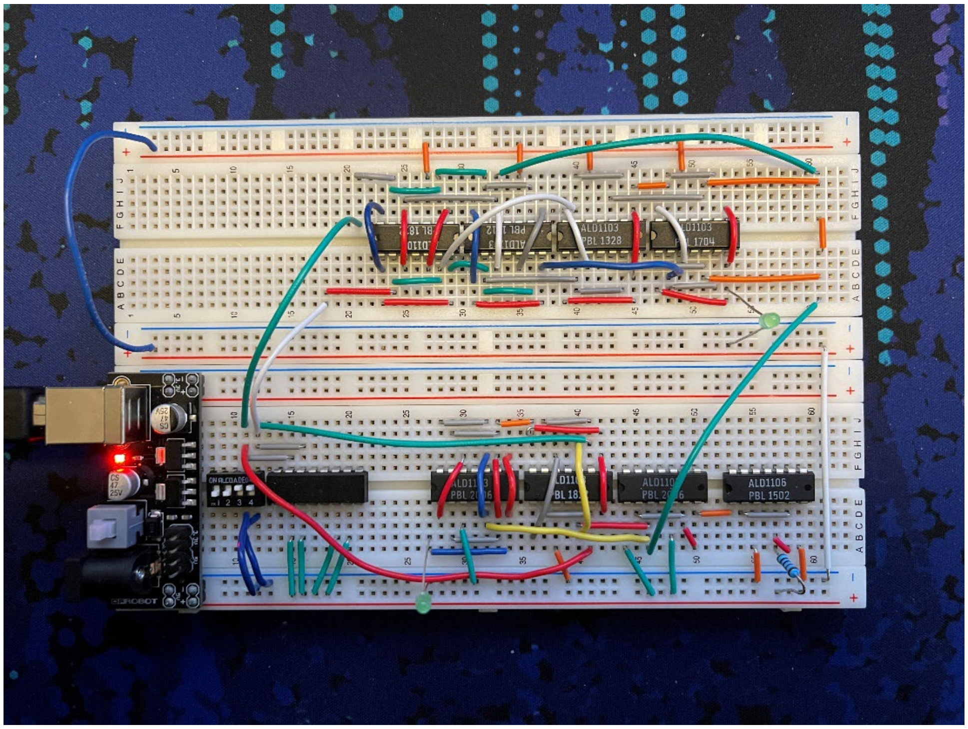

Figure 8: Circuit with both inputs turned off. Neither LED turn on as we are adding 0+0.

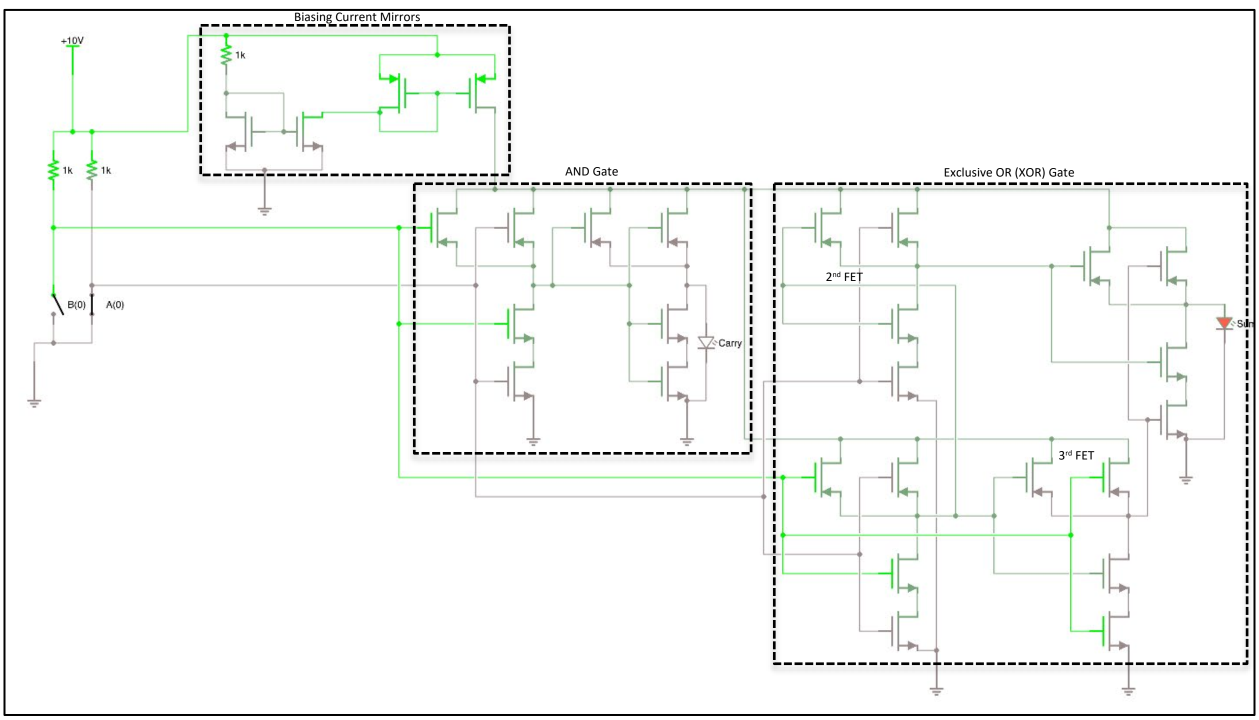

Figure 9: Schematic of our circuit. We divided the different MOSFETs to show the current mirrors, AND gate, and XOR gate.

Results and Analysis:

The project was able to function as expected. The current mirror biased the MOSFETs with 8 mA of current. This current only flows in one logic gate at a time, given that each MOSFET controls the gates of the other ones further down the logic. We tested our design by testing the individual NAND gates before connecting them. For our initial testing we used 5 V as supply power and the circuit logic worked.

As expected, if either of our inputs were on the Sum LED turned on. If both inputs were on, then the Sum LED turned off and the Carry LED turned on. And if both inputs were off, then the output is zero.