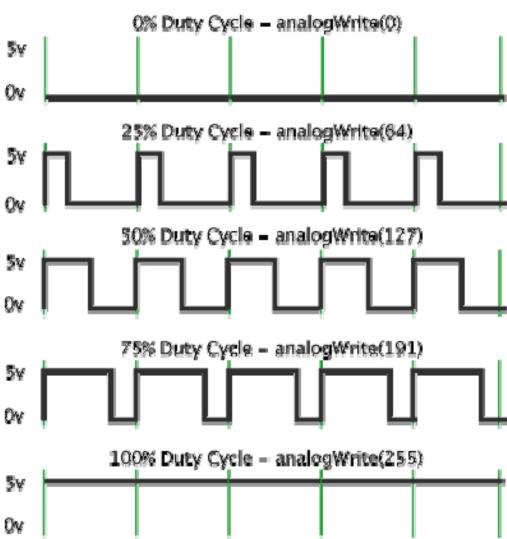
PWM



Disciplina de Sistemas Embarcados - Faculdade de Engenharia Elétrica - Universidade Federal de Uberlândia – Prof. Fábio

Pulse Width Modulation





TENSÃO MÉDIA

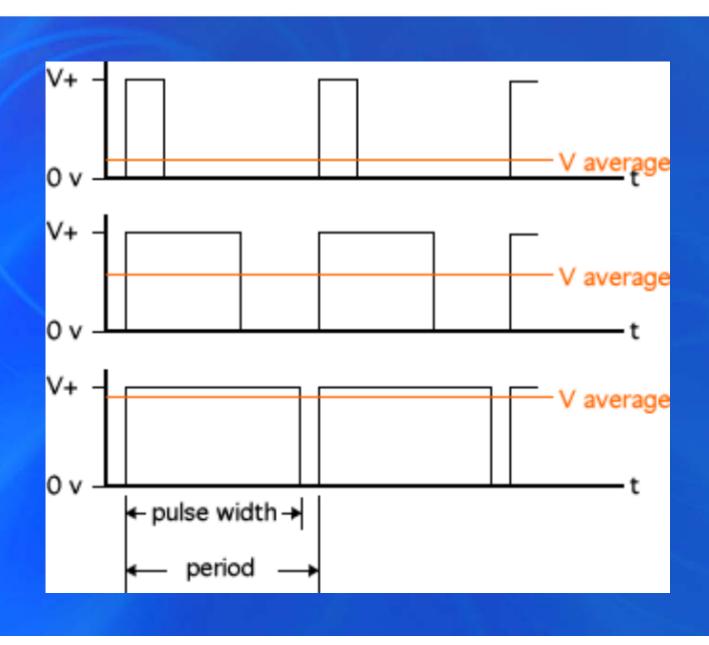
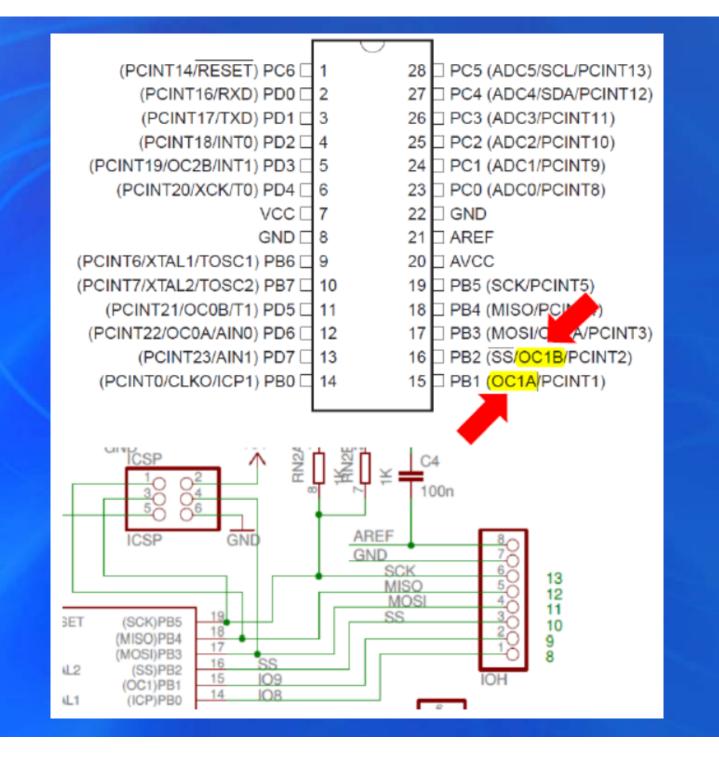
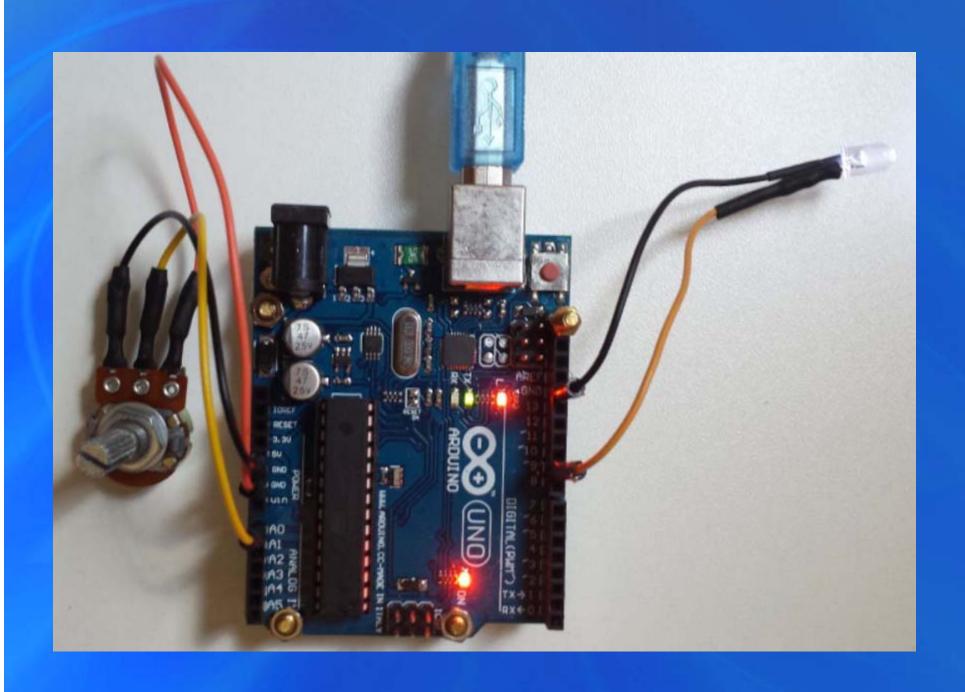
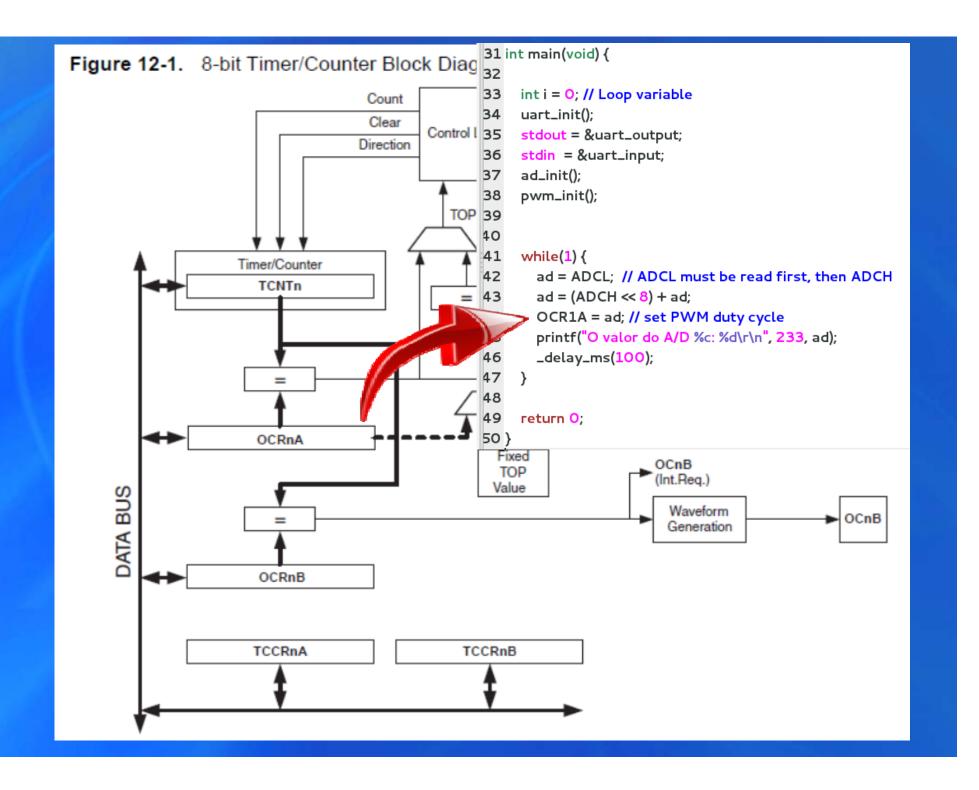


Figure 12-1. 8-bit Timer/Counter Block Diagram Count TOVn (Int.Req.) Clear Control Logic $\mathsf{clk}_{\mathtt{Tn}}$ Clock Select Direction Edge Tn Detector TOP BOTTOM (From Prescaler) Timer/Counter **TCNTn** = 0OCnA (Int.Req.) Waveform OCnA Generation **OCRnA** Fixed OCnB (Int.Req.) TOP Value DATA BUS Waveform **OCnB** Generation **OCRnB TCCRnA TCCRnB**





```
10 int ad = 0;
11 int temp = 0;
12 char snum[10];
13
14
15 void pwm_init(void) {
16
17
       DDRB = (1 \ll DDB1);
                                // PB1 is now output - OC1A
       TCCR1A |= (1 << COM1A1); // overrides the normal port functionality of the I/O pin to OC1A - Output Compare Pin
18
19
                                // Pino PB1 do uC e Pino 9 do Kit Arduíno (Pag. 131).
20
21
       TCCR1A |= (1 << WGM11) | (1 << WGM10); // Timer/Counter Mode of Operation = Fast PWM-10-bit, TOP = 0x03FF,
22
                                              // Update of OCR1x at = BOTTOM, TOV1 Flag Set on = TOP (Pag. 132)
23
24
       TCCR1B |= (1 << WGM12); // Timer/Counter Mode of Operation = Fast PWM-10-bit, TOP = 0x03FF,
25
                                // Update of OCR1x at = BOTTOM, TOV1 Flag Set on = TOP (Pag. 132)
26
27
       TCCR1B |= (1 << CS11); // set prescaler to 8 and starts PWM
28}
                           OCRnA
                                                             Fixed
                                                                                  OCnB
                                                            TOP
                                                                                  (Int.Reg.)
                                                            Value
                                                                                    Waveform
                                                                                                            OCnB
                                                                                    Generation
                           OCRnB
                           TCCRnA
                                                       TCCRnB
```





BeagleBone Black

Cape Expansion Headers

DGND VDD 3V3 3 VDD 5V SYS 5V SYS RESETN GPIO 60 UART4 RXD UART4_TXD **EHRPWM1B** GPIO_48 15 16 SPIO_CSO 17 18 SPIO_D1 12C2 SDA 12C2 SCL 19 20 GPIO_49 23 24 UART1_TXD UART1 RXD GPIO 117 25 GPIO_115 27 28 SPI1_CSO SPI1_D0 29 30 **GPIO 112** SPI1 SCLK 31 32 VDD ADC GNDA ADC 35 36 AIN5 AIN6 AIN2 37 AIN3 39 40 GPIO_20 **ECAPPWMO** 43 44 DGND 45 46



LEGEND
Power/Ground/Reset
AVAILABLE DIGITAL
AVAILABLE PWM
SHARED I2C BUS
RECONFIGURABLE DIGITAL

P8

DGND	1	2	DGND
MMC1_DAT6	3	4	MMC1_DAT7
MMC1_DAT2	5	6	MMC1_DAT3
GPIO_66	7	8	GPIO_67
GPIO_69	9	10	GPIO_68
GPIO_45	11	12	GPIO_44
EHRPWM2B	13	14	GPIO_26
GPIO_47	15	16	GPIO_46
GPIO_27	17	18	GPIO_65
EHRPWM2A	19	20	MMC1_CMD
MMC1_CLK	21	22	MMC1_DAT5
MMC1_DAT4	23	24	MMC1_DAT1
MMC1_DATO	25	26	GPIO_61
LCD_VSYNC	27	28	LCD_PCLK
LCD_HSYNC	29	30	LCD_AC_BIAS
LCD_DATA14	31	32	LCD_DATA15
LCD_DATA13	33	34	LCD_DATA11
LCD_DATA12	35	36	LCD_DATA10
LCD_DATA8	37	38	LCD_DATA9
LCD_DATA6	39	40	LCD_DATA7
LCD_DATA4	41	42	LCD_DATA5
LCD_DATA2	43	44	LCD_DATA3
LCD_DATA0	45	46	LCD_DATA1

15.1.2 Integration

The Pulse Width Modulation Subsystem (PWMSS) includes a single instance of the Enhanced High Resolution Pulse Width Modulator (eHRPWM), Enhanced Capture (eCAP), and Enhanced Quadrature Encoded Pulse (eQEP) modules. This device includes three instantiations of the PWMSS.

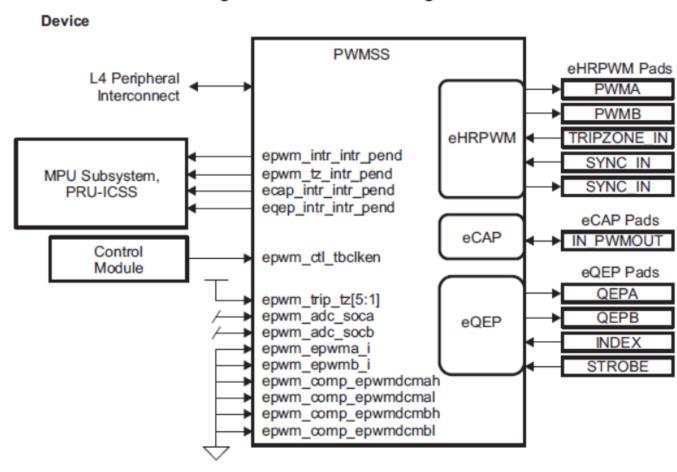
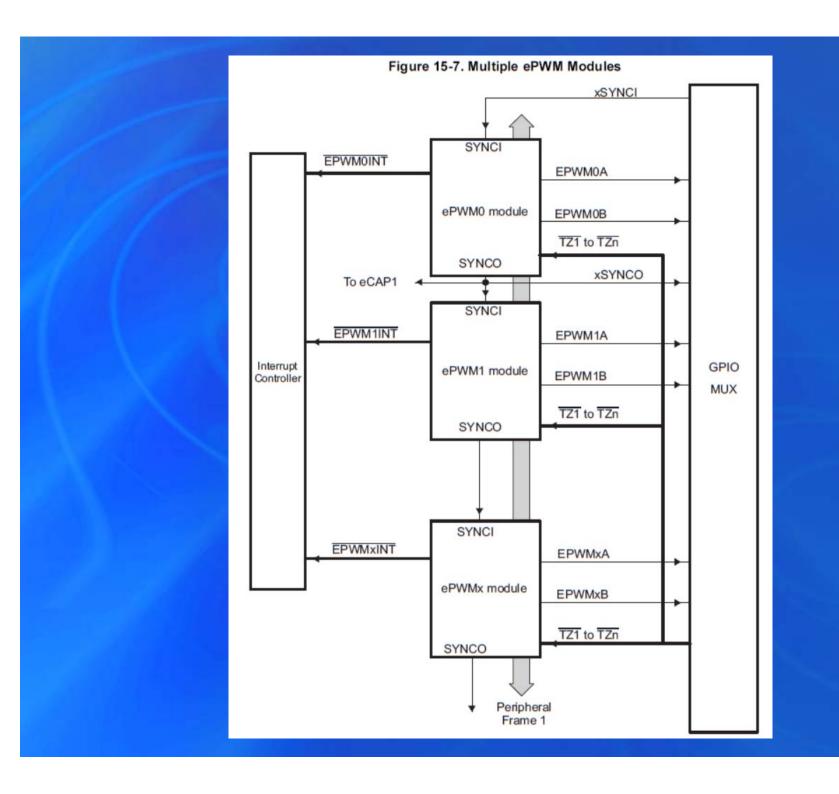


Figure 15-1. PWMSS Integration

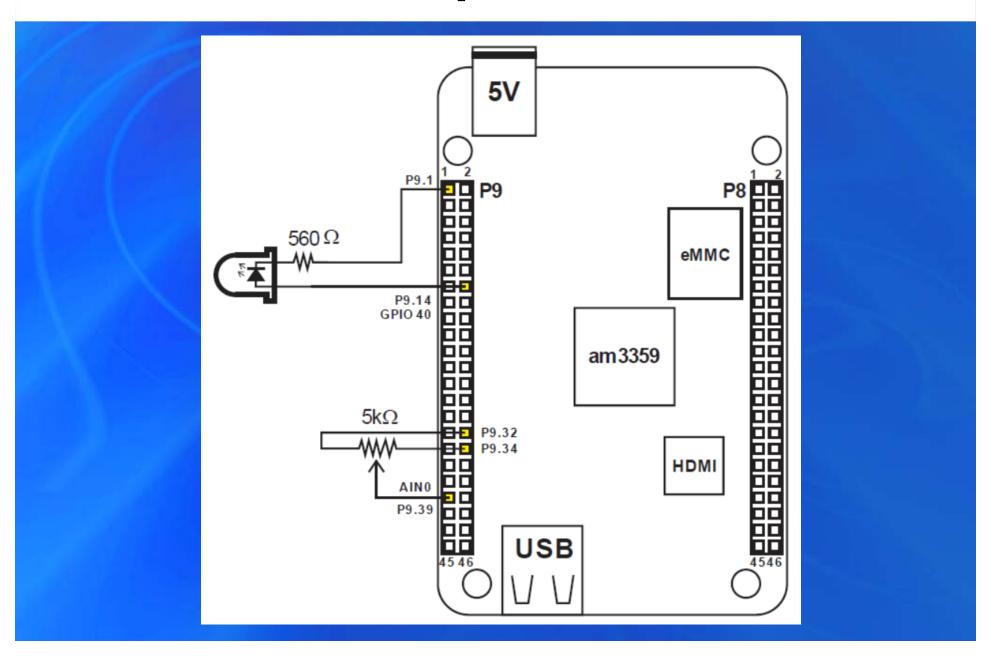


EHRPWM0A	1	P9_31	P9_22
EHRPWM0B	2	P9_21	P9_29
EHRPWM1A	3	P9_14	P8_36
EHRPWM1B	4	P9_16	P8_34
EHRPWM2A	5	P8_19	P8_45
EHRPWM2B	6	P8_13	P8_46
ECAPPWM0	7	P9_42	
ECAPPWM2	8	P9_28	

8 PWMs and 4 timers

P9			P8				
DGND	1	2	DGND	DGND	1	2	DGND
VDD_3V3	3	4	ADD ³ A3	GPIO_38	3	4	GPIO_39
VDD_5V	5	6	VDD_5V	GPIO_34	5	6	GPIO_35
SYS_5V	7	8	SYS_5V	TIMER4	7	8	TIMER7
PWR_BUT	9	10	SYS_RESETN	TIMER5	9	10	TIMER6
GPIO_30	11	12	GPIO_60	GPIO_45	1.1	12	GPIO_44
GPIO_31	13	14	EHRPWM1A	EHRPWM2B		14	GPIO_26
GPIO_48		16	EHRPWM1B	GPIO_47	15	16	GPIO_46
GPIO_5	17	18	GPIO_4	GPIO_27		18	GPIO_65
I2C2_SCL	19	20	I2C2_SDA	EHRPWM2A	19	20	GPIO_63
EHRPWMOB		22	EHRPWMOA	GPIO_62	21	22	GPIO_37
GPIO_49		24	GPIO_15	GPIO_36		24	GPIO_33
GPIO_117		26	GPIO_14	GPIO_32		26	GPIO_61
GPIO_115		28	ECAPPWM2	GPIO_86		28	GPIO_88
EHRPWMOB		30	GPIO_112	GPIO_87		30	GPIO_89
EHRPWMOA		32	VDD_ADC	GPIO_10		32	GPIO_11
AIN4		34	GNDA_ADC	GPIO_9		34	EHRPWM1B
AIN6	35	36	AIN5	GPIO_8		36	
AIN2		38	AIN3	GPIO_78		38	GPIO_79
AINO	39	40	AIN1	GPIO_76		40	GPIO_77
GPIO_20		42	ECAPPWMO	GPIO_74		42	GPIO_75
DGND	43	44	DGND	GPIO_72		44	GPIO_73
DGND	45	46	DGND	EHRPWM2A	45	46	EHRPWM2B

Exemplo PWM



```
8 #define SYSFS_ADC_DIR "/sys/bus/iio/devices/iio:device0"
 9 #define SYSFS_PWM_DIR "/sys/devices/ocp.3/pwm_test_"
10 #define MAX_BUF 64
11 #define P9_14 "P9_14.16"
12 // O valor 16 do 14.16 deve ser configurado de acordo com o valor do arquivo
13 // (pwm_test_P9_14.x) encontrado na pasta "/sys/devices/ocp.3/"
14 // O valor de ocp.x também pode variar, por isso verifique o valor de x na pasta "/sys/devices/"
15
16 #define PERIOD 409500 //Frequency = (1x10E9) = 1Hz
17
              //Frequency = 1x10E9/409500 = 2442Hz
18 #define DUTY 0
                      // Duty Depends on Polarity
19 #define POLARITY 0 // Polarity 0 = duty = 0 = 0% duty cycle and duty = PERIOD = 100% duty cycle
              // Polarity 1 = duty = PERIOD = 0% duty cycle and duty = 0 = 100% duty cycle
20
21
22
23 int adc_read(int);
24 void configPWM(const char*, unsigned long, unsigned long, int);
25 void setDuty(const char*, unsigned long);
26
27 int main()
28 {
29 int valorAD;
```

```
103 // Função para atualizar o Duty Cycle
104 void setDuty(const char* pino, unsigned long duty)
105 {
106
      int fd, len;
107
      char buf[MAX_BUF];
108 snprintf(buf, sizeof(buf), SYSFS_PWM_DIR "%s/duty", pino);
109 fd = open(buf, O_WRONLY);
      len = snprintf(buf, sizeof(buf), "%lu", duty);
110
111
      write(fd, buf, len);
112
      close(fd);
113 }
```

```
Arquivo Editar Ver Pesquisar Terminal Ajuda
root@beaglebone:~# cd /sys/devices/ocp.3/pwm_test_P9_14.16/
root@beaglebone:/sys/devices/ocp.3/pwm_test_P9_14.16# ls
driver modalias polarity run uevent
duty period power subsystem
root@beaglebone:/sys/devices/ocp.3/pwm_test_P9_14.16#
```

```
43 // Função para a leitura do ADC - canal O a 6
44 int adc_read(int pin)
45 {
46
       int fd;
47
       char buf[MAX_BUF];
48
       char ch[5];
49
50
       snprintf(buf, sizeof(buf), SYSFS_ADC_DIR "/in_voltage%d_raw", pin);
51
       fd = open(buf, O_RDONLY);
52
       if (fd < 0) {
53
54
            perror("adc/get-value");
55
56
57
       read(fd, ch, 4);
58
59
     close(fd);
     return atoi(ch);
60
61 }
```

