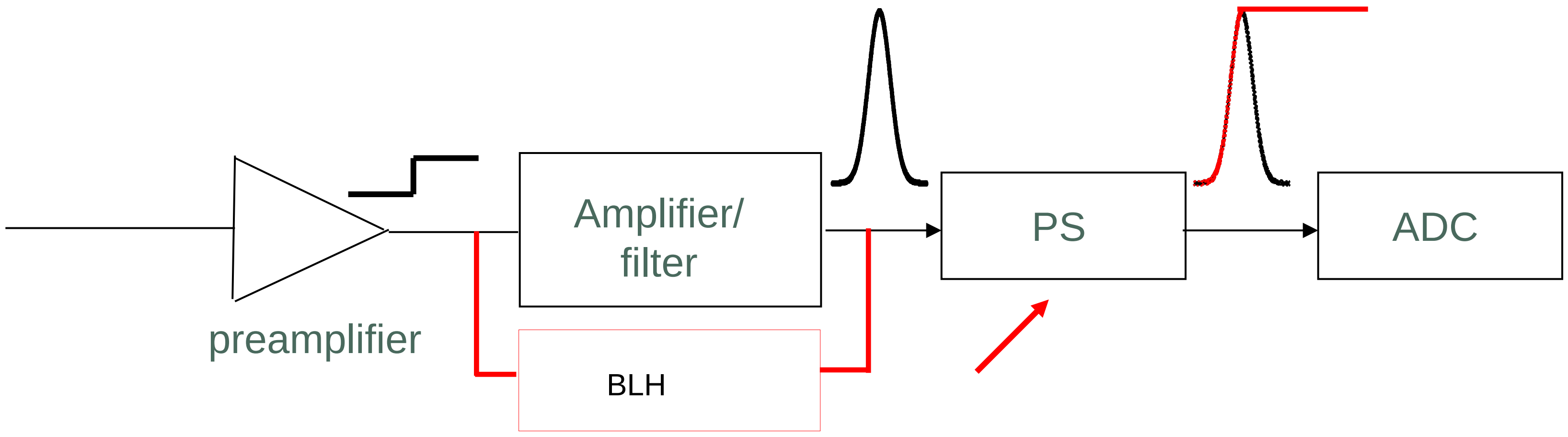
The Peak Stretcher



goal: to stretch the signal peak at the filter output for the time necessary for the ADC conversion

Peak stretch: "stretch" the peak of gaussian pulse, b/c amplitude of gaussian is the information we need, but it last for few time. So in this way the adc can convert in time. Once the conversion is done => reset.

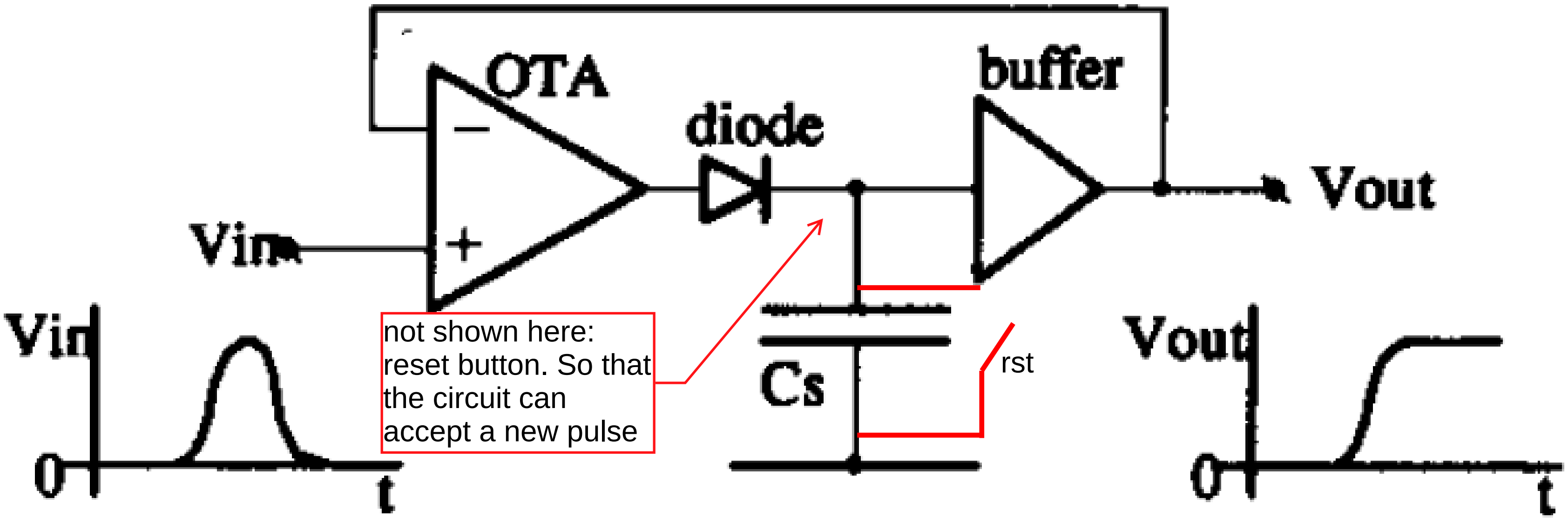
Common/Traditional schematic of peak-stretch.

[audio perché leggevi email]

The traditional Peak Stretcher

problem: Diode not implemented in CMOS :(We want the same circuit but with a substitute for it

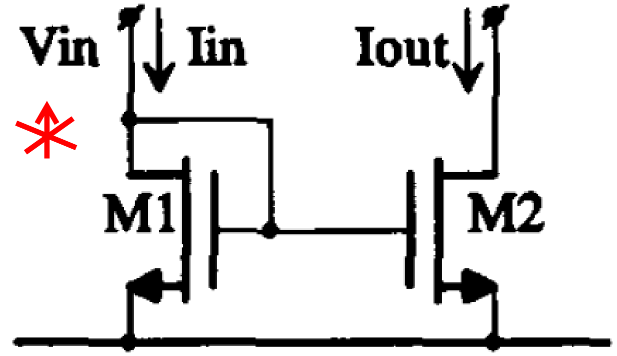
CLOSED: => PERFECT NEGATIVE FEEDBACK!



OTA = operational amplifier but with current output. buffer to separa cap. from world. Then loop closed.
EXPL: Ving like the drawing, Cs=0V at the beginning, the buffer keeps the "-"at 0V. When Vin starts to grow, V+ > V-, the OTA start providing a positive output, drives the diode (sends current). With this polarity the diode turns on and charge the cap. **THE LOOP IS CLOSED IF THE DIODE IS TURNEDON => perfect negative feedback**. the buffer transver Vcs, so also V- start to grow up. Since there's a loop a virtual short circuit is enstablished between the two inputs. Thus, if we have a short circuit V- and V+ the output is following V+, thus we have a buffer, enabled by the DiodeON. When the input start to decrease (After the peak), V+ starts to drop, the negative input is still high. So we have an inversion of polarity at the input of OTA, thus the ouptut starts to get negative (current in the other direction) but this is not possible, due to the diode, which turnsOff, and the loop is open. [2 phases: 1loop closed it works as a buffer, 2loop open, Cs stops to be charged, the Cs holds the final value of the peak voltage, and the output is ketp at this]

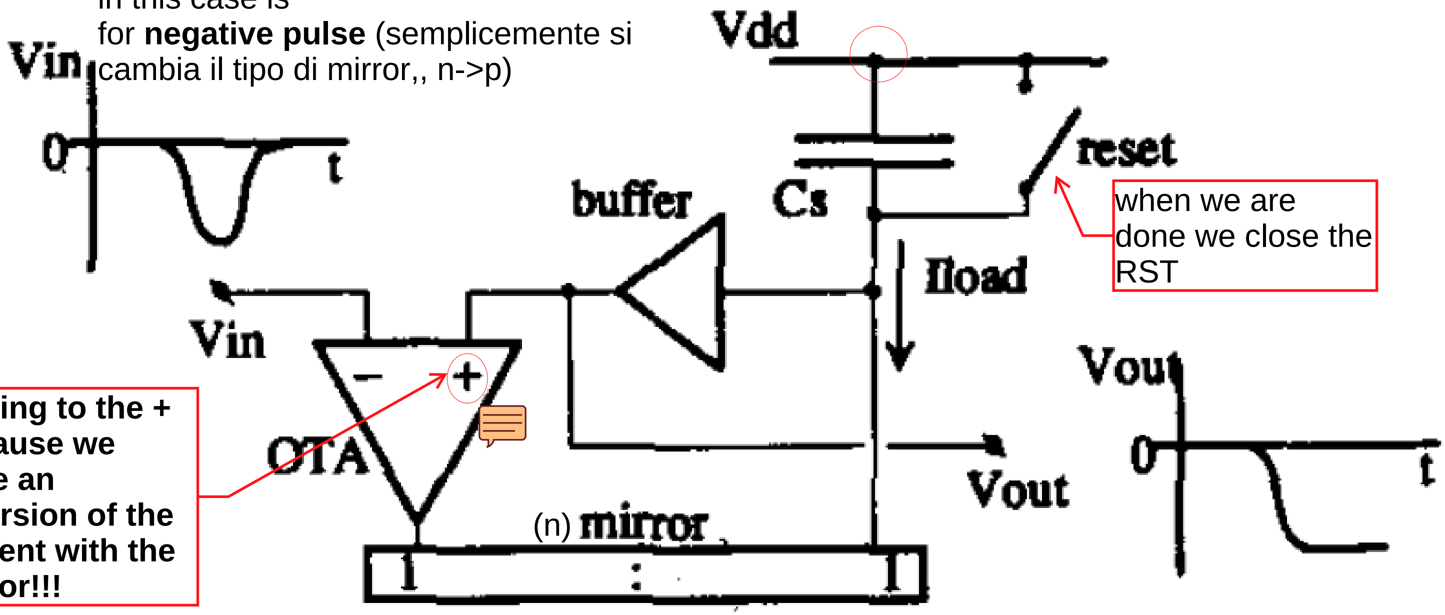
Candidate for subsistute of diode: current mirror. Why: it's On as long as you have an input current in THAT direction (example NMIRROR under). It's a current buffer. If you try to feed the current in the opposite direction it cannot work![indeed that was why we used a diode]

The integrated Peak Stretcher: a current mirror used in place of the diode



Peak Stretcher implemented with CMOS

in this case is
for **negative pulse** (semplicemente si cambia il tipo di mirror,, n->p)



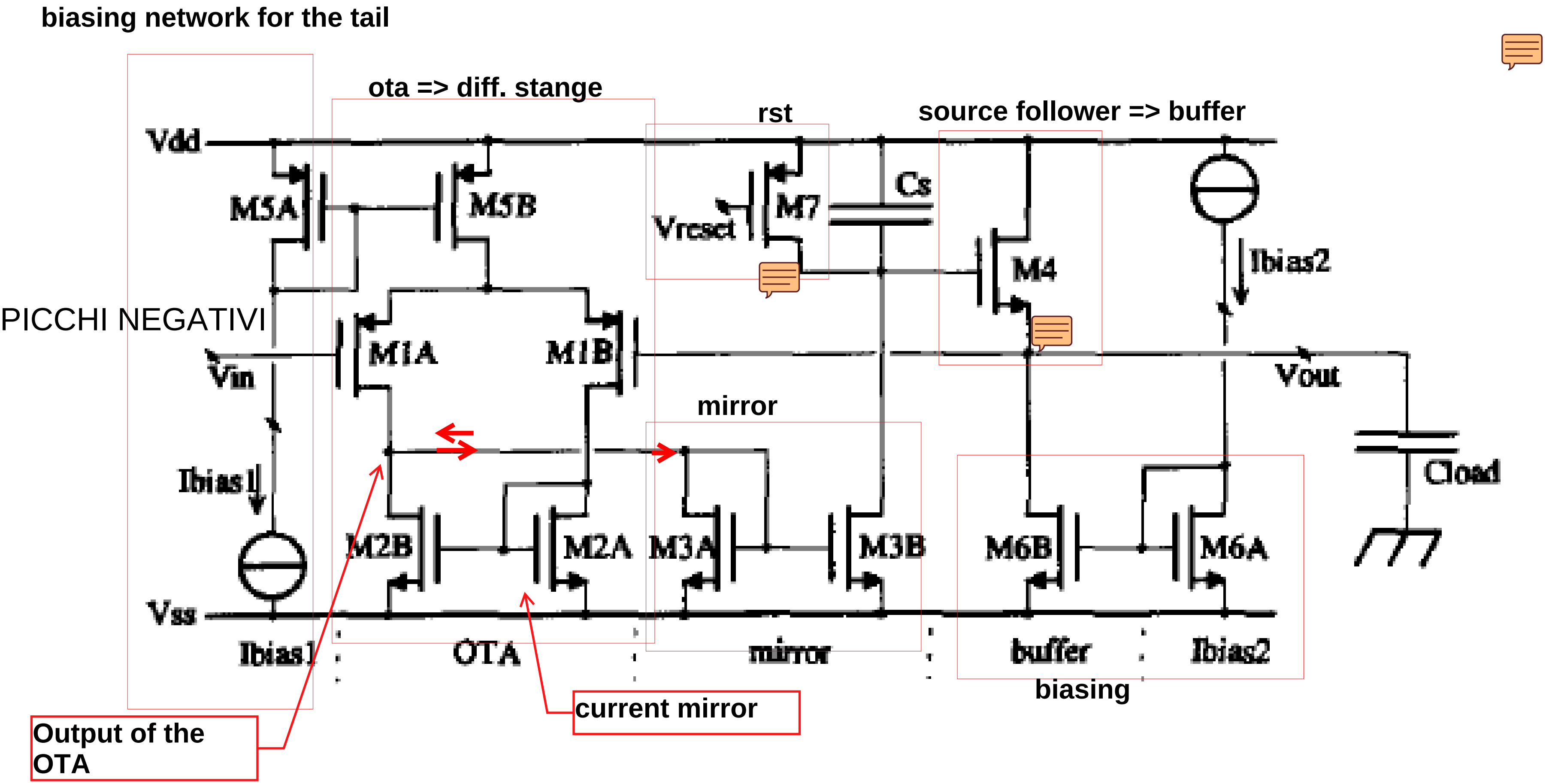
when we are done we close the RST

closing to the + because we have an inversion of the current with the mirror!!!

1.input drops down, is lower than V+, a current is driven at the output, we are PUSHING a current into the mirror, we have an entering output current in the other part (Iload). which is "disharching/dropping" the voltage on VCs. The node drops down, and there's the buffer with a closed loop and tracking of the output. Once we pass the peak the OTA tries to have current in the other direction, but the mirror can't! IT **SWITCHES OFF**! Cs stops to change voltagae. We have frozen Vcs, and V+, and the output voltage.

REAL SCHEMATIC

.doc



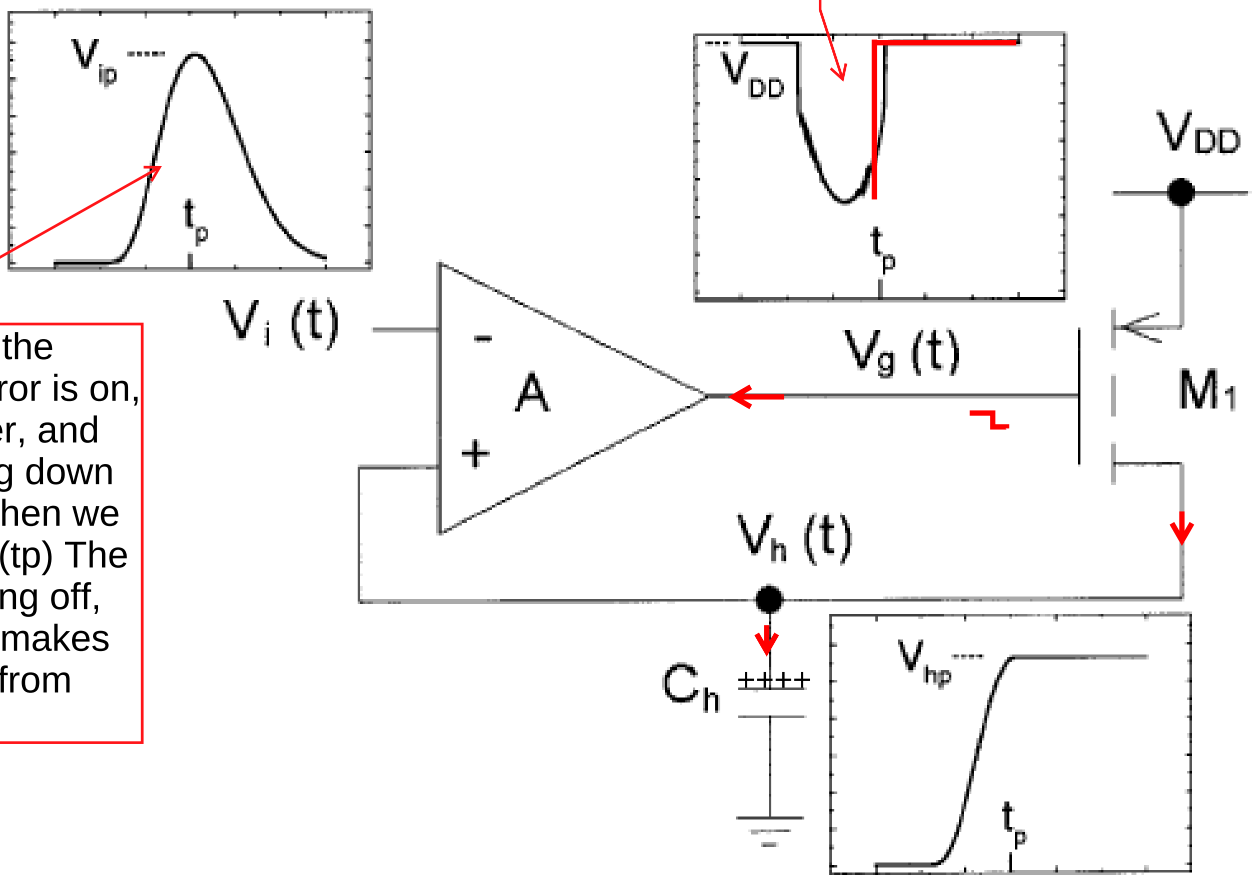
1) $G_{loop} = -GM_{OTA} \cdot 1/SC_S$

2) "Droop rate" = $dV_{out}/dt = (I_{offM7} - I_{offM3B})/C_S$

3) Figure of Merit? we need to dimesnion various W/L. => 1. LOOP GAIN (when we are tracking the input, we'd like to have the best possible replica) Cutting the loop at the output and appliying a generator, we have the gain, which is the transconductance of the ota (each of the input of transistors), then it feeds into the mirror(g=1), then it's converted into V. with Cs (1/sCs) then buffer. So we have a frequecny dependent loopgain. We need to check the loopgain in the BW of our signal. There's not an unic dimensioning of the loop gain, the design depends on where we have our signal!! if it's high freq. it's hard! if it's at low freq. it's easier. btw this just means: slow gaussian pulses, fast gaussian pulses![it's more challenging to track the peak of a fast pulse! we have to have a high loopgain] If the loop gain is low, the peak stretch cannot track the steepness of the pulse, and just take a part of amplitude :(We either increase Gmota or put a low cap. Indeed if it's small.. it was a good idea to put a buffer!

positive polarity

voltage on the gate of TWO transistor of current mirror



when we are in the tracking the mirror is on, we have a buffer, and the gate is going down (is a PMOS). When we reach the peak (tp) The mirror is switching off, hold phase. Vg makes a "pulse down" from Vdd.

ignora il circuito e pensa solamente alla tensione Vg dei mirror. all'inizio c'è differenza, viene erogata corrente (in questo caso negativa, quindi avremo dei pmos). Più tirano corrente dal mirror, più la Vg dovrà abbassarsi (siamo in PMOS.. come nel disegno). Quando smette di essere prelevata corrente, perché hanno raggiunto la parità gli ingressi, l'unica condizione è Vg = Vs, che nel caso del pmos è Vdd. (*Vg = Vs spegne il mirror)

3 options for the buffer.

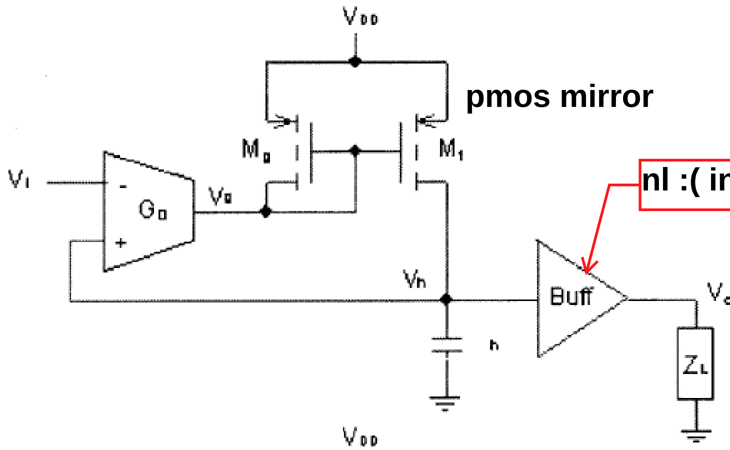
Why a buffer: in principle we can do a loop without the buffer and it would work. PROBLEM: it's also the output node. If we close the cap to the output without buffer, it's loaded with external loads. With capacità parassite. Se non facciamo buffer ci vanno in parallelo (come nel CCD)

1. close the loop directly, and then external-to-the-loop buffer. Not usually a good idea, because we introduce the NL of the buffer.

2. BEST! use a "nice buffer", opamp in buffer mode (Vout=V-), inside the loop, preserving the quality of output vs input, b/c buffer is in the input. Problems: we introduce in the loop the singularity of buffer TDF. So for stability of loop we need to consider also the pole of the buffer. BTW when the loop is closed the overall circuit is a buffer.. which is usually the most probable to be unstable (lowest gain, largest BW).

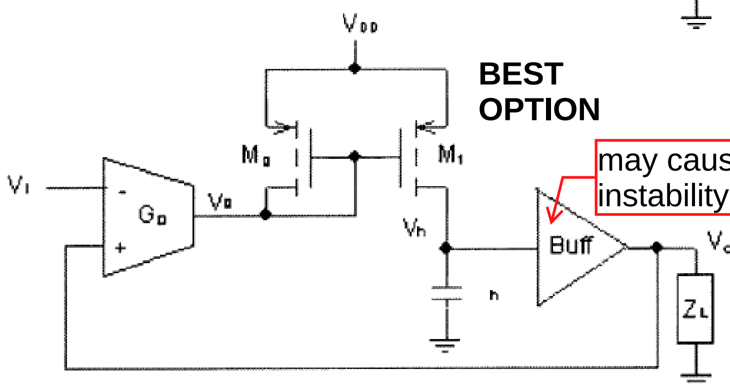
3. advantage: just single stage transistor, which usually has a large BW.

same circuit for positive polarity: same circuit just flipped for polarity.



pmos mirror

nl :(introduced

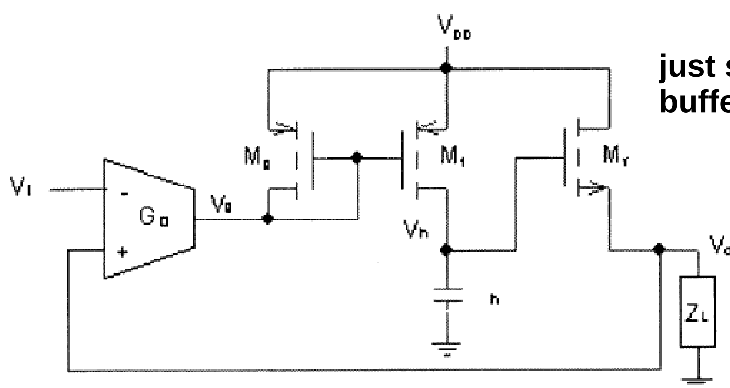


BEST OPTION

"nice opamp"
instability due to opamp TDF

may cause instability

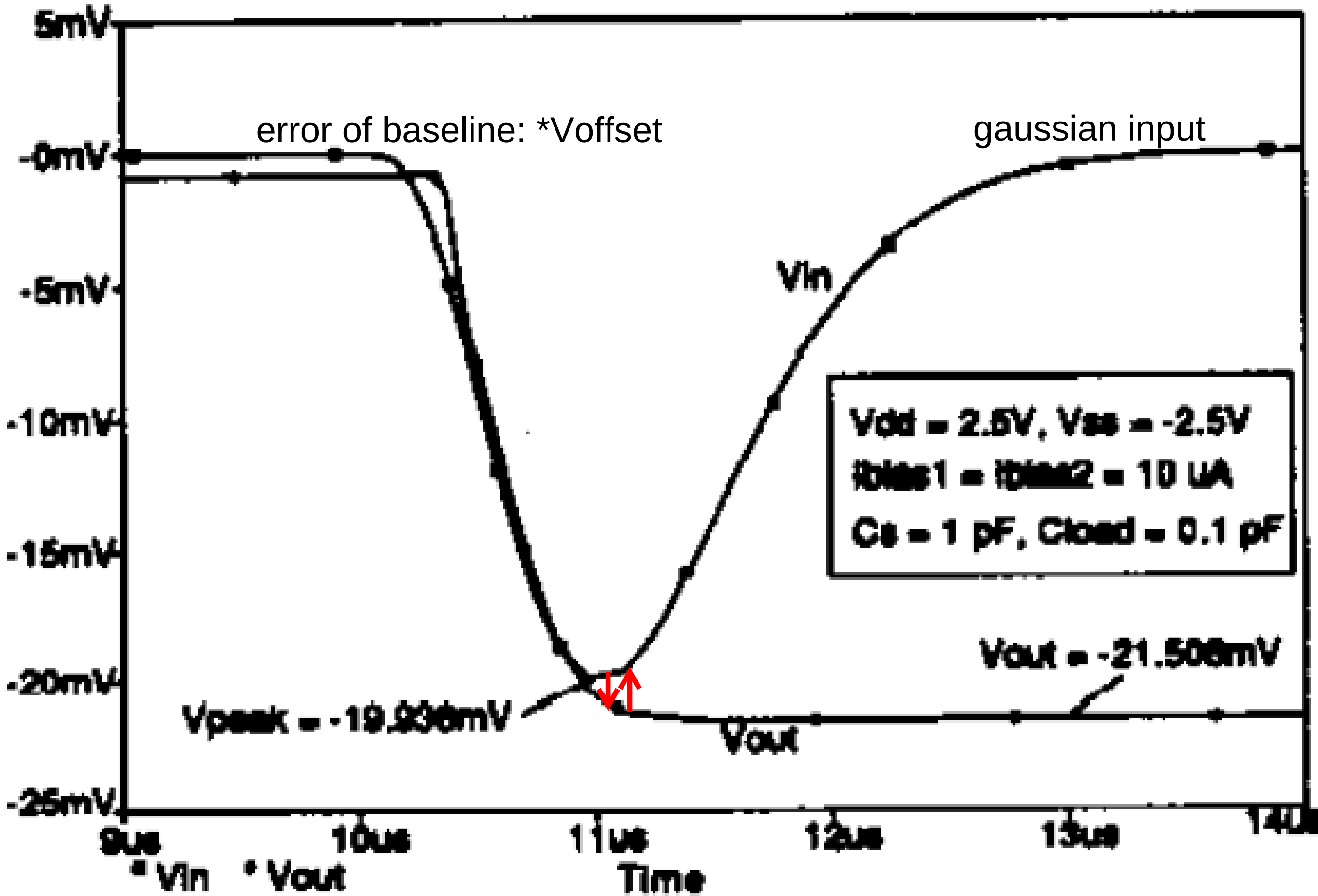
reason why we use a buffer



just seen:
buffer made with SourceFollower

only one stage
large bw

negative pulse

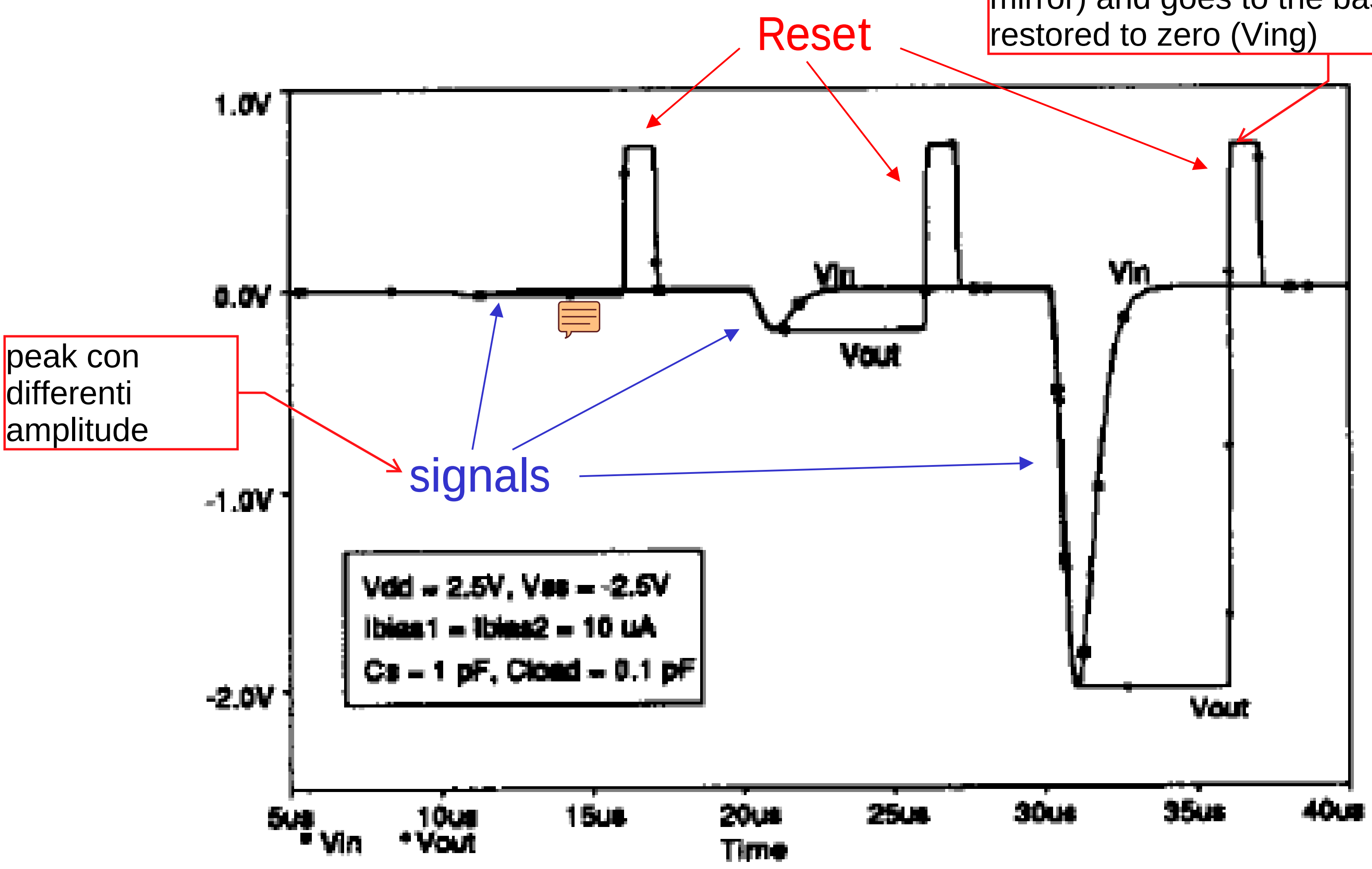


Per il max abbiamo:
- overshoot (il mirror non si è spento abbastanza velocemente)
- undershoot (GLOOP basso)
- overshoot/ushoot presenza di un offset dell'opamp

DC offset and error on V_{out} limited by OTA bandwidth and by the speed of the current mirror to switch off

The gap represent how good/bad you were in the design. If the loop gain is limited we can't track very well. Extra voltage: b/c the mirror has to be switched off,, but if the speed of the loop is not sufficient to turn it off, for a small time we give current to the cap, which is extra charged.

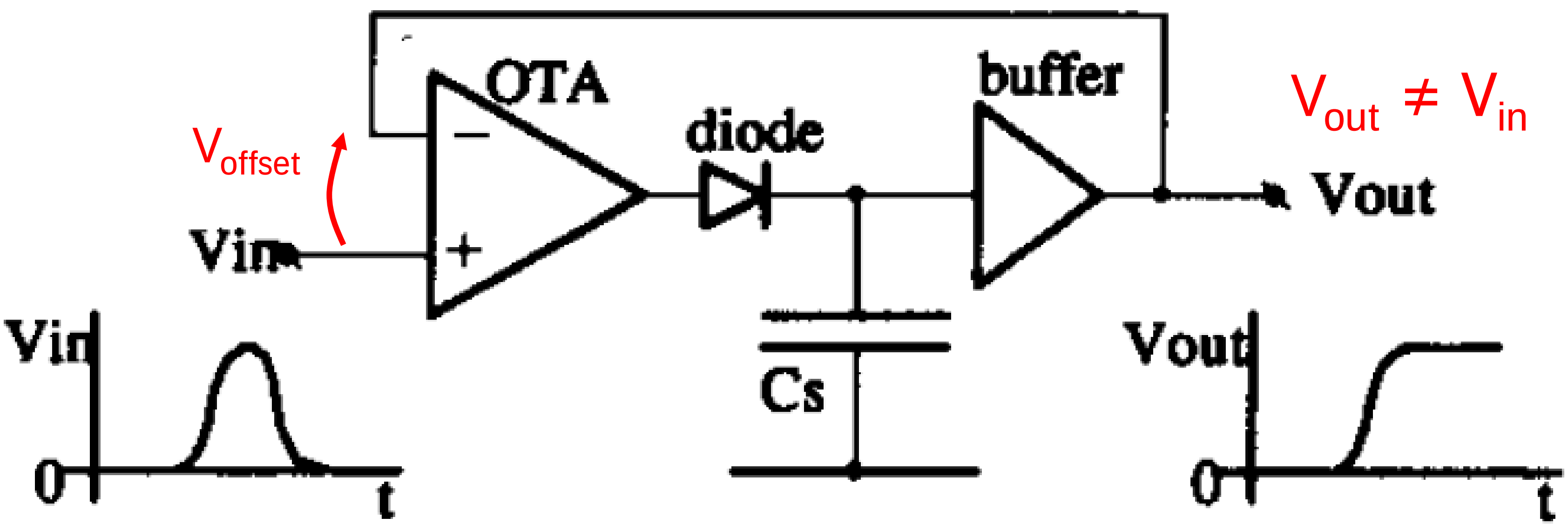
you dont reset to ground but to vdd. Once you release the peak stretcher finds itself in tracking mode! So it turns on (the current mirror) and goes to the baseline, while it's restored to zero (Ving)



Why resetting to Vdd: this way we can automatically track the baseline of the shaper, whatever it is. (Zero in the graph... won't really be zero). In questo modo possiamo fare il tracking verso ogni baseline.. se il cap. fosse stato chiuso vs ground non possiamo essere certi che fosse uguale al ground di ingresso. Whatever pulse we have, same reset. (*Ma cmq) if the loop is not perfect, again the tracking of baseline is not perfect (slide 7). significa semplicemente che se c'è voffset allora nemmeno il tracking della baseline viene fatto correttamente!

problem: OFFSET OF THE OTA, due to mismatch of differential pair. 0ddp => not 0 output => means Voffs at the input. Simply means, output not equal to the input, Vout = Vin + Voffs.

Limit of the traditional configuration (with both diode and mirror configurations): offset of the OTA

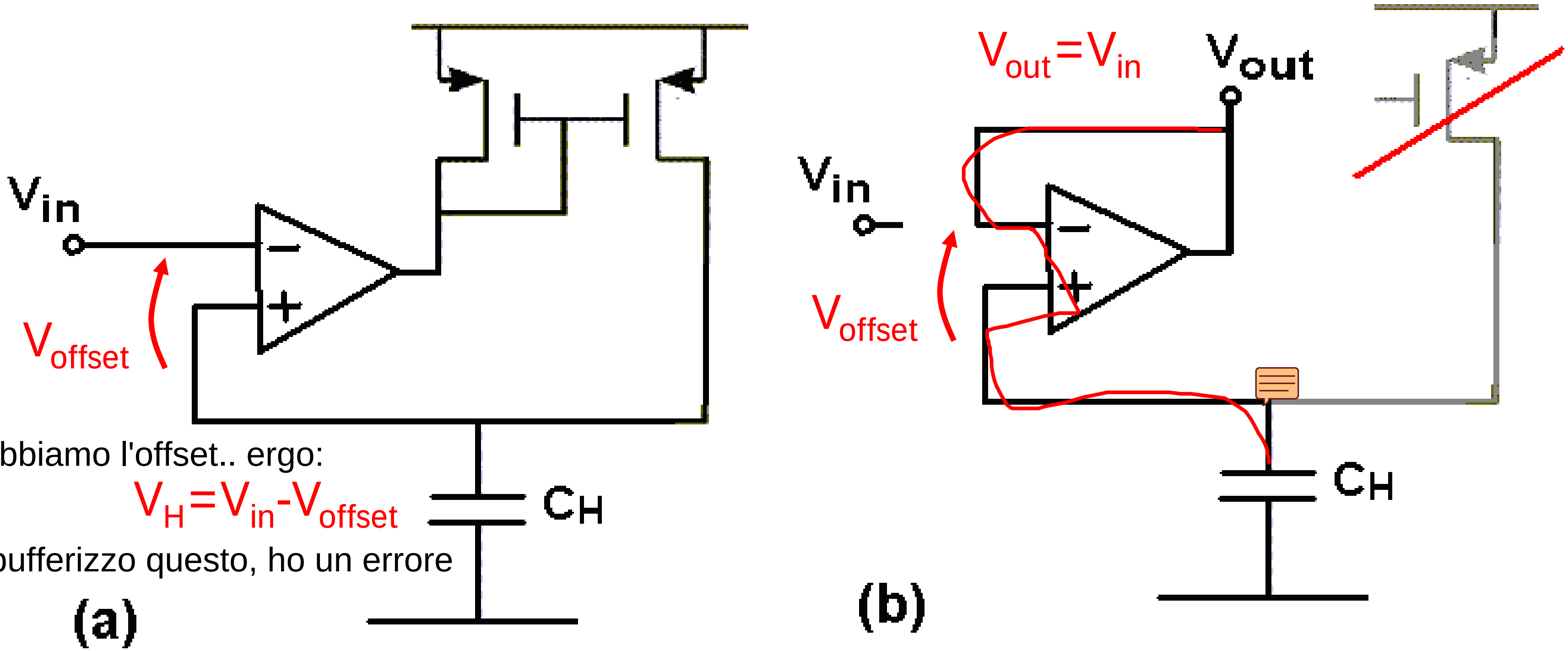


This is a problem if we want output exactly equal to the input. SOLUTION: next slide

(here there's not the buffer ma non c'entra con la soluzione)

Solution: "two phases" peak stretcher

traditional peak stretch, tracking phase



abbiamo l'offset.. ergo:

$V_H=V_{in}-V_{offset}$

se bufferizzo questo, ho un errore

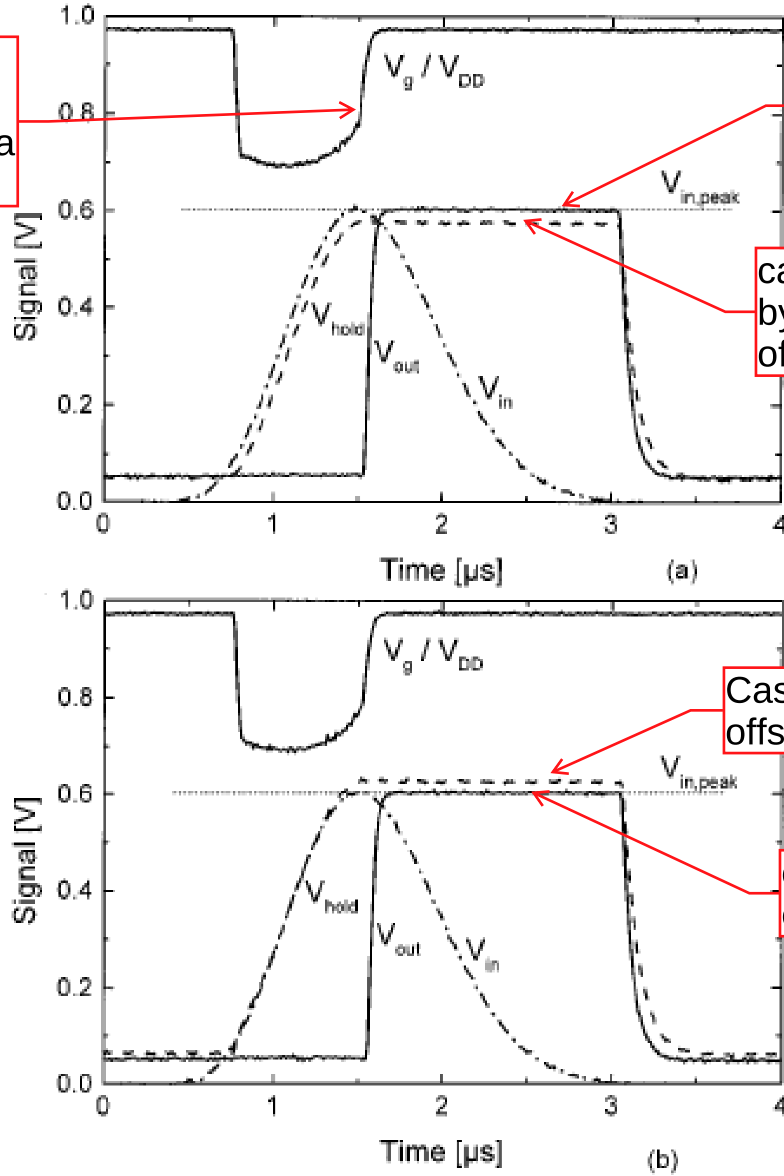
a) normal operation

b) amplifier operated as buffer

il vgate sparisce quando inizia la fase di hold!!

voltage amp. closed as a buffer. THE OUTPUT IS IDENTICAL!

case: affected by negative offset.



Case: positive offset

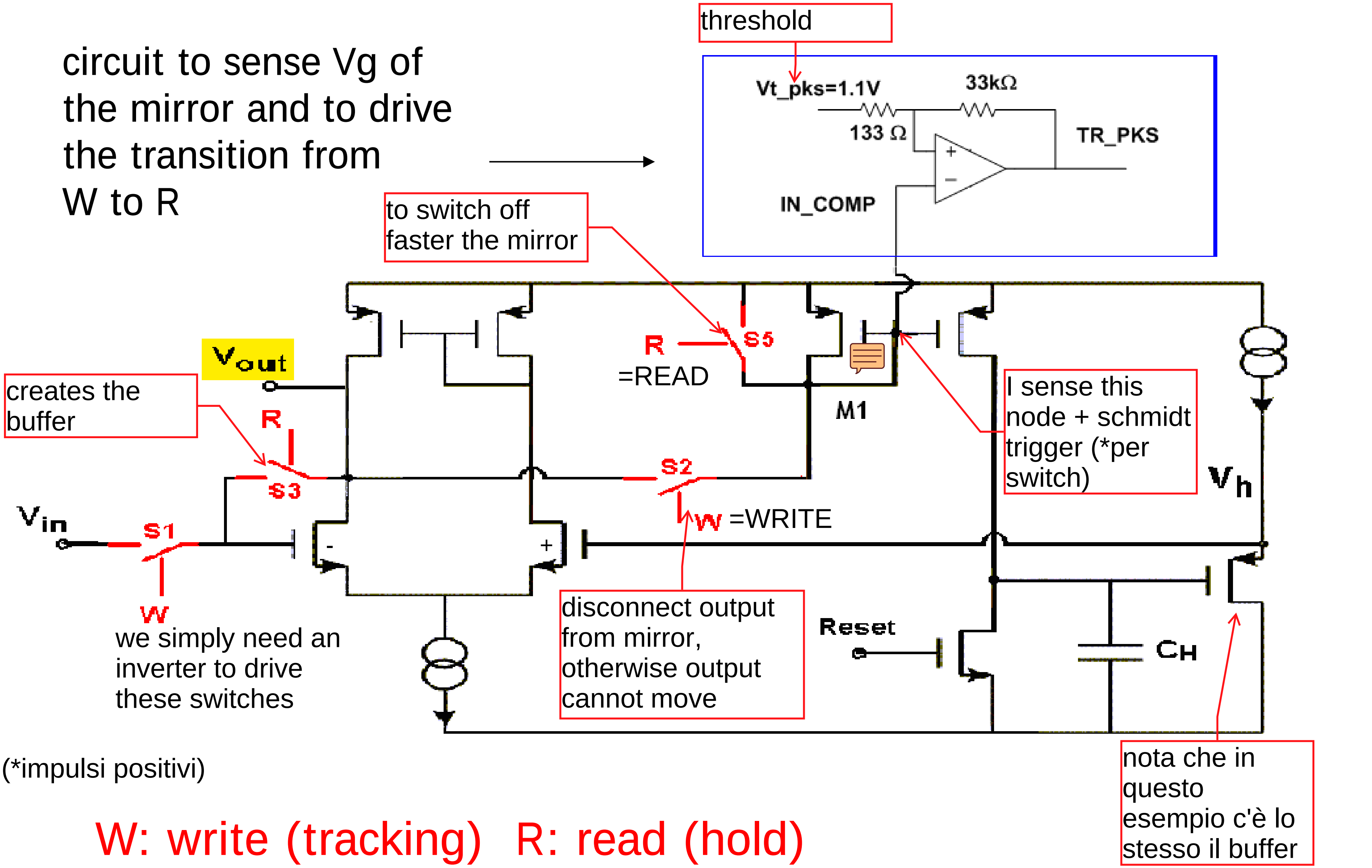
output of buffer equal!

example of response in case of offsets with opposite sign

(V_g: gate voltage of the mirror MOSFETs)

Con gli switch di cui ho bisogno...:

circuit to sense Vg of the mirror and to drive the transition from W to R



(*impulsi positivi)

W: write (tracking) R: read (hold)

Quindi.. che segnale digitale usiamo per fare il driving di questi switches? IL GATE VOLTAGE Vg(t), che fa una sharp transition quando sono al peaking time. Quindi, il trigger per il transformation è generato autonomosly using Vg.

Derandomization of the events

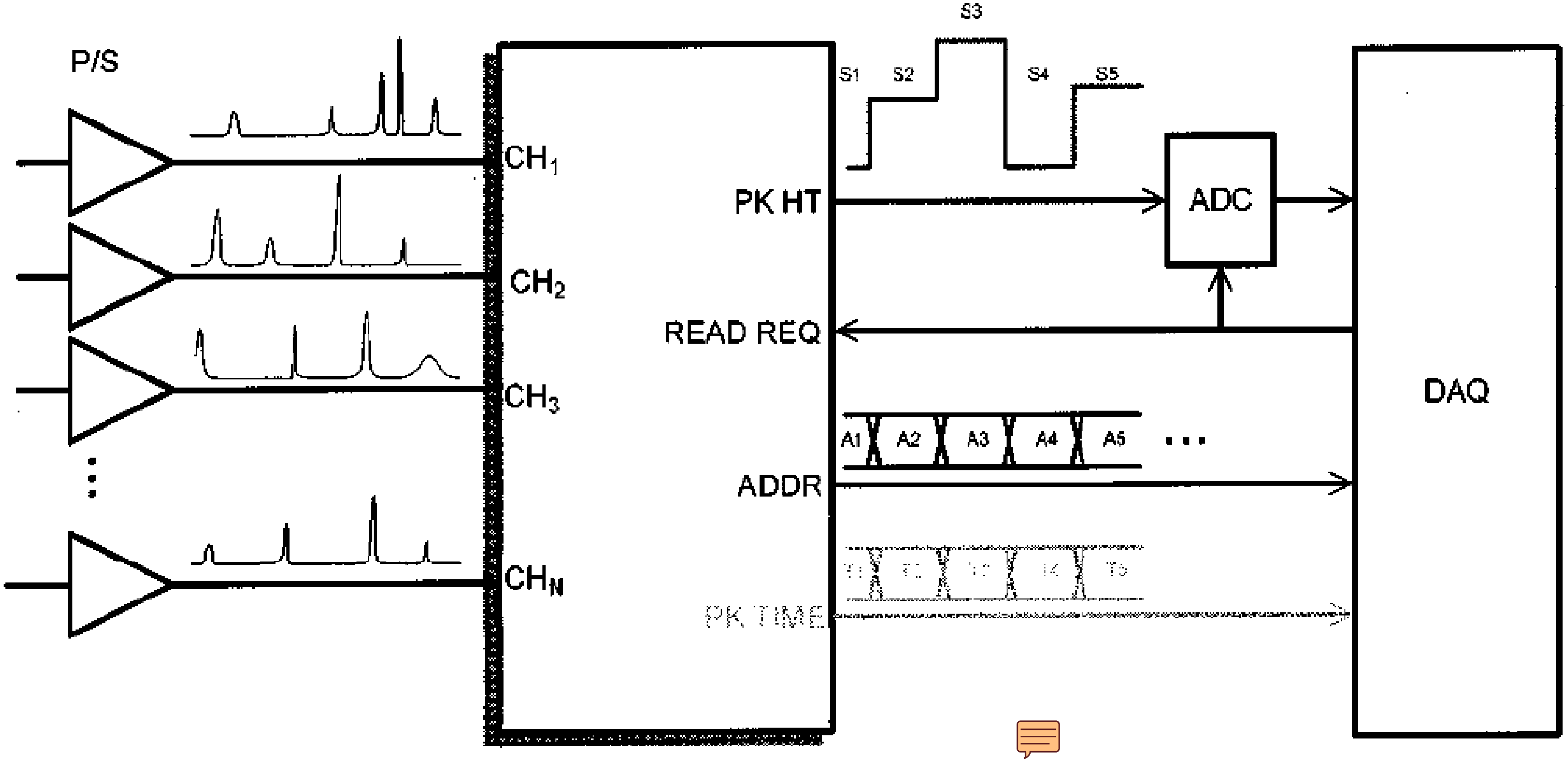
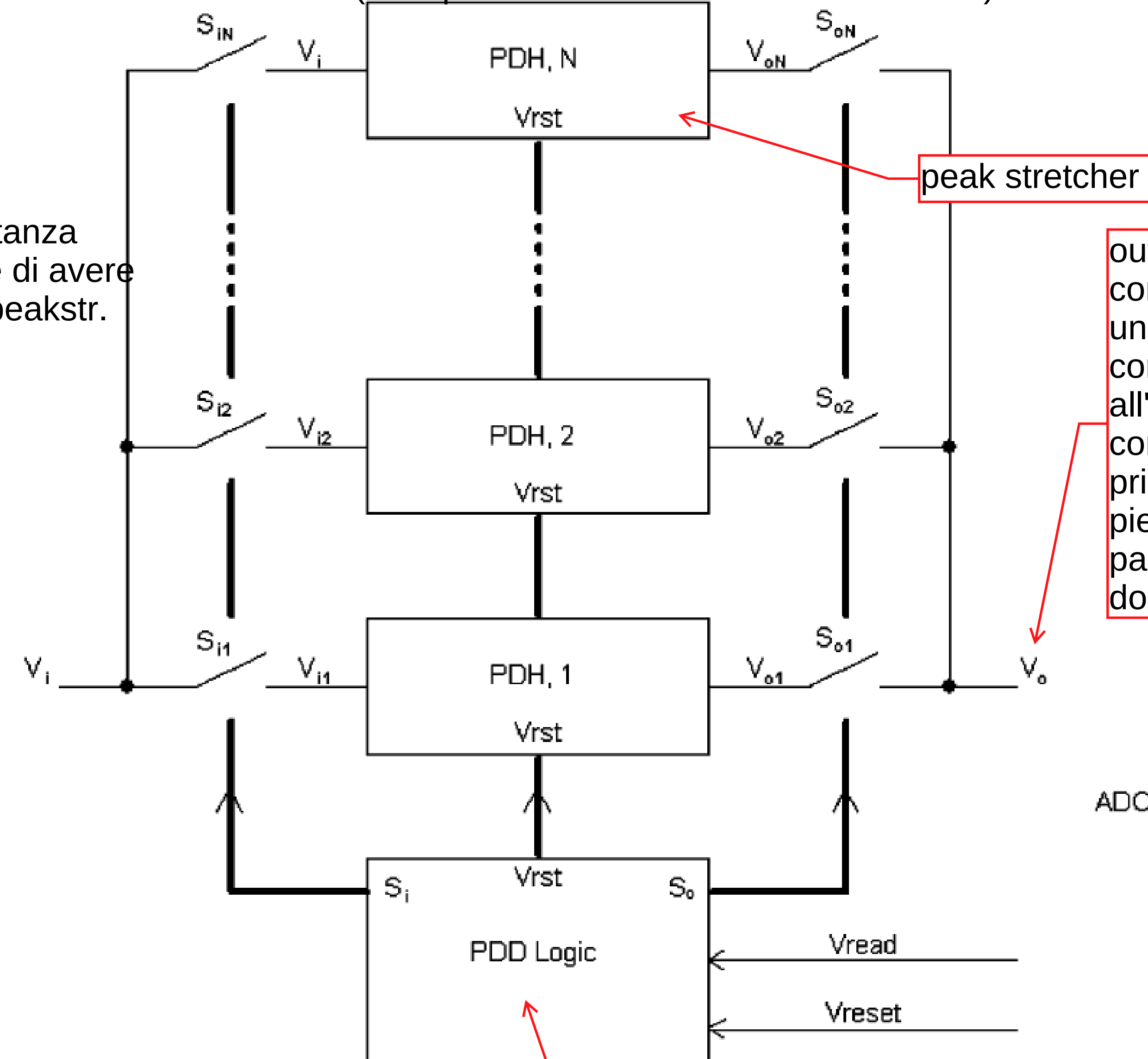


Fig. 6. Ideal self-triggered, self-sparsifying, derandomizing, and dead-timeless multichannel readout system.

Powerful use of peak stretcher: **ANALOGUE MEMORY** (as long as the ADC has not converted, we have a storing of the analogue value of Vin_peak). We can use this to solve problem in pulse processing for detectors: photons in the various channels arrives totally random. Vorremmo un adc che va in running con una det. frequenza però : (disegno quaderno. Ovviamente se tadc = average arriving pulse, non è abbastanza, perché significa che abbiamo gruppi di eventi che arrivano più velocemente, ed altri più lentamente.

CASE: SINGLE INPUT, in caso di arrivo viene connesso al primo peak stretcher available (che quindi non è in attesa di essere letto)

Dobbiamo avere N peakstrecher abbastanza grande per garantire di avere sempre almeno un peakstr. free.

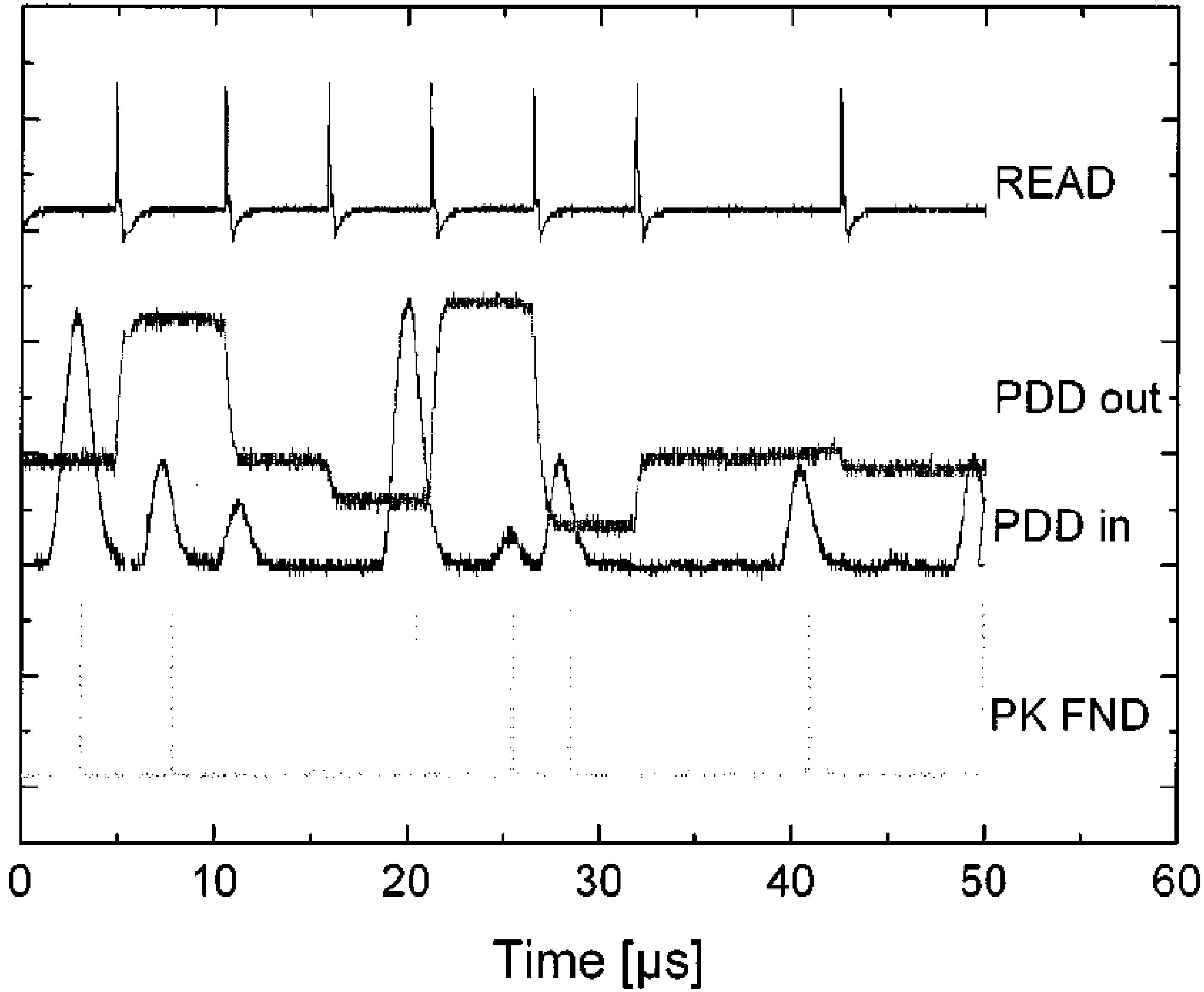


peak stretcher

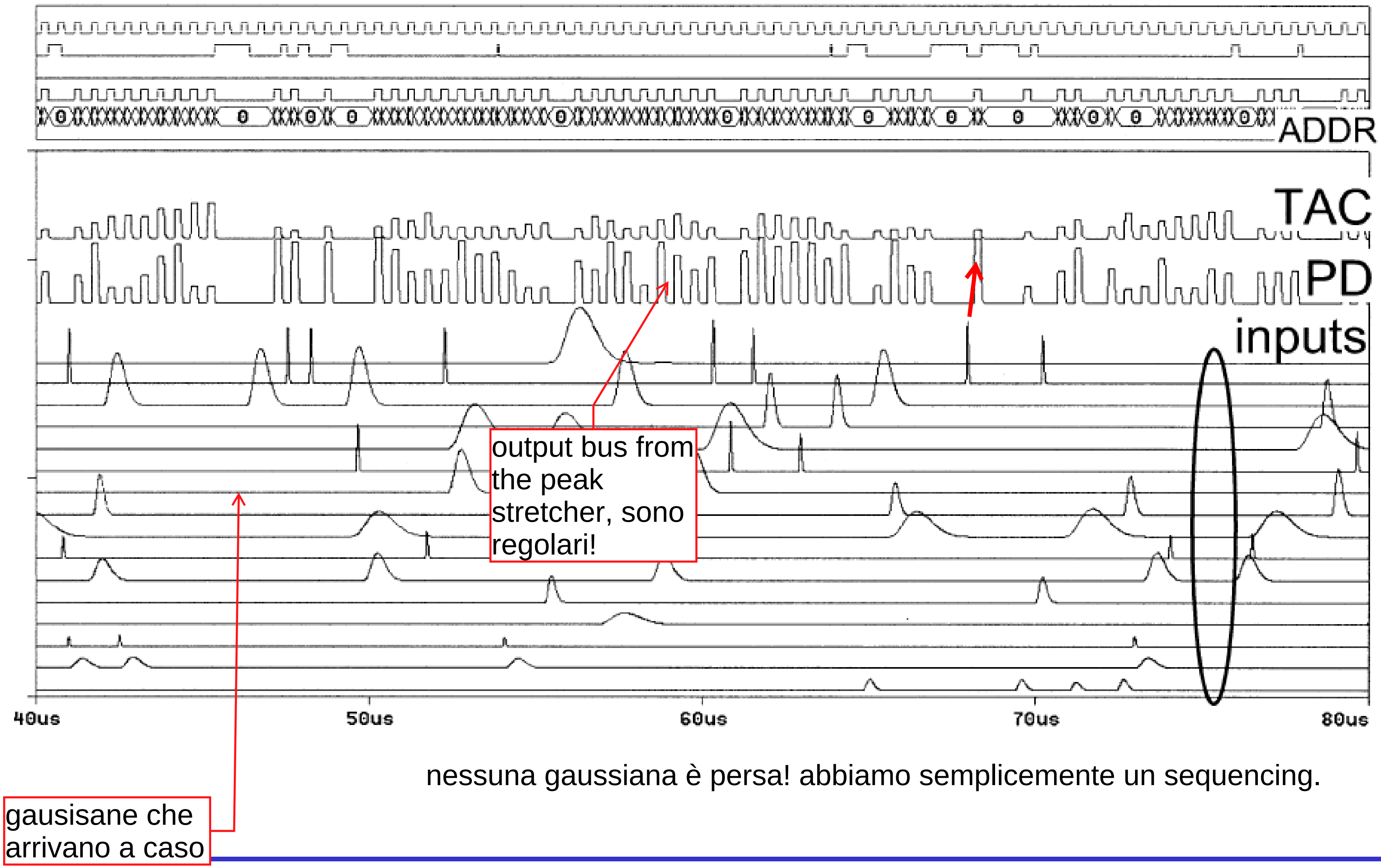
output connessi su un unico bus connesso all'ADC che converte il primo peakstr. pieno. (poi passa a quello dopo etc.)

logica per fare funzionare tutto

no



..how it works



nessuna gaussiana è persa! abbiamo semplicemente un sequencing.