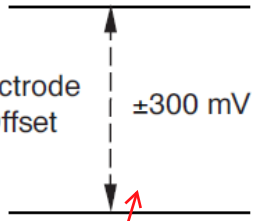
Why do we need an INA? Summary of voltage level in typical signals in electrocardiography.

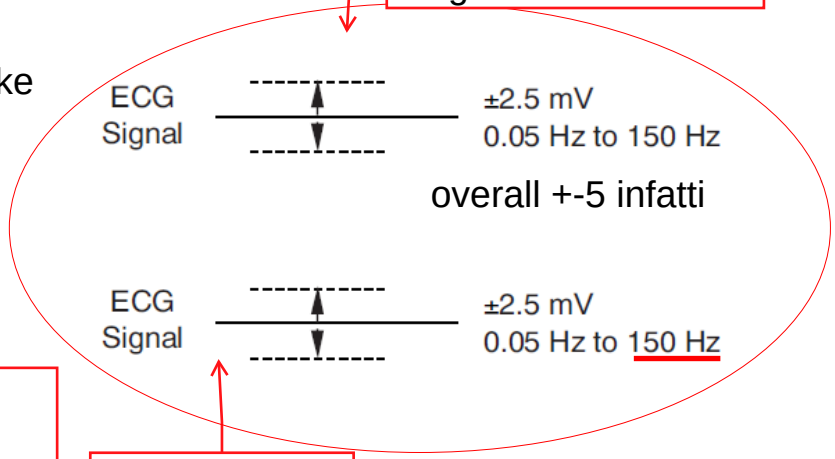
CM across the body. It's floating, irradiated by EM waves. :(Could be up to 10V. IT's not constant! that you would reject with fully AC coupled. It's slowly variable CM. 50Hz, freq of power lines. [* ci sarebbe anche una componente DC derivante dal contact potential degli elettrd]

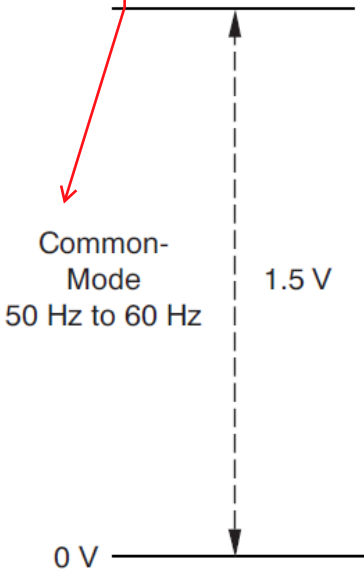
ECG signal characteristics

We want the differential of this, superimposed to other things

*segnale differenziale, Vdfake

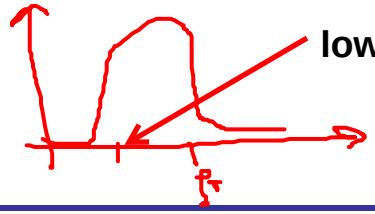






Volt difference created by the common mode. Only hope: it's almost DC, in this case we may reject using a low freq pole of ampop. [vedi: lect5, 5]
Mismatch b/w Z1 e Z2 + Rin != inf
"electrode" b/c Zs are el. impedances

Each electrode provide a signal



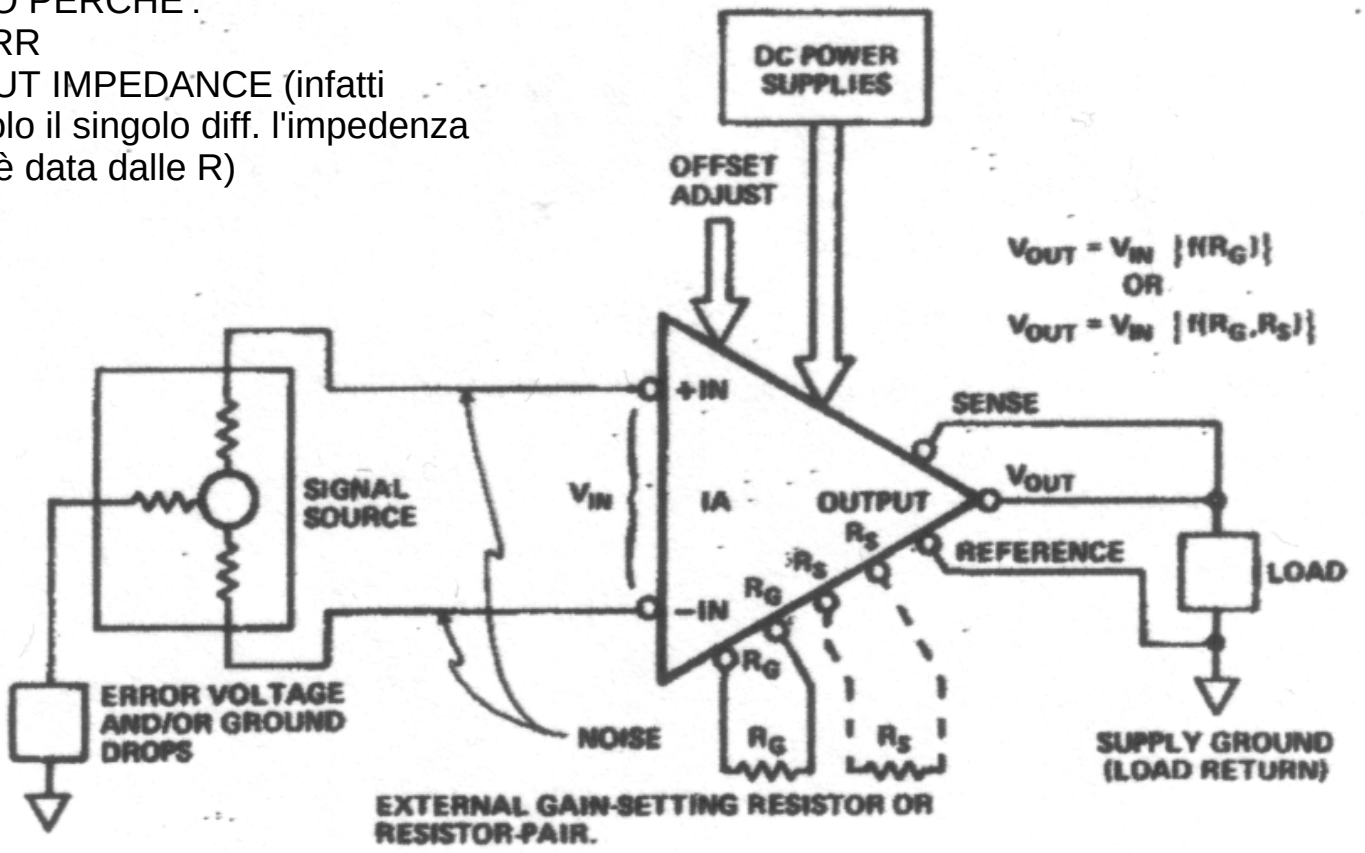
low freq rejection to be insensitive to DC differential signal

infatti ecg hanno bp attorno a 50hz tipicamente, come ad es zadeh 50+-30 hz; od il ventricular sense

technical note cover this

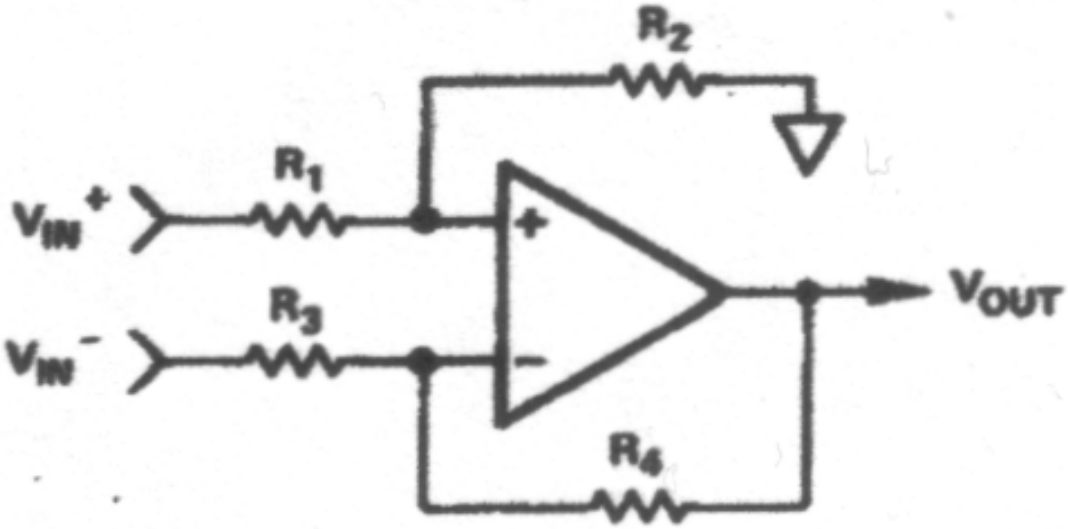
Instrumentation amplifiers

*INA USATO PERCHE':
- HIGH CMRR
- HIGH INPUT IMPEDANCE (infatti se prendi solo il singolo diff. l'impedenza di ingresso è data dalle R)



- High input impedance, suitable for sources with high and unbalance impedances
- High CMRR, necessary for large common-mode voltages

Differential amplifier



$$V_{OUT} = V_{IN}^{+}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right) - V_{IN}^{-}\left(\frac{R_4}{R_3}\right)$$

if $R_4/R_3 = R_2/R_1$

$$V_O = \left(V_{IN}^{+} - V_{IN}^{-}\right)\frac{R_4}{R_3}$$

This is not good because the input impedance is not infinite, quite small, thus' not good. "Perfect differential amplifier" if V+ = V- => Vo = 0.

Common mode rejection

$$V_{OUT\ CM} = V_{OUT} \text{ for } V_{IN}^{+} = V_{IN}^{-}$$

$$= V_{IN}\left[\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_3 + R_4}{R_3}\right) - \left(\frac{R_4}{R_3}\right)\right]$$

If that equation (R1 = ... etc.) is not fullfilled we have a sensibility to CM :(

$R_1 = R_3 = R_4 = R$ ← Theoretically, but R2 deviates from R by 1 ppthousand; mismatch. [In this case we would have 1 as a differential gain]

$R_2 = 0.999R$ e.g., R2 sbaglia di 0.1%, significa che c'è un guadagno CM

$$V_{O\ CM} = V_{IN}\left[\left(\frac{0.999R}{1.999R}\right)\left(\frac{2R}{R}\right) - \left(\frac{R}{R}\right)\right]$$

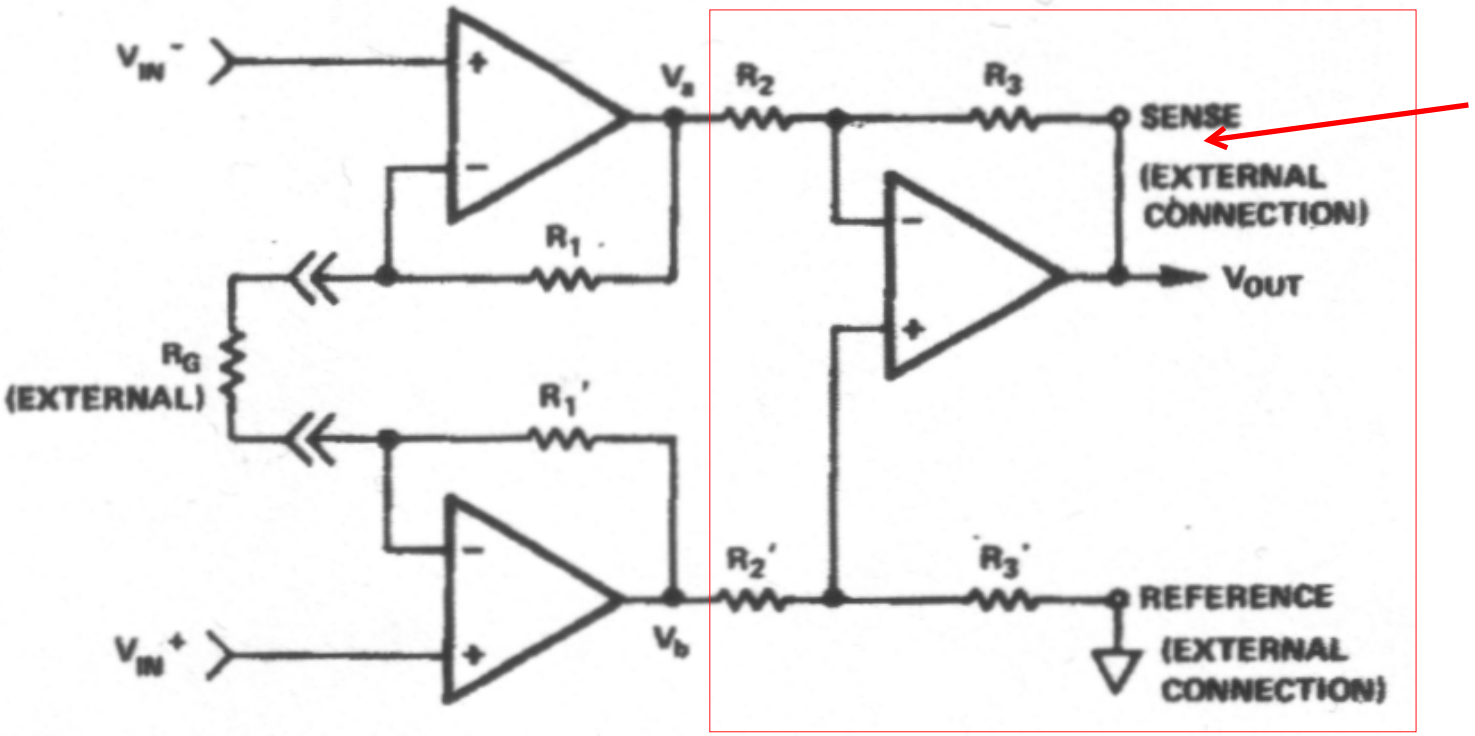
$= 0.0005V_{IN}$ ← Output not zero! 66db is bad, we need at least 100db

$CMR = 66dB$

if source impedances are low and/or unbalance, CMRR worsens further

[breve e veloce spiegazione sul gain del primo blocco, differenziale e CM]

Instrumentation amplifier with 3 OPAs



In principle insenstive to CM :).

$$V_{OUT} = (V_{IN}^+ - V_{IN}^-)\left(\frac{2R_1}{R_G} + 1\right)\left(\frac{R_3}{R_2}\right)$$

Advg: 1) high input impedance 2)CMRR, for diff signal we have two gains multiplicated. For the CM the first part doesnt make current flow in Rg, thus G1cm=1.

Common mode rejection

$V_a = V_b = V_{CM} \rightarrow G_{CM1} = 1 \rightarrow G_{CMtot} = G_{CM1} \cdot G_{CM2} = 1 \cdot G_{CM2}$

$G_D = G_{D1} \cdot G_{D2}$

Il gain differenziale avviene in entrambi gli stage (prodotto dei due), il gain common avviene solo nel secondo, quindi abbiamo un incremento del CMRR

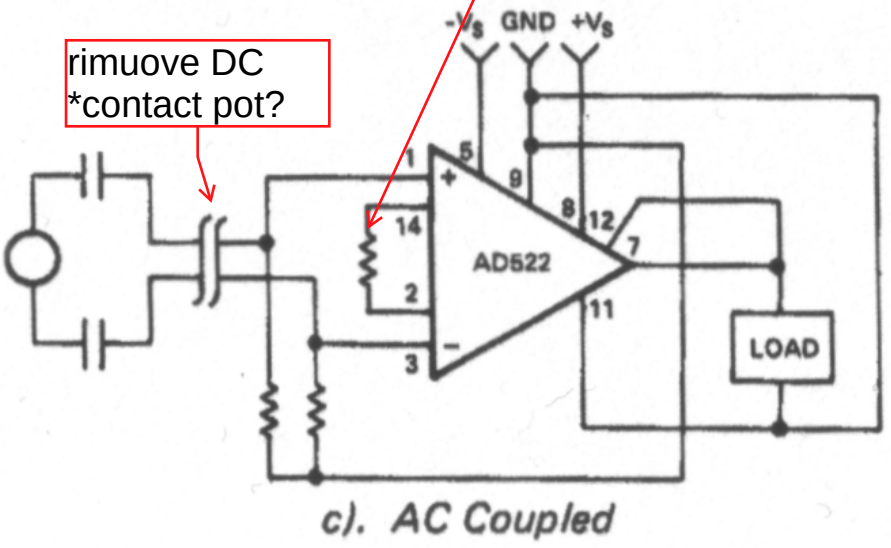
$CMRR_{tot} = (G_{D1} \cdot G_{D2})/1 \cdot G_{CM2} = G_{D1} \cdot CMRR_2$

$\Rightarrow$ CMRRtot increases with G_{D1}

(and does not worsen if R1 e R1' are different)

alto ed i mismatch rompono meno (*ring, *not Rgain)

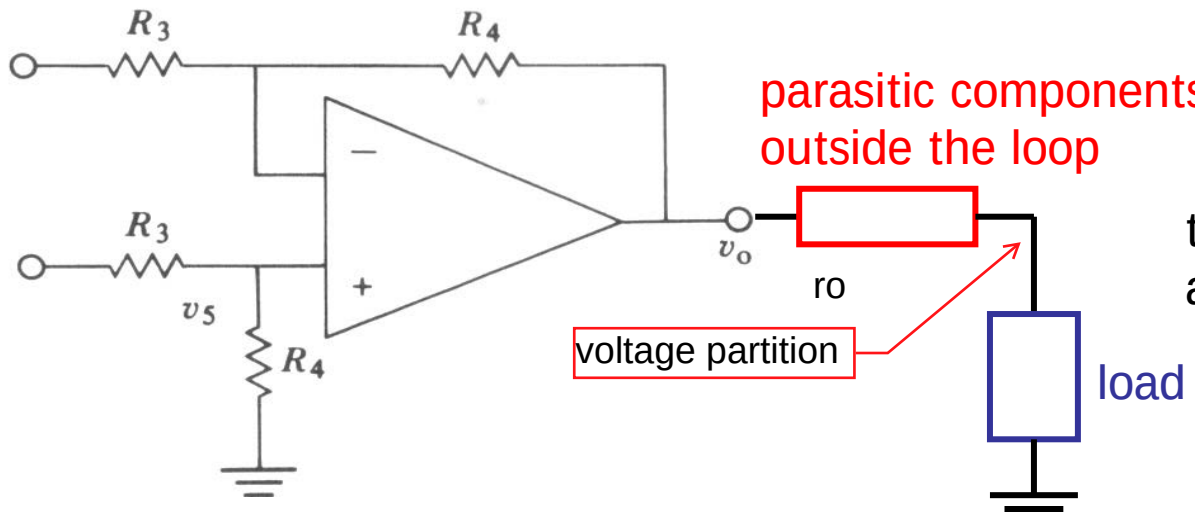
rimuove DC *contact pot?



notes: *JFET!! ring alta e 1/f minore che CMOS

- IA with FET inputs have larger input impedances and very low input bias currents
- remember to provide a DC path to discharge input IBias, in particular in case with sources AC coupled

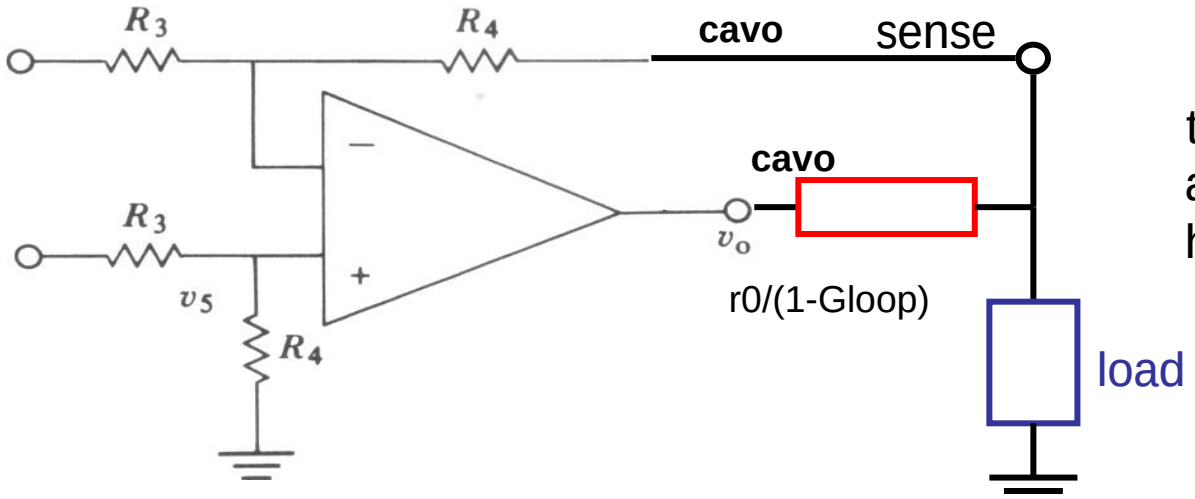
Role of the “sense” electrode



parasitic components (R,C,L) outside the loop

the effects of the parasitic are outside the loop

voltage partition with load :(

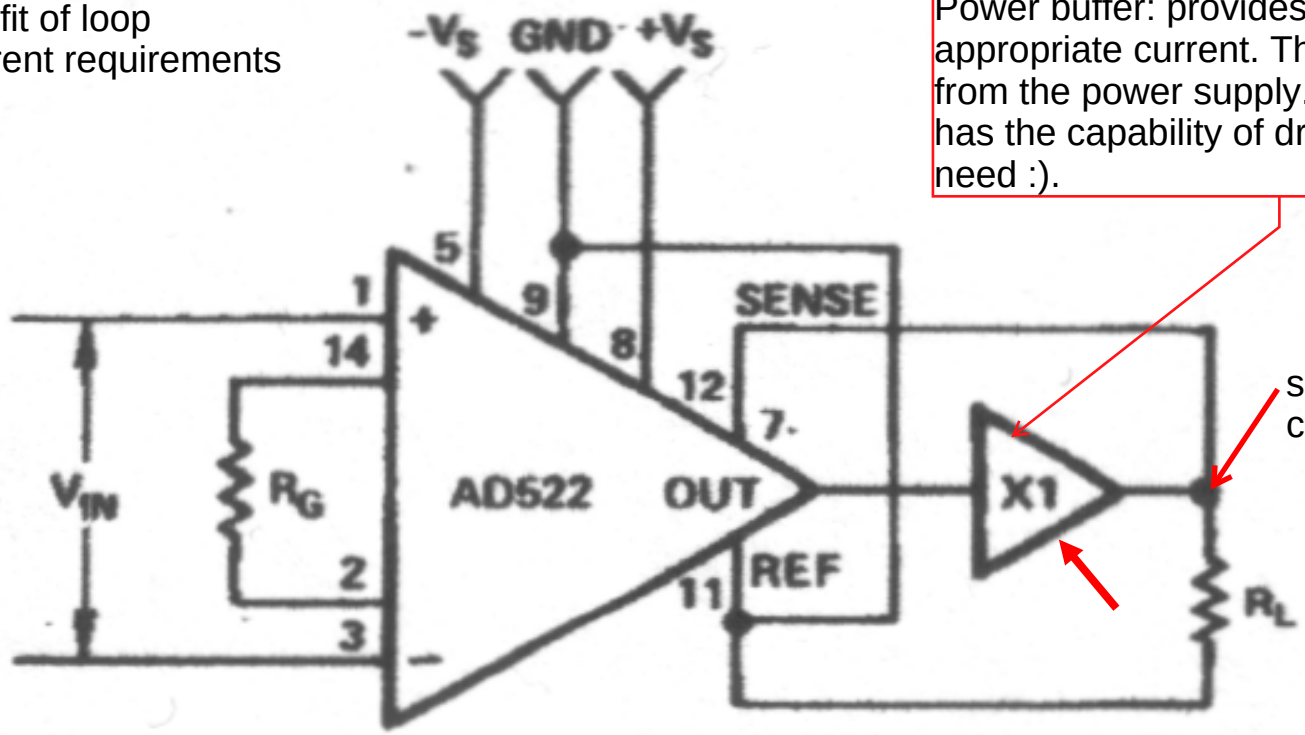


the effects of the parasitic are reduced because are held inside the loop

Another use of the “sense” electrode

Extend benefit of loop
for large current requirements

Power buffer: provides to the load the appropriate current. The current comes from the power supply. The power buffer has the capability of draw the current we need :).

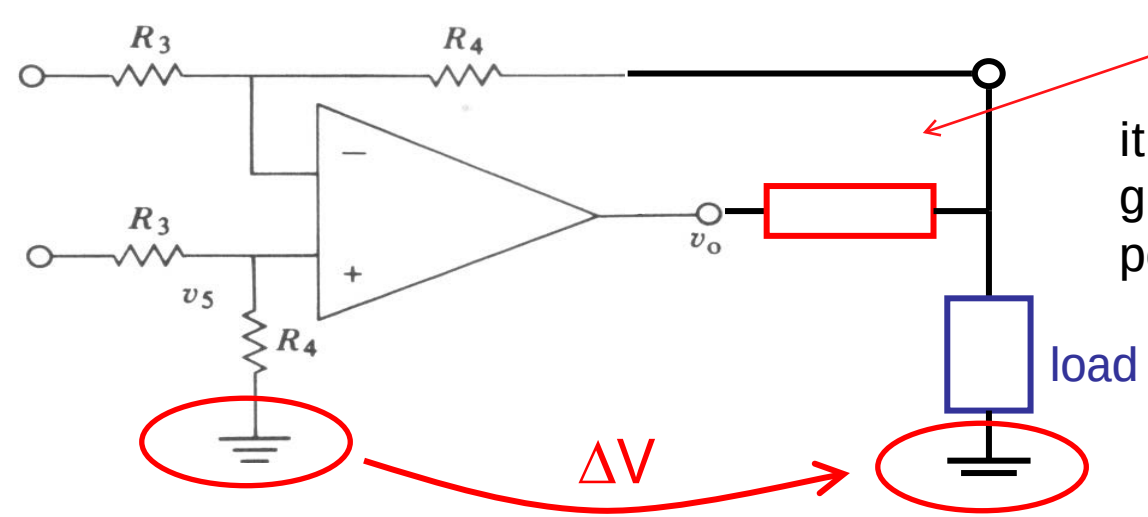


Current-booster output:

the driver provides high current into the load, but being inside the loop it does not change the characteristics of the transfer function

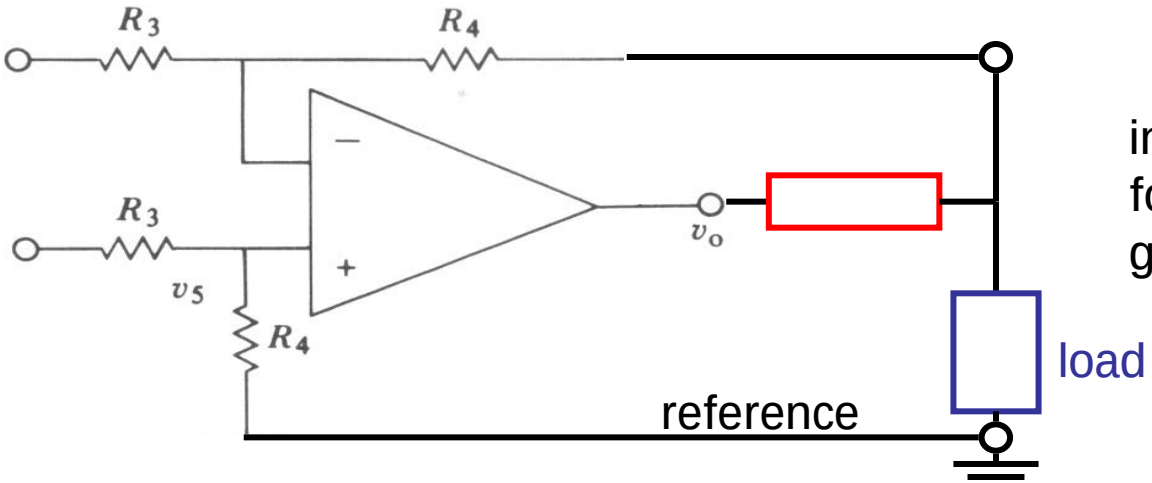
Another adv of the sense electrode. Generally speaking we need to provide current from the amplifier to the load. I0 = V0/Rload This could be very large (eg Rload bassa). In case of very large voltage across small resistor we may have a current req. from the amp which may exceed the ratings of amplifier :(eg 20mA max output. In this case we may add a power buffer! Again we dont want this outside of the loop, because we would lose the benefits of loop! With the sense pin we can include the power buffer into the output, closing the loop on the load!

Role of the “reference” electrode



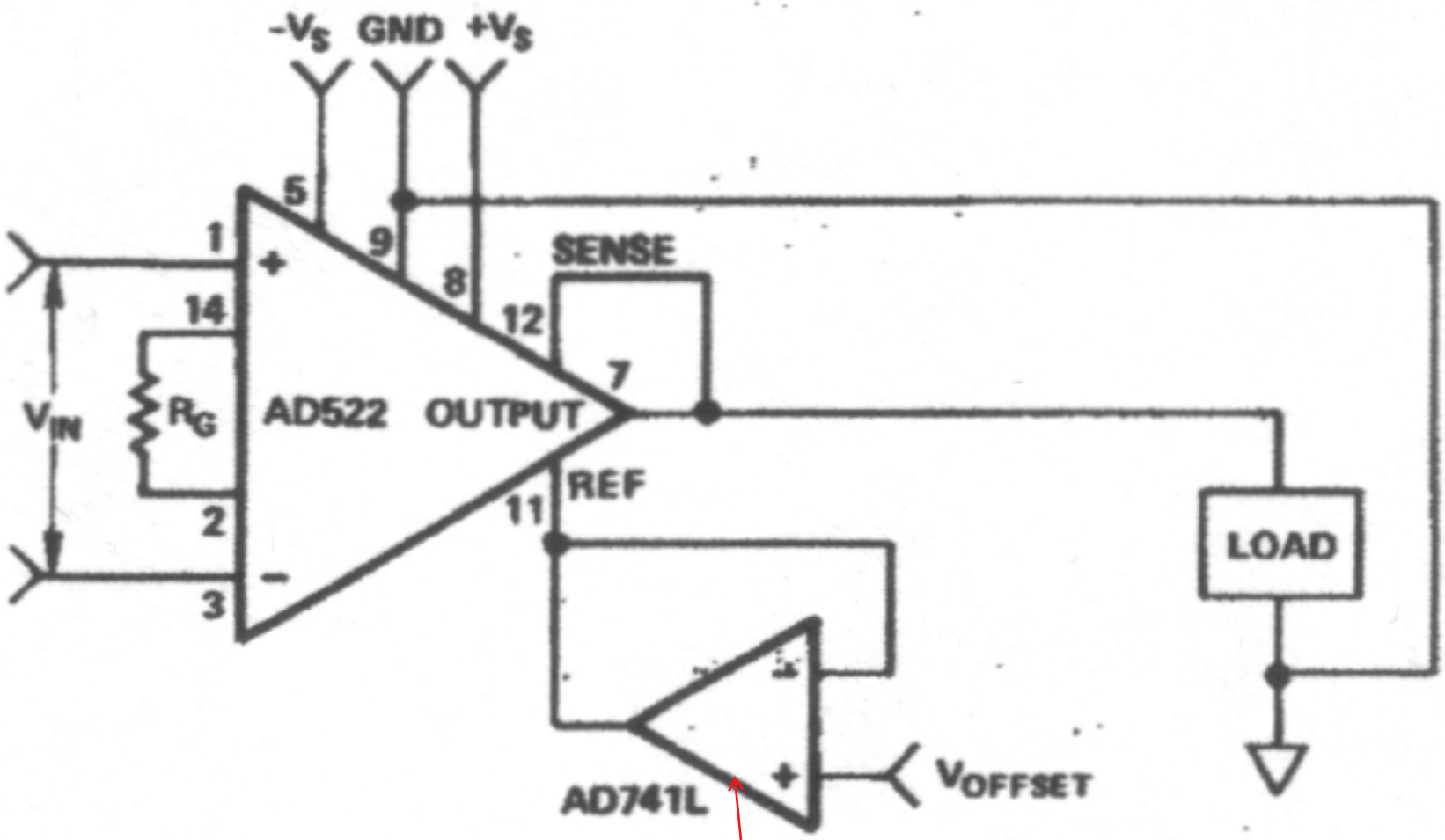
it could happen that the grounds are at a different potential

Reference electrode. If it's internally grounded, again due to distance between amplifier and load the 2 could have different ground voltage. So solution: take another wire and connect the ground of the ampop to the ground of the load.



in this way a unique ground for amplifier and load is granted

Use of the “reference” electrode to provide an offset on the load



Use of the common-mode voltage measured by the amplifier to drive guards

Output of the first stage is common mode + differential signal. So we need two equal resistance and it becomse just sensitive to CM. Il middle point rimane a zero (*altrimenti sarebbe virtual gnd)

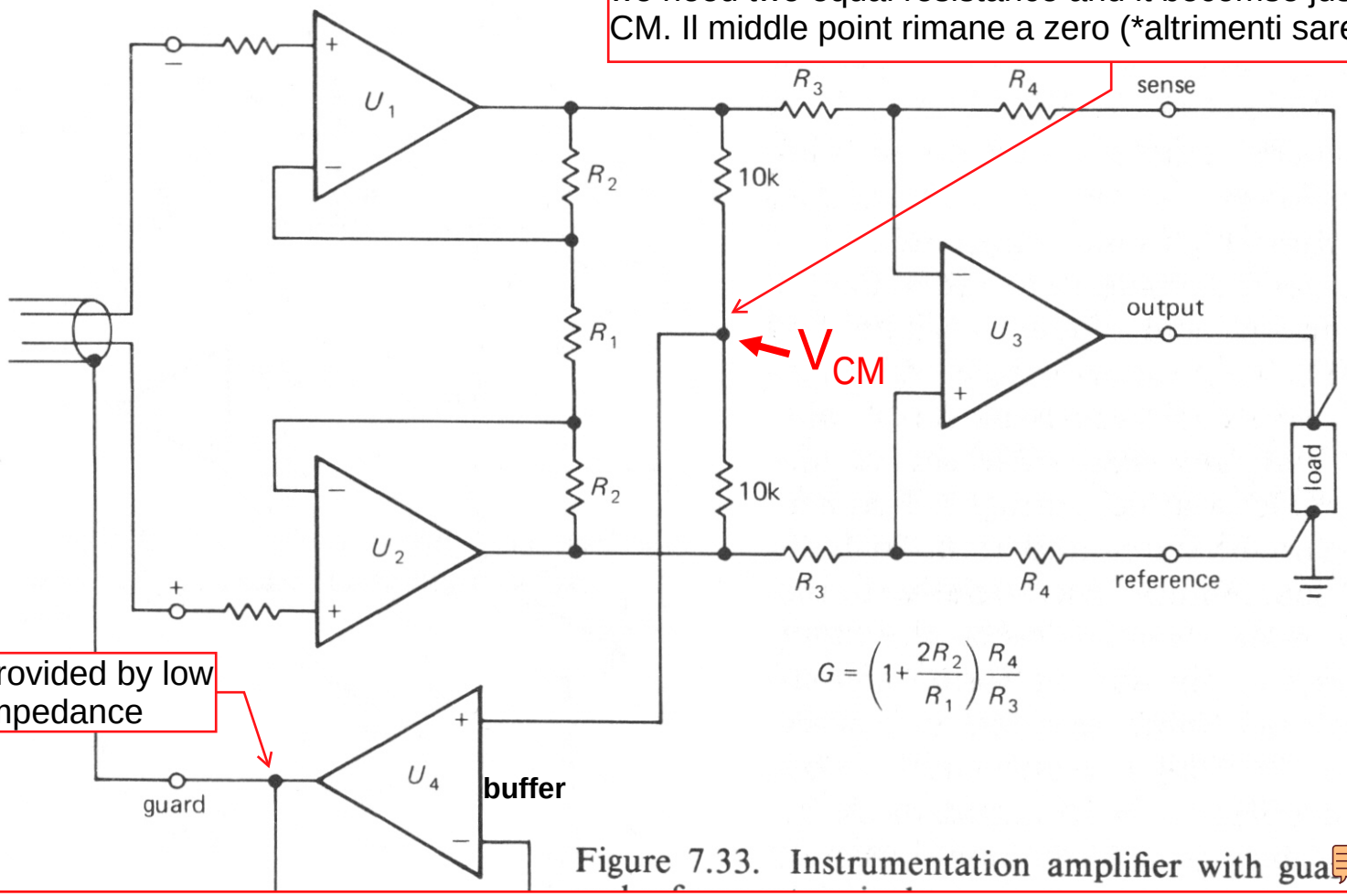
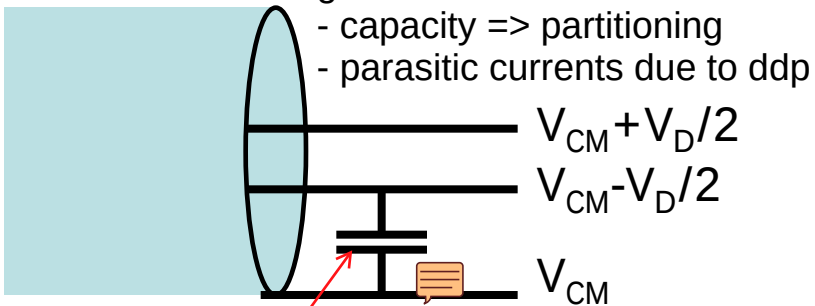


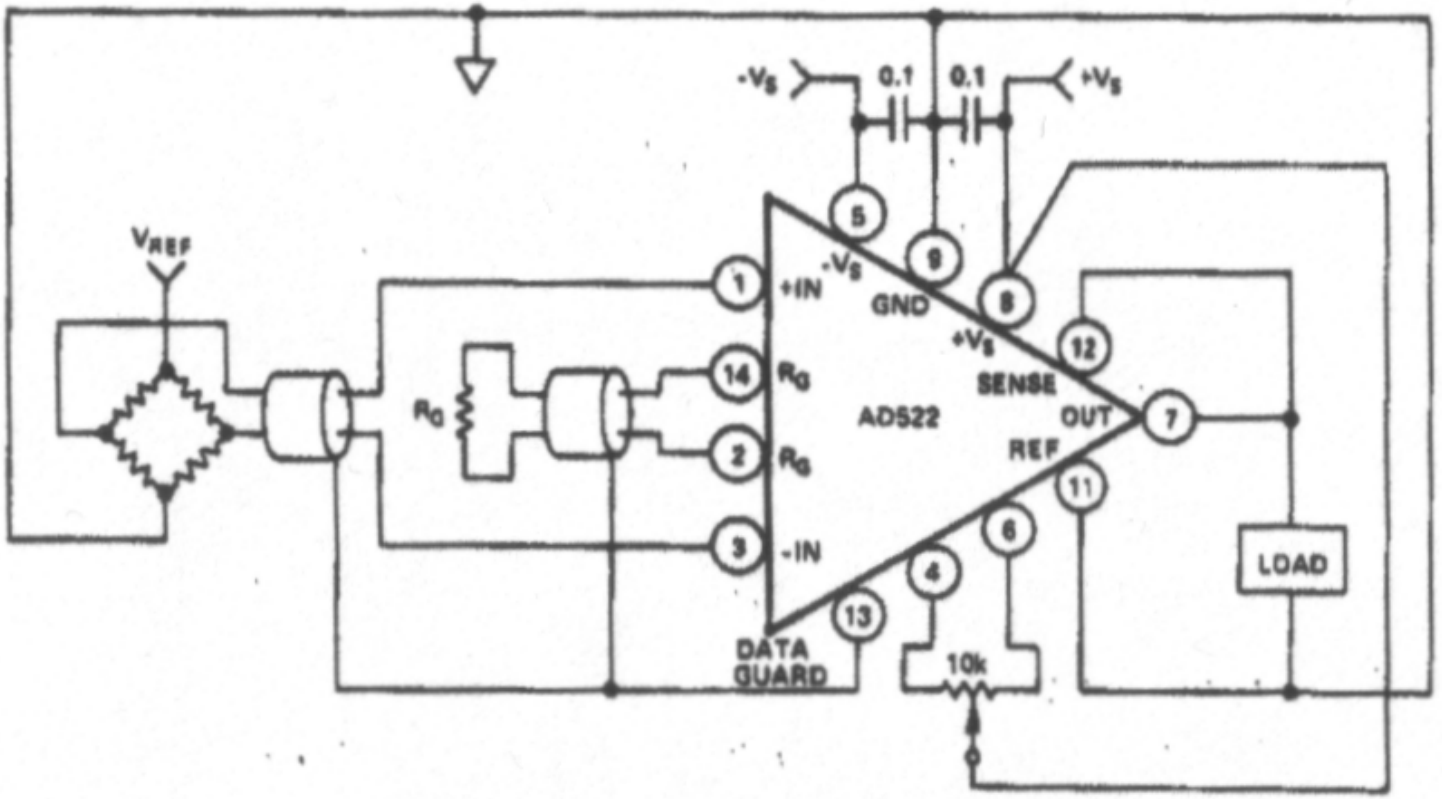
Figure 7.33. Instrumentation amplifier with gua… sense,

(2)How to measure the CM. I take the CM and buffer it (not to load the sensing point).Now with the CM I can 1) shield the wires coming from the electrodes. Problem of grounding shielding: the internal wire has the CM+Vdiff. There's a ddp between shield and internal wire (eg 1.5V).Because of the material separating the two is a conductor we have conducibility and **parasitic currents**; also: this shielding is the "cilindric capacitor!"[fisica].So we have a **cap**



at 60hz crea partizione

biasing the guards to V_{CM}
reduces the effects of capacitances
(and therefore of their mismatch) at
higher frequency for the CM
and of parasitic currents between
internal electrodes and shield



(1)Electrodes + couple of meters between them and INA. We must shield the wires. Otherwise there's electrical pickup of wires from EM waves. The wires becomes antennas lol (wires connected to high impedances). Usually external shielded put to ground => faraday caging. The charges induced by EMwaves is collected by the ground and not affecting the internal wire.

Another use of CM => reduce its effect

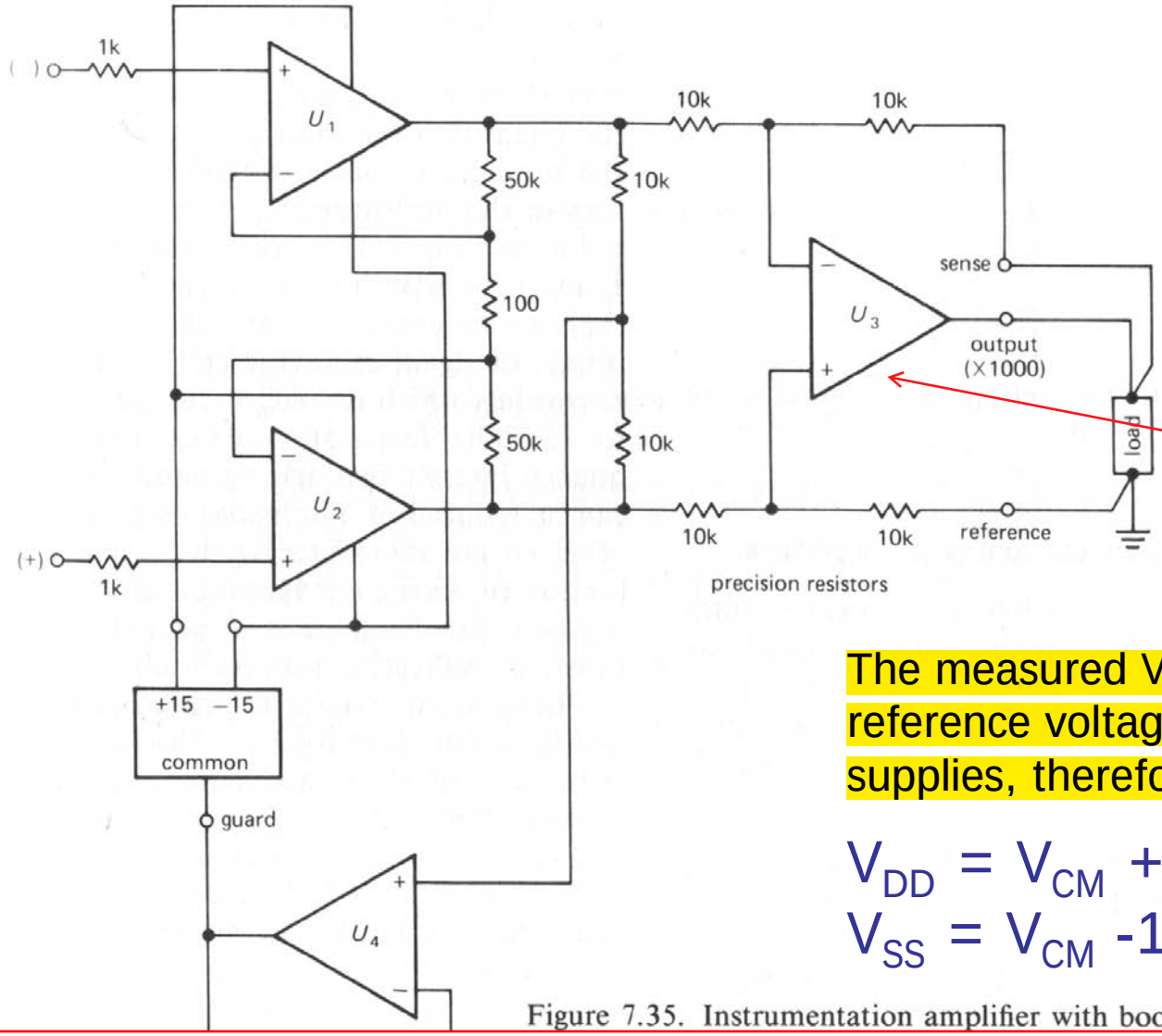


Figure 7.35. Instrumentation amplifier with bootstrapped

Bootstrap of power supplies (to reduce the effect of V_{CM})

not necessary for this, there'll be a big ddp at the input tho'!

The measured V_{CM} is provided to the reference voltage of the power supplies, therefore:

$$V_{DD} = V_{CM} + 15V$$
$$V_{SS} = V_{CM} - 15V$$

We make the INA "not aware" of the CM. We have the two pin di power supply, che genericamente hanno ddp relativa tra di loro e non assoluta. To respect a ref pin (!= ground pin). so eg +-15V is to respect the ref. Usually short circuit between ref and gnd. But we can also not do it. If we bias the ampop with +-15V to respect the gnd, the CM is referred to respect this ddp. eg 0V (from 10V - 10V) is [audio] So idea: take again CM, and we use this as reference. So the two voltages will be referred to the CM. The two will be. +-15V on top of CM (eg 15->25V, the other -5v) I CENTER THE DDP AROUND THE CM. The ampop is not experiencing the CM. We reduce its effect