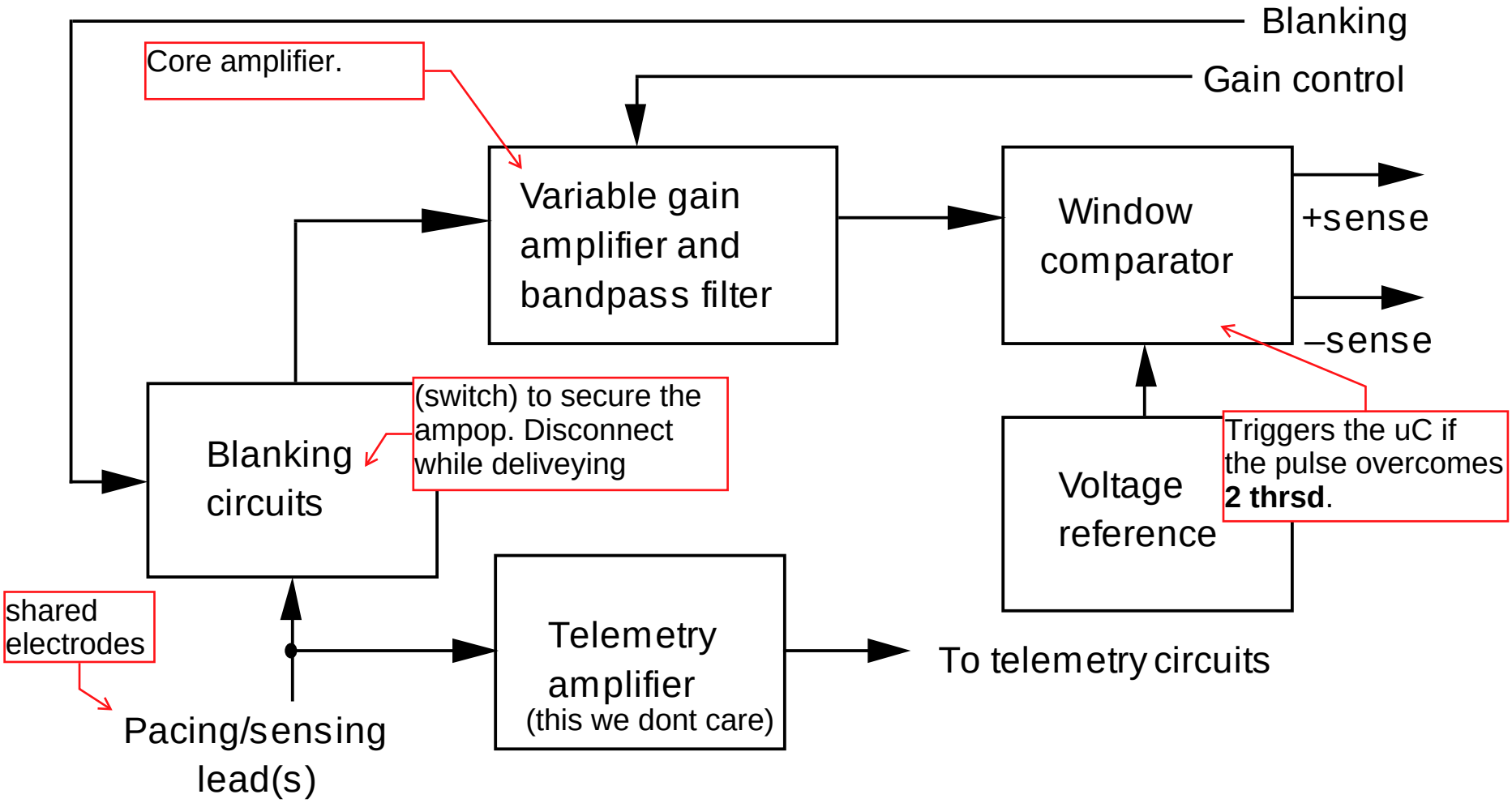
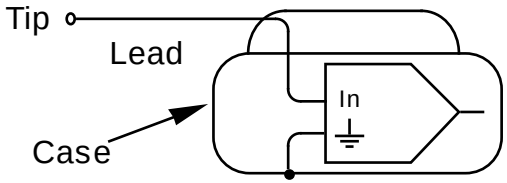
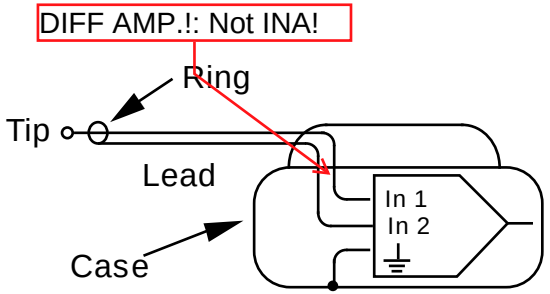
Basic components of the analog section of the Pacemaker



We do also ECG with the pacemaker (best we can have) indeed we need to sense the starting of a **SPONTANEOUS PULSE**. Cardiac pulses are actually **BIPOLAR.** So we can put 2 threshold, because we may have a very NOISY situation, to be more resistent.



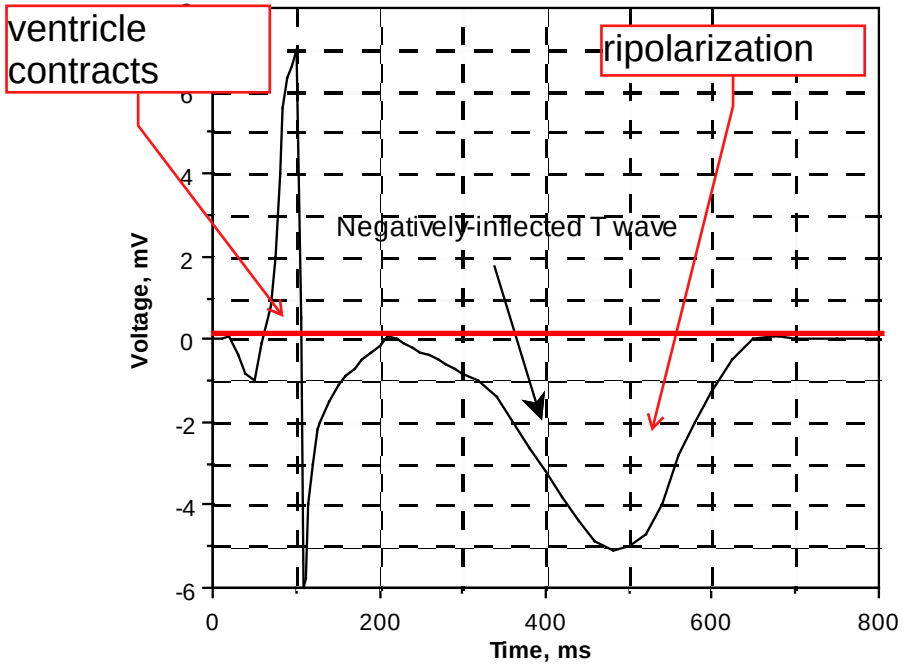
Unipolar



Bipolar

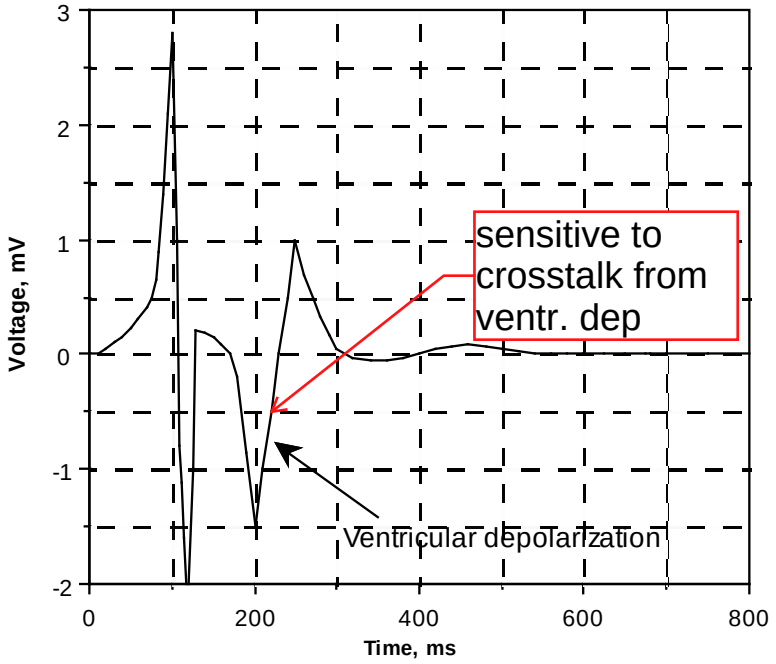
*dobbiamo stimolare il ventricolo. Gli elettrodi sono sul ventricolo. Facciamo anche sense: se si misura una contrazione ventricolare allora il timing viene resettato. oppure in generale vogliamo valutare l'ECG

waveform detected by pacemaker inside the ventricule



ECG intracardiac ventricular

case of atrial

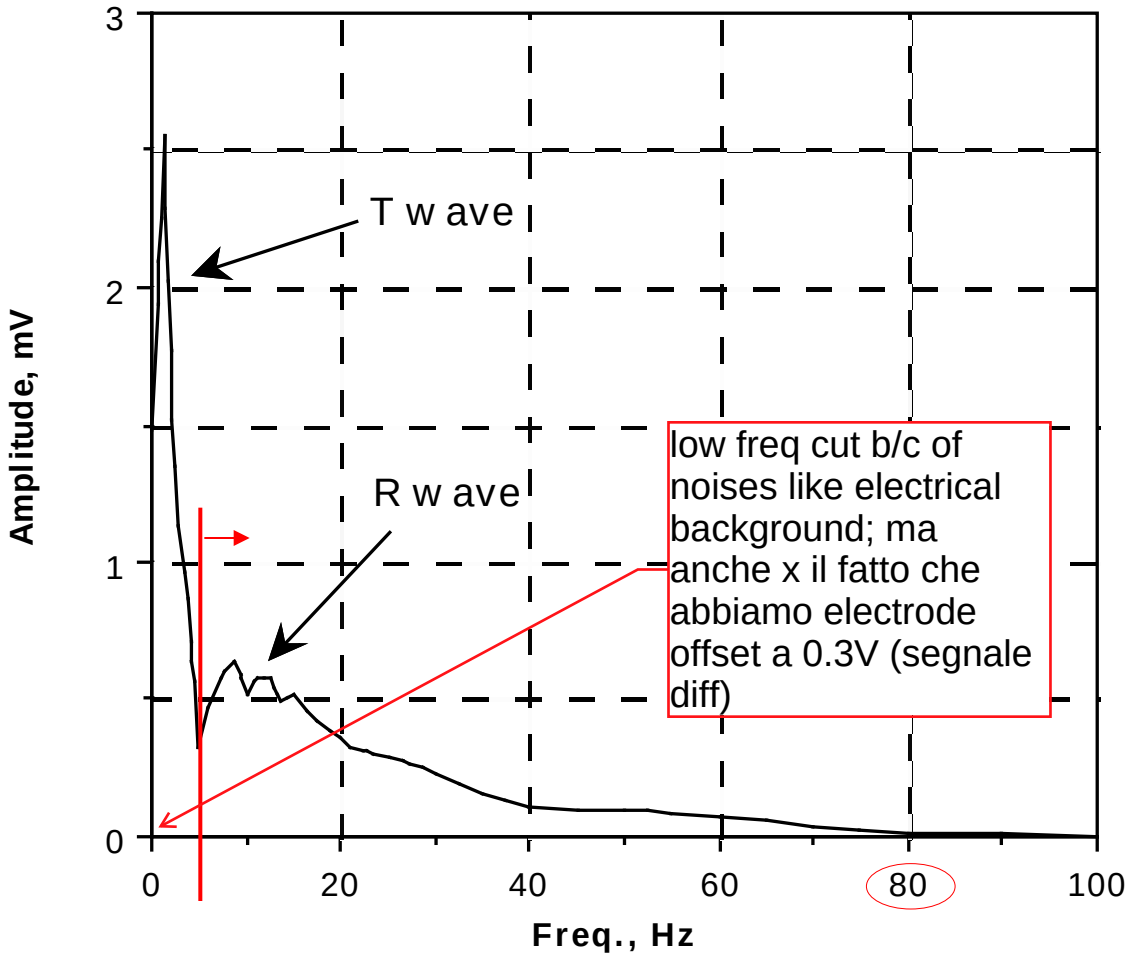


ECG intracardiac atrial

Unipolar sensing vs Bipolar sensing (just like in stimulating.. we 1 or the other?). Unipolar=> rx gnd case of pacemaker. Bipolar => voltage ddp between tip and ring. In this case we need a differential amplifier (**not INA b/c draws too much current**).

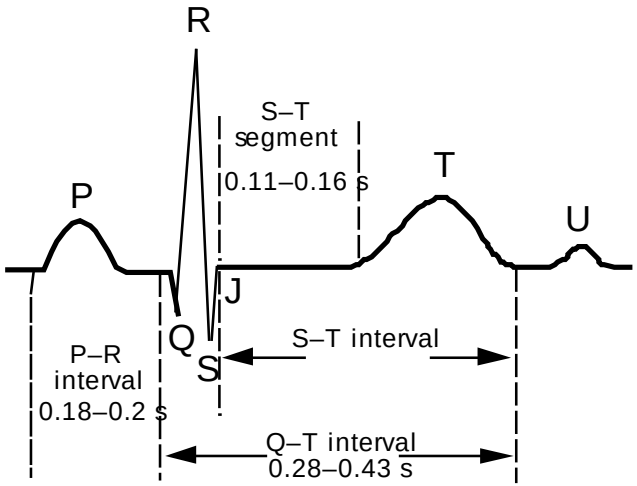
ECG intracardiac ventricular: frequency spectrum

*infatti la banda è come quella dell'ECG normale



not the transform of this!! just as a rimender

for reference:
external ECG signal



Slow and fast components. R is the steepest, indeed we have largest freq components.. up to 80Hz at MAX. We need to design amp up to 100hz. Problem: **low freq, we have many noises: eg. electrical background. So we need BP from very low to 100 Hz.**

(this is actually old)

ventricular sense amplifier

BP amplifier

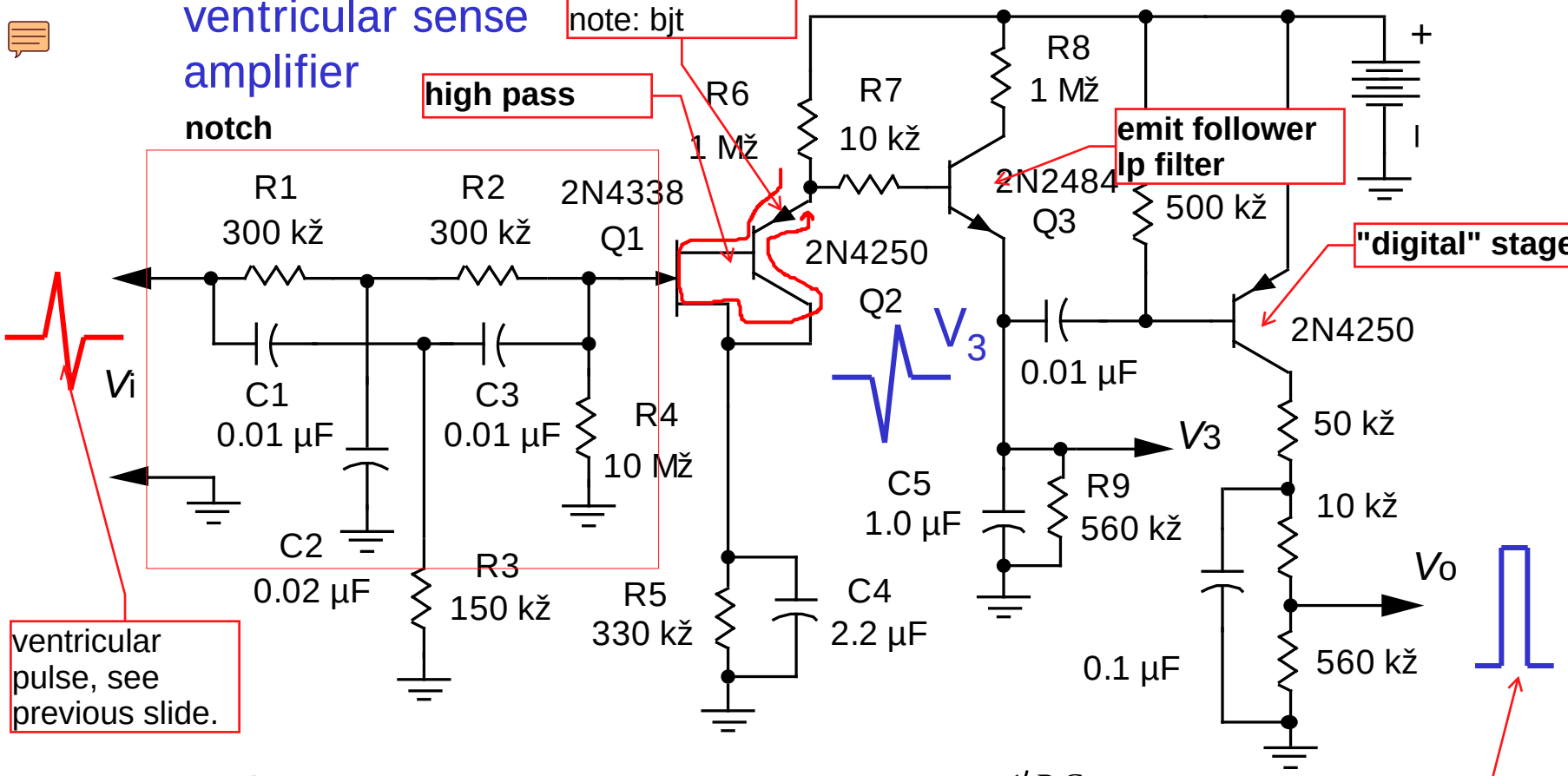
to boost "Rd"
note: bjt

high pass

notch

emit follower lp filter

"digital" stage



ventricular pulse, see previous slide.

Notch

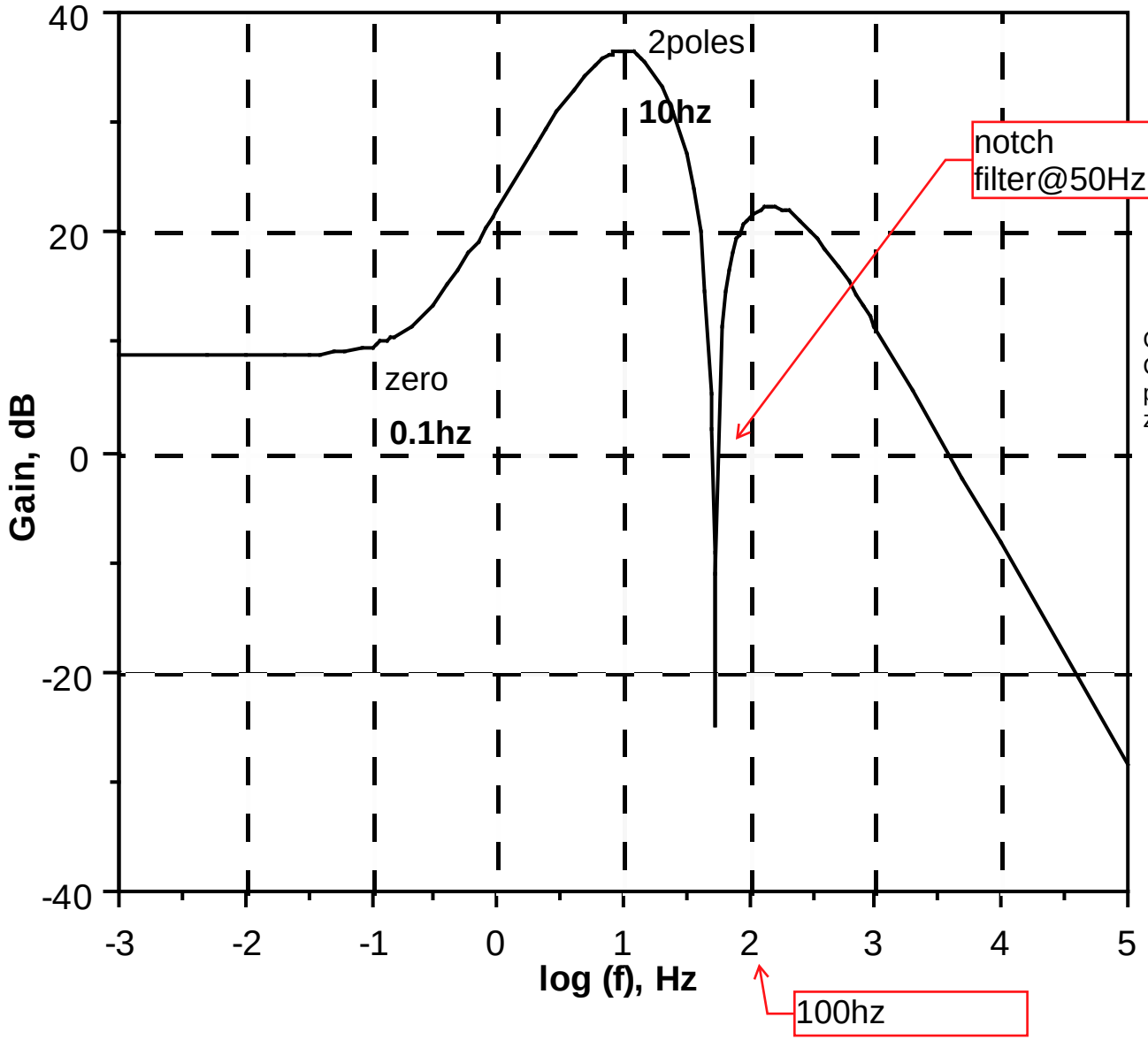
$$\frac{V_3}{V_i} = T(s) \times \frac{-g_m(1+h_{fe2})(1+h_{fe3})R_6(s-z_1)}{(R_6+R_7+h_{ie2})C_5(s-p_1)(s-p_2)}$$

$$z_1 = -1/R_5C_4$$

$$p_1 = -\left(\frac{1+g_mR_5(1+h_{fe2})}{R_5C_4}\right) \quad \text{1z, 2p}$$

$$p_2 = -\left(\frac{R_6+R_7+h_{ie2}+R_9(1+h_{fe3})}{R_9(R_6+R_7+h_{ie2})C_5}\right)$$

prevents the pacemaker of supplying the stimulus

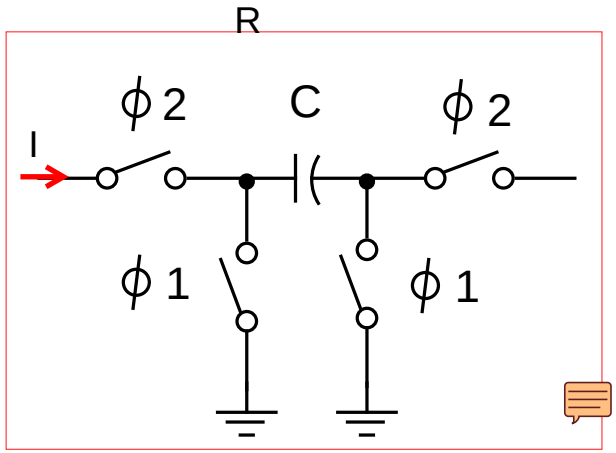


OCCHIOOOOOO NEL QUADERNO DICE:
polo in 10Hz e 100hz
zero in 0.1Hz

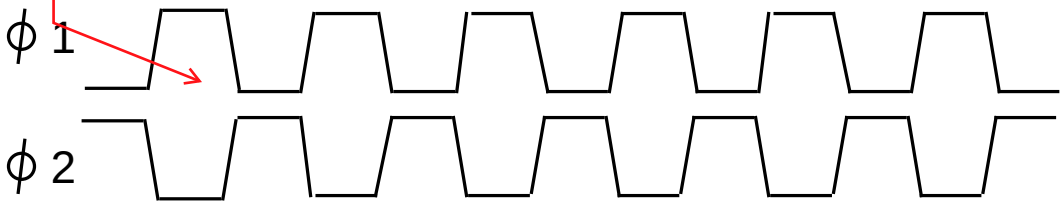
create very low freq poles. Called SWITCHED CAP AMPLIFIERS: emulate **very large R** without using R

problem: implement low freq poles in CMOS. Indeed that's the problem in pacemaker: design filters with low freq poles and zeroes. we need big time constant. [C molto basse nei CMOS]

Switched capacitors amplifiers



opposite. Never closed together. **Better all open for short time**



VALIDITY OF THIS: the average can be considered "constant" at least in the time change of the ddp. If ddp changes every clock it doesnt work

hypotheses:

1) clocks never overlapped in the high value
(switches never closed contemporary)

2) Vi and Vo change slowly with respect to the clock

R high=>smaller the cap <3, and smaller the clock

$$R_{\text{eff}} = \frac{(V_i - V_o)}{I} = \frac{(V_i - V_o)}{fC(V_i - V_o)} = \frac{1}{fC}$$

avg curr.

ex. C=2pF, f=10KHz
⇒ Reff=50MΩ

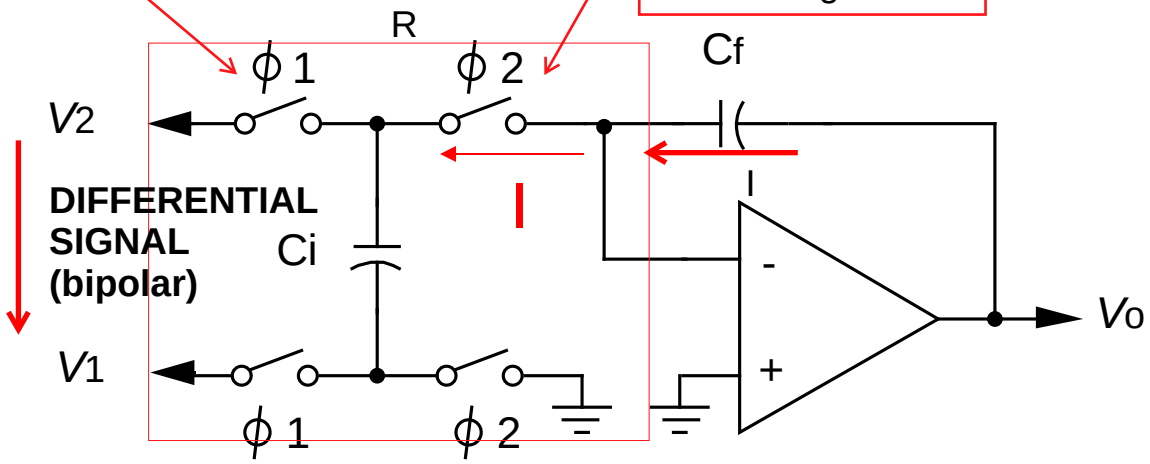
We can do nothing for the cap. We recover the penalty emulating a super-resistor. "Virtual ohm law" by using small set of capacitors and switches. We apply ddp, I want to know the current flowing. Req=ddp/I. Closing phi2 we charge C with Q=ddp*C. Then we open phi2 and close phi1. We discharge. Then the opposite and we charge, and so on. Doing so we are continously drawing a current I which puts charge over the cap. We can consider a kind of average draw of current. In a period of time t: Iavg = Q/(T) (clock period T). In reality, half of period is supplying, next half discharged. => ddp*C/T => ddp*C*f

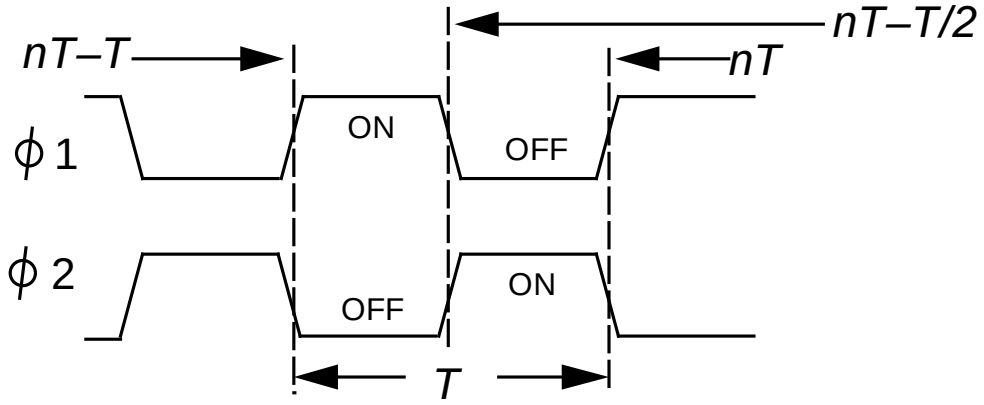
How to use this to create a filter?

Ideal integrator

it's a bit different, we charge with phi1

when we close phi2 we discharge





$\Delta Vi = V1-V2$

I=charge*freq

$I = \Delta Vi \times f \times Ci$

$Reff = \Delta Vi/I = 1/f \times Ci$

standard analysis using I

$Vo = I \times 1/j\omega C_f$

$= \Delta Vi \times f \times Ci/j\omega C_f$

FDT:

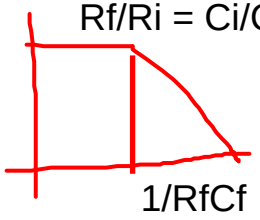
$$\frac{V_o}{\Delta V_i} = \frac{C_i}{C_f}\frac{1}{j\omega T}$$

Starting from the classical integrator.. R and the C in the feedback of an opamp. We put swtiched cap instead of R. Bonus solution: the classical way was UNIPOLAR. This solution IT'S **BIPOLAR**!!!

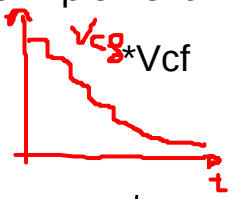
*il cap è scaricato completamente(?) direi proprio di sì

Real integrator (low-pass filter)

Rf/Ri = Ci/Cx [yes ratio!]



"**lossy resistor**", we implement a real pole



We apply also a Rf. Gain= Rf/R

(if they are in the same region of the wafer) So this gain is quite robust from uncertainty of production. Same thing for the cutoff frequency!

ϕ1: Cx is charged to Vo(t)
ϕ2: Cx is discharged on the virtual ground and the lost charge goes to discharge Cf

$$Qx = Vo(t) \times Cx$$
$$Ix = f \times Qx = f \times Vo(t) \times Cx$$
$$Ix = Vo(t)/Rf$$
$$\Rightarrow Rf = 1/(f \times Cx)$$

DC component of the transfer function == to constant gain

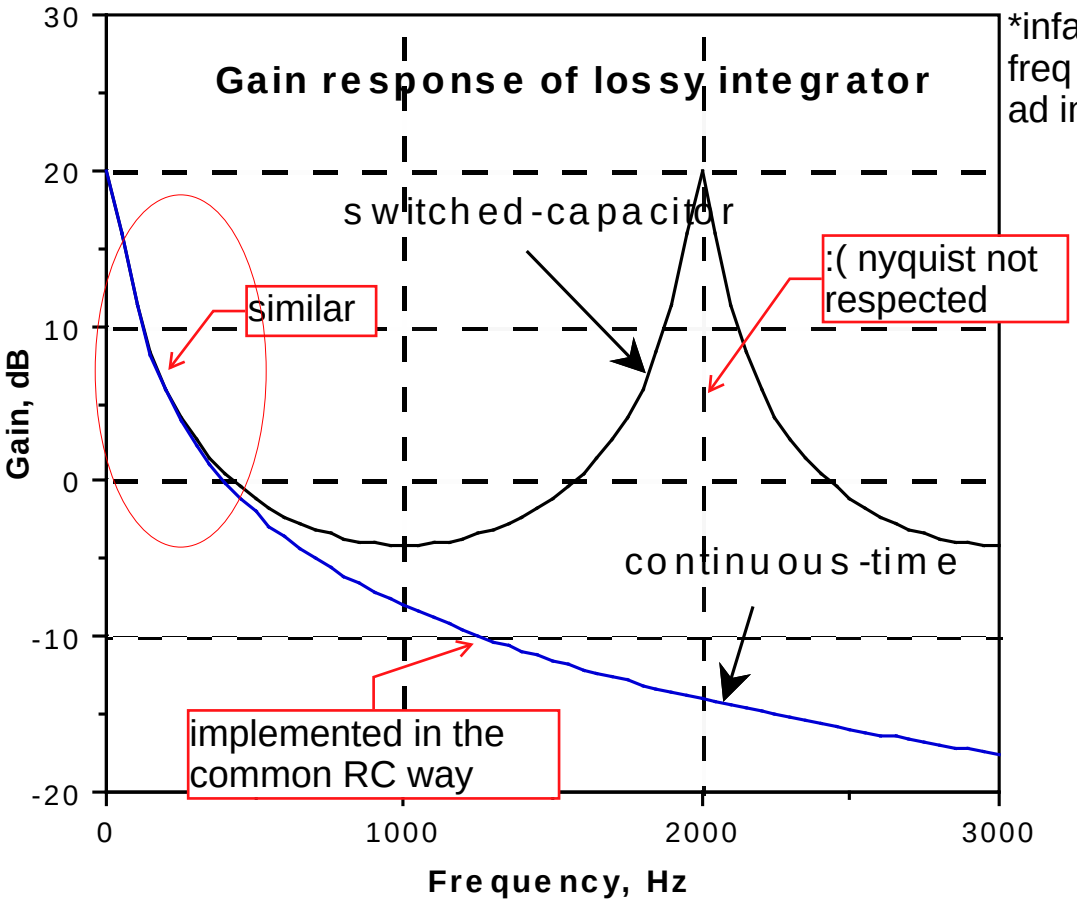
$$\frac{Vo}{Vi} = \frac{\frac{Rf}{1+j\omega CfRf}}{Ri} = \frac{\frac{\frac{T}{Cx}}{1+j\omega Cf\ T/Cx}}{T/Ci} = \frac{Ci}{Cx}\ \frac{1}{1+j\omega Cf\ T/Cx}$$

pole

$$G_{DC} = Ci/Cx$$
$$\omega_T = Cx/(Cf\ T)$$

Thanks to phi1 and phi2 the capacitor (Cx) gets the voltage from the output when you close phi1, and it's charged (Q=Vo*Cx). You then open phi1, close phi2, the charge accumulated on Cx is then FLOWING TO CF and contributes to discharge it. Can these charges goes elsewhere? both phi2 are closed together. But NO! because **there's ground on both pins of Ci, so it can't accumulate charges**. For exclusion the charges will flow into Cf. Is it a DISCHARGING CHARGE?

Freq. response of the filter (not bode b/c freq not in db)



*infatti qst serviva p' era difficile fare filtro hp ok in freq basse! no prob. aggiungere lp filter davanti ad ingressi

$C_x = 1pF$
$C_f = 8pf$
$C_i = 10pF$
$f = 2kHz$

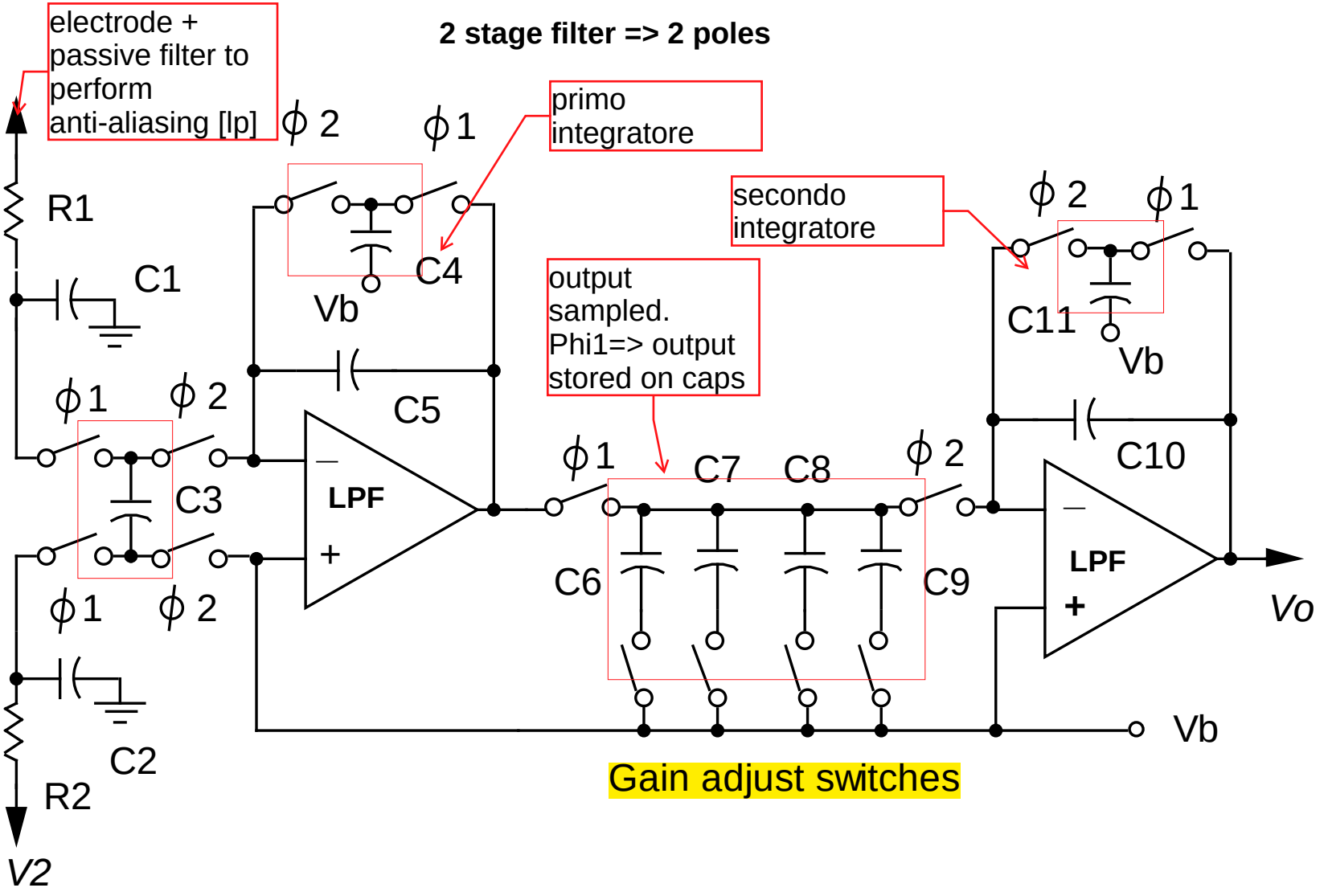
$G_{DC} = 10$
$f_T = 40Hz$

Freq. resp. of SC filter ~ freq. resp. of analog filter up to 300Hz

Notes:

1) characteristics of the SC filter depend on C ratio and not of C abs. values
2) low f_T obtained with small capacitances (integrated!); f_T adjustable with f
3) digital system: attention to aliasing (filter input), clock feedthrough, ..

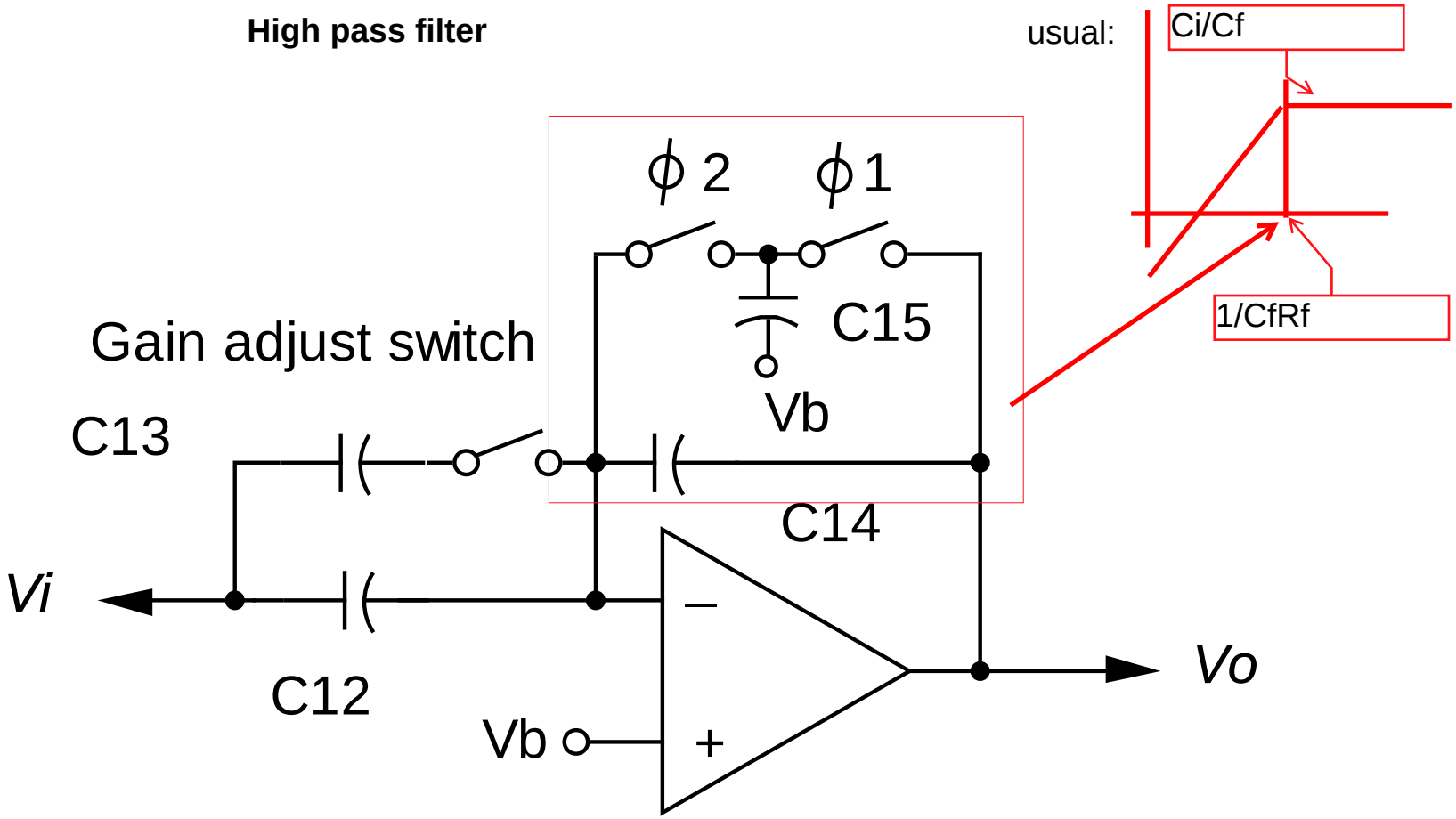
Switched-cap filter: strange behaviour after a while in freq. region where the nyquist condition is no more satisfied. With a clock of 2khz, it works only up to 1khz.



(a) Differential–input amplifier and low–pass filter

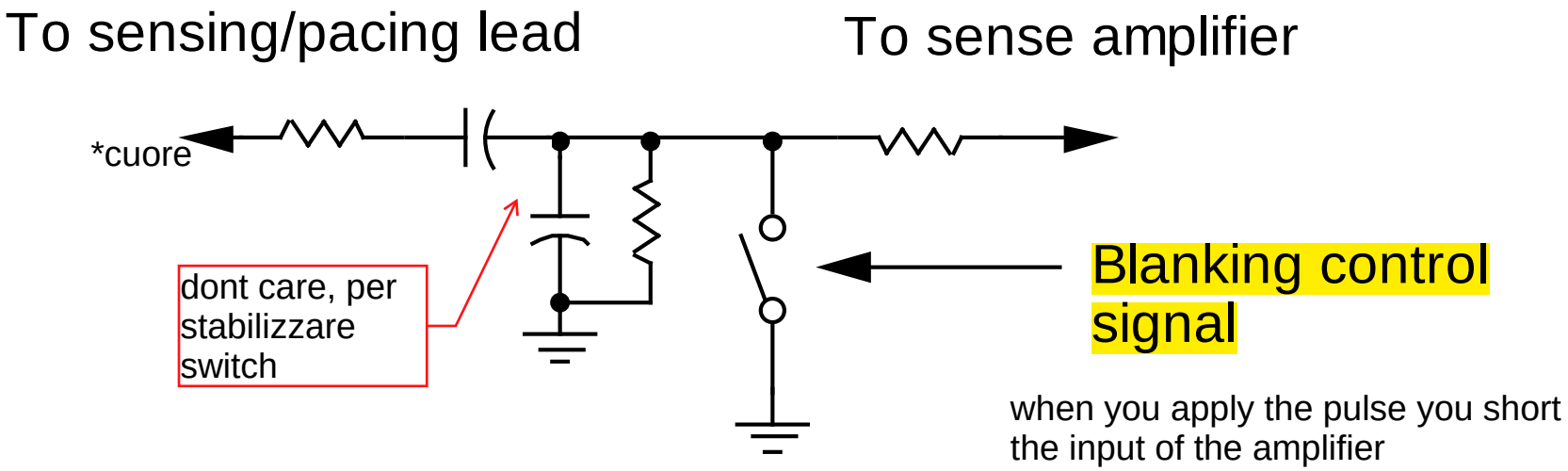
eg poles at same freq => -40db/dec. Between the two output there's... (phi1 charge, phi2 discharge). Battery of several caps, they are NOT SWITCHED DINAMICALLY, THEY ARE STATIC SWITCHES. you close 1 to 4 caps, these are gain factors. More cap you put into the gain, more charge you store overall for a voltage. Thus more charge will be injected into the 2nd cap.

High pass filter

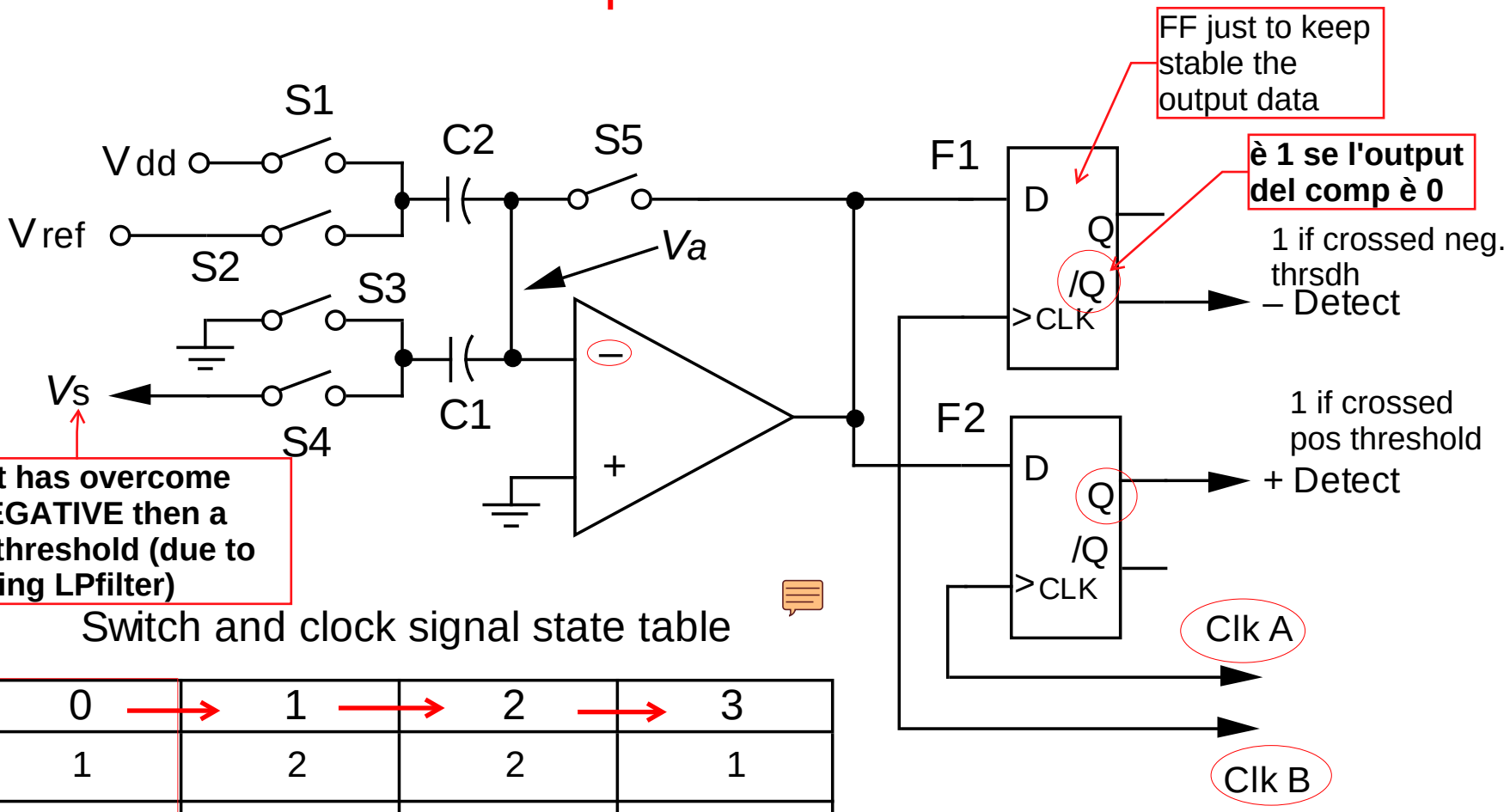


(b) Adjustable–gain high–pass filter

At the input there's a cap instead of a R. Input cap can be put in parallel to another to change the gain (without changing the pole.


To sensing/pacing lead
To sense amplifier
*cuore
dont care, per stabilizzare switch
Blanking control signal
when you apply the pulse you short the input of the amplifier

Comparator **less power consuming!**



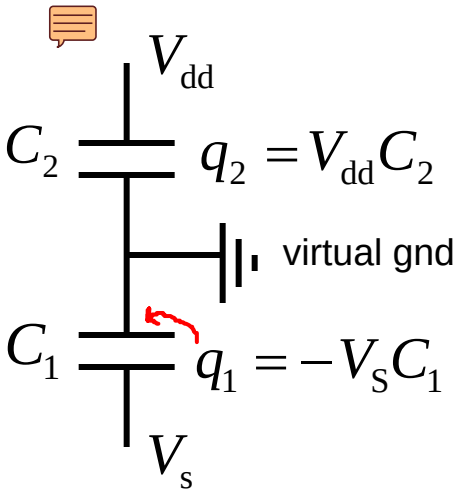
Switch and clock signal state table

0 →	1 →	2 →	3
1	2	2	1
4	3	4	3
5	Clk ~~A~~ B	5	Clk ~~B~~ A

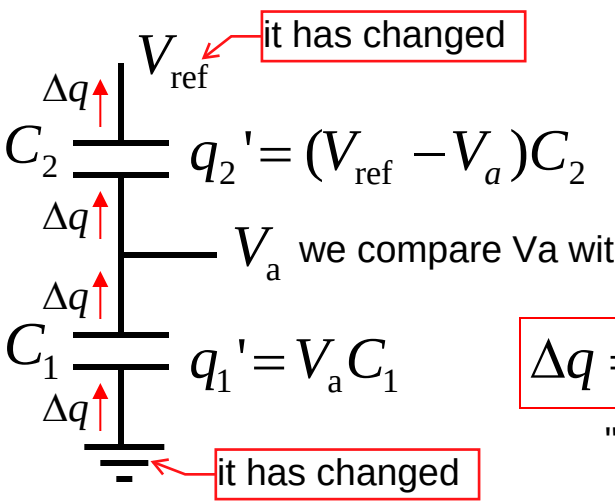
Check the pulse (stimulus). **Problem: power consumption for std comparators** (they have **dc currents**, not good in power consmpt). Topology based on capacitors => we dont have a dc current! (which would mean continous power consumption). If uC sees the two threshold passed, it understand a valid stimulus has occured. We'd like to be able to **adjust the thresholds, this can be done by acting on the reference voltages**.

semplified situation

phase 0



phase 1



$$\Delta q = (V_{ref} - V_a)C_2 - V_{dd}C_2$$

they should be the same

$$\Delta q = V_a C_1 + V_S C_1$$

"meno per meno"

I obtain an equation where the unknown is Va

after phase 0 and 1

$$V_a = C_2 \frac{(V_{ref} - V_{dd})}{(C_1 + C_2)} - C_1 \frac{V_s}{(C_1 + C_2)}$$

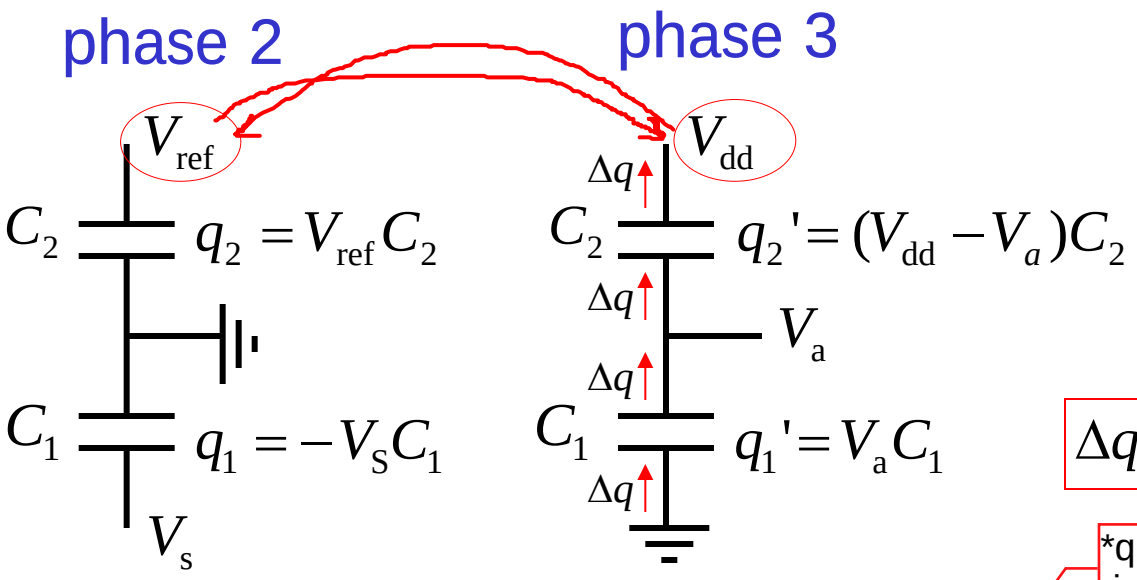
CERCO PRIMA VOUT NEGATIVO

$\overline{Q}$ FF1 high if:

$V_a > 0$ (V-)

$$V_s < -\frac{C_2(V_{dd} - V_{ref})}{C_1}$$

negative threshold



$$\Delta q = (V_{dd} - V_a) C_2 - V_{ref} C_2$$

$$\Delta q = V_a C_1 + V_S C_1$$

*queste due si invertono rispetto a prima

after phase 2 and 3

$$V_a = C_2 \frac{(V_{dd} - V_{ref})}{(C_1 + C_2)} - C_1 \frac{V_s}{(C_1 + C_2)}$$

Q FF2 high if: $V_a < 0$

$$V_s > \frac{C_2 (V_{dd} - V_{ref})}{C_1}$$

positive threshold

pin di va: passa da gnd a Va alternandosi a seconda della fase. quindi è ciclico (s5 chiuso,aperto,chiuso,aperto)
pin sotto c1: cicla Vs/gnd
pin sopra C2: il primo colpo alterna Vdd/Vref, il secondo Vref/Vdd (così da cambiare il segno di Va, ed evidentemente il threshold cercato