DIPARTIMENTO di ELETTRONICA, INFORMAZIONE e BIOINGEGNERIA

POLITECNICO DI MILANO

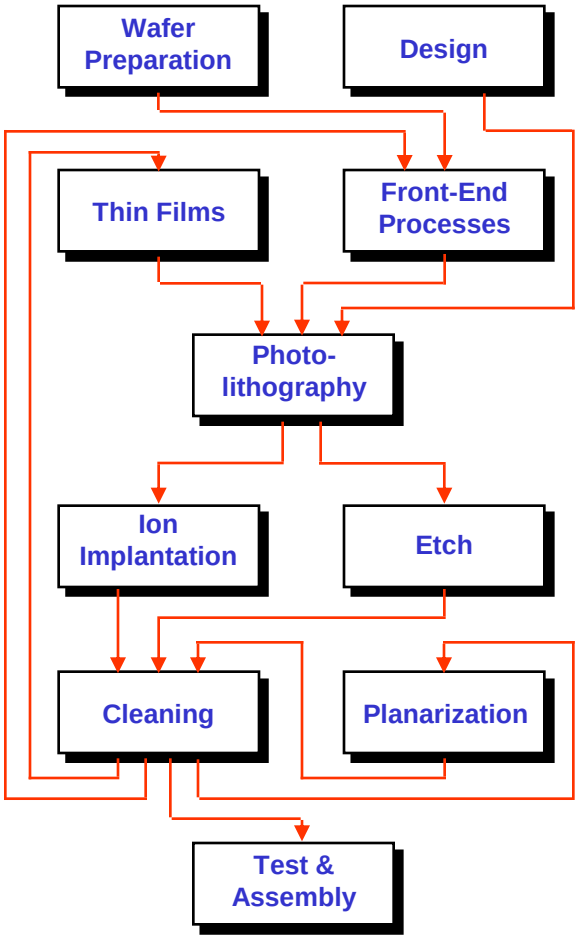




Lecture 4
Semiconductor Manufacturing Technologies

Semiconductor Manufacturing Processes

- Wafer Preparation
- Design
- Front-end Processes
- Photolithography
- Etching
- Cleaning
- Thin Films
- Ion Implantation
- Planarization
- Test and Assembly



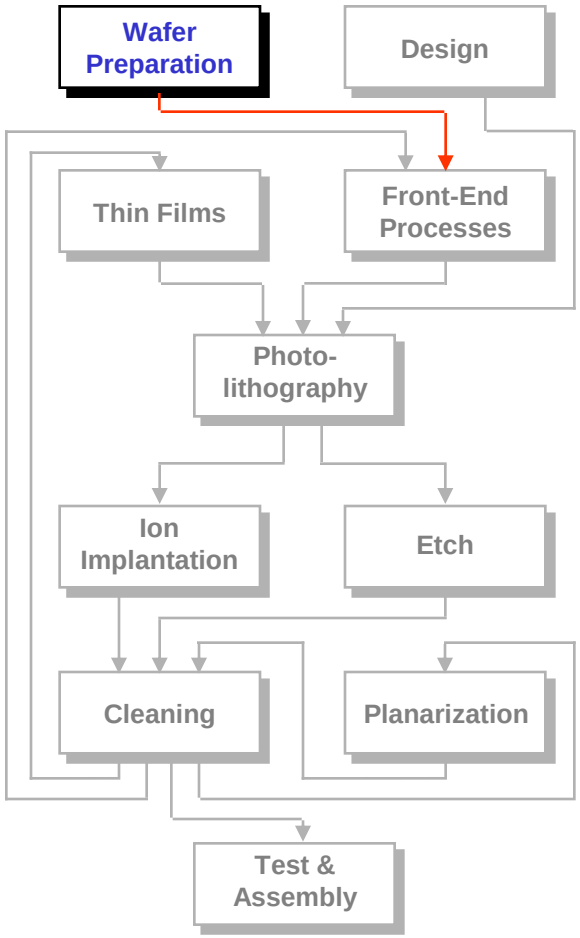
Wafer Preparation

Polysilicon Refining

Crystal Pulling

Wafer Slicing & Polishing

Epitaxial Silicon Deposition



Semiconductor Tecnologies: materials

- Single crystal silicon (SCS)
  anysotropic crystal
  semiconductor, optimal heat conductor
- Polysilicon
  isotropic material
  semiconductor
- Silicon dioxide (SiO_2)
  excellent thermal and electrical insulator
- Silicon nitride (Si_3N_4)
  excellent electrical insulator
- Aluminium (Al)
  Metal – excellent thermal and electrical insulator

Metallurgic grade silicon

Elemental silicon not alloyed with significant quantities of other elements, and usually >95%, is often referred as **silicon metal**. **Metallurgical grade silicon**, at least 98% pure, is commercially prepared by the reaction of high-purity silica with wood, charcoal, and coal in an electric arc furnace using carbon electrodes. At temperatures over 1900°C, the carbon in the aforementioned materials and the silicon undergo the chemical reaction

$$SiO_2 + 2\ C \rightarrow Si + 2\ CO$$

Liquid silicon collects in the bottom of the furnace, which is then drained and cooled.

Note: Using this method, silicon carbide (SiC) may also form from an excess of carbon in one or both of the following ways:
$SiO_2 + C \rightarrow SiO + CO$ or $SiO + 2\ C \rightarrow SiC + CO$.
However, provided the concentration of SiO_2 is kept high, the silicon carbide can be eliminated by the chemical reaction $2\ SiC + SiO_2 \rightarrow 3\ Si + 2\ CO$

Electronic grade silicon

The majority of silicon crystals grown for device production are produced by the **Czochralski process**, (CZ-Si) since it is the cheapest method available and it is capable of producing large size crystals. However, single crystals grown by the Czochralski process contain impurities because the crucible containing the melt often dissolves.

Today, silicon is purified by converting it to a silicon compound that can be more easily purified by distillation than in its original state, and then converting that silicon compound back into pure silicon.

Trichlorosilane ($SiHCl_3$) is the silicon compound most commonly used as the intermediate, although silicon tetrachloride and silane are also used. When these gases are blown over silicon at high temperature, they decompose to high-purity silicon.

Polysilicon Refining

Chemical Reactions

Silicon Refining: $SiO_2 + 2\,C \rightarrow Si + 2\,CO$

Silicon Purification: $Si + 3\,HCl \rightarrow HSiCl_3 + H_2$

Silicon Deposition: $HSiCl_3 + H_2 \rightarrow Si + 3\,HCl$

Reactants

H_2

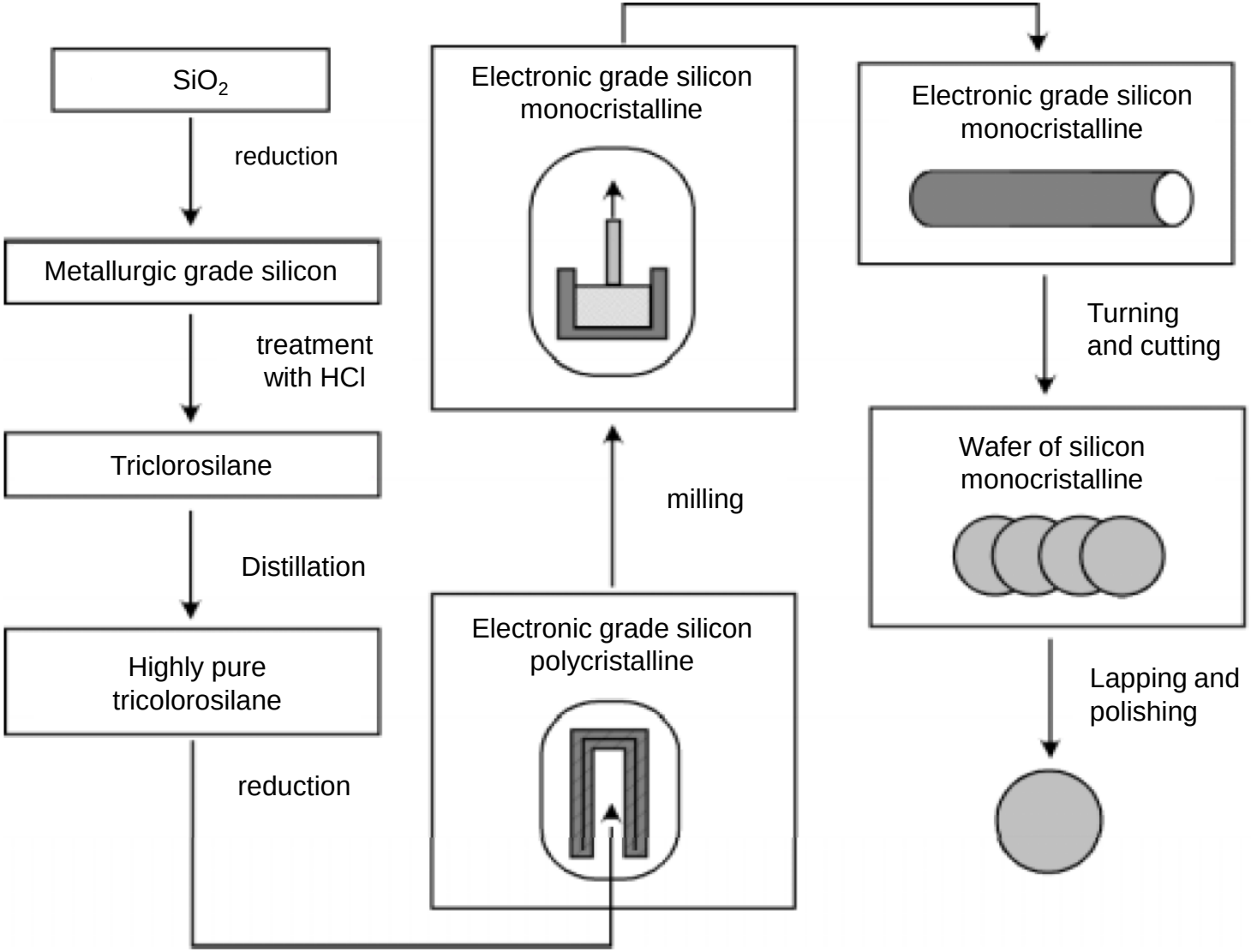
Silicon Intermediates

H_2SiCl_2

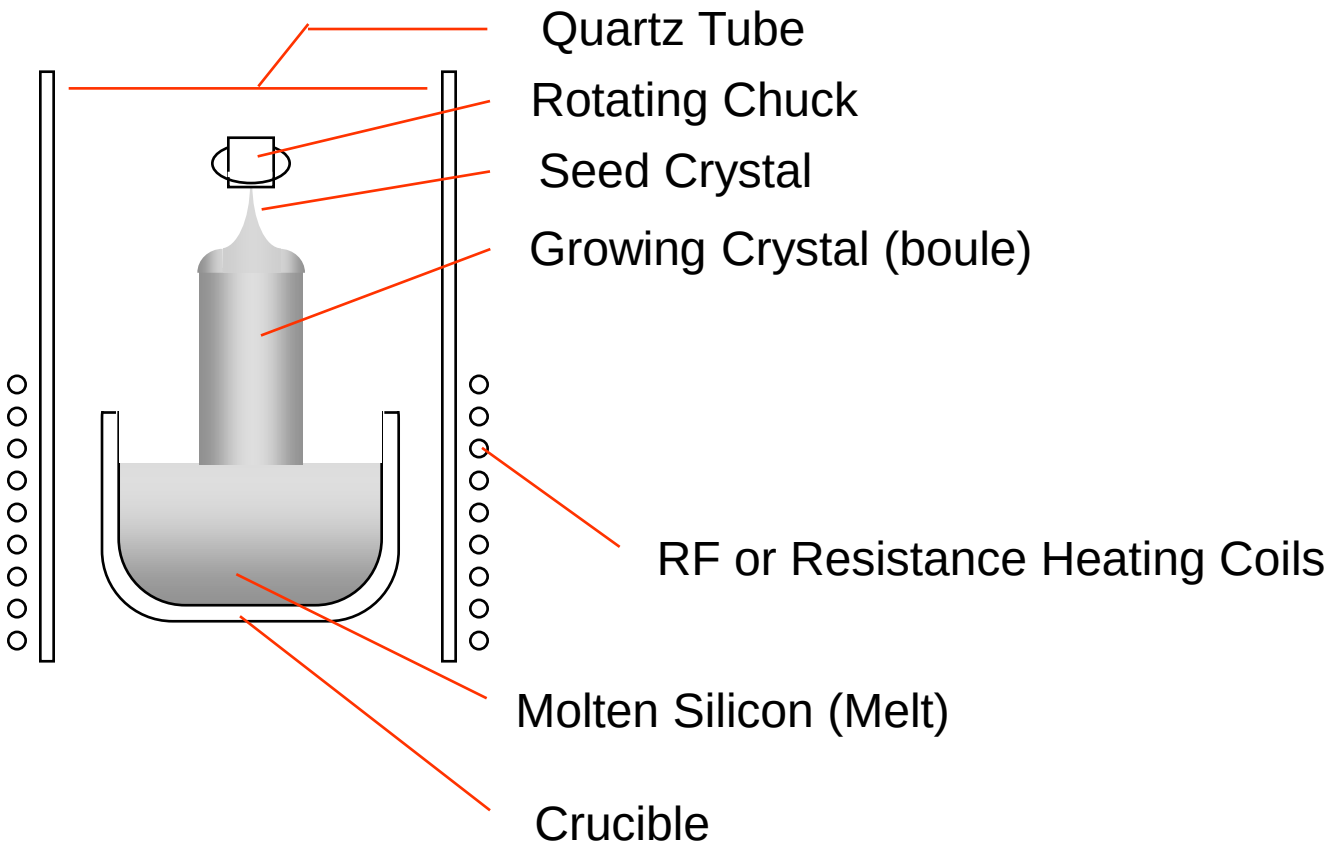
$HSiCl_3$

Polysilicon Ingots

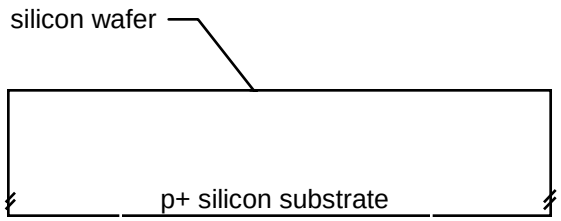
Preparation of silicon wafers

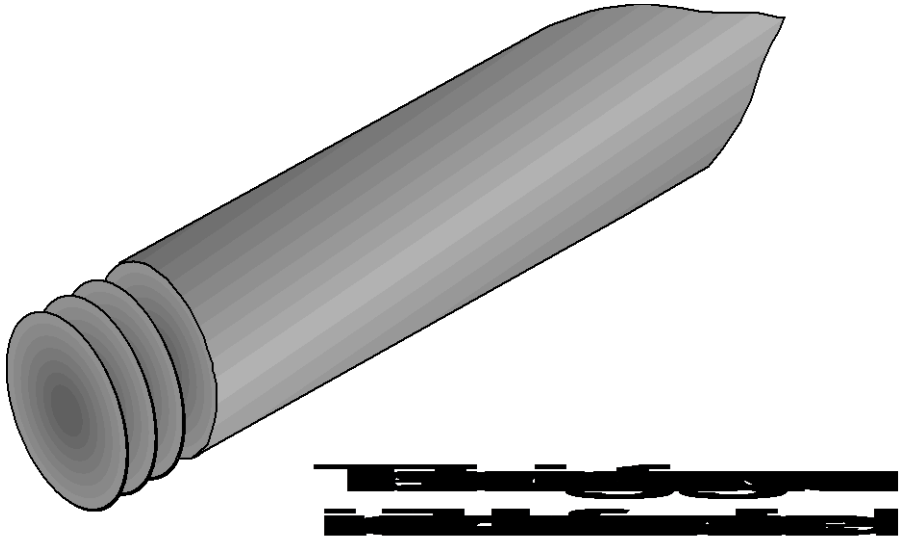


Czochralski process: crystal pulling



Wafer Slicing & Polishing





The silicon ingot is sliced into individual wafers, polished, and cleaned.

Miller indices

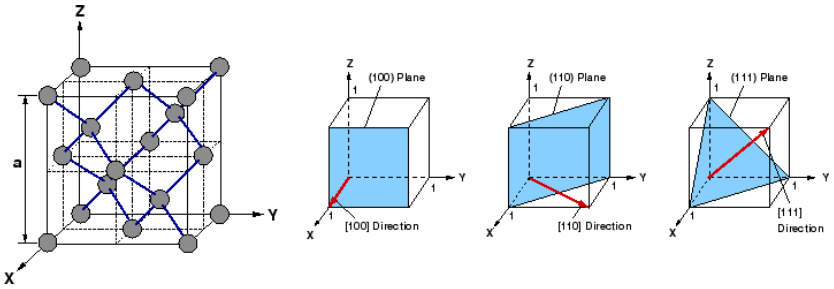
This notation indicates crystal directions:

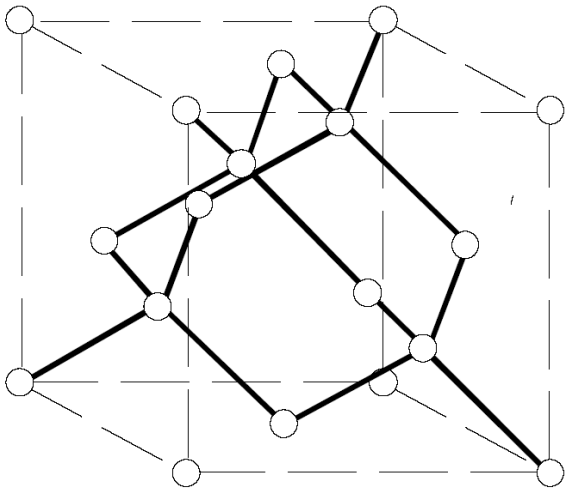
[111] indicates a set of planes parallel to the plane that crosses the three axes in point a (a = reticular step);

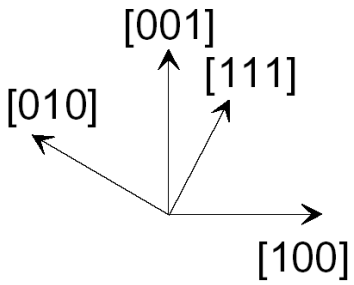
[100] set parallel to the plane which is perpendicular to x-axis;

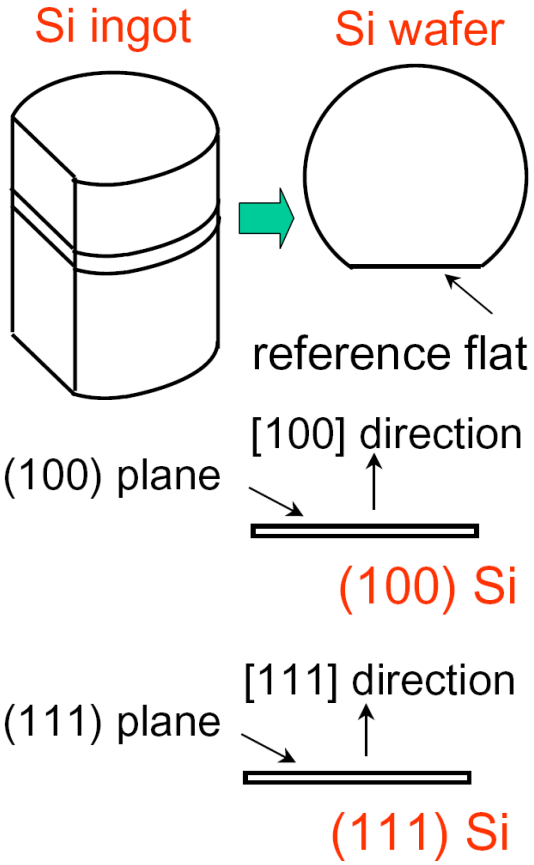
[010] .. to y-axis,

[001] … to z-axis

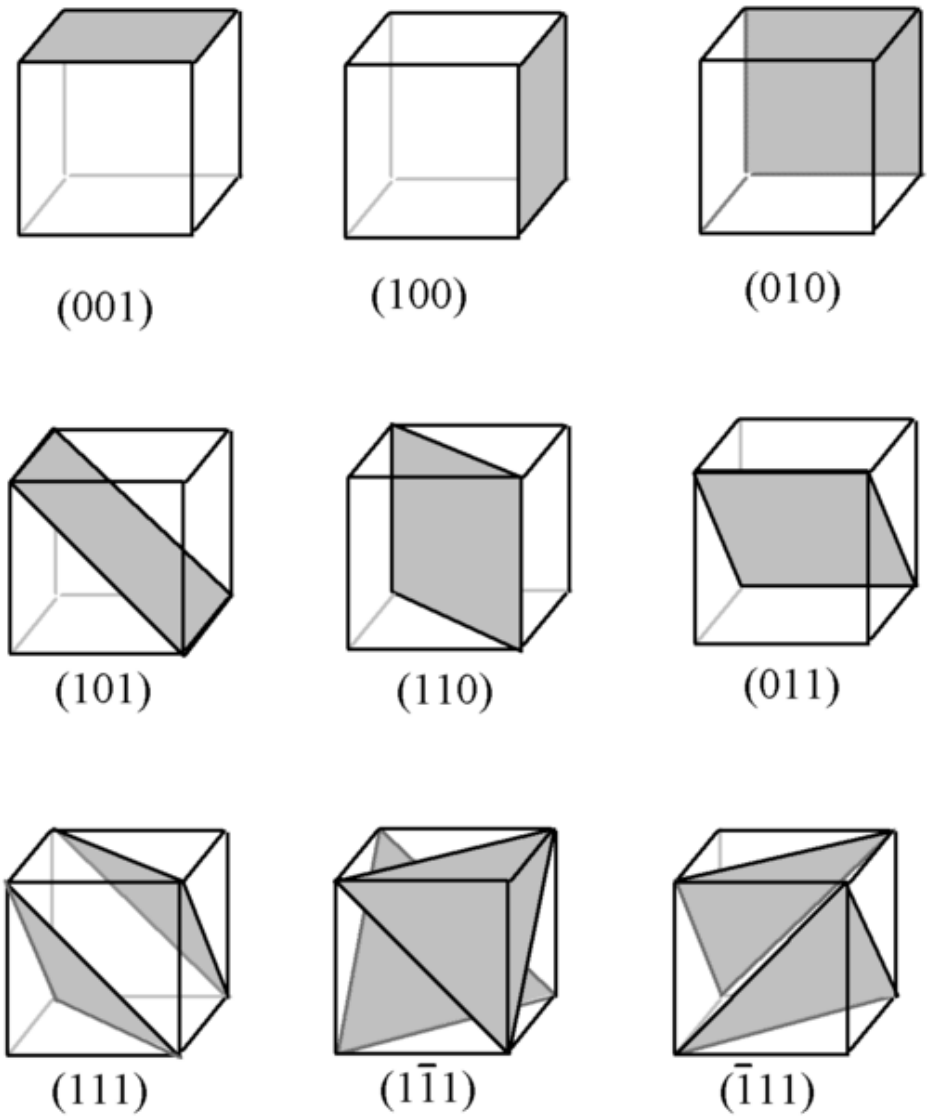






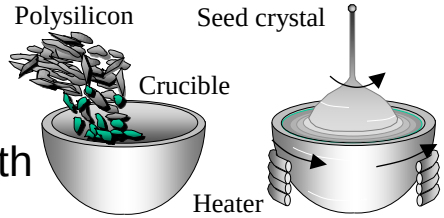


Miller indices

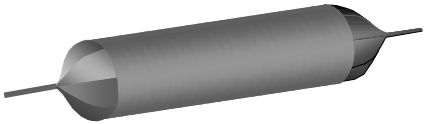


Preparation of silicon wafers

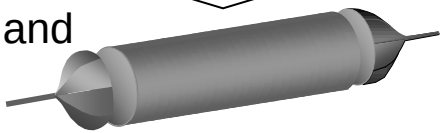
1. Crystal Growth



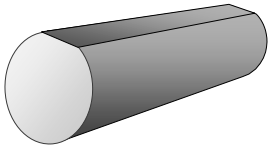
2. Single Crystal Ingot



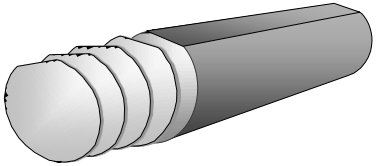
3. Crystal Trimming and Diameter Grind



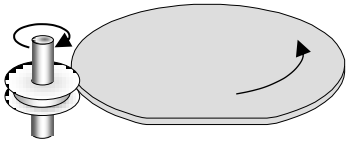
4. Flat Grinding



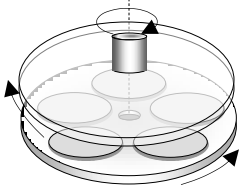
5. Wafer Slicing



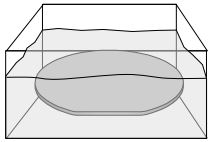
6. Edge Rounding



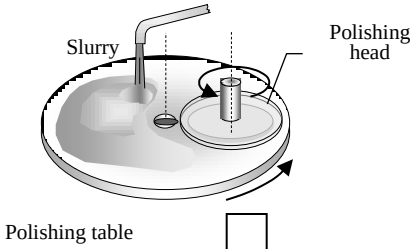
7. Lapping



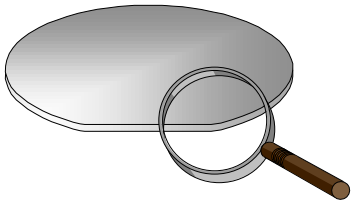
8. Wafer Etching



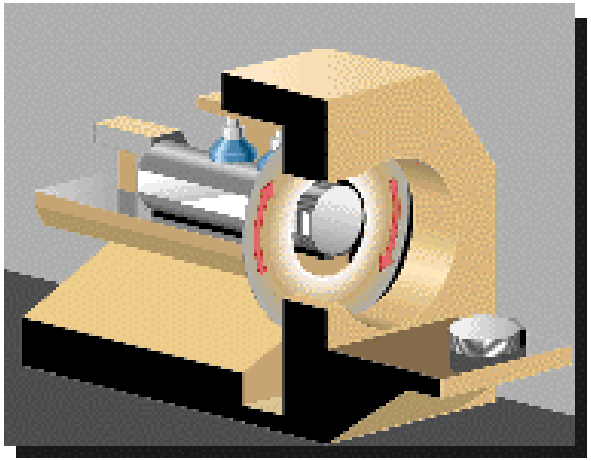
9. Polishing

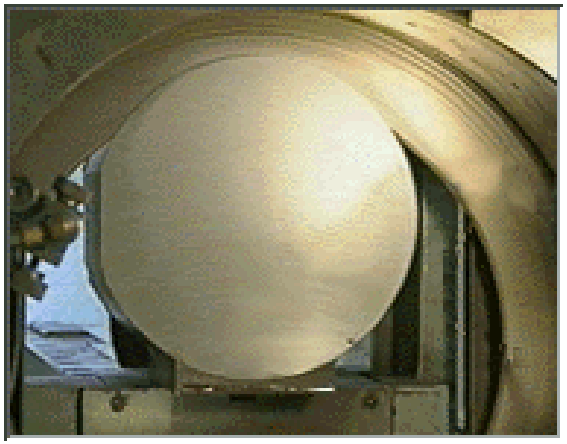


10. Wafer Inspection

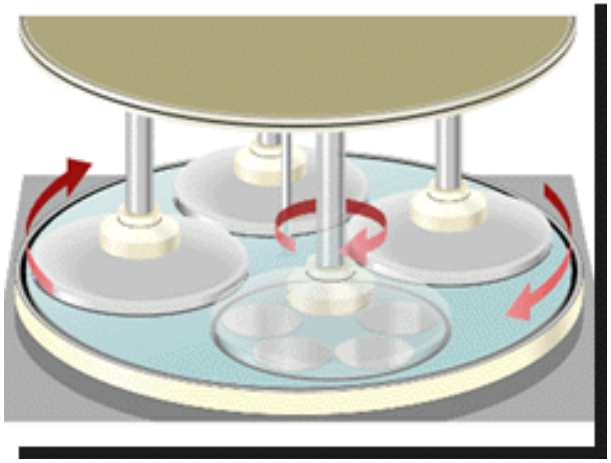


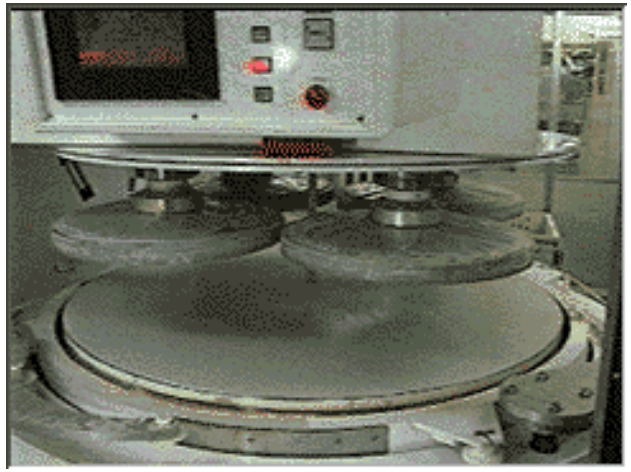
Cutting





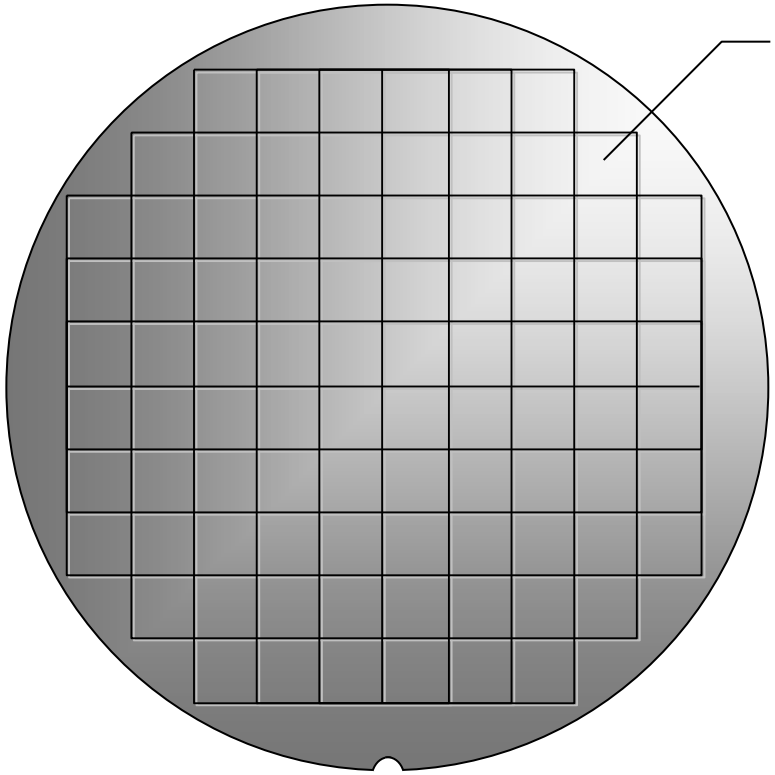
Lapping and polishing





Evolution of Wafer Size

Top View of Wafer with Chips



A single integrated circuit, also known as a die, chip, and microchip

Thin Films deposition

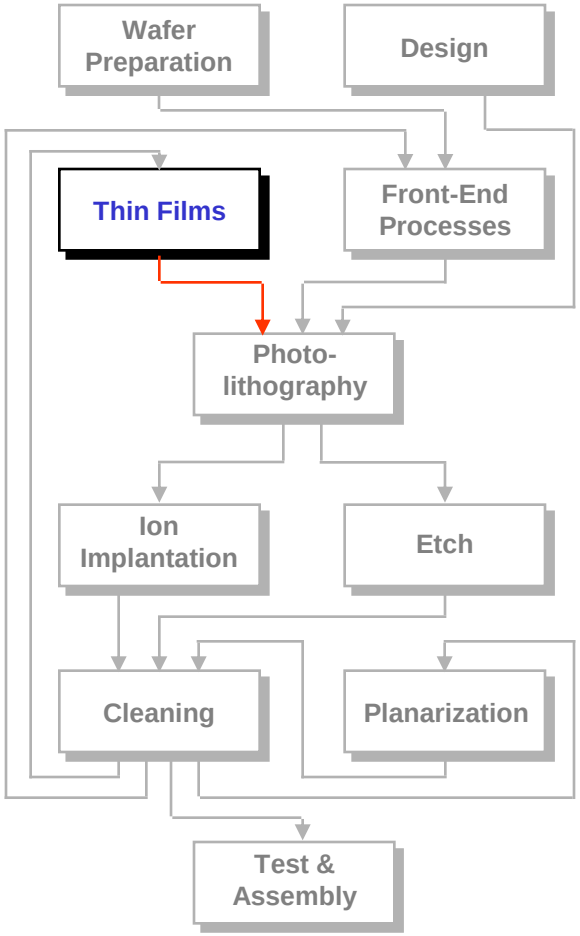
Two types:

Chemical Vapor Deposition (CVD)

- Reactive gases interact with substrate
- Used to deposit Si and dielectrics
- Good film quality
- Good step coverage

Physical Vapor Deposition (PVD)

- Used to deposit metals
- High purity
- Line of sight
- Dielectric

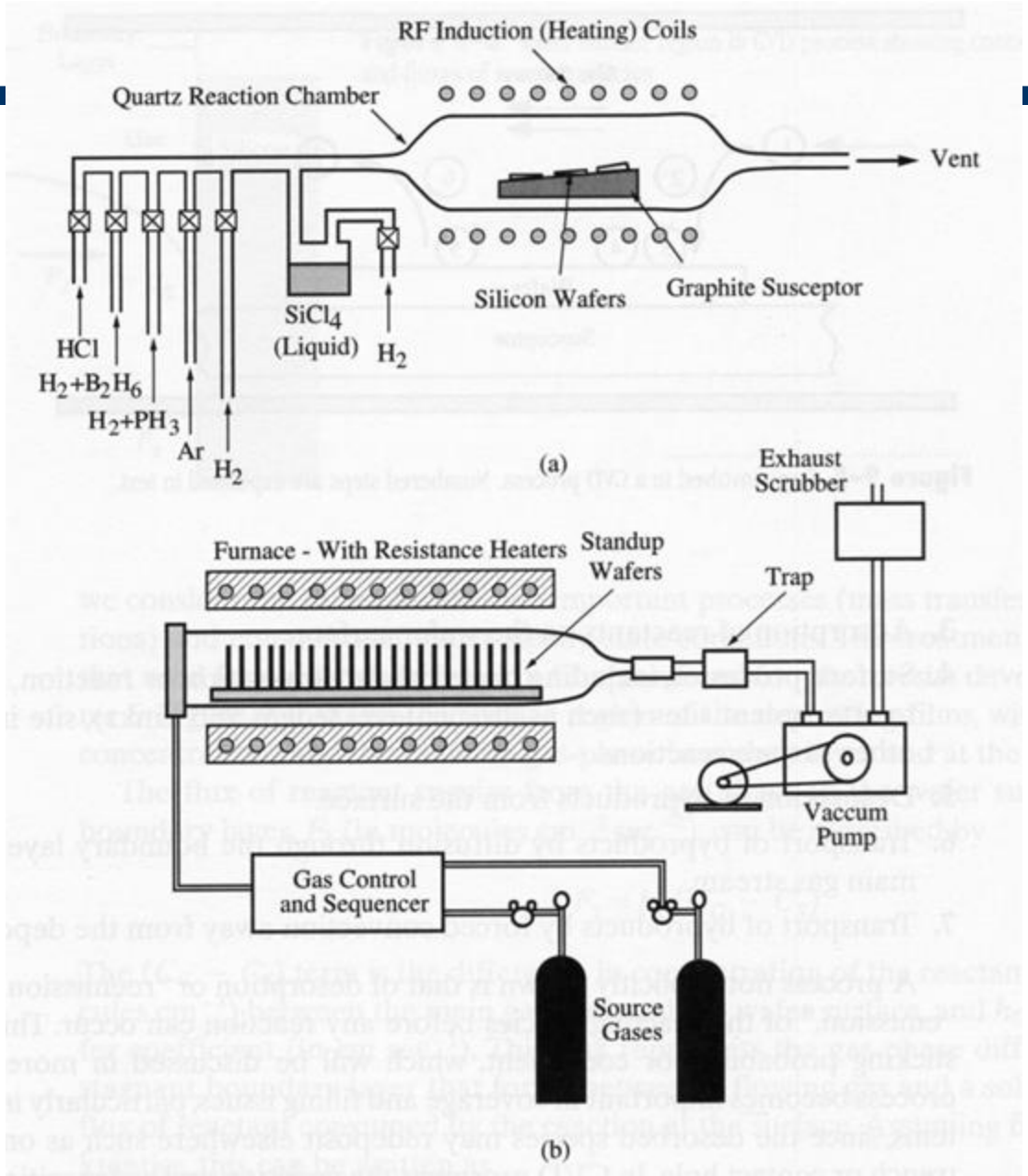


Chemical Vapor Deposition (CVD)

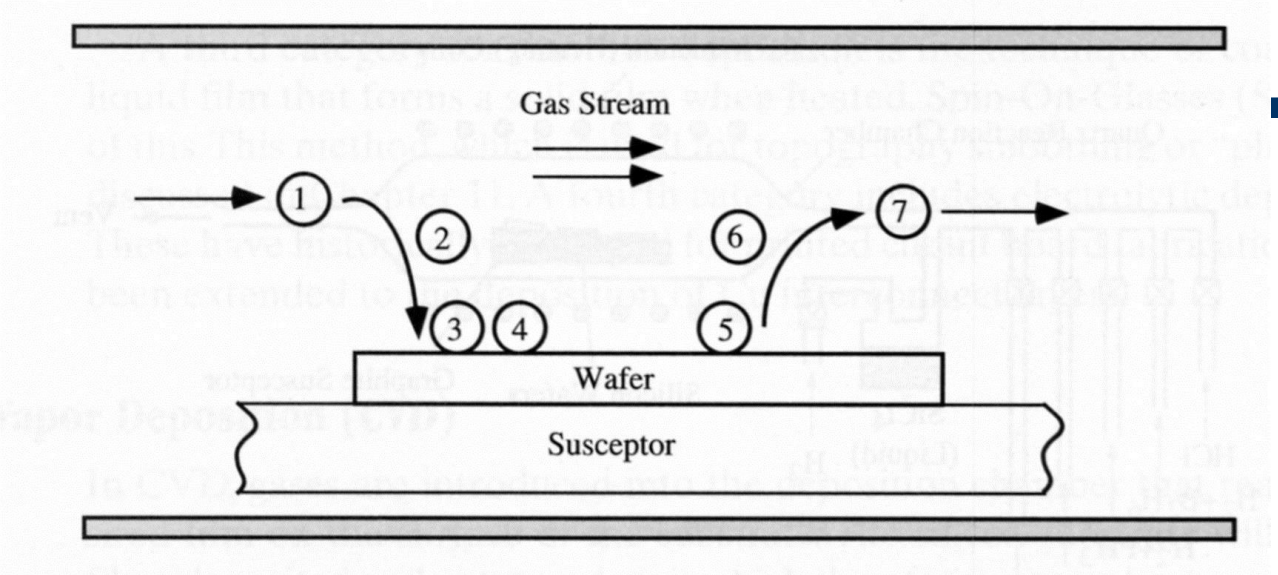
Gases react with substrate

Various types of CVD:

- Atmospheric pressure – APCVD
- Low pressure – LPCVD
- Plasma enhanced – PECVD
- High density plasma - HDPCVD

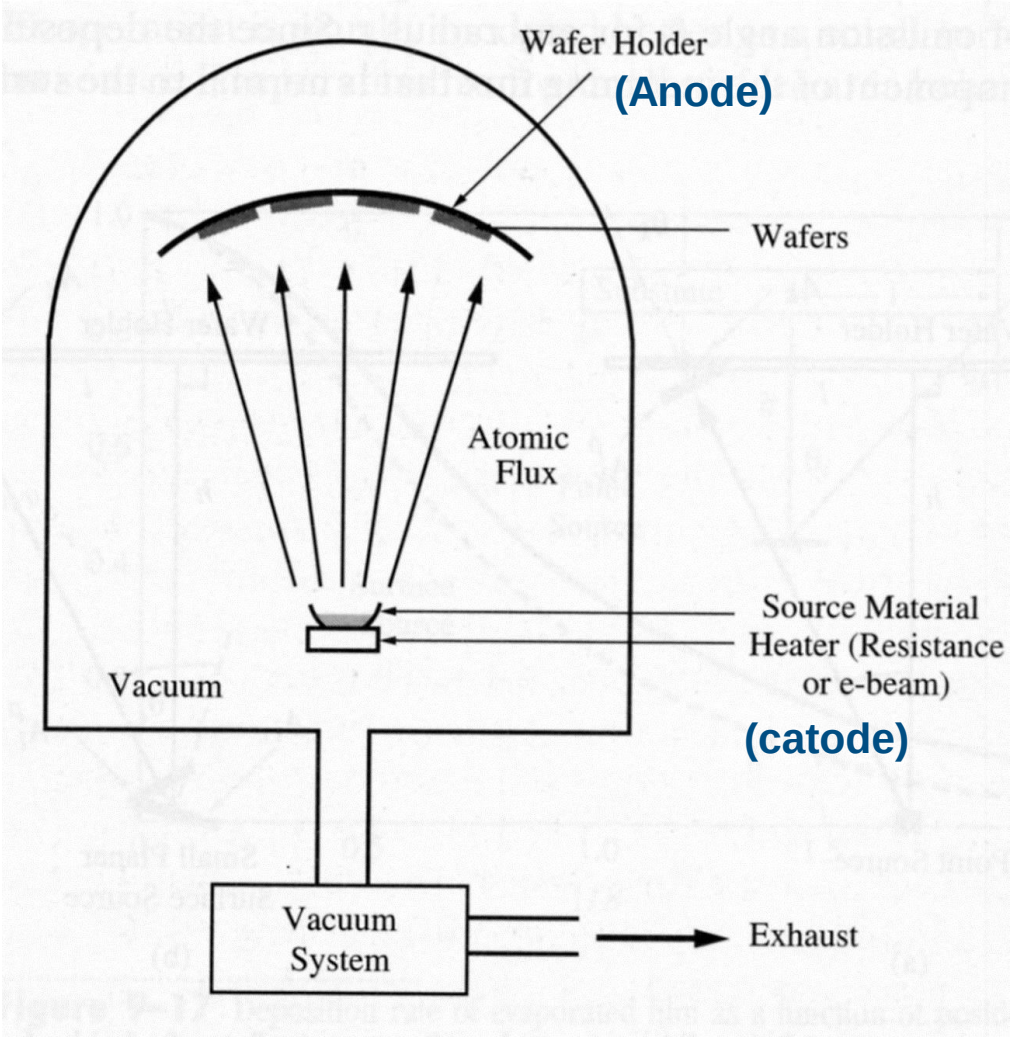


Steps in CVD



1. Transport reactants via forced convection to reaction region
2. Transport reactants via diffusion to wafer surface
3. Adsorb reactants on surface
4. Surface processes: chemical decomposition, surface migration, site incorporation, etc.
5. Desorption from surface
6. Transport byproducts through boundary layer
7. Transport byproducts away from deposition region

Physical Vapor Deposition (PVD)



2 types: *evaporation* and *sputtering*

Advantages:
Versatile – deposits almost any material
Very few chemical reactions
Little wafer damage

Limitations:
Line-of-sight
Shadowing
Thickness uniformity
Difficult to evaporate materials with low vapor pressures

Front-End Processes

Thermal Oxidation

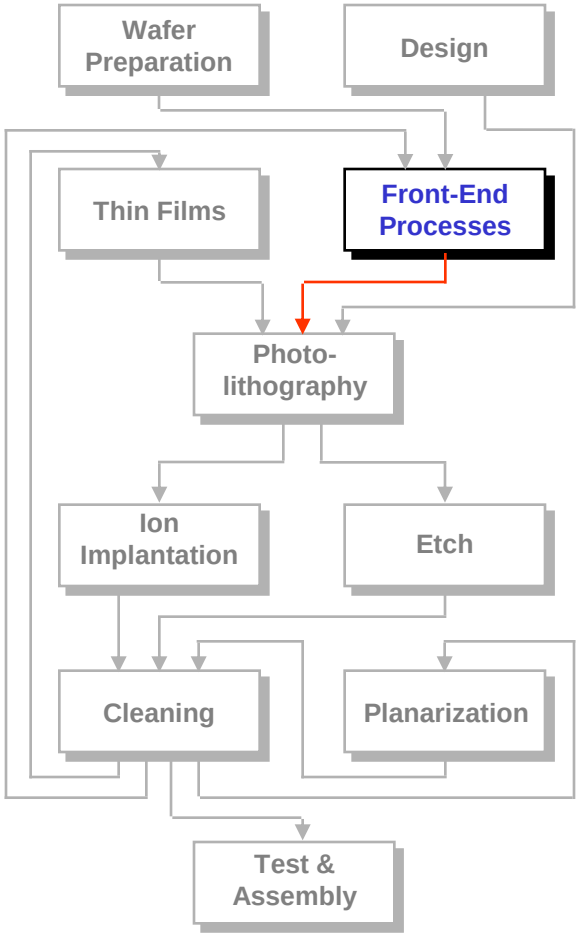
Silicon Nitride Deposition

- Low Pressure Chemical Vapor Deposition (LPCVD)

Polysilicon Deposition

- Low Pressure Chemical Vapor Deposition (LPCVD)

Annealing



Design

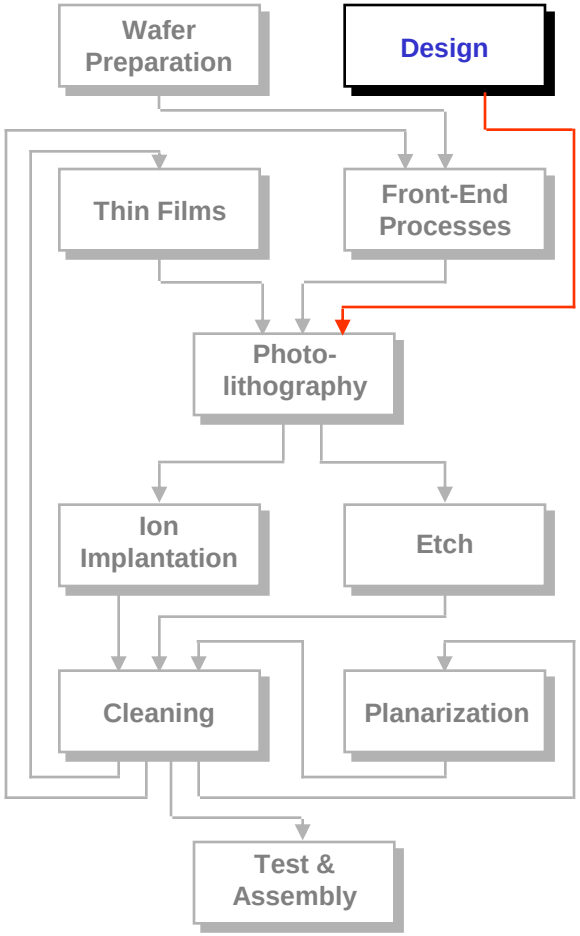
Establish Design Rules

Circuit Element Design

Interconnect Routing

Device Simulation

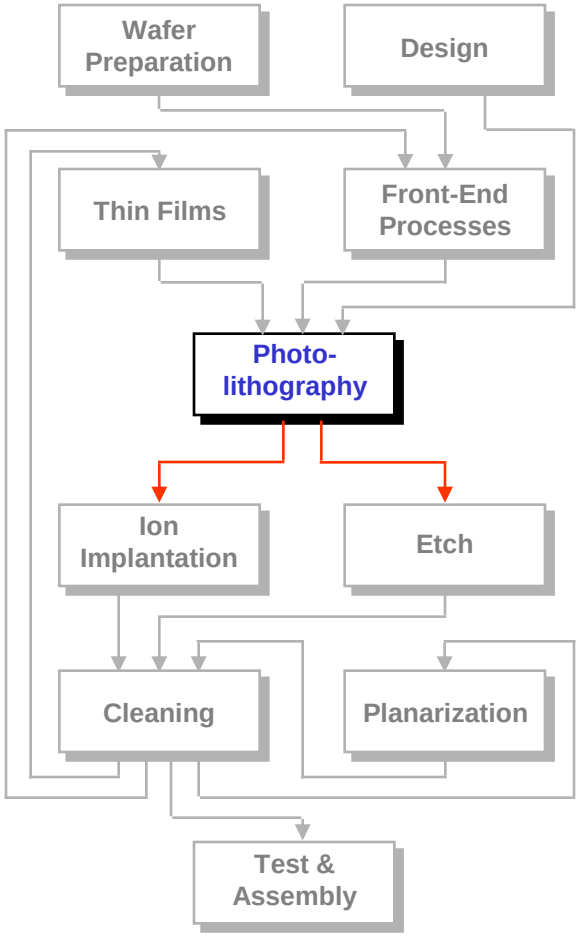
Pattern Preparation



Photolithography

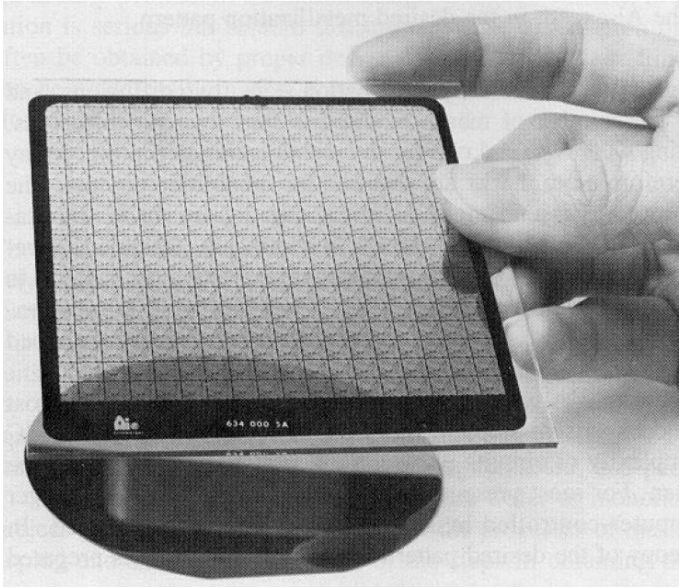
Photoresist Coating Processes

Exposure Processes

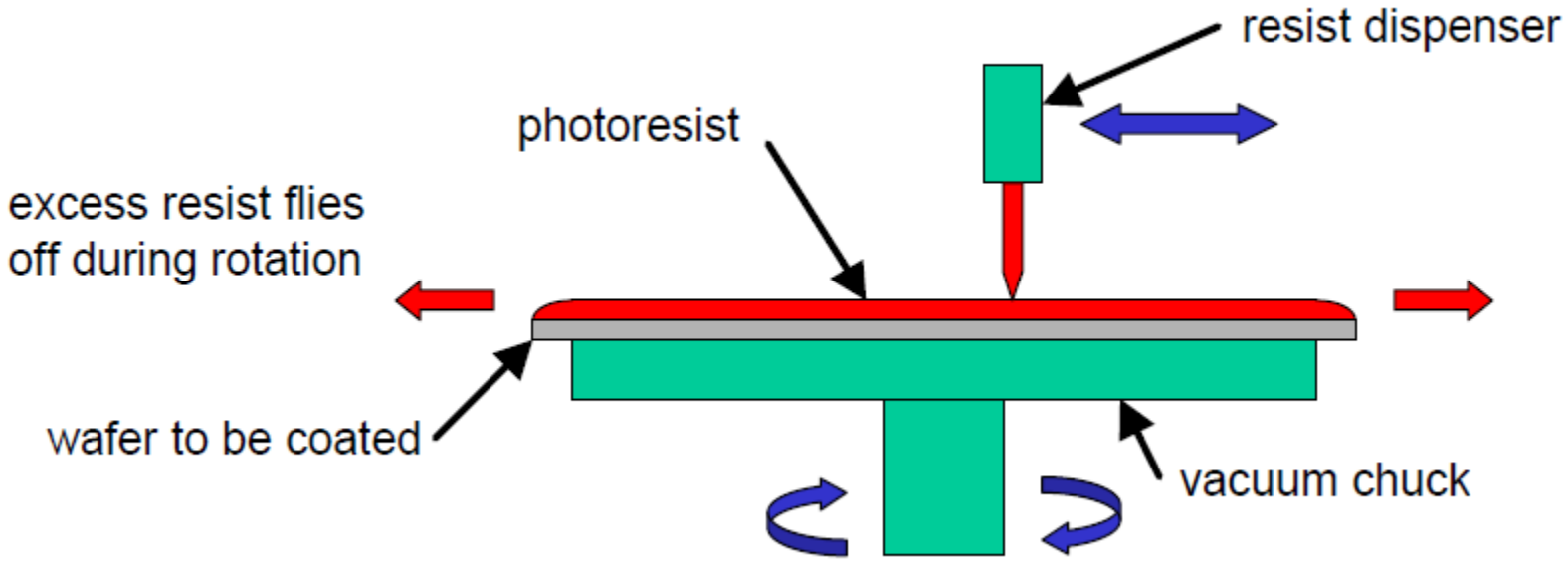


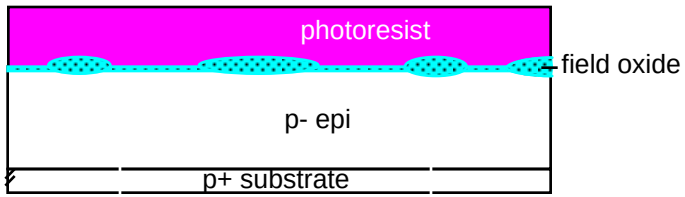
Photolithography

- Photo-litho-graphy: latin: light-stone-writing
- Photolithography is an optical means for transferring patterns onto a substrate. It is essentially the same process that is used in lithographic printing.
- Patterns are first transferred to an imagable photoresist layer.
- Photoresist (or ‘resist’) is a liquid film that can be spread out onto a substrate, exposed with a desired pattern, and developed into a selectively placed layer for subsequent processing.
- Photolithography is a binary pattern transfer: there is no gray-scale, color, nor depth to the image.



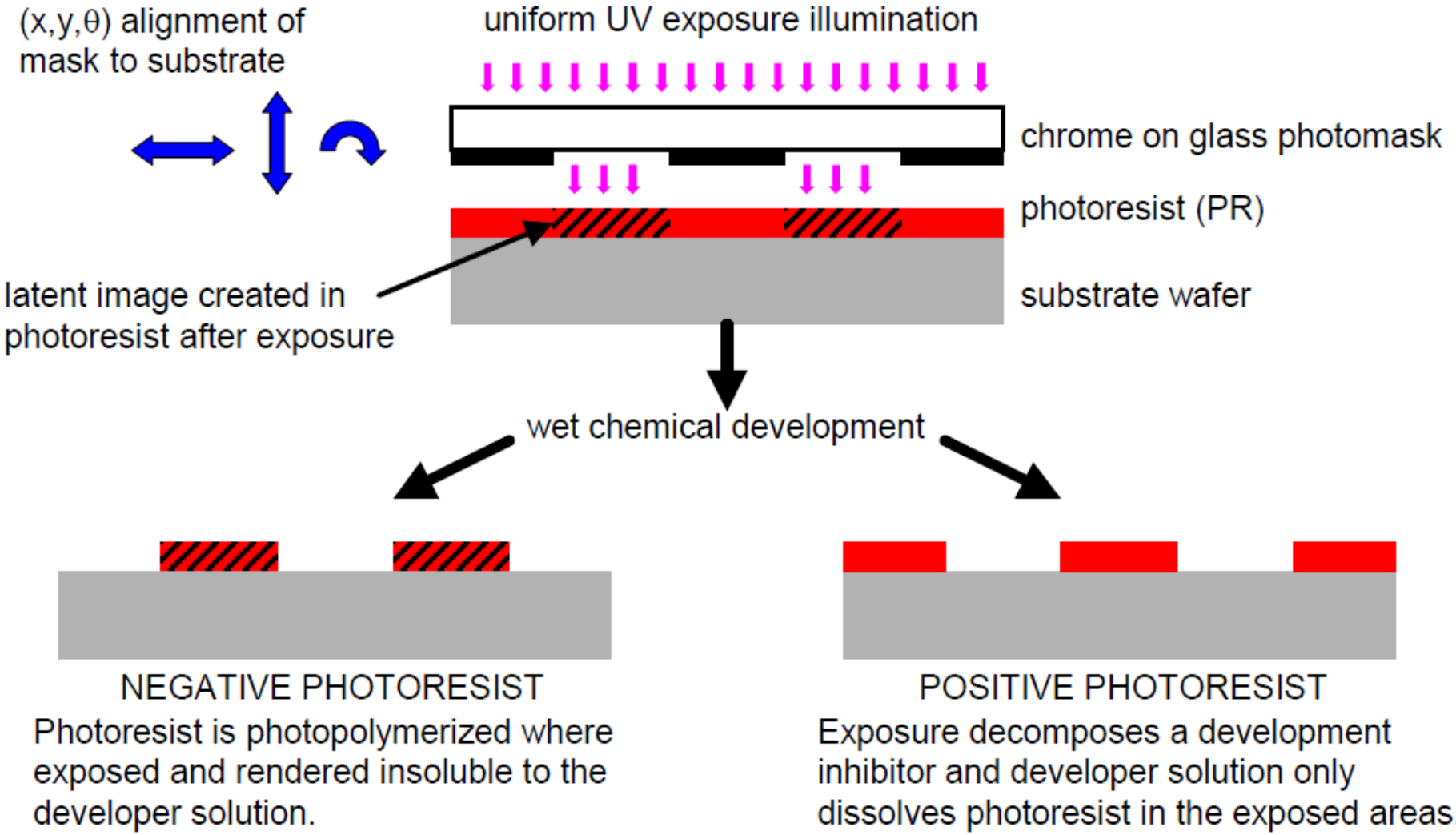
Photoresist Spin Coating





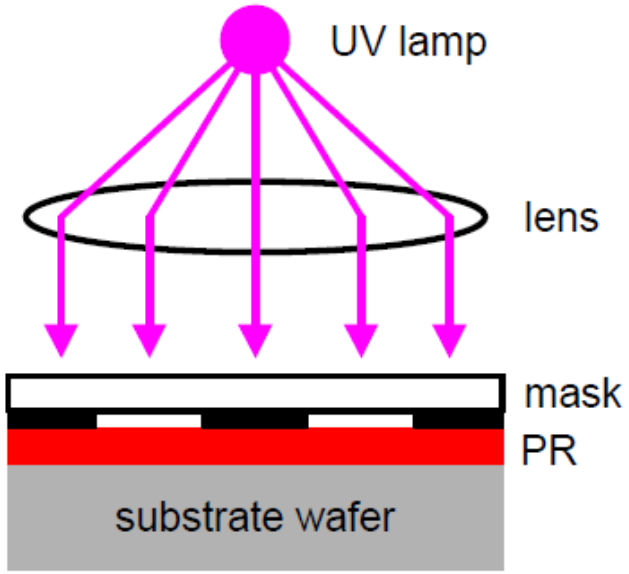
Photoresist Application
(Ontrak)

Alignment, exposure, development processes



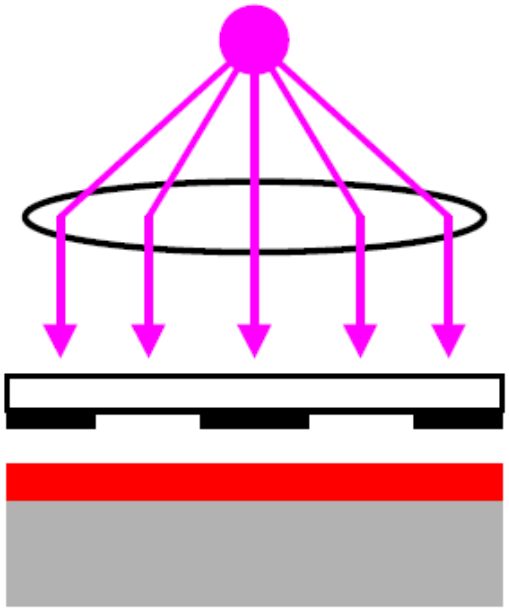
Alignment and exposure hardware

CONTACT ALIGNER



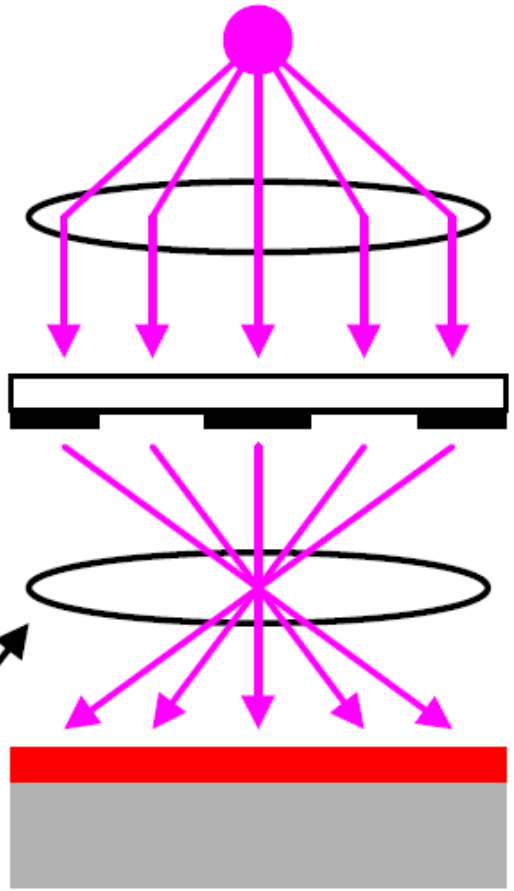
2 operating modes:
contact for expose;
separate for align.
Examples:
Kaspar 17A
Oriel
Karl Suss MJB3

PROXIMITY ALIGNER



less wear on mask, but poorer image than from a contact aligner.
Examples:
Kaspar-Cobilt

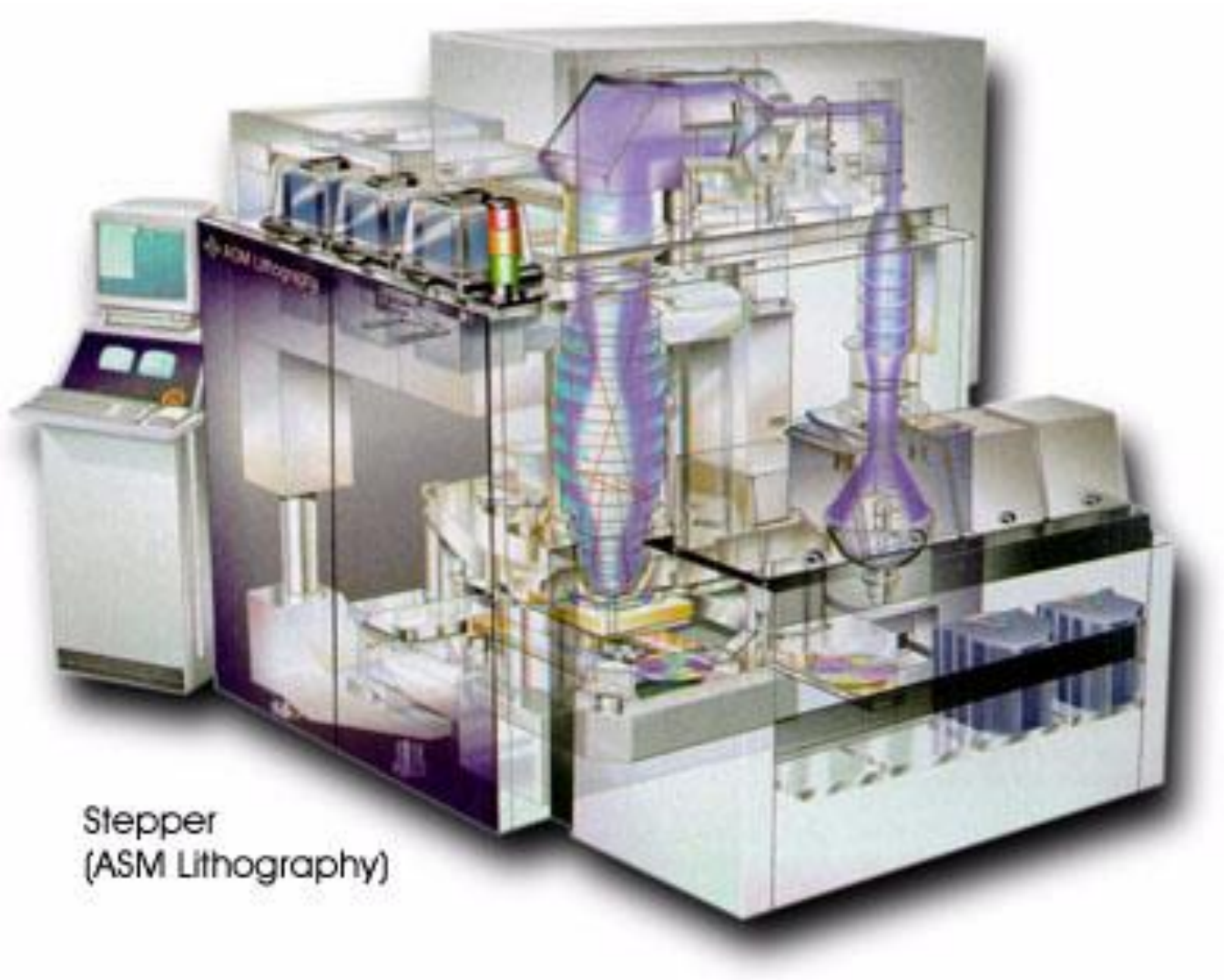
PROJECTION ALIGNER



Examples:
Perkin-Elmer Micralign

Projection systems use imaging optics in between the mask and the wafer

Exposure Processes

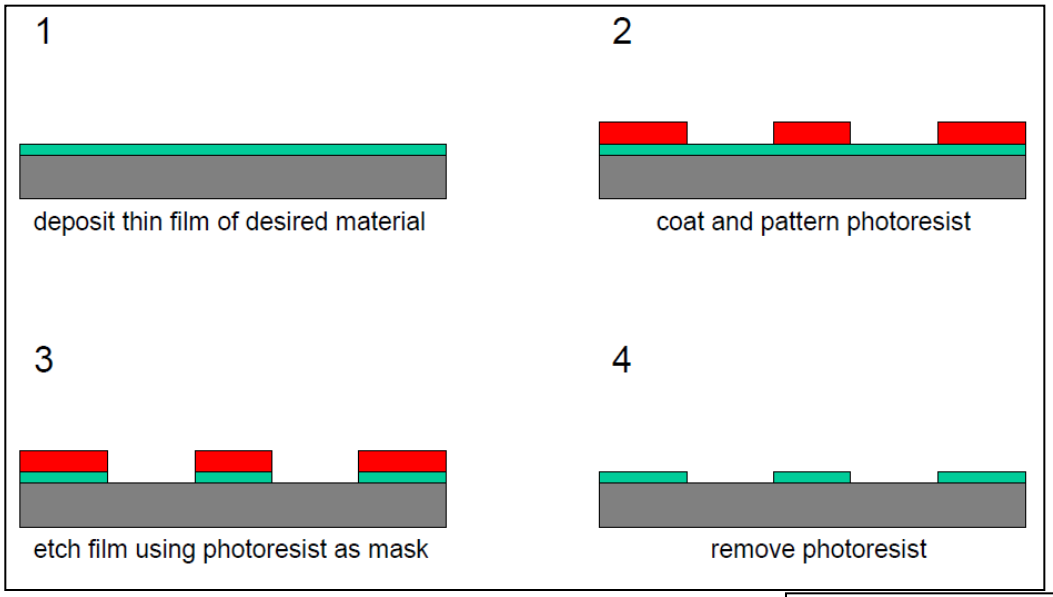


Additive → deposition

Subtractive → etching

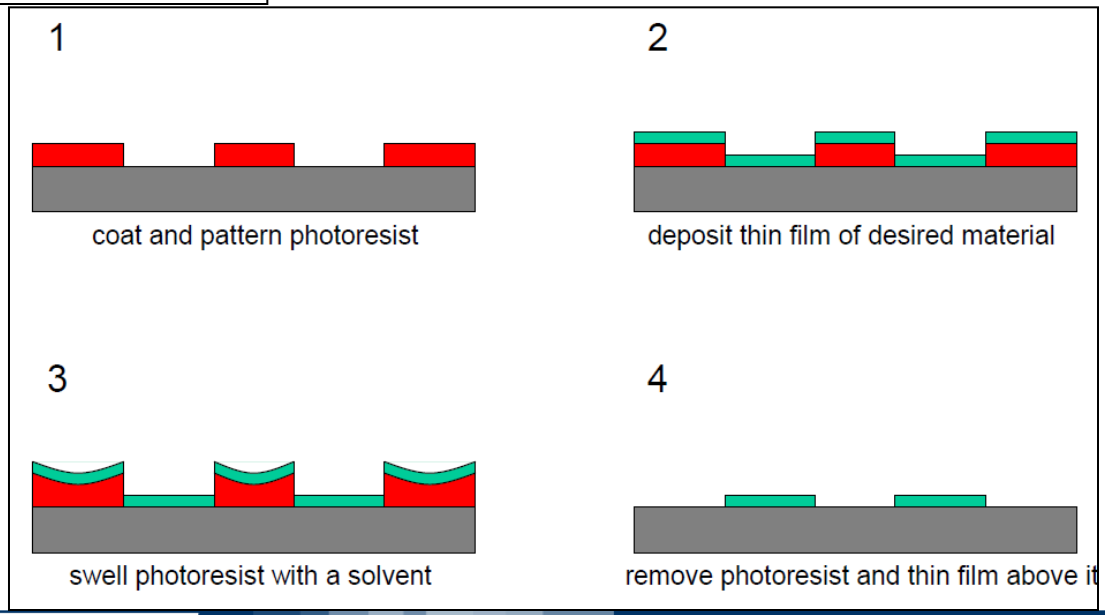
Modifying → doping, annealing, or curing

Etch back and Lift off



'**Etch back**' (additive process):
- photoresist is applied overtop of the layer to be patterned
- unwanted material is etched away

'**Lift off**' (subtractive process):
- patterned layer is deposited over top of the photoresist
- unwanted material is lifted off when resist is removed

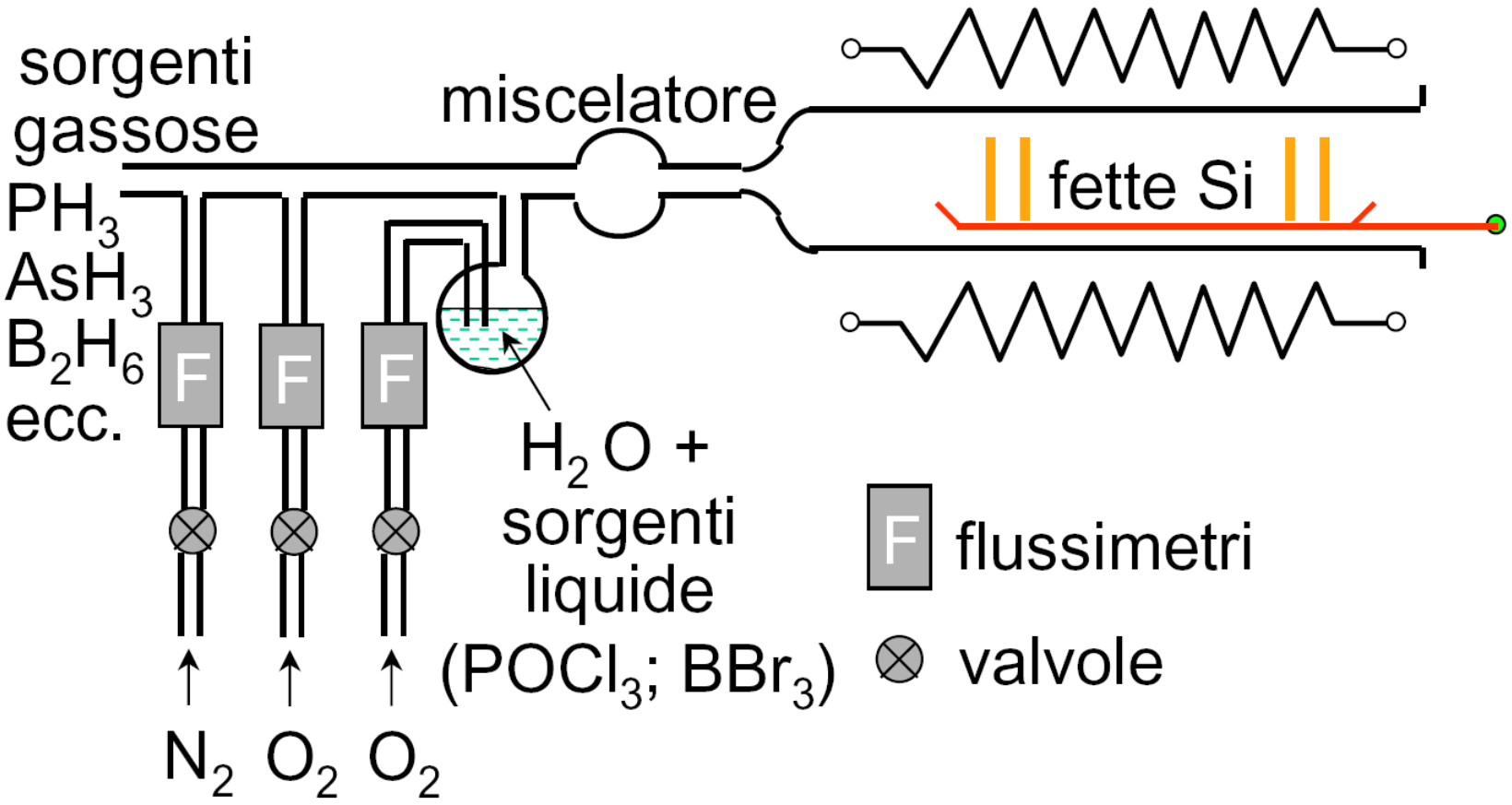


Doping

- **Diffusion**: dopant atoms are brought onto the wafer surface by chemical deposition, at high temperature (e.g. 900-1000 °C) and then they diffuse into the substrate.
  - Monotonic, decreasing profile of dopants into the substrate (not very flexible and controllable)
  - treatment at high temperature, potentially destructive

- **Ion implantation**: dopants are implanted into the substrate as high energy ‘bullets’.
  - the concentration profile in the substrate can be controlled
  - treatment at intermediate temperature

Diffusion

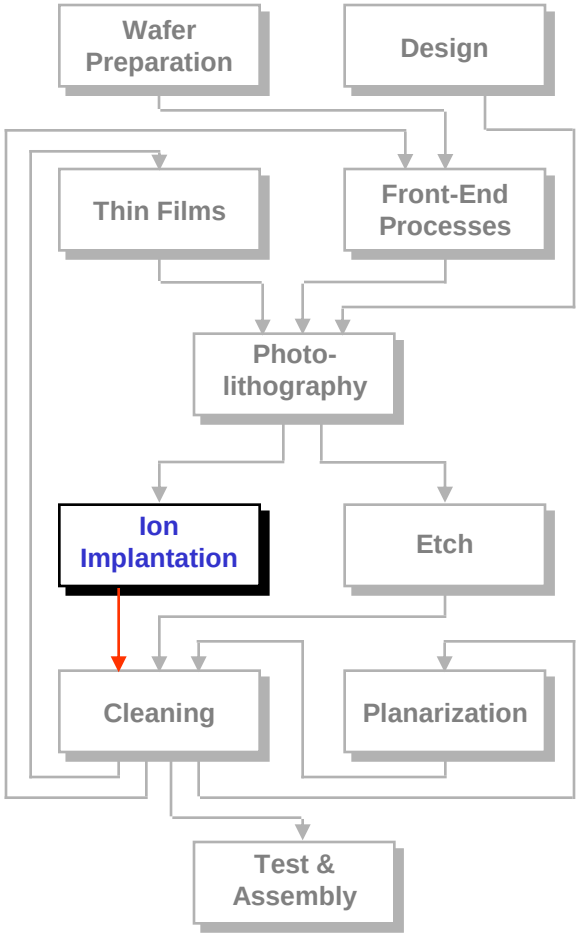

sorgenti
gassose
PH_3
AsH_3
B_2H_6
ecc.
F
F
F
miscelatore
fette Si
H_2O +
sorgenti
liquide
($POCl_3$; BBr_3)
N_2 O_2 O_2
F flussimetri
valvole

Ion Implantation

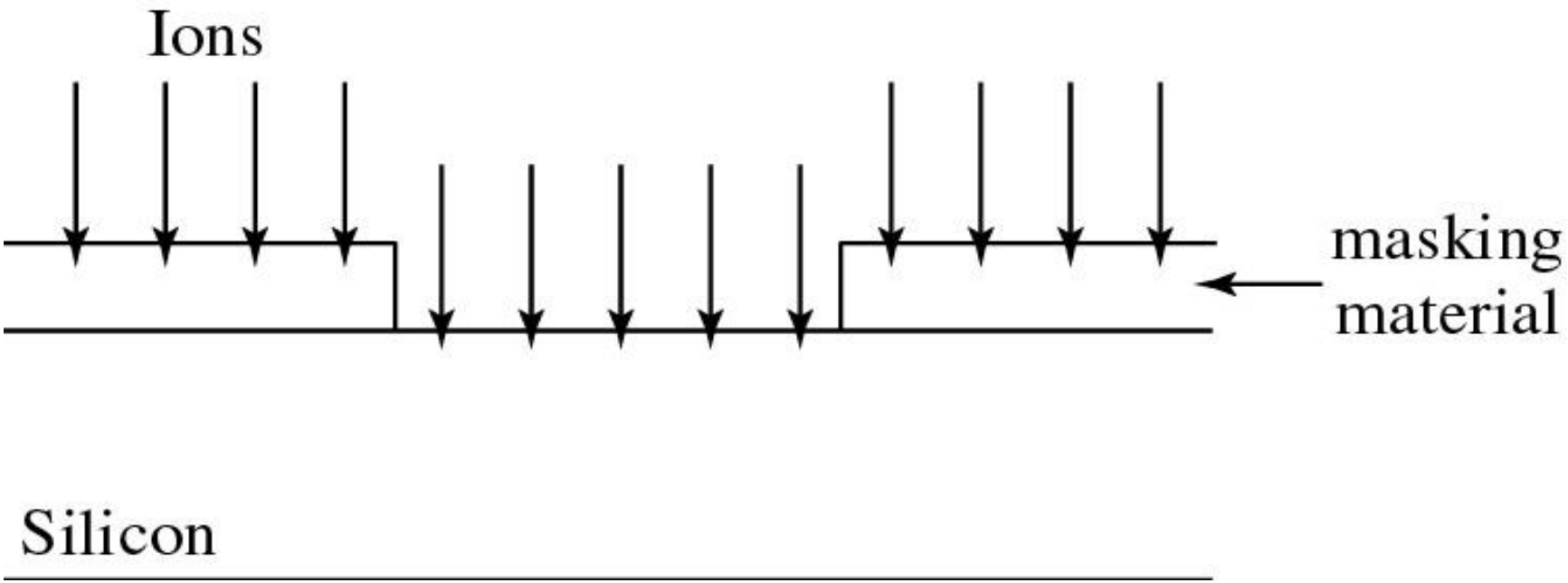
Well Implants

Channel Implants

Source/Drain Implants

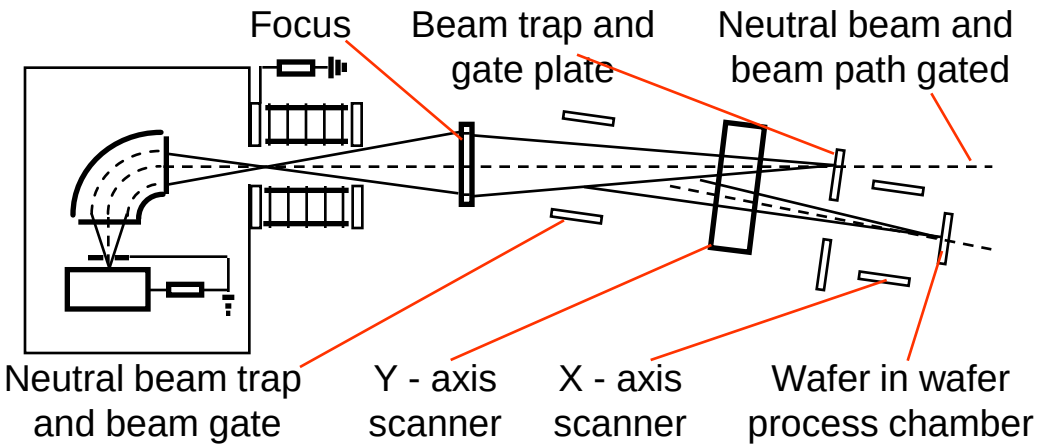


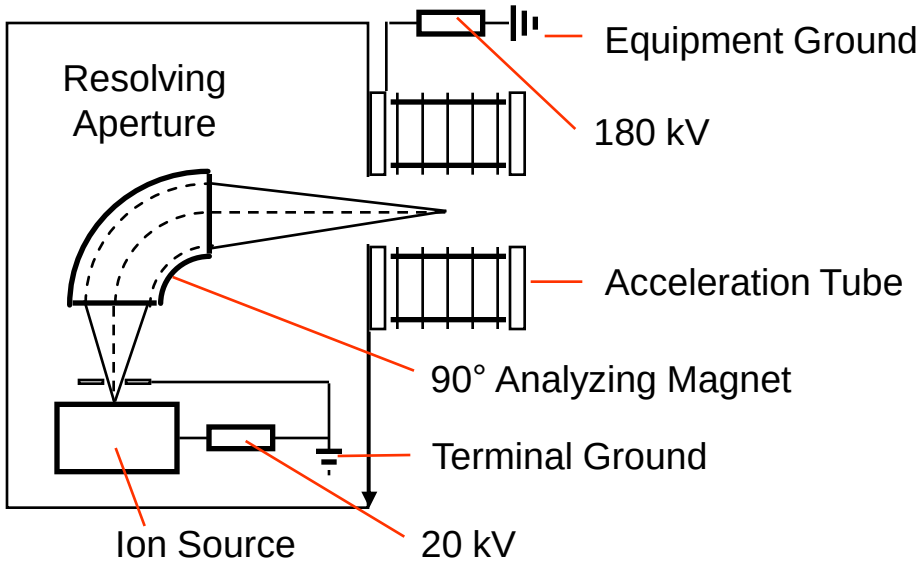
Ion Implantation

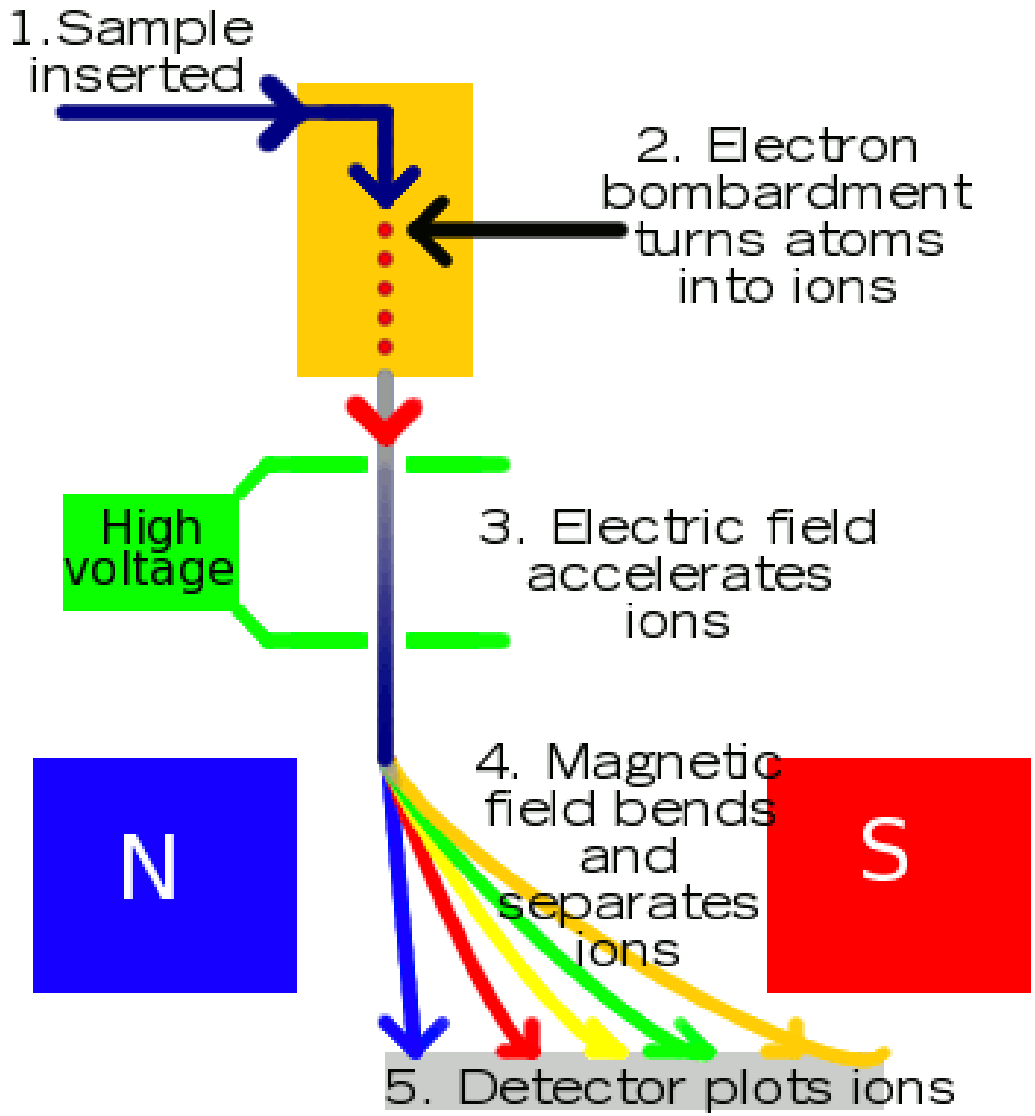


A high-energy beam of ions hits selected regions on semiconductor surface, and penetrate in them.

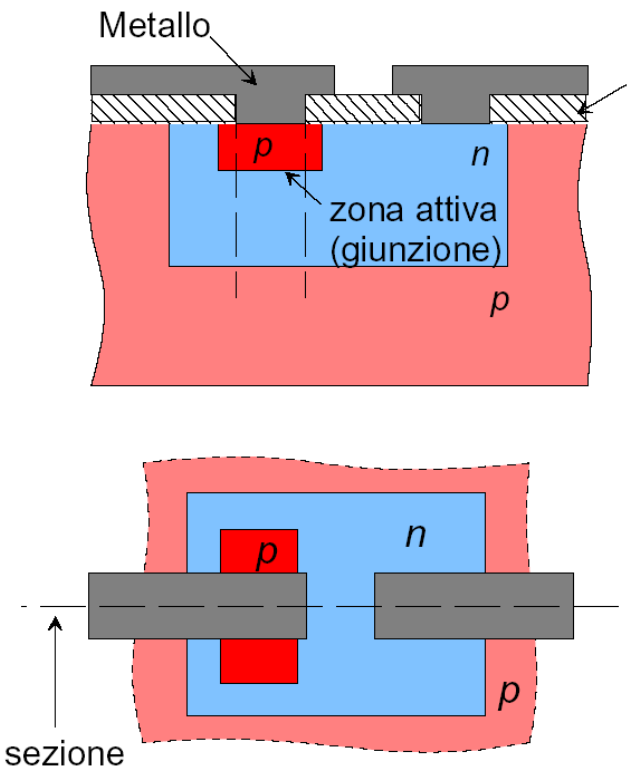
Ion Implantation

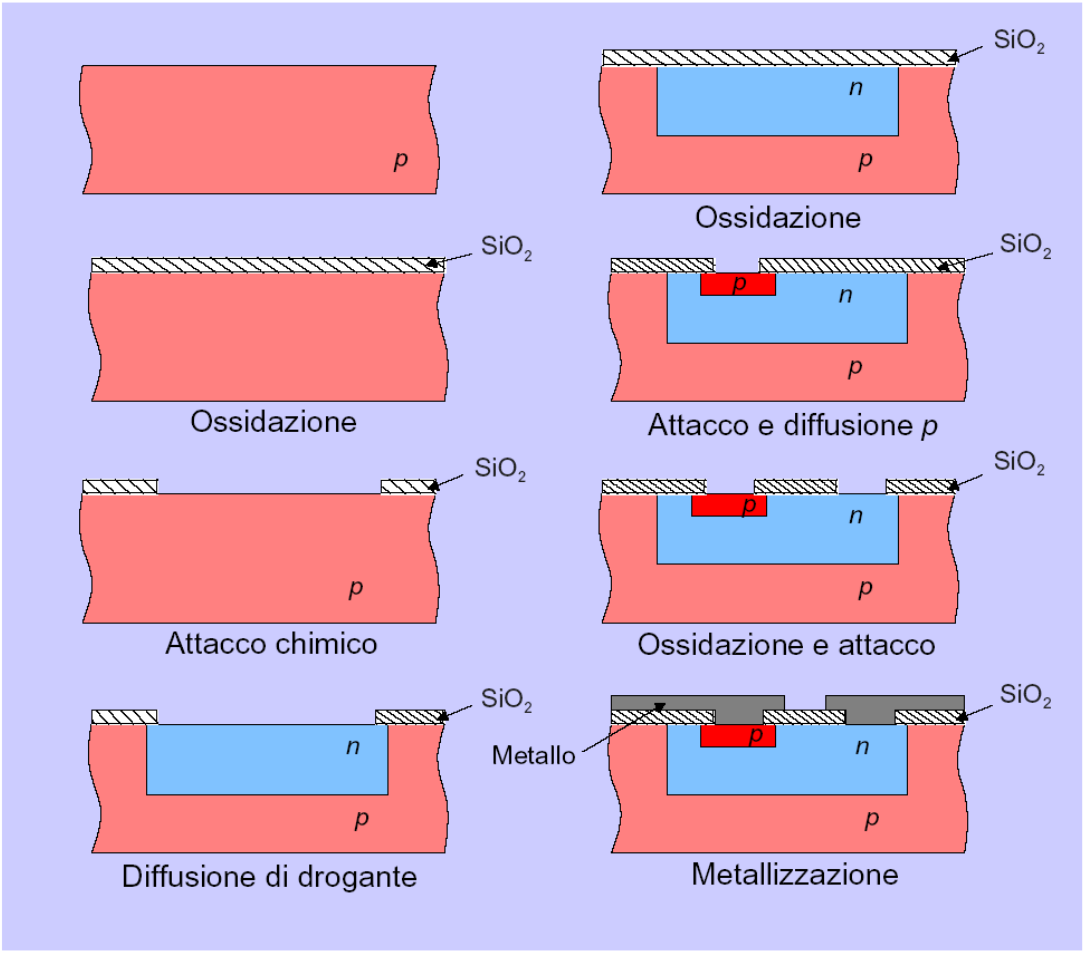




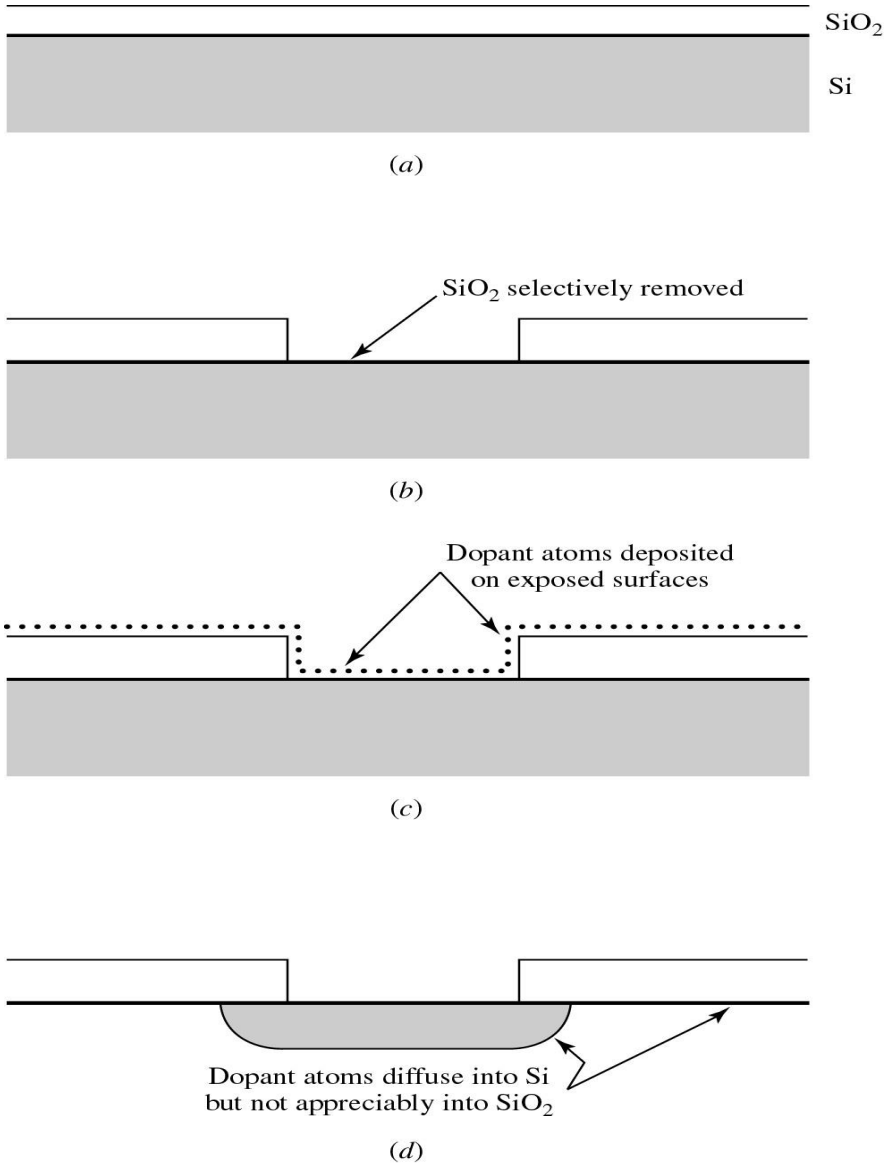

1.Sample inserted
2. Electron bombardment turns atoms into ions
High voltage
3. Electric field accelerates ions
N
4. Magnetic field bends and separates ions
S
5. Detector plots ions

Example: integrated p-n diode





Planar process



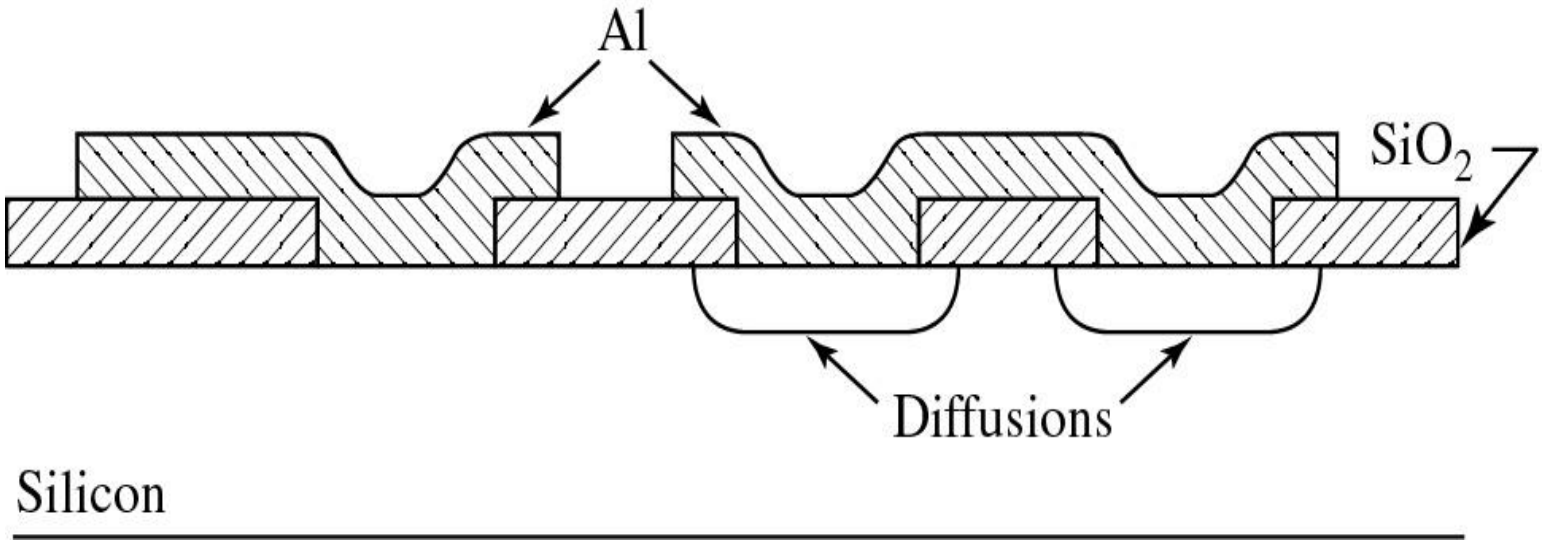
(*a*) Oxide formation,

(*b*) Oxide removal

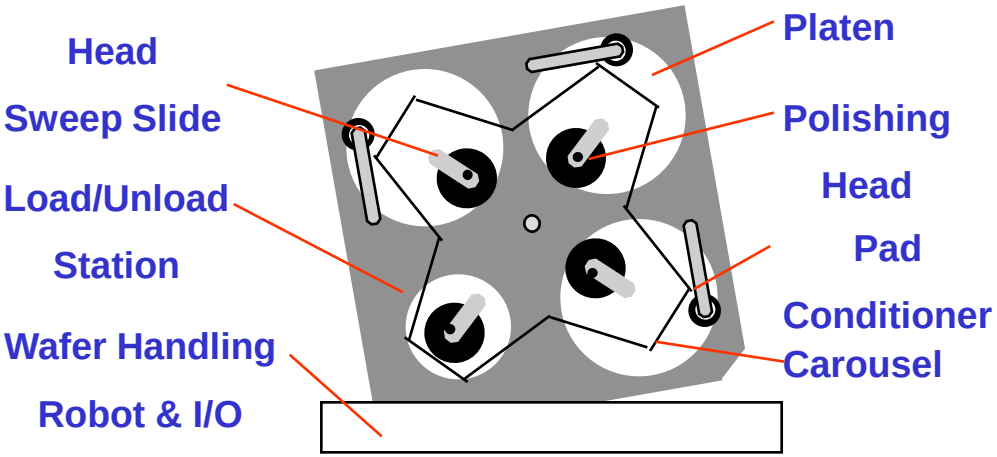
(*c*) Deposition of dopant atoms

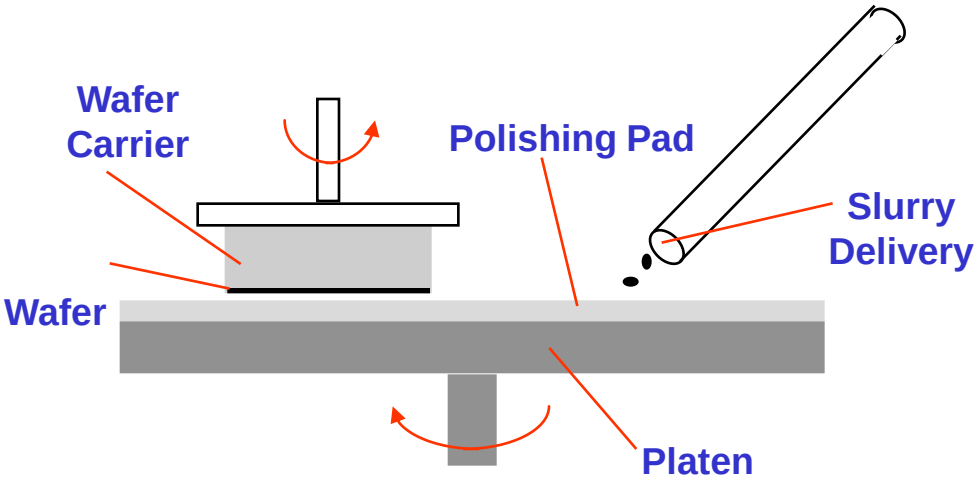
(*d*) Diffusion of dopant atoms in the exposed regions

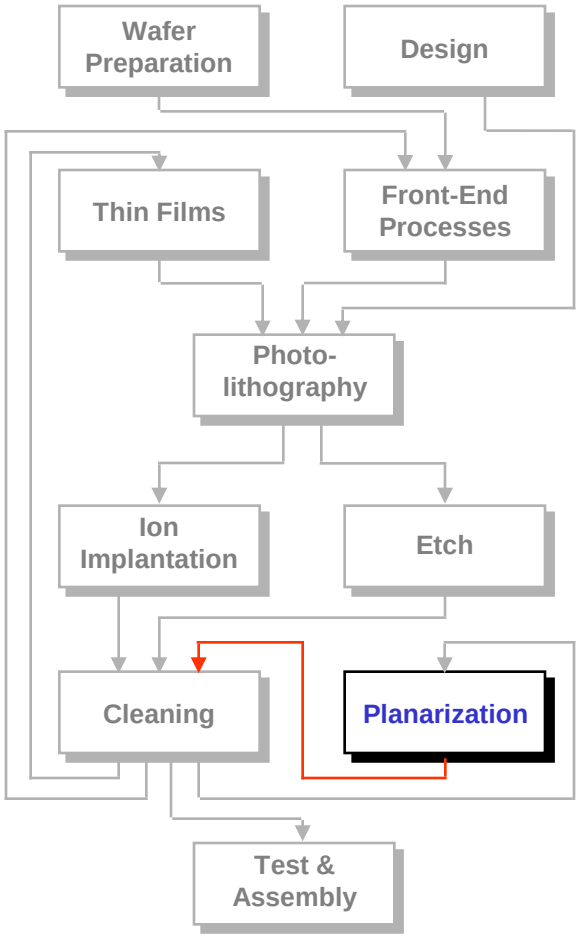
Metallic (Al) connections



Oxide/metal mechanical Planarization







* High proportion of the total product use.

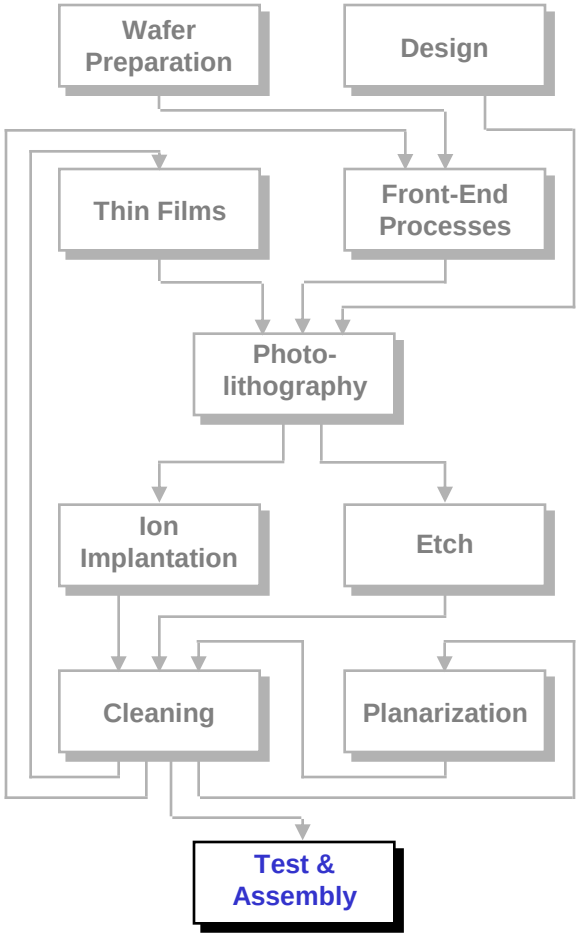
Test and Assembly

Electrical Test Probe

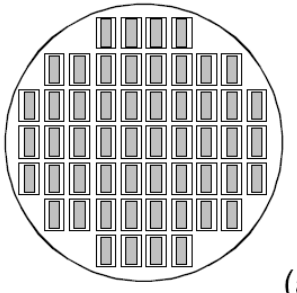
Die Cut and Assembly

Die Attach and Wire Bonding

Final Test

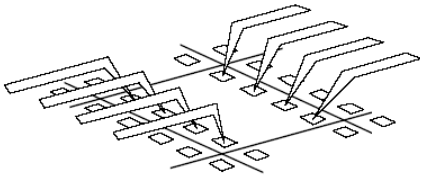


Dicing, testing, packaging



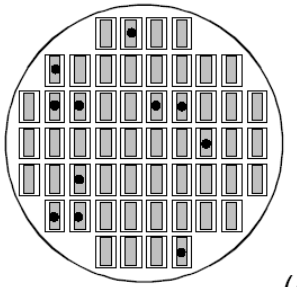
Substrate at the end of the process

(a)



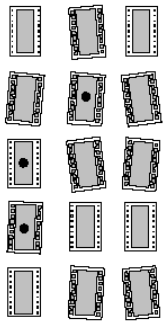
(b)

Automatic testing
(chips are electrically tested under varying environmental conditions)



Identification of the chips with defects

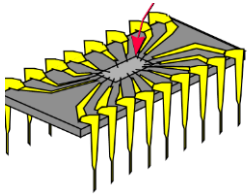
(c)

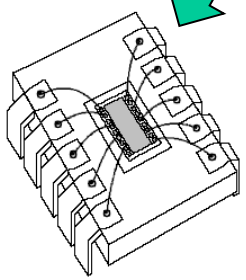


Dicing of the substrate in the single chips

(d)

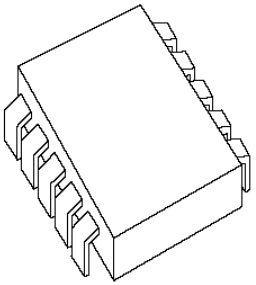
Good chips are attached to a lead frame package





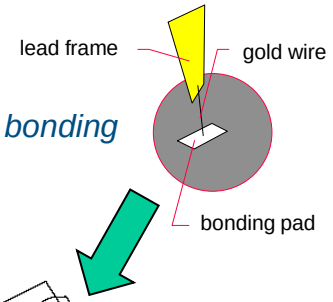
Assembly in a dual-in-line package

(e)

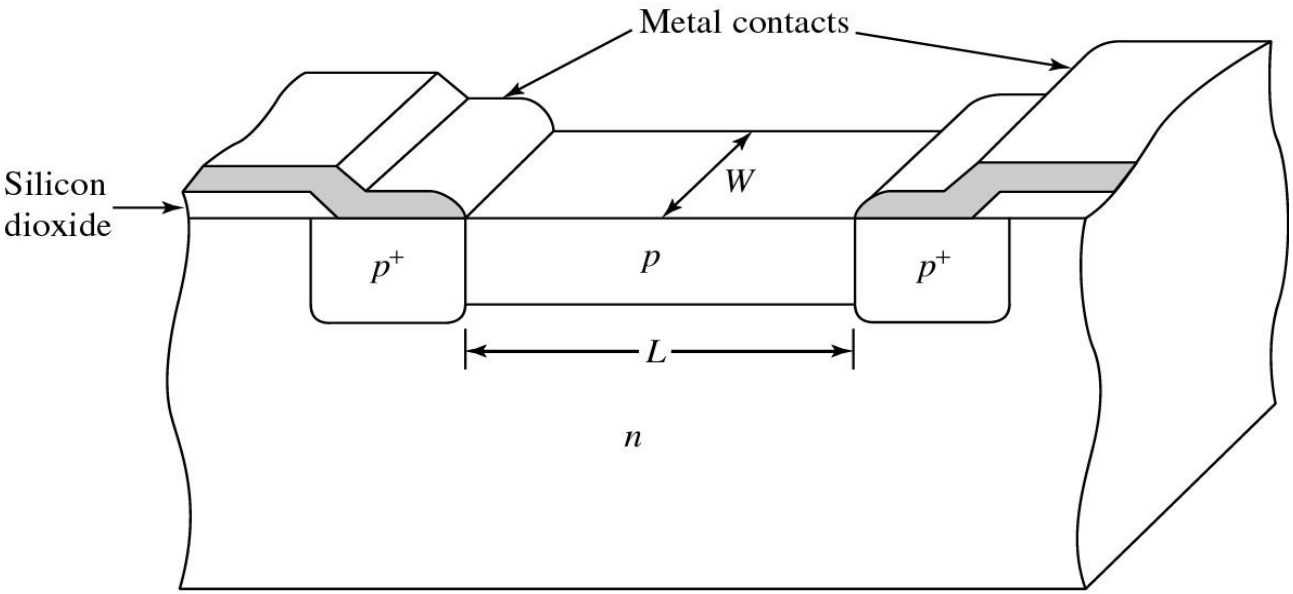


Package closure

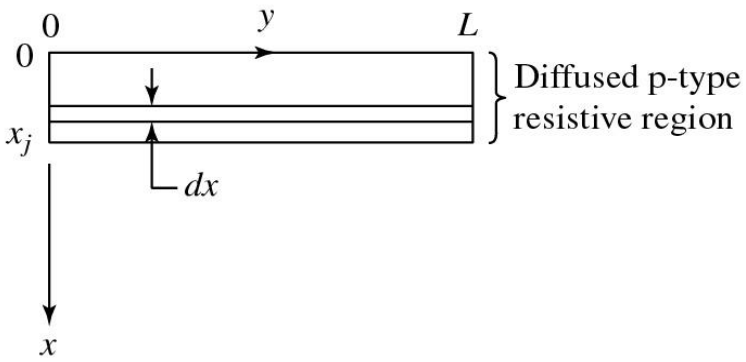
(f)



Diffused or Implanted IC Resistor



(a)



(b)

Sheet resistivity

Resistivity (Ω· m) of the sample:

$$\rho = \frac{R\,Wh}{L} = \frac{V\,Wh}{I\,L}$$

V voltage measured by the voltmeter in V
W width of the sample measured in m
h thickness of the sample measured in m
I current flowing through the sample measured by an ammeter in A
L is the length of the film measured in m

For the special case of a **square film** (width *W* equal to the length L) we have:

$$\rho\,(of\ square\ film) = \rho_s = \frac{V\,h}{I}$$

The resistivity of a square film of material is called the “sheet resistivity” of the material and is usually represented by the symbol ρ_s.

Sheet resistivity

The “sheet resistance” R_S is defined by

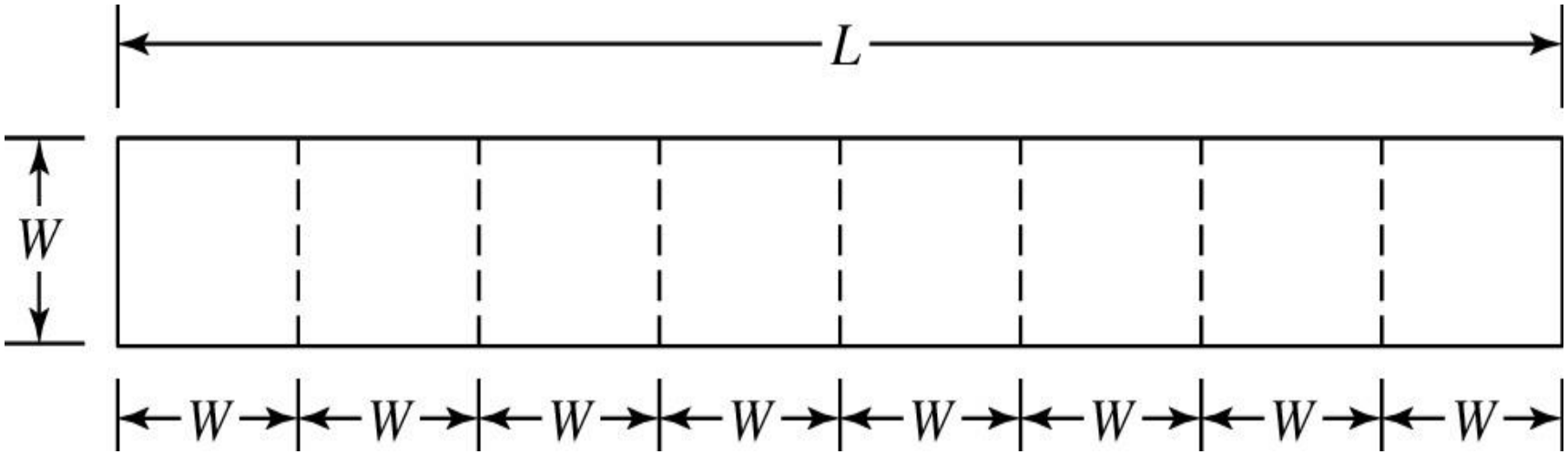
$$R\ (of\ square\ film) = R_s\ = \frac{V}{I}$$

V is the voltage measured by the voltmeter in V;
I is the current the ammeter measures flowing through the sample in A.

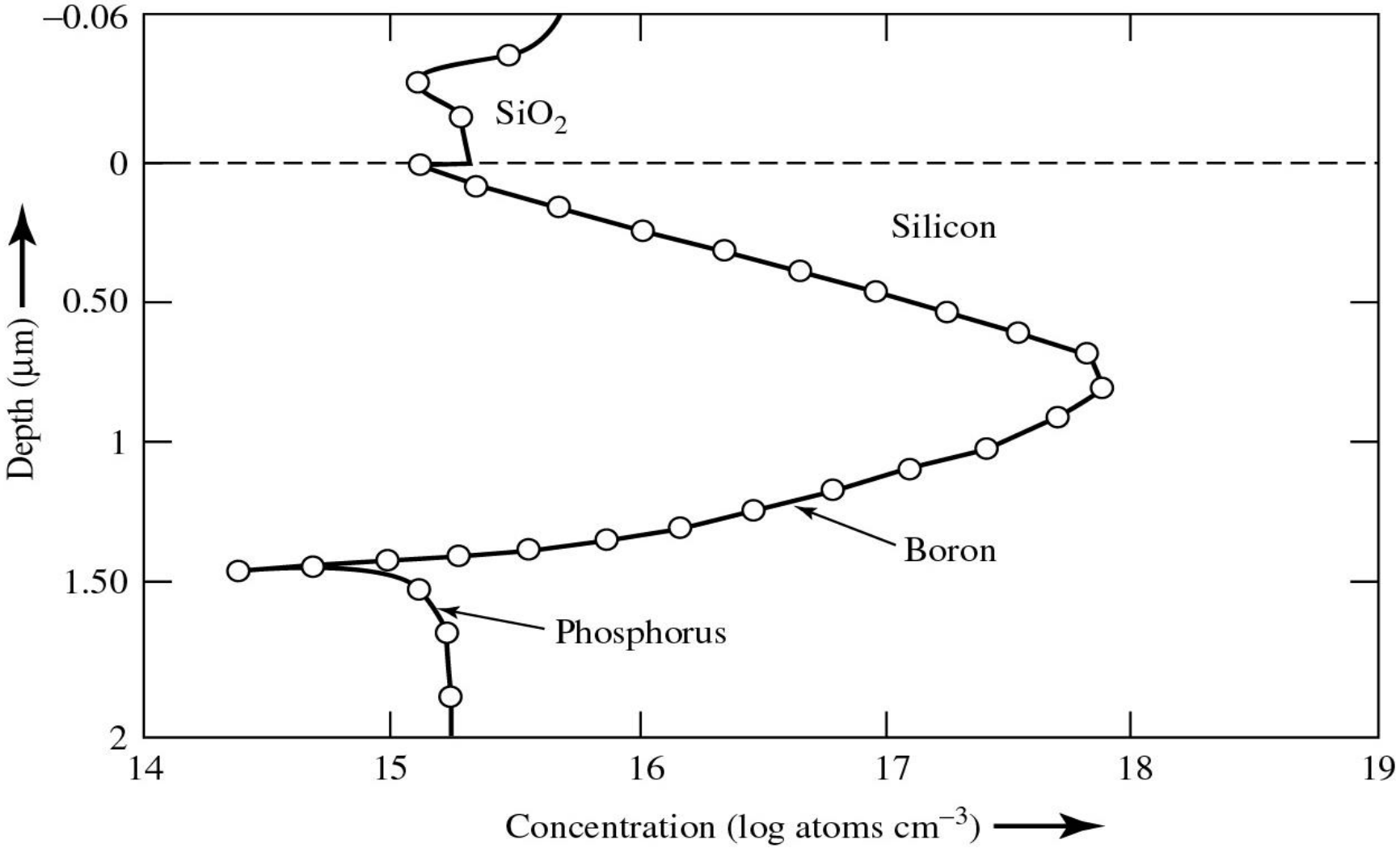
The units for sheet resistance are Ω, but people commonly use the units “**Ω per square**”.

→ The sheet resistance is numerically equal to the measured resistance of a square piece of the material. Note that sheet resistance is independent of the size of the square measured, and it is not necessary to know the film thickness to measure sheet resistance. This makes sheet resistance a useful quantity for comparing different thin films of materials.

An IC Resistor with $N_s = 8$, $R = 8R_s$



Typical IC doping profile



Silicon-based sensors: examples

Stimuli	Effects
Radiant	Photovoltaic effect, photoelectric effect, photoconductivity, photo-magneto-electric effect
Mechanical	Piezoresistivity, lateral photoelectric effect, lateral photovoltaic effect
Thermal	Seebeck effect, temperature dependence of conductivity and junction, Nernst effect
Magnetic	Hall effect, magnetoresistance, Suhi effect
Chemical	Ion sensitivity

Example 1: capacitive accelerometer

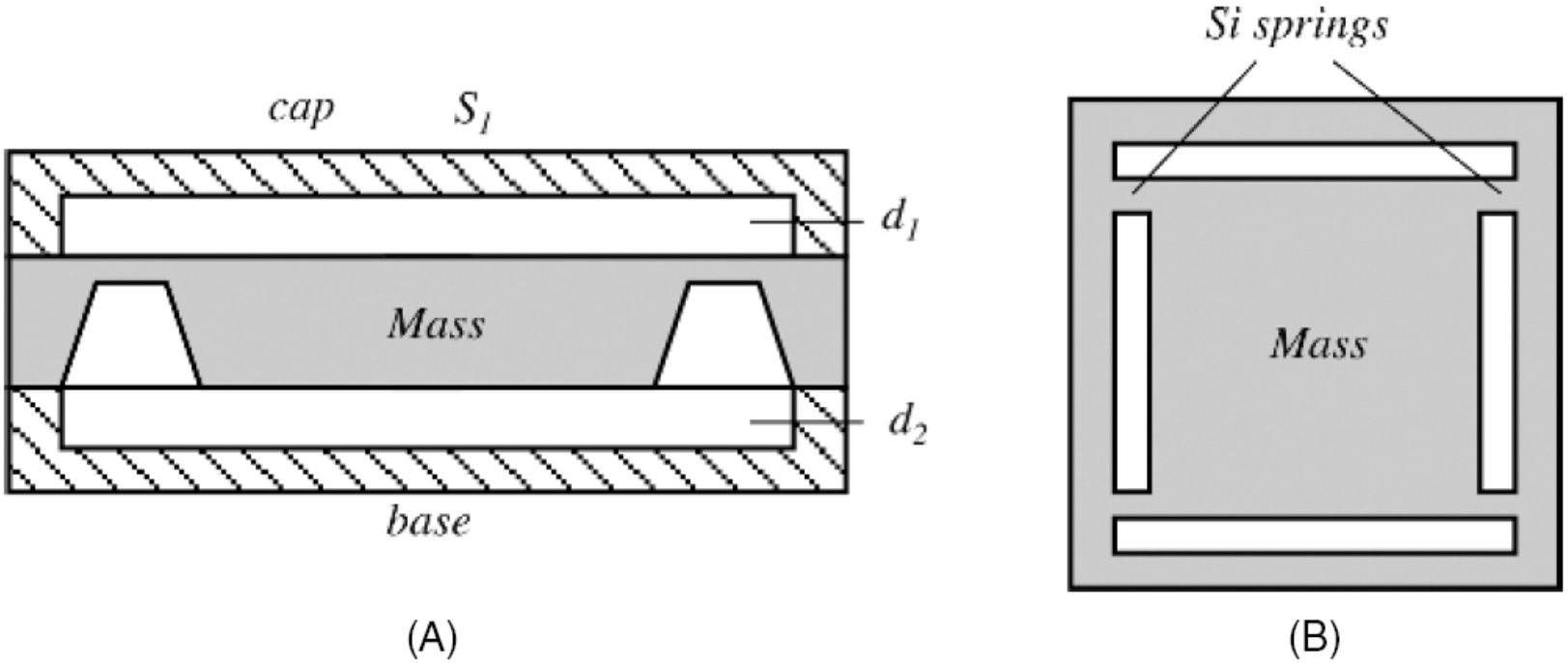


Fig. 8.3. Capacitive accelerometer with a differential capacitor: (A) side cross-sectional view; (B) top view of a seismic mass supported by four silicon springs.

Example 2:
Vacuum diode force sensor

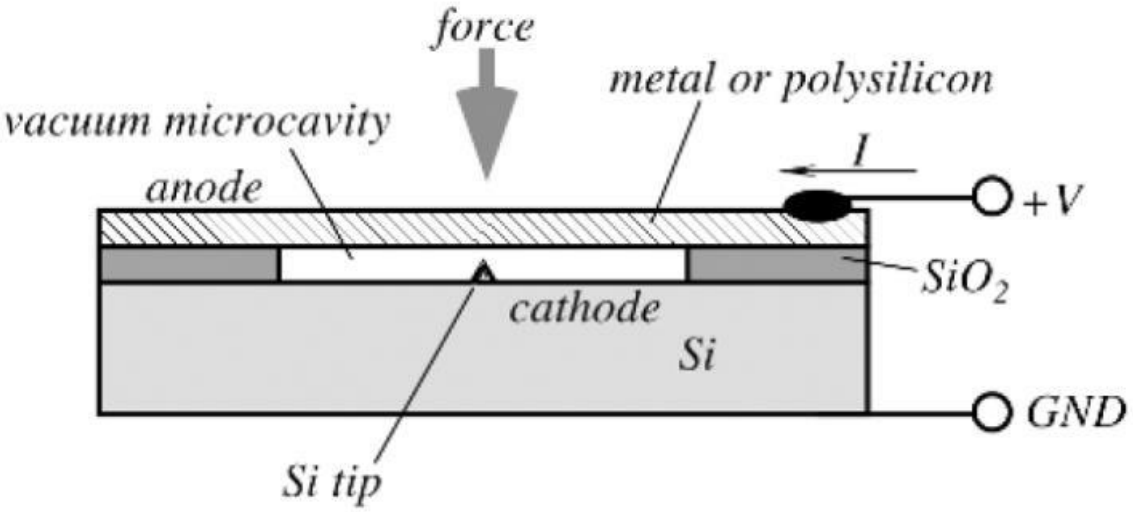


Fig. 9.11. Schematic of a vacuum diode force sensor. (Adapted from Ref. [11].)

Example 3: piezoresistive pressure sensors

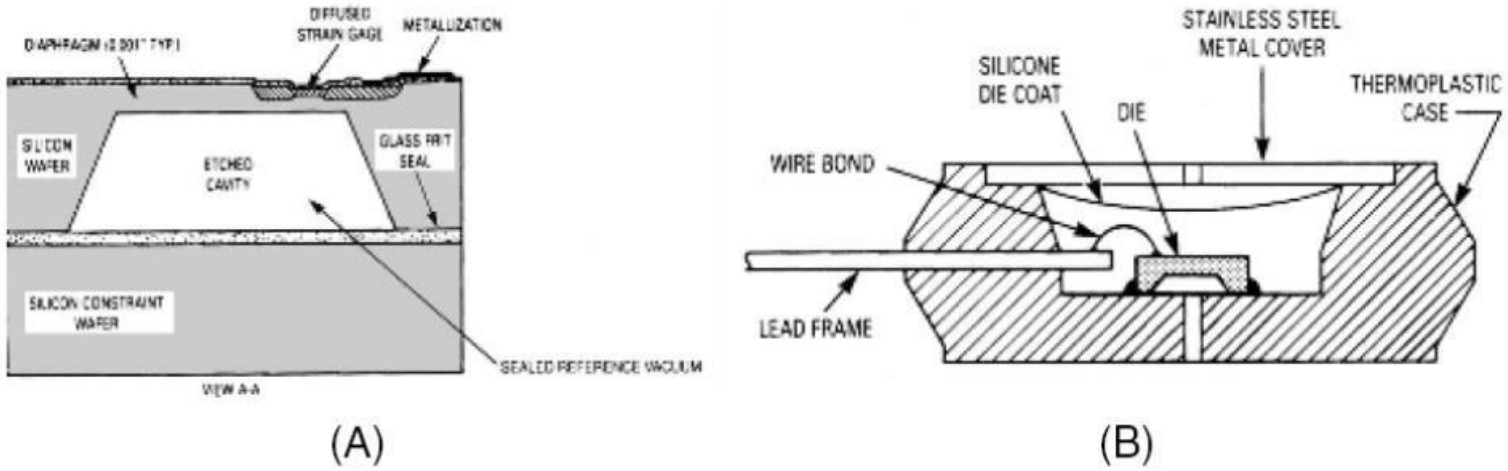


Fig. 10.7. Absolute (A) and differential (B) pressure sensor packagings. (Copyright Motorola, Inc. Used with permission.)

Example 4: SFB process

Silicon Fusion Bonding (SFB) = method of diaphragm fabrication, where single crystal silicon wafers can be reliably bonded with near perfect interfaces without the use of intermediate layers. This technique allows the making of very small sensors which find use in catheter-tip transducers for medical in vivo measurements.

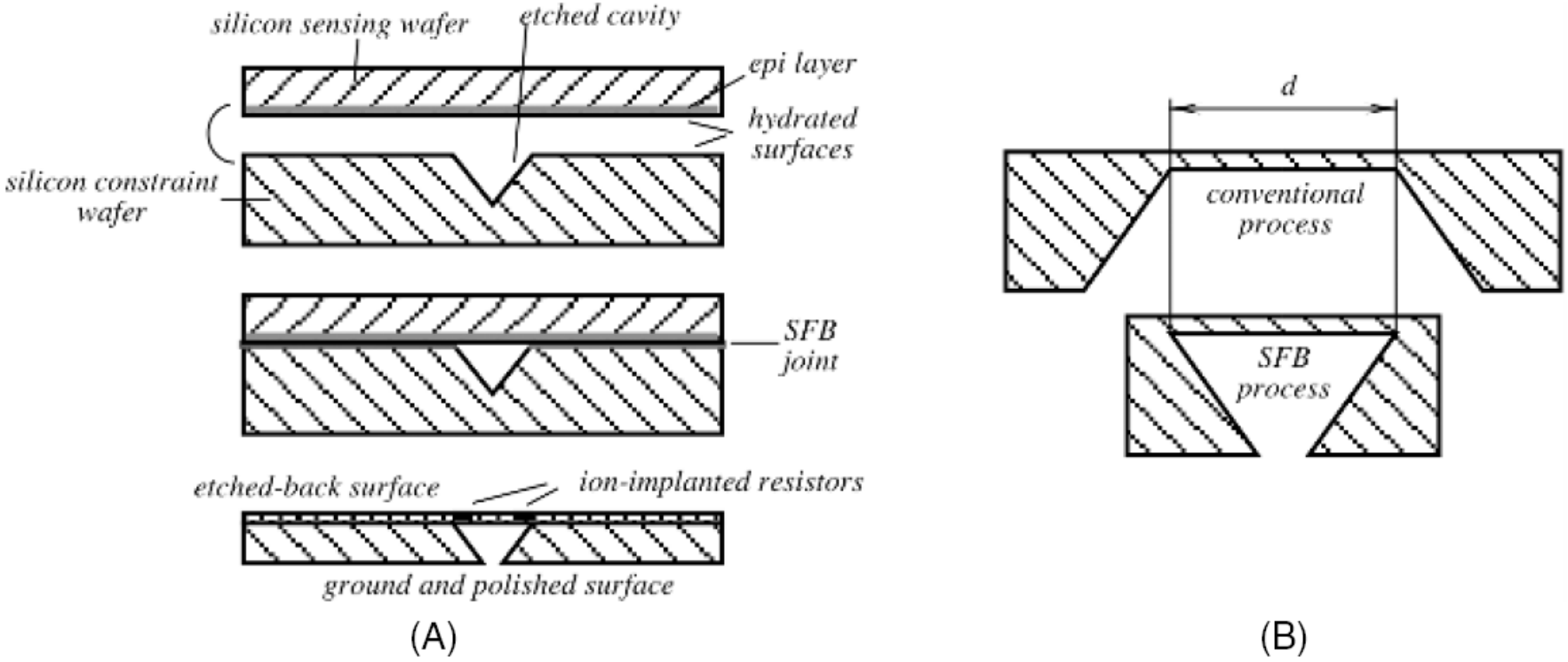


Fig. 10.6. Silicon fusion bonding method of a silicon membrane fabrications: (A) productions steps; (B) comparison of an SFB chip size with a conventionally fabricated diaphragm.

Example 5: optoelectronic pressure sensor

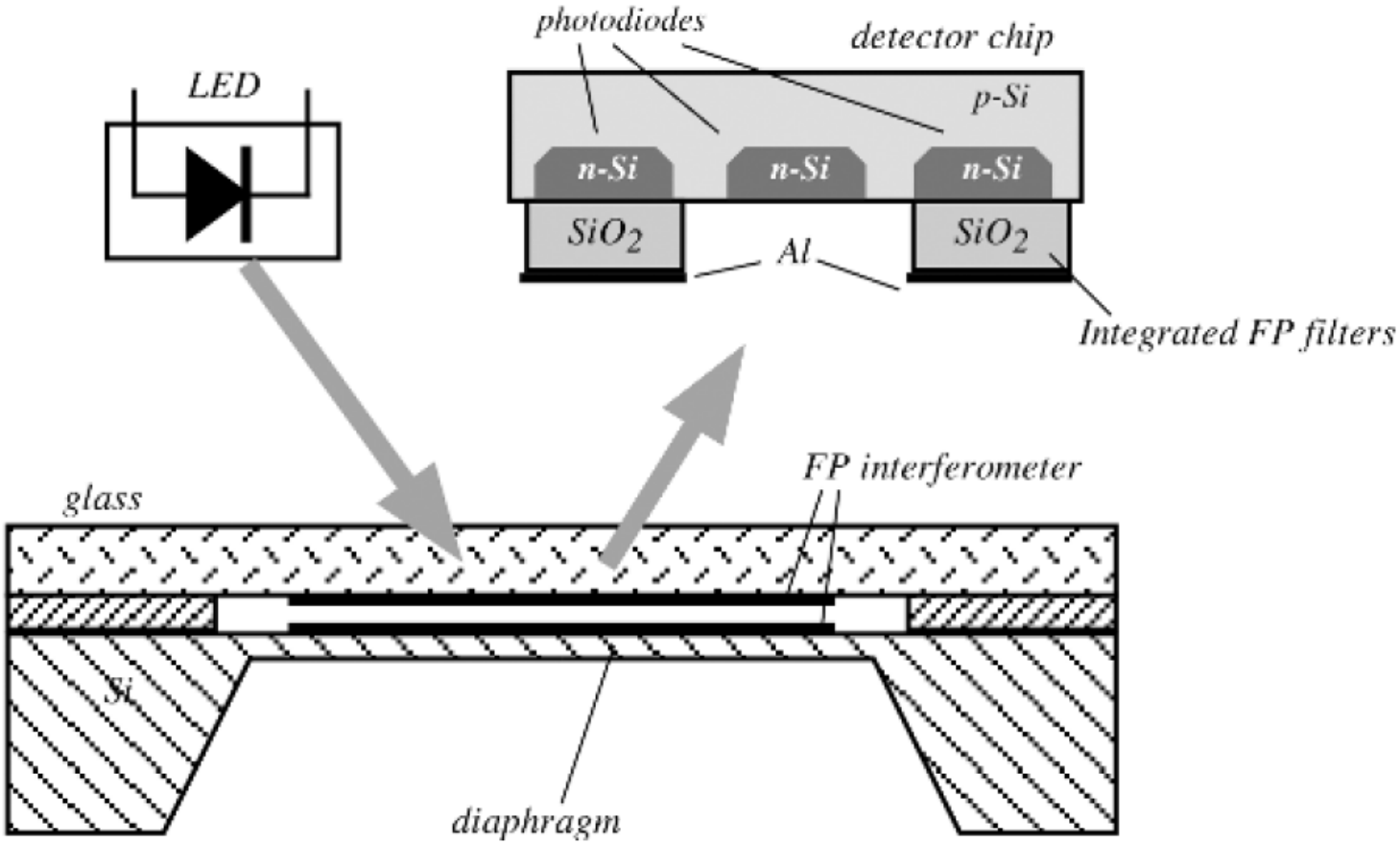


Fig. 10.13. Schematic of an optoelectronic pressure sensor operating on the interference phenomenon. (Adapted from Ref. [12].)

Example 6: gas microflow sensor

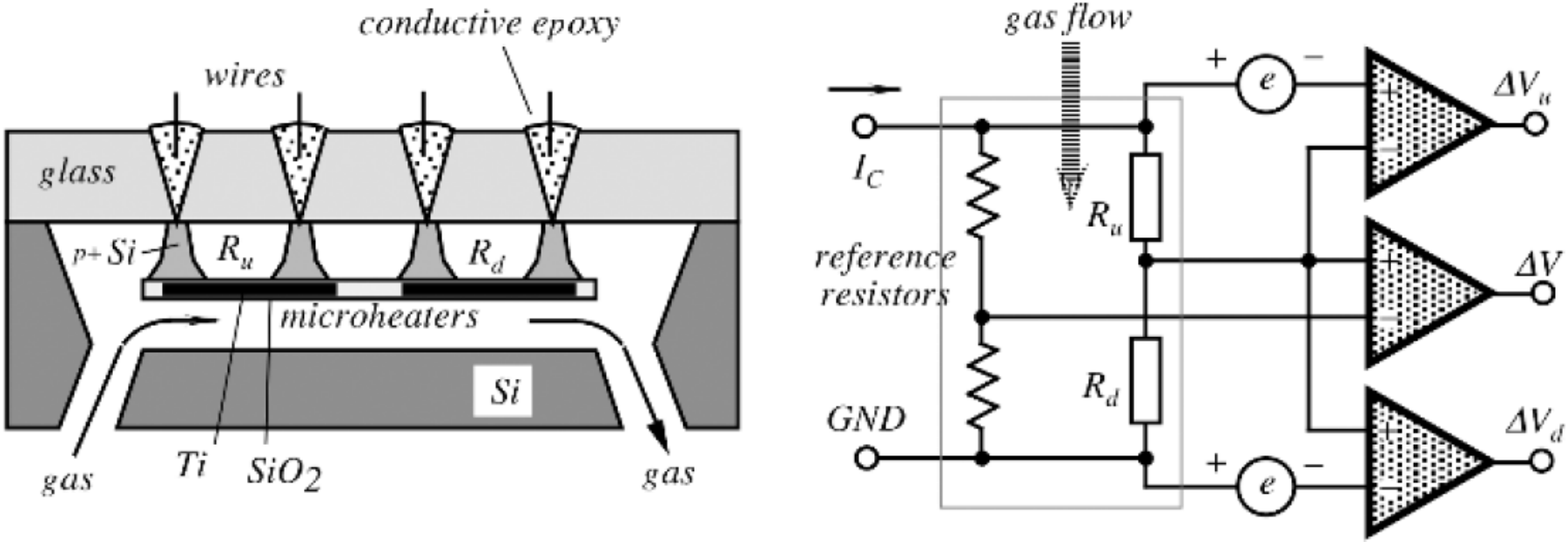


Fig. 11.13. Gas microflow sensor with self-heating titanium resistors: (A) sensor design; (B) interface circuit: R_u and R_d are resistances of the upstream and downstream heaters, respectively. (Adapted from Ref. [7].)

Example 7: gas microflow sensor with capacitive pressure sensor

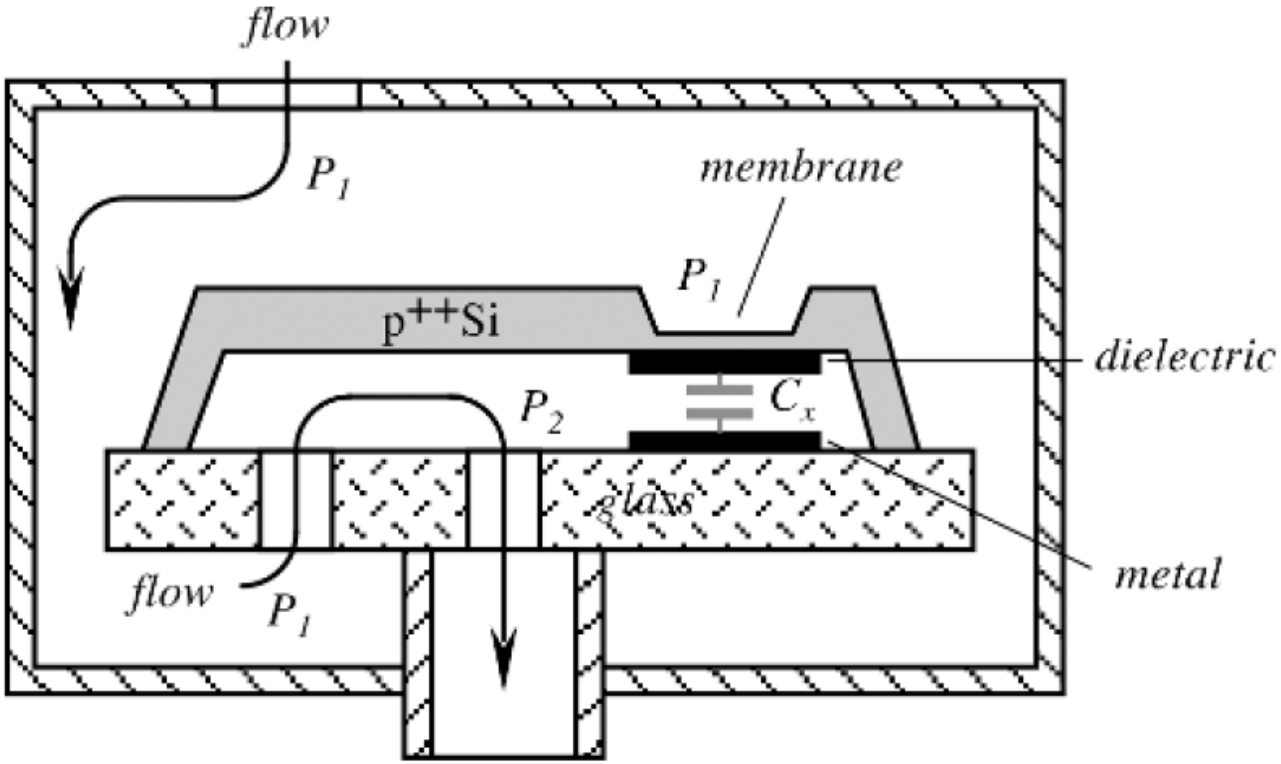


Fig. 11.14. Structure of a gas microflow sensor utilizing capacitive pressure sensor. (Adapted from Ref. [9].)

Example 8: capacitive thin humidity sensor

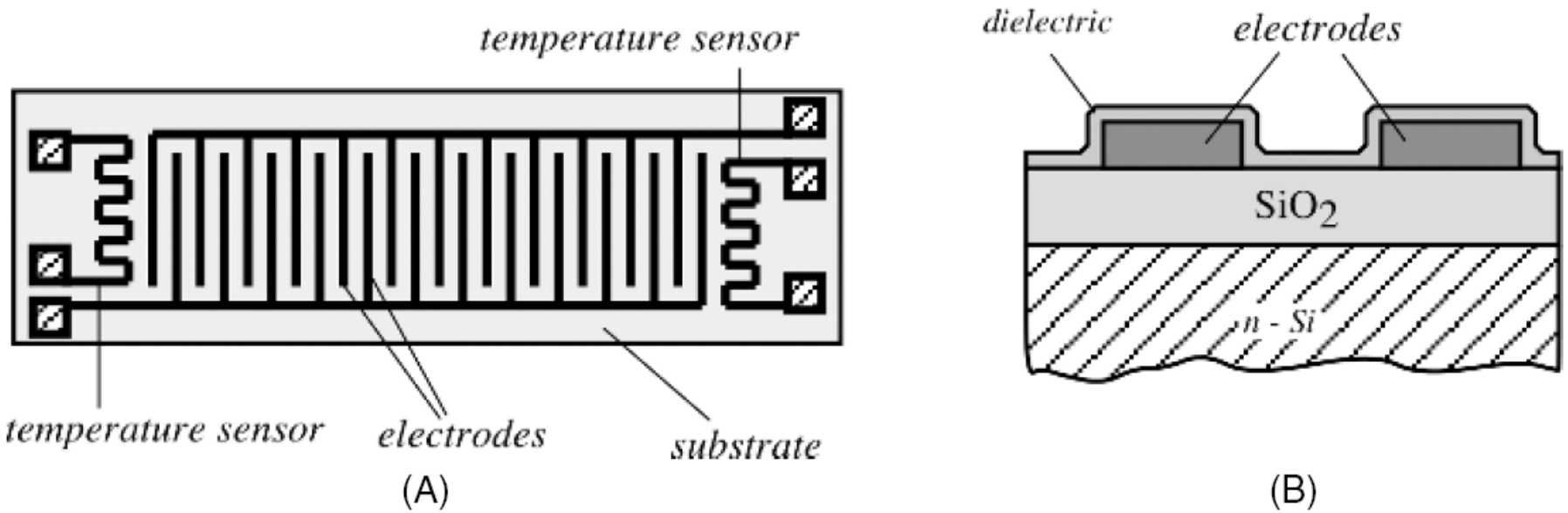


Fig. 13.4. Capacitive thin-film humidity sensor: (A) interdigitized electrodes form capacitor plates; (B) cross section of the sensor.

Example 9: photodiodes (six types)

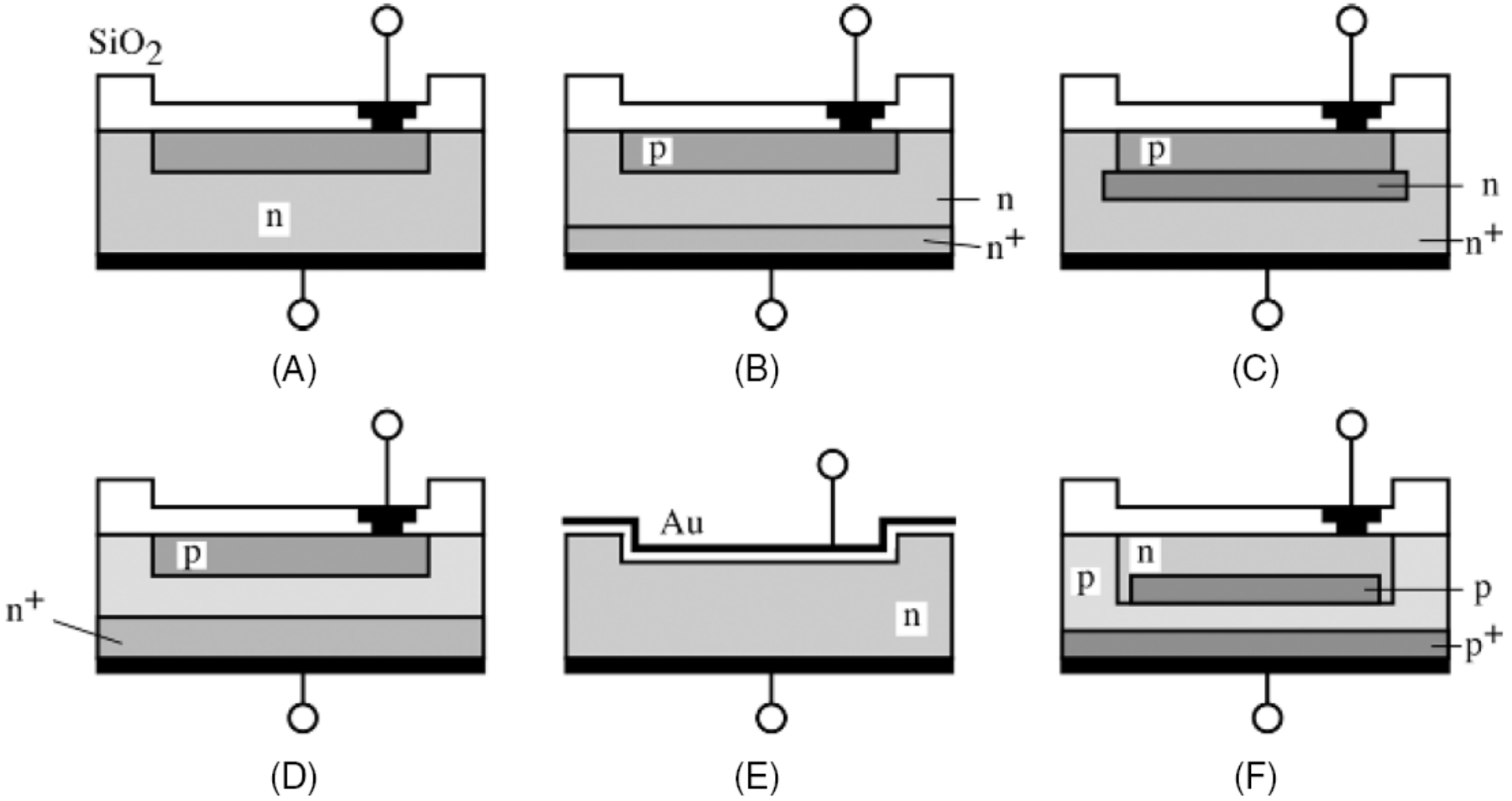


Fig. 14.6. Simplified structures of six types of photodiode.

Example 10: liquid chemFET sensor

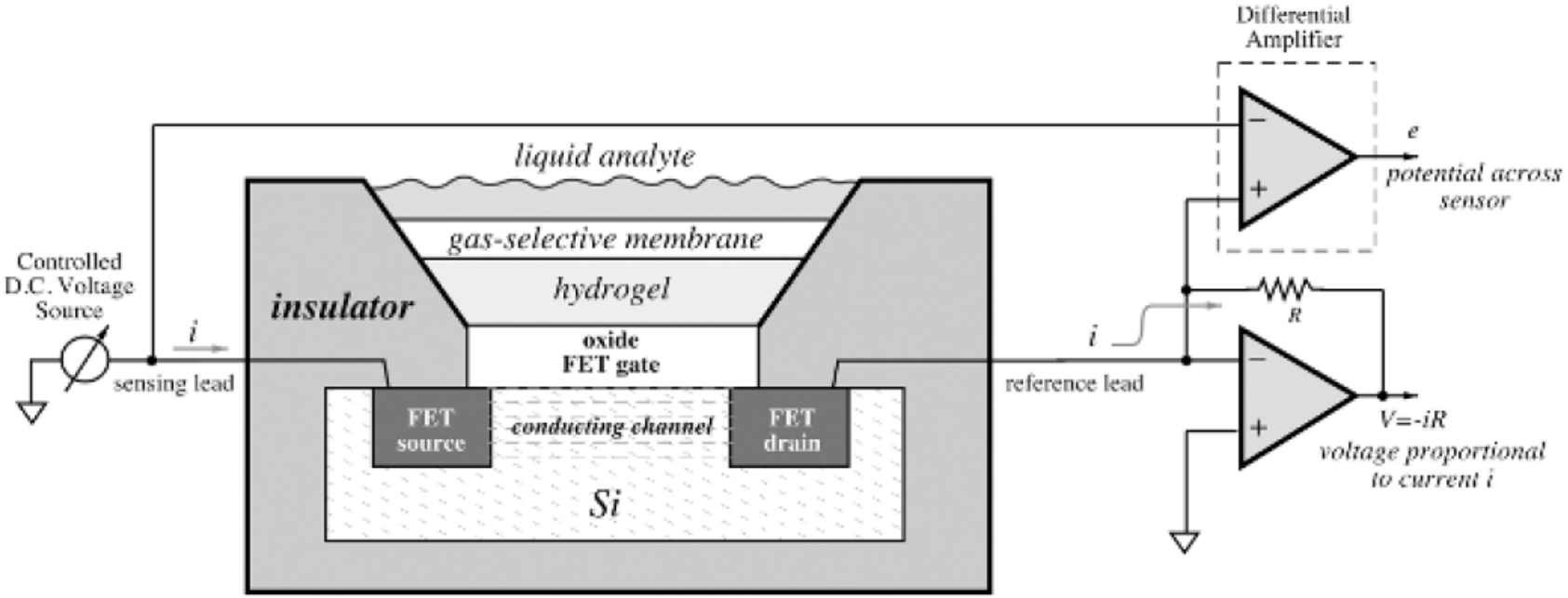


Fig. 17.5. Liquid ChemFET construction and electrical connection.

Example 11: optical CO_2 sensor

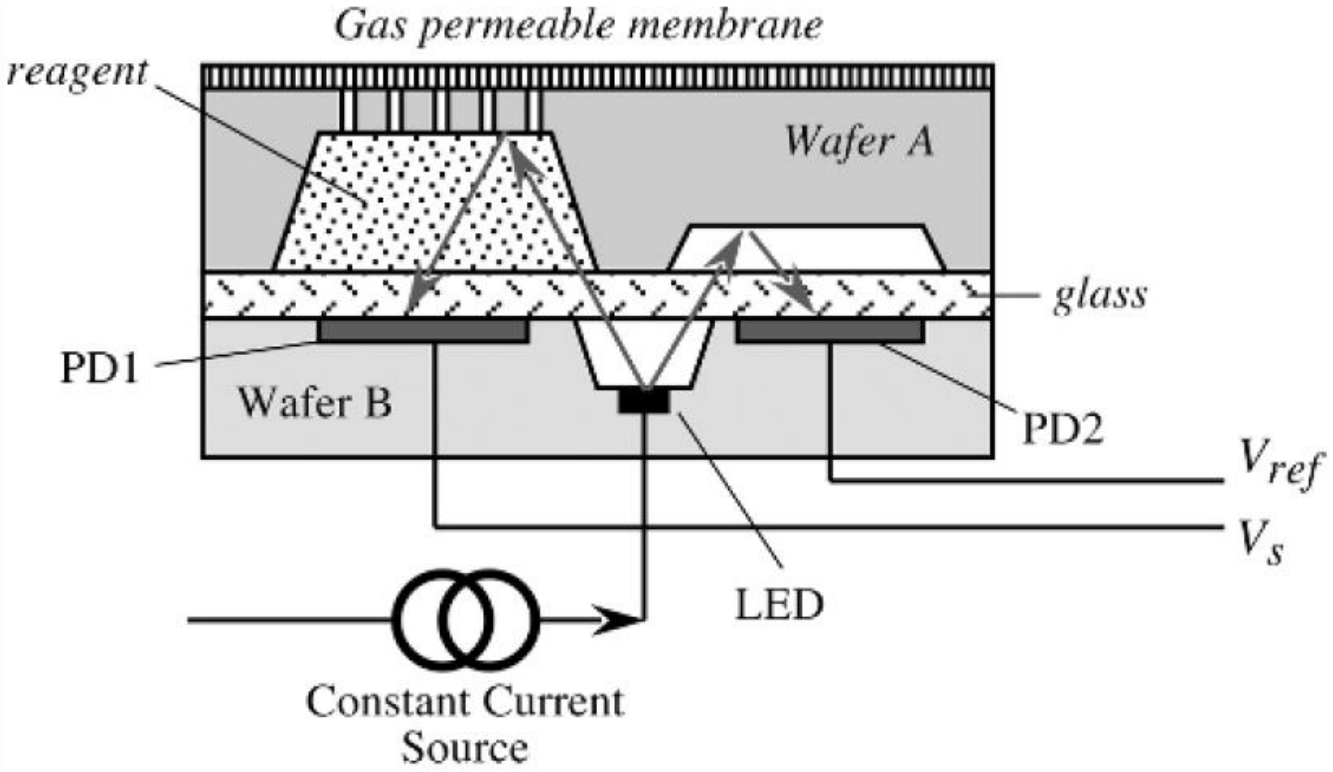


Fig. 17.12. Simplified configuration of an optical CO_2 sensor.