Addressing

Introduction

For the CPU to access RAM/ROM, the following signals must be set. Only /M1+/MReq is concerned by this paper.

/M1 + /MReq = Opcode Fetch

/M1 = 0 : Machine Cycle

/MReq = 0 : Addr bus have memory Addr

/Rd = 0 : Read

/M1 + /IOReq = Interrupt Ack (interrupt vector can be placed on data bus)

/M1 = 0 : Machine Cycle

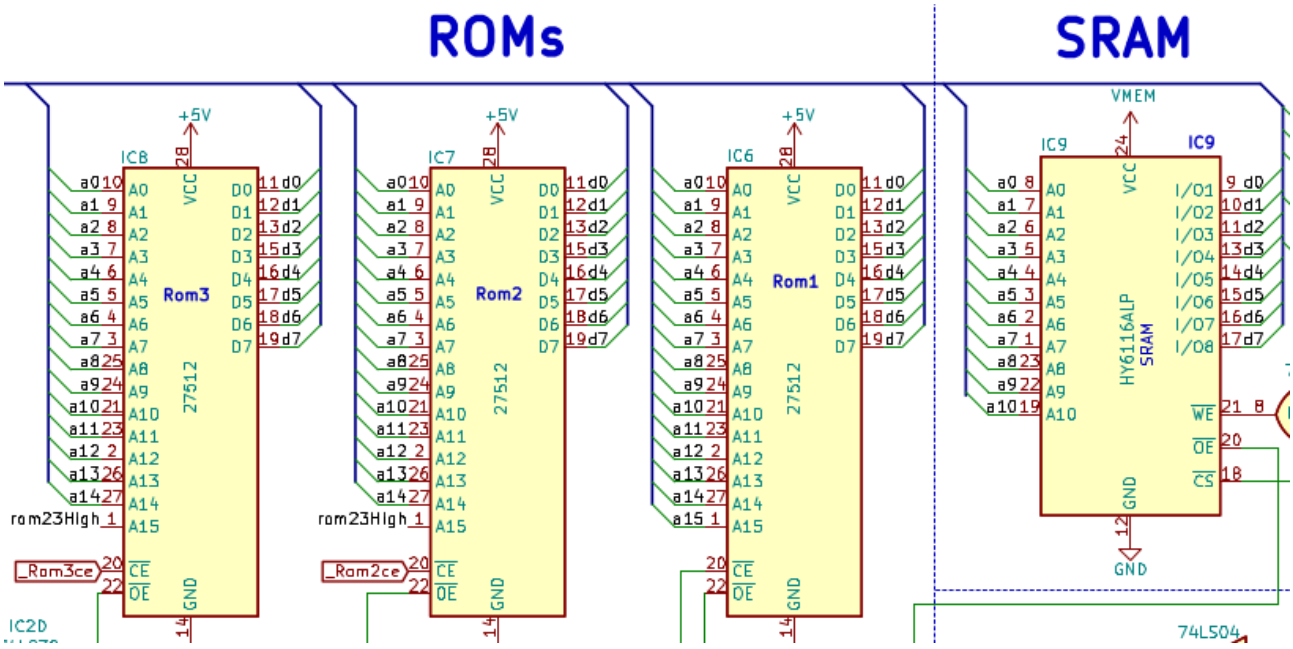
/MReq = 0 : Addr bus have IO Addr to read & write (8 bits only)

Multiple ROMs

The board feature 3x ROMs (64 Kbyte) and 1x SRAM (2 Kbyte).

The ROM1 is the default ROM to fetch opcode from 0x0000.

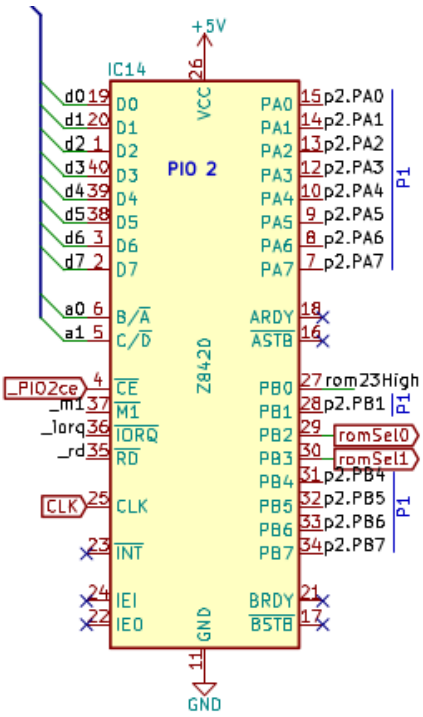
ROM1 and SRAM are available in the default address space (without selection artefact).



The ROM2 and ROM3 are selectable with the signal `romSel0` & `romSel1` combined with bits A15 & A13 on the address bus.

Signal `romSel0` & `romSel1` are handled by the PIO2 (IC14) see PB2 & PB3 outputs.

As the most significant bit (A15) is involved into extra ROM selection, it cannot be used to address higher address range on ROM2 & 3.
To workaround this limitation, the A15 bit on ROM2 & 3 is managed with signal `rom23High` from PIO2.PB0 (IC14).



Address Space

romSel1	romSel0	rom23High	From addr	To A15	To addr	Target
x	x	x	0x0000	0	0x1FFF	ROM1
x	**x**	x	0x2000	**0**	0x27FF	SRAM
x	x	x	0x2800	0	0x7FFF	ROM1
0	0	x	0x8000	1	0xFFFF	ROM1 – Higher 32K
0	1	0	0x7FFF	1	0xFFFF	ROM2 – Lower 32K.
0	1	1	0x7FFF	1	0xFFFF	ROM2 – Higher 32K.
1	0	0	0x7FFF	1	0xFFFF	ROM3 – Lower 32K
1	0	1	0x7FFF	1	0xFFFF	ROM3 – Higher 32K

ROM Selection

WHEN A15 is HIGH THEN the selected ROM depends on romSel0 & romSel1 bits

RomSel1	RomSel0	Selected ROM
0	0	ROM 1 – default ROM, A15 is acting as the most significant bit in the address space.
0	1	ROM 2 selected, ROM's A15 is managed by rom23High signal.
1	0	ROM 3 selected, ROM'sA15 is managed by rom23High signal.

ROM2 & ROM3 address selection

Lower Addr Space

When `rom23High=0` then `rom_addr = bus_addr & 0x7FFF.`

Higher Addr Space

When `rom23High=1` then `rom_addr = 0x8000 + (bus_addr & 0x7FFF).`

Generic addr calculation

```
rom_addr = (0x8000*rom23High) + (bus_addr & 0x7FFF)
```

Quick SRAM address falback (tips)

When running code from non default ROM (ROM2 or ROM3) the following signals will have following characteristics :

- A15 = 1
- romSel0 or romSel1 = 1
- rom23High may be 1 or 0

Whatever are the romSel0 or romSel1 states, **selecting a SRAM address** (0x2000-0x27FF) will jump straight into the SRAM ! (notes that A15 bit is reset in such case).

Outside of SRAM address space, reseting the A15 bit will automatically jump into the lower address of the ROM1 (default ROM).