Watchdog

Introduction

The CPU Board watch dog is based on the IRQs occuring on the board.

As long as IRQ are generated the CPU is running and manage the CTC (counter) and PIO (GPIO expander). As the CTC is properly configured then it generates IRQ signal at 30,7 Hertz (when the board is powered up and having no interface wired to port P1).

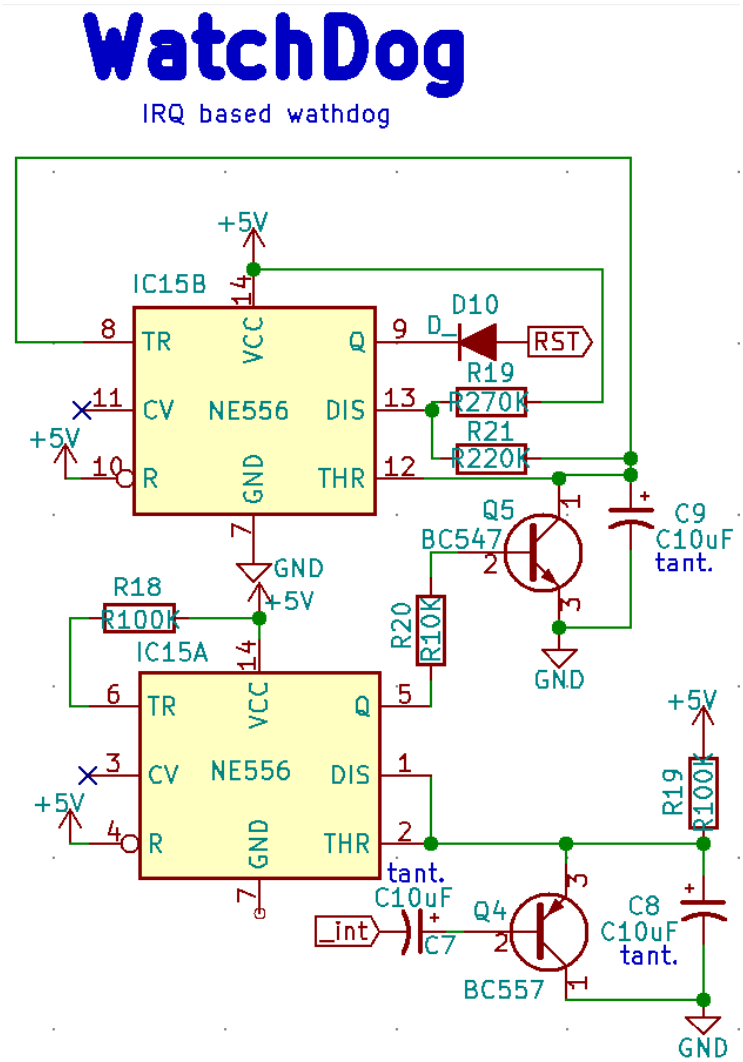
Based on oscilloscope check, each IRQ pulse have a duration of 5 to 14 µSec.

When removing the CTC then NO IRQ is generated anymore. The CTC is the initial generator of IRQ.

When not IRQ is generated, the WatchDog issue a Reset signal every after 5 seconds.

Circuitery

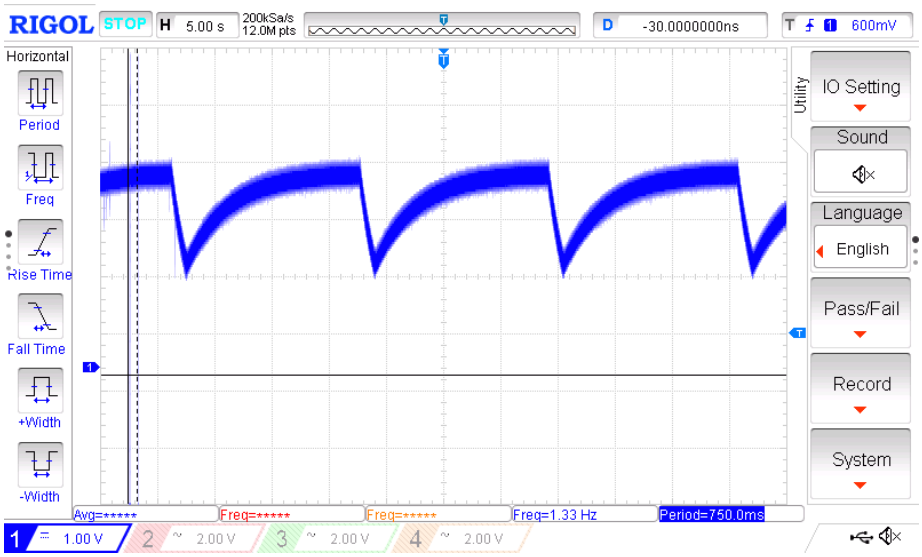
The watchdog is running with both 555 asynchronous clock encloed within a single package (so a 556).



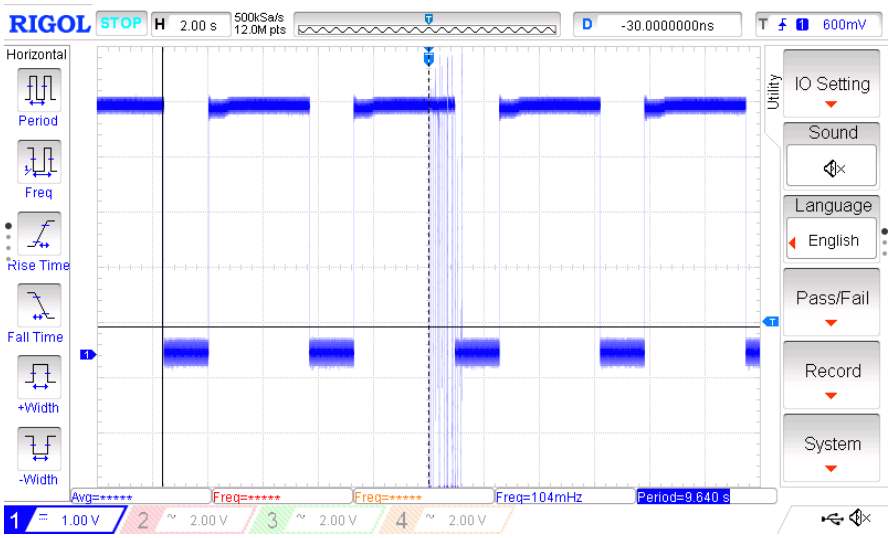
Without IRQs (CTC disconnected)

When No IRQ are generated then the watchdog should reset the board.

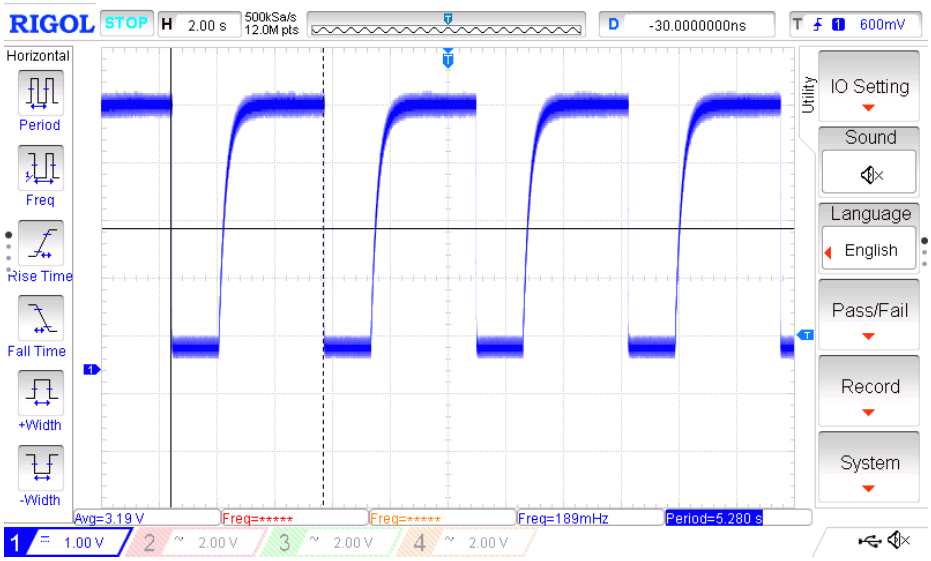
The signal on Thr @ pin12 is the following :



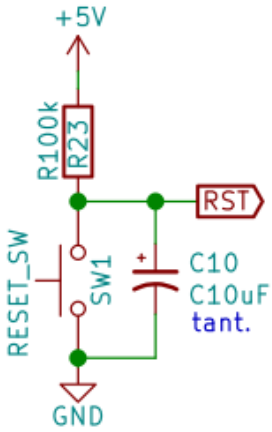
As a consequence, the Q output @ pin9 looks like the following :



When the signal is low the D10 diode get conductive. The Reset Signal is placed to the Ground which resets the Z80. The Reset make 2 seconds long. We can see that it occurs after 4 seconds without IRQ (time when the signal keeps High).



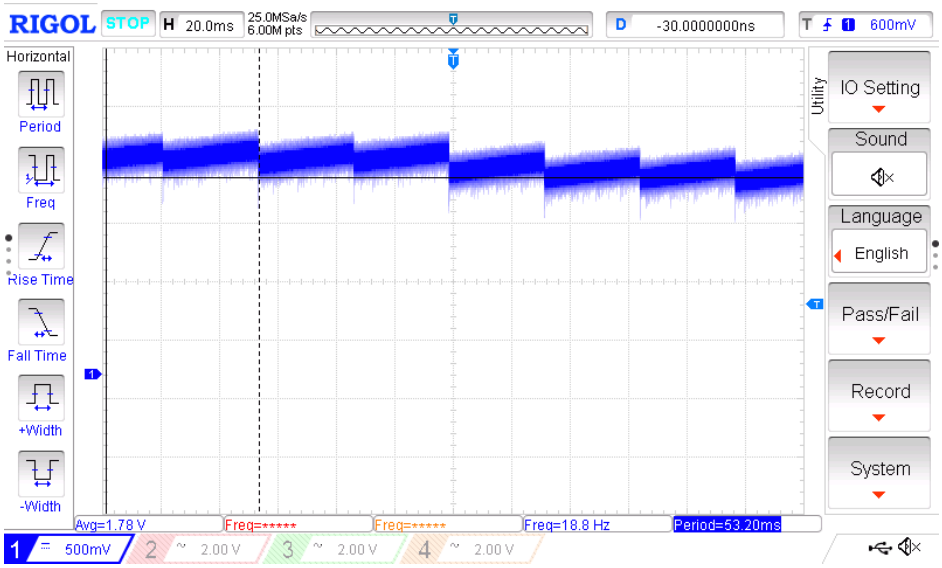
Finaly, you will see the following reset signal. The RC curve is due to the R23 & C10 making the Manual Reset circuitery (activated as soon as the D10 is no more conducting).



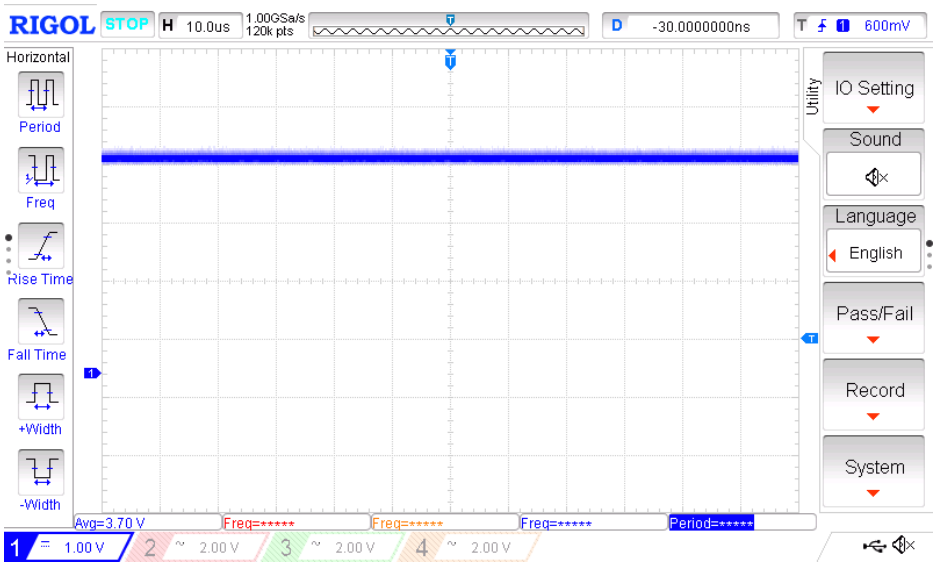
With IRQs (CTC connected)

When the CTC is initialized on the CPU board, the CTC generates 30 IRQ each seconds.
This means that watchdog is retained from sending reset signal to the CPU.

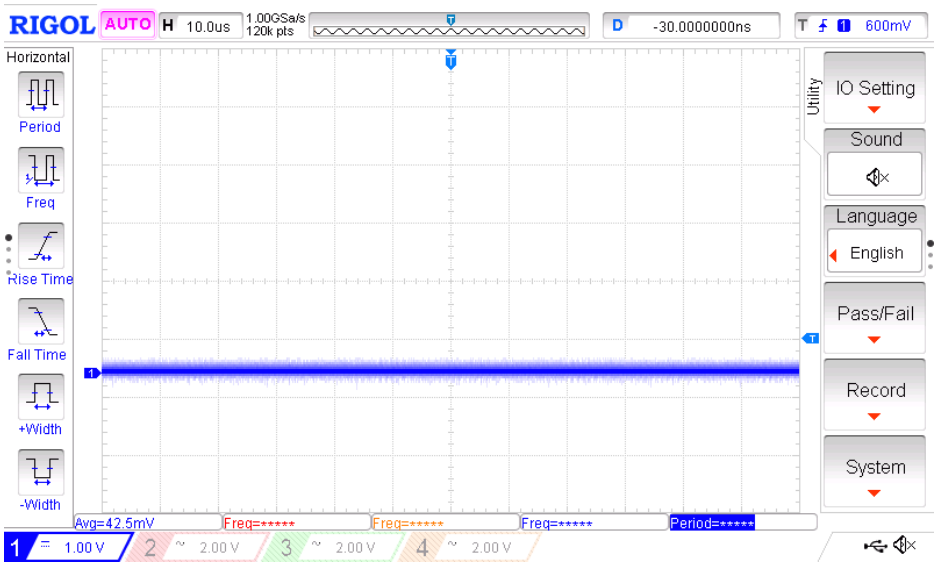
The IRQs will commute the Q4 from time to time avoiding the C8 voltage to increase toward 5V and reaching the activation threshold.
The Thr @ pin2 will look like the following (C8 voltage is maintained around 1,75V).



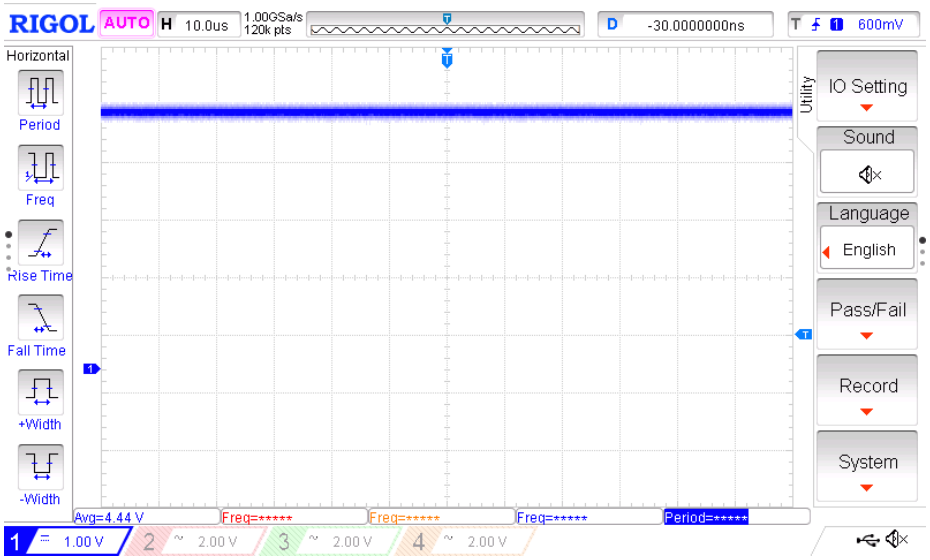
As the Timer doesn’t reach the threshold then then Q output at pin5 will stays HIGH.



As a result the threshold pin @ pin12 stays down (because Q5 is conducting).



Because the second asynchronous clock keeps its Q output @ pin9 HIGH.



As a consequence, the D10 diode will not conduct any current and Reset signal will stay HIGH.

Modifying the board

Using the board as it implies to generates a Z80 program making the CTC generating IRQ at 30 Hz minimim.

It is also possible to disable the watchdog by **removing the IC15** (NE556) at the heart of the watchdog operation. As the output Q9 is not wired (ar IC15 is removed) the RST signal cannot be sink to the ground.