I/O access

Z80 I/O access

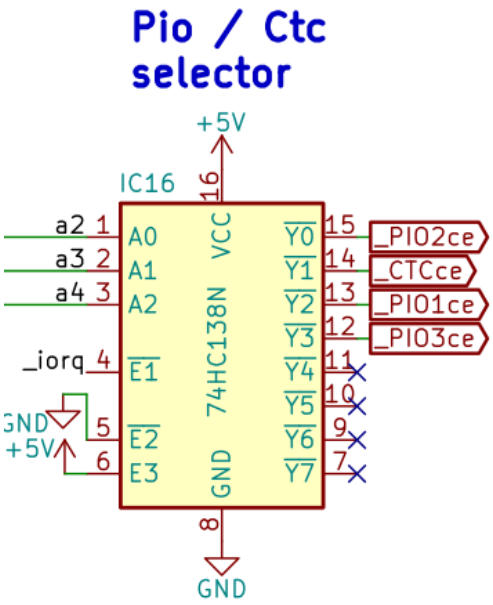
When accessing I/O device, the Z80 set the 8 lower bits on the address bus. This offers up 256 I/O register to manage external device.

When dealing an I/O access, the Z80 sets the following signals :

- /M1 = 1 : M1=0 is reserved to IRQ Ack.
- /IORQ = 0 : we made a I/O request (A0 to A7 contains the register)
- /RD = 0 : make an I/O read. Set to 1 for I/O write.

Device selection

On the original CPU board, the device is enabled with a 74HC138N.



As the 3 address bits are set on address-bus a2,a3,a4 we will have the following base address.

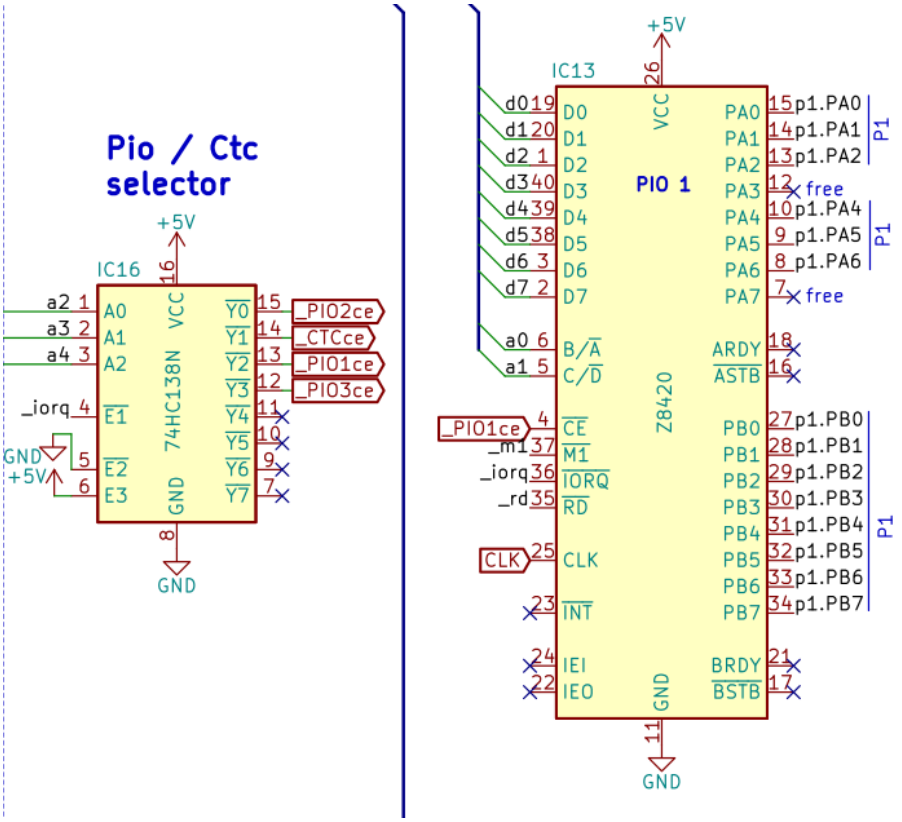
So the device address is shifted left by 2.

Bus addr.	Base address	Device
0b00000	0x00	/Y0. PIO 2
0b00100	0x04	/Y1. CTC
0b01000	0x08	/Y2. PIO 1
0b01100	0x0C	/Y3. PIO 3
0b10000	0x10	/Y4. *Not used.*
0b10100	0x14	/Y5. *Not used.*

0b11000	0x18	/Y6. *Not used.*
0b11100	0x1C	/Y7. *Not used.*

PIO Access

The /CE can be used to activate the PIO based on a selection address.



The PIO offers 4 registers selected based on signals :

- B/_A : Low for Register A, High for register B.
- C/_D : Low for **D**ata register, High for **C**ontrol register

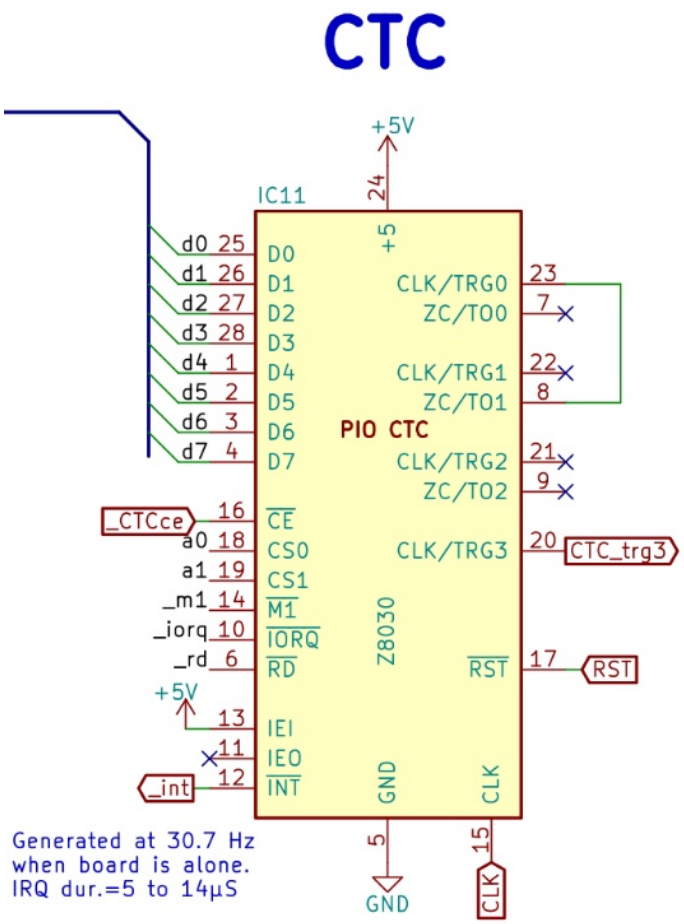
As the pins are tied to a0 & a1, the following address will allow to select registers

Reg. address	Description
+ 0	PIO Data register A
+ 1	PIO Data register B
+ 2	PIO Control register A
+ 3	PIO Control register B

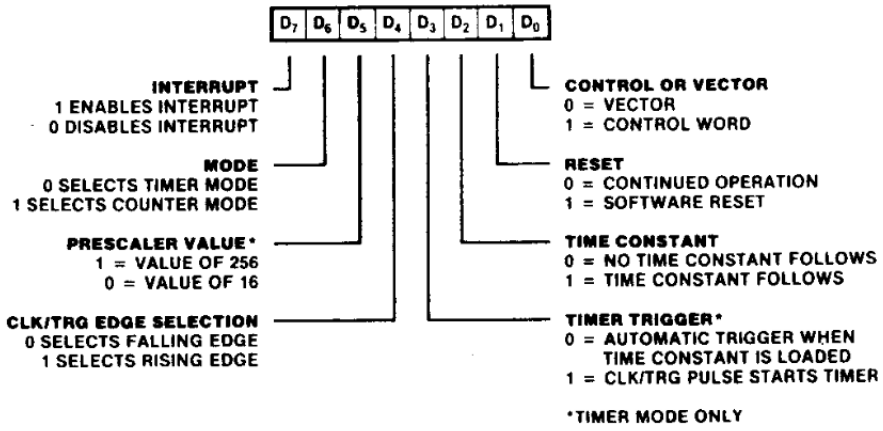
CTC Access

The /CE can be used to activate the CTC based on a selection address. From the 74HC138N, the _CTCce is enabled for the base address 0x04.

When /CE is LOW, the CTC accepts control words for one of its 4 channels.



The CTC is configured thank to the CS0 & CS1 signals which allows to select one of the 4 CTC channels (prior to send the control word over the data bus).



The CTC requires only 2 bytes of configuration (3 bytes when Interrupt is involved) to get it working.

I/O Address Summary

Here is the summary of I/O devices and register address.

Base address	Reg. address	Description
0x00		**PIO 2 on /Y0**
	0x00	Data register A
	0x01	Data register B
	0x02	Control register A
	0x03	Control register B
0x04		**CTC on /Y1**
	0x04	CTC channel 0 configuration word
	0x05	CTC channel 1 configuration word
	0x06	CTC channel 2 configuration word
	0x07	CTC channel 3 configuration word
0x08		**PIO 1 on /Y2**
	0x08	Data register A
	0x09	Data register B
	0x0A	Control register A
	0x0B	Control register B
0x0C		**PIO 3 on /Y3**
	0x0C	Data register A
	0x0D	Data register B
	0x0E	Control register A
	0x0F	Control register B