

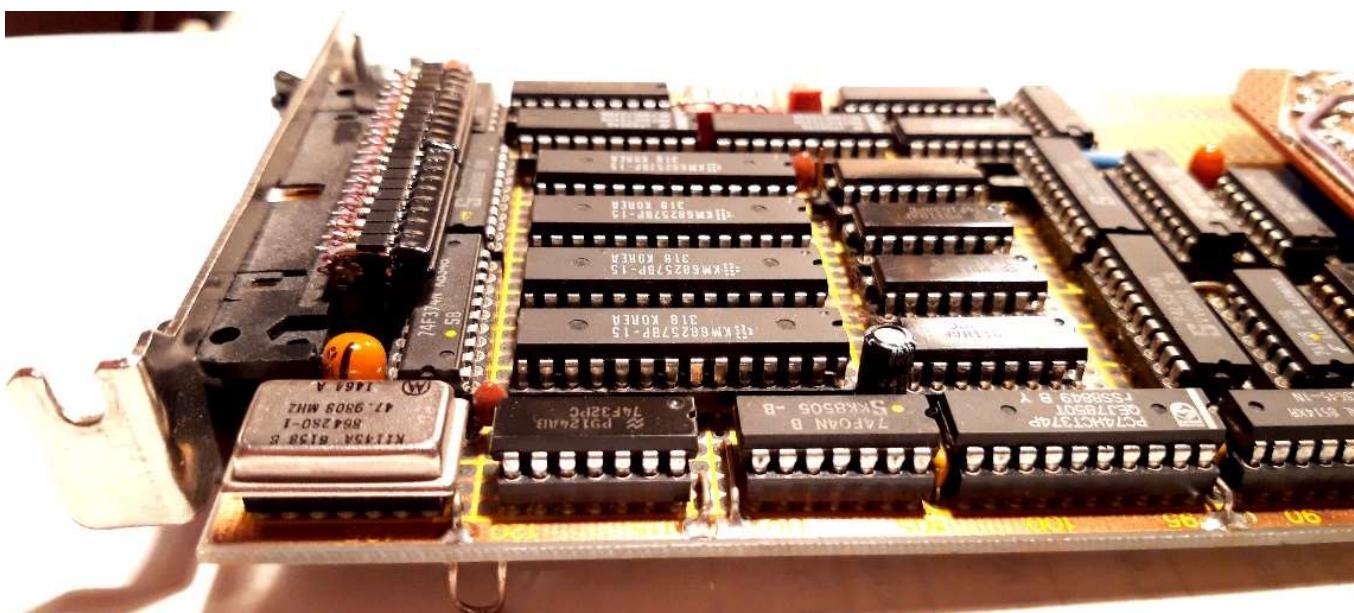
16-Bit Logik-Analyzer (for PC-AT bus)

13.04.1993

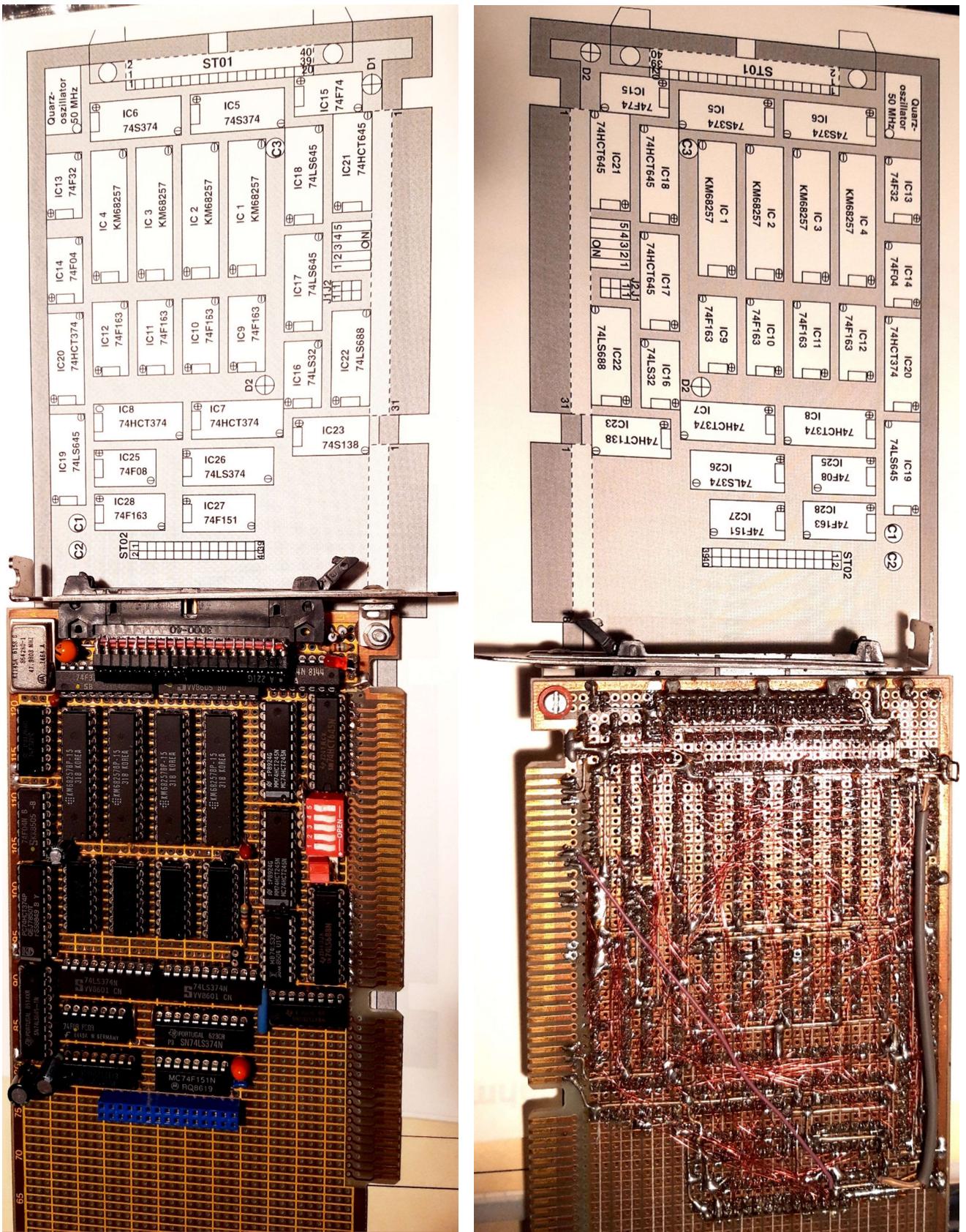
by Randolph Esser

Technical Data

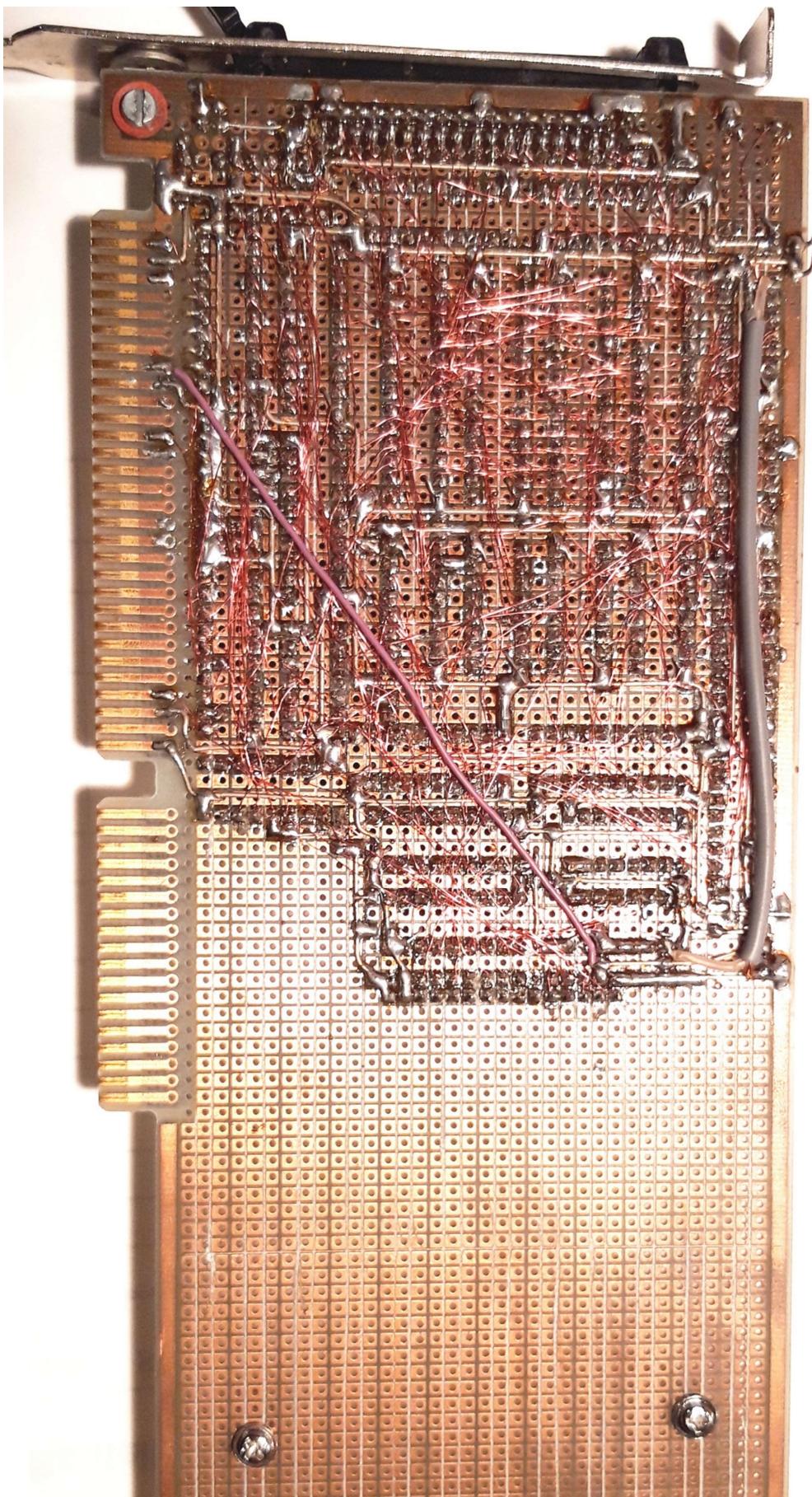
Sample Rate:	50 Mhz (options 1:1/2/4/8/16)
Cache-Buffer:	128kByte (64K x 16 Bit)
Data-Channel IN:	16 Bit
Trigger:	positiv + negativ
PC-Connector:	ISA Port-Control



LOGAN – Logikanalyser for 16 Bit/50MHz channel probes

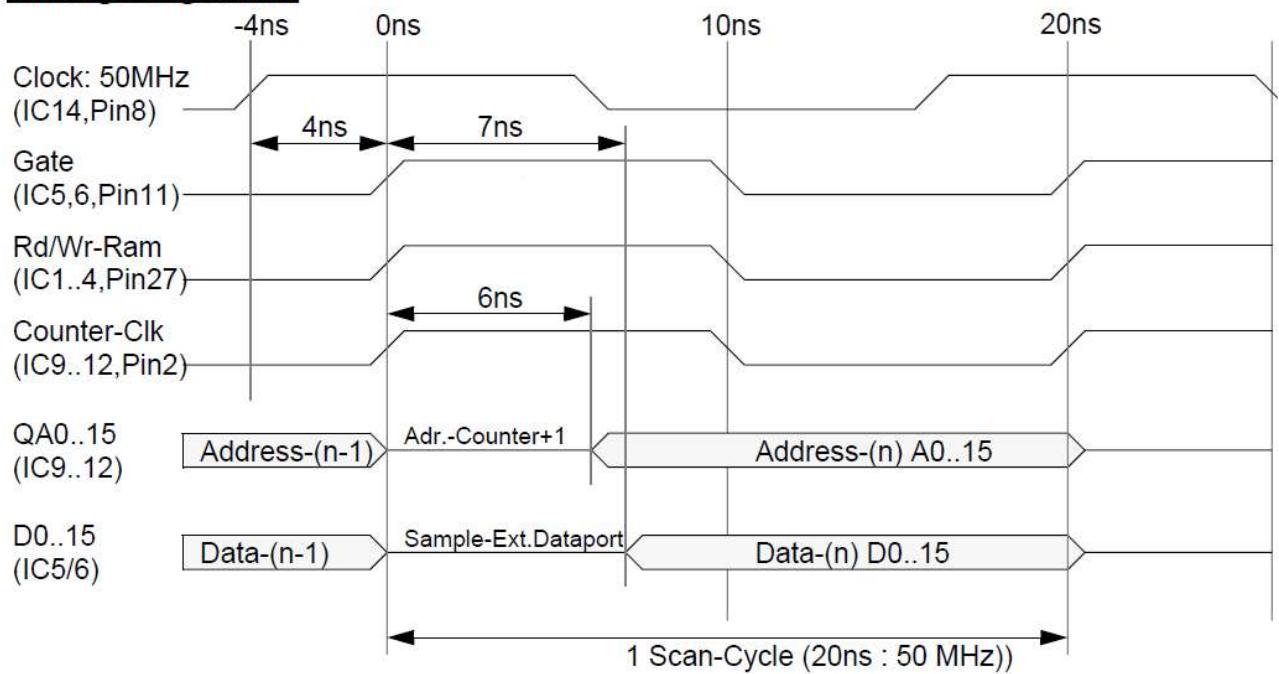


LOGAN51 - Bottom Side detailed

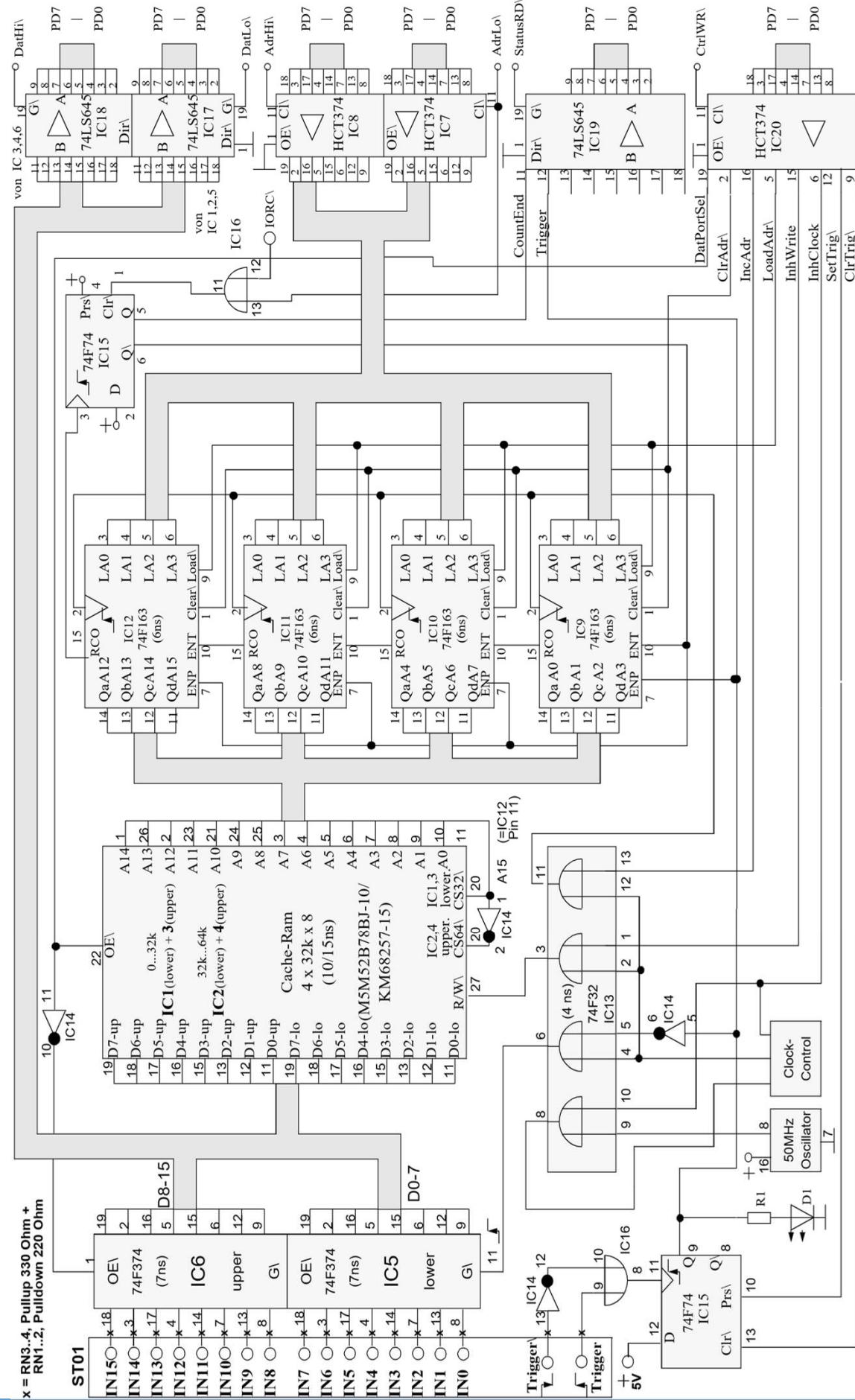


LOGAN51 – Sample Cache Protocol

Timing-Diagramm:

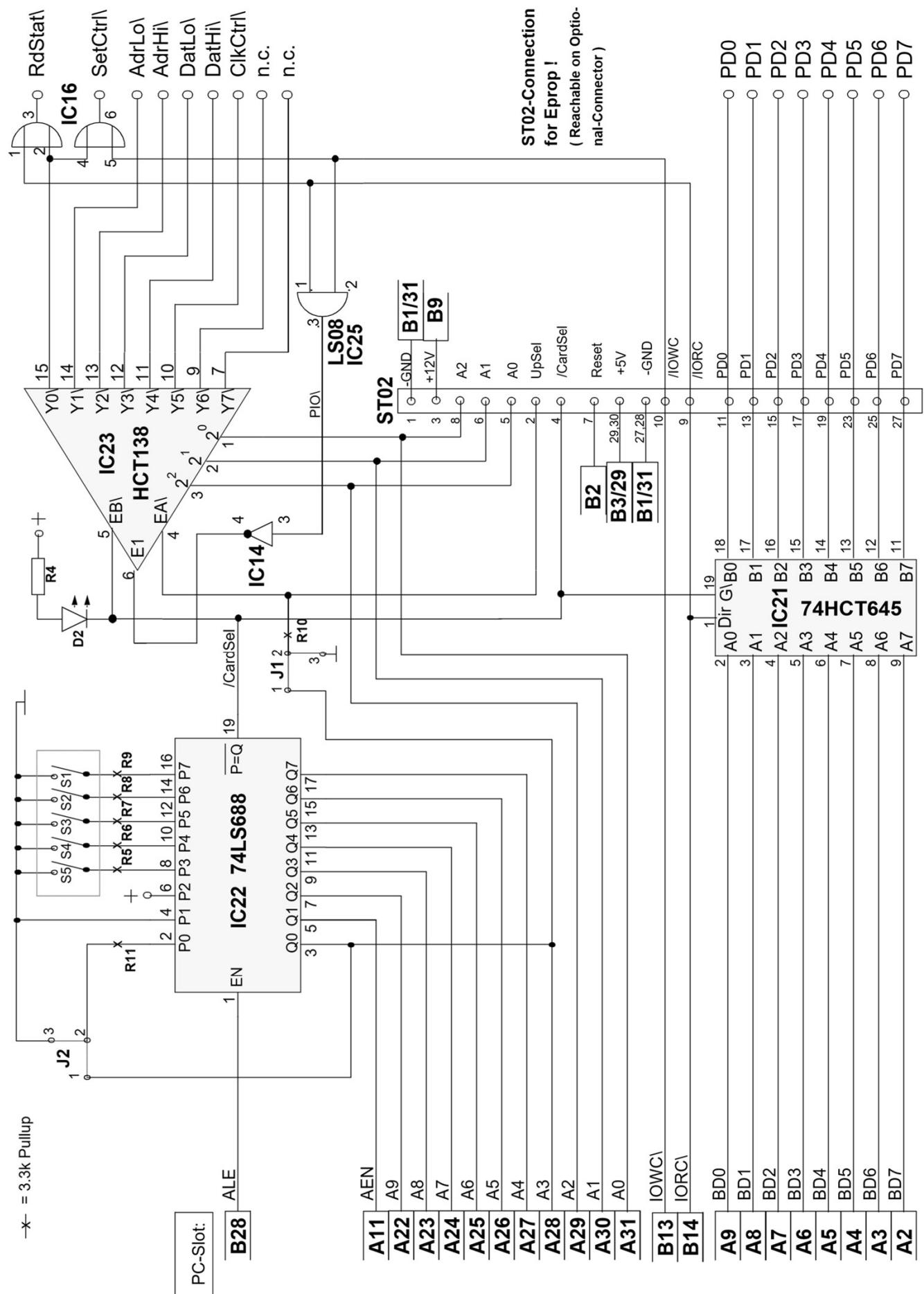


LOGAN51 Logic: PC ISA-Card -> Datenspeicherung + Steuerteil)



$\times = RN3..4$, Pullup 330 Ohm +
 $RN1..2$, Pulldown 220 Ohm

LOGAN51 - Address Decoder

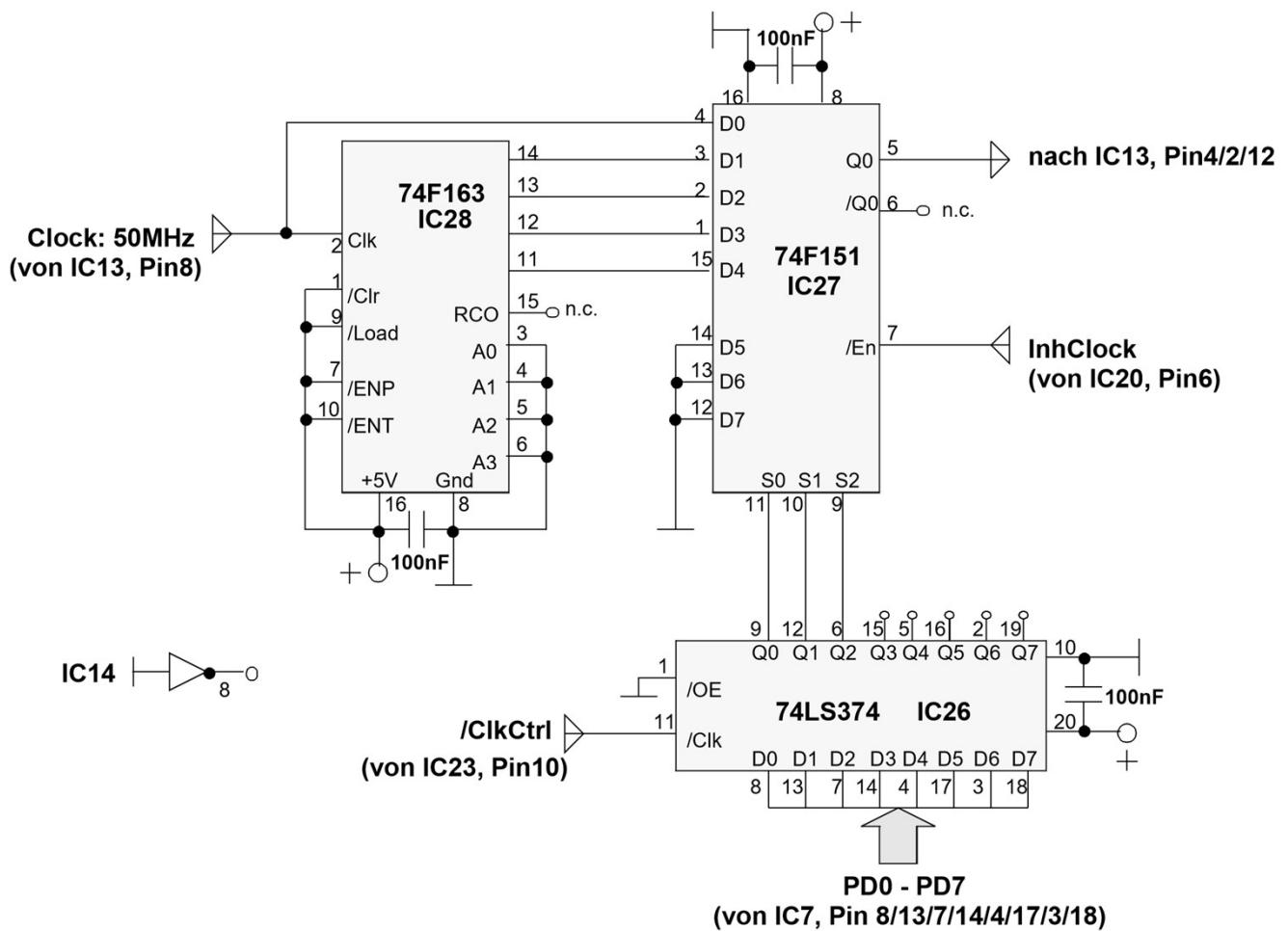


PC-Steckkarte: Clock-Control Schematics

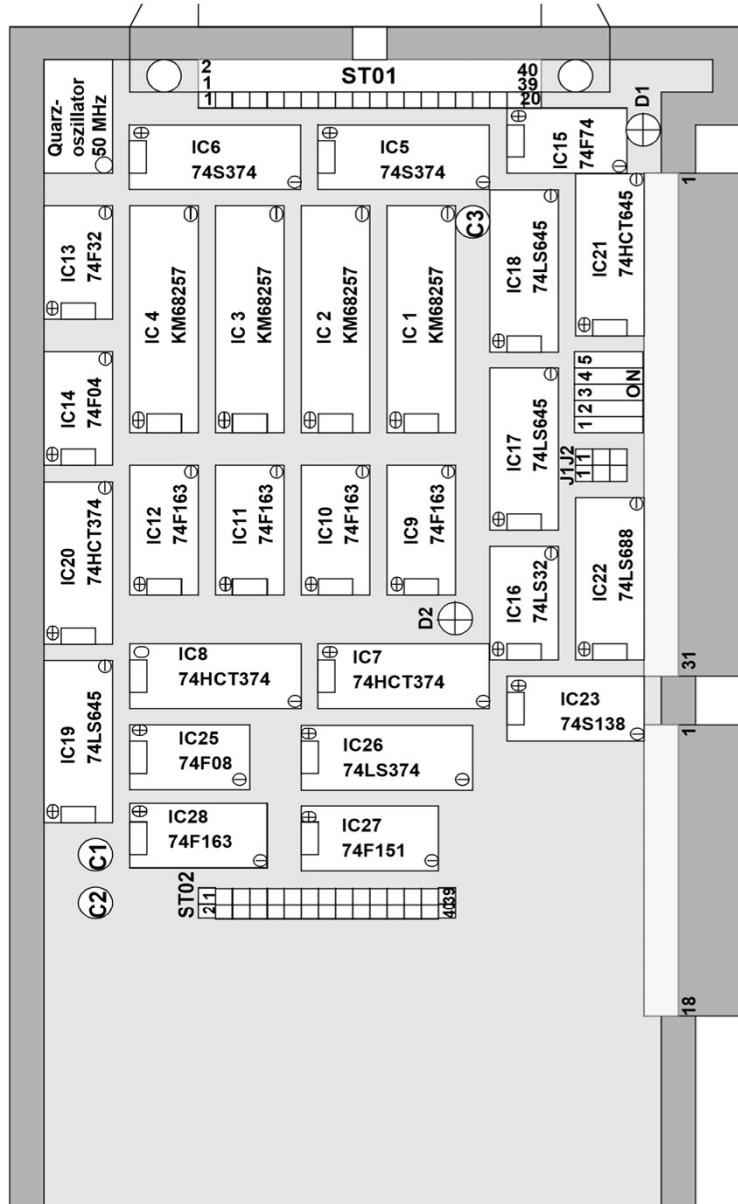
Einstellungen durch Clock-Control-Port:

Funktion:	Port:	Sample-Clock:
Clock: 48MHz/1	0	-> 48MHz
Clock: 48MHz/2	1	-> 24MHz
Clock: 48MHz/4	2	-> 12MHz
Clock: 48MHz/8	3	-> 6 MHz
Clock: 48MHz/16	4	-> 3 MHz

WR-Portadresse: IO-Base + 0x05



Board Layout- TOP Side



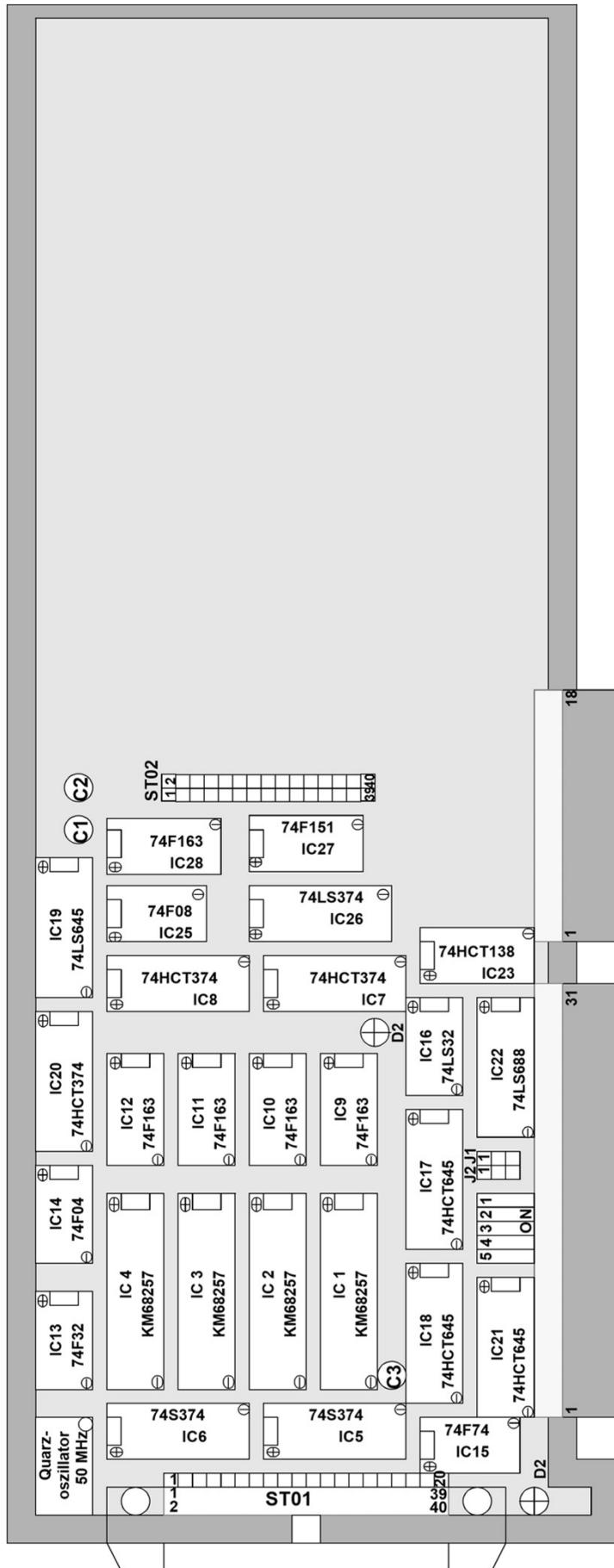
Der **Stecker ST02** ist für weitere IO-Port-Schaltungen vorgesehen, welche Piggy-Back auf die Long-Card des Logik-Analyser aufgesteckt werden können.

Dafür ist der Raum für eine vollständige Europakartenlänge von 20cm Länge und 9.5cm Breite vorgesehen.

Auf der Basiskarte sind alle Spannungen (+5V, +12V) mit mind. 50uF sowie 100nF gegen GND gepuffert. Die Basiskarte (Logik-Analyser-Teil) verbraucht statisch bei +5V 700mA. Demnach stehen der Expansionskarte noch maximal 800mA auf der +5V-Schiene zur Verfügung.



Board Layout- Bottom Side



LOGAN51 – ISA/AT Bus Port Address Selection

Tabelle 1: LOGAN51 Data Port-Addressing

Addr. Offset	Lese- Zugriff	Schreib- Zugriff	RD/WR- Selektion
+0x00	StatusRD	ControlWR	ja
+0x01	reserviert	WR-Address lower	nein
+0x02	reserviert	WR-Address upper	nein
+0x03	RD-Data lower	reserviert	nein
+0x04	RD-Data upper	reserviert	nein
+0x05	n.c.	Clock-Control	nein
+0x06	n.c.	n.c.	-
+0x07	n.c.	n.c.	-

Tabelle 2: LOGAN51 Address Base for IO-Ports at PC-AT Bus

J1 1-2	J1 2-3	J2 1-2	J2 2-3	Logan16	Expansion
				-	HI
x				-	HI
	x			-	-
		x			HI + LO
x		x		LO	HI
	x	x		HI + LO	-
			x	-	-
x			x	LO	-
	x		x	LO	-

LO = lower IO-Ports +00h - +07h

HI = higher IO-Ports +08h - +0Fh

HI + LO = beide Hälften in sich gespiegelt

,-' = keine IO-Port Zuordnung

x = Jumper gesetzt

LOGAN51 - Port Address Selection

Tabelle 3: Probe I/O-Kartenstecker ST01 (40pol. AWG-Leiste)

Stift-Nr	Funktion	Stift-Nr	Funktion
1	+5V	2	Anal.-IN 0 (opt.)
3	Data-IN 15	4	Ground
5	Data-IN 14	6	Ground
7	Data-IN 13	8	Ground
9	Data-IN 12	10	Ground
11	Data-IN 11	12	Ground
13	Data-IN 10	14	Ground
15	Data-IN 9	16	Ground
17	Data-IN 8	18	Ground
19	Data-IN 7	20	Ground
21	Data-IN 6	22	Ground
23	Data-IN 5	24	Ground
25	Data-IN 4	26	Ground
27	Data-IN 3	28	Ground
29	Data-IN 2	30	Ground
31	Data-IN 1	32	Ground
33	Data-IN 0	34	Ground
35	Trigger \	36	Ground
37	Trigger	38	Ground
39	+5V	40	Anal.-In1 (opt.)

Tabelle 4: Expansion-Connector ST02" (Steckkarten-Mitte, 30 pol. Buchsenleiste)

Stift-Nr	Funktion	Stift-Nr.	Funktion
1	GND	2	UpSel
3	+12V	4	/CardSel
5	A0	6	A1
7	Reset	8	A2
9	/IORC	10	/IOWC
11	IO-Data PD0	12	reserved
13	IO-Data PD1	14	reserved
15	IO-Data PD2	16	reserved
17	IO-Data PD3	18	reserved
19	IO-Data PD4	20	reserved
21	IO-Data PD5	22	reserved
23	IO-Data PD6	24	reserved
25	IO-Data PD7	26	reserved
27	GND	28	GND
29	+5V	30	+5V

Parts List: LOGAN51 - Board (for 16-Bit channel)

Bauteil #	Stückzahl	Bezeichnung	Funktion	Sockel-Pinning
IC1...4	4	KM68257 / M5M52B78	Scan-cache-Ram 10ns : 50MHz (128kB; TTL-compatible) 15ns : 33 MHz	DIP-28 (schmal)
IC5...6	2	74F374	Dig. Sample & Hold for Ext. Dataport (F/S)	DIP-20
IC7...8	2	74HCT374	up. + low. Addressport for IO-Ctrl. (HCT/LS)	DIP-20
IC9...12	4	74F163	Address-counter for Scan-Ram	DIP-16
IC13	1	74F32	Clock-Delay-Control	DIP-14
IC14	1	74F04	6 x Inverter (F/S/AS)	DIP-14
IC15	1	74F74	a) Trigger-FF b) Count-End-FF (F/S/AS)	DIP-14
IC16	1	74LS32	4 x OR (LS/HCT/ALS)	DIP-14
IC17...18	2	74HCT645	up. + low. Dataport for IO-Ctrl. (HCT/LS; 245)	DIP-20
IC19	1	74LS645	Status-Register (HCT/LS/ALS; 245)	DIP-20
IC20	1	74HCT374	IO-Ctrl-Port (HCT/LS/ALS)	DIP-20
IC21	1	74HCT645	Central Dataport to AT-Bus (HCT/LS/ALS)	DIP-20
IC22	1	74LS688	Address-compare for IO-Ctrl (LS/HCT/ALS)	DIP-20
IC23	1	74HCT138	IO-Ctrl-Register-selector for Scan-HW (HCT/LS)	DIP-16
IC24	(1)	74HCT138	IO-Ctrl-Register-selector (optional) (HCT/LS)	DIP-16
IC25	1	74LS08	4 x AND (LS/ALS/HCT)	DIP-14
IC26	1	74LS374	Clock-Control-Register	DIP-20
IC27	1	74F151	Clock Frequency Demultiplexer 1:1/2/4/8/16	DIP-16
IC28	1	74F163	4-Bit-Binär-Counter; divide by 1:2/4/8/16	DIP-16
J1...2	2	Jumper-3	Jumper for IO-Register-Paging-Ctrl	1-2-3
S1...5	1	5x-Dip-SW	Switches for Card-base-Address-selection	DIP-10
D1...2	2	LED (3mm)	D1: Trigger-Select D2: Port-Select	2 Pin
C4..34	30	100nF Mini	IC-Koppelkondensator im Sockel, Keramik	standing
C1..3	3	47uF/25V	Stabilisierung für 5V + 12V an Expans.Con.ST02	stehend
R1, R4	2	R560/ 1/4W	Driver-Resistant for D1/2	standing
R5...9	5	3.3k/ 1/4W	Pull-Up for Dip-Switch S1...5	standing
R10	1	3.3k/ 1/4W	pull-Up for Jumper J1	standing
RN1..2	2	8 x 220Ohm	8+1 R-Array gekoppelt, Abschluß für Flachband	8R+1C
RN3..4	2	8 x 330Ohm	8+1 R-Array gekoppelt, Abschluß für Flachband	8R+1C
ST01	1	40 pol.Stick	Ext. AWG-Leiste für Scan- und Trigger-Anschluß	Printm.90°
ST02	1	30pol.AWG	Optional-Connector for Card-Expansion (Eprop)	steh. Buchse
Board	1	AT-Bus	16-bit AT-Bus-Card (short-Type) (9,5 x 31cm)	16-bit

Probe51 – for 8031/51 CPU - Layout -> Top Side

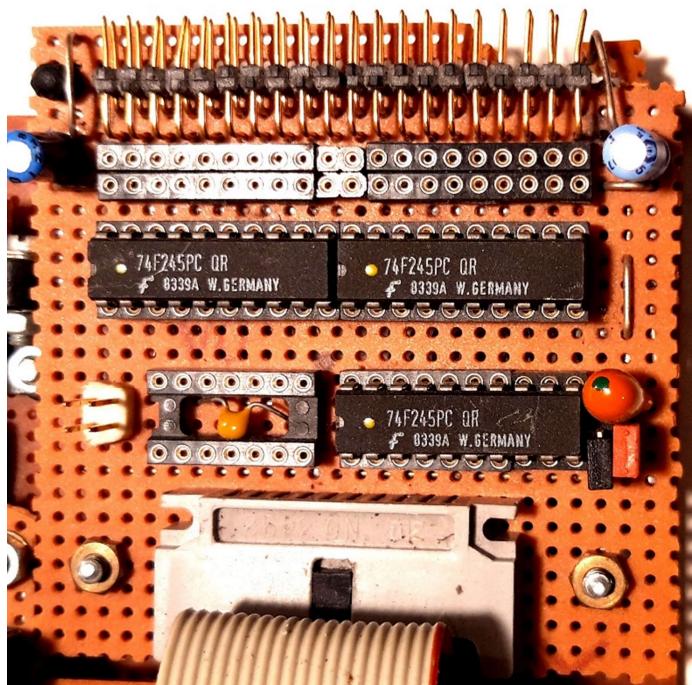
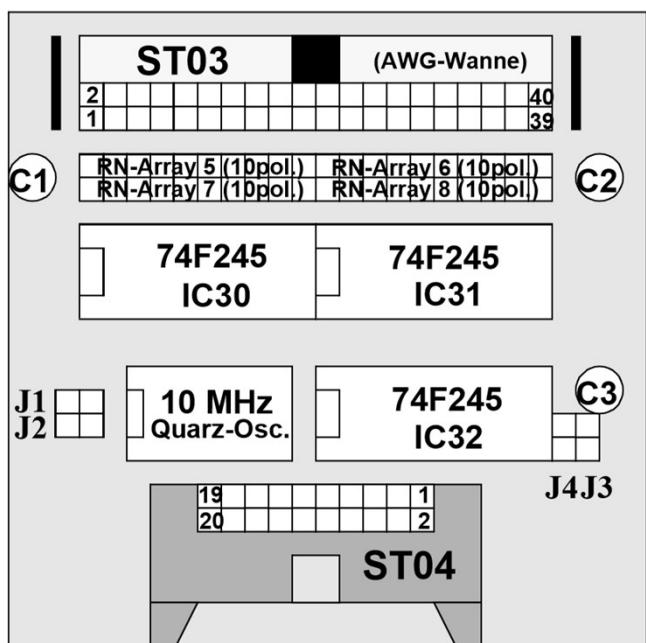


Tabelle 5: Generic Probe-Connector ST04
(Probe-Anschluss, 20 pol. AWG-Stecker)

PIN	Funktion
1	GND
2	GND
3	Trigger 0
4	/Trigger 1
5	Probe 0
6	Probe 1
7	Probe 2
8	Probe 3
9	Probe 4
10	Probe 5
11	Probe 6
12	Probe 7
13	Probe 8
14	Probe 9
15	Probe 10
16	Probe 11
17	Probe 12
18	Probe 13
19	Probe 14
20	Probe 15

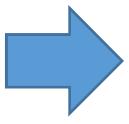
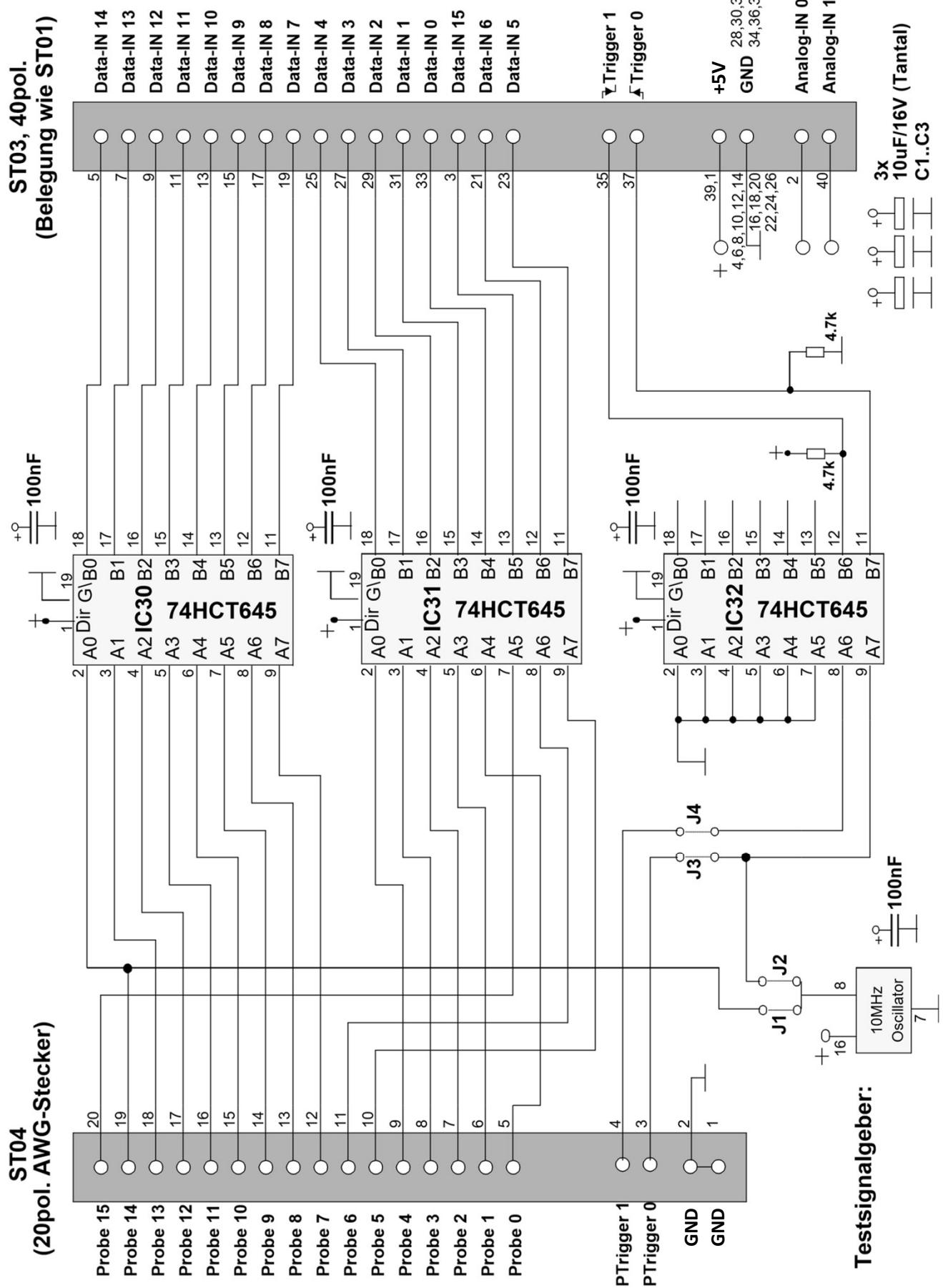


Tabelle 6: MON51 Probe-Connector ST04
(Port-Interpretation for M8051-CPU-Socket)

PIN	ST04-Line	M8051-Socket	IC-Pin
1	GND	Vss	20
2	GND	Vss	20
3	Trigger 0	/Int 0	12
4	/Trigger 1	Reset	9
5	Probe 0	/RD (P3.7)	17
6	Probe 1	/WR (P3.6)	16
7	Probe 2	A8 (P2.0)	21
8	Probe 3	A9 (P2.1)	22
9	Probe 4	A10 (P2.2)	23
10	Probe 5	A15 (P2.7)	28
11	Probe 6	/PSEN	29
12	Probe 7	ALE	30
13	Probe 8	A/D7	32
14	Probe 9	A/D6	33
15	Probe 10	A/D5	34
16	Probe 11	A/D4	35
17	Probe 12	A/D3	36
18	Probe 13	A/D2	37
19	Probe 14	A/D1	38
20	Probe 15	A/D0	39

Prob51 – Probe for 8031/51 -> Data channel driver



Probe51 - Parts List:

Bauteil #	Stückzahl	Bezeichnung	Funktion	Sockel-Pinning
IC30..32	3	74F245	Flachband-Driver of Scan/Trigger-Lines	Dip 20
Quarz	1	10MHz	Test-Signalgenerator, on D14 and Trigger 0	Dip 14
J1..4	4	Jumper	each 2-Sticks + Jumper, Trigger-Connection	standing1x2
C1..3	3	10uF/16V	Coupling-Condensator (Tantal), Stabilization	standing
C4..7	4	100nF/Cer.	IC-Block-Condensator inside the IC-socket, Mini	standing
ST03	1	40pol.AWG	40pol. AWG-Stick-Connector, Lines to PC-side	90° print
ST04	1	20pol.AWG	20pol. AWG-Stick-Connector, Probe-side	90° print
RN1..2	2	8x220Ohm	8+1 R-Array coupled, Flachband-Abschluss, optional	8 + 1 stand.
RN3..4	2	8x330Ohm	8+1 R-Array coupled, Flatcable-Ending, optional	8+1 stand.
PC-Cable	1	1.5m/40pol.	Twisted-Pair parallel-Flatcable, Z=100Ohm	40-pol/ 2 x drilled
Con01/3	2	40pol.AWG	Connector 40-pol., for ST03/ST01	Buchse 40pol.
Con04	1	20pol.AWG	Connector 20pol., for Probe-connection	Buchse 20pol.
Probe51	1	IC-Socket	8051-IC-Socket (leer) + Flatcable for Probe connection	DIP 40
Probe Board	1	Board 7x7	Probe-board (7x7cm) + Coverbox	Print 0,24mm