CPEN 311: Digital Systems Design

On-Chip In-System Debug

(only useful if you have DE1-SoC board)

1

Debugging large designs using simulation:

Simulation can be A BILLION TIMES slower than real chip execution

Suppose our design contains a processor which will run Windows.
- Just to boot Windows would require 3,000 years in simulation!
- The Romans would have had to start it running…. and it still wouldn't be done!

It is *impossible* to cover **all** operations in simulation

2

Intel Pentium 4 Verification/Validation[1]:

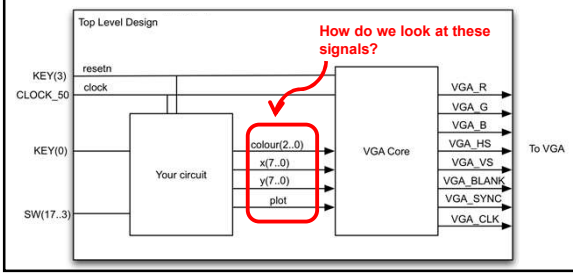
- 6,000 CPUs, running simulations, 24/7 for 2 years
  - produced less than 1 minute of real-time operation
- 60 person-year formal verification effort
  - found ~20 high-quality bugs
- $2^{10,441}$ distinct configurations in a "simple" out-of-order X86 processor model
  - only 2^{37} were covered in verification
- 10 months of validation from first-silicon to release-to-production
  - (… but Intel aims to release a new processor every year…)

[1]B. Bentley, "Validating a modern microprocessor", Proc. Int. Conf. CAV

3

For some debugging tasks, we want to run chip at-speed.
- Allows for much more complete tests
- Allows for testing connected to real-world I/O

Problem, how do we look at internal signals?
- Bringing them out to pins is a lot of work, not necessarily effective



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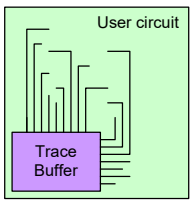
Trace Buffers: Embedded Logic Analyzers

Store "key" signals in an on-chip memory
- This allows the chip to run at speed
- After the chip runs, you can read out from the trace buffer and analyze off-line



Some issues:
- Need to decide which signals to monitor
- Need a mechanism to "trigger" (stop recording)
- Could use compression to store more data
- What about multiple clock domains?

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Embedded logic analyzers are included as part of FPGA design tools:

Intel -> Quartus SignalTap
Xilinx -> ChipScope

There are third party tools as well (eg, Certus from Mentor)

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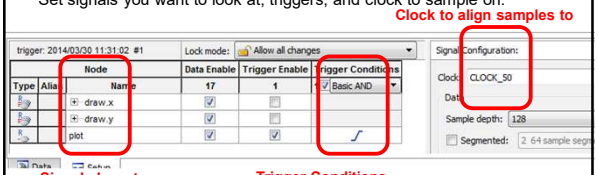
Quartus SignalTap

Set signals you want to look at, triggers, and clock to sample on:



Then recompile, and logic analyzer will be included in your design

- Uses logic elements and memory blocks just as any other circuit

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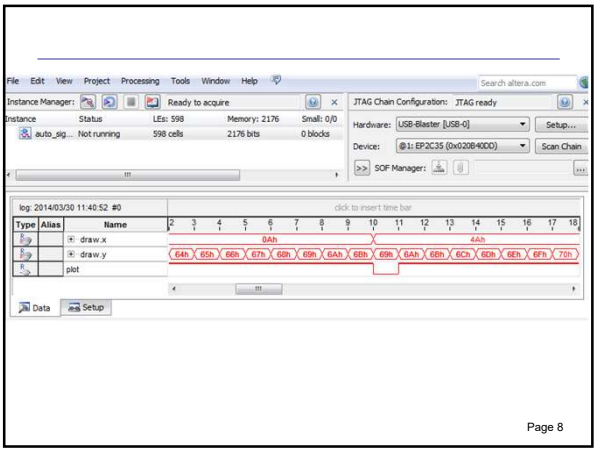

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"An engineer is as only as good as his/her tools…"

Should be:

"An engineer is only as good as the tools he or she knows how to use…"

There are a lot of advanced features of design tools, and they are worth getting to know.

Lots of information and tutorials on the web.

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