UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ELEC 402: Introduction to VLSI Design
Fall 2021
Assignment 3: The MOS Transistor / Cadence
Due Date: Sunday, Oct 24 th (via Email)

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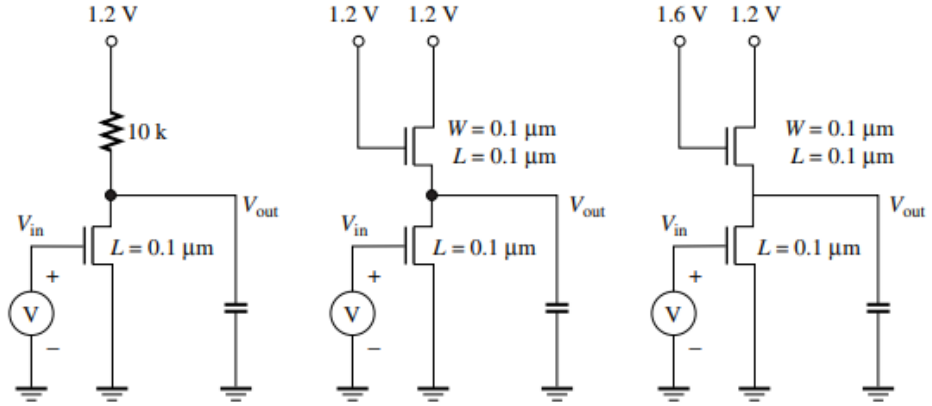
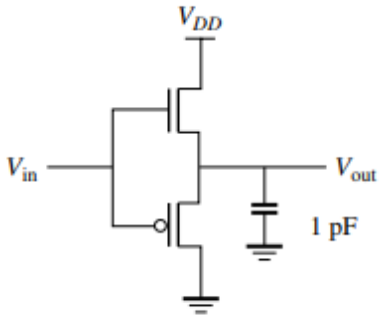
1. In the circuits of Figure , design the widths of the pull-down tran sistors so that $V_{OL} = 0.1$ V. (All transistors are minimum size, $L = 0.1$ μm.) Explain the results. (15 points)



$\mu_n = 270$ cm^2/V-s, $C_{ox} = 1.0$ μF/cm^2, $V_{T0} = 0.4$ V, $V_{DD} = 1.2$ V

$E_{CN}L = 0.6$ V, $v_{sat} = 8 \times 10^6$ cm/s, $\gamma = 0.2$ V$^{1/2}$ $2|\phi_F| = 0.88$ V,

2. (a) What is the intended function of the circuit shown in Figure ? What is the output swing?



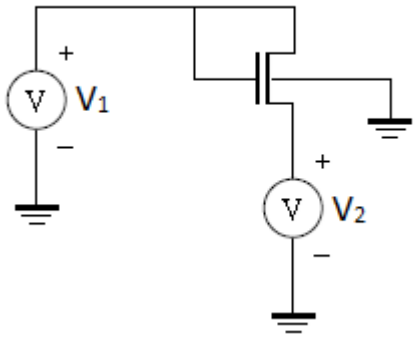
(b) Draw the dc voltage transfer characteristic of the above gate. Label V_{OL} and V_{OH}, and any other interesting values in the VTC. Since the gate has hysteresis, be sure to handle both the rising and falling cases.

(c) What is the gain of the circuit? Is this a valid gate (i.e., does it have the needed noise rejection properties)?

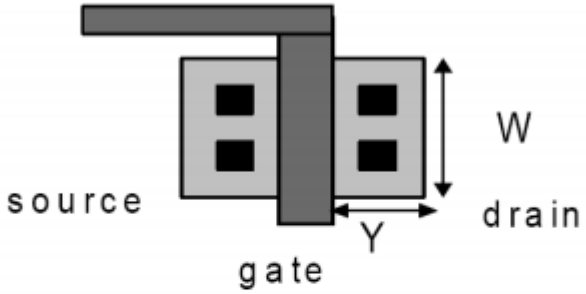
(d) Use CAD to validate your solution by plotting the VTC (20 points)

- For CAD simulation in Q2 assume V_{DD} = 0.9 V, and use two fingers per transistor.

3. Figure shows a circuit used to measure the effective value of body effect factor (γ) (by measuring V_T at different source voltages) and channel length modulation factor (λ) (by measuring I_d at different Vds values). Assume in formula for threshold voltage (slide 7 lecture set 4 – MOS basics), $2\varphi_F$ = 0.88 V, and calculate VT0, γ, and λ for a device with 2 fingers. Can you justify the value of γ for the FinFET device you are simulating? Attach your CAD netlist, graphs and measurement data to your answers (**25 points**)



4. Consider the layout in the figure below implemented in a 180nm technology. Assume that the transistor has W=900nm, L=180nm and a source/drain dimension Y=800nm and a lateral diffusion of 22nm. Let tox =40 Å (Angstroms). (12 points)



a. Compute the worst case gate capacitance per unit width, C_g, in units of fF/um. Estimate C_{GS}, C_{GD} and C_{GB} in linear, saturation and cutoff, including overlap effects.

b. If $N_A=3x10^{16}/cm^3$ and $N_D=3x10^{19}/cm^3$, x_j=300nm, compute the worst-case capacitance value per unit width, C_j, in units of fF/um.

c. Compute the drain junction capacitance for the following cases (m=0.5):
   i. V_D=1.8V, V_B=0V
   ii. V_D=0V, V_B=0V

5. A CMOS inverter in 45 nm technology has a pull-up device that is 8λ:2λ and a pull-down device that is 4λ:2λ. It drives four identical inverters at its output. Compute the inverter delay (use C_g = 2 fF/um) and assume a ramp input. Re-calculate the delay if we have a chain of 4 inverters, i.e. 4 inverters in series (**13 pts**) Note: 2λ = 45nm