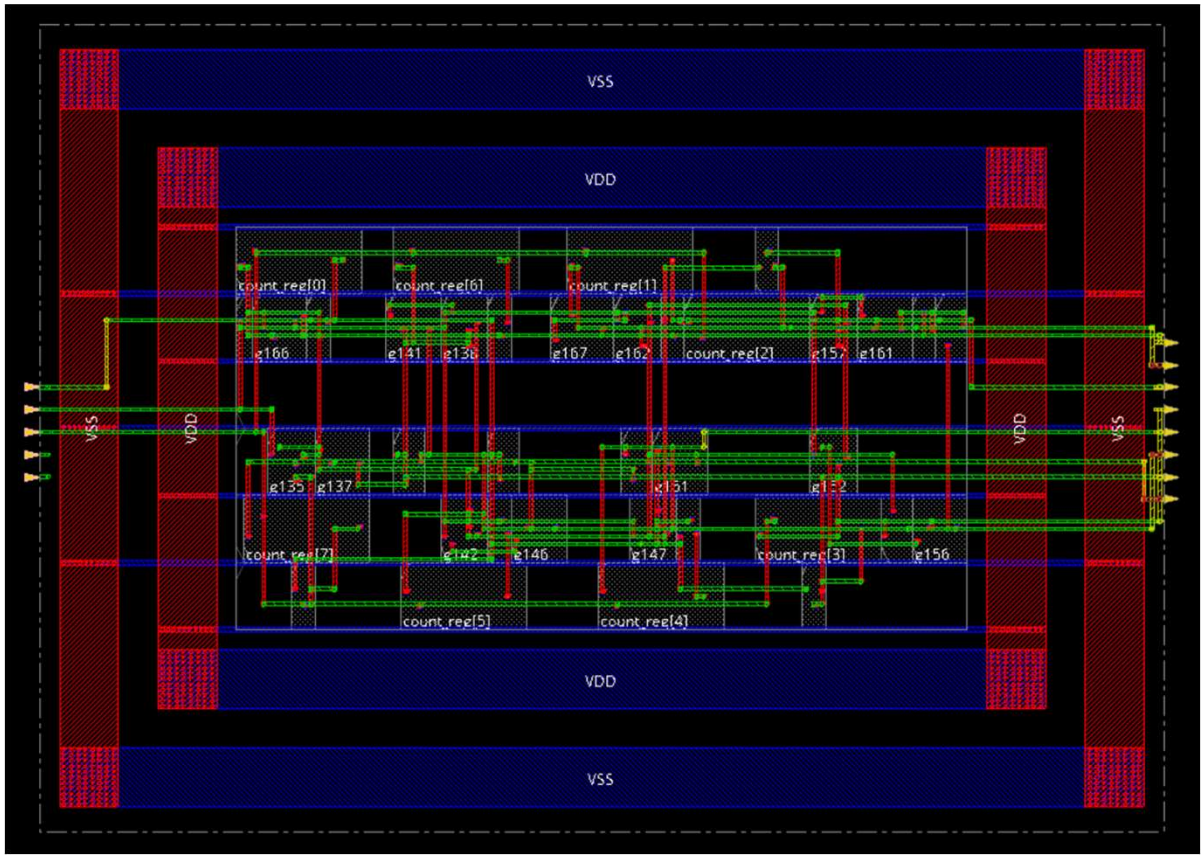
Tutorial 5:
Place and Route (PnR)

Sean Lam
seanlm@student.ubc.ca

Outline

Goal: Synthesize mapped Verilog file, run Innovus to auto-route your Verilog, export GDS and netlist, and simulate.



Synthesizing in 45nm

Previously, we used the 15nm PDK to synthesize a mapped Verilog file and perform layout in 15nm…

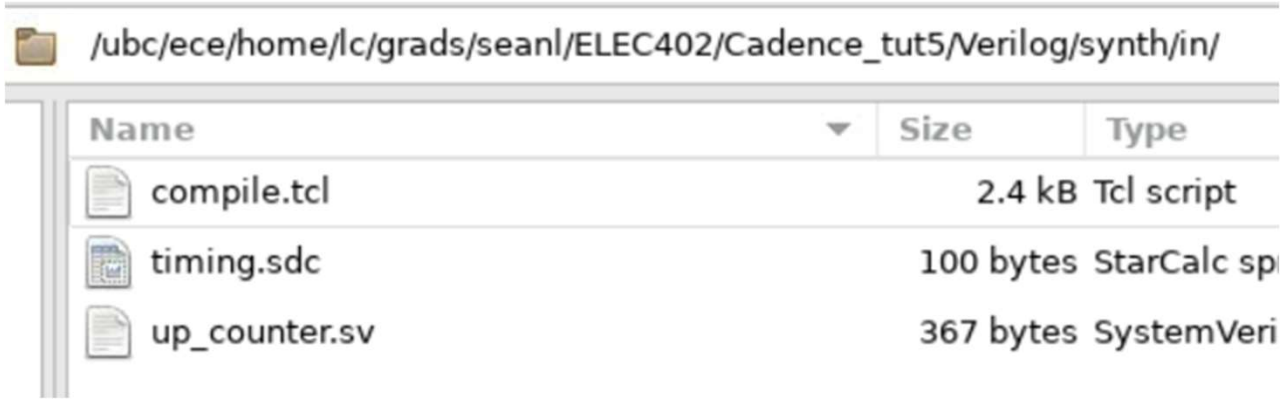
15nm PDK is missing files for PnR 

We will use 45nm PDK to synthesize our Verilog and run PnR.

```
# Create project directory
>> mkdir Cadence_tut5
>> cd Cadence_tut5

# Create synthesis directory
>> mkdir Verilog
>> cd Verilog

# Source scripts
>> source /CMC/kits/AMSKIT616_GPDK/underg_install.csh
>> source setup_local.csh
```

Synthesizing in 45nm

Copy the compile script (compile.tcl), timing constraint file (timing.sdc), and System Verilog file (up_counter.sv) from tutorial 2 / assignment 2 to the synth/in folder:



Synthesizing in 45nm

Open the compile script (compile.tcl) in a text editor and change the following lines. We are setting the libraries to reference the 45nm cells and library.

Before

```
# Set PDK Library
set PDKDIR /ubc/ece/data/cmc2/kits/ncsu_pdk/FreePDK15/
set_attribute lib_search_path
/ubc/ece/data/cmc2/kits/ncsu_pdk/FreePDK15/NanGate_15nm_OCL_v0.1_2014_06_Apache.A/front_end/timing_power_noise/CCS
set_attribute library {NanGate_15nm_OCL_worst_low_conditional_ccs.lib}
```

After

```
# Set PDK Library
set PDKDIR /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/
set_attribute lib_search_path /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/timing
set_attribute library {slow_vdd1v0_basicCells.lib}
```

Synthesizing in 45nm

Compile script (compile.tcl) should look like the following:

Open ▾ | compile.tcl
~/ELEC402/Cadence_tut5/Verilog/synth/in

```
# Include TCL utility scripts
include load_etc.tcl

# Timestamp
date

# Print status
puts "\n\n> Setting up Synthesis Environment . . ."

# Top level design name variable
set DESIGN up_counter

# Set synthesis, mapping, and working directory
set SYN_EFF medium
set MAP_EFF medium
set SYN_PATH "."

# Set PDK Library
set PDKDIR /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/
set_attribute lib_search_path /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/timing
set_attribute library {slow_vdd1v0_basicCells.lib}

# Read in user Verilog files (add -sv flag for SystemVerilog files)
read_hdl -sv ./in/up_counter.sv

# Elaboration validates the syntax (elaborate top-level model)
elaborate $DESIGN

# Status update
puts "> Reading HDL complete."
puts "> Runtime and memory stats:"
timestat Elaboration

# Show any problems
puts "\n\n> Checking design . . ."
check_design -unresolved

# Read timing constraint and clock definitions
puts "\n\n> Reading timing constraints . . ."
read_sdc ./in/timing.sdc

# Synthesize generic cell
puts "\n\n> Synthesizing to generic cell . . ."
synthesize -to_generic -eff $SYN_EFF
puts "> Done. Runtime and memory stats:"
timestat GENERIC

# Synthesize to gates
puts "\n\n> Synthesizing to gates . . ."
synthesize -to_mapped -eff $MAP_EFF -no_incr
puts "> Done. Runtime and memory stats:"
timestat MAPPED

# Incremental synthesis
puts "\n\n> Running incremental synthesis . . ."
synthesize -to_mapped -eff $MAP_EFF -incr
puts "\n\n> Inserting Tie Hi and Tie Low cells . . ."
insert_tiehilo_cells
puts "> Done. Runtime and memory stats:"
timestat INCREMENTAL

# Generate report to files
puts "\n\n> Generating reports . . ."
report area > ./out/${DESIGN}_area.rpt
report gates > ./out/${DESIGN}_gates.rpt
report timing > ./out/${DESIGN}_timing.rpt
report power > ./out/${DESIGN}_power.rpt

# Generate output verilog file to be used in Encounter and ModelSim
puts "\n\n> Generating mapped Verilog files . . ."
write_hdl -mapped > ./out/${DESIGN}_map.v

# Generate constraints file to be used in Encounter
puts "\n\n> Generating constraints file . . ."
write_sdc > ./out/${DESIGN}_map.sdc

# Generate delay file to be used in ModelSim
puts "\n\n> Generating delay file . . ."
write_sdf > ./out/${DESIGN}_map.sdf

# Status update
puts "> Synthesize complete. Final runtime and memory:"
timestat FINAL

# Done
puts "\n\n> Exiting . . ."
quit
```

Synthesizing in 45nm

Open the System Verilog file (up_counter.sv) and add ‘VDD’ and ‘VSS’ as inout ports:

Open ▾ | up_counter.sv
~/ELEC402/Cadence_tut5/Verilog/synth/in

```
/* Name:
 * Student ID: XXXXXXXX
 * Purpose: A simple up-counter
 */
module up_counter (
        input logic clk,
        input logic rst,
        input logic en,

        output logic[7:0] count,
        inout VDD,
        inout VSS
);

always_ff @(posedge clk) begin
        if (rst) begin
        count <= 0;
        end
        else if (en) begin
        count <= count + 1;
        end
end
endmodule
```

VDD and VSS ports will be used in Innovus to route VDD and VSS rails.

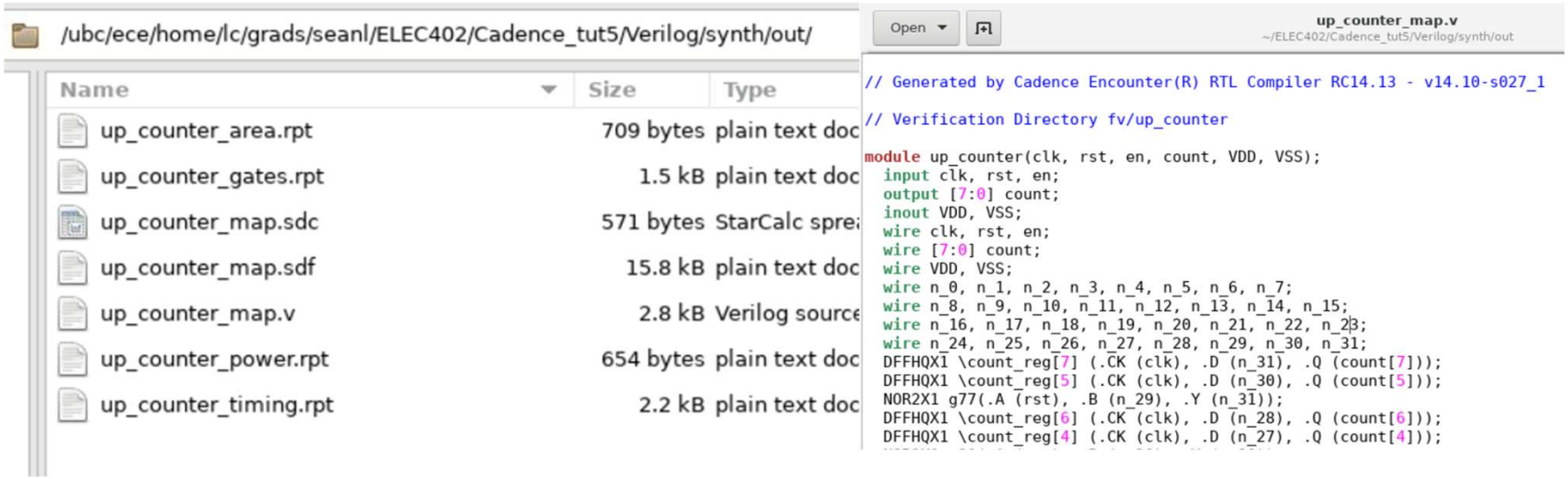
Synthesizing in 45nm

Keep the timing constraint file (timing.sdc) the same. Run synthesis.

From the synth folder
>> source ../setup_local.csh && rc

After the checkout process completes, source the compile script
>> source ./in/compile.tcl

Note/fix any errors that show in the terminal.

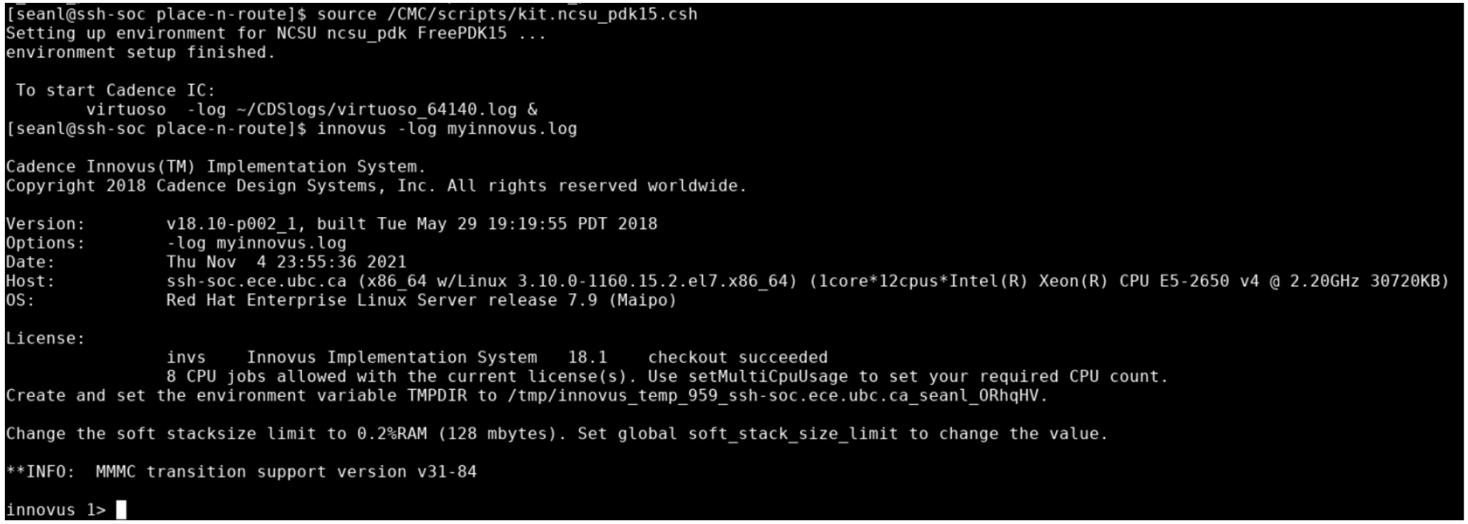


Innovus Place and Route

To start using Innovus to perform place and route, create a working directory for place and route:

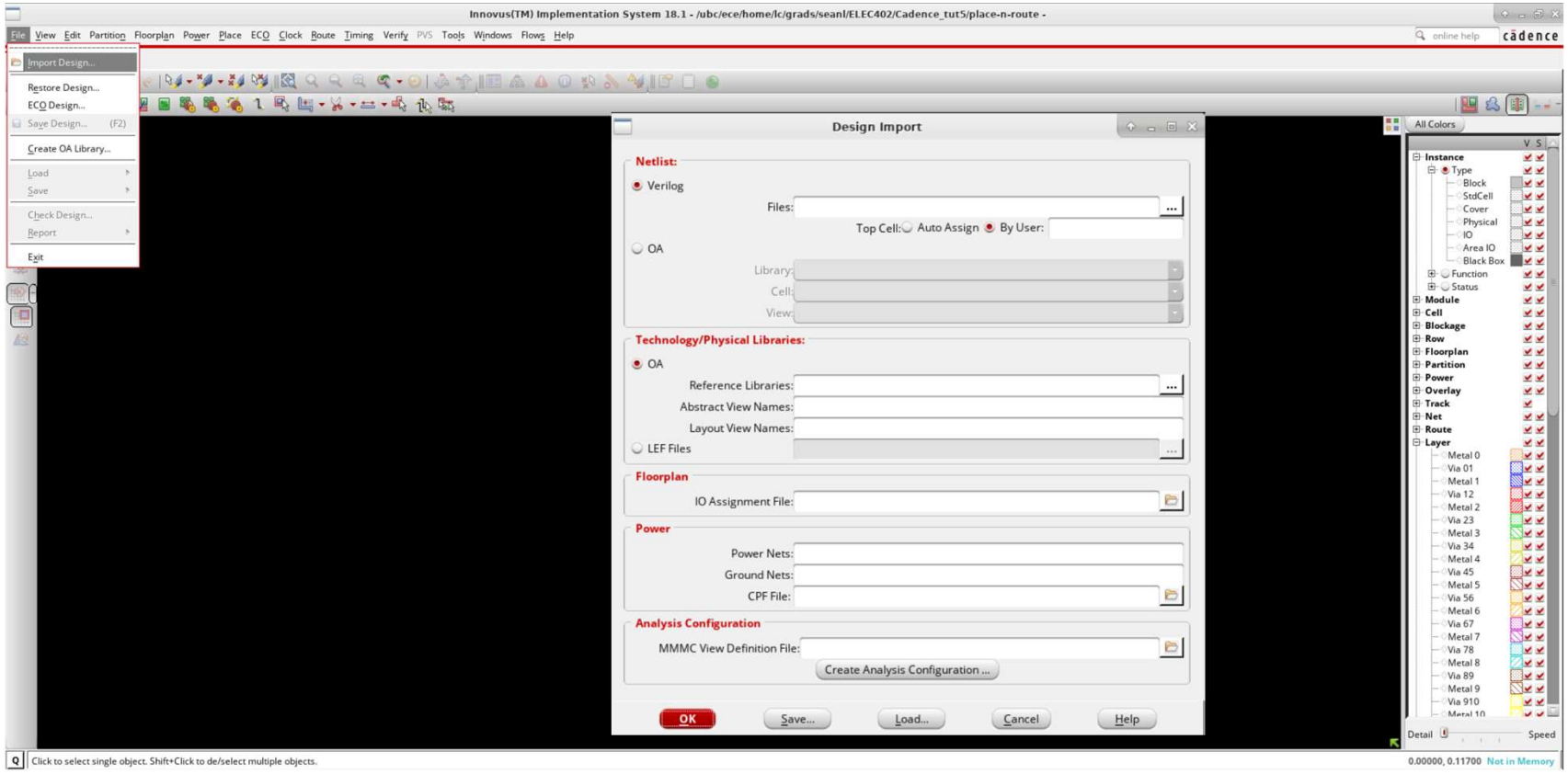
From project directory, create working directory for place and route
>> mkdir place-n-route
>> cd place-n-route

Source script to set up Innovus, then launch Innovus. NOTE: The 15nm script is used here ONLY
to set up Innovus. We are NOT using the 15nm PDK to perform place and route.
>> source /CMC/scripts/kit.ncsu_pdk15.csh
>> innovus –log myinnovus.log



Innovus Place and Route

Innovus window will show. Navigate to File → Import Design.



Innovus Place and Route

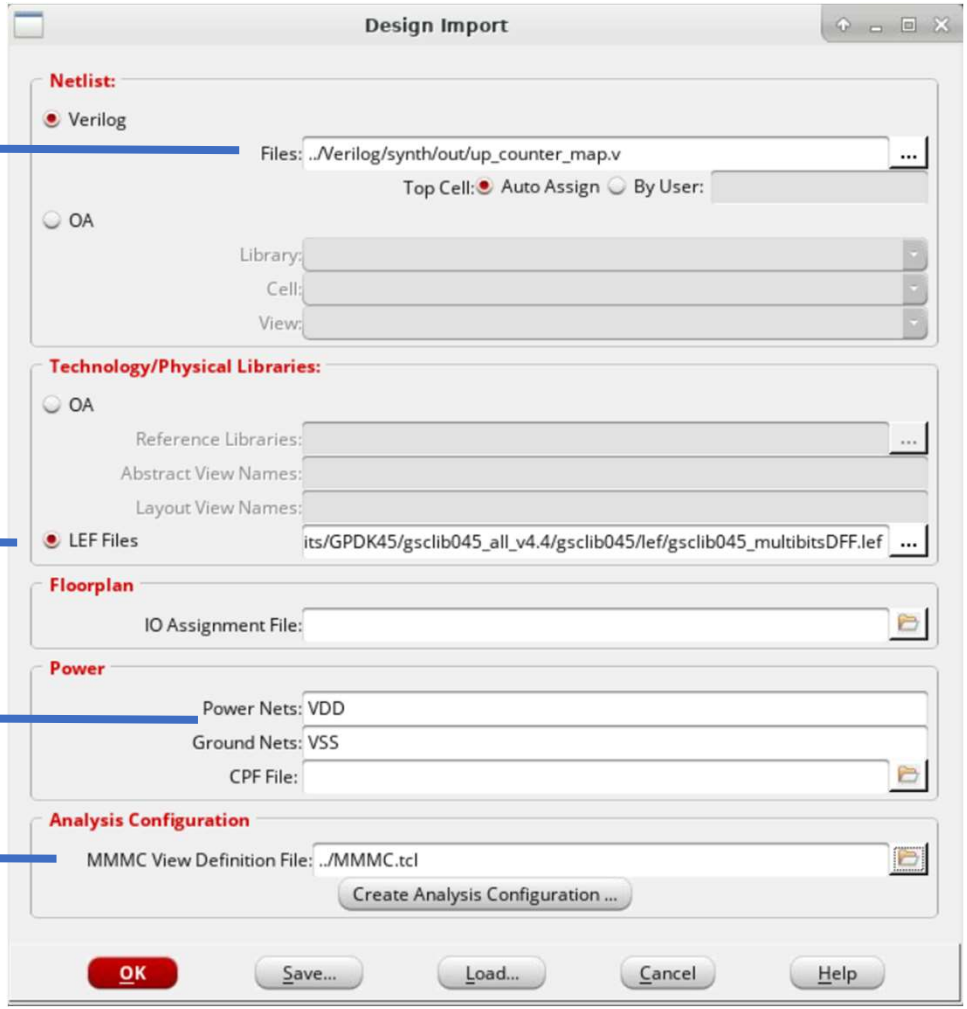
Set the fields accordingly…

Path to mapped Verilog file (from synthesis)

See next slide(s) on how to set LEF files.
LEF files configure routing based on DRC.
Order matters!

Label VDD and VSS nets

See next slide(s) on how to edit MMMC file.
Browse to find MMMC file.
This file performs analysis across PVT variation.

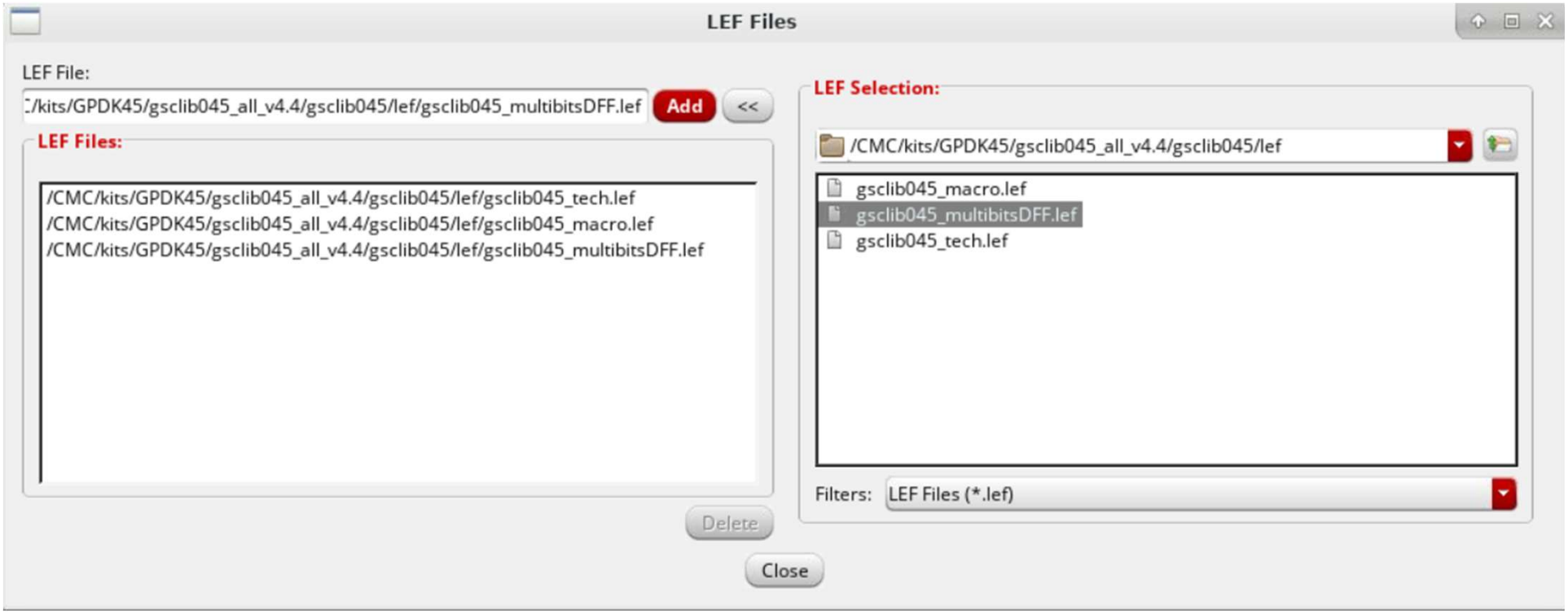


Innovus Place and Route

IMPORTANT: Set the LEF files based on the following order:

1. ..._tech.lef
2. …_macro.lef
3. …_multibitsDFF.lef

LEF files found in /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/lef



Innovus Place and Route

Edit the MMMC file (MMMC.tcl).

Ensure libraries are set as shown.

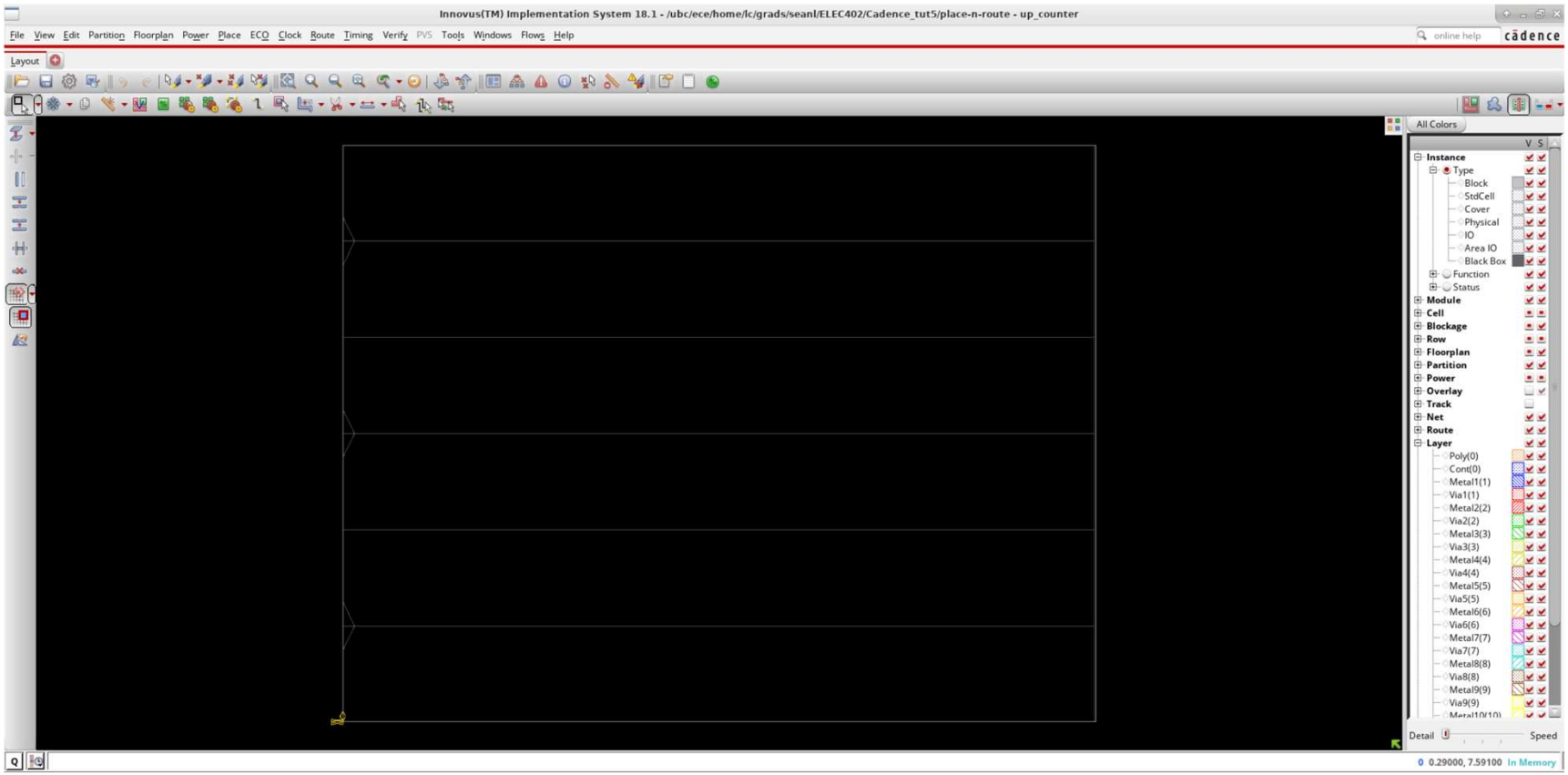
Set path to synthesized timing constraint file (up_counter_map.sdc).

MMMC.tcl
~/ELEC402/Cadence_tut5

```
# Pass in variables that where defined in the run.1.tcl script
global PDKDIR
global SDC_FILE

create_library_set -name lsMax \
   -timing \
    [list /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/timing/slow_vdd1v0_basicCells.lib]

create_library_set -name lsMin \
   -timing \
    [list /CMC/kits/GPDK45/gsclib045_all_v4.4/gsclib045/timing/fast_vdd1v0_basicCells.lib]

create_rc_corner -name rcWorst\
   -qx_tech_file /CMC/kits/AMSKIT616_GPDK/tech/gsclib045_all_v4.4/gsclib045/qrc/qx/gpdk045.tch \
   -preRoute_res 1\
   -postRoute_res 1\
   -preRoute_cap 1\
   -postRoute_cap 1\
   -postRoute_xcap 1\
   -preRoute_clkres 0\
   -preRoute_clkcap 0

create_rc_corner -name rcBest\
   -qx_tech_file /CMC/kits/AMSKIT616_GPDK/tech/gsclib045_all_v4.4/gsclib045/qrc/qx/gpdk045.tch \
   -preRoute_res 1\
   -postRoute_res 1\
   -preRoute_cap 1\
   -postRoute_cap 1\
   -postRoute_xcap 1\
   -preRoute_clkres 0\
   -preRoute_clkcap 0

create_delay_corner -name dc_lsMax_rcWorst\
   -library_set lsMax\
   -rc_corner   rcWorst
create_delay_corner -name dc_lsMin_rcBest\
   -library_set lsMin\
   -rc_corner   rcBest

#Change .SDC directory
create_constraint_mode -name cmFunc\
   -sdc_files\
    [list /ubc/ece/home/lc/grads/seanl/ELEC402/Cadence_tut5/Verilog/synth/out/up_counter_map.sdc]


create_analysis_view -name av_lsMax_rcWorst_cmFunc -constraint_mode cmFunc -delay_corner dc_lsMax_rcWorst
create_analysis_view -name av_lsMin_rcBest_cmFunc  -constraint_mode cmFunc -delay_corner dc_lsMin_rcBest

set_analysis_view -setup [list av_lsMax_rcWorst_cmFunc] -hold [list av_lsMin_rcBest_cmFunc]
```

Innovus Place and Route

After successfully importing layout, boundaries of area and in/out pins can be seen at bottom left corner.

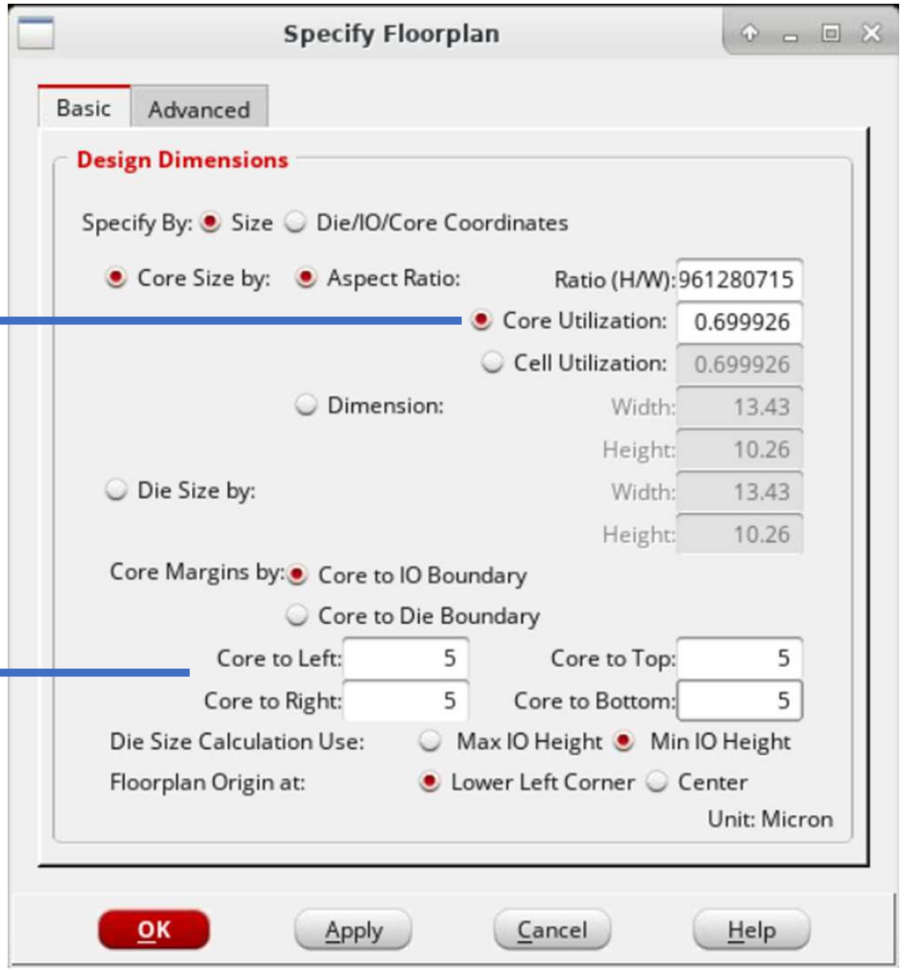


Innovus Place and Route

Select dimensions of your layout, IO ring spacing, and core utilization.
Go to Floorplan→Specify Floorplan

Increasing core utilization
→ smaller footprint
→ harder for tool to route
→ potential LVS issues

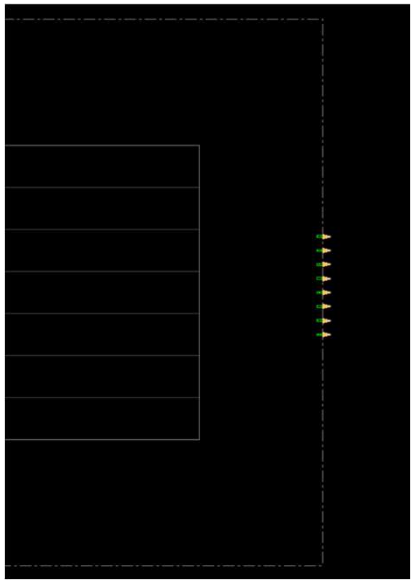
Leave space around the core for VDD and VSS rings.

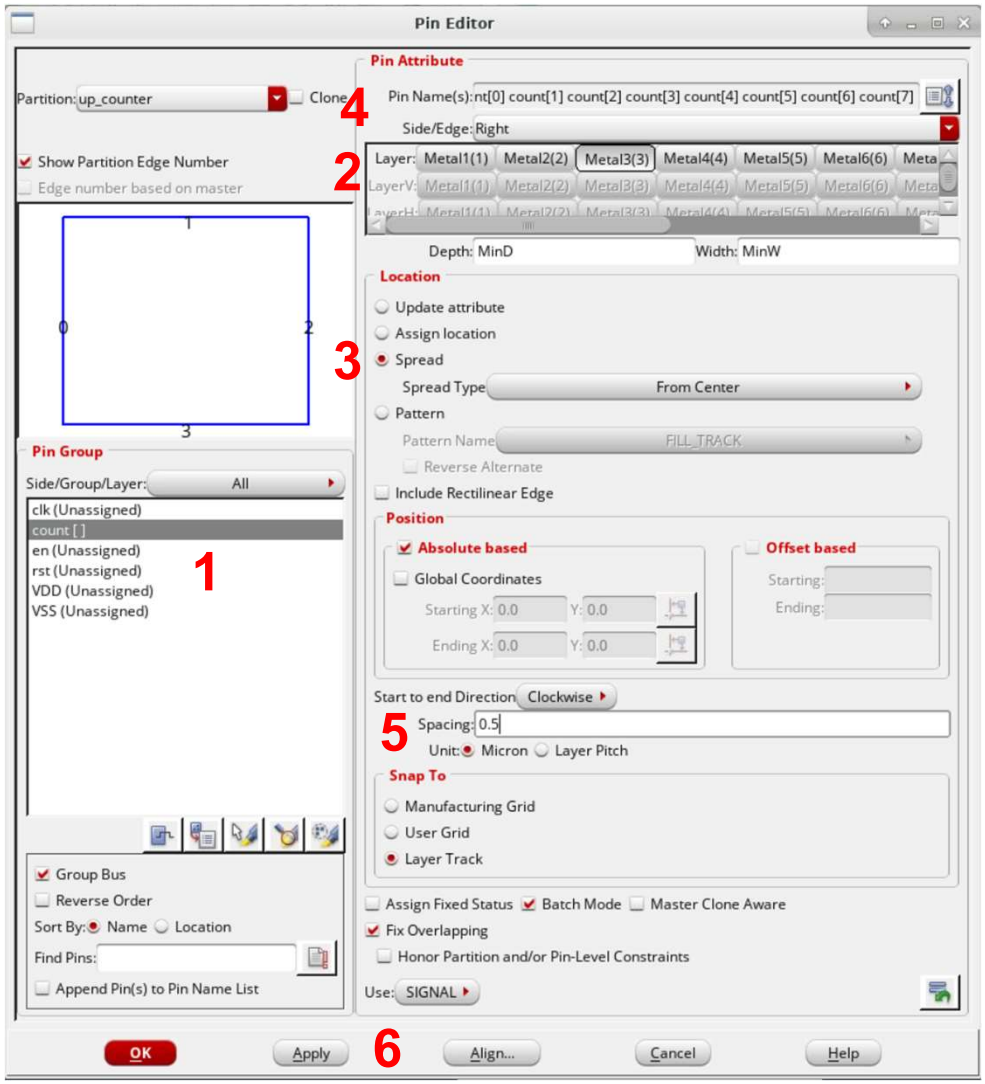


Innovus Place and Route

Edit the location of pins.
Navigate to Edit→Pin Editor

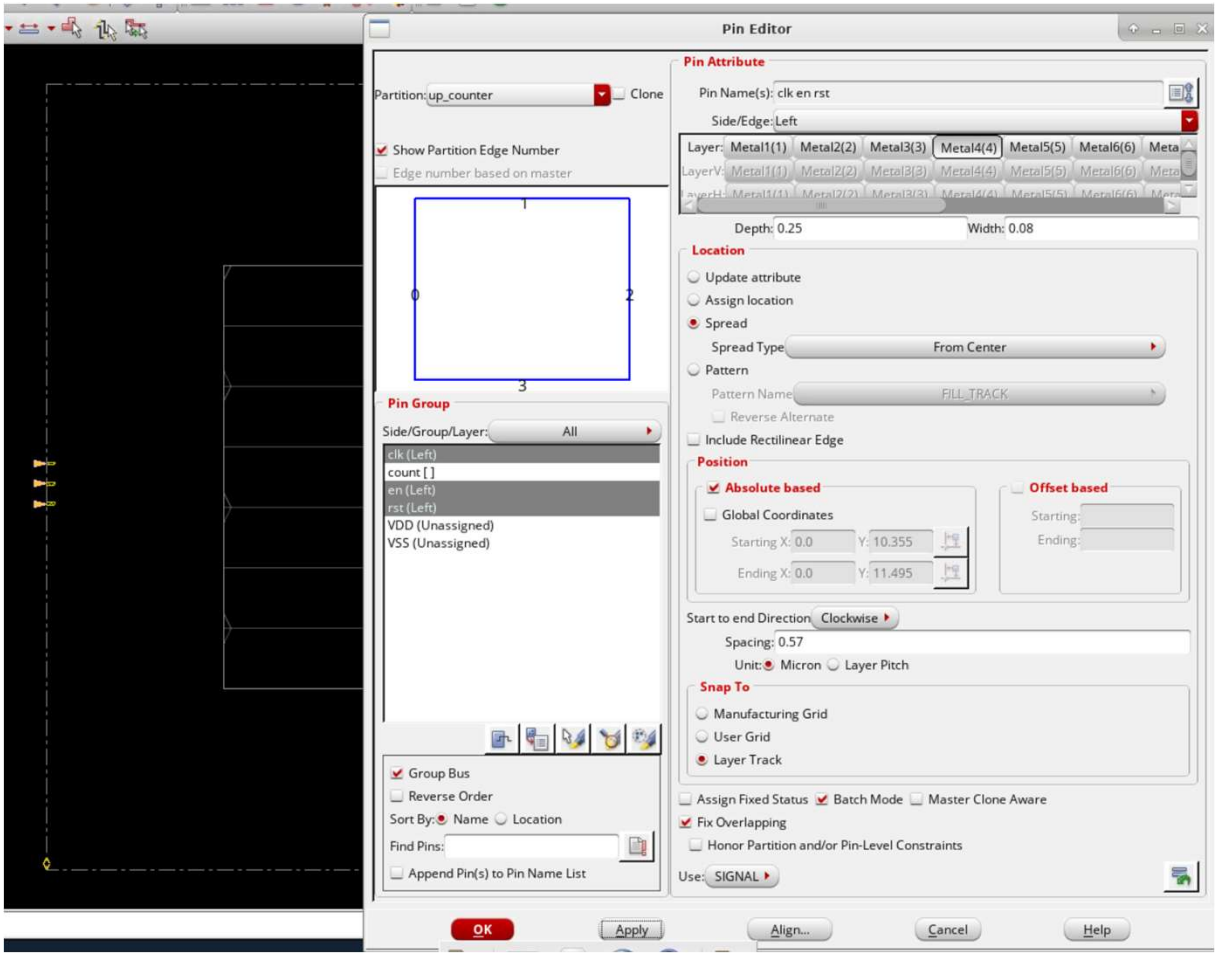
1. Select signal to assign to pin
2. Select layer
3. Check “Spread”
4. Select Side/Edge (right, left, top, bottom)
5. Set spacing (units: um)
6. Click Apply to see it on the layout





Innovus Place and Route

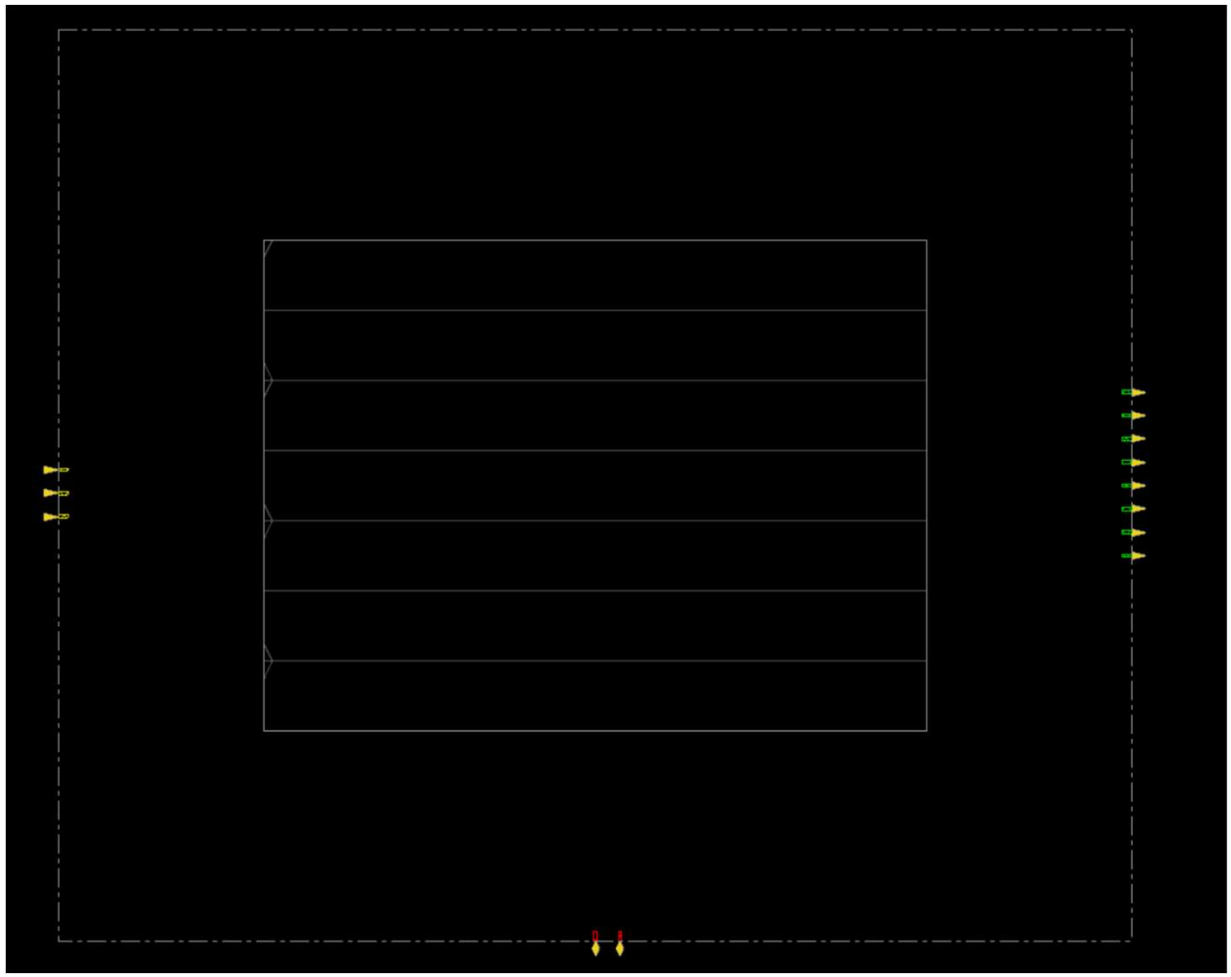
Set location of other pins along with VDD and VSS.



Innovus Place and Route

Layout with pins only

EN, RST, CLK



COUNT[7:0]

VDD, VSS

Innovus Place and Route

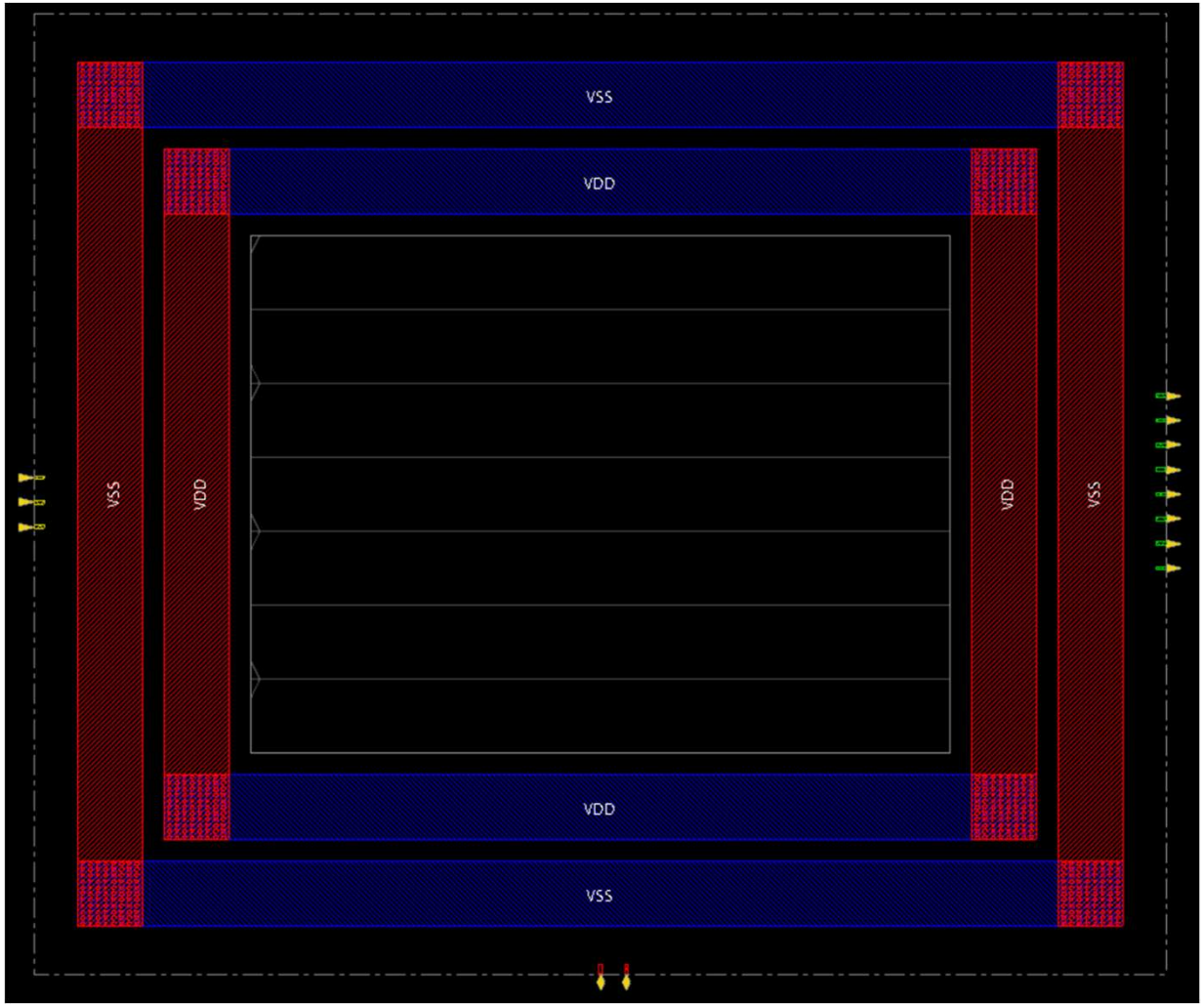
Add VDD and VSS rings.
Navigate to Power→Power Planning→Add ring

Choose power nets

Choose metal layer, proper width (based on power consumption and DRC), and proper spacing between rings.

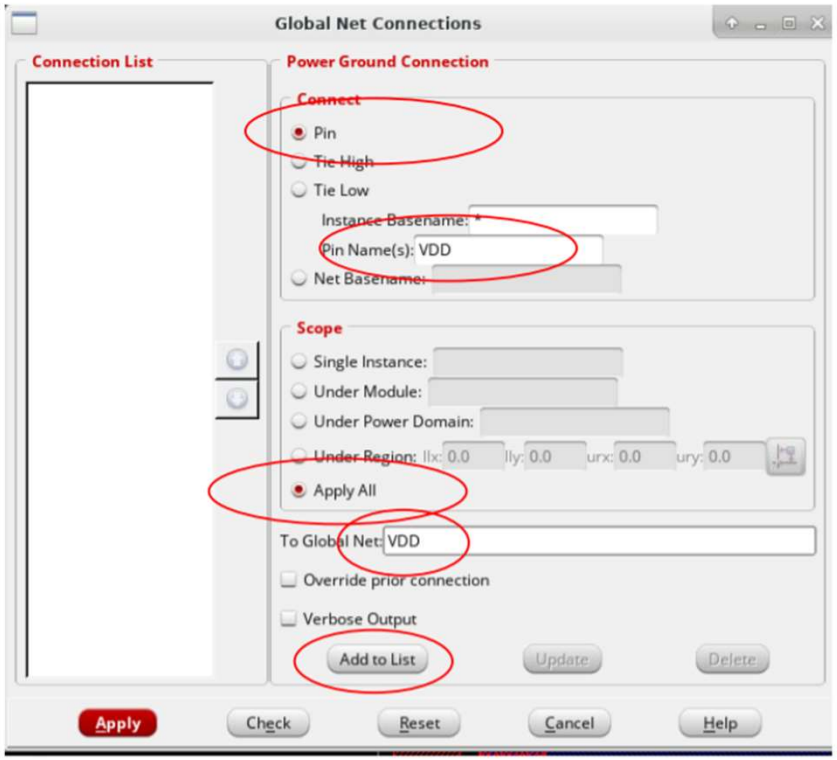
Innovus Place and Route

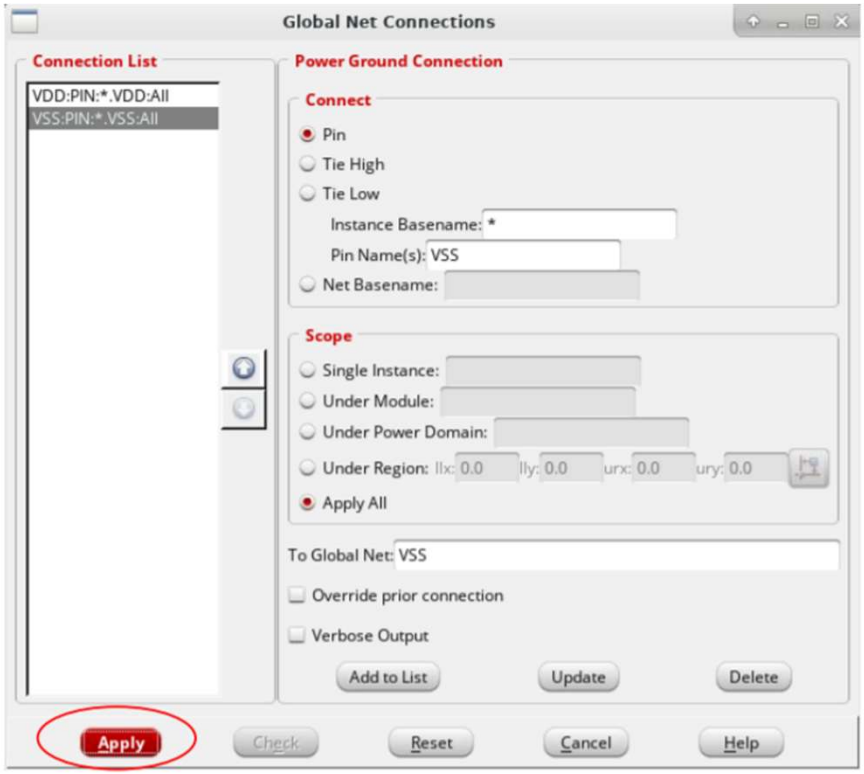
After adding VDD and VSS rings.



Innovus Place and Route

Set Global VDD and VSS connections.
Navigate to Power→Connect Global Nets.
Add VDD and VSS to connection list.



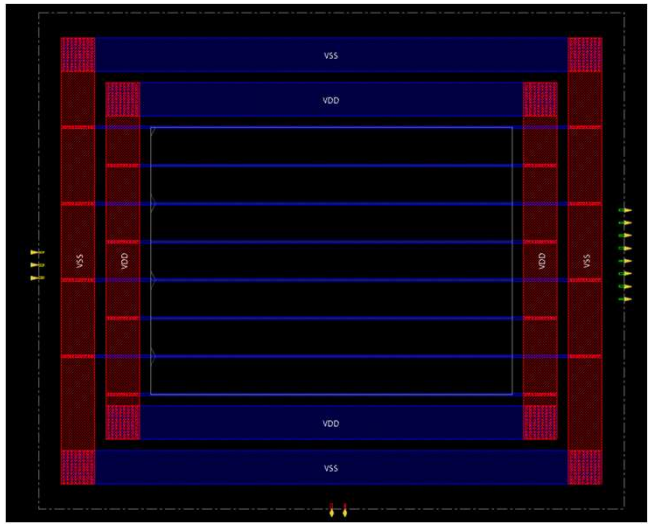


Innovus Place and Route

To route VDD and VSS, go to Route→Special Route

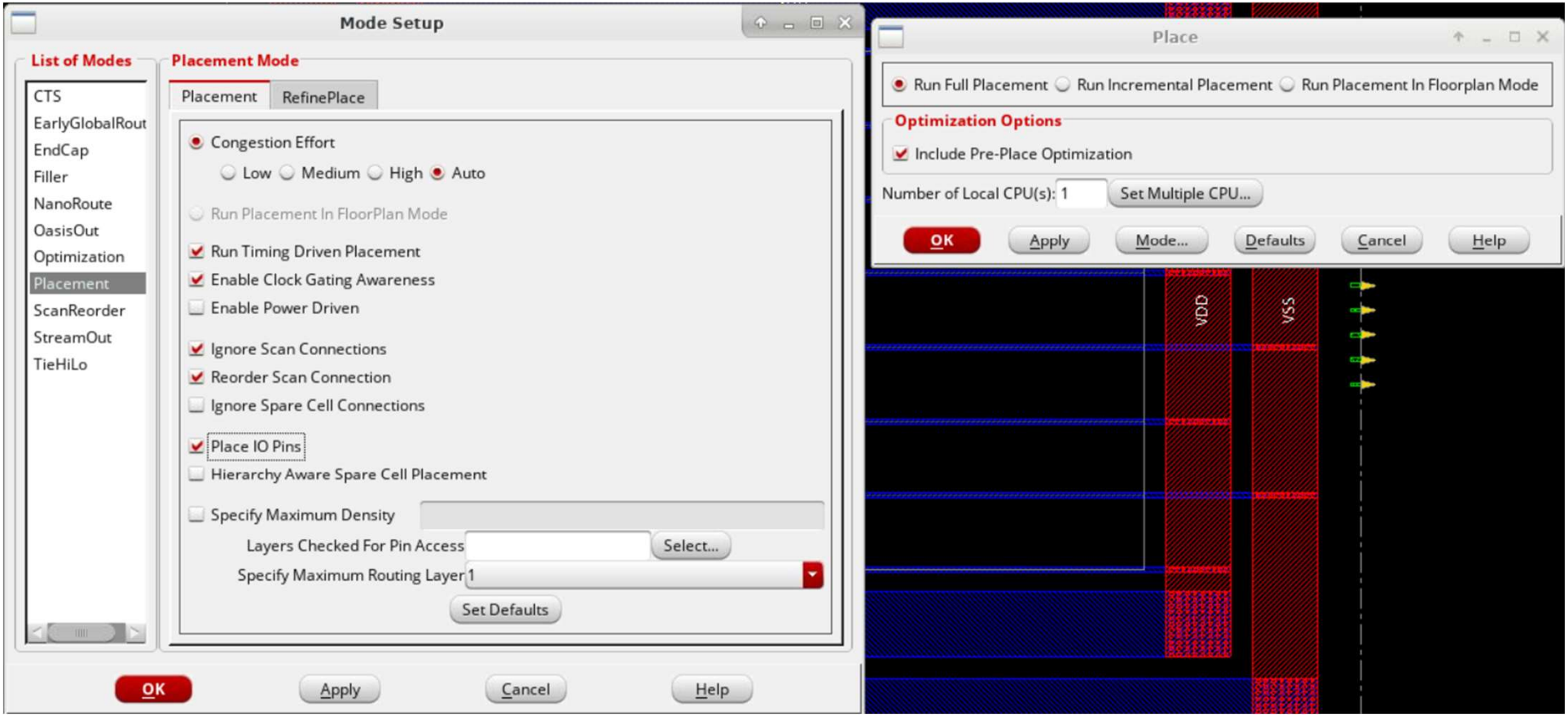
Choose power nets

Select layers to route VDD and VSS upon



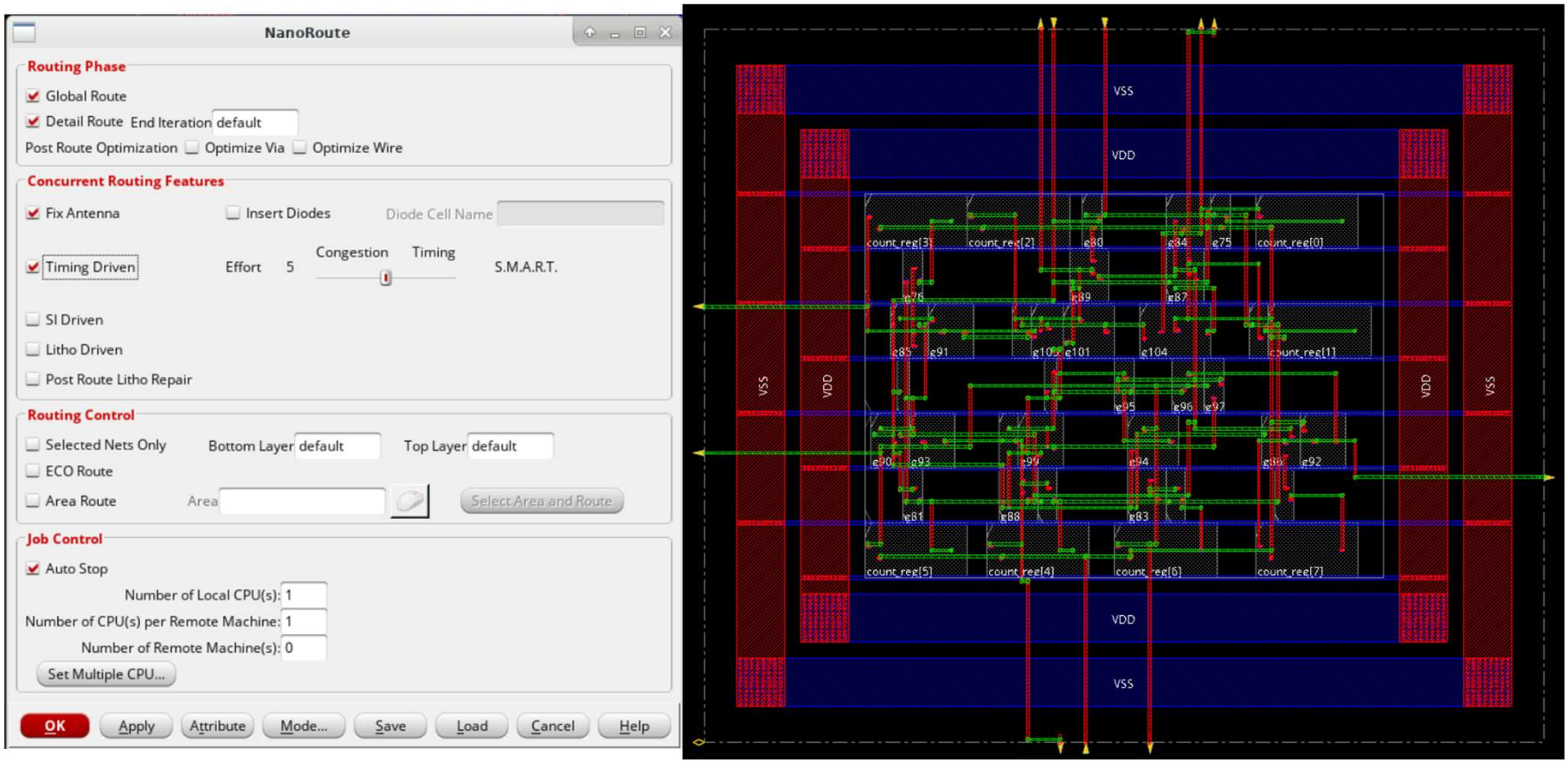
Innovus Place and Route

To place standard cells, go to Place→Standard Cell Placement. Click on Mode to configure the Placement Mode settings as below. The, click OK.



Innovus Place and Route

Layout is generated, but note how the cells are black boxed cells (i.e. empty). We will map them to layout cells from 45nm library later.
OPTIONAL: You can optimize the layout for lower latency by opening Route→Nano Route→Route.



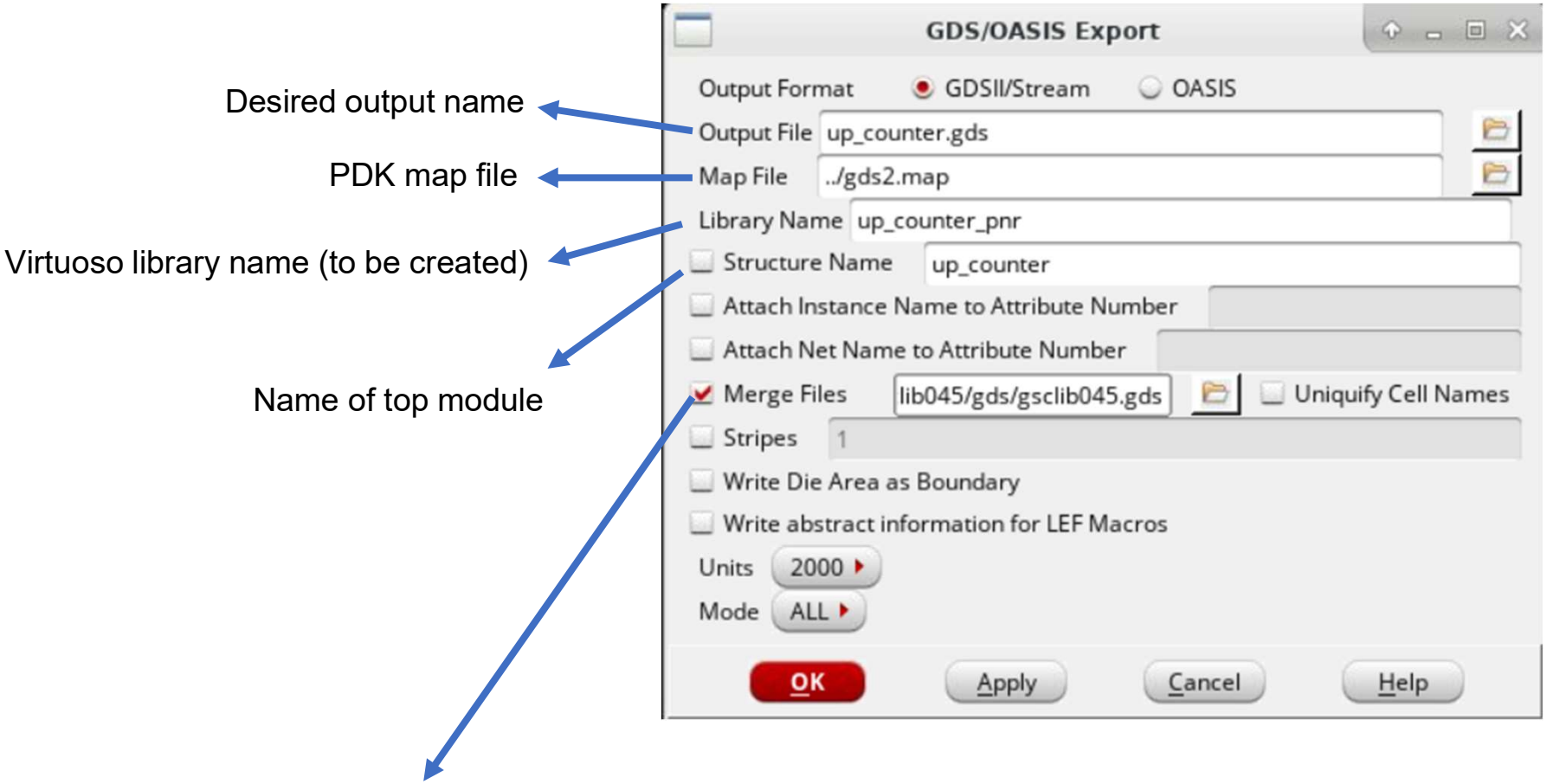
Innovus Place and Route

Verify connectivity by running Verify→Verify Connectivity. Important after any modifications to routing. Check Terminal for results.

```
innovus 1> VERIFY_CONNECTIVITY use new engine.

******** Start: VERIFY CONNECTIVITY ********
Start Time: Fri Nov  5 00:55:59 2021

Design Name: up_counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (26.2000, 22.2300)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Nov  5 00:55:59 2021
Time Elapsed: 0:00:00.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)

innovus 1>
```

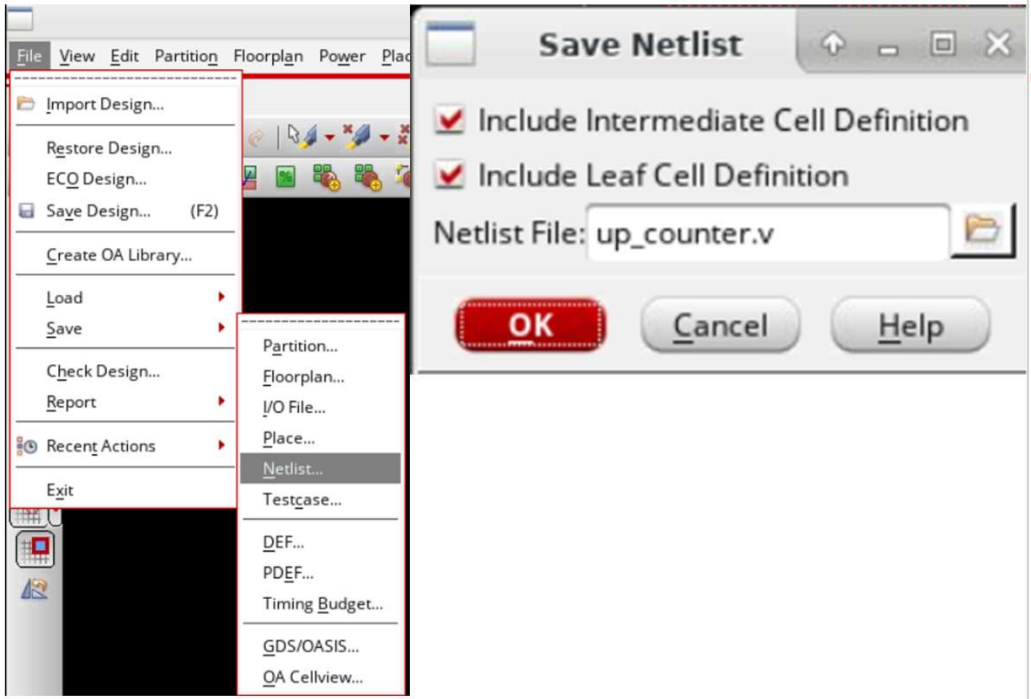
Innovus Place and Route

To export layout to GDS and replace black box cells, go to File→Save→GDS/OASIS Export



Innovus Place and Route

Next, we save the netlist/export a Verilog file as a netlist.
File→Save→Netlist



Open ▾ up_counter.v
~/ELEC402/Cadence_tut5/place-n-route

```
/*
##############################################################
#  Generated by:      Cadence Innovus 18.10-p002_1
#  OS:                Linux x86_64(Host ID ssh-soc.ece.ubc.ca)
#  Generated on:      Mon Nov  8 20:39:59 2021
#  Design:            up_counter
#  Command:           saveNetlist up_counter.v
##############################################################
*/
// Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
// Verification Directory fv/up_counter
module up_counter (
        clk,
        rst,
        en,
        count,
        VDD,
        VSS);
   input clk;
   input rst;
   input en;
   output [7:0] count;
   inout VDD;
   inout VSS;

   // Internal wires
   wire n_0;
   wire n_1;
   wire n_2;
   wire n_3;
   wire n_4;
   wire n_5;
   wire n_6;
   wire n_7;
   wire n_8;
   wire n_9;
   wire n_10;
   wire n_11;
   wire n_12;
   wire n_13;
   wire n_14;
   wire n_15;
   wire n_16;
   wire n_17;
   wire n_18;
   wire n_19;
   wire n_20;
   wire n_21;
   wire n_22;
   wire n_23;
```

Virtuoso: Post Place and Route

After completing place and route, we exported/saved:
1. GDS (layout of your design)
2. Netlist (Verilog that describes your design)

We will now open Virtuoso to import the layout and netlist to run simulations and check the layout.

From project directory, create working directory for place and route
>> mkdir virt
>> cd virt

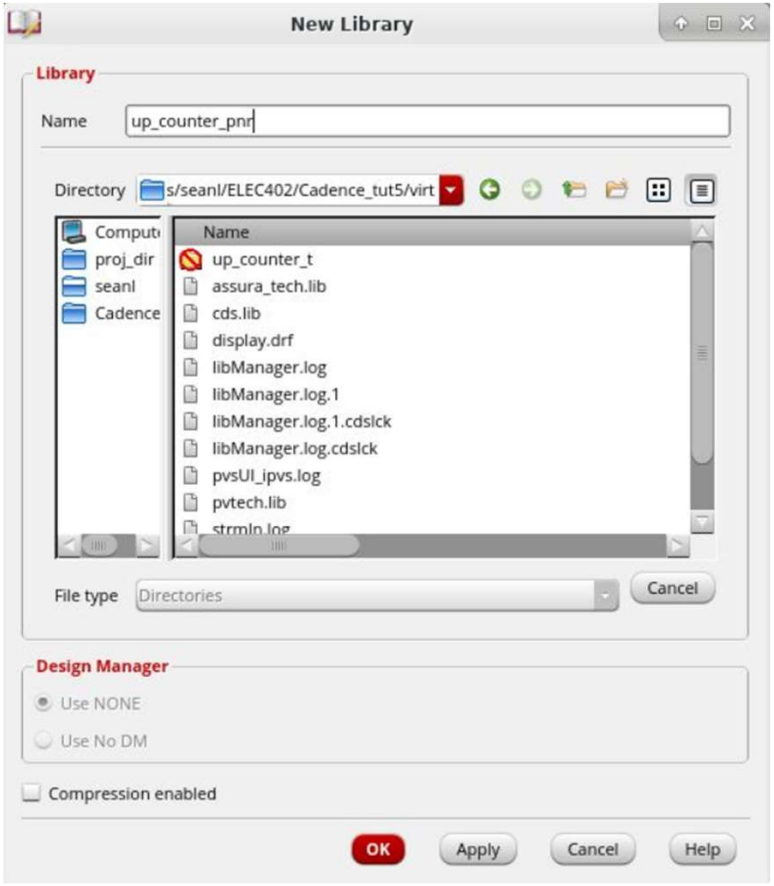
Source script
>> source /CMC/scripts/kit.gpdk45_OA.csh
>> source /CMC/scripts/cadence.spectre18.10.235.csh

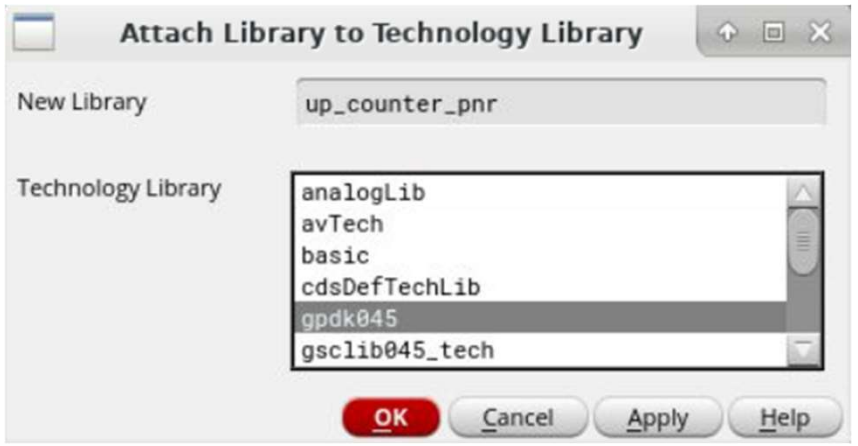
Open Virtuoso
>> virtuoso &

 # NOTE: If errors show up while opening Virtuoso and you cannot see 45nm libraries, close
 # Virtuoso and source the following before opening virtuoso
>> source /CMC/scripts/kit.gpdk45_OA_v5.csh
>> source /CMC/scripts/cadence.spectre18.10.235.csh
>> virtuoso &

Virtuoso: Post Place and Route

Create a library with the same name as specified when saving/exporting a GDS in Innovus.
Attach to an existing technology library and specify ‘gpdk045’.





Virtuoso: Post Place and Route

From the CIW window, go to File→Import→Stream and import the GDS file.

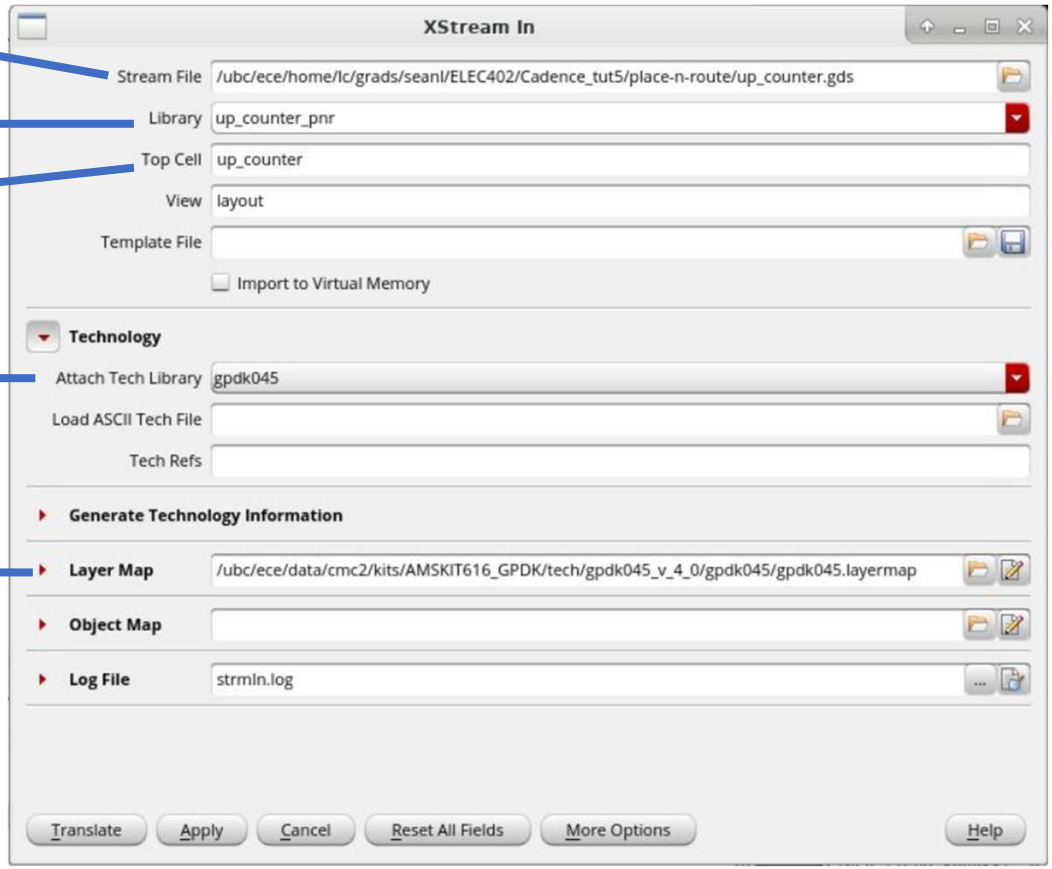
GDS File

Library name

Top cell name in GDS (use module name)

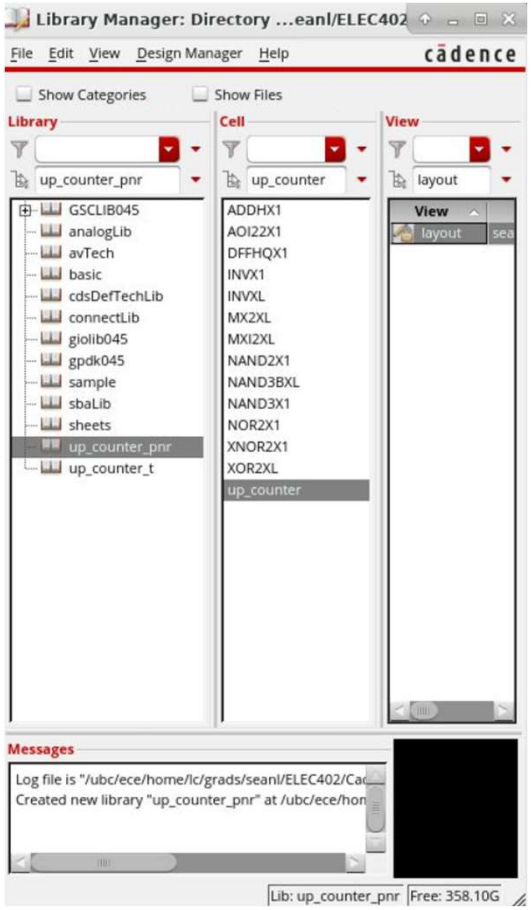
Attach to gpdk045

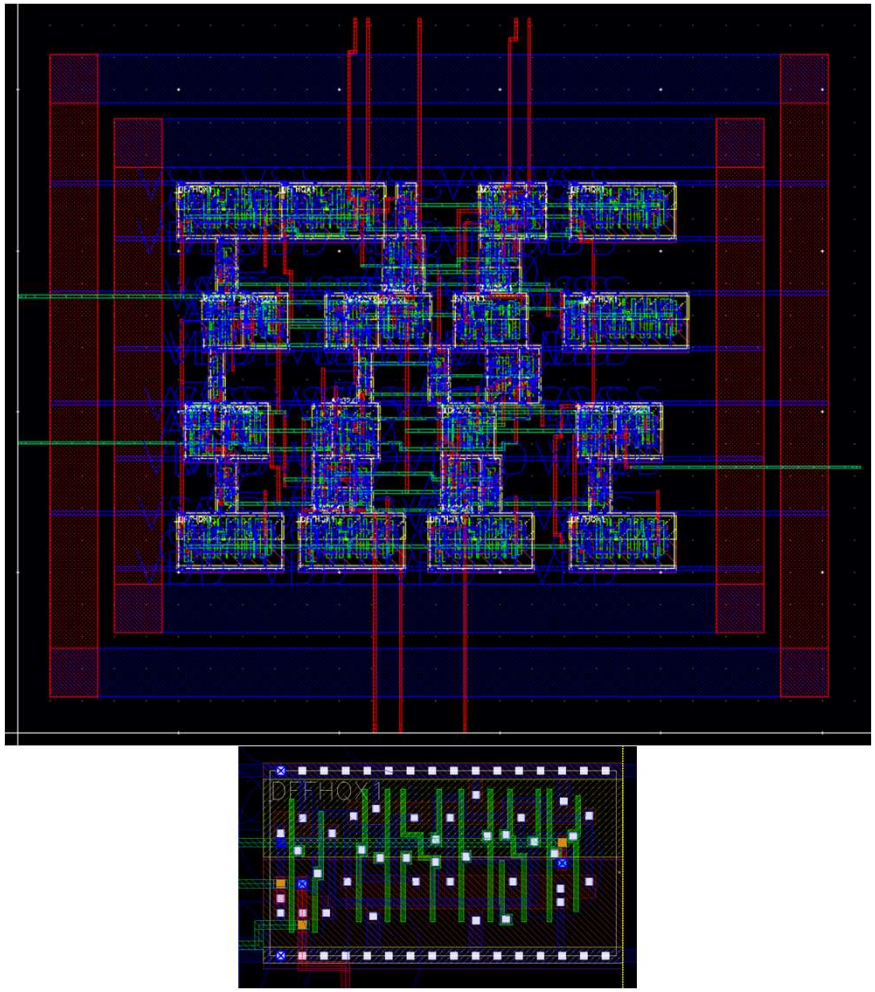
Specify layermap file.
This maps names of layers to GDS layer number and datatype.



Virtuoso: Post Place and Route

Highlight your library and notice how additional cells are generated from importing your layout. These cells are part of your layout. Open the layout to see the transistor level layout.





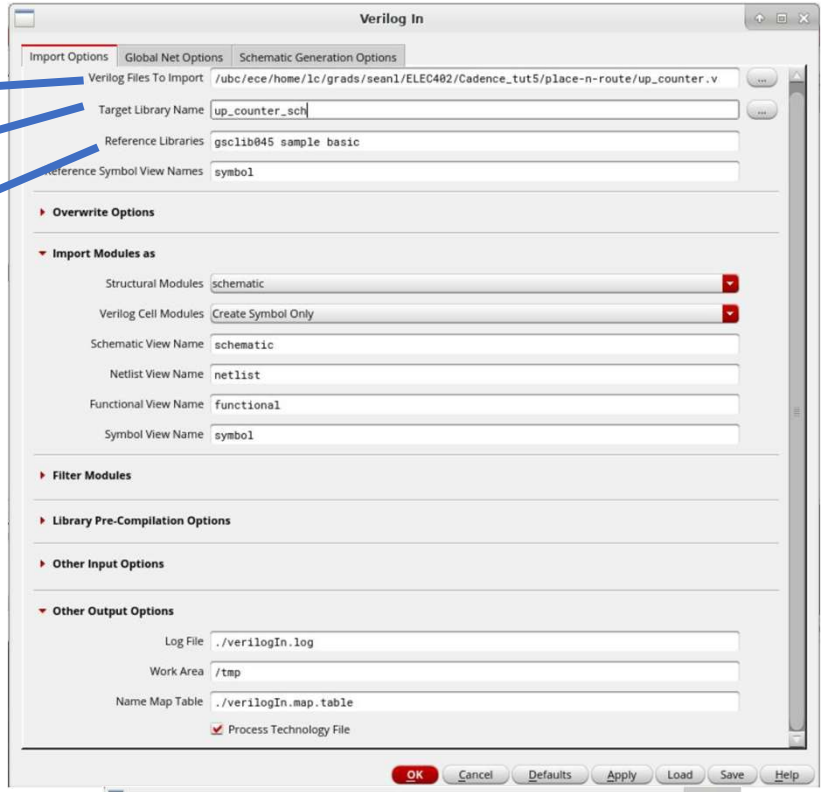
Virtuoso: Post Place and Route

To simulate your layout, we must import the generated Verilog file. From the CIW window, go to File→Import→Verilog.

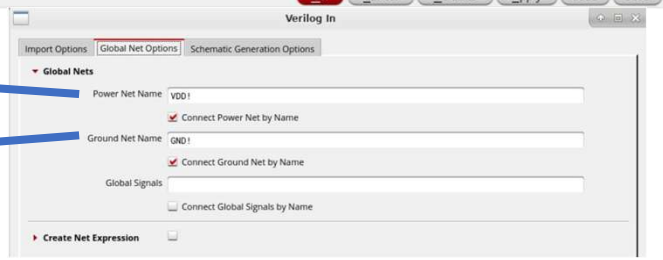
Verilog file from Innovus

New library to store imported Verilog

Ensure that gsclib045 is specified in reference libraries.

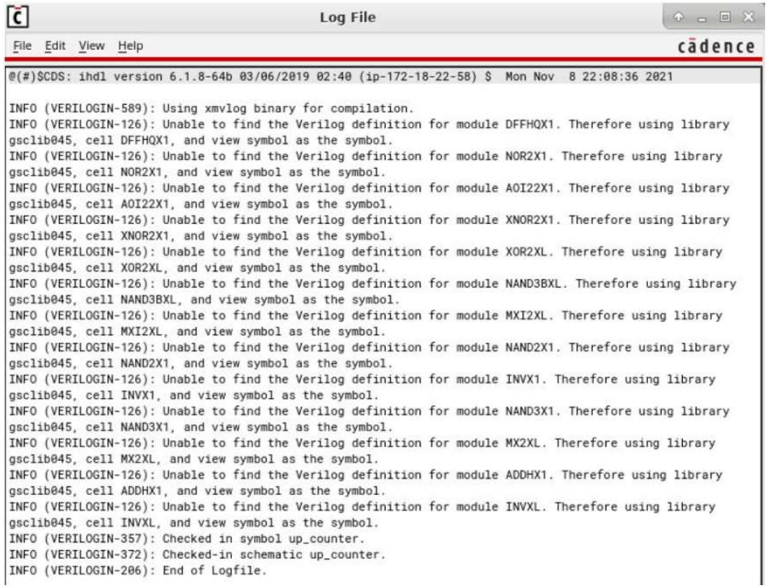


Ensure VDD and GND are named. The other cells do not have VDD and GND pins in their symbol, so they must connect to global nets.



Virtuoso: Post Place and Route

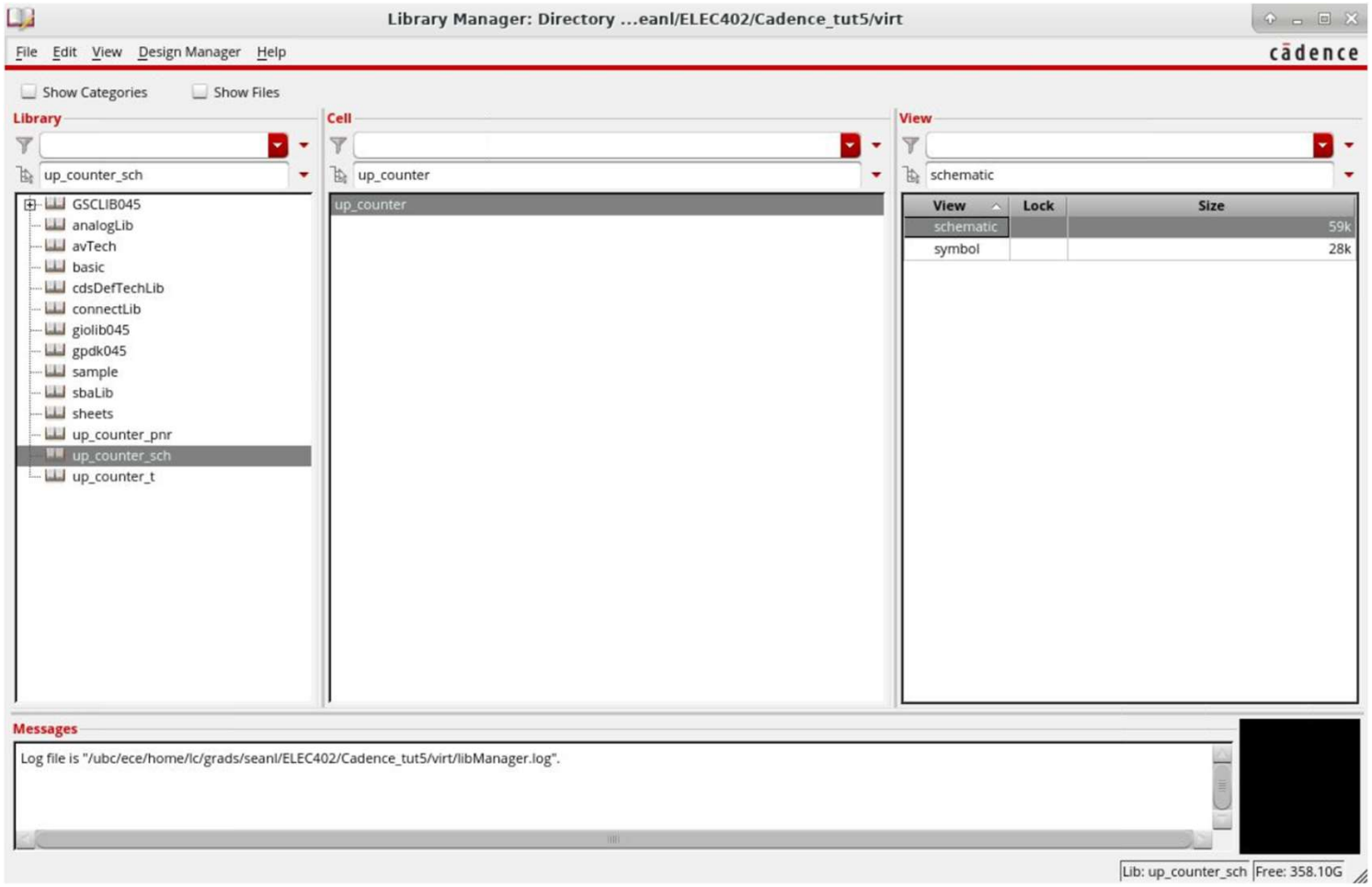
Import completion window should show.



NOTE: If you cannot import the Verilog file, close Virtuoso and source the following script, reopen Virtuoso, and import Verilog file.
>> source /CMC/scripts/kit.gpdk45_OA.csh

Virtuoso: Post Place and Route

Open the schematic to view the generated schematic that came from Verilog.



Virtuoso: Post Place and Route

Open the schematic and symbol to view the generated schematic and symbol that came from Verilog. You can place the symbol in your own testbench and simulate the circuit.