ELEC 402
Introduction to VLSI Systems
INFORMATION SHEET

Day/Time/Location: Tues and Thurs, 5:30 pm – 7 pm – Frank Forward 317 (In-person)
Work-in-progress to provide parallel zoom sessions. However, provided that lecture materials are presented in a mixture of powerpoint slides/Board notes, attending online session/material is only recommended when in-person attendance is not possible, e.g. you are sick).

INSTRUCTOR: Reza Molavi
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T.A.:
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Tutorials on Wed 10 am – 12 pm, join Piazza from Canvas!

Grading:

Assignment :	35% (Mini Projects and Assignments)
Midterm:	25%
Final:	40%
	(pass at least one exam to pass the course)

Textbook:
1) CMOS VLSI Design,4th edition, Neil Weste, David Harris
2) Digital Integrated Circuits: A design perspective, 2nd Edition, J. Rabaey
3) *Analysis and Design of Digital Integrated Circuits, In Deep Submicron*, D. Hodges, H. Jackson, R. Saleh, McGraw-Hill, 2004.

Other Useful References:
1) *CMOS Digital Integrated Circuits: Analysis and Design*, S. Kang and Y. Leblebici, 2nd Edition.
2) *Logical Effort: Designing Fast CMOS Circuits*, I. Sutherland, B.Sproull and D. Harris

Prerequisites: CPEN 311 or familiarity with circuits, digital logic, and SPICE. EECE 480 (Device physics) is useful but not mandatory.

Assignments: Hand in partially done homework by the due date. Generally, **no late homework** will be accepted.

Mini Projects: There are few projects in this course that would be handed out throughout the course. You must hand in the projects by the due date (Email TA). We

use EDA CAD tools such as Cadence to complete projects.

Tutorial Session: There will be tutorial sessions on Wednesday to review CAD tools (ModelSim, Cadence, Virtuoso, HSPICE).

Main Topics:

1. Into to VLSI Design
2. SystemVerilog RTL
3. MOS (device) Physics (current, capacitance, operation)
4. Inverter Topologies, Noise Margin
5. Inverter Delay
6. Static Logic Design
7. Standard Cell Design
8. Pass Transistor Logic
9. Dynamic Logic Design, Elmore delay
10. Sequential Circuit Design
11. Manufacturing / Layout
12. Power Consumption
13. Interconnects
14. Power Distribution, Chip Level Considerations

Additional Notes and suggestions:

For Zoom sessions enabled during in-person classes

- Please mute your microphone as it may pick up on background noises which will be distracting during the lecture.
- Please be aware while your instructor may be making a Zoom session available, they may not be able to monitor the Zoom Chat or Raise Hand feature. Live-streaming is being provided to aid students in staying up to date with course material if they cannot attend class, but it is not the primary mode of instruction.
- information about academic concessions, see the UBC policy here: http://www.calendar.ubc.ca/vancouver/index.cfm?tree=3,329,0,0

- Make a connection early in the term to another student or a group of students in the class so that you can ask what was missed if you are unable to attend lecture/tutorial.
- Consult the class resources on Canvas. We will post [all the slides, readings, recordings …] for each class day.
- Attend tutorials to learn about CAD tools which greatly helps your project/assignment delivery