# ELEC 402

# Dynamic Logic Design

## (Domino Logic)

## Lecture 13

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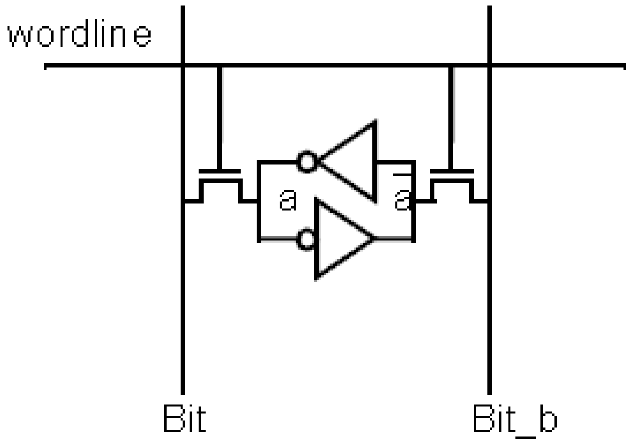
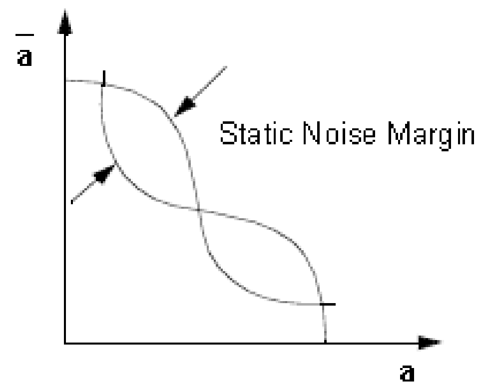
# Building a Storage Cell – SRAM Basic

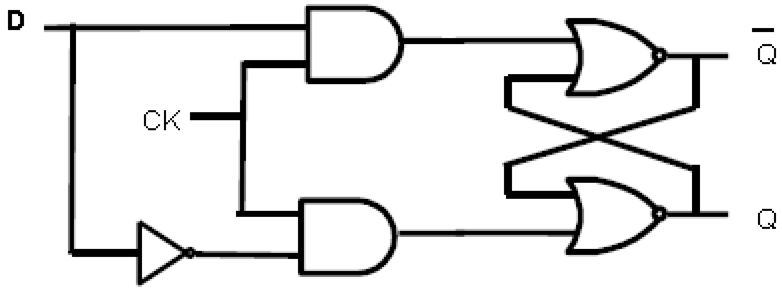
Uses only six transistors (called 6T cell):

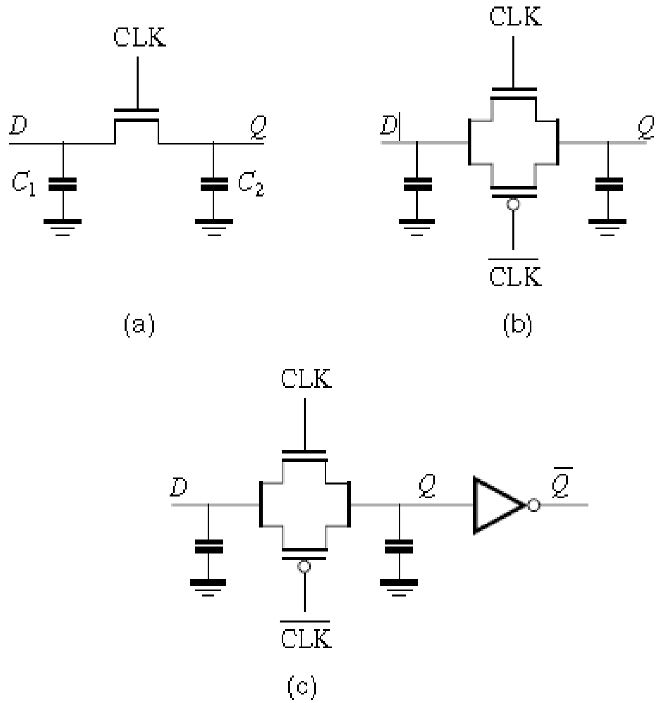



Read and write operations use the same port. There is one wordline and two bit lines. The bit lines carry complementary data. The cell layout is small since it has a small number of wires.

# Dynamic Latch




Remember D-latch from previous chapters

(main building block of sequential logic)

All three do D-latch, however they have several

Issues:

a) For D=1, output only reaches $V_{DD} – V_T$

- Clock feedthrough

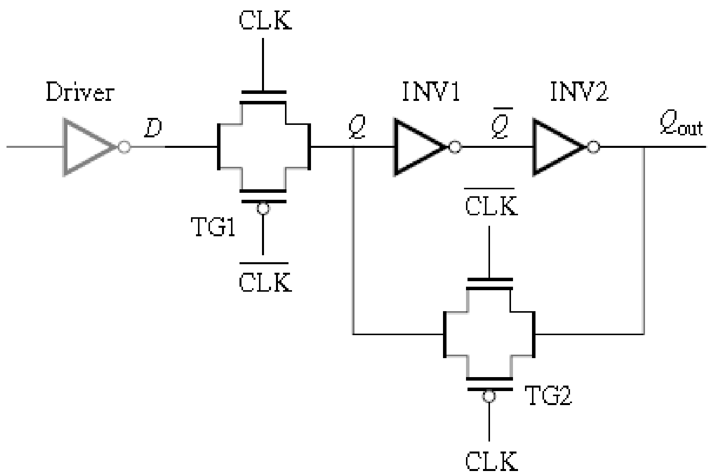
a) No complementary output!

b) still prone to all dynamic logic problems

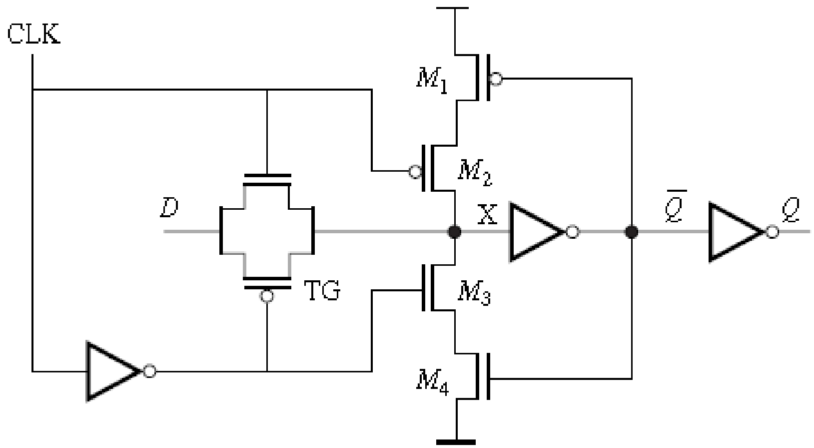
(leakage, cross-talk, etc)

- When clk is low, what can we do?

# Dynamic Latch - II

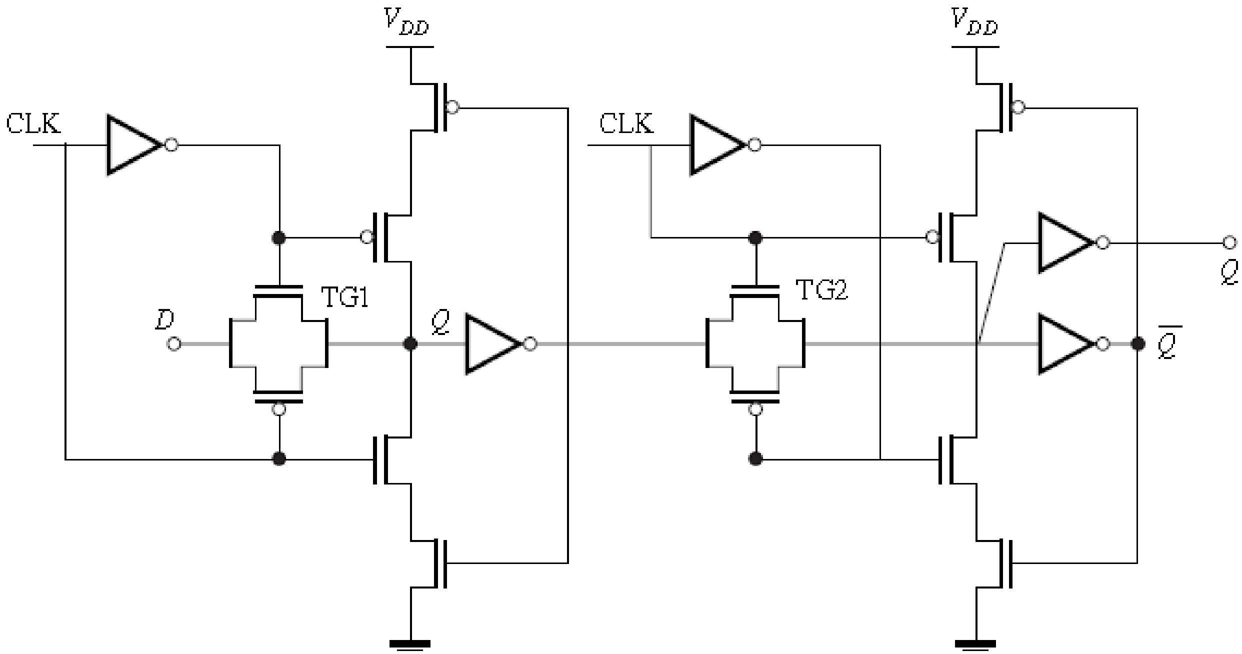



The feedback path ensures that the Value of Q is maintained while CLK = 0 (the feedback TG2 should be weak to avoid Conflict)




Another popular structure of D-latch (note that if X=Q=1, the pull-up path creates a Feedback and holds the value and if X=Q=0, the Pull-down path is responsible for the feedback)

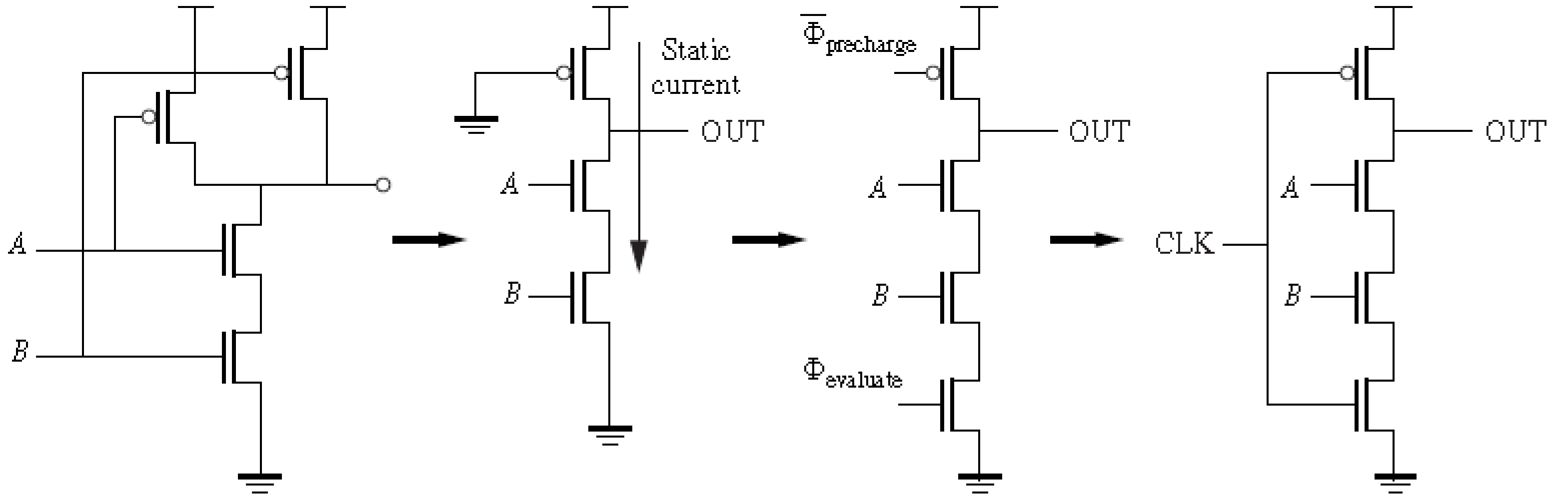
# Dynamic D FF (Master-Slave)




"Positive edge-triggered Master-Slave D Flip-flop"

When the clock goes high, the Master latch shuts-off and holds its value at internal Q while the slave latch becomes transparent and passes the Q to the output, the overall action is sampling D at this moment (rising edge of CLK)

# Dynamic Logic vs. Static Logic




CMOS — Psuedo-NMOS — Dynamic — Single clock dynamic

Pseudo NMOS has only one pull-up device but consumes static power, why not turn it off then?

Dynamic logic uses similar structure to pseudo-NMOS (an extra foot NMOS), using a CLK

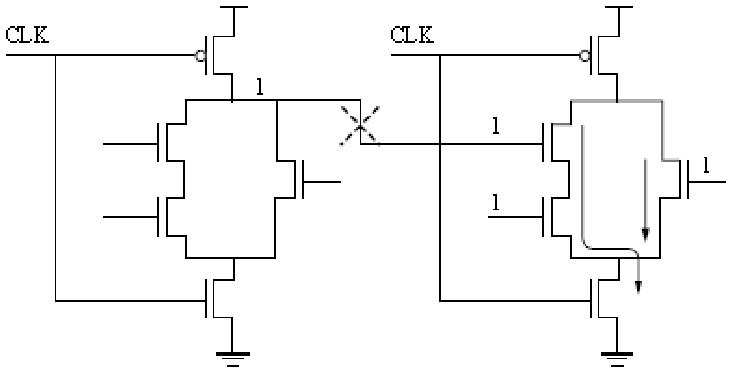
During the pre-charge phase, PMOS pulls-up the OUT, during evaluation phase the pull-down

Network gets activated and decides whether to discharge OUT (or not).

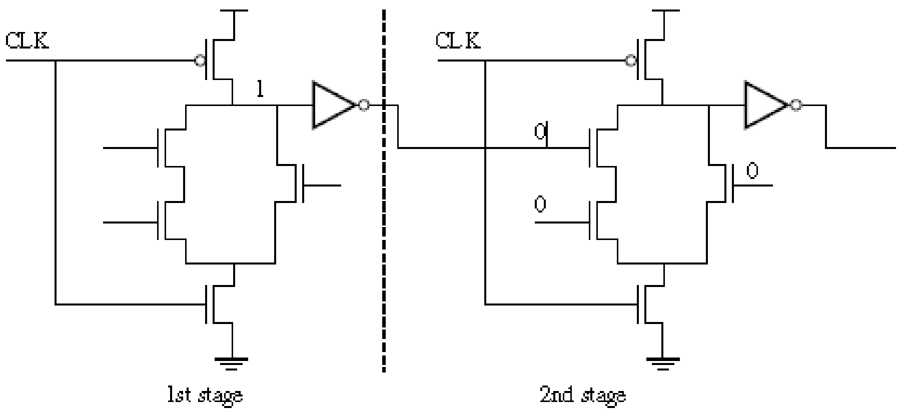
# Design using Dynamic Logic - Example

Implement a 3-input NOR gate in dynamic logic and explain its operation. Size the transistors to deliver the same delays as a conventional CMOS inverter (PMOS $8\lambda{:}2\lambda$, NMOS $4\lambda{:}2\lambda$).

# Domino Logic




(a) Direct connection not possible




(b) Insert inverter between dynamic gates

In dynamic logic every output node

Is pre-charged to $V_{dd}$, therefore, a direct

connection between cascaded stages

causes malfunction (during the evaluation

it always goes low

To avoid the issue we define the logic as

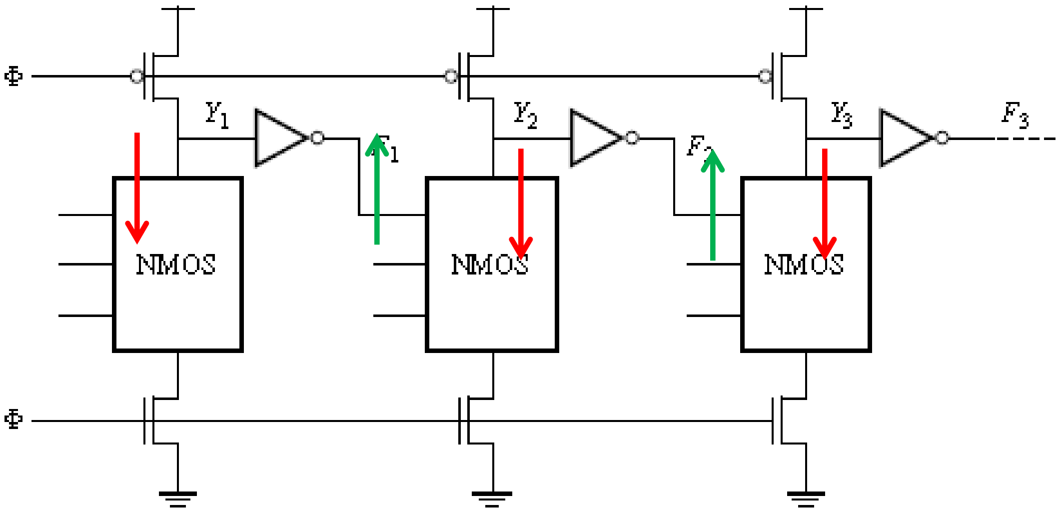
dynamic logic+inverter, therefore after

Precharge all inputs are low, this is called

Domino logic

- Only for non-inverting functions

# Cascaded Domino Logics

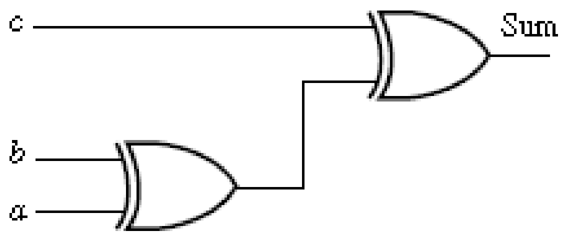



When several domino stages are put in series

The output nodes fall in order similar to domino game!

# Domino Logic - Example

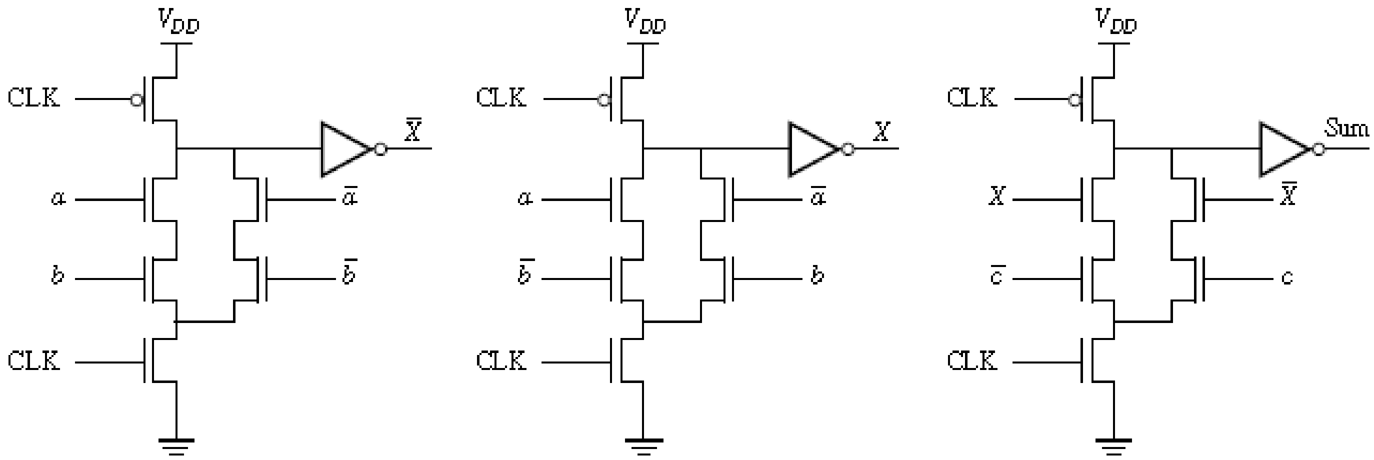
Implement the function $sum = a \oplus b \oplus c$ in domino logic. Assume that the literals $a, \overline{a}, b, \overline{b}$ are available as stable inputs to the gates.



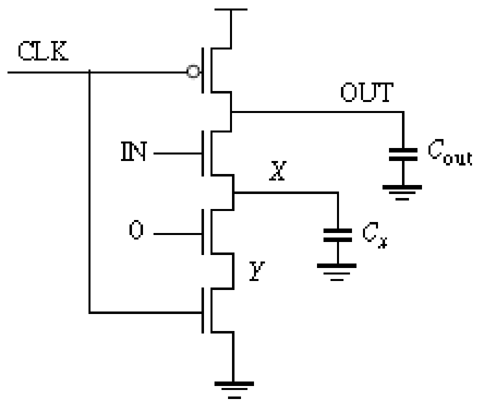

$$X = a \oplus b = a\overline{b} + \overline{a}b$$

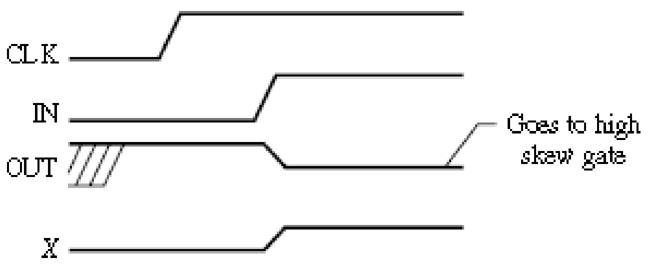
$$\overline{X} = \overline{a \oplus b} = ab + \overline{a}\,\overline{b}$$

$$\text{Sum} = c \oplus X = c\overline{X} + \overline{c}X$$



# Domino Logic - issues




Through the evaluation phase, imagine there is no pull-down path, however, there are some

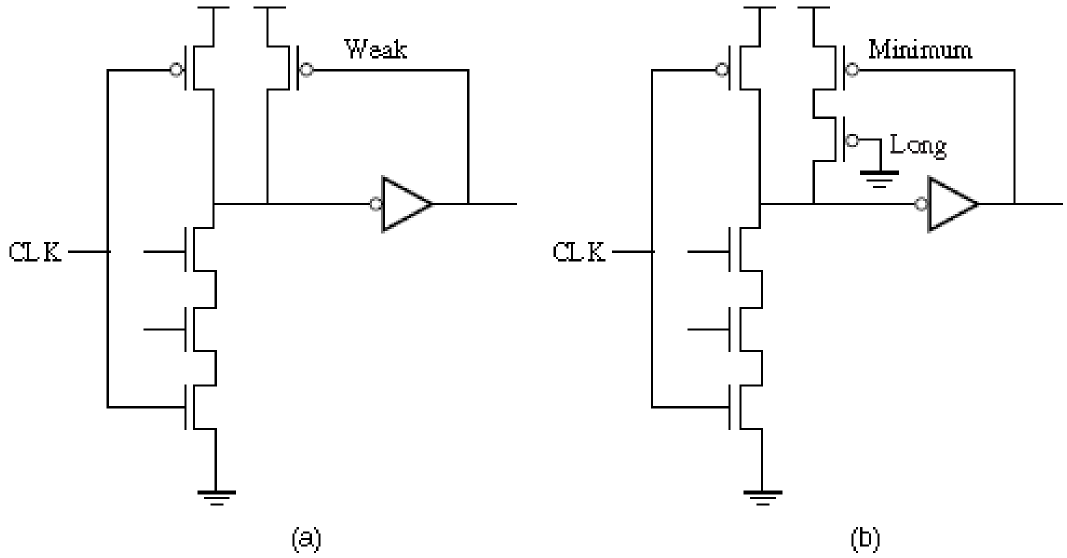
On Transistors, Charge sharing can potentially lower the output voltage below the

Threshold voltage of the subsequent inverter and fail the gate, there are several remedies

1. Increases Cap at OUT

2. skew the inverter

# Keeper cell in Domino Logic




A Popular remedy is to place a weak pull-up transistor connected to the output

This will supply the required charge during the evaluation phase.

To avoid large loading on the inverter we can place two transistors in series

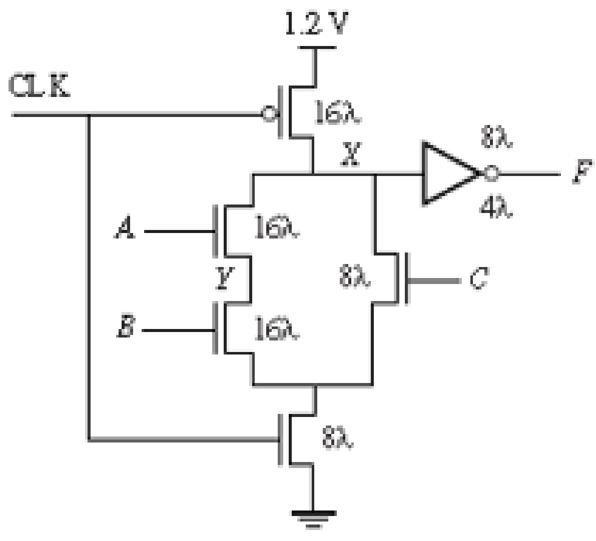
# Domino Logic - Example

For the domino function shown below, assume 45 nm technology parameters and answer the following questions:

a) What functions does the gate perform at the output F

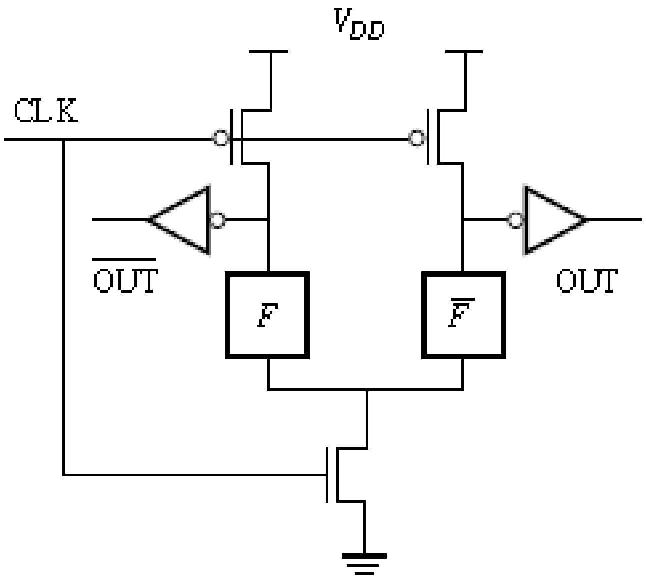
b) How much clock feedthrough do we observe at the internal node X? is this a potential problem?

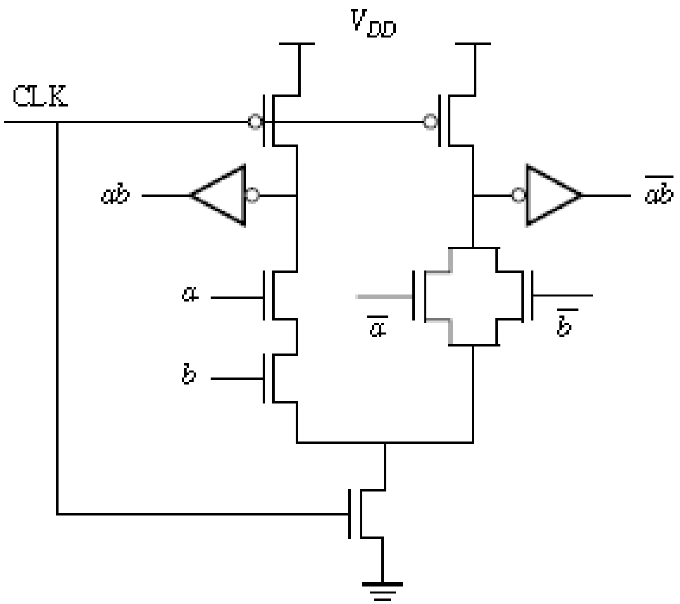
c) What is the worst-case charge sharing that we observe at node X?



# Domino Logic - Example

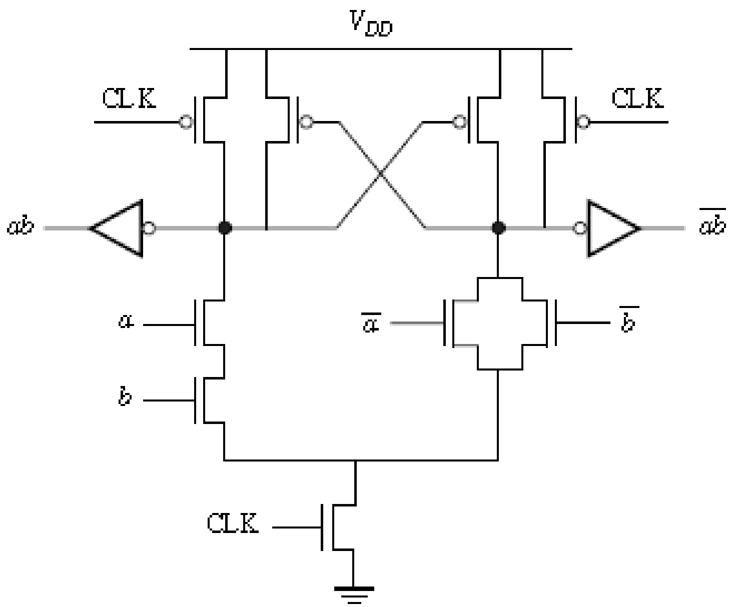
# Differential Domino Logic

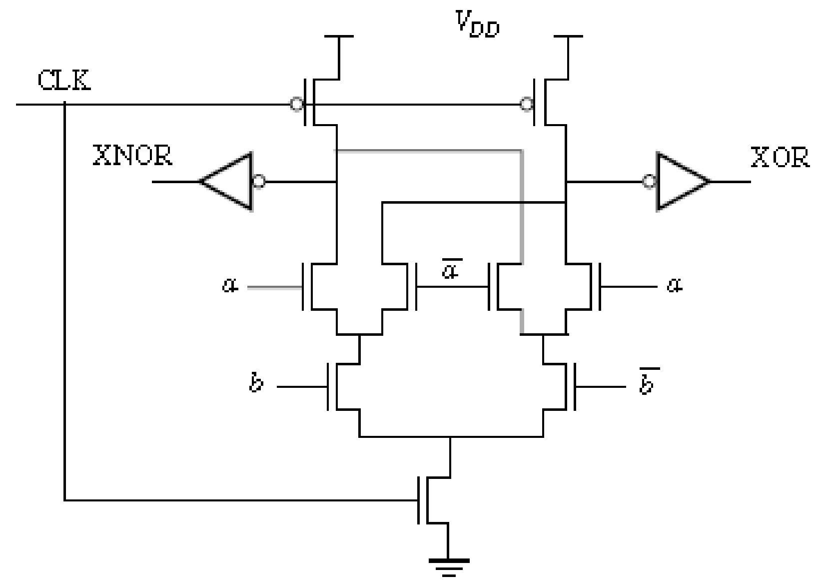



To overcome the problem of non-inverting output we can adopt the differential architecture

# Improved Differential Domino Logic




Differential Architecture helps reduce the devices for both

1. Keeper cells 2. Pull-down paths