ELEC 402

Delay in CMOS circuit
Lecture 8

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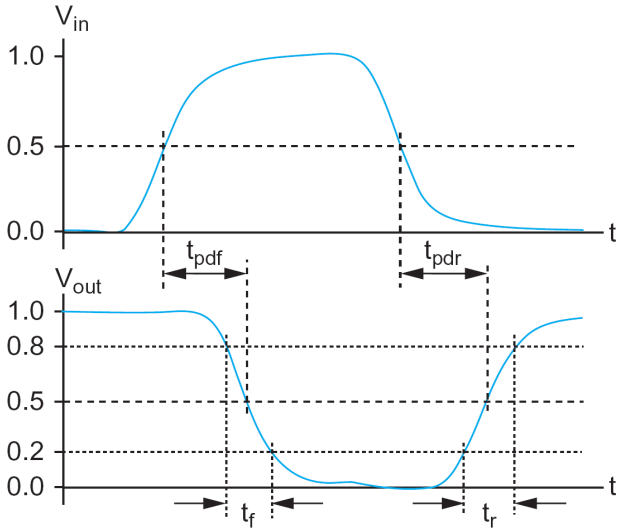
Slides Courtesy : Dr. Res Saleh (UBC), Dr. Sudip Shekhar (UBC)

Different Delay Definitions



"Delay" → t_{pd}
Max-time → Propagation time
Min-time → Contamination time

Rise Time (t_r, t_{LH}): time taken to rise from 10% to 90% (sometimes 20% to 80%) **Fall Time (t_f, t_{HL})**: time taken to drop from 90% to 10% (sometimes 80% to 20%) **Edge Rate (t_{rf})**: $(t_r + t_f)/2$.

Rise propagation delay (t_{pdr}, t_{pLH}): maximum time from the input crossing 50% to output crossing 50%, with output rising

Fall propagation delay (t_{pdf}, t_{pHL}): maximum time from the input crossing 50% to output crossing 50%, with output falling

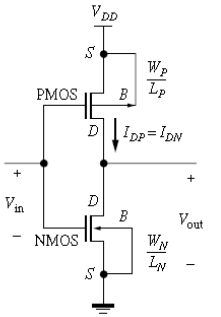
Propagation Delay (t_{pd}): $(t_{pHL} + t_{pLH})/2$.

Contamination Delay (t_{cd}): minimum time from the input crossing 50% to the output crossing 50%.

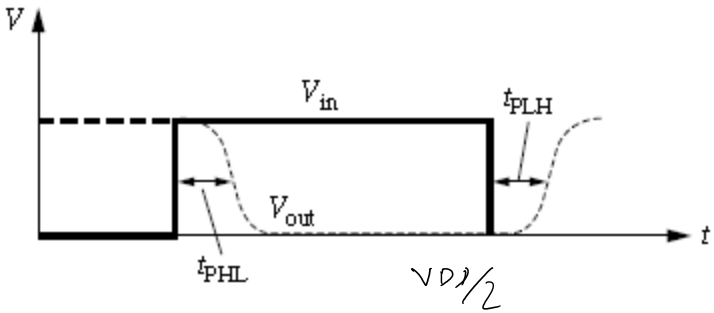
Inverter – Sizing

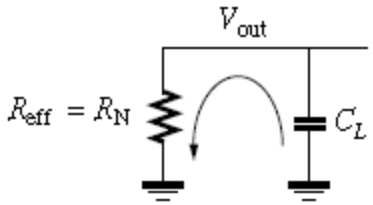
- In ratioed logic families (such as diode-connected load or pseudo NMOS, V_{OL} is a priority so the Size of load is mainly determined by the choice of V_{OL}

- In non-ratioed logic families (such CMOS inverters) propagation delay is important



Speed





Pull-down (output capacitor discharge)

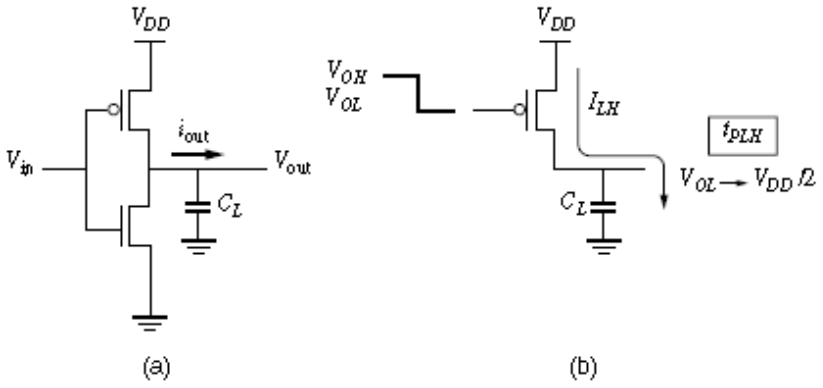
through the NMOS transistor

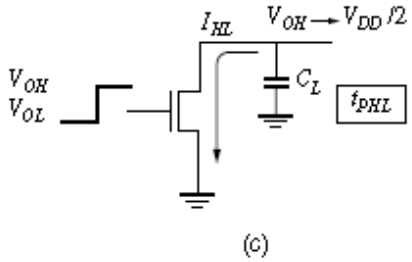
$$V_{out}(t) = V_{DD}\, e^{-t/R_N C_L}$$

T_{PHL} is the time it take for the capacitor to discharge to 50% of the final value

(Board notes)

Effective Resistance Calculations





Calculate the delay from the charge/discharge of capacitor

$$I = C_L \frac{dV}{dt} \rightarrow \Delta t \approx \frac{C_L \Delta V}{I_{DS}}$$

$$t_{PHL} = \frac{C_L (V_{DD}/2)}{I_{HL}}$$

Assuming **45 nm process**: VDD = 1 V, V_T = 0.35 V, and E_cL = 0.3 V

$$\text{Vdsat} = \frac{(1-0.35)(0.3)}{(1-0.35+0.3)} \sim 0.2\ V$$

Since for T_{pHL} V_{out} changes from V_{DD} to $V_{DD}/2$ ⇒ $t_{PHL} = \frac{C_L (V_{DD}/2)}{(I_{Dsat})_n}$ $R_N = \frac{V_{DD}/2}{0.7(I_{Dsat})_n}$

NMOS remains in Saturation throughout T_{PHL} , i.e. $I_{HL} = I_{dsat}$

equivalent resistance

Inverter – Resistance

-The value of T_{PHL} or T_{PLH} determine the value of the resistor (average on-resistance)

• Note that in the pull-down case (NMOS on) device starts in saturation (V_{DD} across its V_{DS} and might enter triode at some point, therefore it makes sense to define an effective resistance

• This **effective resistance** is inversely proportional to W/L for long channel devices (motivates a $R_{\square}$ value) while it is inversely proportional to W in short channel devices (motivates a kΩ.µm number for transistors)

note the ration 2 or 2.4 between NMOS and PMOS, does this remind you of a Particular property?

45 nm

$R_n = R_{n\_unit} / W$

$R_p = R_{p\_unit} / W$

$R_{n\_unit} = 34\ k\Omega.\ \mu m$

$R_{p\_unit} = 68\ k\Omega.\ \mu m$

130 nm

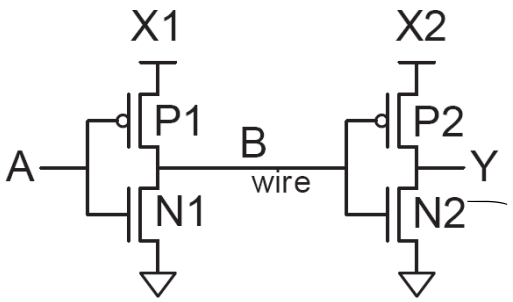
$$R_N = R_{eqn} \times \frac{L_N}{W_N}$$

$$R_P = R_{eqp} \times \frac{L_p}{W_p}$$

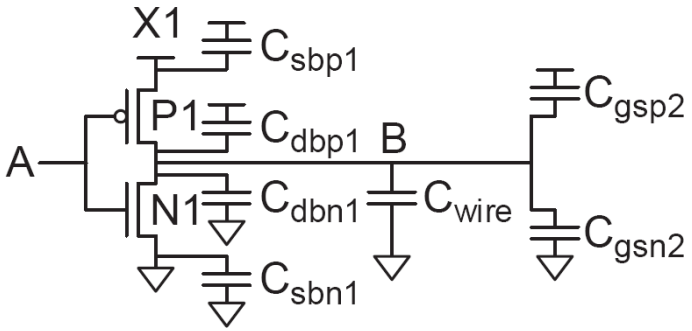
$R_{eqn} = 12.5\ k\Omega/\square$

$R_{eqp} = 30\ k\Omega/\square$

Inverter- Capacitances

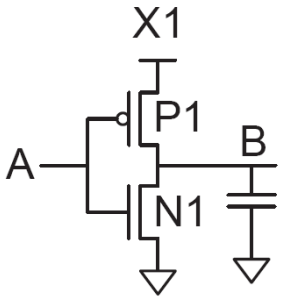


One inverter driving another



Showing all capacitances

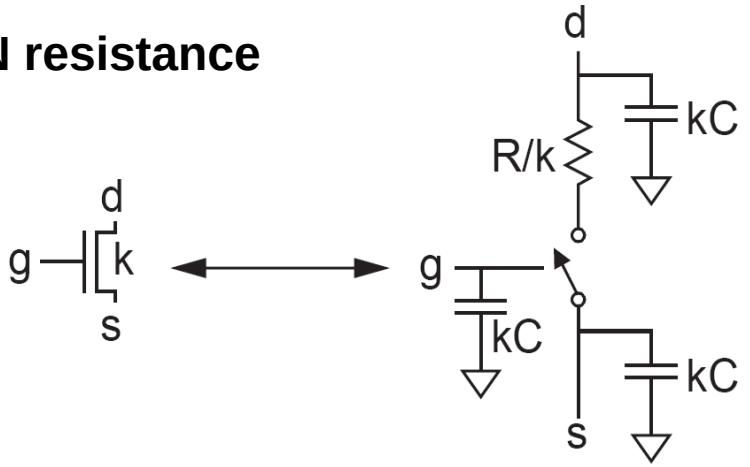
Capacitance relevant for delay calculation, i.e.
Sum of all capacitance at the output of first inverter



$C_{out} = C_{dbn1} + C_{dbp1} + C_{wire} + C_{gsn2} + C_{gsp2}$

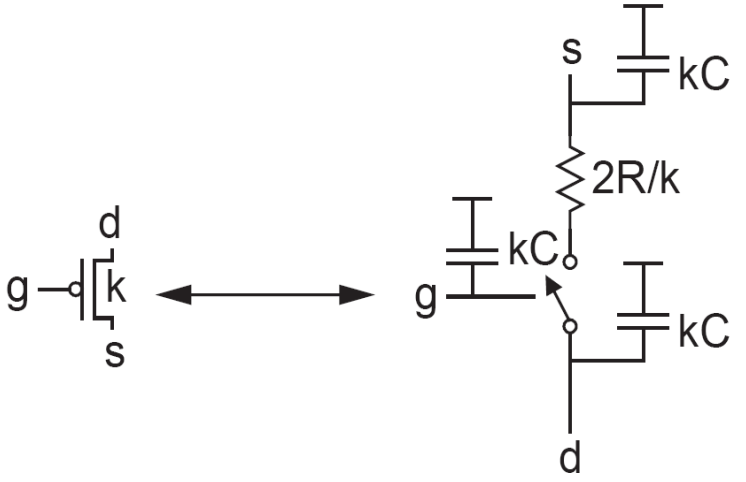
Equivalent Circuits for Transistors

- **MOS transistor == Ideal switch + cap and ON resistance**
- **Unit nMOS has res R, cap C**
- **Unit pMOS has res 2R, cap C**
- **Cap proportional to width**
- **Res inversely proportional to width**



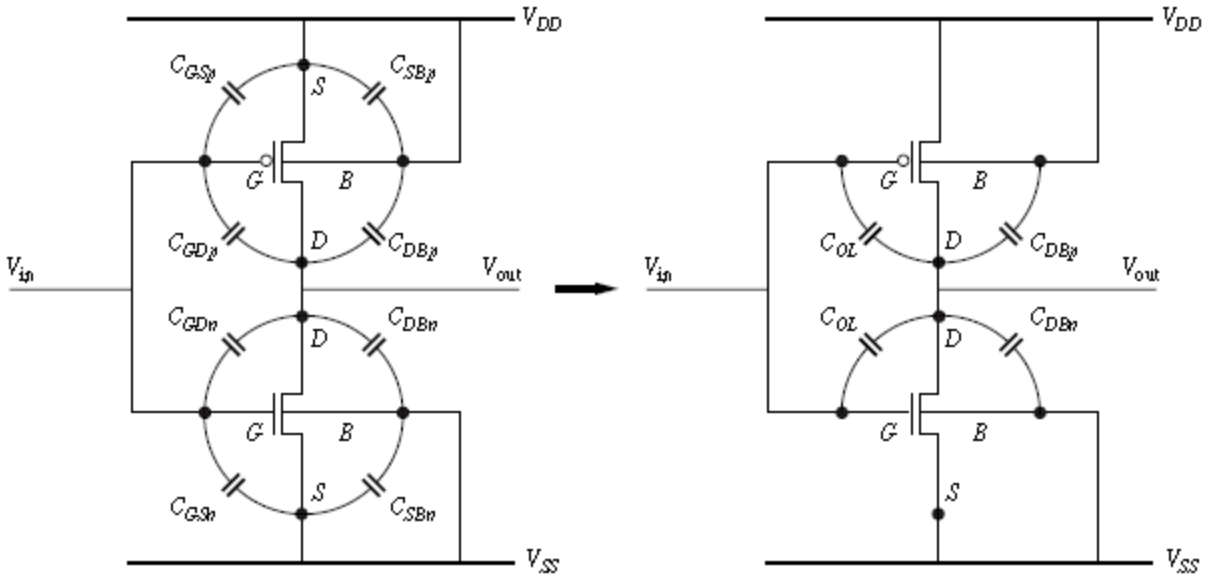
- **Some capacitances may be shorted!**

- **Capacitance**
  - **$C = C_g = C_s = C_d = 2$ fF/μm of gate width before 65 nm**
  - **Gradually decline to 1 fF/μm in 65 nm and below**



Load Capacitance Calculations

"Self Capacitance"



$C_{GDp,n} = C_{ol}$ (?)

Another term in load caclulations is the load presented by

The driver itself (all capacitances connected to V_{out})

We have to consider Miller effect! In calculating C_{self}

$$C_{self} = C_{DBn} + C_{DBp} + 2C_{OL} + 2C_{OL}$$

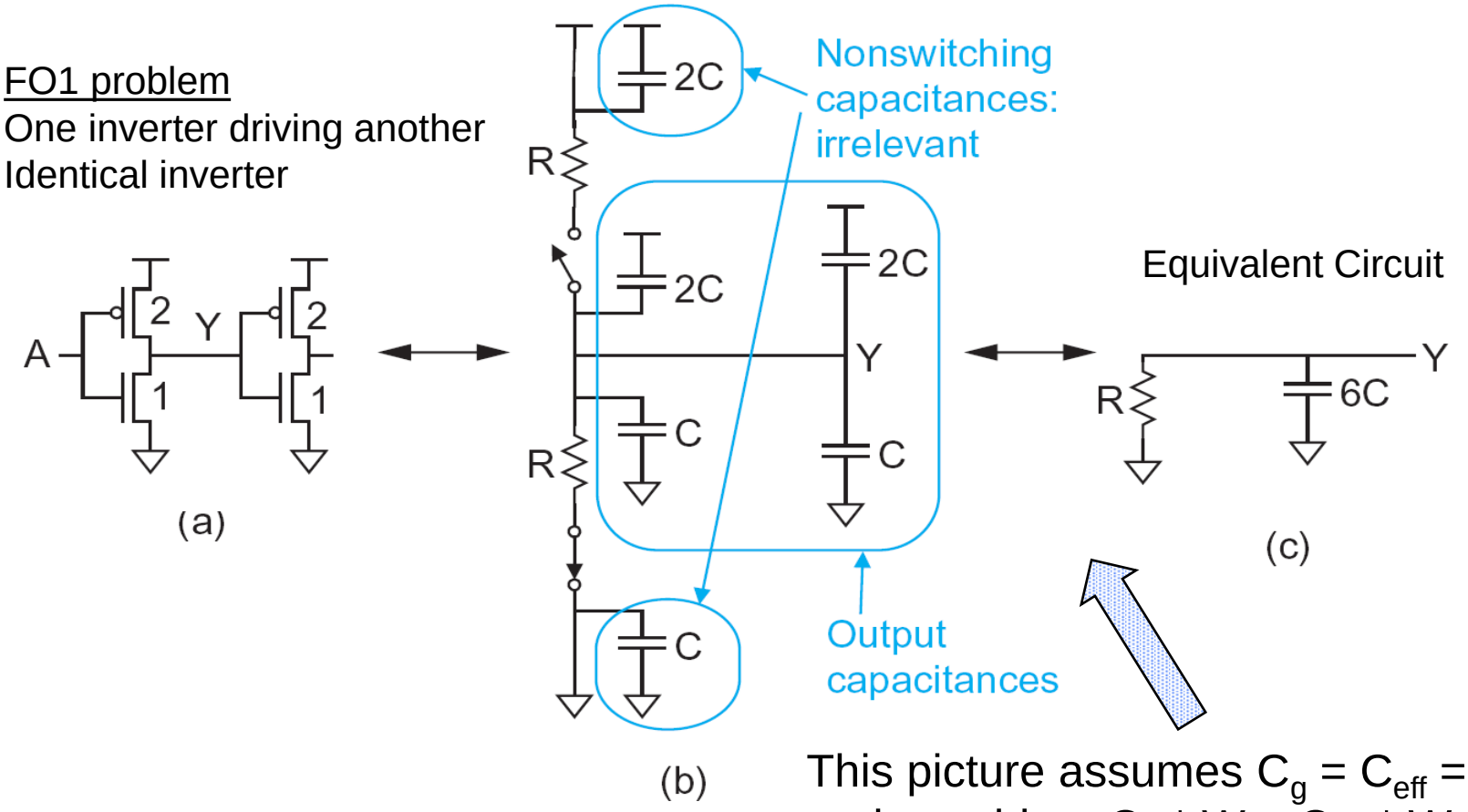
$$= C_{jn}W_n + C_{jp}W_p + 2C_{ol}(W_n + W_p)$$

$$= C_{eff}(W_n + W_p)$$

(Board Notes)

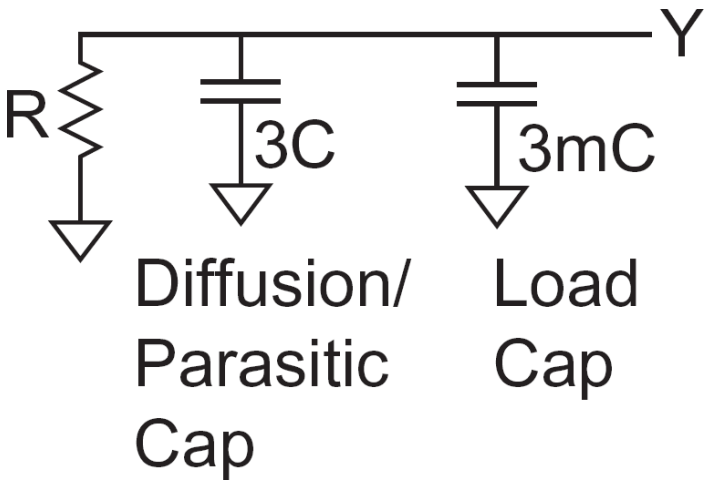
FO1 Inv

FO1 problem
One inverter driving another
Identical inverter

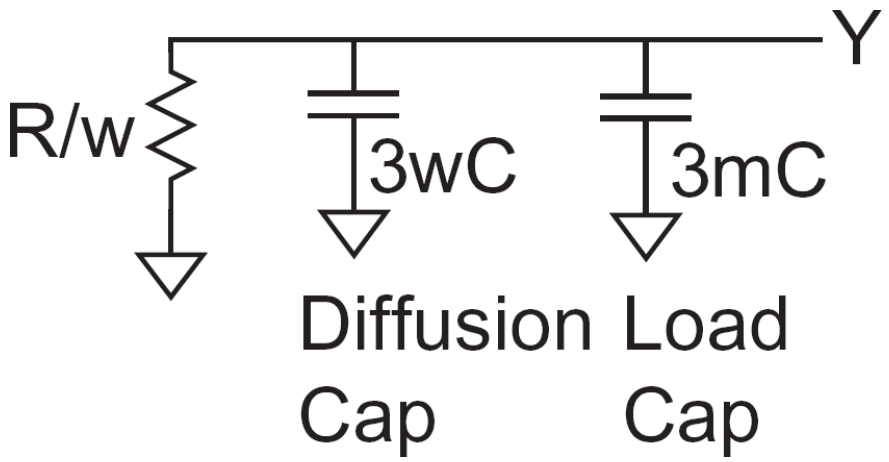


This picture assumes $C_g = C_{eff} = 1$ fF/um
and considers $C_g * W = C_{eff} * W = C$

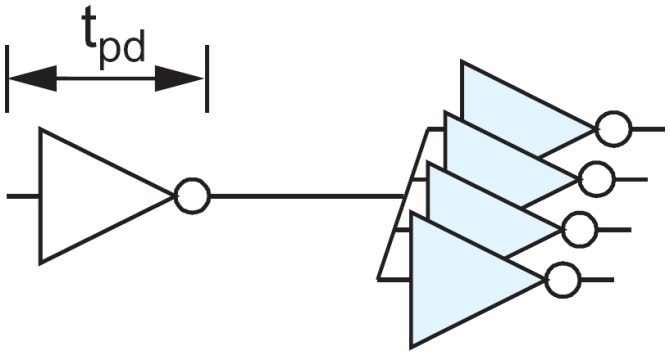
FO4 & FO*M*

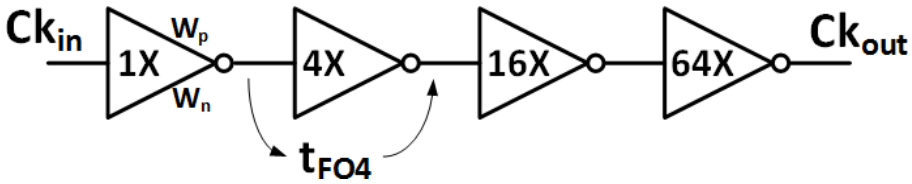


FO*M* Inverter Loading



FO*M* Loading w/ wider Driver





FO*4* Inverter Delay ~ 5 - 15ps (FinFET devices are extremely fast)

Delay Calculation - Example

If a unit transistor has R = 10 kΩ and C = 0.1 fF in a 65 nm process, compute the delay in the picoseconds of the inverter shown below with a fanout of 4?