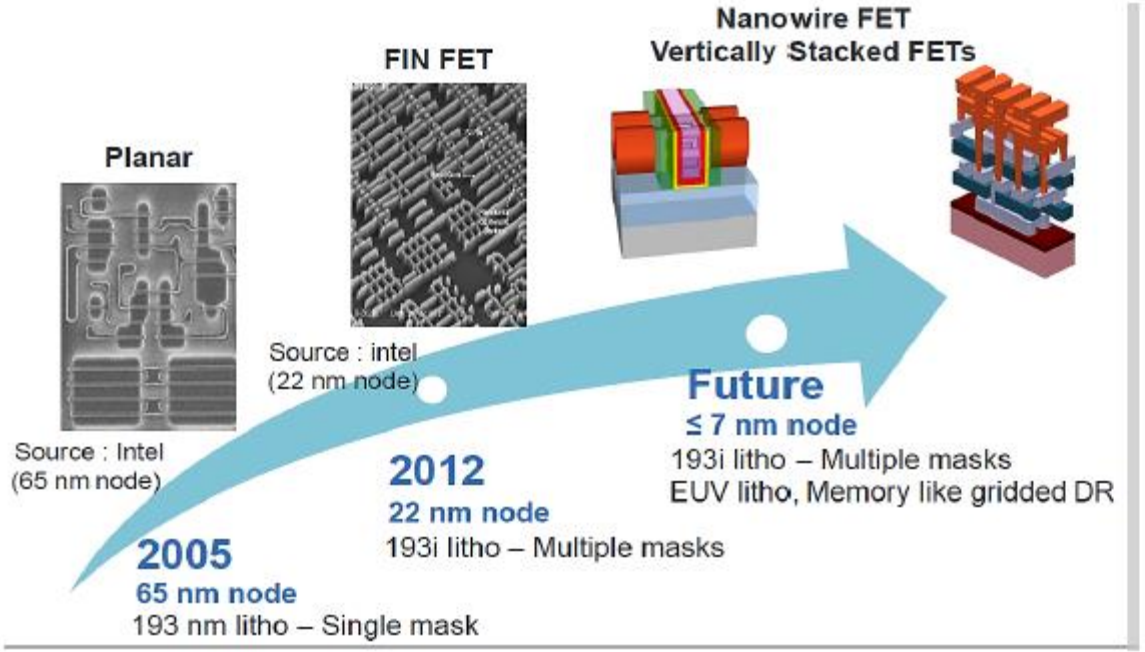
# ELEC 402
# FinFET

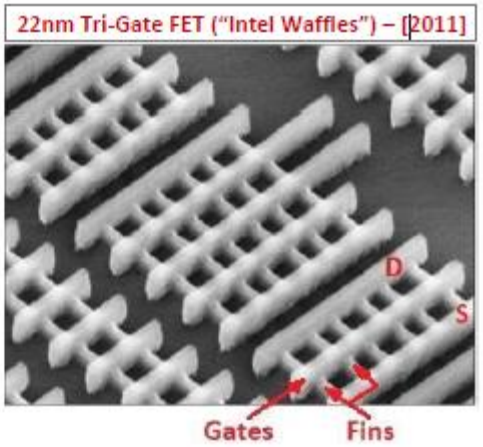
Reza Molavi
Dept. of ECE
University of British Columbia
reza@ece.ubc.ca

Slides Courtesy : Dr. Hormoz Djahanshahi (Microchip)

# Evolution of MOSFET devices

- **Evolution of MOSFET**: From Planar MOSFET to Tri-Gate FET/FinFET, to Nanowires and Vertically Stacked FinFETs (VFET)



# Motivation

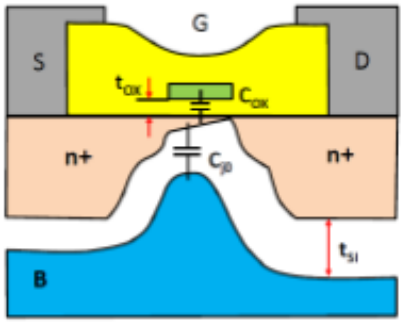
- I-V relation of the MOSFET in Subthreshold is exponential

$$I_{D(sub-th)} \cong I_{D0}\left(\frac{W}{L}\right)e^{(qV_{eff}/nkT)}$$

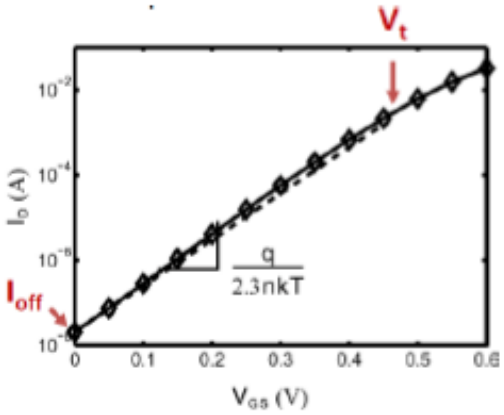
$$V_{eff} = V_{GS} - V_t$$

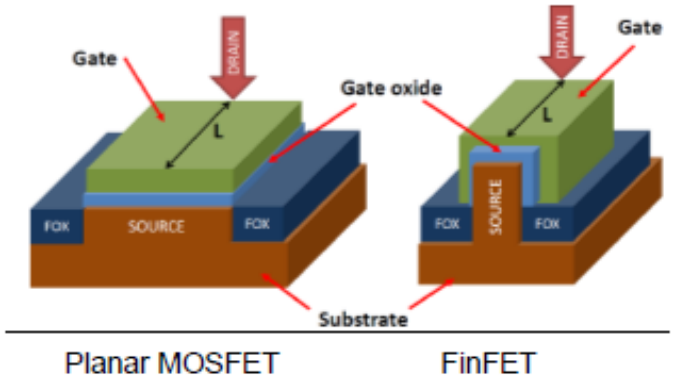
- We want a steep slope for I-V curve in sub-threshold
  - i.e. a large ION/IOFF ratio
- What determines the subthreshold slope is 1/n
  - n = (Cox+Cj0)/Cox ≈ 1.5 … (in Planar MOSFET)
- Planar channel is not completely under Gate's control
  - Smaller Cj0 means smaller n and steeper slope
  - Better electrostatic control on the channel, higher ION/IOFF

- FinFET geometry reduces Cj0 relative to Cox, hence reduces n
  - Improves subthreshold slope: higher ION/IOFF ratio
  - Reduces Body Effect
    - Modulation of Vth by Bulk voltage
  - Reduces DIBL (Drain-Induced Barrier Lowering)
    - Modulation (reduction) of Vth at high VDS




$$n = \frac{C_{ox} + C_{j0}}{C_{ox}}$$

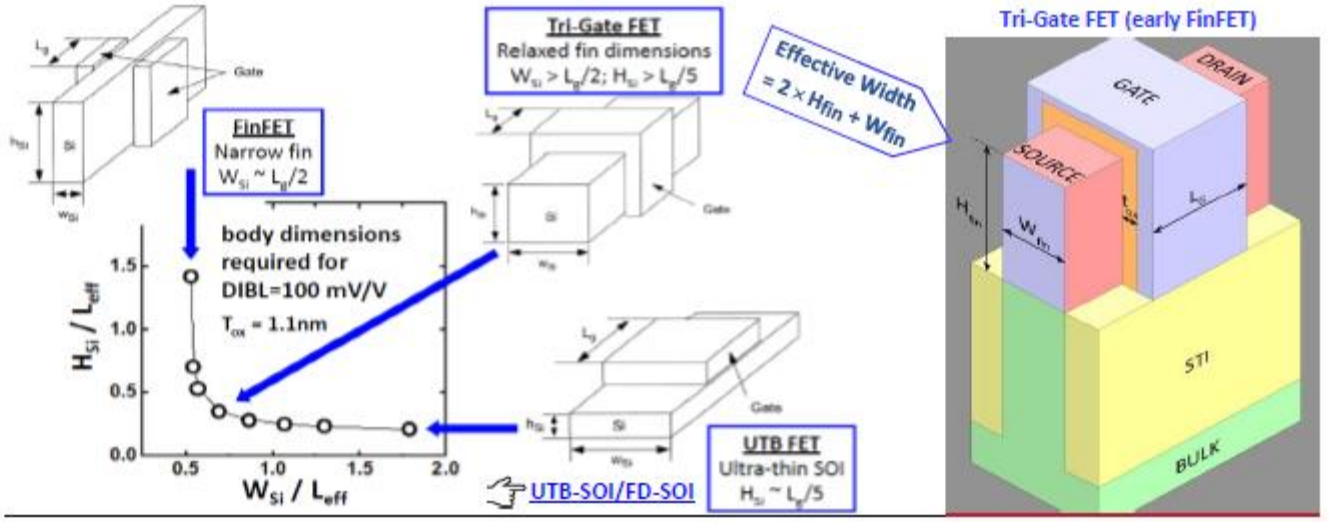


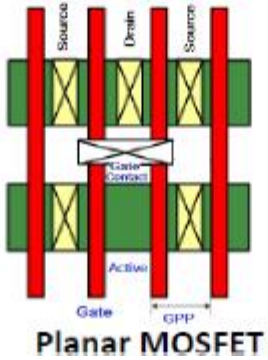




Courtesy of Tony C. Carusone, Univ. of Toronto, CMC Workshop, Toronto, Canada, December 2018

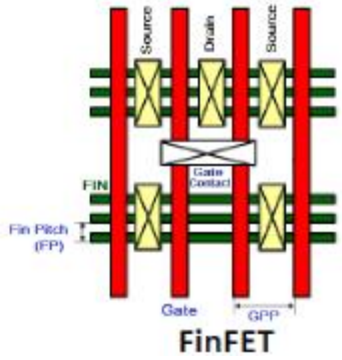
# Planar vs. FinFET

- Solutions for better Electrostatic control of MOSFET channel

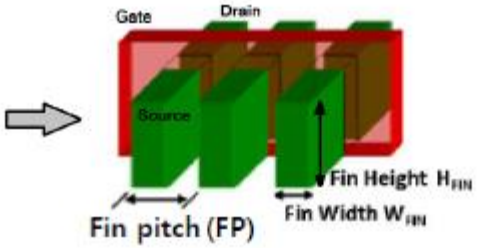



Planar MOSFET

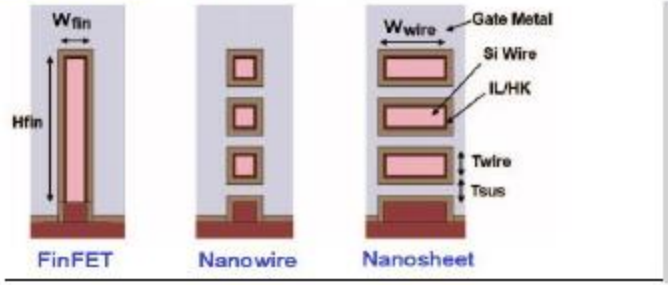



FinFET



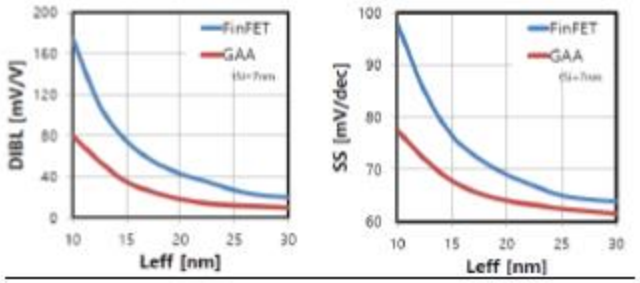
# FinFET Evolution

- **FinFET Evolution** – GAA (Gate All-Around): Horizontal Nanowire/ Nanosheet, Stacked Nanowire/ Nanosheet, Vertical Nanowire

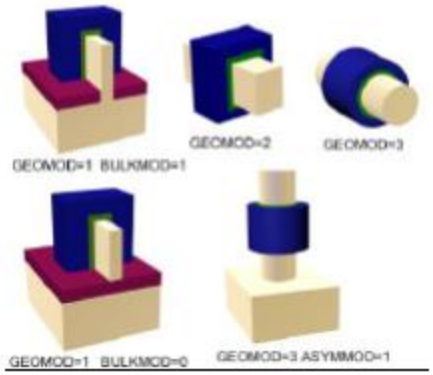




- GAA: Superior electrostatic control over channel
  - Lower DIBL ($\Delta V_{TH}/\Delta V_{DS} \leq$ **80 mV/V**)
  - Improved Subthreshold Swing (SS)
  - Lower $I_{DS,OFF}$
  - :

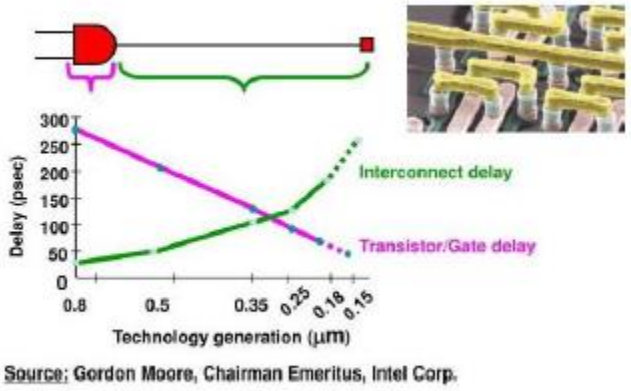



- *BSIM CMG* (Compact model for Multi-Gate transistors) supports different FinFETs and GAA FETs
  - GEOMOD selects the gate-channel geometry
  - BULKMOD selects the substrate (SOI or Bulk)
  - ASYMMOD enables an asymmetric I-V



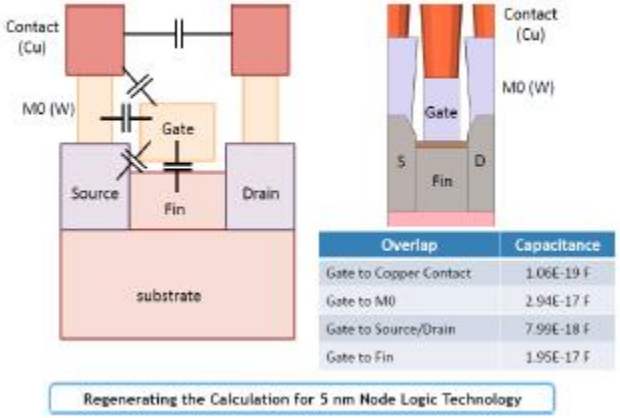
# Interconnect Challenge

- **Interconnect Scaling**: The struggle to keep scaling BEOL, and what we can do next
  *[IEDM'16 Tutorial 1, by GF]*
  - Scaling the metallization, a.k.a. Back-End Of Line - **BEOL**, limiting the circuit performance
    - Interconnect **RC** dominates vs. transistor or gate delay … (old prediction comes true)
  - *Physics limitations*: Narrower wire has **more R**; tightly spaced/stacked wires have **more C**
    - What we do to improve C tends to degrade Reliability; what we do to improve R tends to worsen EM



Source: Gordon Moore, Chairman Emeritus, Intel Corp.

- FinFET's 2.5D structure creates/augments many parasitic capacitance components
  - e.g. ~2-3x gate capacitance and output capacitance compared to planar




| Overlap | Capacitance |
|---|---|
| Gate to Copper Contact | 1.06E-19 F |
| Gate to M0 | 2.94E-17 F |
| Gate to Source/Drain | 7.99E-18 F |
| Gate to Fin | 1.95E-17 F |

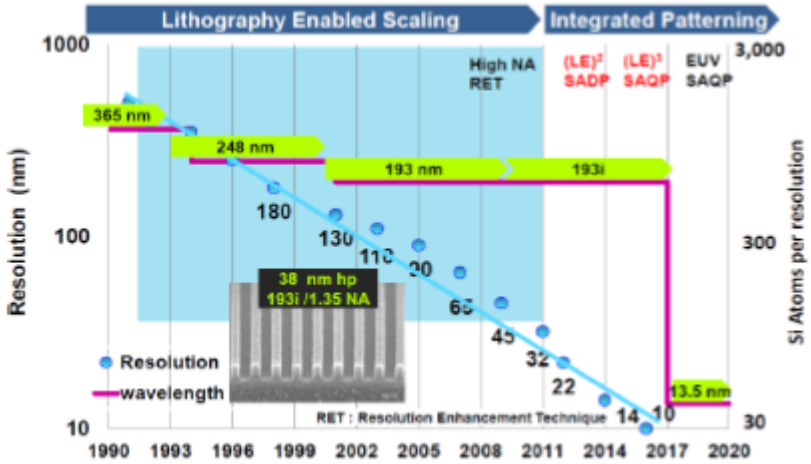
Regenerating the Calculation for 5 nm Node Logic Technology

# Fabrication Technology

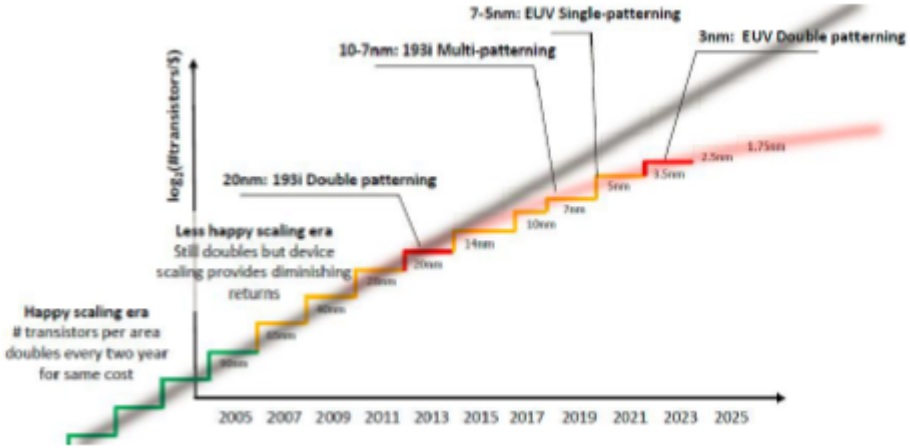
- **Patterning Technology Towards N5**

*[IEDM'16 Short Course: Technology Options at 5 nm Node, Pt. 1, Tokyo Electron]*

- **193i**: Existing Immersion Lithography (enhanced in water)
  - → λ = 193nm used since 0.13 μm node
  - → 193i (immersion) since ~45 nm node
  - → Double- or Quad-Patterning since ~22nm
- **EUV**: Ultraviolet w/ Extreme (short) wavelength
  - → λ = 13.5 nm, single patterning
  - → Multi-patterning and layout coloring goes away

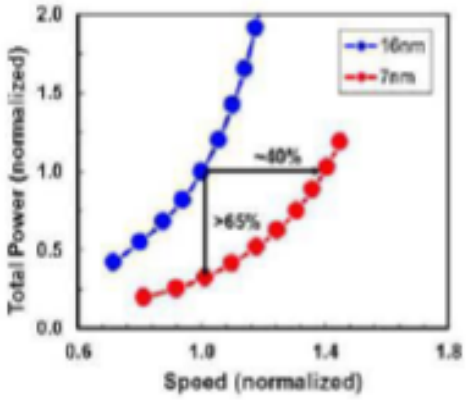


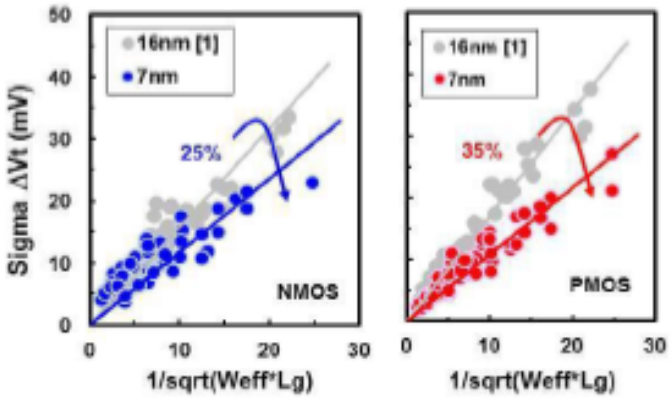

- Dimensional Scaling under pressure since ~22nm node
- EUV lithography replacing 193i Self-Aligned Double/Quad Patterning
  - → 7nm production with EUV in 2019
    - TSMC and Samsung
  - → 5nm is expected to be in early production in 2020
  - → "3nm" projected to use EUV Double patterning



# 7-nm Technology

- **7nm Technology** debuted in 2 "Late-News" papers from **TSMC** and **GlobalFoundries** at IEDM'16 (Dec. 2016)
- IEDM'16 Paper 2.6: A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors …, by TSMC (32 co-authors)
  - 12-level metal stack: m0-m4 (1X), m5-m9 (1.9X), m10+ (thick metal)
  - EUV lithography "under development" at TSMC
    - 7N process avaialble in 2017 - still using 193i lithograhpy
    - 7N+ to use EUV later in 2019
  - Comparison made vs TSMC's 16nm node 16FF+:
    - 40% faster –or– 65% lower power
    - Transistor **mismatch improved** by 25% (NMOS) and 35% (PMOS)
    - Reliability parameters very similar to 16nm



# FinFET Evolution

➔ FinFET scaling

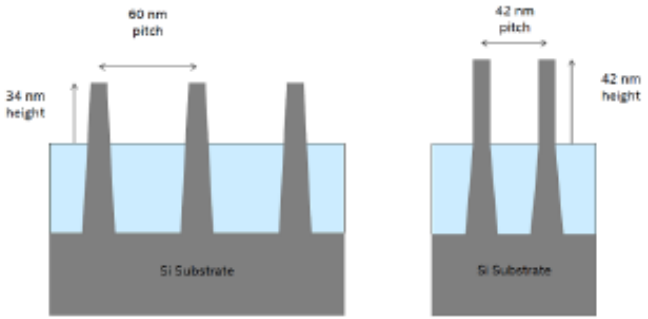
- Narrower, taller, and fewer fins
- Improved electrostatics demands fin width reduction
- Note physical channel length is now bigger than the nominal/node's marketing name!

## Fin Shape Evolution

| | 22nm | 14/16nm | 10nm | 7nm |
|---|---|---|---|---|
| Channel length | 25 | 22 | 19 | 16 |
| Fin width | 10 | 9 | 8 | 7 |
| Fin height | 34 | 42 | ~50 | 50+ |
| Aspect ratio | 3 : 1 | 5 : 1 | 6 : 1 | 7 : 1 |

L/W ratio ~2.5


- Two taller narrower fins in 14nm are equivalent to 3 fins in older 22nm →→
- Fin pitch reduction further reduces area (e.g. 42 nm pitch in 14nm node)

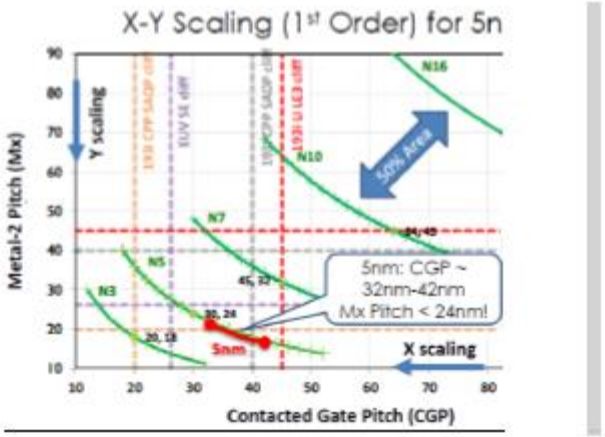


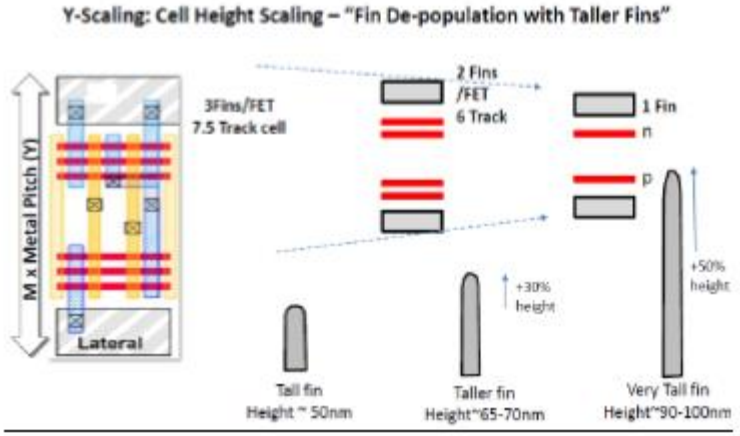

22 nm Process 14 nm Process

**Idea Courtesy of Dr. Djahanshahi (Microchip)**

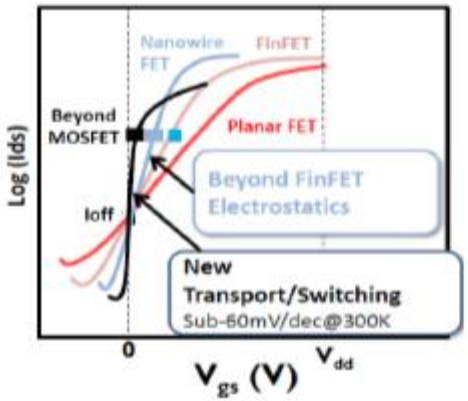
# FinFET Advantages - I

- **FinFET Scaling**: Smaller Fin pitch and metal pitch, fewer but taller Fins




- **FinFET Advantages**
  - FinFET improves Subthreshold Swing/Slope (SS) vs the planar FET, thanks to the better electrostatic control over the channel
  - For the same reason, FinFET has much less Body Effect, higher output impedance rds, and higher intrinsic gain (gm*rds)
- Gate-All-Around (GAA) or Nanowire has the best electrostatic
  - Si Nanowire: Reaches the limit of MOSFET SS → End of FinFET scaling
  - Need new transistor devices to lower SS beyond MOSFET limit (e.g. TFET, or Negative-Cgate FET) – more on this later



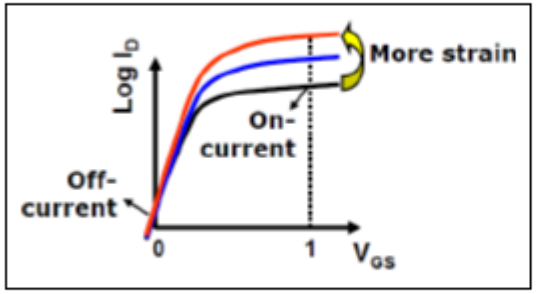
# FinFET Advantages - II

- **Channel material and stress engineering for advanced FinFETs**

  - Simple MOS scaling is not enough, e.g. increases $I_{OFF}$
  - Explore FinFET stress engineering & high-mobility channel materials

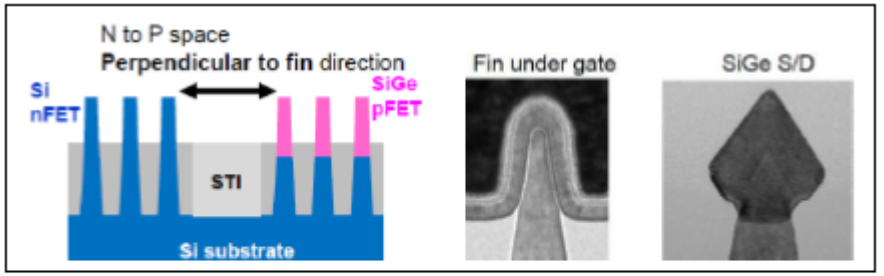
    - Mechanical strain ("good stress") increases the channel mobility of the MOS transistor

$$I_{on} \approx \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS}-V_T)^2$$

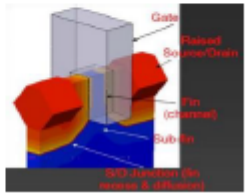



  - Compared to planar, in FinFET: $\mu_P$ improves and $\mu_N$ degrades due to surface orientations

    - FinFET S/D "stressors" increase the mobility by ~2x
      - Si S/D stressor for NMOS
      - SiGe S/D stressor for PMOS
    - Substrate "stressor": Si on $Si_{1-x}Ge_x$ substrate buffer
    - S/D & substrate stressors help scaling down to 5nm



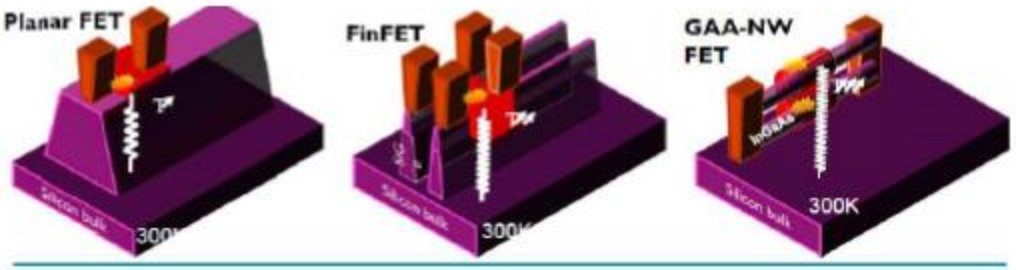

  - p-FinFET with SiGe channel stressor has higher mobility and improved reliability (NBTI)



# FinFET Problems

- **FinFET's Problem: Self-Heating Effect (SH or SHE)**: Joules heat generation vs. heat dissipation

  - **Issue in FinFET:** More power dissipation per volume in Fins – and – less dissipation path to substrate
    - Thermal conduction and heat transfer from FET channel to Si substrate worsens as we move from planar to FinFET to Gate-All-Around Nanowire (GAA NW)
    - SH complicates reliability analysis, i.e. extrapolation of other degradation mechanisms to locally heated operating condition




  - Foundry's spice-like models (e.g. TSMC, GF) support SHE flow:
    - 1st simulation run creates ΔT for every individual transistor
    - If ΔT ≤ 5°C or so, we can igonre the SHE
    - Else, ΔT from SHE can be factored in with a 2nd simulation run
  - SHE tips for **design** (choice of transistor finger & Fins) and **layout** (add heat sink structures)

| | |
|---|---|
| ○ Design<br>✓ Lower current per fin<br>✓ Fewer # of fins per OD<br>✓ Fewer # of fingers per OD<br>✓ Longer channel length | ○ Layout – Use heat sinks:<br>✓ Wide Guard Rings: "cold OD" w/ dummy MOS on top<br>✓ Metal stacks at D/S<br>✓ Dummy metal gates inserted within Active/hot OD<br>✓ Resistors in proximity to hot FinFET (e.g. for CML) |