Some useful formula

Parameters	NMOS	PMOS
V _{TO} (zero-bias threshold)	0.4V	-0.4V
γ (body-bias factor)	$0.2V^{1/2}$	$0.2V^{1/2}$
Req	12.5ΚΩ/□	30ΚΩ/□
$2 \Phi_{\rm F} $	0.88V	0.88V
u _n , u _p (mobility)	$270 \text{ cm}^2/\text{V-s}$	70cm ² /V-s
E _c (critical field)	6V/um	24V/um
C _{ox} (oxide capacitance)	$1.6 \times 10^{-6} \text{ F/cm}^2$	$1.6 \times 10^{-6} \text{ F/cm}^2$
C _{eff} (total self capacitance)	1fF/um	1fF/um
Cg (total gate capacitance)	2fF/um	2fF/um
υ _{sat} (velocity saturation)	8 x 10 ⁶ cm/s	8 x 10 ⁶ cm/s
λ	0	0

$$V_T = V_{T0} + \gamma (\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|})$$

$$I_{DS} = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_c L}\right)} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS}$$

Linear current

$$I_{DS} = W \nu_{\rm sat} C_{\rm ox} \, \frac{(V_{\rm GS} - V_{\rm T})^2}{(V_{\rm GS} - V_{\rm T}) \, + E_{\rm c} L}$$

Sat current short channel device

$$C_{J} = \frac{C_{j0} A}{\left(1 - \frac{V_{J}}{\phi_{B}}\right)^{m}}$$

Junction capacitance V_J is **forward** bias voltage junction

$$V_{\text{S}} = \frac{V_{\text{DD}} - |V_{\text{TP}}| + \chi V_{\text{TN}}}{1 + \chi}$$

Switching voltage of CMOS inverter where

$$\chi = \sqrt{rac{rac{W_N}{E_{\mathit{CN}}L_N}}{rac{W_P}{E_{\mathit{CP}}L_P}}} = \sqrt{rac{\mu_{\,n}W_N}{\mu_{\,p}W_P}}$$