ELEC 402
Chip-Level Issues
Lecture 17

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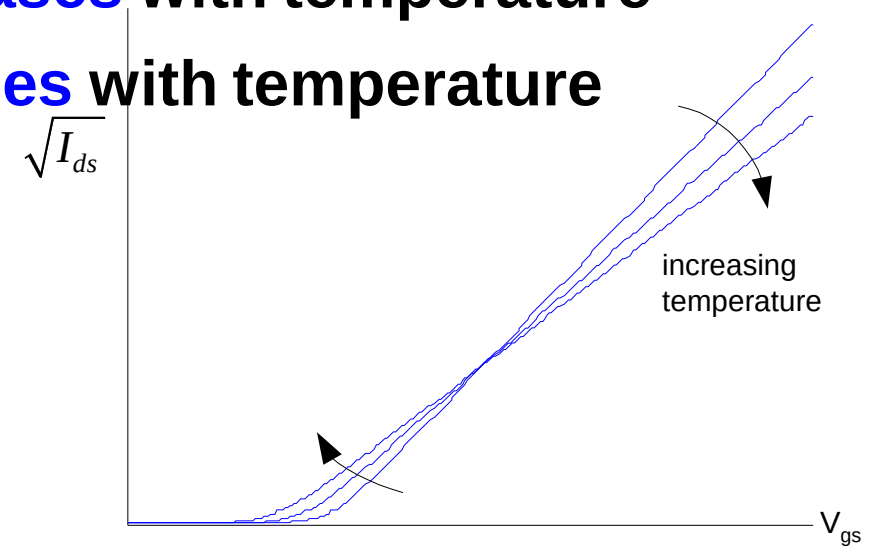
Slides Courtesy : Prof. S. Shekhar (UBC), Dr. H. Djahanshahi (Microsemi)

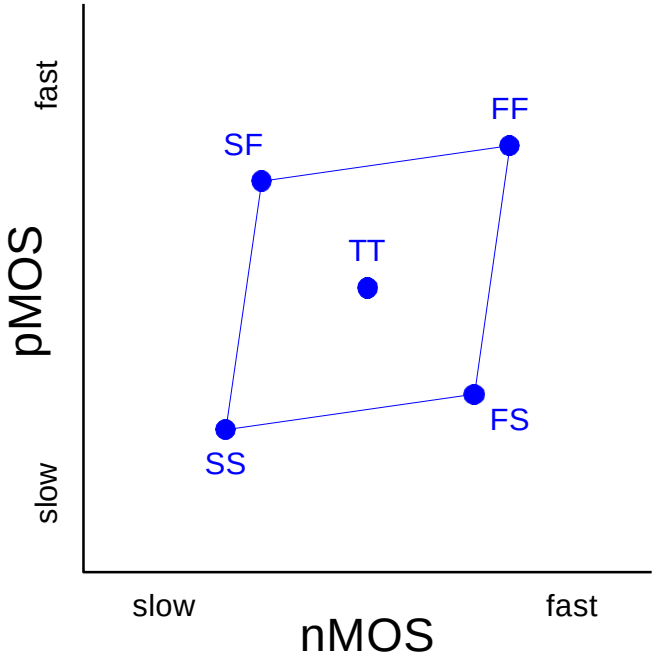
Simulation Coverage - Temperature Sensitivity

- **Increasing temperature**
  - **Reduces mobility**
  - **Reduces V_t**
  - **Increases resistance**
- **I_{ON} decreases with temperature**
- **I_{OFF} increases with temperature**



Simulation Coverage - Parameter Variation

- **Transistors have uncertainty in parameters**
  - **Process: L_{eff}, V_t, t_{ox}**
  - – Vary around typical (T) values
  - Fast (F)
    - **L_{eff}: short**
    - **V_t: low**
    - **t_{ox}: thin**
  - Slow (S): opposite



- Not all parameters are independent, corner for passive devices may be defined as well to consider WC designs

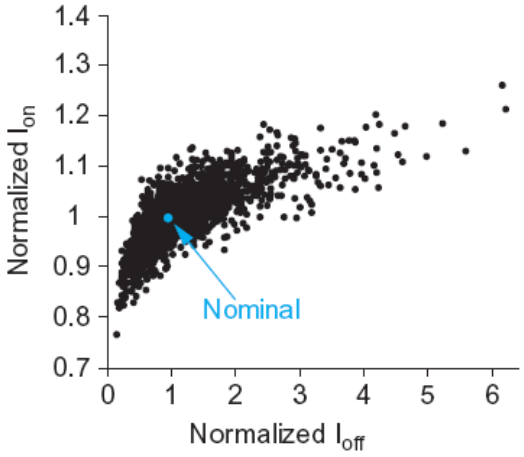
Simulation Coverage - Environmental Variation

- **V_{DD} and T (both ambient and local to the chip) also vary in time and space**
- **Fast:**
  - **V_{DD}: high**
  - **T: low**

Corner	Voltage	Temperature
F	1.1	0 C
T	1.0	70 C
S	0.9	125 C

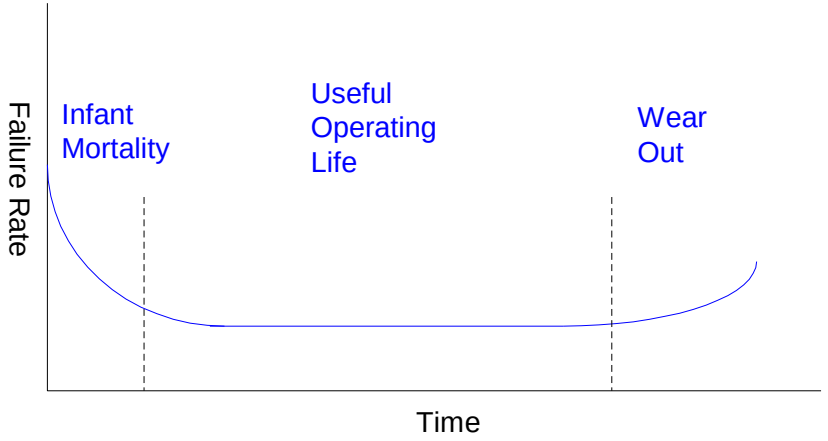
Monte Carlo Simulation

- As process variation increases, the worst-case corners become too pessimistic for practical design
- Monte Carlo: repeated simulations with parameters randomly varied each time
- Look at scatter plot of results to predict yield
- Ex: impact of V_t variation
  - ON-current
  - leakage



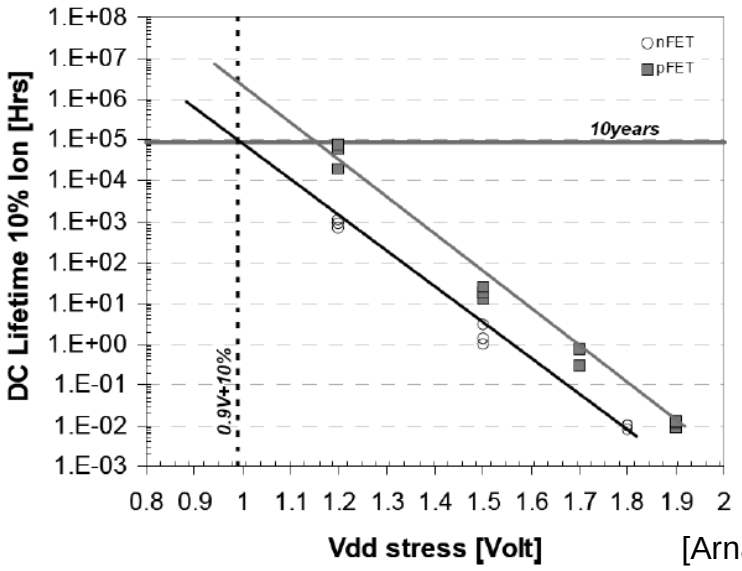
Reliability

- Hard Errors
  - Oxide wearout
  - Interconnect wearout
  - Overvoltage failure
  - Latchup
- Soft Errors
- Characterizing reliability
  - Mean time between failures (MTBF)
    - # of devices x hours of operation / number of failures
  - Failures in time (FIT)
    - # of failures / thousand hours / million devices



Accelerated Lifetime Testing

- Expected reliability typically exceeds 10 years
- But products come to market in 1-2 years
- Accelerated lifetime testing required to predict adequate long-term reliability

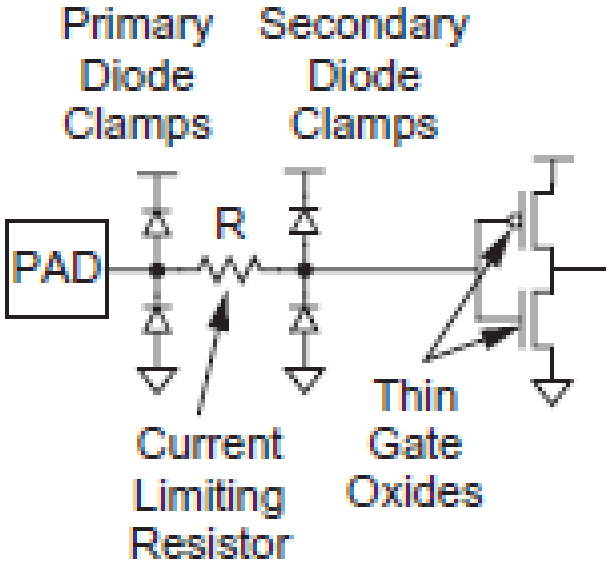


[Arnaud08]

Overvoltage Failure (ESD)

- High voltages can blow out tiny transistors
- *Electrostatic discharge* (ESD)
  - kilovolts from static electricity when the package pins are handled
- *Oxide breakdown*
  - In a 65 nm process, $V_g \approx 3$ V causes *arcing* through thin gate oxides

The current through primary diode might Be so large (10-20 A) that still damages device, hence a current-limiting resistor and Second layer of protection might be necessary



Power Distribution in ICs

Proper power grid design is very critical in IC design

It has several off-chip (Supply choice, PCB design, packaging, power pins/solder bumps)

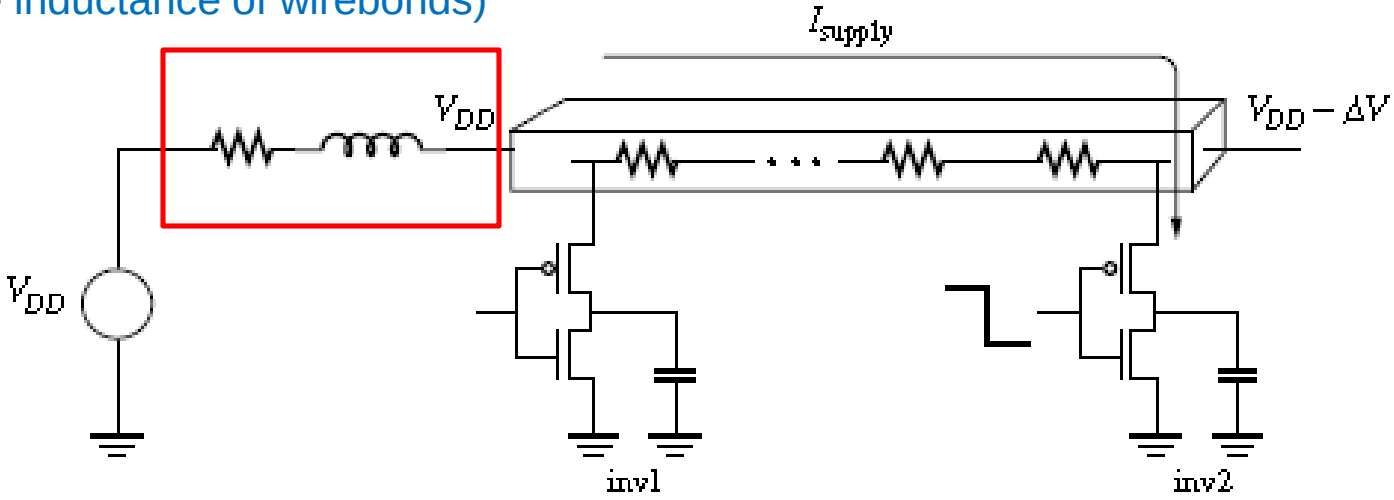
As well as on-chip (power grid design, minimum power drops and fluctuations).

The voltage drop along the package and

PCB traces (note the inductance of wirebonds)

The voltage drop along the interconnects

Known as IR drop



Wirebond Modeling/Compensation

- IR drop due to the resistance of interconnects drops the V_{dd} at local connection to the gates

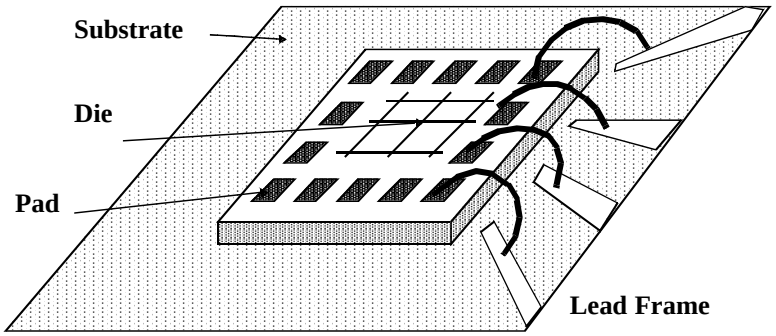
Therefore impacting the functionality and timing

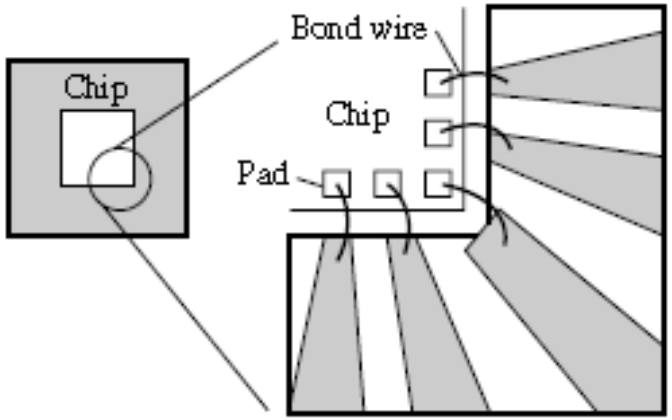
- In High speed design Ldi/dt (voltage drop on the inductance of paths) is also an issue.

-Long wirebonds (in the package) and long interconnects (on chip) create tangible values of inductance (almost 1pH/um of length) creating ~1nH for wire bond traces

At high-frequencies these wirebond may pose impedance mismatch and may be compensated

Wire Bonding

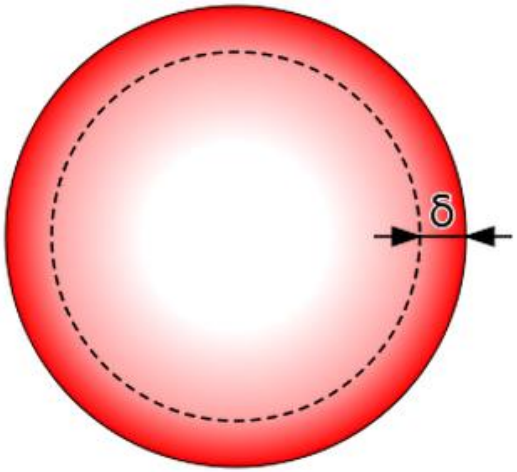




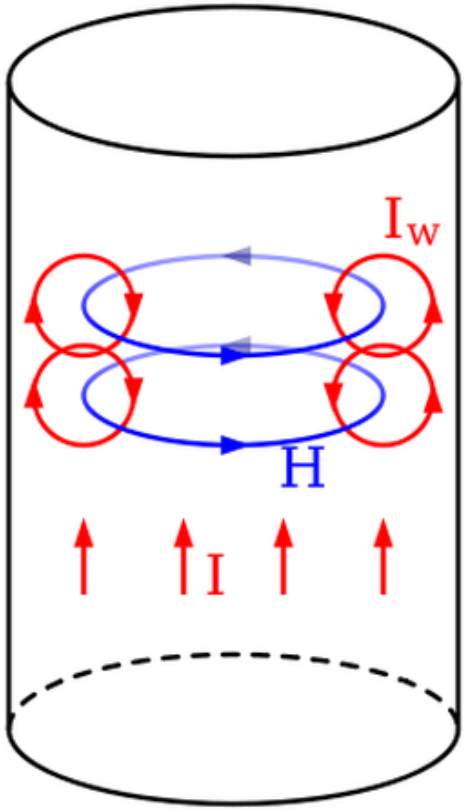
IR Drop – Skin effect

At high frequencies, current does not go through the Entire cross-section of wire uniformly. It tends to move Toward the edges due to magnetic fields and circulating Current (called *eddy-current*) hence lowering the effective Cross-section of wire

- Resistance increases even more in high frequencies!



Cross section of wire and skin depth (δ), most of current passes through thickness of δ only



Eddy current is circulating

Source: Wikipedia

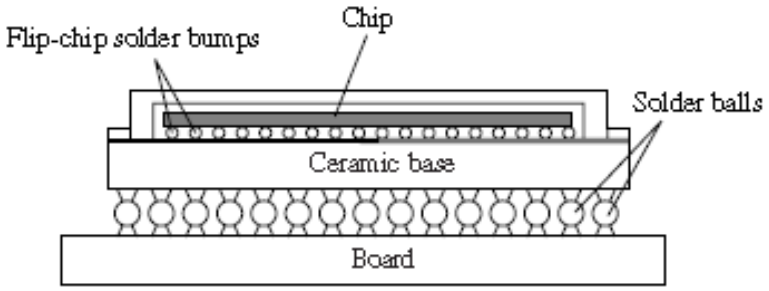
Flip chip Packaging

-Number of I/Os have increased several times recently

- High performance operation requires several power and ground (known as V_{dd} and V_{ss}) connections

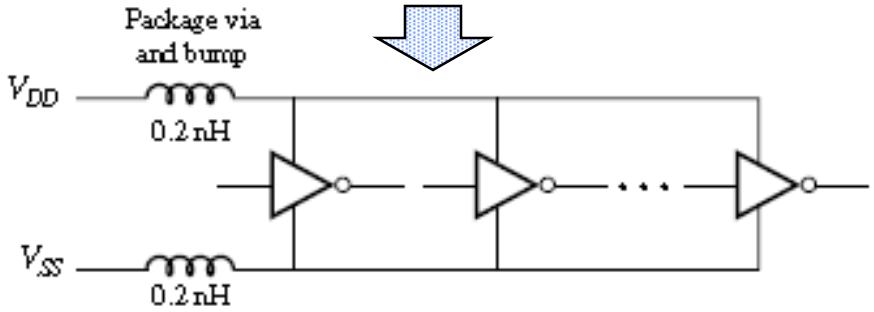
- The large inductance of wirebonds becomes problematic for low-voltage and high frequency

- Solder ball and bumps and ceramic Ball-grid-array (BGA) replaces the old fashion (costs more)

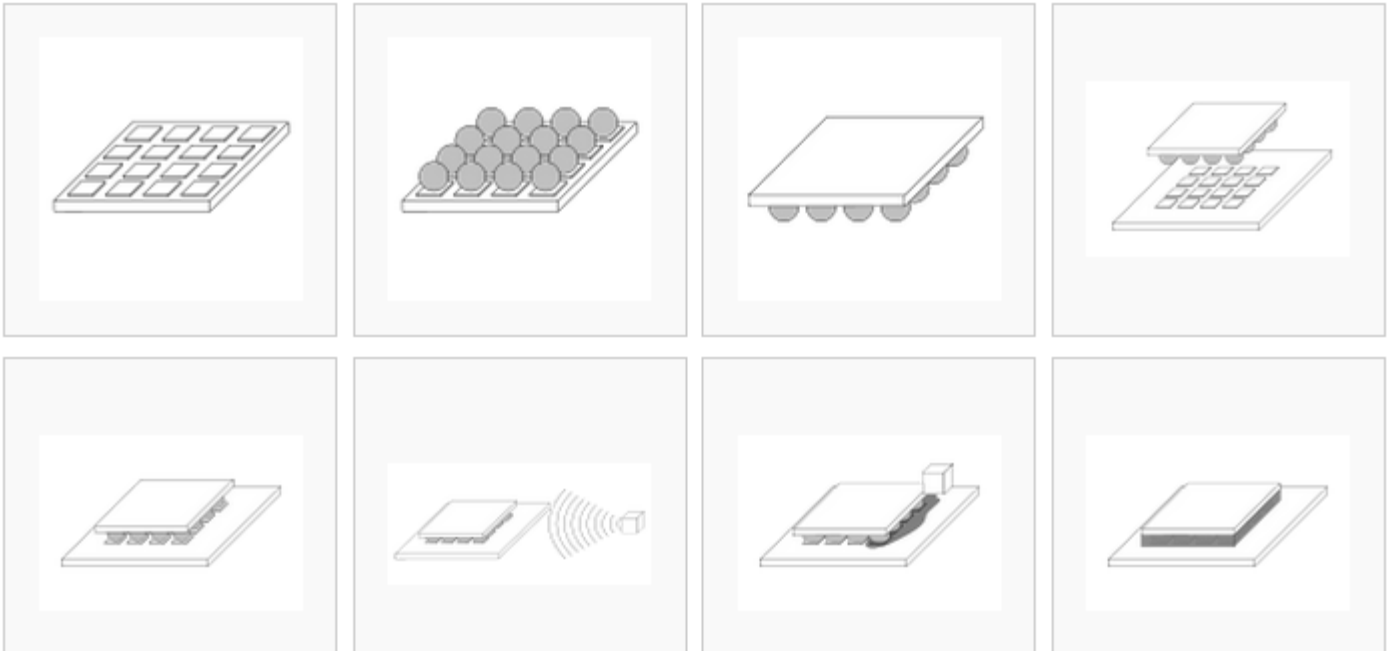


(b) Ball grid array packaging

Q: Imagine the system provides 25mA in 100ps for the switching of inverters what is the voltage drop on the supply of inverters due to switching current?



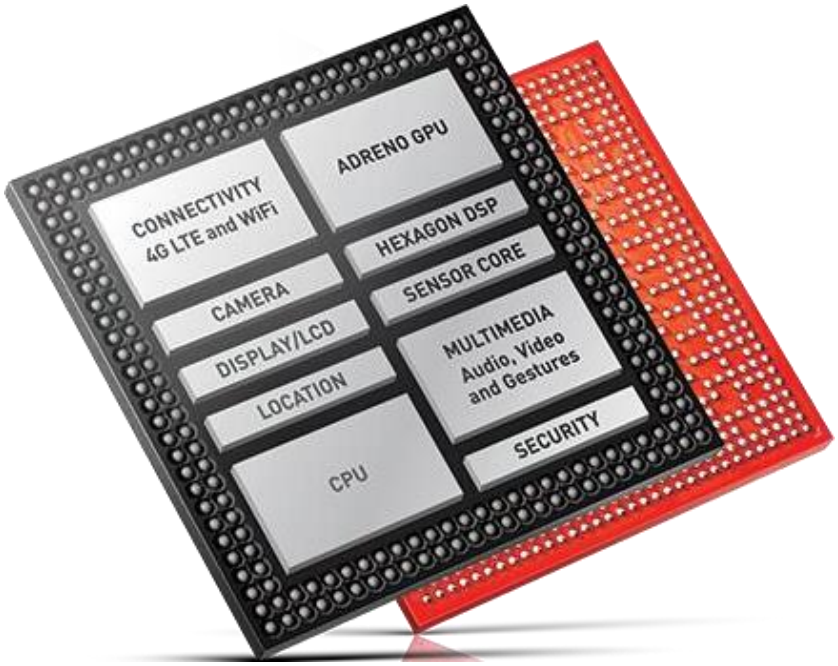
Flip chip Packaging - II



1. Integrated circuits are created on the wafer
2. Pads are metalized on the surface of the chips
3. Solder dots are deposited on each of the pads
4. Chips are cut
5. Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry
6. Solder balls are then remelted

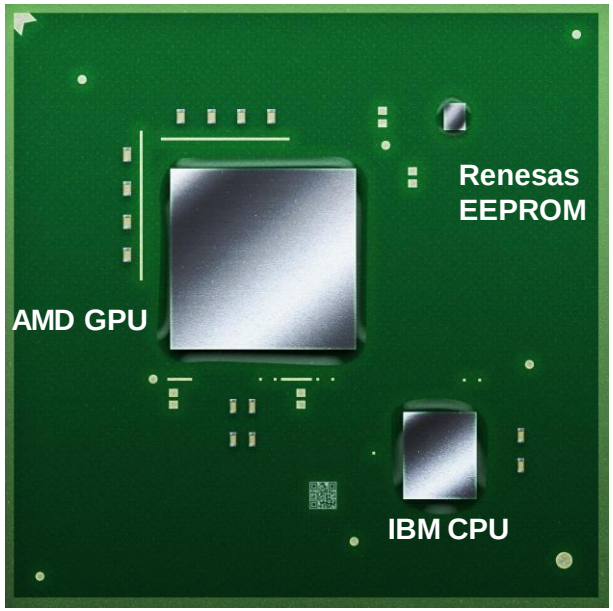
SoC, MCM

- System on chip (SoC): IC that integrates all components of a system (often digital, analog, mixed-signal, RF) on a single chip substrate



Qualcomm Snapdragon SoC

- Multi-Chip Module (MCM) Package: Number of ICs tiled horizontally in a single package

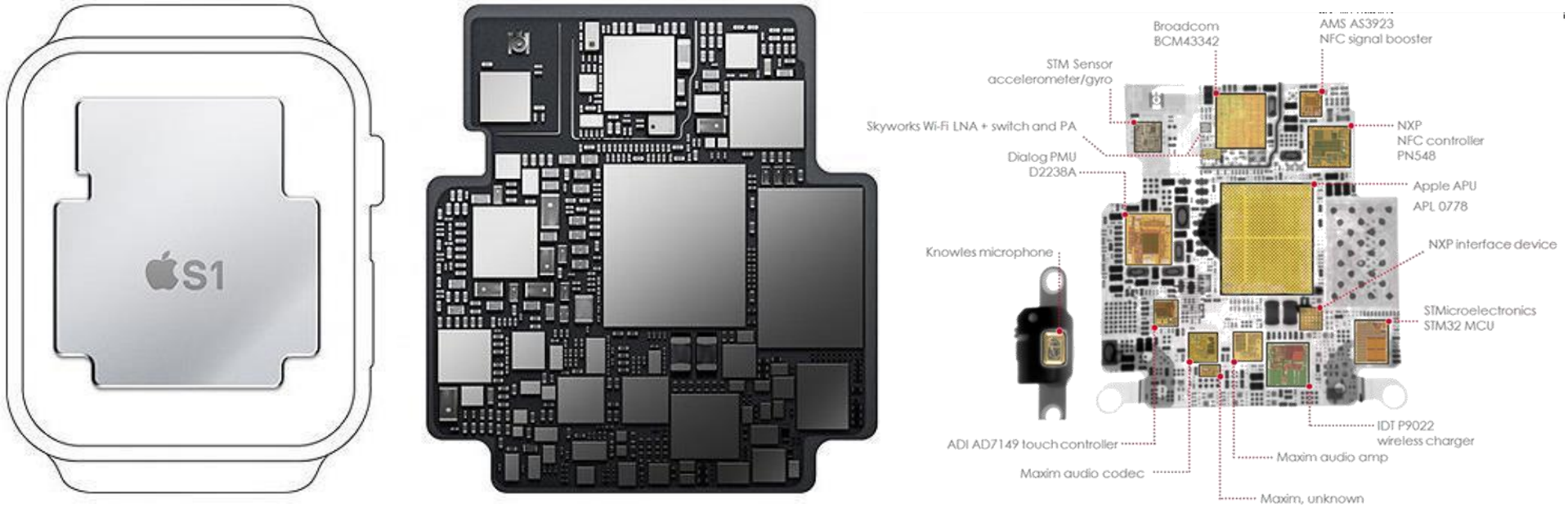


Wii U MCM

Source: Qualcomm, Wikipedia

SiP

- System in Package (SiP): “Dense MCM” with a number of ICs tiled horizontally *or stacked vertically* in a single package, connected using off-chip wirebonds or solder bumps.



Apple Watch SiP

Source: Chipworks

Electromigration (EM)

- High speed of electrons in metal interconnects eventually causes material transport

  In other words, *washes away the metal just like river water does to base rocks!*

- Large current in thin wires is of most critical situation

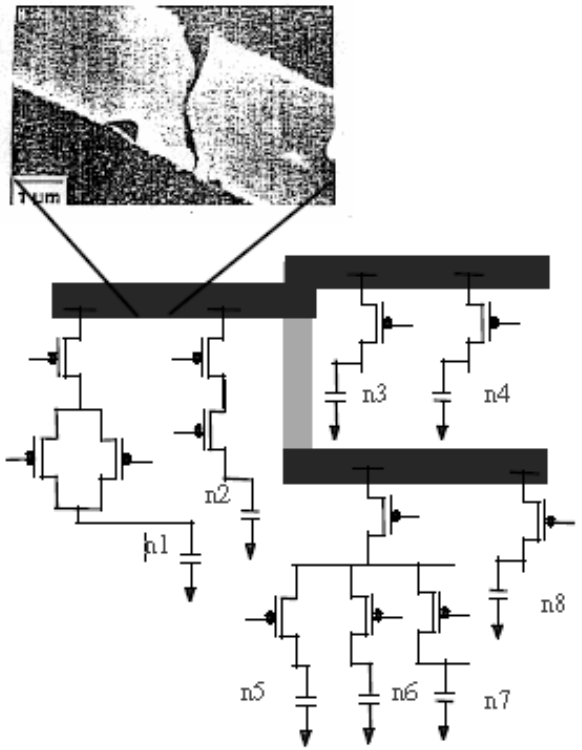
- There may sometimes be cracks in metal lines through fabrication that will speed up the EM

- Switch from Al to Cu was in favor of EM effect.

-DC (average current) is the most dominant source of EM.

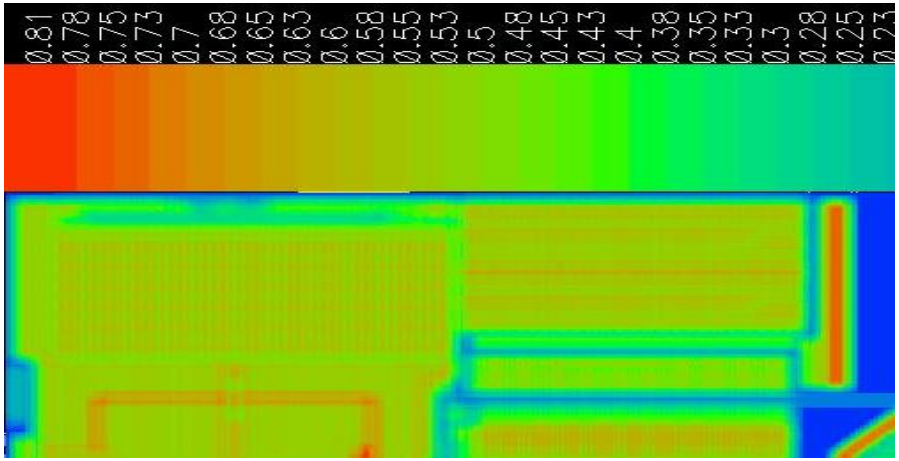
-Every metal piece (based on its thickness and width) has an allowable current density (J_{max}) corresponding to certain *mean-time –to-failure* (*MTTF*). MTTF simply tells you the lifetime of a chip. The average current density (based on design) J_{avg} must be less than J_{max} for reliability

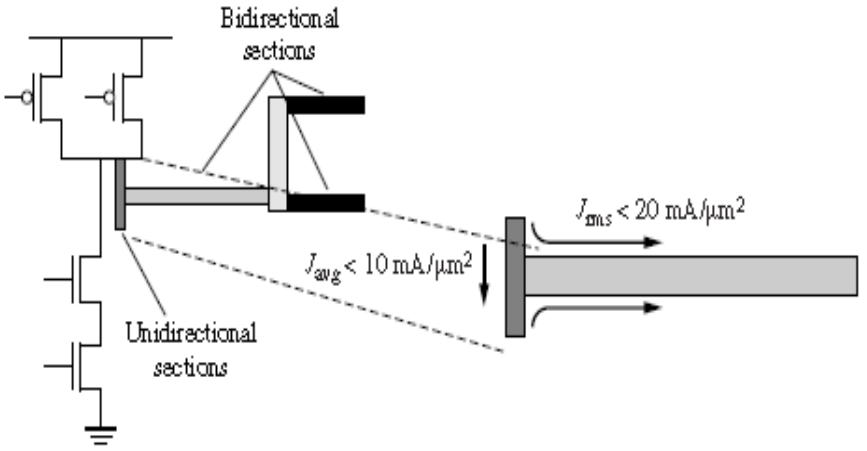
$$J_{avg} = I_{avg} / (W \times T) < J_{max}$$



EM - II

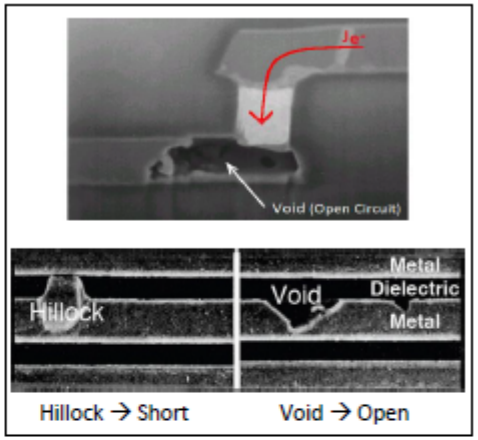
- In high-speed clock design, a new factor has become a source of EM, J_{RMS} in clock lines (note that J_{avg} is ideally zero in a clock line (unlike power lines)
- J_{RMS} should be smaller than a value set by *MTTF* and heat $J_{RMS} < J_{AC,max}$ (note that $J_{AC,max}$ is larger than J_{max}) .
- Both Unidirectional and bidirectional paths can be a source of EM
- Use *multi-phase clocking* and *stagger* inverter to reduce both effects (complexity trade-off)
- Color-coded IR drops and EM graphs are mainstream in industry

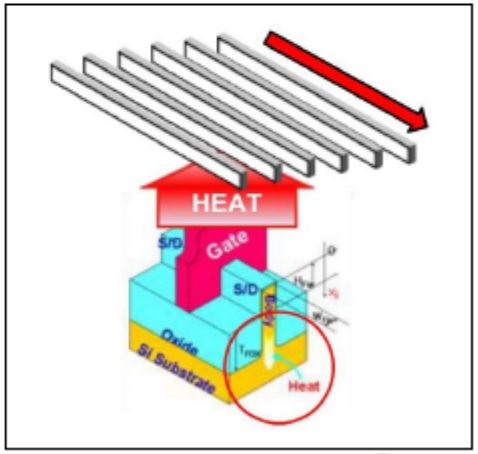




FinFET Thermal EM Flow

- **Electromigration** (EM): High current density (J_{e^-}) or "*electron wind*" causes gradual *migration* of metal atoms, potentially creating "void" (high resistance/open circuit) or short circuit
  - Industry practice for EM failure is a resistance increase (**ΔR**) above ~10-20% over lifetime
- EM happens above a certain current density (mA/μm^2, or mA/μm for fixed thickness metal)
  - Only **AVERAGE** (DC) current matters, not instantaneous current
  - AC current > ~10 MHz exhibits EM "healing" effect in psitive & negative cycles, BUT **JOULE HEATING** due to **RMS** current degrades the DC EM limit
  - EM exponentially accelerates with temperature: ΔT ≈ **10°C** degrades EM lifetime by **2x**
- EM is increasingly more challenging in **FinFET** processes, because:
  - Cross section of metal wires & vias in FinFET processes keeps shrinking
  - Higher drive strength (I_{ON}) and faster switching speeds create higher AC RMS currents
  - FinFET self-heating effect (**SHE**) causes local temperature rise (**ΔT**) in transistors that gets partially transferred to the metal stack above, thus degrading EM limits → →
- Traditional EM flows ignore any transistor Self Heating, and may use a ΔT margin (e.g. 5°C) for Joule Heating due to AC RMS current (e.g. analyze EM at 105°C using derated limits of 110°C)
- **FinFET reliabilty requires Thermal-aware EM flow**
  - Calculate metal temperature rise due to **(1)** local SHE in FinFET, **(2)** metals Joule Heating
  - Set Average current EM limits for each wire according to calculated local temperature





Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability

$$I_{rms} = \sqrt{\frac{\int_0^T I(t)^2 dt}{T}}$$

  - Typical limits: $J_{rms} < 15$ mA / μm^2

Decoupling Capacitors

Large capacitor around every block can act as the reservoir of charge (providing the instantaneous current to the circuit and later be charged back through the supply network)

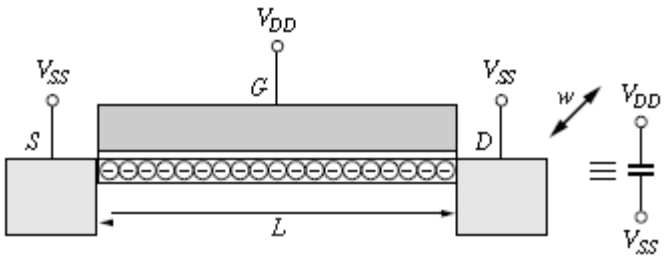
-Heavily helps with the IR drops and ripples on the power network

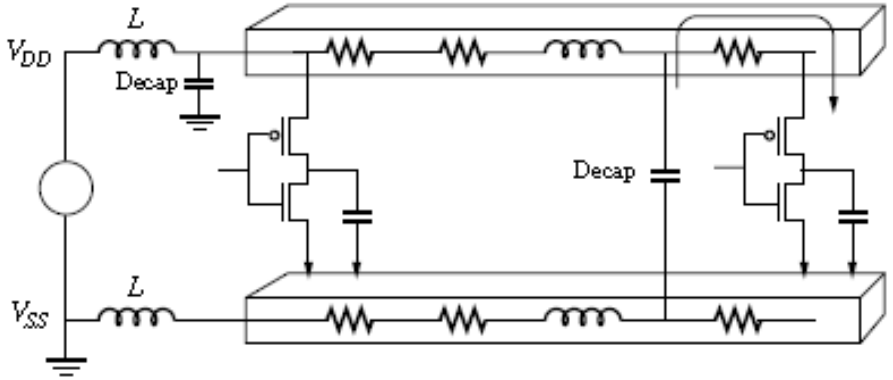
-Large amount of chip area is covered by *De-caps.*

- Places with large switching currents require more decaps.

- Since MOS capacitor provides the largest density and the linearity of capacitance is not critical, an NMOS in triode (gate to V_{dd} and source/drain to gnd) provides a large value.

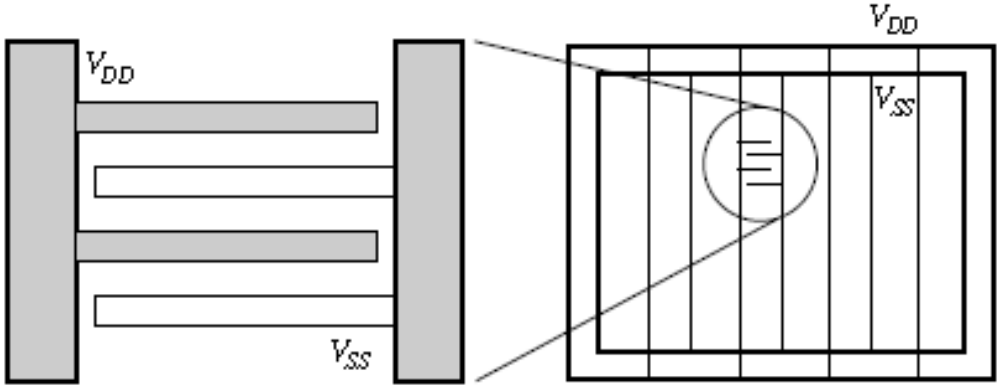
$C_{decap} = C_{ox}\, WL + C_{ol}\, W$





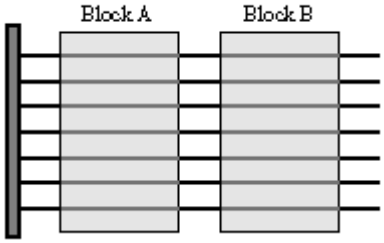
Power Distribution on-chip

Keep the balance and symmetry is of utmost importance



Power grid using

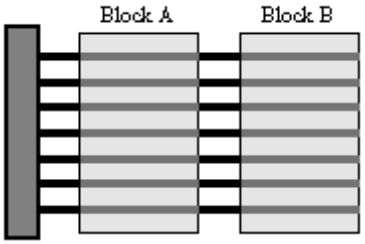
Dual-ring



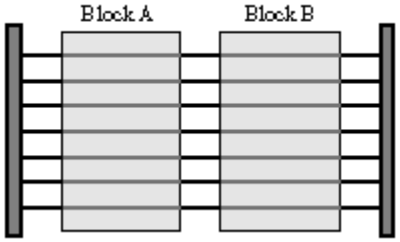
Poor routing IR drop

No timing match between

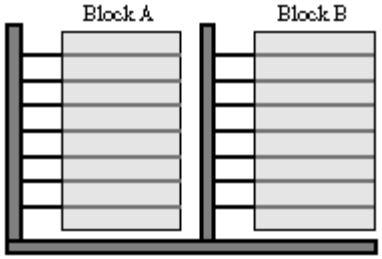
A and B



better Design

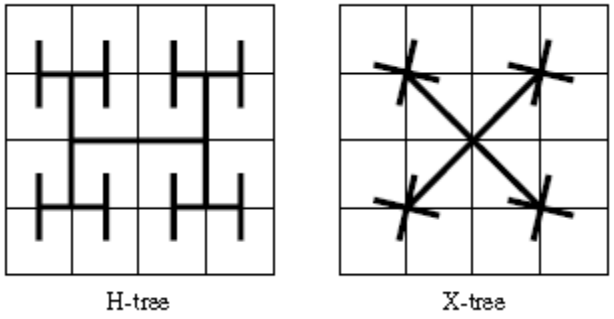


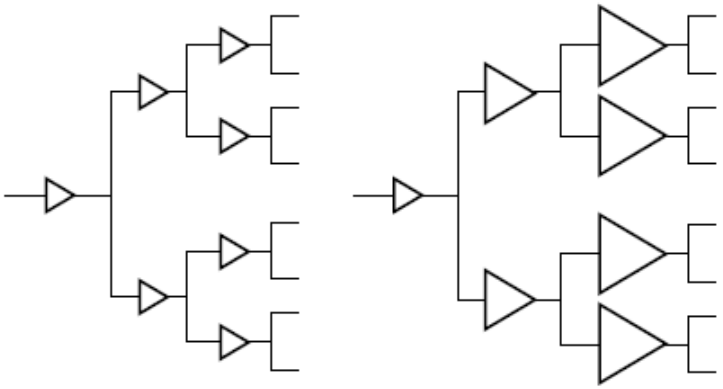
Best (double –sided)

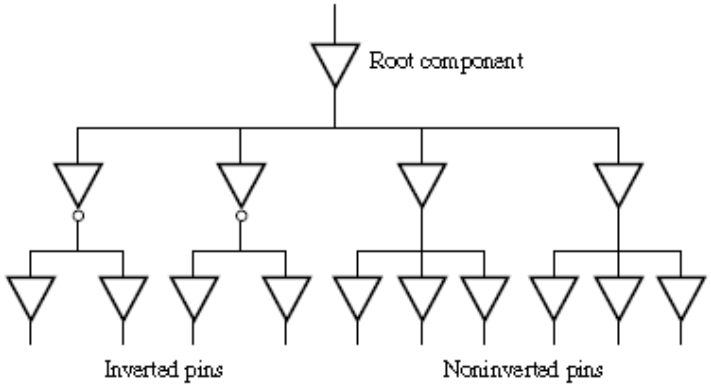


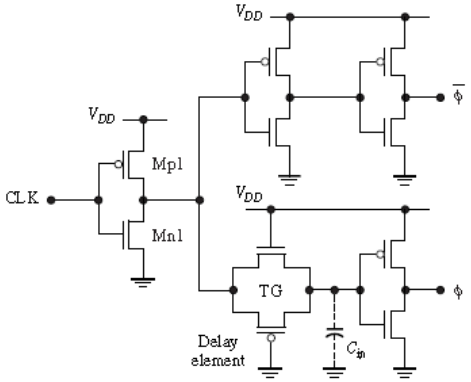
Best (Tree approach)

Clock Distribution on-chip









Board notes

Several techniques in the literature to keep the clock grid as symmetrical and balanced as possible