Project / Assignment #4

Due Sun Nov 14th, 11:59PM to elec402project@gmail.com – **No Exceptions (no late submissions)**

1. NAND3 Simulation & Layout [**82pts**]

Introduction:

For this project, you will use the Cadence Design tools to layout and characterize a simple NAND3. This project will get you familiar with Cadence and also with the simulation of the layouts that you create.

Description/Requirements:

Work through the Cadence tutorial.

Layout and simulate the NAND3.

You will be designing a symmetrical NAND3 with equal $t_{p,LH}$ and $t_{p,HL}$ (measured from 50% to 50%). Please get the time difference within 5ps.

The input clock slew rate is 10ps (time for input to go from high to low, and vice versa)

Assume a 10fF of load capacitance when simulating

VDD = 1V and GND=0V

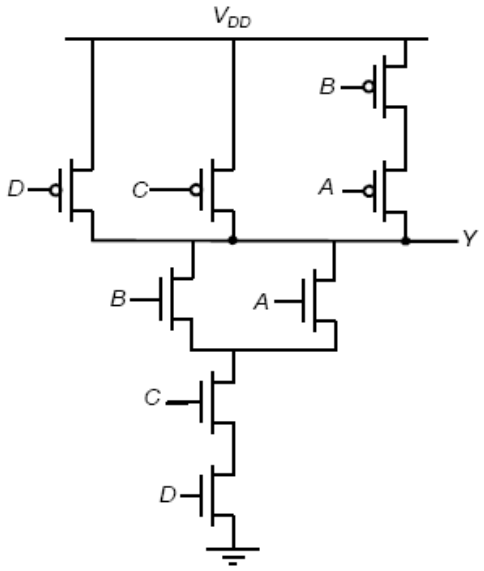
Report Layout

1. Name, student number and project title on the first page of your project report
2. Just below the project title, clearly state your area (widths and lengths are measured from highest IMP layer to the lowest IMP layer), delay and area x delay [**7pts**]
3. NAND3 layout with rulers (from Cadence) showing the dimensions of the layout, label pins and show distance between them, and (snapshot of) DRC summary [**20pts**]
4. Waveforms showing t_{pHL} and t_{pLH} measured using Cadence ADE. Show the pattern for the worst-case delay and use extracted view including all parasitics [**25pts** – symmetry between t_{pHL} and t_{pLH} matters]
5. Cadence Schematic clearly showing the 12 fF of load cap has been included. [**5pts**]

The grading will be competition based.

We are looking for the smallest AND fastest NAND3 that meet the requirements. In other words, all other things being equal, the project with the smallest product of area x delay will be deemed the best. [**25pts**]

2. Consider the following circuit. What is the logic function for this block (Boolean expression) (**3pts**)



(a) Size the gates such that the output resistance is same as that of an inverter with NMOS W/L = 4λ and PMOS W/L = 8λ. (**5pts**)

(b) What are the input patterns (input pattern example ABCD=0000) that give **worst case** t_{pHL} and t_{pLH}. State clearly the initial input pattern and which input(s) have to make transition in order to achieve this maximum propagation delay. (Hint: consider internal nodes and use the results of question 1). Verify your result with Cadence schematic simulations. Measure the delay using WV. Submit the schematic netlist as well as the waveform output used for measuring the worst case delay. (**10pts**)

3. For the circuit shown in Figure 1, assume that the transmission gates are all 4λ:2λ and that the inverters driving the transmission gates have PMOS transistors that are 8λ:2λ and NMOS transistors that are 4λ:2λ, where λ = 0.1μm. The output inverter drive a 50 fF load. The output inverter is *f* times larger than the input inverters. Answer the following questions (**15 points**)

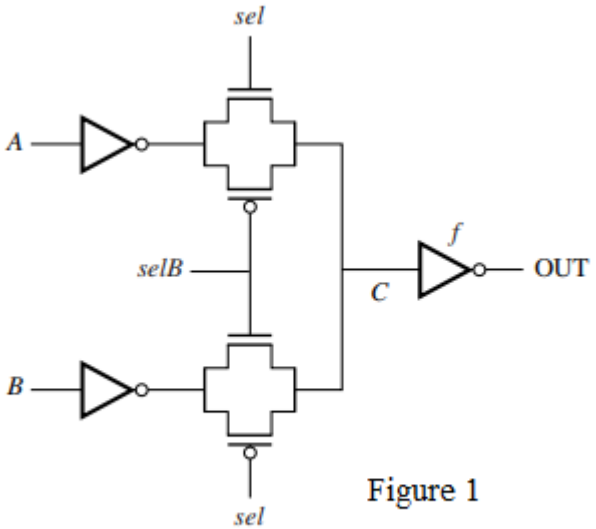


Figure 1

(a) Write the expression for the output function in terms of *A*, *B*, *sel*, and *selB*.

(b) Draw an equivalent *RC* circuit model for the path from *A* to *C* assuming that the *sel* signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c) What is the expression for the delay from *A* to *C*? Use Elmore delay here.

(d) Write down the expression for the delay through the output inverter knowing that it is *f* times larger than the input inverters. Use an *RC* delay here.

(e) Determine the optimal size of the output inverter to minimize the total delay from *A* to OUT. That is, write the complete expression for the delay and then derive the best value of *f* that would produce the smallest delay.