Project/Assignment 5
Due Friday Dec 3rd, 11:59 PM to elec402project@gmail.com – **No Exceptions (no late submissions)**

This assignment has more than 50% bonus point (75/115 is considered full mark, if you receive more than 70 it will be added to your previous assignments)

1. Cell Library Layout (45 points) – Bonus

Introduction:

For this project, you will take your Verilog code from project 1 and 2, then synthesize it with 45nm standard cell library, and finally lay it out using Cadence Innovus tool.

Project Goals:

Auto-route and layout FSM using Innovus
Test the final layout.

Project Description/Requirements:

Assume a 10fF of load capacitance when simulating for all your outputs.

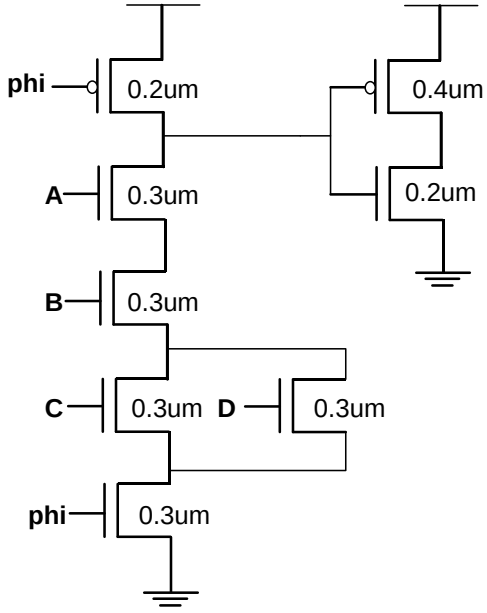
Report Layout

1. Name, student number and project title on the first page of your project report.
2. Your report must include, but not limited to, the following:
    a. Description regarding the function of your FSM design
    b. Description in detail for all the inputs and outputs
    c. Testing procedure
3. Complete layout with rulers (from Cadence) showing the dimensions of the full layout.
4. Output waveforms of the original Verilog code along with the waveforms from simulations of the FSM layout.
5. Test files to show that you tested your schematic properly.

2. Domino Logic (12 points)

1. (a) Determine the logic function OUT (3 points)

2. (b) Determine the reduction in voltage at the input of the inverter under the worst case charge sharing condition. C_{eff} = 1fF/um and C_g = 2 fF/um technology. (9 points)



3. In the circuit of Figure **4** , determine the capacitance of each node and calculate the minimum and maximum delay. (All transistors are minimum size, $L = 2\lambda$ and $W = 2\lambda$, unless otherwise specified.)

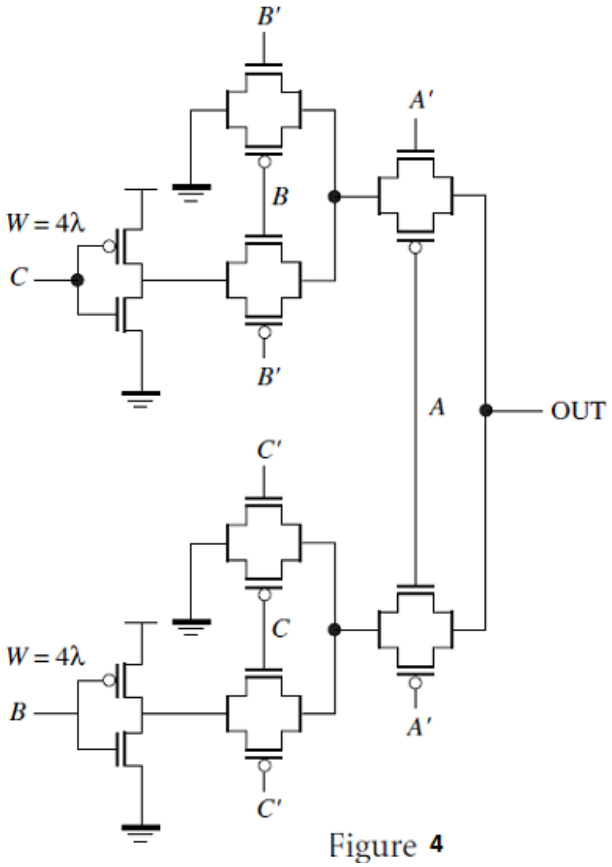
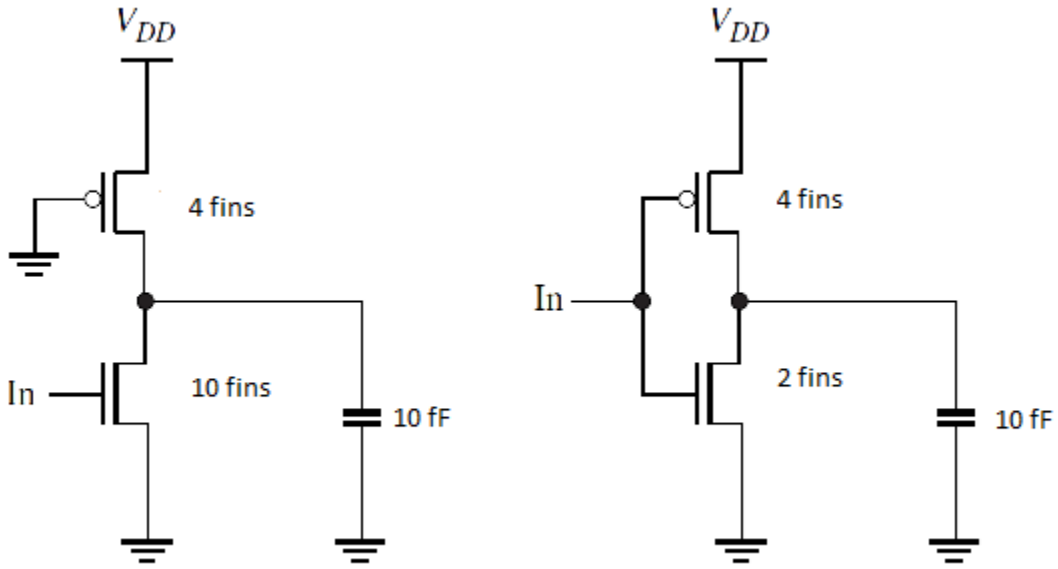


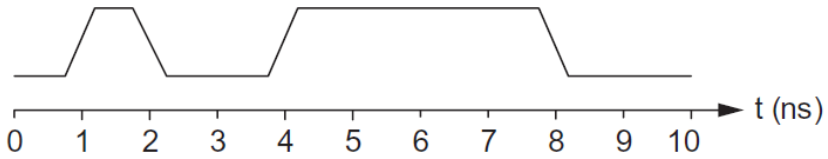
Figure **4**

(14 points)

4) (**Power consumption**) Analytically estimate the static (only for left circuit) and dynamic power consumption of the two inverters below **(8 points)** and compare your analytical results with that of simulation **(8 points)**. Sketch VTC and show on the graph in which region we have power due to DC current, subthreshold current and short circuit current (**4 points**). Use 15 nm simulations and use an input frequency of 100 MHz for calculation/simulation. 10 fF is an explicit capacitor at the output of inverters.



2 Determine the activity factor for the signal shown The clock rate is 1GHz.



(4 points)

6. (15 points) Interconnects

Consider an 18 mm Metal 7 wire in a 40 nm technology. Assume the wire is 0.4 μm wide and 0.8 μm thick with a spacing to adjacent wires of 2 μm. The height above and below to Metal 8 and Metal 6 is 0.5 μm. Assume Cu for interconnect ($\rho = 0.017\ \Omega$-μm) and a low-k dielectric material ($\epsilon_r = 3.0$). Assume a worst-case coverage of Metal 6 below, Metal 8 above, and Metal 7 for adjacent lines that are shielding the wire of interest.

(a) Compute the resistance per unit length and capacitance per unit length for this wire.

(b) Estimate the delay of the distributed *RC* wire, assuming that the driver is a perfect voltage source and that the load capacitance is 50 fF.

(c) Assume that the wire is being driven by a 25X inverter. What is the new delay?