ELEC 402 – October 24, 2021

Project 3 Report

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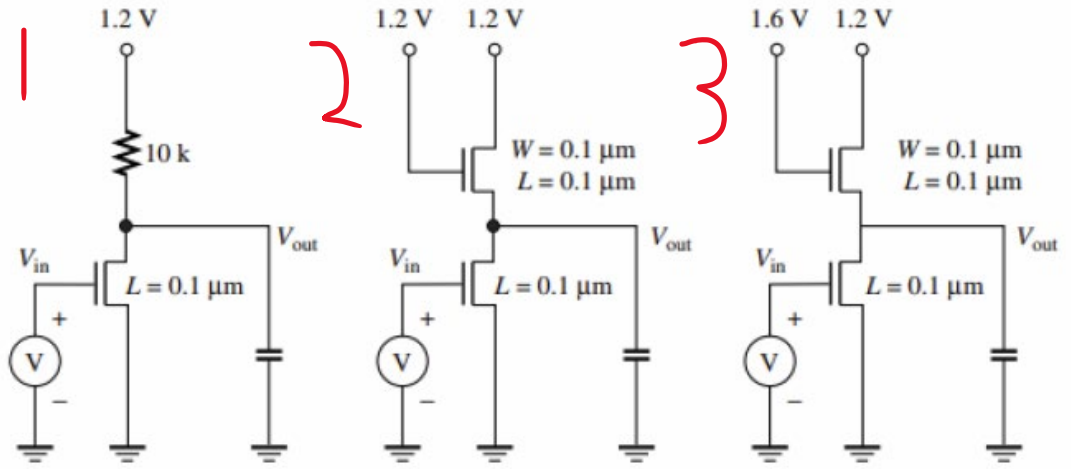
1. In the circuits of Figure , design the widths of the pull-down tran sistors so that $V_{OL} = 0.1$ V. (All transistors are minimum size, $L = 0.1\ \mu$m.) Explain the results. (15 points)



$\mu_n = 270\ \text{cm}^2/\text{V-s}, \quad C_{ox} = 1.0\ \mu\text{F/cm}^2, \quad V_{T0} = 0.4\ \text{V}, \quad V_{DD} = 1.2\ \text{V}$

$E_{CN}L = 0.6\ \text{V}, \quad \upsilon_{sat} = 8 \times 10^6\ \text{cm/s}, \quad \gamma = 0.2\ \text{V}^{1/2} \quad 2|\phi_F| = 0.88\ \text{V}$

a) Resistive load inverter

At one extreme, V_{in} is high, transistor is off and no current flows because MOS is in cut-off region, $V_{OH} = V_{DD}$. At the other extreme, $V_{in} = V_{OH} = V_{DD}$ substituted into $I_{OUT} = I_{load}$ g $I_R = I_{DS}$(lin), and the transistor operates in linear region. Using the useful formula for linear current:

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{W}{L} * \frac{\mu_n C_{ox}}{1 + \frac{V_{DS}}{E_C L}} \left[V_{GS} - V_T - \frac{V_{DS}}{2}\right] V_{DS}$$

Now we can also just straight up plug-in everything (taken from question):

- $V_{in} = V_{GS} = V_{OH} = V_{DD} = 1.2$ V
- $V_{DS} = V_{out} = V_{OL} = 0.1$ V
- L = 0.1 µm
- $R_L = 10$ kΩ
- $\mu_n = 270\ \text{cm}^2\text{V}^{-1}\text{s}^{-1}$
- $C_{ox} = 1.0\text{E-}6\ \text{F/cm}^2$
- $E_C = 6$ V/µm
- $V_T = 0.4$ V

Equating for W and throwing into wolfram:

$$W = 6.3375 * 10^{-7}\ m = 0.634\ \mu m$$

b) Saturated-enhancement-load inverter

With this layout, we know the top pull-up transistor is the load and bottom pull-down transistor is the inverter. We know the load is always in saturation and the inverter should be linear because we want

$V_{out} = V_{OL} = 0.1$ V. Using the useful formulas for linear (left) and saturated (right) current, we can equate the two and get:

$$\frac{W_{inverter}}{L} * \frac{\mu_n C_{ox}}{1 + \frac{V_{DS}}{E_C L}} \left[V_{GS} - V_T - \frac{V_{DS}}{2}\right] V_{DS} = W_{load} v_{sat} C_{ox} * \frac{(V_{GS} - V_T)\text{^}2}{V_{GS} - V_T + E_C L}$$

Using the following substitutions (inverter):

- $V_{in} = V_{GS} = V_{OH} = V_{DD} = 1.2$ V
- $V_{DS} = V_{out} = V_{OL} = 0.1$ V
- L = 0.1 µm
- $\mu_n = 270$ cm^{2}V^{-1}s^{-1}
- $C_{ox} = 1.0E\text{-}6$ F/cm^2
- $E_C = 6$ V/µm
- $V_T = 0.4$ V

Using the following substitutions (load):

- $V_{in} = V_{OH} = V_{DD} = 1.2$ V
- $V_{GS} = 1.2 - 0.1 = 1.1$ V
- $v_{sat} = 8E6$ cm/s
- $W_{load} = 0.1$ µm
- L = 0.1 µm
- $C_{ox} = 1.0E\text{-}6$ F/cm^2
- $E_C = 6$ V/µm
- $V_T = 0.4$ V

Note that although the left side units cancel out nicely due to the cm^2/cm^2, we need to convert the right-side units from cm (1E-2) to µm (1E-6) after the $C_{ox}v_{sat}$ cancellation as there is still a cm unit left, done by multiplying the right side with 1E-4.
Equating for $W_{inverter}$ and throwing into wolfram:

$$Winverter = 1.73726 * 10^{-7}\ m = 0.174\ \mu m$$

c) Linear-Enhancement-Load inverter

To overcome low V_{OH}, in the saturated-enhancement-load inverter, instead of V_{DD} for both gate and drain of the load transistor, it is separated with $V_{GG} = 1.6$ V and $V_{DD} = 1.2$ V. Its linear region of operation is then $V_{GG} > V_{DD} + V_{TL}(V_{DD})$. Again, we equate currents but this time, the right side is not in saturation, but linear operation as well:

$$\frac{W_{inverter}}{L} * \frac{\mu_n C_{ox}}{1 + \frac{V_{DS}}{E_C L}} \left[V_{GS} - V_T - \frac{V_{DS}}{2}\right] V_{DS} = \frac{W_{load}}{L} * \frac{\mu_n C_{ox}}{1 + \frac{V_{DS}}{E_C L}} \left[V_{GS} - V_T - \frac{V_{DS}}{2}\right] V_{DS}$$

Using the following substitutions (inverter):

- $V_{in} = V_{GS} = V_{OH} = V_{DD} = 1.2$ V
- $V_{DS} = V_{out} = V_{OL} = 0.1$ V
- L = 0.1 µm
- $\mu_n = 270$ cm^{2}V^{-1}s^{-1}
- $C_{ox} = 1.0E\text{-}6$ F/cm^2
- $E_C = 6$ V/µm
- $V_T = 0.4$ V

Using the following substitutions (load):

- $V_{in} = V_{DS} = V_{OH} = V_{DD} = 1.2$ V
- $V_{out} = V_{OL} = 0.1$ V
- $V_{GS} = 1.6 - 0.1 = 1.5$ V
- L = 0.1 µm
- $\mu_n = 270$ cm^{2}V^{-1}s^{-1}
- $C_{ox} = 1.0E\text{-}6$ F/cm^2
- $E_C = 6$ V/µm
- $V_T = 0.4$ V

Note that the difference this time between linear-enhancement and saturated-enhancement is V_{GS} of the load pull-up transistor. Also note that V_{in} for the linear region inverter pull-down transistor remains at 1.2 V.

Equating for $W_{inverter}$ and throwing into wolfram (no need to simplify if wolfram does it all 😊):

$$Winverter = 1.4 * 10^{-7}\ m = 0.140\ \mu m$$

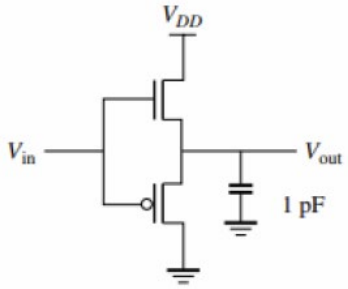
d) Results explanation

Resistive Load	Saturated-Enhancement-Load	Linear-Enhancement-Load
0.634 µm	0.174 µm	0.140 µm

Table 0. Calculated widths for each inverter.

The resistive load inverter appears to have the highest width, followed by Saturated-Enhancement, then Linear-Enhancement. The resistor in digital design is probably worse than using a MOSFET due to area which in turn means a slower and larger circuit. The Saturated-Enhancement load inverter replaces the resistor with a MOSFET, where the max input voltage is limited by $V_{DD} - V_T$., which has tradeoffs such a lower saturation operation threshold. The Linear-Enhancement load inverter introduces a higher V_{GG}, which means that biasing the gate voltage to exactly V_T above drain voltage allows linear operation and increases the saturation operation threshold.

2. (a) What is the intended function of the circuit shown in Figure ? What is the output swing?



(b) Draw the dc voltage transfer characteristic of the above gate. Label V_{OL} and V_{OH}, and any other interesting values in the VTC. Since the gate has hysteresis, be sure to handle both the rising and falling cases.

(c) What is the gain of the circuit? Is this a valid gate (i.e., does it have the needed noise rejection properties)?

(d) Use CAD to validate your solution by plotting the VTC (20 points)

- For CAD simulation in Q2 assume $V_{DD} = 0.9$ V, and use two fingers per transistor.

a) The intended function of the circuit should be as a non-inverting buffer. It resembles an inverter except the PMOS and NMOS are switched, with the V_{out} at the source. If we set logic in to be HIGH, we get HIGH as output, and vice-versa setting logic in to LOW, gets LOW as output, with

V_{OH} being maximum $V_{DD} - V_T$ due to NMOS pull-up and V_{OL} being minimum V_T due to PMOS pull-down, assuming same threshold voltage V_T for both PMOS and NMOS.

b) The dc voltage transfer characteristic is drawn below with the following notes:
   a. We start from $V_{in} = 0$ V and output is $V_{OL} = V_T$ and increase the voltage. The output should not change until NMOS turns on and pulls output up at $V_{in} = 2V_T$.
   b. Output voltage increases as input voltage increases until V_{DD}, where output is at most $V_{OH} = V_{DD} - V_T$.
   c. When decreasing V_{in}, the output does not decrease until V_{in} drops below $V_{DD} - V_T$
   d. Then at $V_{DD} - 2V_T$ we see that the output decreases until V_T is reached at output, or V_{OL}

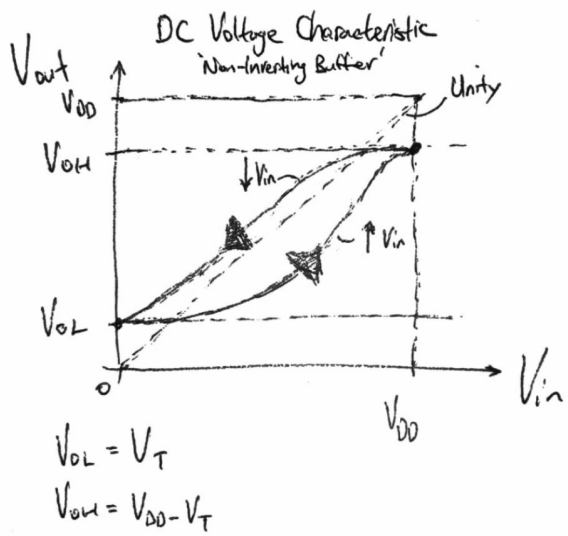


Figure 1. DC Voltage Characteristic of a 'Non-inverting Buffer' depicting hysteresis

c) Ideally, gain should be 1. However from the plot, we see slopes that indicate not 1, because of the fact that V_{in} of 0 to V_{DD} does not correspond to a V_{in} of 0 to V_{DD}, but rather V_{OL} to V_{OH} which each differ by V_T. Also, the output high and low must be above and below V_{IL} respectively, which is not the case. Thus the circuit is not a valid gate. Output is not ideal; output low is not tied to zero, but rather V_T because the PMOS turns off before V_{OL} reaches 0 V.

d) CAD Tool Validation with $V_{DD} = 0.9$ V. Here is the buffer:

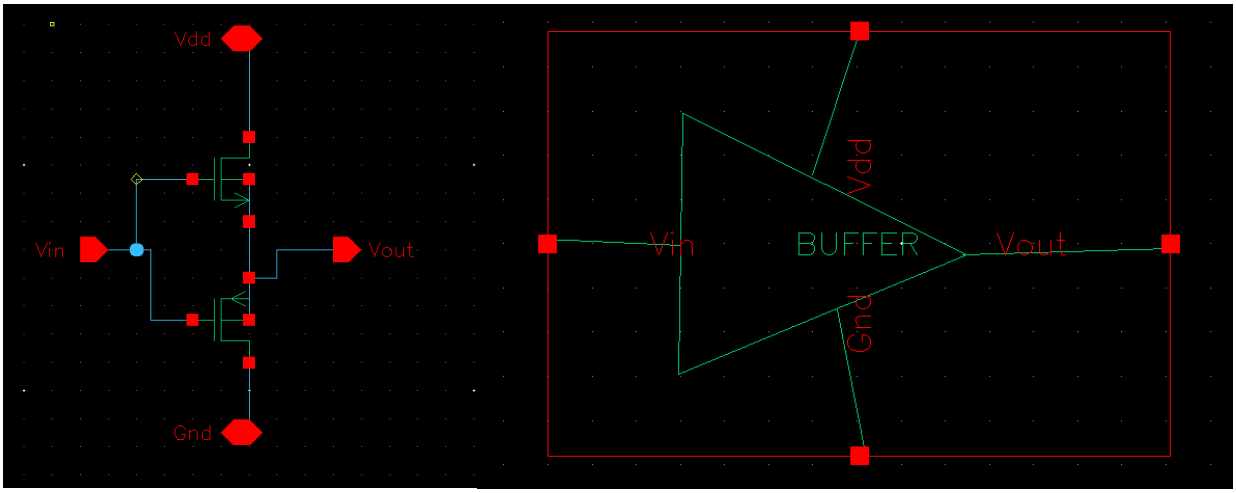


Figure 2. Buffer schematic (left) and buffer symbol (right)

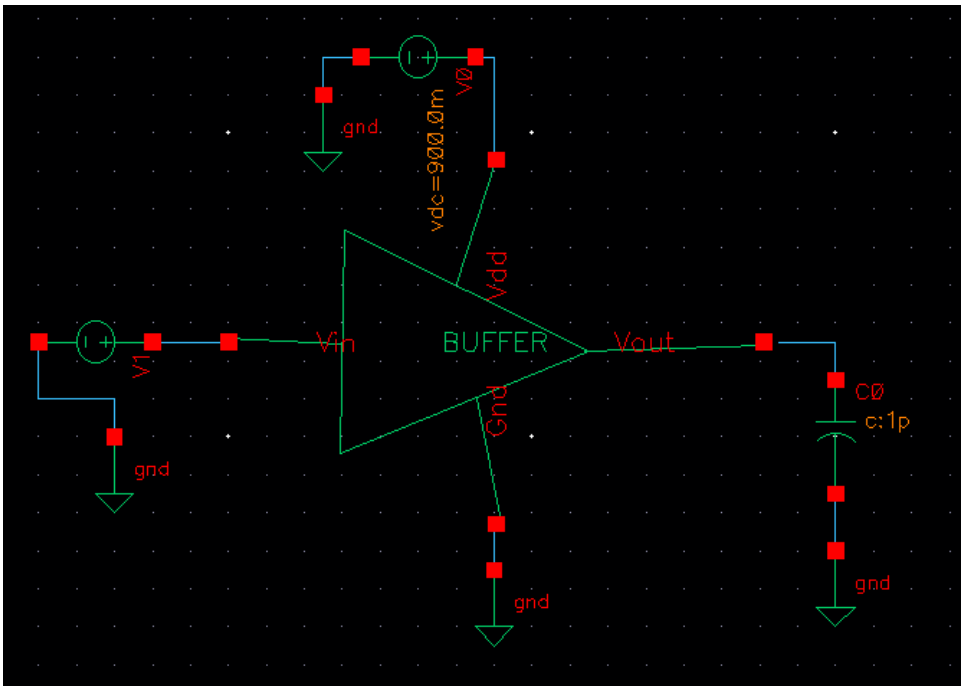


Figure 3. Buffer test bench circuit with V_{dd} = 0.9 V and V_{out} attached to 1pF capacitor.

Figure 4. Sweep of V_{in} from 0 to 0.9 V (Green) with output V_{out} (Red).

Figure 5. Differences in Input vs Output (Not exactly 0 to V_{DD})

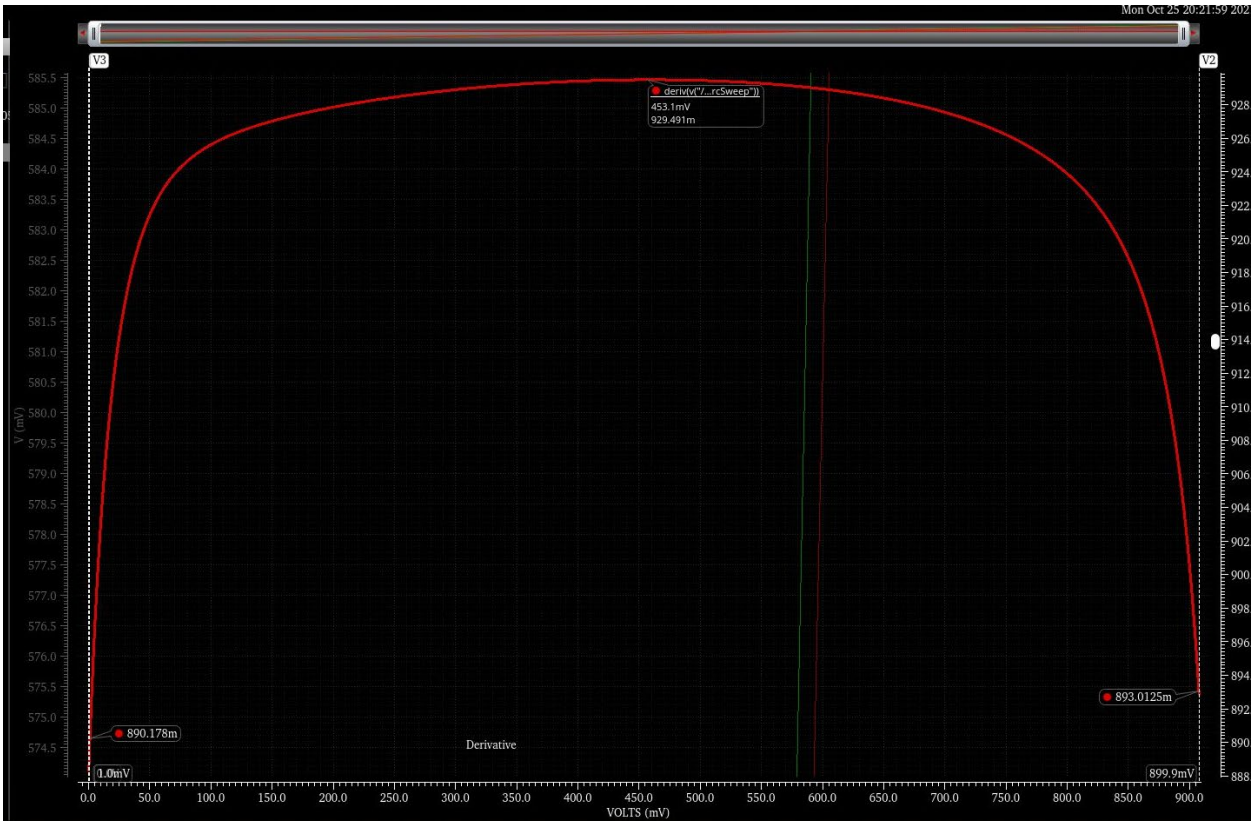
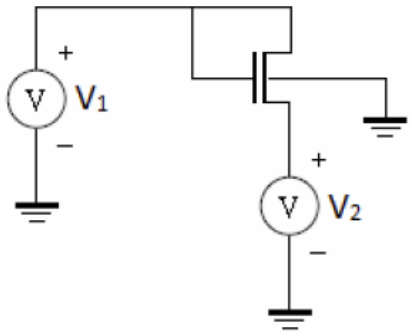


Figure 6. Derivative of output.

From figure 5, we can see that there are differences between Vin and Vout and it does not match 1:1 due to the bound of V_T. Figure 6 tells us information about the gain. Although it has a high gain region between two low gain regions, the gain must be greater than 1 for the high gain region, so the design is still invalid. Hysteresis is difficult to see in the outputs, which can be explained that perhaps there is not much hysteresis as is exaggerated by the hand-drawn plot in figure 1.

3. Figure shows a circuit used to measure the effective value of body effect factor (γ) (by measuring V_T at different source voltages) and channel length modulation factor (λ) (by measuring I_d at different Vds values). Assume in formula for threshold voltage (slide 7 lecture set 4 – MOS basics), $2\varphi_F = 0.88$ V, and calculate VT0, γ, and λ for a device with 2 fingers. Can you justify the value of γ for the FinFET device you are simulating? Attach your CAD netlist, graphs and measurement data to your answers (**25 points**)



a) Body effect factor

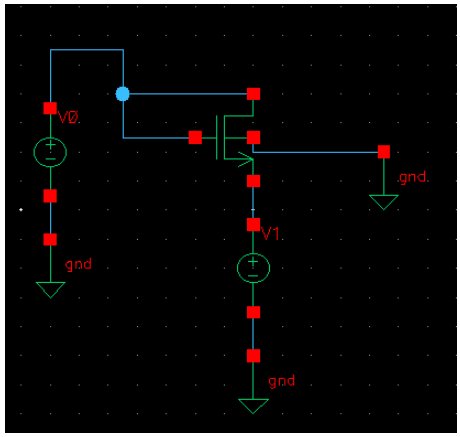


Figure 7. Body Effect schematic

We measure V_T at different source voltages. V2 is fixed to a certain value, and DC sweep is performed for V1 from 0 to 5 V and V_T is measured at the point where current rises, with arbitrary threshold at 1 µA.

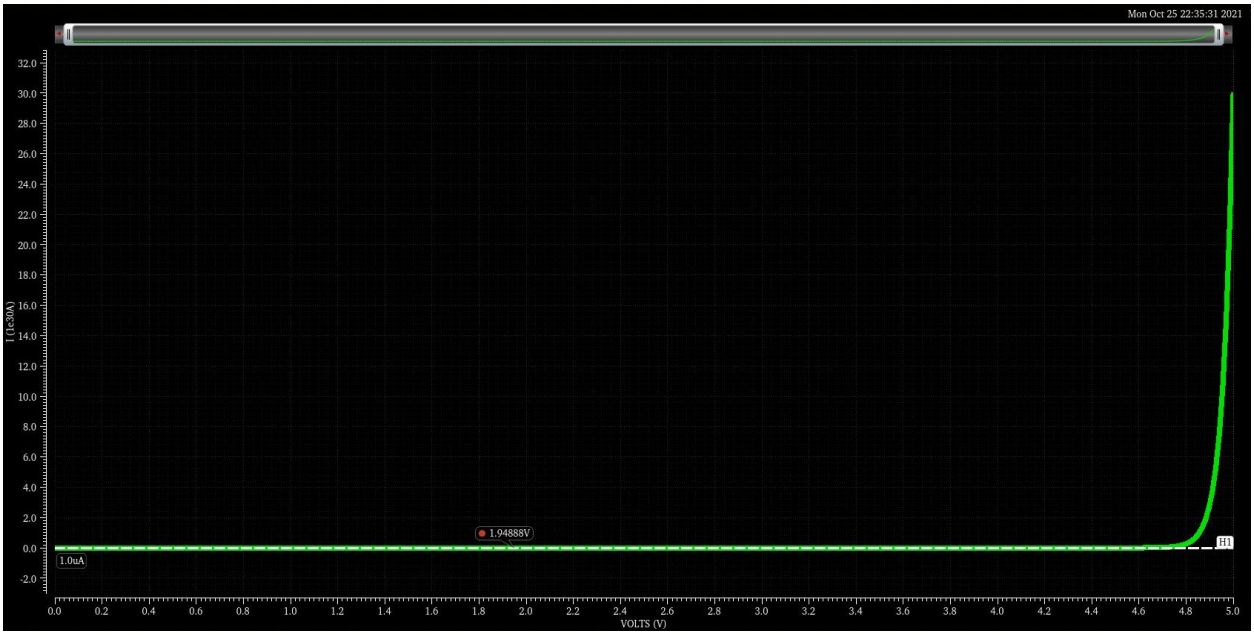


Figure 8. Sample plot of V_{in} vs I_{DS}, where marker is placed at threshold of 1 µA. V_T is recorded and put into a table.

Note that for all $V_2 > 0$, we will need to subtract V_T by V_2 since that $V_{DS} = V_1 - V_2$.

V_2 (V)	V_{raw} (V)	V_T (V)
0	1.653	1.653
0.1	1.752	1.652
0.2	1.850	1.650
0.3	1.949	1.649
0.4	2.048	1.648
0.8	2.443	1.643
1.1	2.740	1.640
1.5	3.137	1.637

Table 1. Values collected for V_T while varying V_2.

Now we can use the formula below to calculate body-effect:

$$V_T = V_{T_0} + \gamma(\sqrt{V_{SB} + |2\phi_f|} - \sqrt{|2\phi_F|})$$

We're given $2\phi_F$ in the question, and V_{T0} is calculated to be 1.653 when $V_{SB} = 0$. V_{SB} is V_2.

V_2 (V)	V_T (V)	$\gamma(\sqrt{V})$
0	1.653	0
0.1	1.652	-0.01928
0.2	1.650	-0.02966
0.3	1.649	-0.02699
0.4	1.648	-0.02587
0.8	1.643	-0.02793
1.1	1.640	-0.02772

1.5	1.637	-0.02646

Table 2. Calculated body-effect using formula above

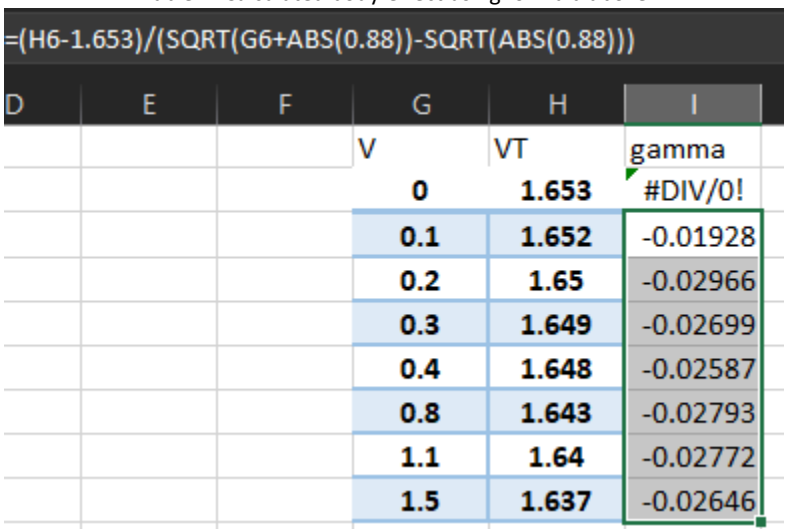


Figure 9. Excel calculated value with formula at top of figure.

Thus we see that body-effect varies from ~-0.02 to -0.026 given varying voltage between source and substrate bulk. Since V_T is basically constant for varying levels of V_{GS}, we can conclude that body effect has a minimal effect on the threshold voltage of the transistor and is relatively insignificant in this case.

Netlist is below:

```
** Generated for: hspiceD
** Generated on: Oct 25 22:40:24 2021
** Design library name: ELEC402
** Design cell name: blackbody
** Design view name: schematic
.PARAM v1=1 v0=0


.PROBE DC
+    I2(m0)
.DC v0 0.0 5.0 1e-3

.TEMP 25.0
.OPTION
+    ARTIST=2
+    INGOLD=2
+    PARHIER=LOCAL
+    PSF=2
.LIB "/ubc/ece/data/cmc2/kits/ncsu_pdk/FreePDK15/hspice/models/fet.inc" CMG

** Library name: ELEC402
** Cell name: blackbody
** View name: schematic
m0 net1 net1 net2 0 nfet AD=608e-18 AS=608e-18 PD=168e-9 PS=168e-9 M=2
v1 net2 0 DC=1.5
v0 net1 0
.END
```

Figure 10. Netlist for Q3 circuit.

b) Channel Length modulation factor (λ)

Figure 11. Setting sweep of V_{DS} from 0 to 100 V.

Below two methods will be used: method one uses figure 11 with a very high V (also rip transistor). Method two sweeps to 5 V and draws a line yielding a similar result for channel length modulation factor (intercept at ~4.6V – 1.65 = 2.95 V = V_{GS}). See figure 12.

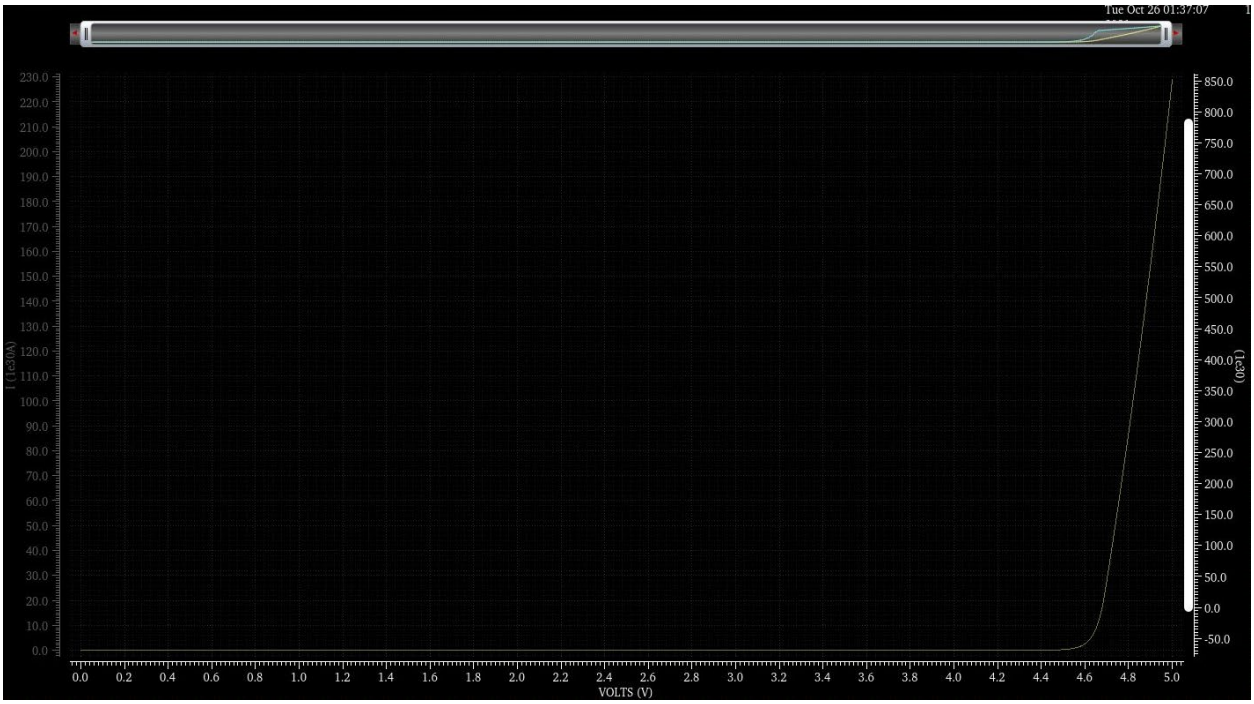


Figure 12. Sweep from 0 to 5 volts. This yields a similar result to finding the derivative for the hyperbole sweep if a best-fit line is drawn to find the intercept.

Channel-length Modulation
(I_{DS} dependence on V_{DS})

$$I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Large drain-source voltage makes the channel effectively smaller, i.e. larger drain current

The reduction in the effective length is due to the increase in the *depletion width* of reverse-biased pn junction.

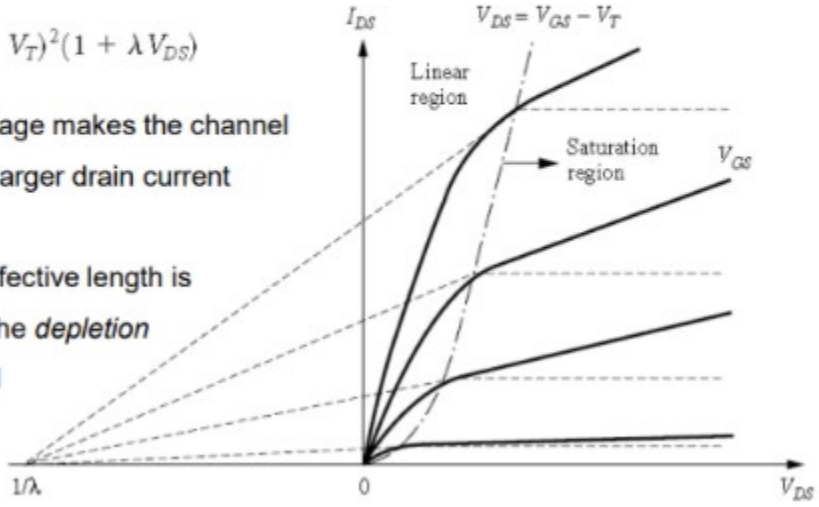


Figure 13. Slide on how to find channel length modulation.

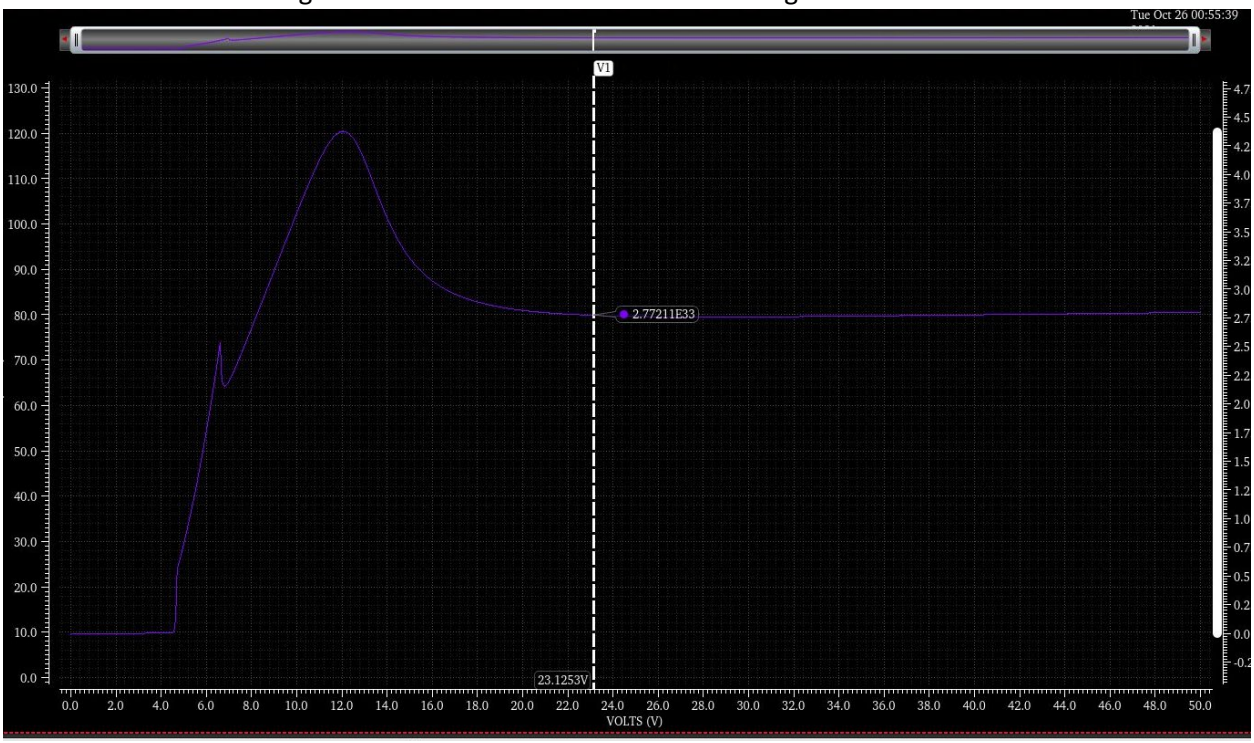


Figure 14. Derivative to get slope of linear ~= 2.77211E33.

Knowing a point (23.1253, 55.6863E33) we can use y = mx + b, and solve for b first, then get point at which y = 0:

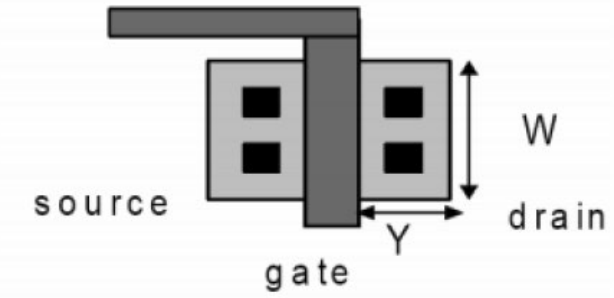
$$y = mx + b$$
$$55.6863E33 = 2.77211E33(23.1253) + b$$
$$b = -8.4196E33$$

For (x, 0):

$$y = 2.77211E33(x) - 8.4196E33$$
$$0 = 2.77211E33(x) - 8.4196E33$$
$$x = 3.03725$$

This is similar to the intercept we get with a 0-5V sweep, 2.95 V. See text above figure 12 for context. Following figure 13, we get λ = 1/x ~= 0.329 or 0.339 depending on following the 100 V sweep or 5 V sweep.

4. Consider the layout in the figure below implemented in a 180nm technology. Assume that the transistor has W=900nm, L=180nm and a source/drain dimension Y=800nm and a lateral diffusion of 22nm. Let tox =40 Å (Angstroms). (12 points)



a. Compute the worst case gate capacitance per unit width, C_g, in units of fF/um. Estimate C_{GS}, C_{GD} and C_{GB} in linear, saturation and cutoff, including overlap effects.

b. If $N_A=3x10^{16}/cm^3$ and $N_D=3x10^{19}/cm^3$, x_j=300nm, compute the worst-case capacitance value per unit width, C_j, in units of fF/um.

c. Compute the drain junction capacitance for the following cases (m=0.5):
   i. V_D=1.8V, V_B=0V
   ii. V_D=0V, V_B=0V

a) First we need C_{ox}, computed using:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = \frac{3.9\epsilon_0}{40E-10} = 8.63283E-3\frac{F}{m^2}$$

ε_{ox} is the SiO_2 permittivity * free space permissibility (F/m). Thickness (m), t_{ox}, is given in the question. We also need C_{ov} computed using:

$$C_{ov} = C_{ox} * L_{diffusion} = 1.8992226E - 10\frac{F}{m}$$

$L_{diffusion}$ is given in the question (m), and we've just previously solved for C_{ox}, (F/m^2). We can also assume fringe capacitance C_f is 0 since T_{poly} is not given.

We also need worst total gate capacitance C_g per unit width:

$$C_g = C_{ox}L = 1.5539094E - 9\frac{F}{m} = 1.554\frac{fF}{\mu m}$$

L is given in question (m). Overlap is not included.
If we include overlap, then it becomes:

$$C_{go} = 2C_{ov} + C_g = 1.93375392E - 9\frac{F}{m} = 1.93\frac{fF}{\mu m}$$

There is two of C_{ov} due to parallel capacitances. Width isn't in calculation because this is in terms of unit width.

	Cutoff	Linear	Saturation
C_{GS}	C_{ov}	$1/2C_gW + C_{ov}$	$2/3C_gW + C_{ov}$
C_{GD}	C_{ov}	$1/2C_gW + C_{ov}$	C_{ov}
C_{GB}	C_gW	0	0

Table 3a. Capacitance equations for gate-source, gate-drain, gate-bulk.

	Cutoff	Linear	Saturation
C_{GS}	0.19	0.89	1.12
C_{GD}	0.19	0.89	0.19
C_{GB}	1.4	0	0

Table 3b. Capacitance values for gate-source, gate-drain, gate-bulk. Units in fF/µm

b) Now we want to find C_j in units of fF/µm. We first need the voltage asymptote ϕ_B:

$$\varphi_B = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) = 0.936\ V$$

These constants are from the question.
Now we want C_{jb}:

$$C_{jb} = \sqrt{\frac{\varepsilon_{Si} q}{2\varphi_B}\frac{N_A N_D}{n_i^2}} = 0.516\frac{fF}{\mu m^2}$$

We use Si permittivity * free space permissibility.
Now we can solve for C_j:

$$C_j = \frac{C_{jb}(Y + 2x_j)W}{\left(1 - \frac{V_j}{\varphi_B}\right)^m} = C_{jb}(Y + 2x_j)W = 0.650\ fF$$

M is 0.5. Worst case takes into account both sides as well as $V_j = 0$ V. Y is given in the question, and so is x_j and W.

c) Drain junction capacitance equation is the same as in b, but just single x_j:

$$C_{drain} = \frac{C_{jb}(Y + x_j)W}{\left(1 - \frac{V_j}{\varphi_B}\right)^m}$$

i. With V_j = -1.8 V, we get C_j = 0.299 fF.
ii. With V_j = 0 V, we get C_j = 0.511 fF.

5. A CMOS inverter in 45 nm technology has a pull-up device that is 8λ:2λ and a pull-down device that is 4λ:2λ. It drives four identical inverters at its output. Compute the inverter delay (use C_g = 2 fF/um) and assume a ramp input. Re-calculate the delay if we have a chain of 4 inverters, i.e. 4 inverters in series **(13 pts)** Note: 2λ = 45nm

a) Inverter delay with four identical inverters at output. Pull-up means PMOS W/L 8λ:2λ, pull-down means NMOS W/L 4λ:2λ. Assuming C_g = 1fF/um from the useful formulas, knowing that 2λ = 45nm:

$$C_L = C_g * (W_n + W_p) = \frac{2fF}{\mu m} * (4 * 0.09\mu m + 4 * 0.18\mu m) = 2.16\, fF$$

The 4 times is for the parallel capacitances at the output of the inverter. Similarly:

$$C_{self} = C_{eff} * (0.09\mu m + 0.18\mu m) = 0.27\, fF$$

And then we can sum the two to get the total capacitance:

$$C_{total} = C_{self} + C_L = 2.43\, fF$$

For delay, as given in class we can approximate the resistance as R = R_{eqn} (L/W), where 45nm R_n is 34k Ω μm and R_p is 68 kΩ μm. We also know that ramp is just RC:

$$\tau^n_{ramp} = \tau^p_{ramp} = RC = 34\, k\Omega * ½ * C_{total} = 41.31\, ps$$

b) Inverter delay with series of 4 identical inverters, so 5 inverters in total in series.

Each inverter would have an equivalent C_{self} = 0.27 fF. Since its cascading, we can simply multiply by 5 to get the equivalent C_{total} = 5C_{self} = 1.35 fF. The load here is a wire. Thus:

$$\tau^n_{ramp} = \tau^p_{ramp} = RC = 34\, k\Omega * ½ * C_{total} = 22.95\, ps$$

References:

Useful physical constants: https://onlinelibrary.wiley.com/doi/pdf/10.1002/9781119009597.app3