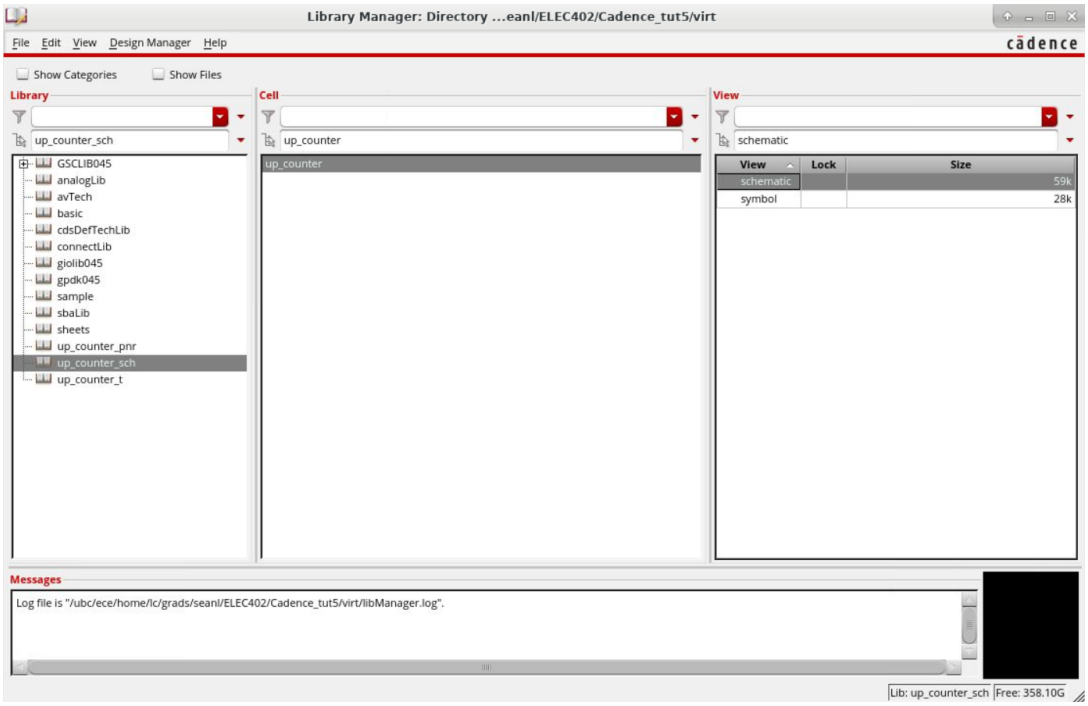
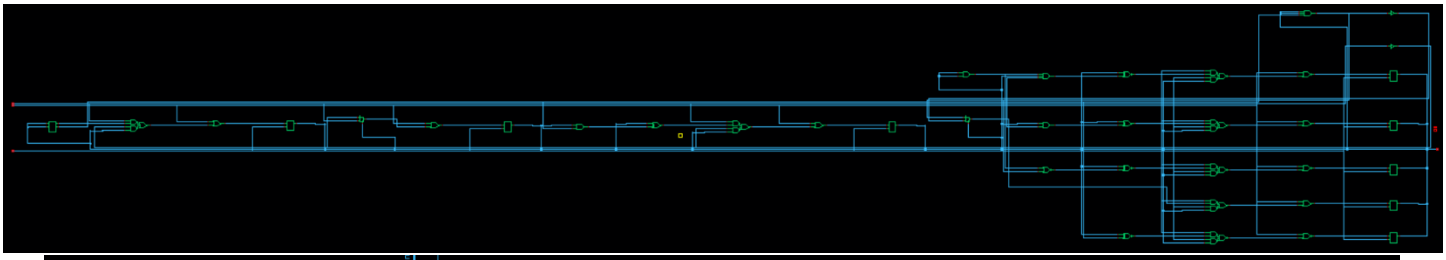
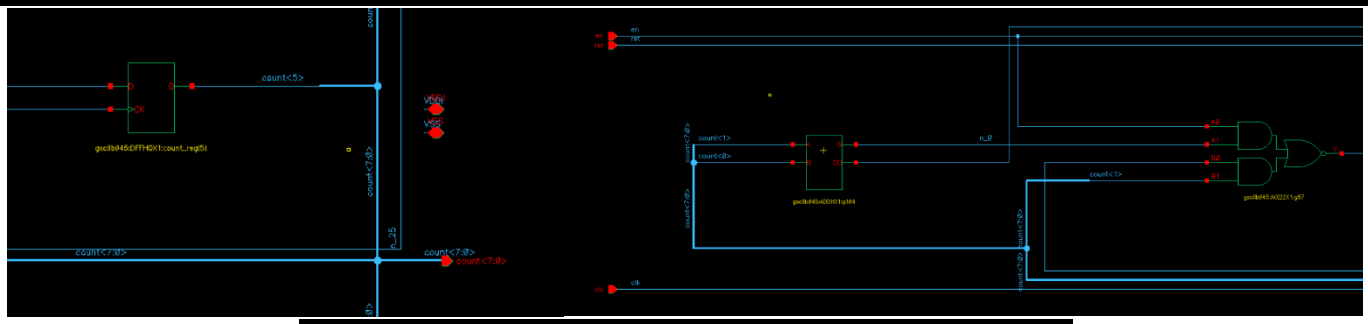
Tutorial 5 Addendum: Simulating PnR Circuit

ELEC 402 - Updated Nov. 17, 2021

To simulate our PnR generated layout, we need to set up our testbench and model libraries in Virtuoso to simulate properly. This tutorial follows **after** the Place and Route tutorial when we have the schematic symbol, schematic, and layout in Virtuoso. The following shows where we left off:



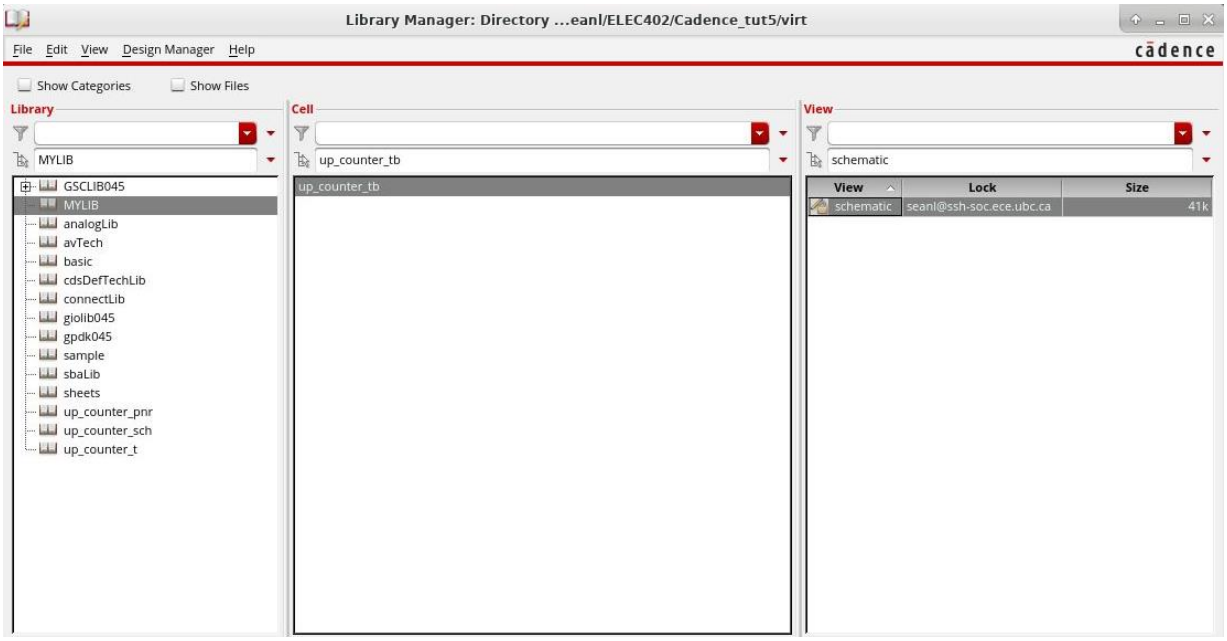




To create a testbench and simulate our PnR layout, follow the below steps:

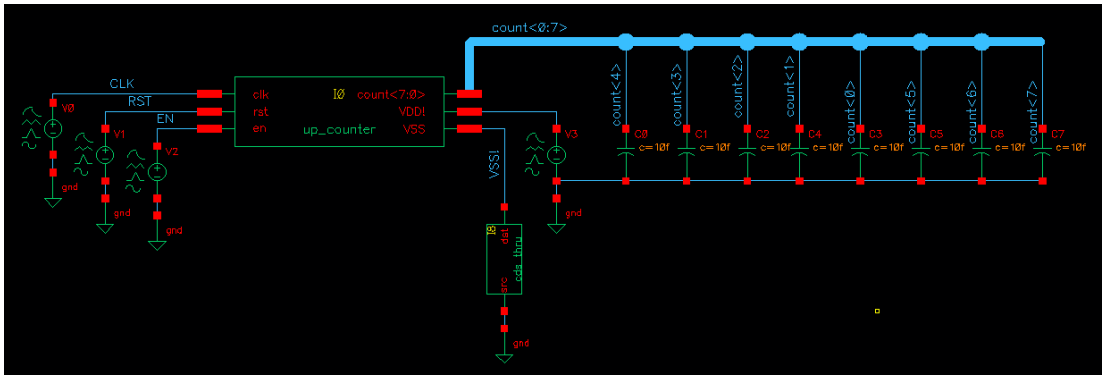
Steps

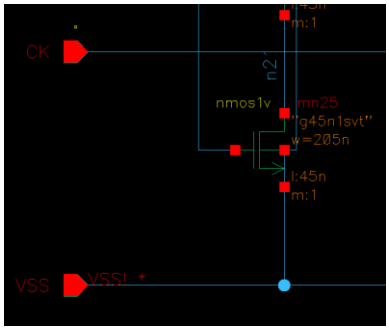
1. Create a new library for your testbench. Here, “MYLIB” library is created with a schematic cell called “up_counter_tb”:

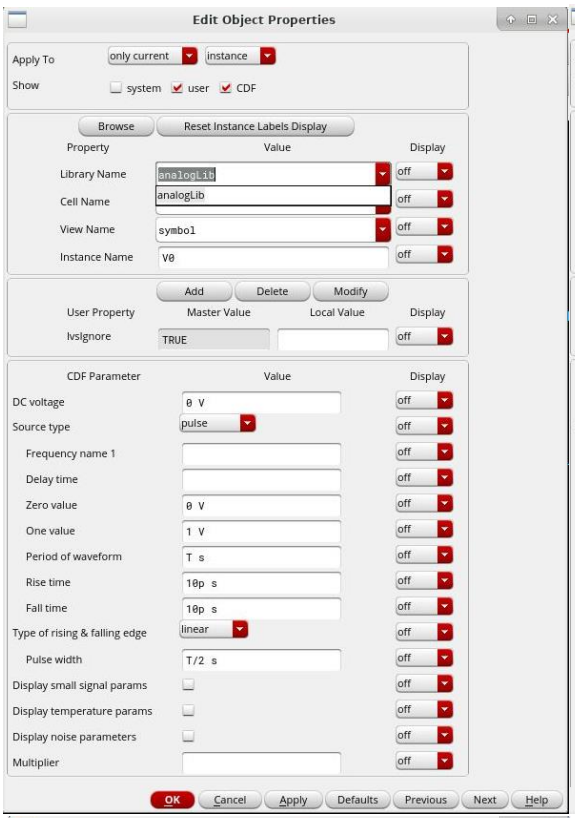


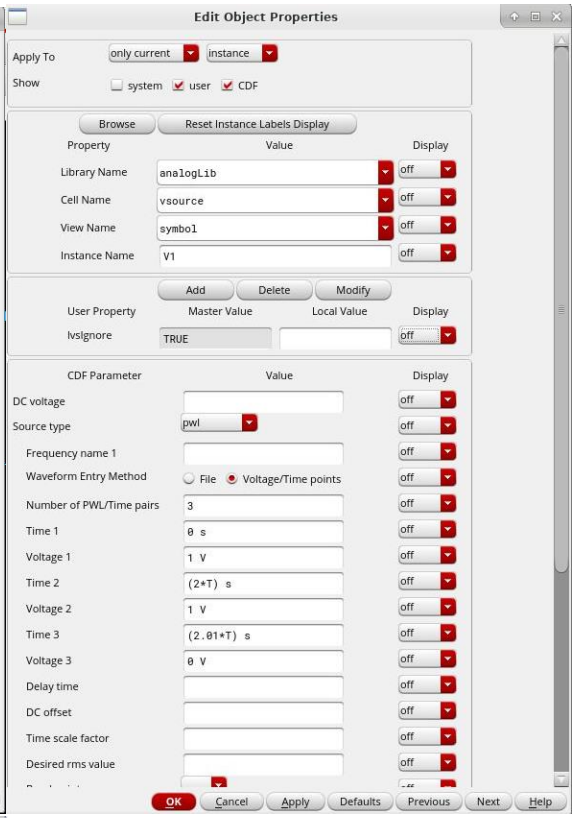
2. Open the schematic and create your testbench. Here, “vsource” components are taken from “analogLib” to generate signals and VDD (see below images for their settings).

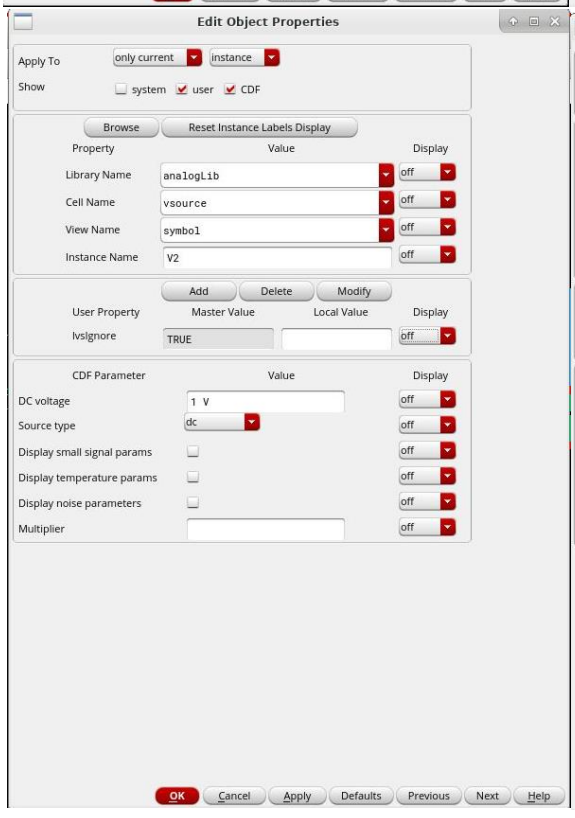
   IMPORTANT: Recall we specified a global net called “VSS” during place and route. This global net is actually called “VSS!” in the schematic (descend into the “up_counter” symbol and descend into gates until you reach the transistor level schematic to see how “VSS” is connected to “VSS!”). **To connect the “gnd” symbol to “VSS!”, we need to use the “cds_thru” cell from the “basic” library and connect to a wire that has the label “VSS!” (see schematic below).** This ensures “gnd” is connected to the transistors.

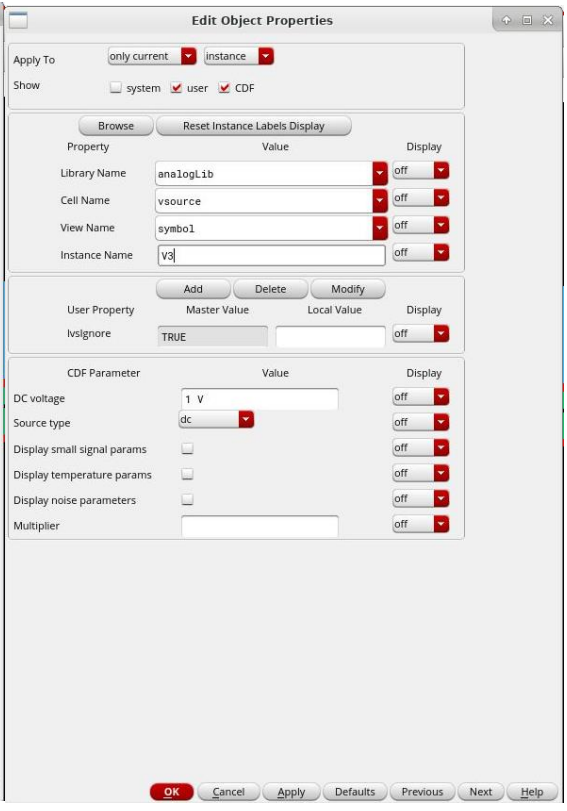




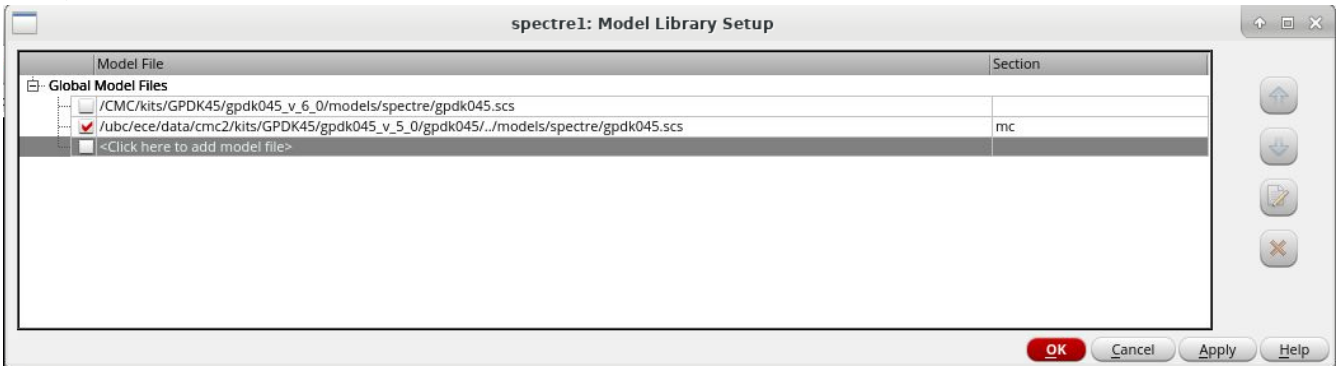

Edit Object Properties
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
analogLib
Cell Name
analogLib
View Name
symbol
Instance Name
V0
Add
Delete
Modify
User Property
Master Value
Local Value
Display
lvsIgnore
TRUE
CDF Parameter
Value
Display
DC voltage
0 V
Source type
pulse
Frequency name 1
Delay time
Zero value
0 V
One value
1 V
Period of waveform
T s
Rise time
10p s
Fall time
10p s
Type of rising & falling edge
linear
Pulse width
T/2 s
Display small signal params
Display temperature params
Display noise parameters
Multiplier
OK
Cancel
Apply
Defaults
Previous
Next
Help


Edit Object Properties
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
analogLib
Cell Name
vsource
View Name
symbol
Instance Name
V1
Add
Delete
Modify
User Property
Master Value
Local Value
Display
lvsIgnore
TRUE
CDF Parameter
Value
Display
DC voltage
Source type
pwl
Frequency name 1
Waveform Entry Method
File
Voltage/Time points
Number of PWL/Time pairs
3
Time 1
0 s
Voltage 1
1 V
Time 2
(2*T) s
Voltage 2
1 V
Time 3
(2.01*T) s
Voltage 3
0 V
Delay time
DC offset
Time scale factor
Desired rms value
OK
Cancel
Apply
Defaults
Previous
Next
Help


Edit Object Properties
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
analogLib
Cell Name
vsource
View Name
symbol
Instance Name
V2
Add
Delete
Modify
User Property
Master Value
Local Value
Display
lvsIgnore
TRUE
CDF Parameter
Value
Display
DC voltage
1 V
Source type
dc
Display small signal params
Display temperature params
Display noise parameters
Multiplier
OK
Cancel
Apply
Defaults
Previous
Next
Help

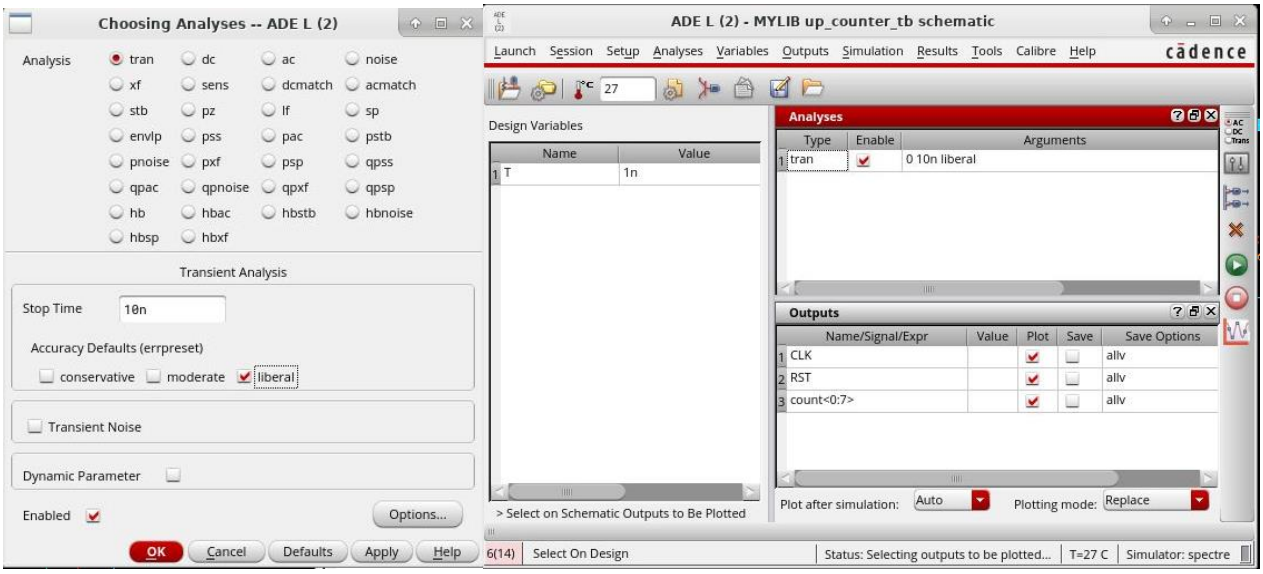

Edit Object Properties
Apply To
only current
instance
Show
system
user
CDF
Browse
Reset Instance Labels Display
Property
Value
Display
Library Name
analogLib
Cell Name
vsource
View Name
symbol
Instance Name
V3
Add
Delete
Modify
User Property
Master Value
Local Value
Display
lvsIgnore
TRUE
CDF Parameter
Value
Display
DC voltage
1 V
Source type
dc
Display small signal params
Display temperature params
Display noise parameters
Multiplier
OK
Cancel
Apply
Defaults
Previous
Next
Help

3. After creating your testbench schematic, open ADE L and set your simulator to “Spectre” and set your model libraries according to the following (ensure that only one gpdk045.scs library is checked and “Section” is set to “mc”):



OPTIONAL: You can set the “Section” parameter to other process corners to run simulations.

4. Set up your simulation settings and parameters. Then, “Netlist and Run”



5. Simulation window will open up where you can see the results: