ELEC 402 – November 14, 2021

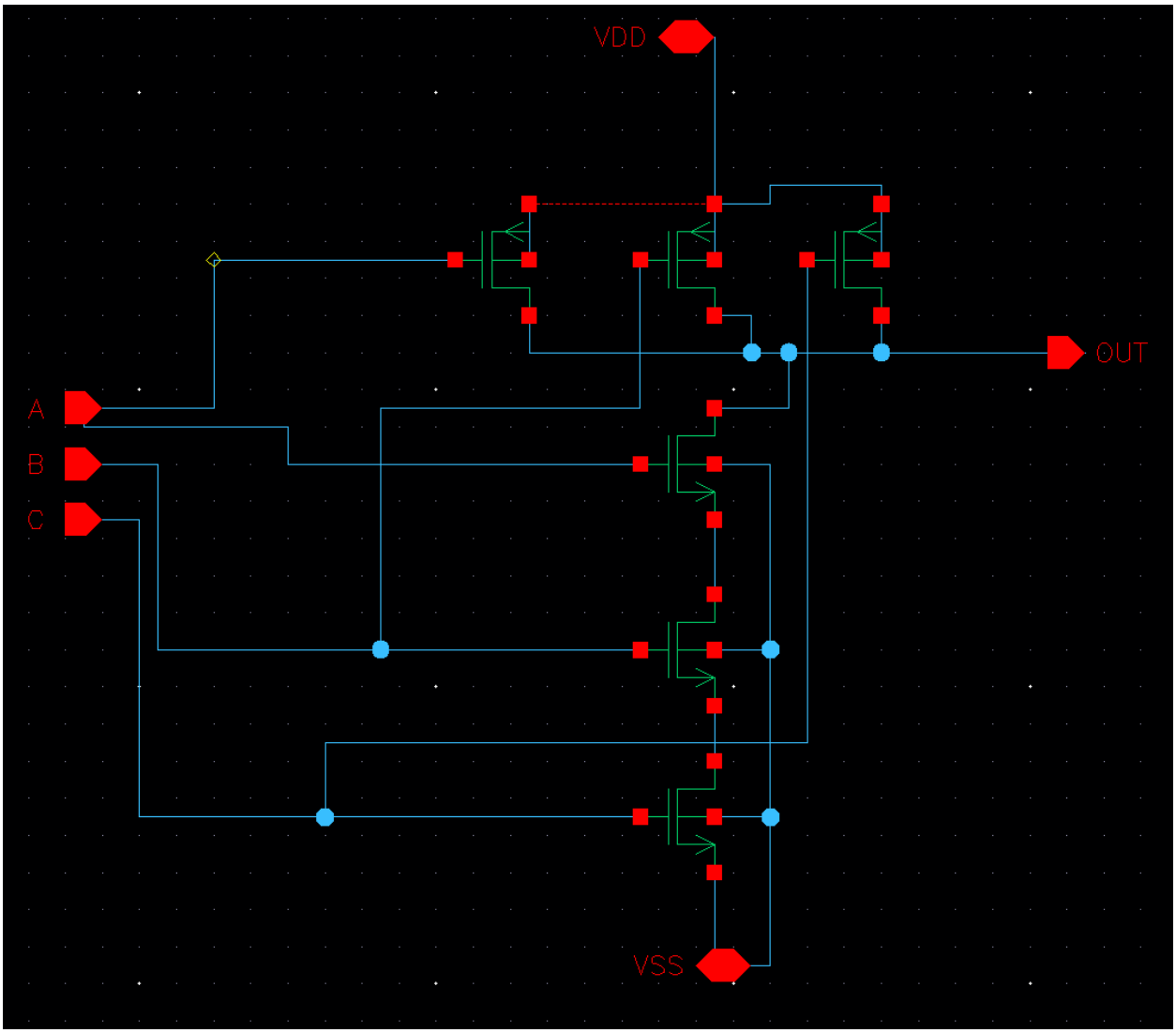
Project 4 Report

Martin Chua – 35713411

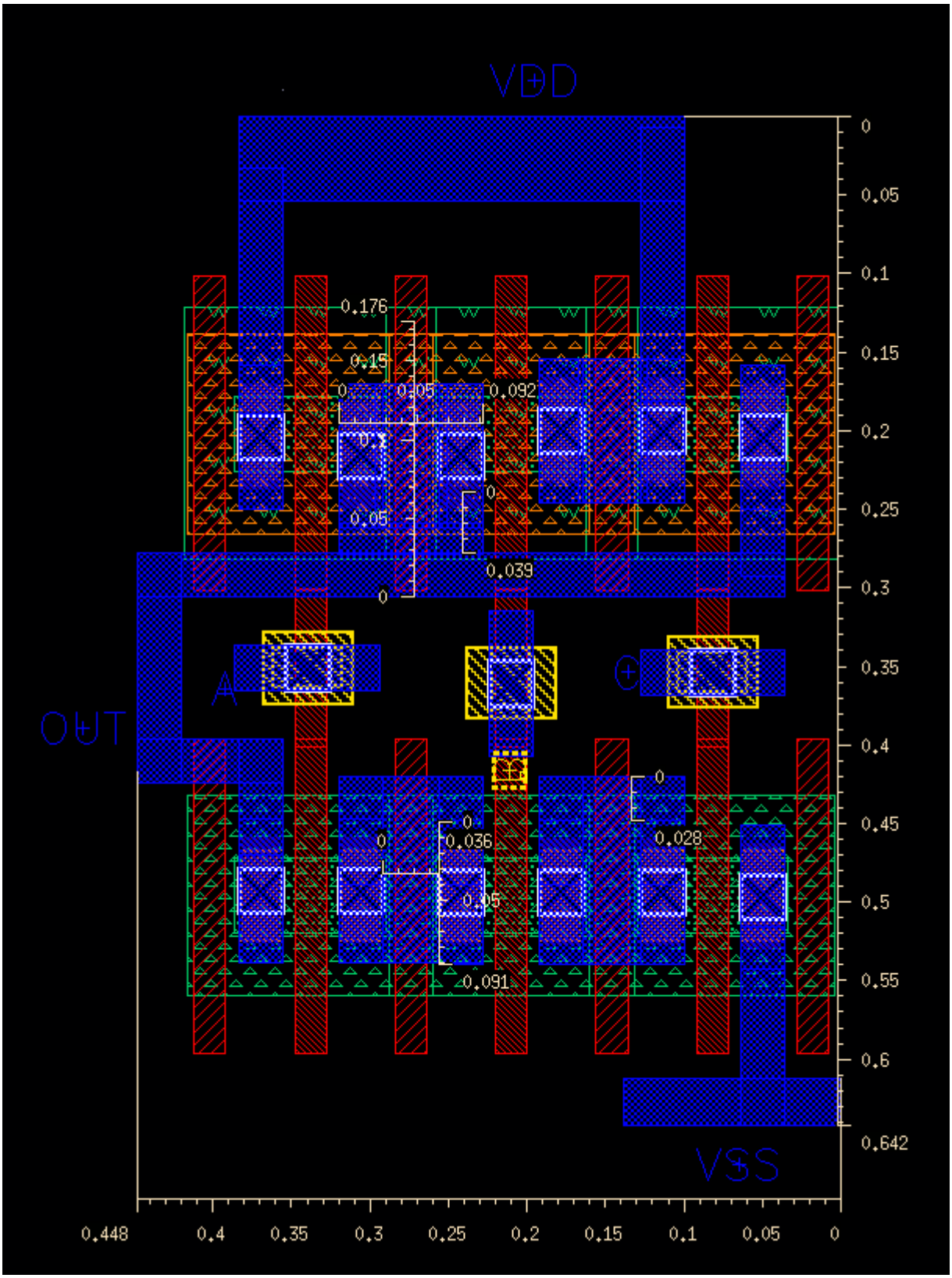
15nm FinFET

Area	Delay (avg)	Area X Delay
0.25978 um^2	23.636ps	6.14 $ps*um^2$

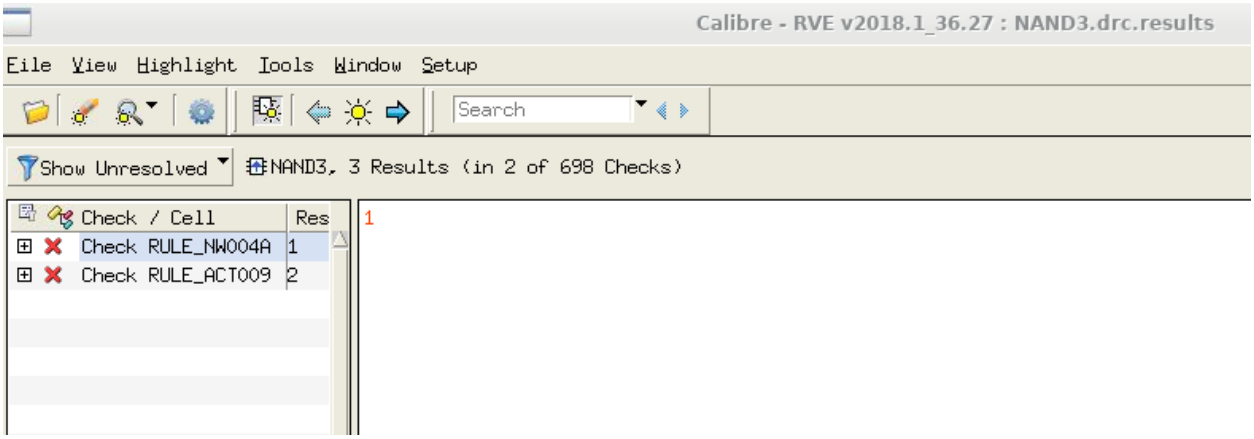
1. NAND3



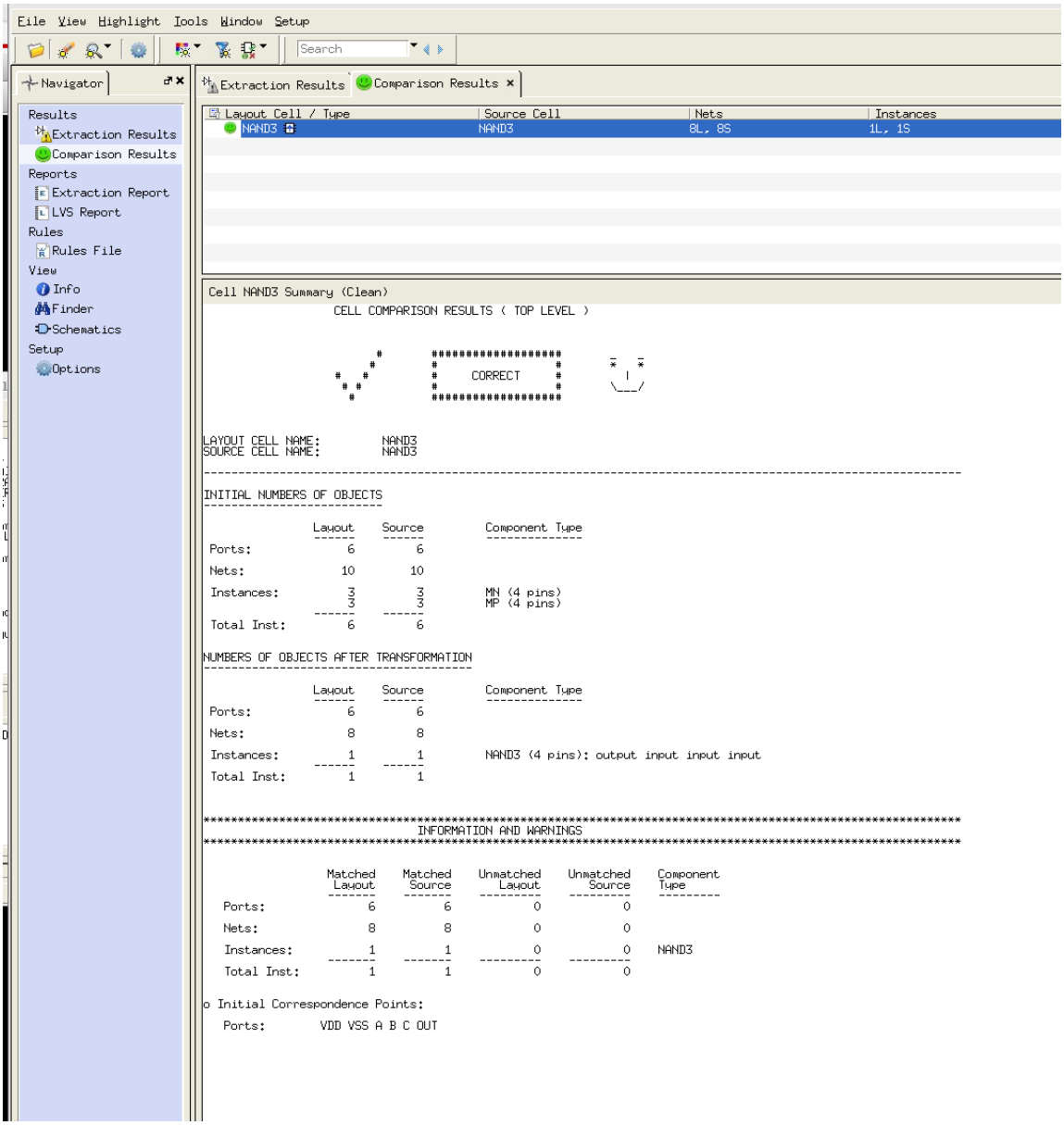
NAND3 Schematic using default widths (2 fingers)


VDD
VSS
OUT
A
C
0.176
0.15
0.092
0.05
0.039
0.036
0.028
0.091
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6
0.642
0.448

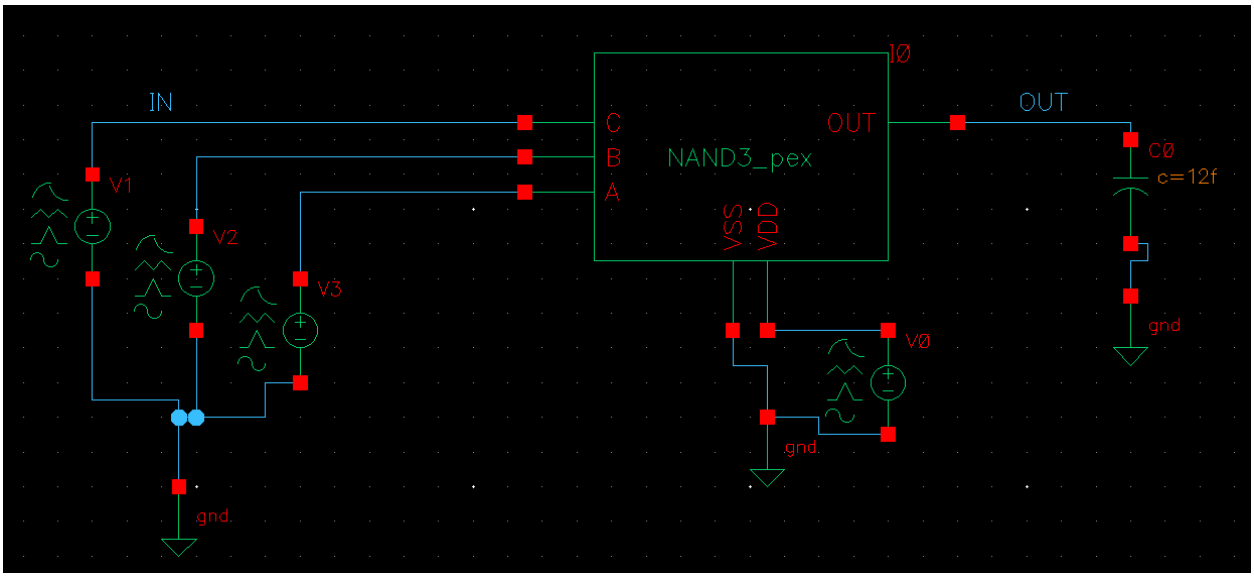
NAND3 Layout. Layout planned using the stick layout method / euler path taught in class, rather than directly translating from schematic to layout. In hindsight, it's possible to use 3 fingers for a two shared diffusion in the center.



DRC Results. DRC Summary can be found in Appendix A.



LVS Results pass! (Final LVS results in Appendix C)

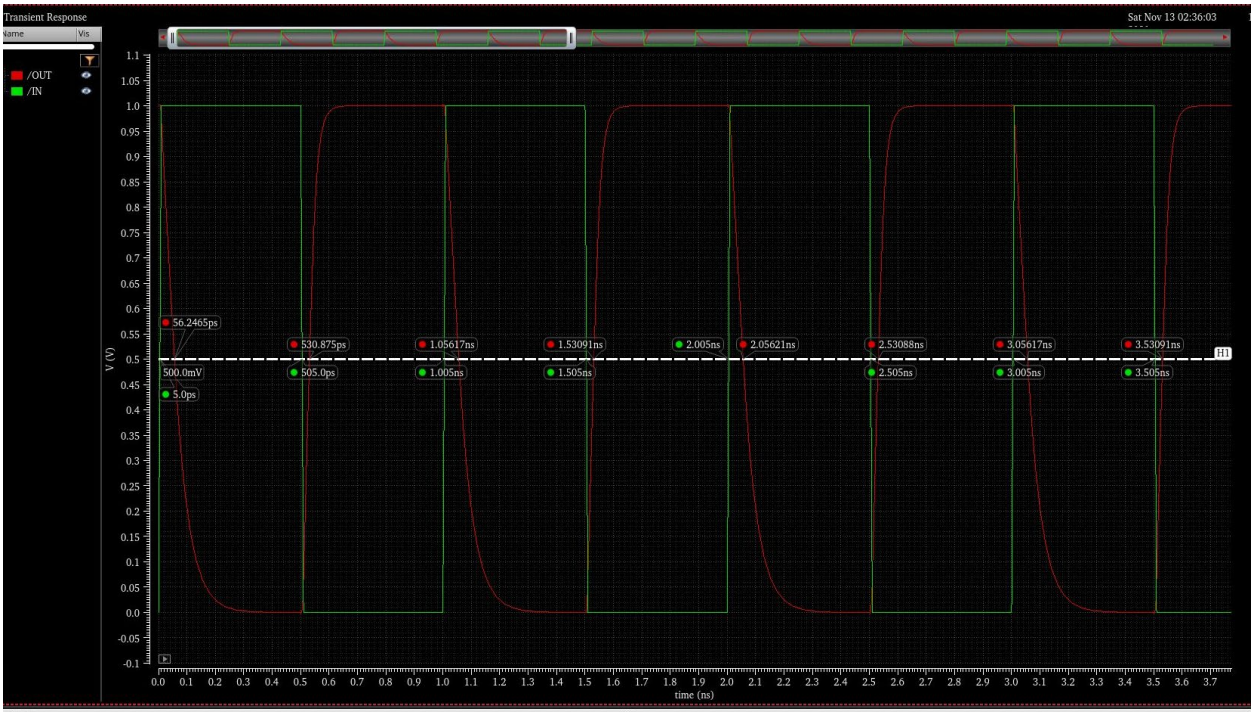


Worst case tau testbench schematic with 12 fF capacitor. V2 = V3 = VDD = 1 VDC. V1:

As seen in circuit schematic, worst case is when 1 transistor is off (pulled high) and others are on (pulled low) then the single transistor is also turned on (pulled low) and viceversa, aka 001 -> 000 -> 001. This is because all transistors are in series (pulldown) and parallel (pullup).

ivsignore	true
DC voltage	0 V
Source type	pulse
Frequency...	
Delay time	0 s
Zero value	0 V
One value	1 V
Period of ...	10n s
Rise time	10p s
Fall time	10p s
Type of rising...	

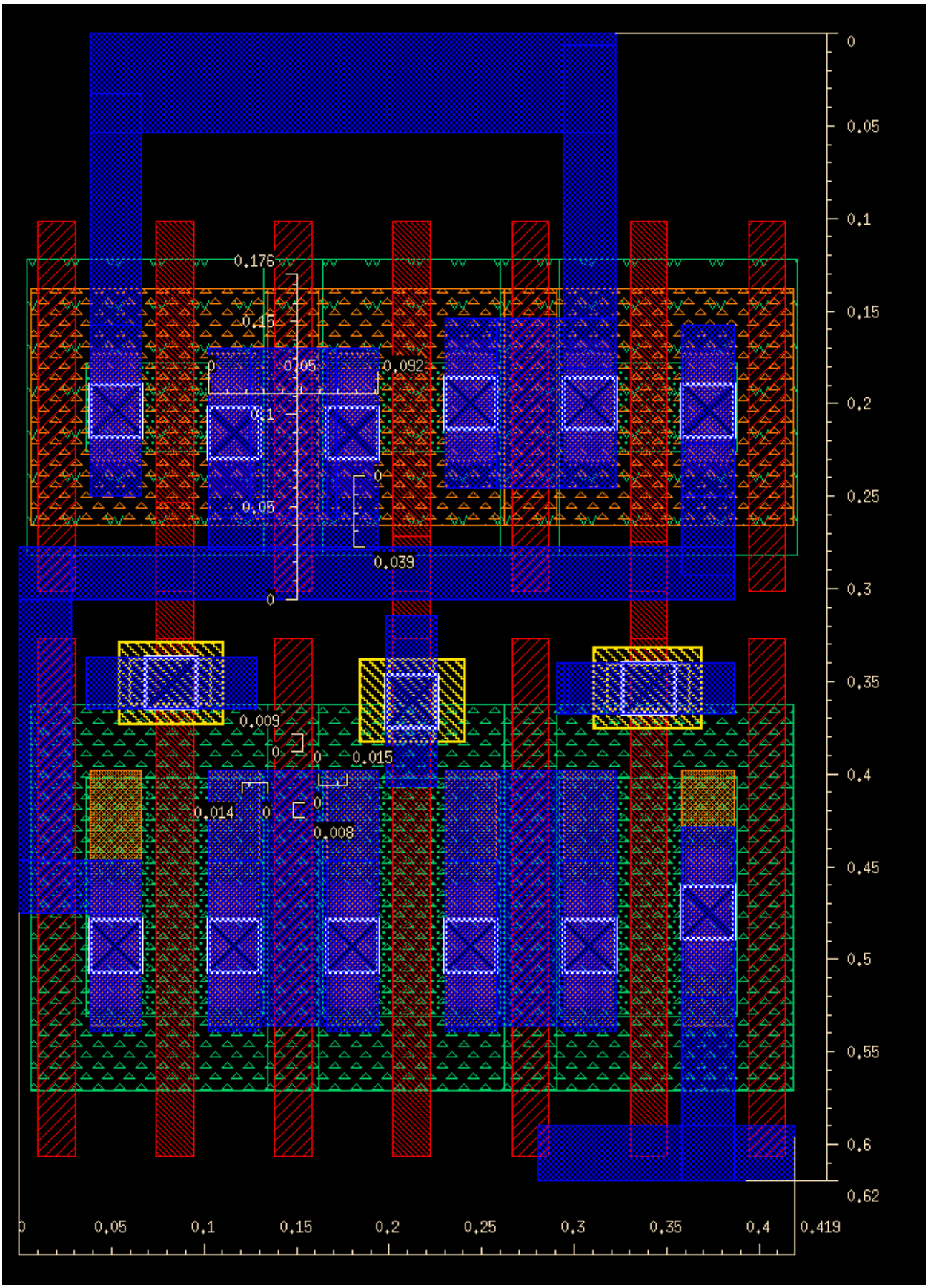
Rise and fall time is specified (slew rate) in the assignment as 10ps.



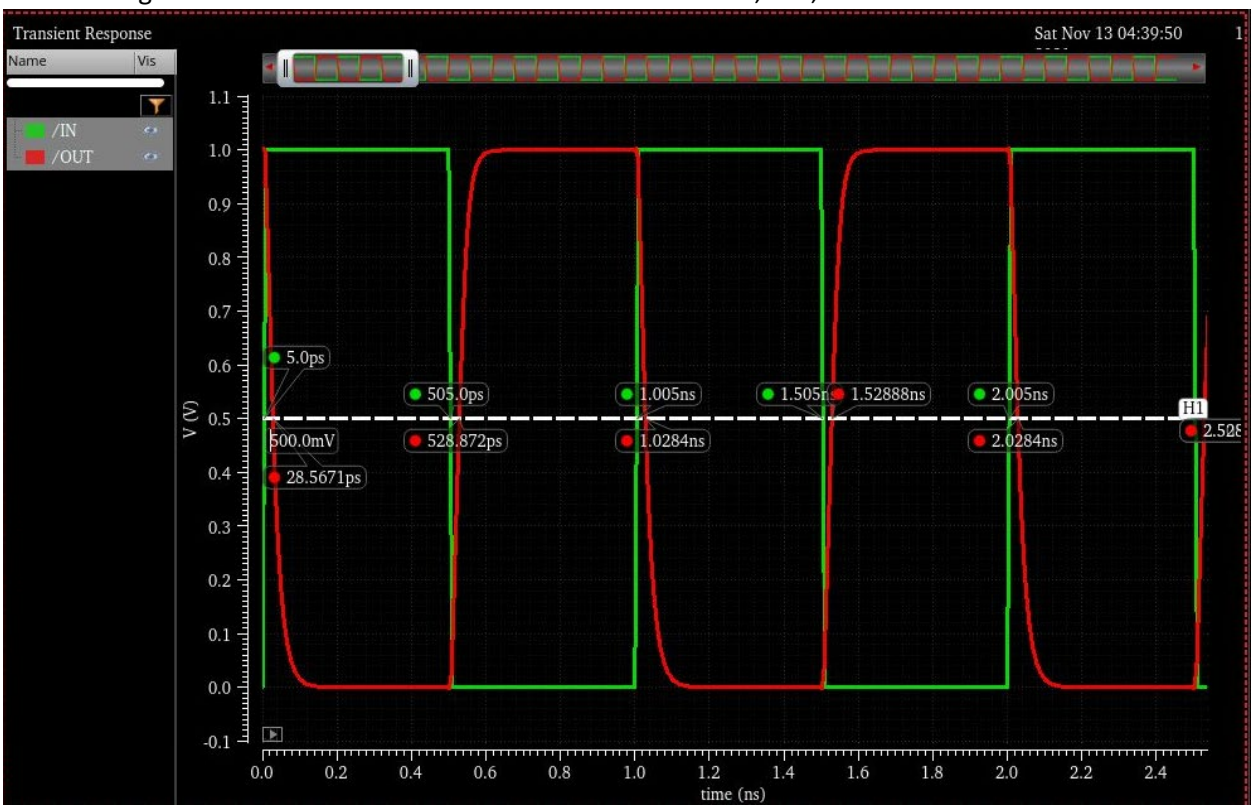
Tau with all parasitics from PEX. TpLH = 25.875 ps. TpHL = 51.17 ps.

This clearly does not match (not equal +-5ps) as specified by the assignment. Widths must be changed.

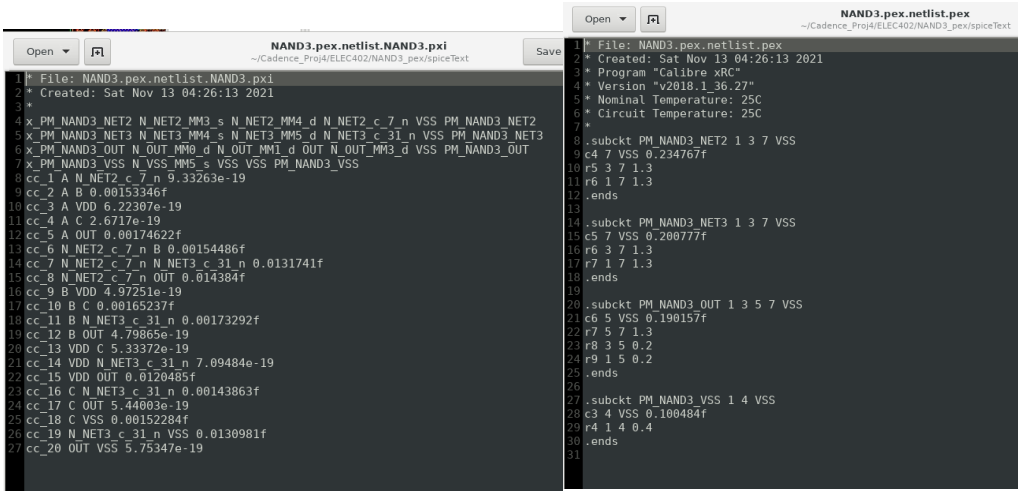
Let’s try doubling the width of the NMOS to 4 fingers (default 2):


0.176
0.46
0
0.05
0.092
0.1
0.05
0
0.039
0
0.009
0
0
0.015
0.014
0
0
0.008
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.419
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
0.6
0.62

I also managed to shrink it a little bit more and re-ran with DRC, LVS, and PEX.



Now**, TpLH = 23.872 ps and TpHL = 23.4 ps.** They match (equal)!

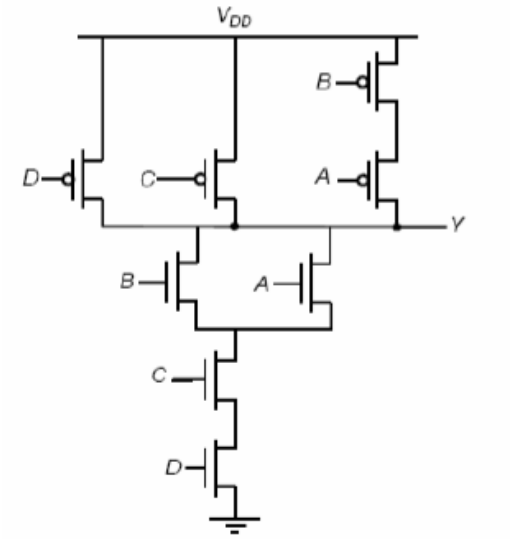


PEX Netlist.

Avg worst case delay is: 23.636ps.

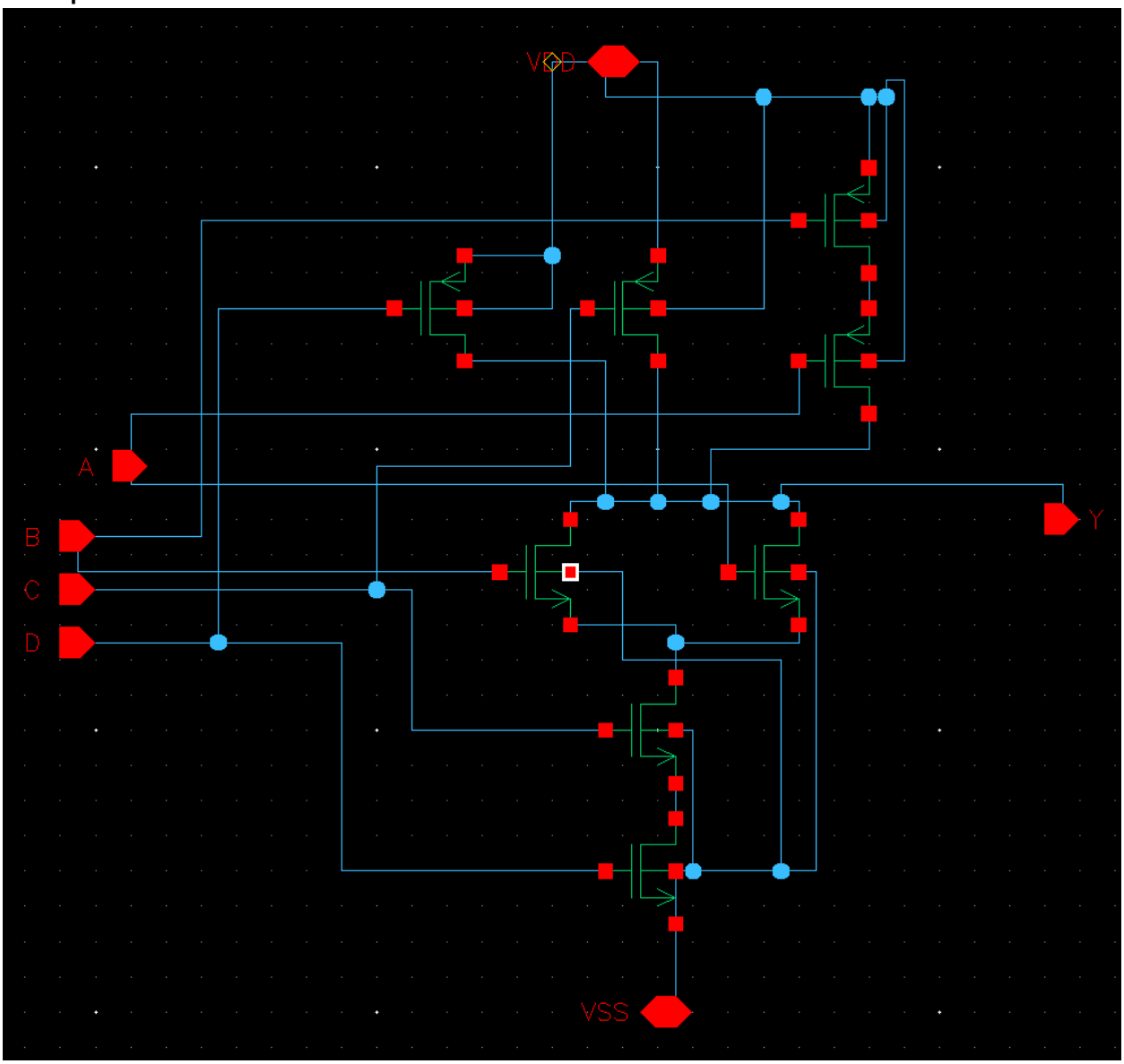
Thus, with area of 0.25978 um^2, the area x delay is 6.14 um^2 x ps. It is probably possible to shrink the area even further at the cost of repeatedly fixing DRC errors, but since fixing DRC + changing width + refixing DRC already took me tons of hours I'm going to not do that 😊.

2. Sizing and Timing of:



   a. The logic function (Boolean) can be obtained by observing the pull-down NMOS. We see A and B in parallel, followed by a series C and D. Hence: Y_bar = (A + B)CD and Y = (AB)_bar + C_bar + D_bar
   b. Sizing can be obtained by finding the worst case, then going off from there. We are told NMOS W/L is 4 lambda and PMOS W/L is 8 lambda.
      i. NMOS: Worst case is through A or B to C to D. There are three transistors, so all their widths are 4 * 3 = 12 lambda
      ii. PMOS: Worst case is through B to A. There are two transistors, so A and B are 8 * 2 = 16 lambda. Single branch for C and D makes them 8 lambda.
   c. Timing to get worst case tpHL and tpLH:
      i. tpHL: For high to low, we need the pull-down network to pull from high to low. So, D should be off initially and on afterwards. For the other ones, we want to maximize capacitance and as many to be up to VDD so that discharging takes the longest, so: ABCD = 1010 -> 1011
      ii. tlLH: For low to high, we need the pull-up network to pull from low to high. So, C and D should be on, and either B or A should also be on. This means that the PMOS side is not pulling up initially. As delay propagates, we want the most delay to be at the beginning, so A should be off and B should be on, then go off: ABCD = 0111 -> 0011.
      iii. Simulation:

15nm pdk circuit:



For the TB images below, V2 pulse (left) and ADE L settings (right):

lvsIgnore	true
DC voltage	0 V
Source type	pulse
Frequency...	
Delay time	0 s
Zero value	0 V
One value	1 V
Period of ...	10n s
Rise time	10p s
Fall time	10p s
Type of rising...	

Analyses

	Type	Enable	Arguments
1	tran	☑	0 10n moderate

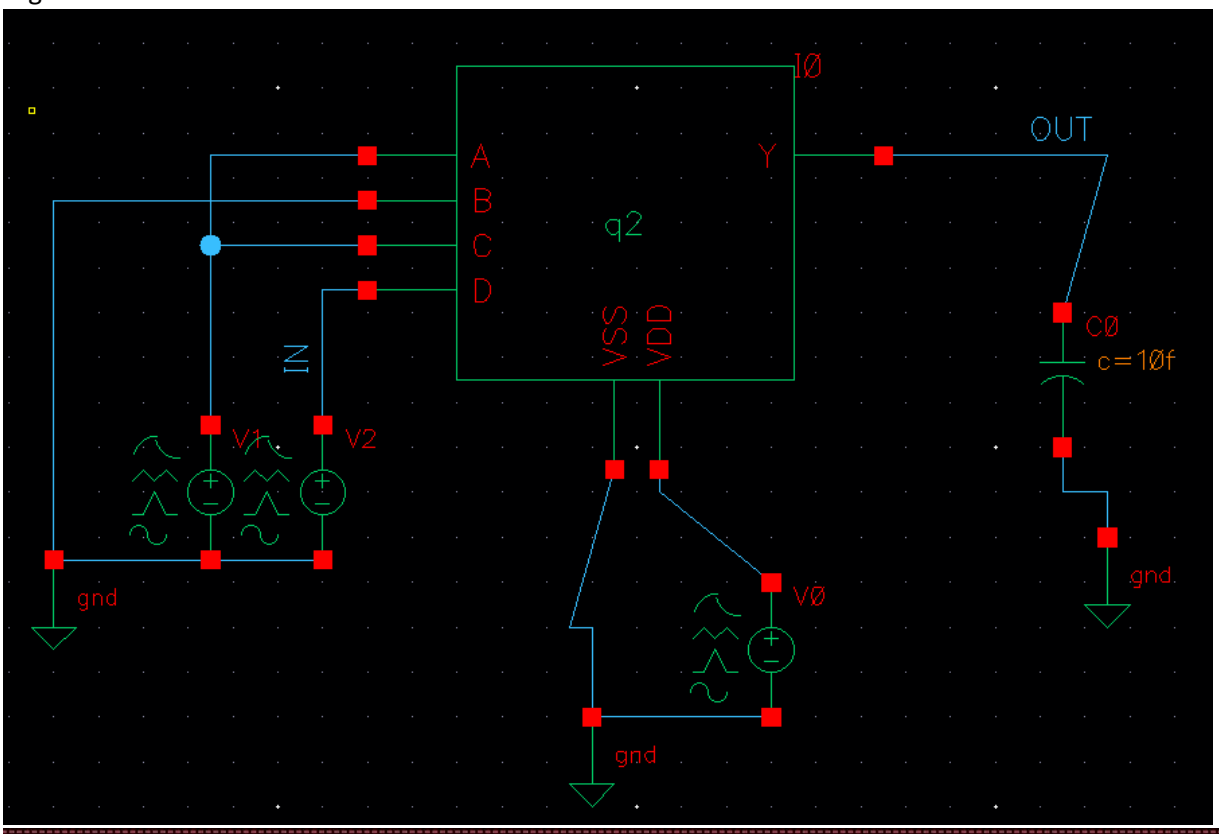
Outputs

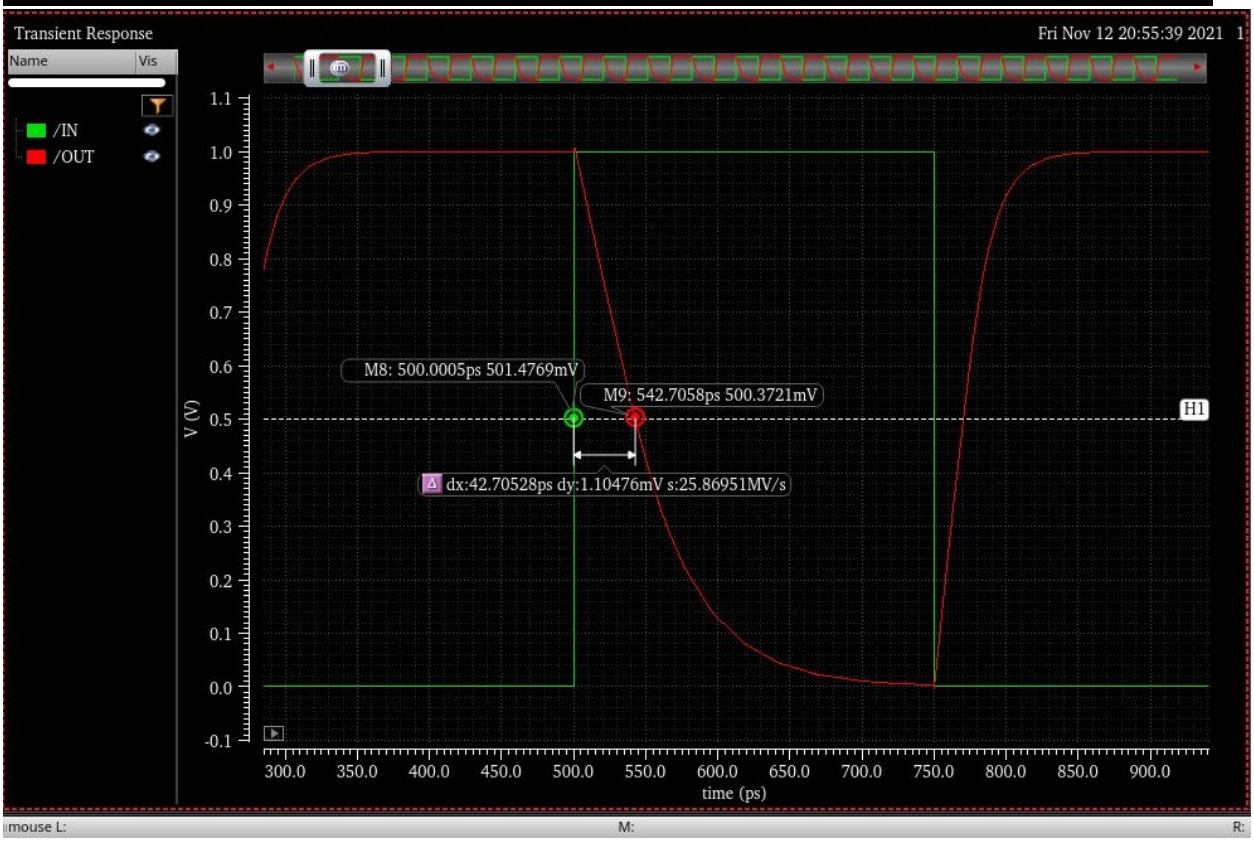
	Name/Signal/Expr	Value	Plot	Save	Save Op
1	IN		☑	☐	allv
2	OUT		☑	☐	allv

VDD = V1 = V0 = 1V DC

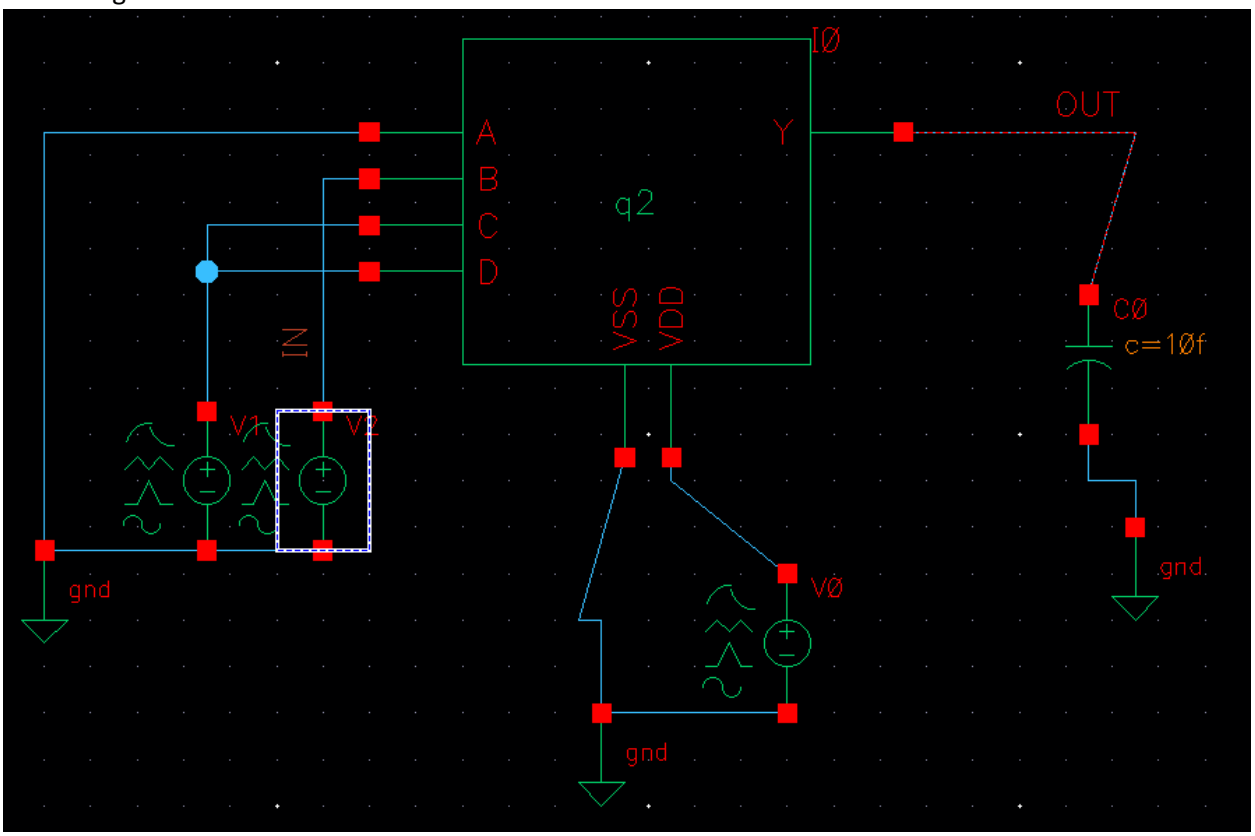
Output cap = 10fF

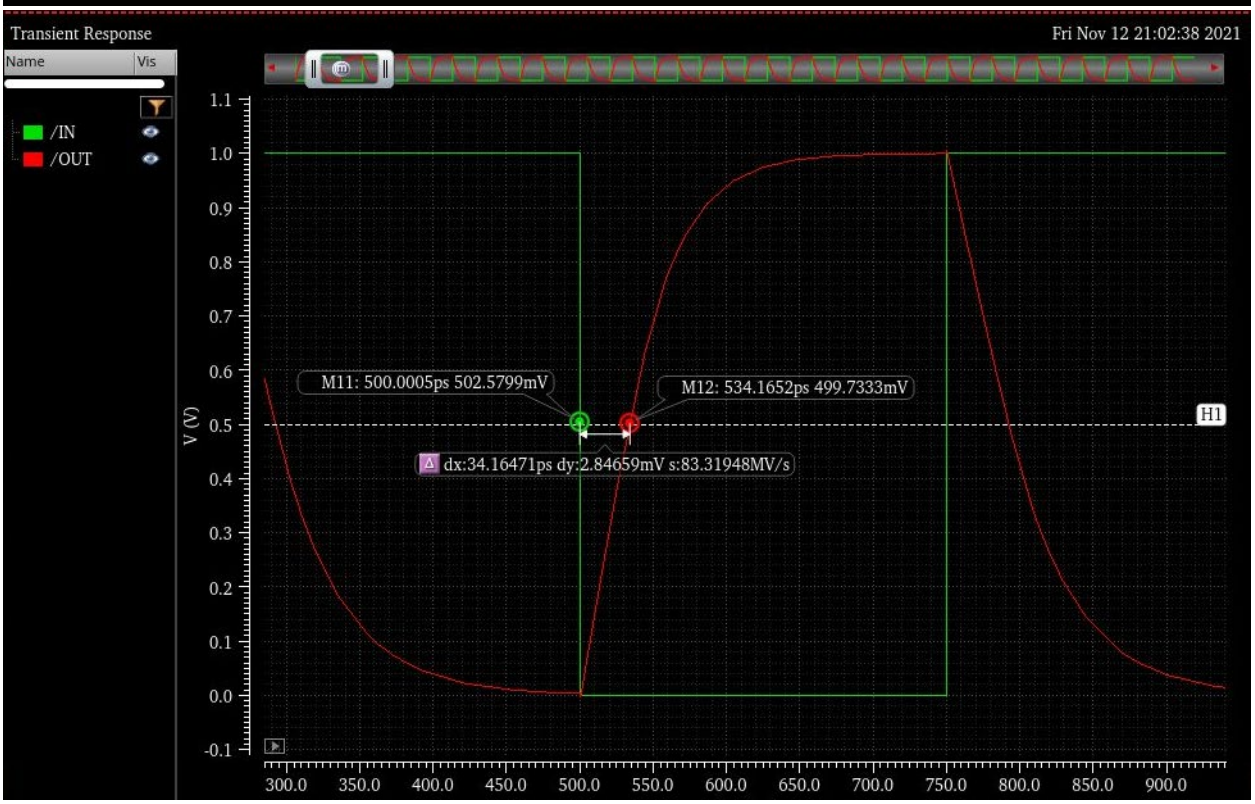
High to low: ABCD = 1010 -> 1011:





Low to high: ABCD = 0111 -> 0011:





T_{pHL}	T_{pLH}
42.7ps	**34.2ps**

Schematic Netlist is in Appendix B.

3. Transmission Gates

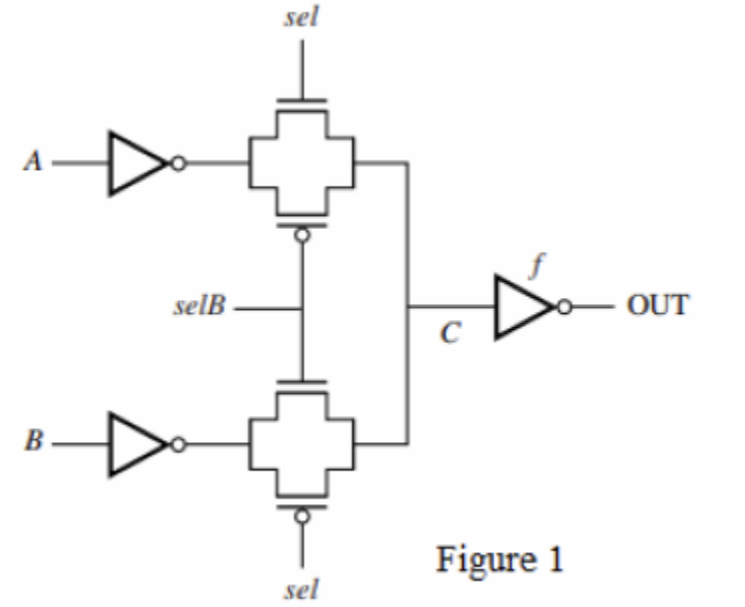
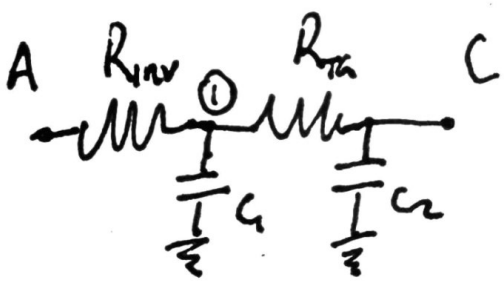


Figure 1

a. Expression for output function in terms of A, B, sel, selB. OUT is C'. A' is controlled by sel, B' is controlled by selB. C is A' and sel or B' and selB, so: OUT = (Asel') + (BselB')
b. Equivalent RC circuit model from A to C, given sel is high. A passes through an inverter, then a transmission gate:

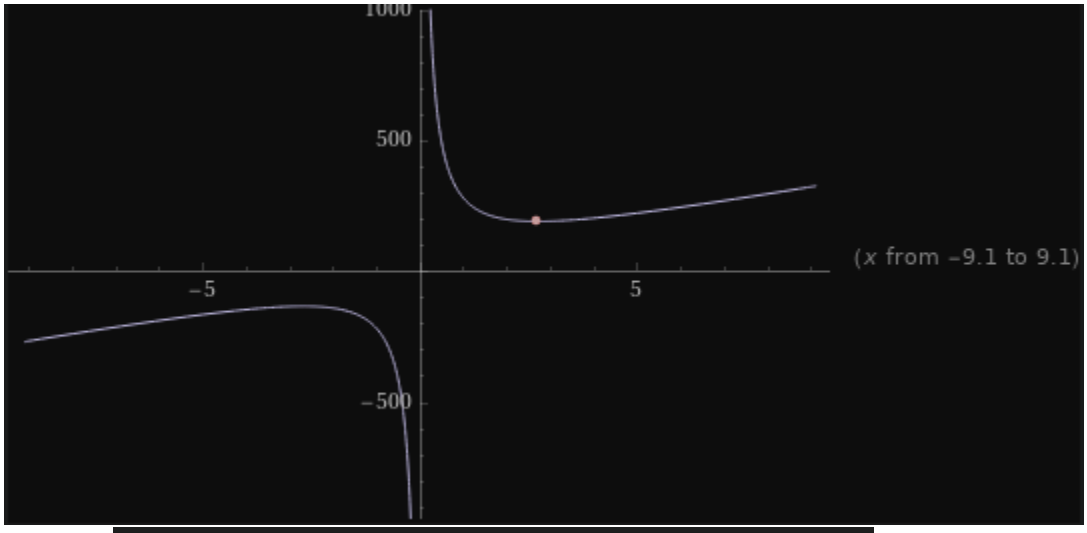


i.
ii. Resistances approximation: R_inv = R_TG = R_eqn (L/W), R_inv = R_TG = 12.5k (2/4) = 6.25k ohms
iii. C1 Capacitance (C_{eff} -> 1, C_g -> 2 from formula):
    1. $C_{inv} = C_{eff}(4 + 8) = 12C_{eff}$
    2. $C_{tg} = C_{eff} * 2 * (4) + C_g (4) = 8C_{eff} + 4C_g$
    3. $C1 = C_{inv} + C_{tg} = (20C_{eff} + 4C_g)\ 0.1 = 2.4$ fF
iv. C2 Capacitances (C_{eff} -> 1, C_g -> 2 from formula), x multiplier from load inverter **(I use x since I already use f for femto for clarity)**:
    1. $C_{inv} = C_g(4 + 8) = 12C_g * x$
    2. $C_{tg} = C_{eff} * 2 * (4) + C_g (4) = 8C_{eff} + 4C_g$
    3. $C2 = C_{inv} + C_{tg} = (8C_{eff} + 12fC_g)\ 0.1 = (2.4x + 1.6)$ fF

c. A to C delay. Since the resistances are the same, Elmore delay t_{elmore} = RC1 + 2RC2, where R is 6.25 k ohms and C1, C2 are above. This can simplify to t_{elmore} = 6.25k * 2.4f + 2*6.25k*(2.4x + 1.6)f = 15 + 30x + 10.4 ps = 25.4 + 30x ps

d. RC Delay, Load is 50fF, R becomes R/x, and C becomes (4 + 8) * x * Ceff + 50fF. Step (0.7) is used because it's RC delay, which is the most ideal case for the output inverter. So, t_{rc} = 0.7 *6.25k/x (50 + 1.2x)f = 4.375 (1.2x + 50) / x ps

e. Optimal output inverter size to minimize A to OUT: elmore + rc delay and minimize: 25.4 + 30x + 4.375 (1.2x + 50) / x



This is at $\min\left\{25.4 + 30x + \frac{4.375\,(1.2x + 50)}{x}\right\} \approx 192.669 \text{ at } x \approx 2.70031$

So optimal multiplier x (aka f) is 2.7.

Appendix A: DRC Summary

NAND3.drc.results | NAND3.drc.summary

```
================================================================================
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Sat Nov 13 00:37:30 2021
Calibre Version:           v2018.1_36.27    Tue Apr 3 12:54:13 PDT 2018
Rule File Pathname:        /ubc/ece/home/ugrads/m/mchuahua/Cadence_Pro.j4/_calibreDRC.rul
Rule File Title:
Layout System:             GDS
Layout Path(s):            NAND3.calibre.db
Layout Primary Cell:       NAND3
Current Directory:         /ubc/ece/home/ugrads/m/mchuahua/Cadence_Pro.j4
User Name:                 mchuahua
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      NAND3.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       NAND3.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER NW ..... TOTAL Original Geometry Count = 1  (3)
LAYER ACT .... TOTAL Original Geometry Count = 2  (6)
LAYER GATEA .. TOTAL Original Geometry Count = 5  (9)
LAYER GATEB .. TOTAL Original Geometry Count = 4  (12)
LAYER GATEAB . TOTAL Original Geometry Count = 0  (0)
LAYER NIM .... TOTAL Original Geometry Count = 1  (3)
LAYER PIM .... TOTAL Original Geometry Count = 1  (3)
LAYER AIL2 ... TOTAL Original Geometry Count = 1  (12)
LAYER AIL1 ... TOTAL Original Geometry Count = 4  (12)
LAYER GATEC .. TOTAL Original Geometry Count = 0  (0)
LAYER VTH .... TOTAL Original Geometry Count = 0  (0)
LAYER VTL .... TOTAL Original Geometry Count = 0  (0)
LAYER GIL .... TOTAL Original Geometry Count = 4  (6)
LAYER M1A .... TOTAL Original Geometry Count = 24 (37)
LAYER V0 ..... TOTAL Original Geometry Count = 2  (15)
LAYER M1B .... TOTAL Original Geometry Count = 0  (0)
LAYER M1 ..... TOTAL Original Geometry Count = 0  (0)
LAYER V1 ..... TOTAL Original Geometry Count = 0  (0)
LAYER MINT1A . TOTAL Original Geometry Count = 0  (0)
LAYER MINT1B . TOTAL Original Geometry Count = 0  (0)
LAYER MINT1 .. TOTAL Original Geometry Count = 0  (0)
LAYER VINT1 .. TOTAL Original Geometry Count = 0  (0)
LAYER MINT2A . TOTAL Original Geometry Count = 0  (0)
LAYER MINT2B . TOTAL Original Geometry Count = 0  (0)
LAYER MINT2 .. TOTAL Original Geometry Count = 0  (0)
LAYER VINT2 .. TOTAL Original Geometry Count = 0  (0)
LAYER MINT3A . TOTAL Original Geometry Count = 0  (0)
LAYER MINT3B . TOTAL Original Geometry Count = 0  (0)
LAYER MINT3 .. TOTAL Original Geometry Count = 0  (0)
LAYER VINT3 .. TOTAL Original Geometry Count = 0  (0)
LAYER MINT4A . TOTAL Original Geometry Count = 0  (0)
LAYER MINT4B . TOTAL Original Geometry Count = 0  (0)
LAYER MINT4 .. TOTAL Original Geometry Count = 0  (0)
LAYER VINT4 .. TOTAL Original Geometry Count = 0  (0)
LAYER MINT5A . TOTAL Original Geometry Count = 0  (0)
LAYER MINT5B . TOTAL Original Geometry Count = 0  (0)
LAYER MINT5 .. TOTAL Original Geometry Count = 0  (0)
LAYER VINT5 .. TOTAL Original Geometry Count = 0  (0)
LAYER MSMG1 .. TOTAL Original Geometry Count = 0  (0)
LAYER VSMG1 .. TOTAL Original Geometry Count = 0  (0)
LAYER MSMG2 .. TOTAL Original Geometry Count = 0  (0)
LAYER VSMG2 .. TOTAL Original Geometry Count = 0  (0)
LAYER MSMG3 .. TOTAL Original Geometry Count = 0  (0)
LAYER VSMG3 .. TOTAL Original Geometry Count = 0  (0)
LAYER MSMG4 .. TOTAL Original Geometry Count = 0  (0)
LAYER VSMG4 .. TOTAL Original Geometry Count = 0  (0)
LAYER MSMG5 .. TOTAL Original Geometry Count = 0  (0)
LAYER VSMG5 .. TOTAL Original Geometry Count = 0  (0)
LAYER MG1 .... TOTAL Original Geometry Count = 0  (0)
LAYER VG1 .... TOTAL Original Geometry Count = 0  (0)
LAYER MG2 .... TOTAL Original Geometry Count = 0  (0)
LAYER HCONT .. TOTAL Original Geometry Count = 0  (0)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS
---
RULECHECK RULE_NW001 ........ TOTAL Result Count = 0 (0)
RULECHECK RULE_NW002 ........ TOTAL Result Count = 0 (0)
RULECHECK RULE_NW003 ........ TOTAL Result Count = 0 (0)
RULECHECK RULE_NW004A ....... TOTAL Result Count = 1 (1)
RULECHECK RULE_NW004B ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_NW005 ........ TOTAL Result Count = 0 (0)
RULECHECK RULE_NW006A ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_NW006B ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_NW006AB ...... TOTAL Result Count = 0 (0)
RULECHECK RULE_ACT001 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_ACT002 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_ACT003 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_ACT004 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_ACT005 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_ACT006 ....... TOTAL Result Count = 0 (0)
```

...

```
RULECHECK RULE_MG2012 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_MG2013 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_MG2014 ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_MIS01 ........ TOTAL Result Count = 0 (0)
RULECHECK RULE_MIS02A ....... TOTAL Result Count = 0 (0)
RULECHECK RULE_MIS02B ....... TOTAL Result Count = 0 (0)
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
CELL pmos_pcell_CDNS_636792648641 ... TOTAL Result Count = 1 (3)
    RULECHECK RULE_ACT009 ........... TOTAL Result Count = 1 (3)
CELL nmos_pcell_CDNS_636792648640 ... TOTAL Result Count = 1 (3)
    RULECHECK RULE_ACT009 ........... TOTAL Result Count = 1 (3)
CELL NAND3 ..................... TOTAL Result Count = 1 (1)
    RULECHECK RULE_NW004A ........... TOTAL Result Count = 1 (1)
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 3
TOTAL Original Layer Geometries: 49 (118)
TOTAL DRC RuleChecks Executed:   698
TOTAL DRC Results Generated:     3 (7)
```

ACT009 and NW004A as mentioned can be ignored.

Appendix B: Schematic Netlist of Q2

```
// Generated for: spectre
// Generated on: Nov 13 01:40:18 2021
// Design library name: ELEC402
// Design cell name: q2_tb
// Design view name: schematic
simulator lang=spectre
global 0
include "/CMC/kits/ncsu_pdk/FreePDK15/hspice/models/fet.inc" section=CMG

// Library name: ELEC402
// Cell name: q2
// View name: schematic
subckt q2 A B C D VDD VSS Y
    M3 (Y A net4 VDD) pfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M2 (net4 B VDD VDD) pfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M1 (Y C VDD VDD) pfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M0 (Y D VDD VDD) pfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M7 (net3 D VSS VSS) nfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M6 (net2 C net3 VSS) nfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M5 (Y A net2 VSS) nfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
    M4 (Y B net2 VSS) nfet as=6.08e-16 ad=6.08e-16 ps=168n pd=168n m=2 \
        degradation=no
ends q2
// End of subcircuit definition.

// Library name: ELEC402
// Cell name: q2_tb
// View name: schematic
I0 (0 IN net3 net3 net2 0 OUT) q2
C0 (OUT 0) capacitor c=10f
V1 (net3 0) vsource dc=1 type=dc
V0 (net2 0) vsource dc=1 type=dc
V2 (IN 0) vsource dc=0 type=pulse delay=0 val0=1 val1=0 period=500.0p \
        rise=10p fall=10p
simulatorOptions options psfversion="1.1.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=10n errpreset=moderate write="spectre.ic" \
    writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

Appendix C: LVS Report Q1

```
        ##################################################
        ##                                              ##
        ##      C A L I B R E   S Y S T E M             ##
        ##                                              ##
        ##        L V S   R E P O R T                   ##
        ##                                              ##
        ##################################################


REPORT FILE NAME:       NAND3.lvs.report
LAYOUT NAME:            /ubc/ece/home/ugrads/m/mchuahua/Cadence_Proj4/svdb/NAND3.sp ('NAND3')
SOURCE NAME:            /ubc/ece/home/ugrads/m/mchuahua/Cadence_Proj4/NAND3.src.net ('NAND3')
RULE FILE:              /ubc/ece/home/ugrads/m/mchuahua/Cadence_Proj4/_calibrePEX.rul_
CREATION TIME:          Sat Nov 13 04:25:06 2021
CURRENT DIRECTORY:      /ubc/ece/home/ugrads/m/mchuahua/Cadence_Proj4
USER NAME:              mchuahua
CALIBRE VERSION:        v2018.1_36.27    Tue Apr 3 12:54:13 PDT 2018


                    OVERALL COMPARISON RESULTS


               #    ###################     _  _
              #     #           #     *  *
             # #    #    CORRECT   #      |
             # #    #           #     \___/
              #     ###################


********************************************************************************************************
                          CELL  SUMMARY
********************************************************************************************************

 Result      Layout                  Source
 ----------  ----------              --------------
 CORRECT     NAND3                   NAND3


********************************************************************************************************
                          LVS PARAMETERS
********************************************************************************************************


o LVS Setup:

  LVS COMPONENT TYPE PROPERTY          element
  LVS COMPONENT SUBTYPE PROPERTY       model
  // LVS PIN NAME PROPERTY
  LVS POWER NAME                    "VDD"
  LVS GROUND NAME                   "VSS"
  LVS CELL SUPPLY                   NO
  LVS RECOGNIZE GATES               ALL
  LVS IGNORE PORTS                  NO
  LVS CHECK PORT NAMES              NO
  LVS IGNORE TRIVIAL NAMED PORTS    NO
  LVS BUILTIN DEVICE PIN SWAP       YES
  LVS ALL CAPACITOR PINS SWAPPABLE  NO
  LVS DISCARD PINS BY DEVICE        NO
  LVS SOFT SUBSTRATE PINS           NO
  LVS INJECT LOGIC                  NO
  LVS EXPAND UNBALANCED CELLS       YES
  LVS FLATTEN INSIDE CELL           NO
  LVS EXPAND SEED PROMOTIONS        NO
  LVS PRESERVE PARAMETERIZED CELLS  NO
  LVS GLOBALS ARE PORTS             YES
  LVS REVERSE WL                    NO
  LVS SPICE PREFER PINS             NO
  LVS SPICE SLASH IS SPACE          YES
  LVS SPICE ALLOW FLOATING PINS     YES
  // LVS SPICE ALLOW INLINE PARAMETERS
  LVS SPICE ALLOW UNQUOTED STRINGS  NO
  LVS SPICE CONDITIONAL LDD         NO
  LVS SPICE CULL PRIMITIVE SUBCIRCUITS  NO
  // LVS SPICE EXCLUDE CELL SOURCE
  // LVS SPICE EXCLUDE CELL LAYOUT
  LVS SPICE IMPLIED MOS AREA        NO
  // LVS SPICE MULTIPLIER NAME
  LVS SPICE OVERRIDE GLOBALS        NO
  LVS SPICE REDEFINE PARAM          NO
  LVS SPICE REPLICATE DEVICES       NO
  LVS SPICE SCALE X PARAMETERS      NO
  LVS SPICE STRICT WL               NO
  // LVS SPICE OPTION
  LVS STRICT SUBTYPES               NO
  LVS EXACT SUBTYPES                NO
  LAYOUT CASE                    NO
  SOURCE CASE                    NO
  LVS COMPARE CASE                  NO
  LVS DOWNCASE DEVICE               NO
  LVS REPORT MAXIMUM                50
  LVS PROPERTY RESOLUTION MAXIMUM   32
  // LVS SIGNATURE MAXIMUM
  // LVS FILTER UNUSED OPTION
  // LVS REPORT OPTION
  LVS REPORT UNITS                  YES
  // LVS NON USER NAME PORT
  // LVS NON USER NAME NET
  // LVS NON USER NAME INSTANCE
  // LVS IGNORE DEVICE PIN
  // LVS PREFER NETS FILTER SOURCE
  // LVS PREFER NETS FILTER LAYOUT

  // Reduction

  LVS REDUCE SERIES MOS             YES
  LVS REDUCE PARALLEL MOS           YES
  LVS REDUCE SEMI SERIES MOS        YES
```

```
  LVS REDUCE SPLIT GATES              YES
  LVS REDUCE PARALLEL BIPOLAR         YES
  LVS REDUCE SERIES CAPACITORS        YES
  LVS REDUCE PARALLEL CAPACITORS      YES
  LVS REDUCE SERIES RESISTORS         YES
  LVS REDUCE PARALLEL RESISTORS       YES
  LVS REDUCE PARALLEL DIODES          YES
  LVS REDUCTION PRIORITY              PARALLEL

  LVS SHORT EQUIVALENT NODES          NO


            CELL COMPARISON RESULTS ( TOP LEVEL )


                #     ###################     _  _
               #      #           #     *  *
              #  #     #    CORRECT    #       |
              # #      #           #     \___/
               #       ###################


LAYOUT CELL NAME:       NAND3
SOURCE CELL NAME:       NAND3

--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

           Layout   Source       Component Type
           ------   ------       --------------
 Ports:         6        6

 Nets:         10       10

 Instances:     3        3       MN (4 pins)
                3        3       MP (4 pins)
           ------   ------
 Total Inst:    6        6


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

           Layout   Source       Component Type
           ------   ------       --------------
 Ports:         6        6

 Nets:          8        8

 Instances:     1        1       NAND3 (4 pins): output input input input
           ------   ------
 Total Inst:    1        1


*************************************************************************************************************
                        INFORMATION AND WARNINGS
*************************************************************************************************************


            Matched   Matched   Unmatched   Unmatched   Component
             Layout    Source    Layout      Source     Type
            -------   -------   ---------   ---------  ---------
  Ports:          6         6          0           0

  Nets:           8         8          0           0

  Instances:      1         1          0           0    NAND3
            -------   -------   ---------   ---------
  Total Inst:     1         1          0           0


o Initial Correspondence Points:

  Ports:      VDD VSS A B C OUT


*************************************************************************************************************
                            SUMMARY
*************************************************************************************************************

Total CPU Time:     16 sec
Total Elapsed Time:  20 sec
```