ELEC 402

Noise Margin In Digital Circuits
Lecture 6

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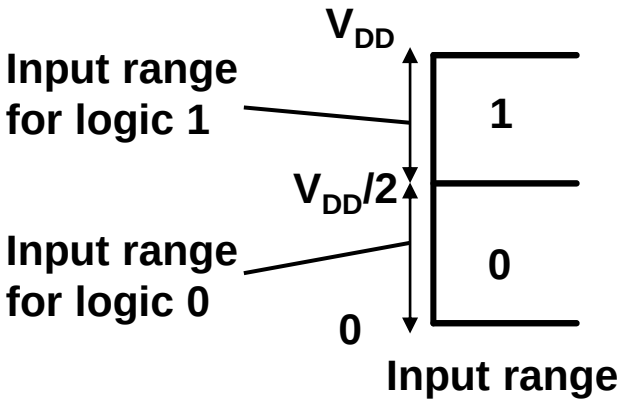
Overview

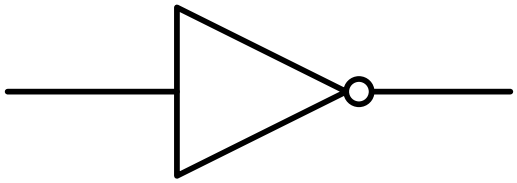
- Background
  - Digital IC designs must operate properly in noisy environments. We would like to have some notion of how robust a circuit is to external noise sources. The classical noise margins are defined based on the unity gain points of the VTC. These metrics eventually lead us to desirable properties that logic gates must have in order to work properly. We will look at how to calculate this for inverters in this lecture.

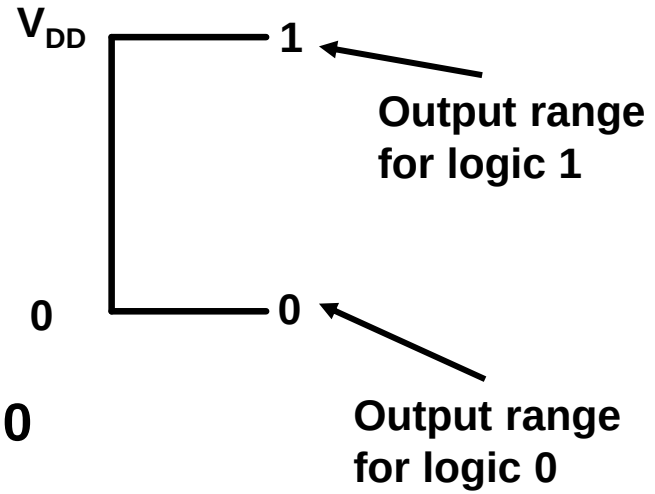
Noise Margin and Sensitivity

- Robustness of a circuit (i.e., its ability to operate properly in the presence of noise) depends on two factors:
    1. Noise margins (voltage metric)
        - how much noise can we apply before the gate fails
        - many different ways to measure this
    2. Noise sensitivity
        - how much noise can actually couple into the gate
        - depends on gate type and its connection to noise source
- Start by examining the first issue using basic inverter circuit…

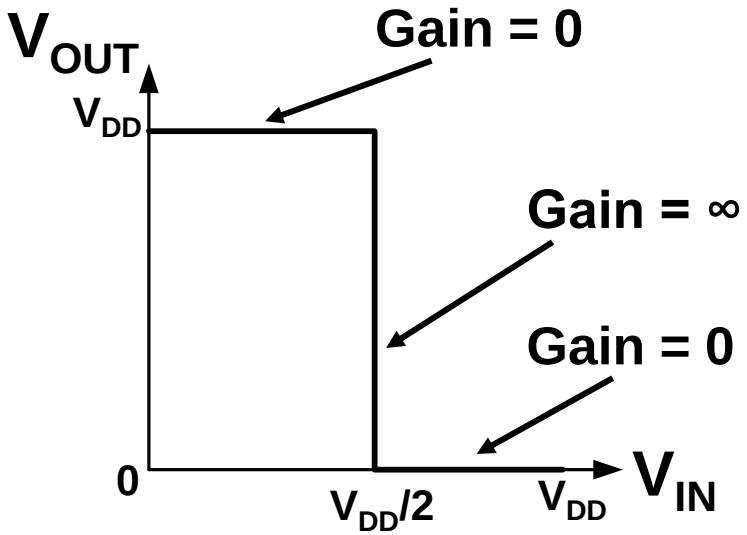
Ideal Inverter Characteristics (VTC)



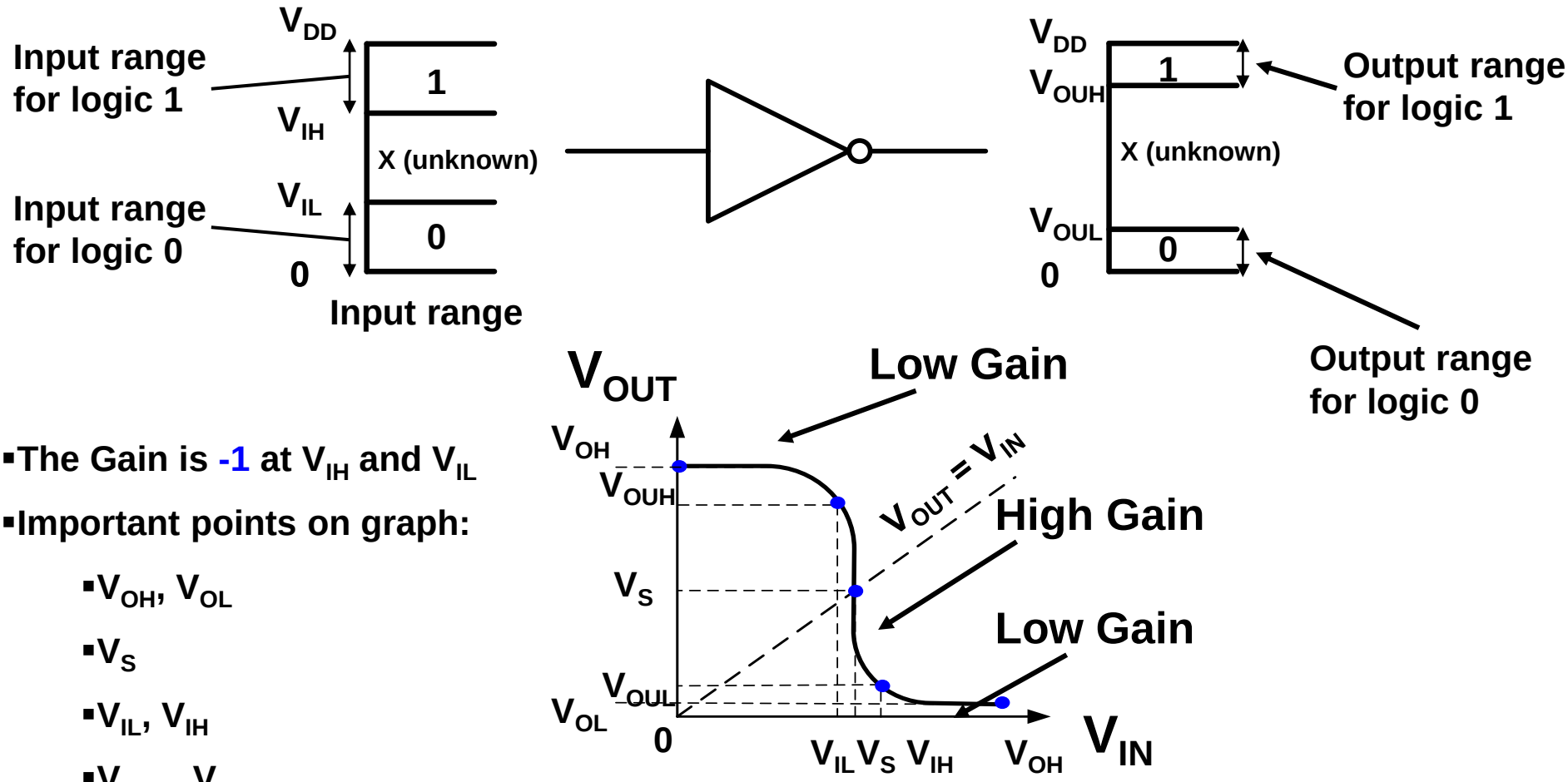




$$\text{Gain} = \frac{\partial Vout}{\partial Vin}$$



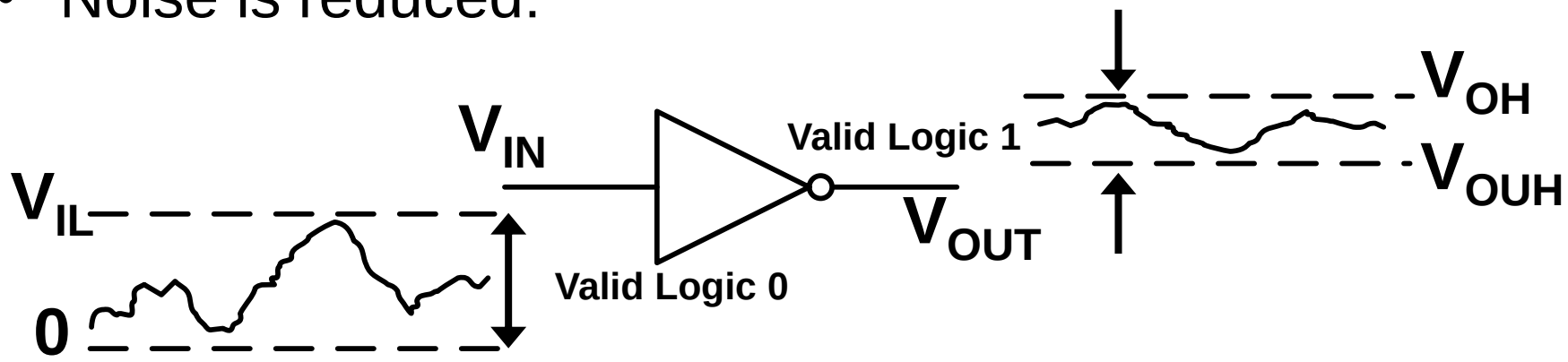
Physical Inverter Characteristics (VTC)



- The Gain is -1 at V_{IH} and V_{IL}
- Important points on graph:
  - V_{OH}, V_{OL}
  - V_S
  - V_{IL}, V_{IH}
  - V_{OUH}, V_{OUL}

Noise Attenuation

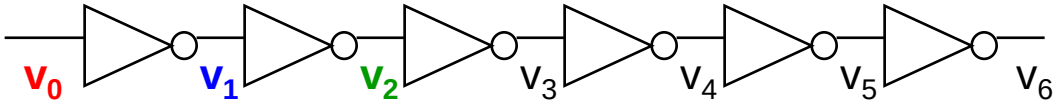
- What does this type of VTC imply about a noisy signal as it passes through a logic gate?
- Noise is reduced:

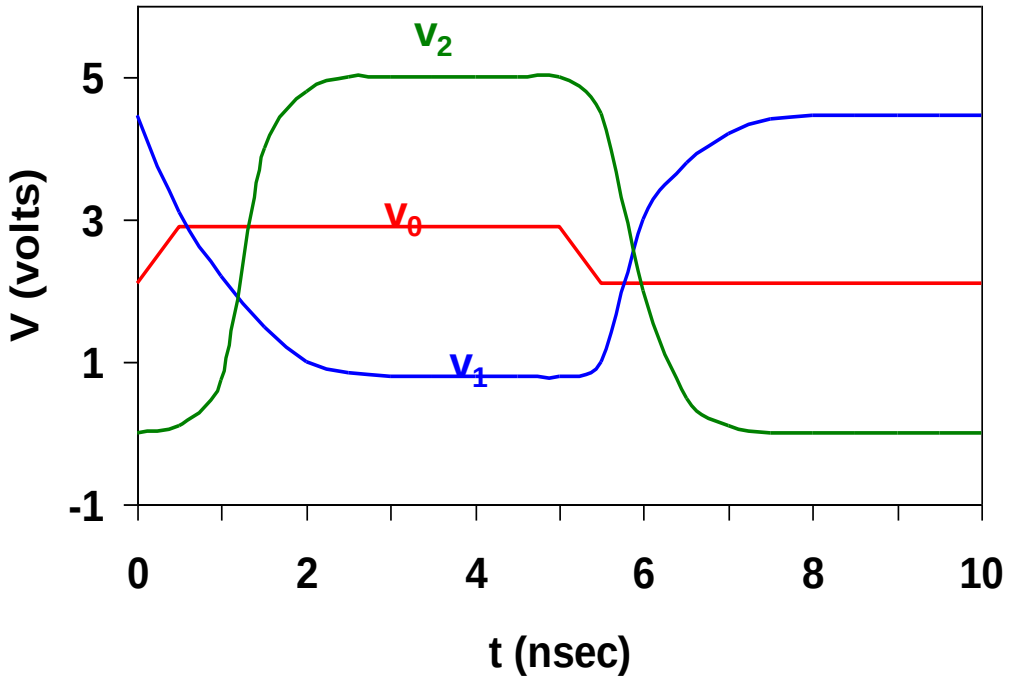


- Next, consider metrics for noise tolerance and the implications on the characteristics of the gate

The Regenerative Property

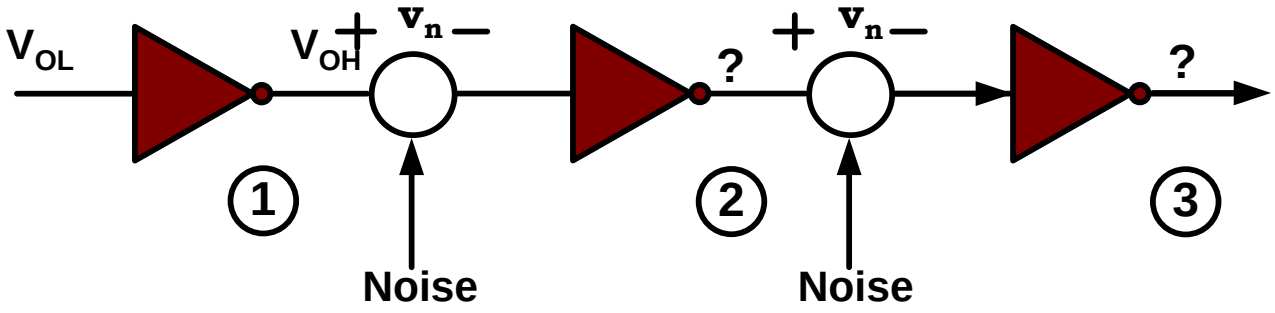
- A gate with regenerative property ensure that a disturbed signal converges back to a nominal voltage level





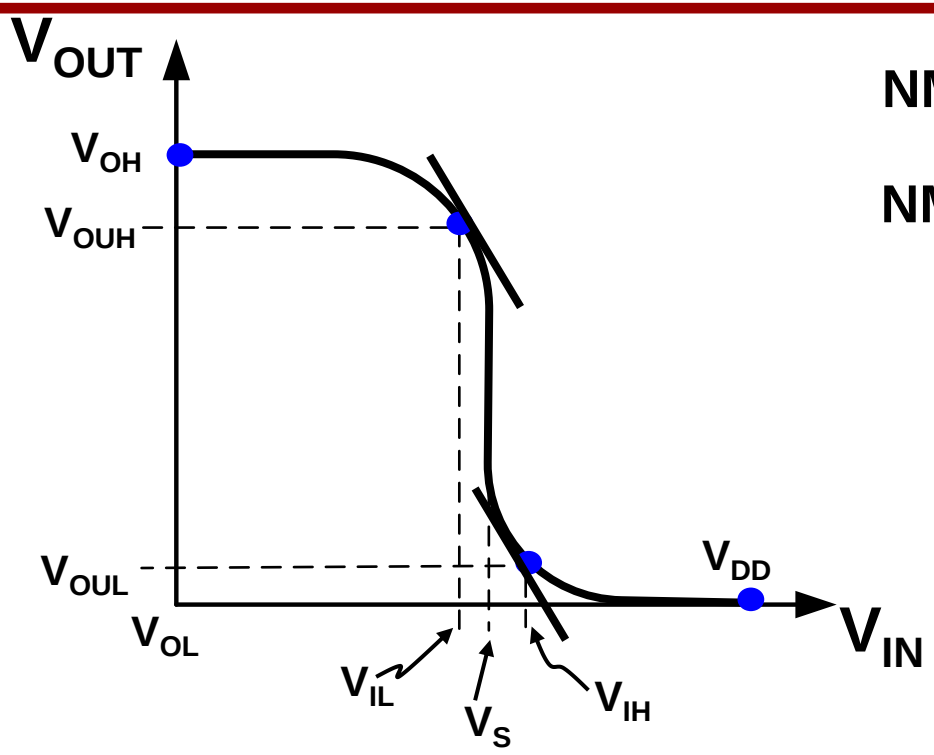
Multi Stage Noise Margin (MSNM)

- Noise actually occurs between every gate and not at a single stage, as we have assumed so far



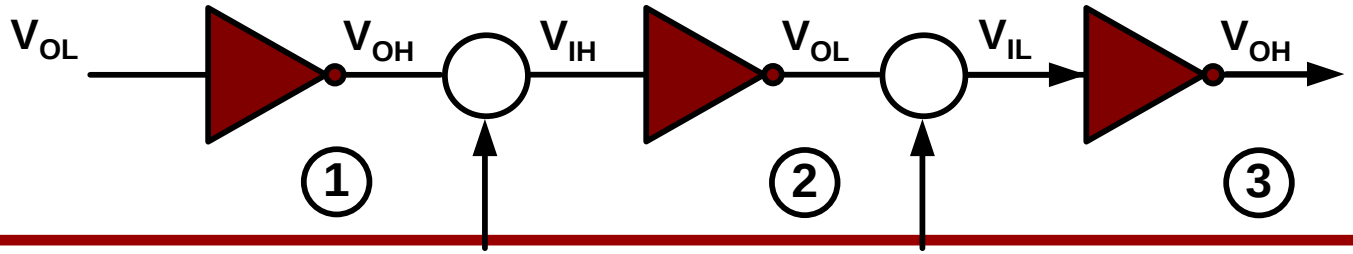
- In the above circuit, we need to determine how much noise we can tolerate before the circuit stops working as expected
- We note that Vout = f(Vin)
- With noise Vout' = f(Vin) + Vnoise x Gain + Higher-order terms
- If the Gain < 1, then noise is attenuated; otherwise it is amplified
- IDEA: Develop a metric based on keeping the Gain < 1

Classical Noise Margin



$NM_L = V_{IL} - V_{OL}$

$NM_H = V_{OH} - V_{IH}$

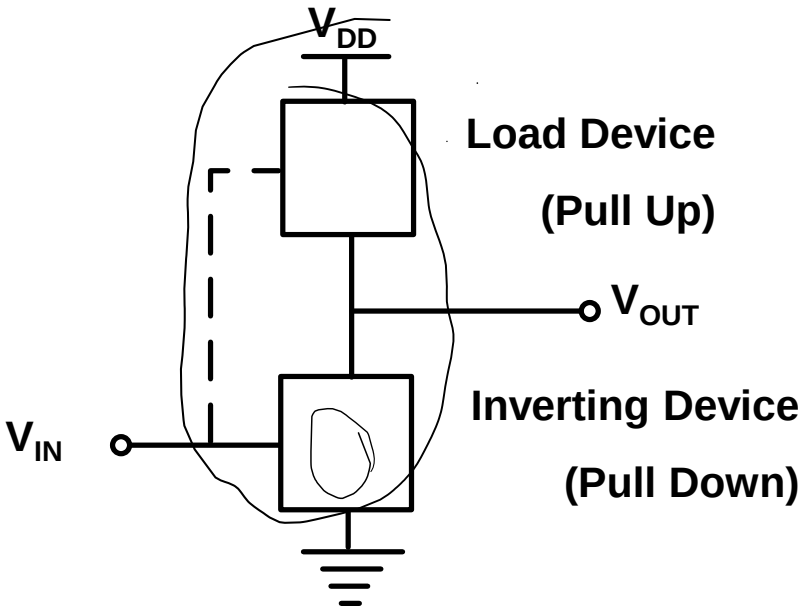


Requirements for a Valid Logic Gate

- Must have a high gain region between two low gain regions
- Gain must be below 1 for low gain regions
- Gain must be greater than 1 for high gain region
- Output must swing from valid low to valid high
  - Low output should be below V_{IL}
  - High output should be above V_{IH}

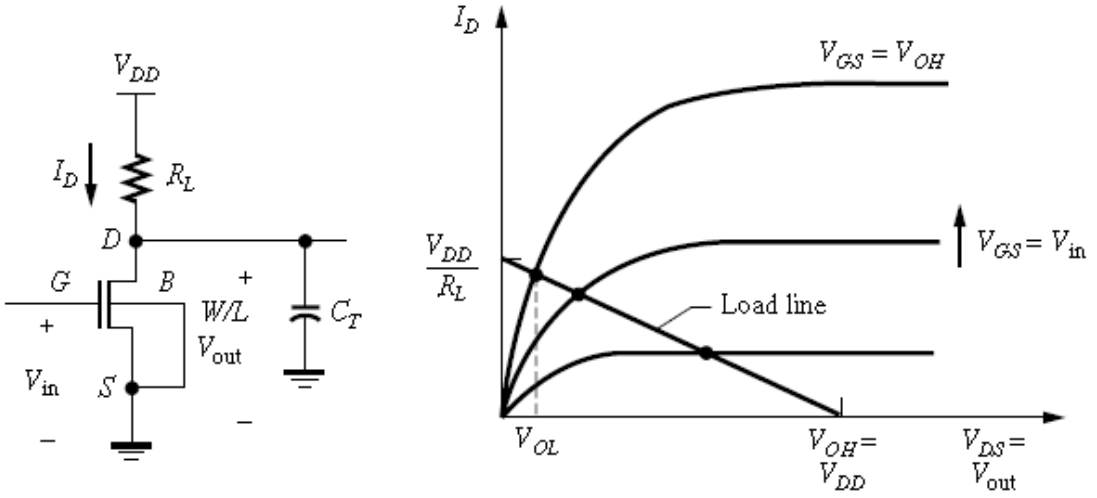
Next …

- Basic structure of MOS inverter is shown below: NMOS pulldown device with a variety of possible pullup devices



- We will derive the noise margin parameters for different types of inverters

Resistive-Load Inverter Design
“5 Point Technique”



How to plot VTC from load line representation?

1) Find the two extremes of output voltage, e.g. V_{OH} and V_{OL} (be careful with the MOS region of operation for each derivation)
2) Express the V_{out}-V_{in} relationship (usually the current equations of the devices provides that) and find points where $\delta V_{out}/\delta V_{in} = -1$ (V_{IH} and V_{IL})
3) Find the switching point where $V_{in}=V_{out}=V_S$
4) Plot VTC using the values of five points and calculate NM as V_{OH}-V_{IH} and V_{IL}-V_{OL}

Resistive-Load Inverter Design – cont'd

Let's apply the technique to resistive-load inverter design

1) The extremes

Remember that in inverters an input value of V_{OH} (it is the output of previous stage) creates an output of V_{OL} and vice versa, hence we first find the easier of the two, i.e. the more straightforward one, and then replace it in expression of $I_{OUT}=I_{load}$ to find the other one

- At one extreme the transistor is off hence no current, $V_{OH}=V_{DD}$

- At the other extreme we use $V_{in}=V_{OH}=V_{DD}$ in the expression of $I_{OUT}=I_{load}$ to find the V_{OL}

$$I_R = I_{DS}\,(\text{lin})$$

Substituting in the expressions for the resistor current and NMOS current:

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{W_N}{L_N}\frac{\mu_n C_{ox}}{2\left(1 + \dfrac{V_{OL}}{E_C L}\right)}\left[2\left(V_{OH} - V_T\right)V_{OL} - V_{OL}^2\right]$$

We know VOL is very small so for your calculations we can ignore it (Engineering approximations are IMPORTANT!)

Resistive-Load Inverter Design – cont'd

$$\text{setting } k = (W/L)\,\mu_n C_{ox}:$$

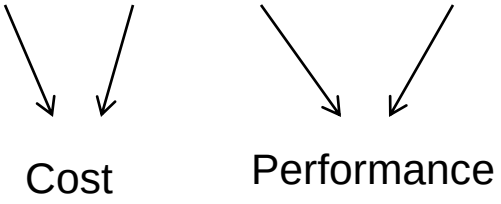
$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k}{2}[2(V_{OH} - V_T)V_{OL} - V_{OL}^2]$$

Knowing that $V_{OH}=V_{DD}$ and neglecting V^2_{OL}

$$V_{OL} \approx \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)}$$

Q: What should V_{OL} ideally be? What are the engineering trade-offs to make it happen?

Note that we always trade-off power, area, timing and noise margin versus one another



Resistive-Load Inverter Design – cont'd

2. Now, let's derive V_{IL}

Note that these values are now input voltages corresponding to $\delta V_{out}/\delta V_{in} = -1$

Step 1: detect the region of MOS operation

For V_{IL} the input is still considered low and output voltage is near V_{DD} (large V_{DS})

$$I_R = I_{DS}\,(\text{sat})$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{W v_{sat} C_{ox}(V_{in} - V_T)^2}{(V_{in} - V_T) + E_C L}$$

Use engineering intuition again: $V_{in} - V_T$ is small

$$\text{Recalling that } v_{sat} = \mu E_C/2 \qquad \text{Setting } k = (W/L)\mu_n C_{OX}$$

Now differentiate with respect to V_{in}, set $\delta V_{out}/\delta V_{in} = -1$, and $V_{in}=V_{IL}$

$$V_{IL} = V_T + \frac{1}{kR_L}$$

Resistive-Load Inverter Design – cont'd

Let's look at NM_L now:

$$V_{IL} = V_T + \frac{1}{kR_L} \qquad V_{OL} \approx \frac{V_{DD}}{1 + kR_L(V_{DD} - V_T)}$$

Q: Do you see the problem with noise margin optimization? (change k and R_L to get a higher NM_L)

Q: Which one would be a higher priority?

Board Discussion

Resistive-Load Inverter Design – cont'd

3. In order to complete the derivation and plot the VTC we only need V_S now (switching point)

Q: what is the MOS region of operation at switching point? Why?

$$I_R = I_{DS} \quad \text{and} \quad V_{\text{in}} = V_{\text{out}} = V_S$$

$$\frac{W v_{\text{sat}} C_{ox} (V_S - V_T)^2}{(V_S - V_T) + E_C L} = \frac{V_{DD} - V_S}{R_L}$$

Side discussion: How to solve higher-order equation?

- Deterministic equations
- Iteration technique
- SPICE

VTC plot