Assignment 3 Solutions

1. Resistive Load inverter:

$$\frac{V_{DD}-V_{OL}}{R_L}=\frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1+\frac{V_{OL}}{E_C L}\right)}\left[\ (V_{OH}-V_T)V_{OL}-\frac{V_{OL}^2}{2}\right]$$

$$\frac{1.2-0.1}{10K}=\frac{W_N}{0.1}\cdot\frac{270\times 1\times 10^{-6}}{1+\frac{0.1}{0.6}}[(1.2-0.4)\times 0.1-\frac{0.1^2}{2}]$$

$$W_N=0.32\mu m$$

b) Saturated Enhancement Load inverter (ignoring body-effect):

$$\frac{W_I}{L_I}\frac{\mu_N C_{ox}}{\left(1+\frac{V_{out}}{E_{CN}L_I}\right)}\left[(V_{in}-V_{TI})V_{out}-\frac{V_{out}^{\ 2}}{2}\right]=\frac{W_L v_{sat}C_{ox}(V_{DD}-V_{out}-V_{TL})^2}{(V_{DD}-V_{out}-V_{TL})+E_{CN}L_L}$$

$$\frac{W_I}{0.1}\cdot\frac{270\times 1\times 10^{-6}}{1+\frac{0.1}{0.6}}\cdot[(1.2-0.4)\times 0.1-\frac{0.1^2}{2}]=\frac{0.1\times 10^{-4}\times 8\times 1\times(1.2-0.1-0.4)^2}{(1.2-0.1-0.4)+0.6}$$

$$\therefore W_N=0.1\mu m$$

c) Inverter (ignoring body-effect):

$$\frac{W_I}{L_I}\frac{\mu_N C_{ox}}{\left(1+\frac{V_{out}}{E_{CN}L_I}\right)}\left[(V_{in}-V_{TI})V_{out}-\frac{V_{out}^{\ 2}}{2}\right]=\frac{W_L v_{sat}C_{ox}(V_{DD}-V_{out}-V_{TL})^2}{(V_{DD}-V_{out}-V_{TL})+E_{CN}L_L}$$

$$\frac{W_I}{0.1}\cdot\frac{270\times 1\times 10^{-6}}{1+\frac{0.1}{0.6}}\cdot[(1.2-0.4)\times 0.1-\frac{0.1^2}{2}]=\frac{0.1\times 10^{-4}\times 8\times 1\times(1.6-0.1-0.4)^2}{(1.6-0.1-0.4)+0.6}$$

$$\therefore W_N=0.6\mu m$$

The linear enhancement load inverter requires the largest pull-down device since it has the strongest pull up device. The resistive load inverter is next and the saturated enhancement load requires the smallest pull-down device.

For parts b and c, a more accurate calculation requires you to calculate Vth including body effect (by solving for V_{OH} first, textbook on Canvas 4.5.1) and use that to find W of transistors. In an exam setting it will be explicit to include/ignore body effects.

2. a) Circuit is a buffer with degraded outputs.

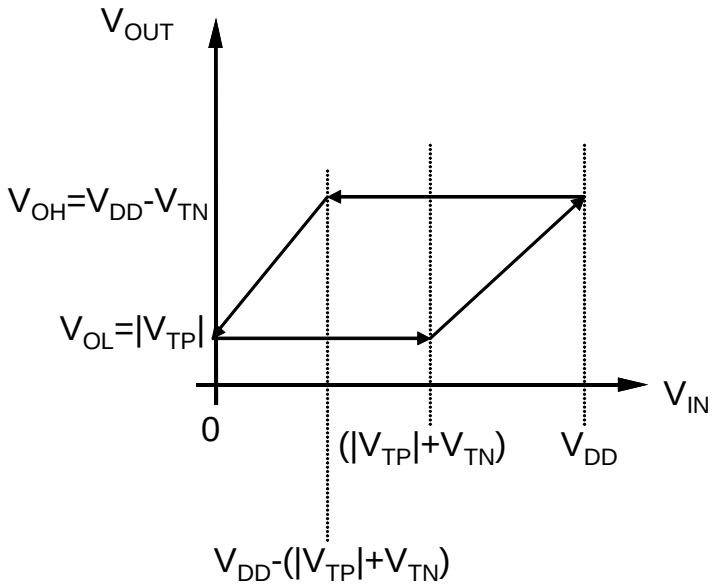
Output swing calculation:

When $V_{IN} = V_{DD}$, output voltage is $V_{OH} = V_{DD} - V_{TN}$. Since the source of NMOS transistor is not connected to substrate (ground), we must take into account body effect.

When $V_{IN} = 0V$, output voltage is $V_{OL} = |V_{TP}|$. Since the source of PMOS transistor is not connected to substrate (V_{DD}), we must take into account body effect.

Therefore the output swing is $V_{DD} - V_{TN}$ to $|V_{TP}|$ with full accounting for body effect.

b) Assume that the input is at 0 and the output is at $|V_{TP}|$. As the input is increased, the output will stay constant until the NMOS device turns on. That will occur at $V_{IN}=|V_{TP}|+V_{TN}$. The upper transistor behaves as a source follower and will pull the output along as the input rises until the output reaches $V_{DD}-V_{TN}$. However, as the input is reduced in value the output stays at its high value until the PMOS device turns on. This occurs at $V_{IN}=V_{DD}-(|V_{TP}|+V_{TN})$. Then the PMOS device acts as a source follower and the output drops linearly to $|V_{TP}|$ as the input is reduced.



c) The gain of the circuit is close to unity but slightly below this value. The circuit has poor noise rejection properties as it lacks the regenerative properties (this is a consequence of low gain).

d) SPICE Simulations

3) SPICE Simulations

4) (a) $C_g = C_{OX} \times L = \frac{\varepsilon_{OX}}{t_{OX}} \times L = \frac{4(8.845 \times 10^{-14} F/cm)}{40\,\overset{o}{A}} \times 0.18um \therefore C_g = 1.6fF/\mu m$

$C_{OL} = 0.2fF/\mu m \times W = 0.2fF/\mu m \times 0.9\mu = 0.18fF$

$\therefore C_G = 1.6fF/\mu m \times W = 1.44fF$

	cut-off	linear	saturation
C_{GS}	$C_{OL} = 0.18fF$	$C_{OL} + \frac{1}{2}C_G = 0.9fF$	$C_{OL} + \frac{2}{3}C_G = 1.14fF$
C_{GD}	$C_{OL} = 0.18fF$	$C_{OL} + \frac{1}{2}C_G = 0.9fF$	$C_{OL} = 0.18fF$
C_{GB}	$\frac{1}{2}C_G = 0.72fF$	0	0

(b) Built in junction potential is given as:

$$\phi_B = \frac{KT}{q} \times \ln \frac{N_A N_D}{n_i^2} = 0.94\text{V}$$

The zero-bias junction capacitance is given as:

$$C_{j0} = \sqrt{\frac{\varepsilon_{si} q N_A N_D}{2\phi_B (N_A + N_D)}} = 0.525fF/\mu m^2$$

$$C_j == 0.525fF/\mu m^2 \times (Y + x_j) = 0.525(0.8 + 0.3) = 0.58fF/um$$

(c)

$$C_J = \frac{C_{j0}(A_b + A_{sw})}{\left(1 - \frac{V_J}{\phi_B}\right)^m} = \frac{C_j W}{\left(1 - \frac{V_J}{\phi_B}\right)^m}$$

(i)

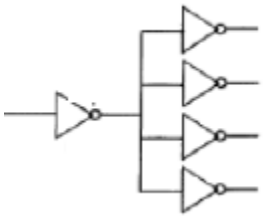
$$V_{BD} = -1.8V \Rightarrow C_D = \frac{(0.58)(0.9)}{\left(1+\frac{1.8}{.9}\right)^{\frac{1}{2}}} = 0.3\,fF$$

(ii)

$$V_{BD} = 0 \Rightarrow C_D = \frac{(0.57)(0.9)}{(1-0)^{\frac{1}{2}}} = 0.52\,fF$$

5.

a)



NMOS is 4λ : 2λ = 100 nm : 50 nm (rounded for simplicity) and PMOS is 8λ : 2λ = 200 nm : 50 nm

For resistance since this is short-channel device, it is more appropriate to use $R = R_{unit} / W$ where R_{unit} is the unit resistance of either NMOS or PMOS depending on whether you want tPHL or tPLH (slide 5 lecture 8) if not specified the actual delay is the average of the two tdelay = (tPHL+tPLH) / 2. R_{n_unit} = 1.7 kΩ.µm and R_{p_unit} = = 3.4 kΩ.µm

$R_{PD} = R_{n\_unit} / W$ = 1.7 kΩ.µm / 0.1 µm = 17 kΩ and $R_{PU} = R_{p\_unit} / W$ = 3.4 kΩ.µm / 0.2 µm = 17 kΩ

(if you use $R_{PD} = R_{\square} * L / W$ = 12.5 kΩ * 2λ / 4λ = 6.25 kΩ and $R_{PU} = R_{\square} * L / W$ = 30 kΩ * 2λ / 8λ = 7.5 kΩ it is also ok)

For $C_{out} = C_{self} + C_{load} = C_{eff}$ * sum of W's + C_g * sum of W's

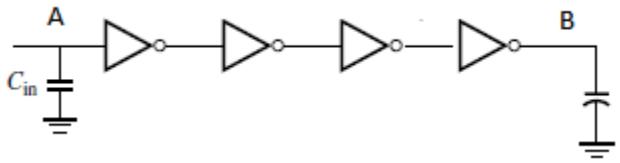
(As discussed in yesterday's lecture and today's tutorial if intermediate nodes need to also get charged (discharged), their W's should be included in C_{self} calculations)

(C_{eff} = 1 fF / µm and C_g = 2 fF / um are typical for both NMOS and PMOS devices)

C_{self} = 1 fF / µm * (0.1 µm + 0.2 µm) = 0.3 fF ,C_{load} = 4 * 2 fF / µm * (0.1 µm + 0.2 µm) = 2.4 fF

tPHL = tPLH = 0.7 * 17 kΩ * 2.7 fF = 28.5 pS

b) This time we would like to calculate the delay from A to B in the following schematic



R calculations are similar (since PD and PU paths are identical). However, each inverter sees only one inverter at its output rather than 4. Therefore:

C_{self} = 1 fF / µm * (0.1 µm + 0.2 µm) = 0.3 fF ,C_{load} = 2 fF / µm * (0.1 µm + 0.2 µm) = 0.6 fF

tPHL = tPLH = 0.7 * 17 kΩ * 0.9 fF = 9.5 pS (delay of each inverter)

Now, we have 4-inverers cascaded, so the delay to the output of 4^{th} inverter is the sum of delays, i.e.

Total delay = 4 * 9.5 pS = 38 pS

Exercise: draw the time domain waveform of voltage at the output of each inverter on the same plot, and notice the polarity change for odd or even number of inverters in chain