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| ELEC 402 – October 24, 2021 |
| Project 3 Report |
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Diagram, schematic

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1. **Resistive load inverter**

At one extreme, V­in is high, transistor is off and no current flows because MOS is in cut-off region, VOH = VDD. At the other extreme, Vin = VOH = VDD substituted into IOUT = Iload g IR = I­DS(lin), and the transistor operates in linear region. Using the useful formula for linear current:

Now we can also just straight up plug-in everything (taken from question):

* Vin = VGS = VOH = VDD = 1.2 V
* VDS = Vout = VOL = 0.1 V
* L = 0.1 µm
* RL = 10 kΩ
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Equating for W and throwing into wolfram:

1. **Saturated-enhancement-load inverter**

With this layout, we know the top pull-up transistor is the load and bottom pull-down transistor is the inverter. We know the load is always in saturation and the inverter should be linear because we want Vout = VOL = 0.1 V. Using the useful formulas for linear (left) and saturated (right) current, we can equate the two and get:

Using the following substitutions (inverter):

* Vin = VGS = VOH = VDD = 1.2 V
* VDS = Vout = VOL = 0.1 V
* L = 0.1 µm
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Using the following substitutions (load):

* Vin = VOH = VDD = 1.2 V
* VGS = 1.2 – 0.1 = 1.1 V
* vsat = 8E6 cm/s
* Wload = 0.1 µm
* L = 0.1 µm
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Note that although the left side units cancel out nicely due to the cm2/cm2, we need to convert the right-side units from cm (1E-2) to µm (1E-6) after the Coxvsat cancellation as there is still a cm unit left, done by multiplying the right side with 1E-4.

Equating for Winverter and throwing into wolfram:

1. **Linear-Enhancement-Load inverter**

To overcome low VOH, in the saturated-enhancement-load inverter, instead of VDD for both gate and drain of the load transistor, it is separated with VGG = 1.6 V and VDD = 1.2 V. Its linear region of operation is then VGG > VDD + VTL(VDD). Again, we equate currents but this time, the right side is not in saturation, but linear operation as well:

Using the following substitutions (inverter):

* Vin = VGS = VOH = VDD = 1.2 V
* VDS = Vout = VOL = 0.1 V
* L = 0.1 µm
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Using the following substitutions (load):

* Vin = VDS = VOH = VDD = 1.2 V
* Vout = VOL = 0.1 V
* VGS = 1.6 – 0.1 = 1.5 V
* L = 0.1 µm
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Note that the difference this time between linear-enhancement and saturated-enhancement is VGS of the load pull-up transistor. Also note that Vin for the linear region inverter pull-down transistor remains at 1.2 V.

Equating for Winverter and throwing into wolfram (no need to simplify if wolfram does it all 😊):

1. **Results explanation**

|  |  |  |
| --- | --- | --- |
| Resistive Load | Saturated-Enhancement-Load | Linear-Enhancement-Load |
| 0.634 µm | 0.174 µm | 0.140 µm |

Table 0. Calculated widths for each inverter.

The resistive load inverter appears to have the highest width, followed by Saturated-Enhancement, then Linear-Enhancement. The resistor in digital design is probably worse than using a MOSFET due to area which in turn means a slower and larger circuit area. The Saturated-Enhancement load inverter replaces the resistor with a MOSFET, where the max input voltage is limited by VDD – VT., which has tradeoffs such a lower saturation operation threshold. The Linear-Enhancement load inverter introduces a higher V­GG, which means that biasing the gate voltage to exactly VT above drain voltage allows linear operation and increases the saturation operation threshold.

Diagram, schematic

Description automatically generated



1. The intended function of the circuit should be as a non-inverting buffer. It resembles an inverter except the PMOS and NMOS are switched, with the Vout at the source. If we set logic in to be HIGH, we get HIGH as output, and vice-versa setting logic in to LOW, gets LOW as output, with VOH being maximum VDD – VT due to NMOS pull-up and VOL being minimum VT due to PMOS pull-down, assuming same threshold voltage VT for both PMOS and NMOS.
2. The dc voltage transfer characteristic is drawn below with the following notes:
   1. We start from Vin = 0 V and output is VOL = VT and increase the voltage. The output should not change until NMOS turns on and pulls output up at Vin = 2VT.
   2. Output voltage increases as input voltage increases until VDD, where output is at most VOH = VDD – VT.
   3. When decreasing V­in, the output does not decrease until Vin drops below VDD – VT
   4. Then at VDD - 2VT we see that the output decreases until VT is reached at output, or VOL

Diagram

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Figure 1. DC Voltage Characteristic of a ‘Non-inverting Buffer’ depicting hysteresis

1. Ideally, gain should be 1. However from the plot, we see slopes that indicate not 1, because of the fact that V­in of 0 to VDD does not correspond to a Vin­ of 0 to VDD, but rather VOL to VOH which each differ by VT. Also, the output high and low must be above and below VIL respectively, which is not the case. Thus the circuit is not a valid gate. Output is not ideal; output low is not tied to zero, but rather VT because the PMOS turns off before VOL reaches 0 V.
2. CAD Tool Validation with VDD = 0.9 V. Here is the buffer:

A screenshot of a computer

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Figure 2. Buffer schematic (left) and buffer symbol (right)

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Figure 3. Buffer test bench circuit with Vdd = 0.9 V and Vout attached to 1pF capacitor.

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Figure 4. Sweep of Vin from 0 to 0.9 V (Green) with output Vout (Red).

Chart, line chart

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Figure 5. Differences in Input vs Output (Not exactly 0 to VDD)

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Figure 6. Derivative of output.

From figure 5, we can see that there are differences between Vin and Vout and it does not match 1:1 due to the bound of VT. Figure 6 tells us information about the gain. Although it has a high gain region between two low gain regions, the gain must be greater than 1 for the high gain region, so the design is still invalid. Hysteresis is difficult to see in the outputs, which can be explained that perhaps there is not much hysteresis as exaggerated by the hand-drawn plot in figure 1.

Diagram

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1. Body effect factor

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Figure 7. Body Effect schematic

We measure VT ­at different source voltages. V2 is fixed to a certain value, and DC sweep is performed for V1 from 0 to 5 V and VT is measured at the point where current rises, with arbitrary threshold at 1 µA.

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Figure 8. Sample plot of Vin vs IDS, where marker is placed at threshold of 1 µA. VT is recorded and put into a table.

Note that for all V2 > 0, we will need to subtract VT by V2 since that VDs = V1 – V2.

|  |  |  |
| --- | --- | --- |
| V2 (V) | Vraw (V) | VT (V) |
| 0 | 1.653 | 1.653 |
| 0.1 | 1.752 | 1.652 |
| 0.2 | 1.850 | 1.650 |
| 0.3 | 1.949 | 1.649 |
| 0.4 | 2.048 | 1.648 |
| 0.8 | 2.443 | 1.643 |
| 1.1 | 2.740 | 1.640 |
| 1.5 | 3.137 | 1.637 |

Table 1. Values collected for VT while varying V2.

Now we can use the formula below to calculate body-effect:

We’re given 2in the question, and VT0 is calculated to be 1.653 when VSB = 0. VSB is V2.

|  |  |  |
| --- | --- | --- |
| V2 (V) | VT (V) | () |
| 0 | 1.653 | 0 |
| 0.1 | 1.652 | -0.01928 |
| 0.2 | 1.650 | -0.02966 |
| 0.3 | 1.649 | -0.02699 |
| 0.4 | 1.648 | -0.02587 |
| 0.8 | 1.643 | -0.02793 |
| 1.1 | 1.640 | -0.02772 |
| 1.5 | 1.637 | -0.02646 |

Table 2. Calculated body-effect using formula above

Table

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Figure 9. Excel calculated value with formula at top of figure.

Thus we see that body-effect varies from ~0.02 to 0.026 given varying voltage between source and substrate bulk.

Netlist is below:

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Figure 10. Netlist for body-effect and channel length modulation factor

1. Channel Length modulation factor (λ)

Chart, line chart

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Figure 11. Setting sweep of VDS from 0 to 100 V.

Although figure 11 sets voltage to 100 V as a hyperbole (also rip transistor), I’ve found that setting to 5V and drawing a line yields a similar result for channel length modulation factor (intercept at ~4.6V – 1.65 = 2.95 V = VGS). See figure 12.

A computer screen capture

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Figure 12. Sweep from 0 to 5 volts. This yields a similar result to finding the derivative for the hyperbole sweep.

Diagram

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Figure 13. Slides on how to find channel length modulation.

Chart

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Figure 14. Derivative to get slope of linear ~= 2.77211E33.

Knowing a point (23.1253, 55.6863E33) we can use y = mx + b, and solve for b first, then get point at which y = 0:

For (x, 0):

This is extremely similar to the intercept we get with a 0-5V sweep, 2.95 V. See text above figure 12 for context. Following figure 13, we get λ = 1/x ~= 0.329 or 0.339 depending on following the hyperbole sweep or 5v sweep.

Graphical user interface, text, application

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1. First we need C­ox, computed using:

ɛox is the SiO2 permittivity \* free space permissibility (F/m). Thickness (m), tox, is given in the question.

We also need Cov computed using:

L­diffusion is given in the question (m), and we’ve just previously solved for Cox, (F/m2). We can also assume fringe capacitance Cf is 0 since Tpoly is not given.

We also need worst total gate capacitance Cg per unit width:

L is given in question (m). Overlap is not included.

If we include overlap, then it becomes:

There is two of Cov due to parallel capacitances. Width isn’t in calculation because this is in terms of unit width.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Cutoff | Linear | Saturation |
| **CGS** | Cov | 1/2CgW + Cov | 2/3CgW + Cov |
| **CGD** | Cov | 1/2CgW + Cov | Cov |
| **CGB** | CgW | 0 | 0 |

Table 3a. Capacitance equations for gate-source, gate-drain, gate-bulk.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Cutoff | Linear | Saturation |
| **CGS** | 0.19 | 0.89 | 1.12 |
| **CGD** | 0.19 | 0.89 | 0.19 |
| **CGB** | 1.4 | 0 | 0 |

Table 3b. Capacitance values for gate-source, gate-drain, gate-bulk. Units in fF/µm

1. Now we want to find Cj in units of fF/µm. We first need the voltage asymptote φB:

These constants are from the question.

Now we want Cjb:

We use Si permittivity \* free space permissibility.

Now we can solve for C­j­:

M is 0.5. Worst case takes into account both sides as well as Vj = 0 V. Y is given in the question, and so is x­j and W.

1. Drain junction capacitance equation is the same as in b, but just single xj:
   1. With Vj = -1.8 V, we get Cj = 0.299 fF.
2. With Vj = 0 V, we get Cj = 0.511 fF.

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1. Inverter delay with four identical inverters at output. Pull-up means PMOS W/L 8λ:2λ, pull-down means NMOS W/L 4λ:2λ. Assuming Cg = 1fF/um from the useful formulas, knowing that 2λ = 45nm:

The 4 times is for the parallel capacitances at the output of the inverter. Similarly:

And then we can sum the two to get the total capacitance:

For delay, as given in class we can approximate the resistance as R = Reqn (L/W), where 45nm Rn is 34k Ω µm and Rp is 68 kΩ µm. We also know that ramp is just RC:

1. Inverter delay with series of 4 identical inverters, so 5 inverters in total in series.

Each inverter would have an equivalent Cself = 0.27 fF. Since its cascading, we can simply multiply by 5 to get the equivalent Ctotal = 5Cself = 1.35 fF. The load here is a wire. Thus:

**References:**

Useful physical constants: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/9781119009597.app3>