ELEC 402

Sequential Design (Timing)

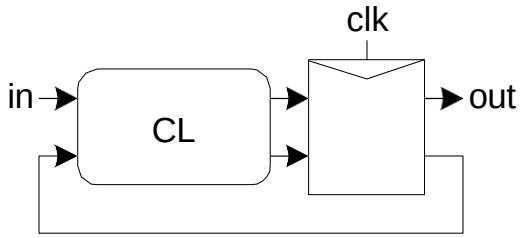
Lecture 14

Reza Molavi
Dept. of ECE
University of British Columbia
reza@ece.ubc.ca

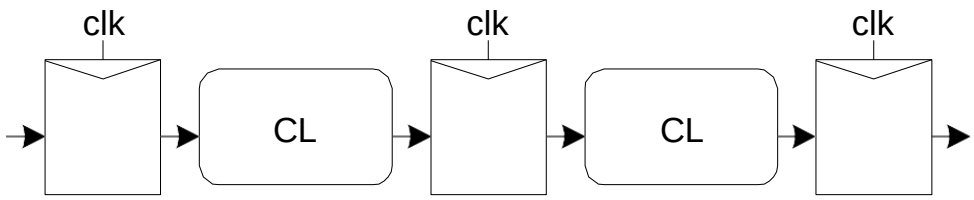
Slides Courtesy : Prof. Sudip Shekhar (UBC)

Combinational vs. Sequential Logic

- ***Combinational logic***
  - **output depends on current inputs**
- ***Sequential logic***
  - **output depends on current and previous inputs**
  - **Requires separating previous, current, future**
  - **Called *state* or *tokens***
  - **Ex: FSM, pipeline**

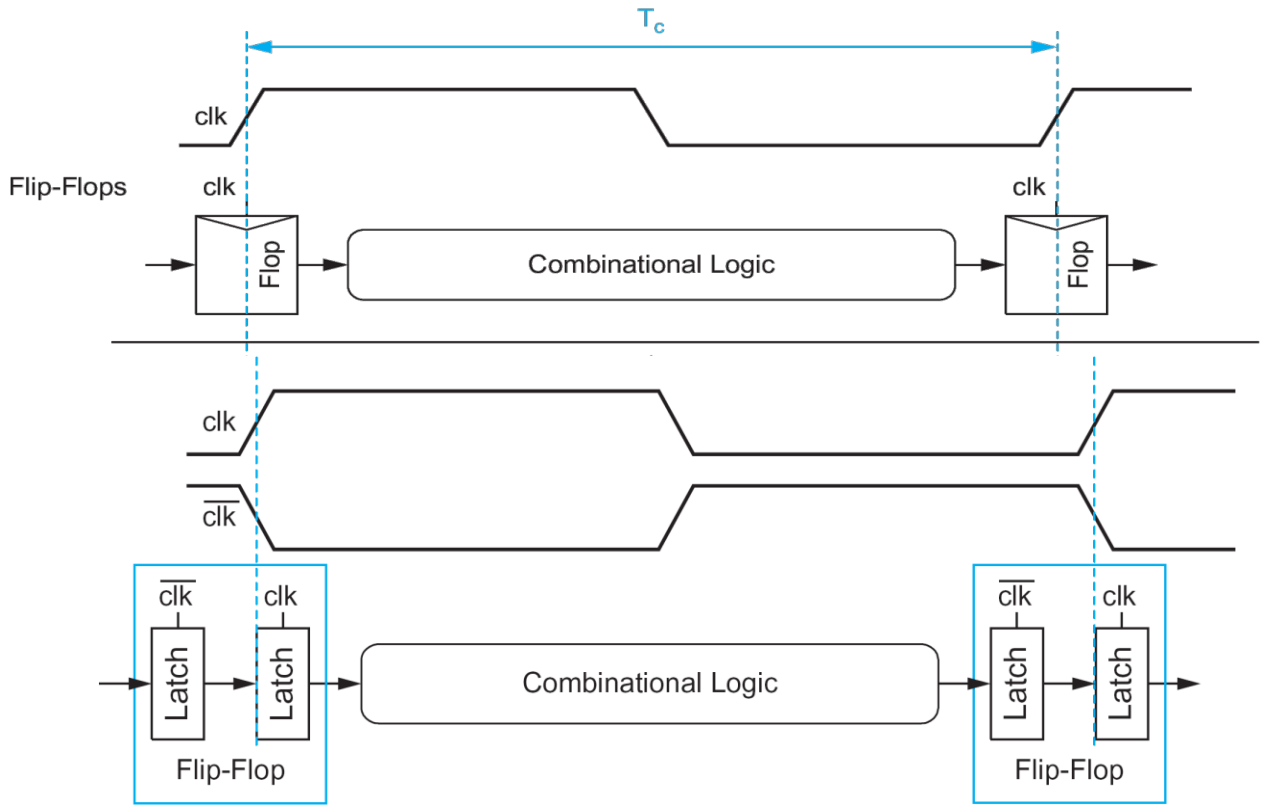


Finite State Machine



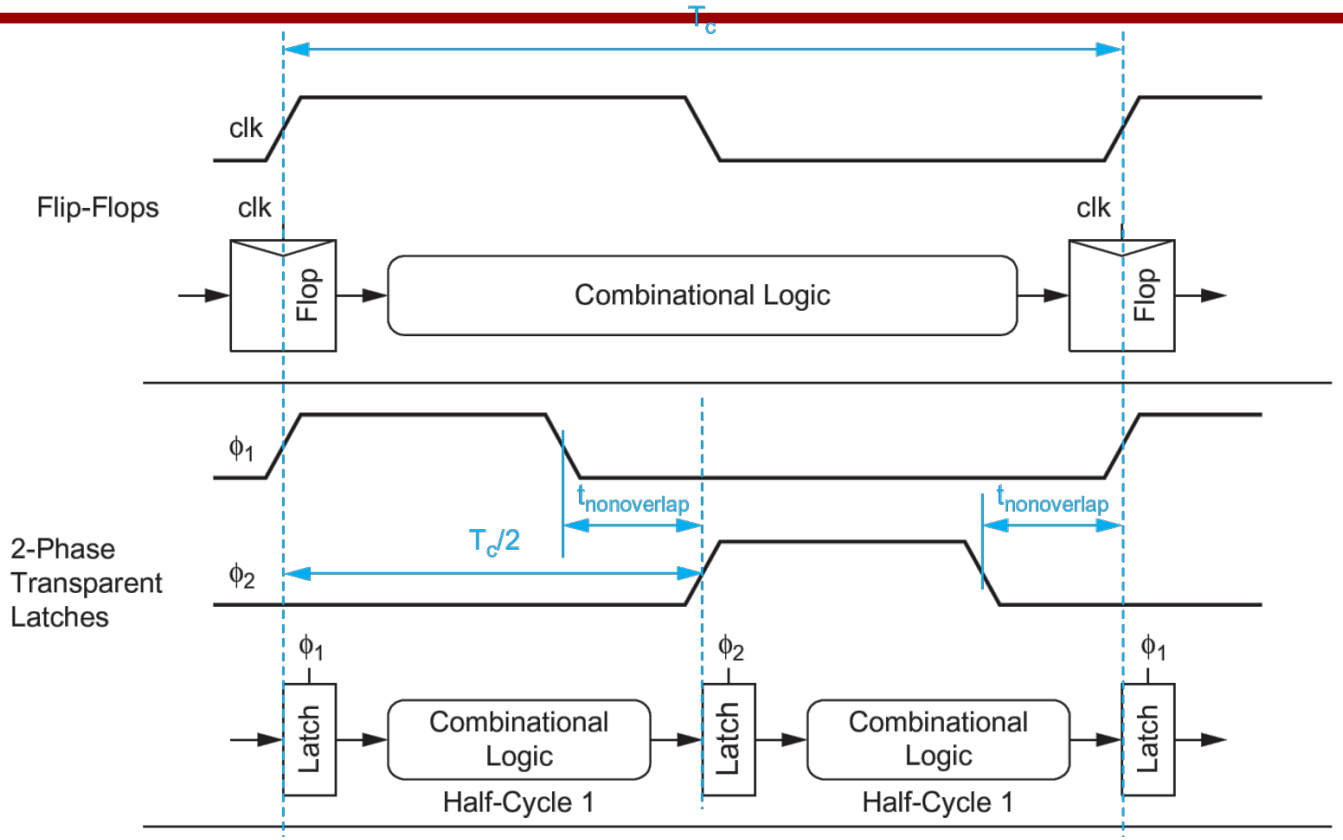
Pipeline

Sequencing using F/Fs



- **Can we separate the latches and divide the fullcycle of combinational logic into 2 phases, called half-cycles?**
- **The two latch clocks can be clk and clk', or nonoverlapping ϕ_1 and ϕ_2.**

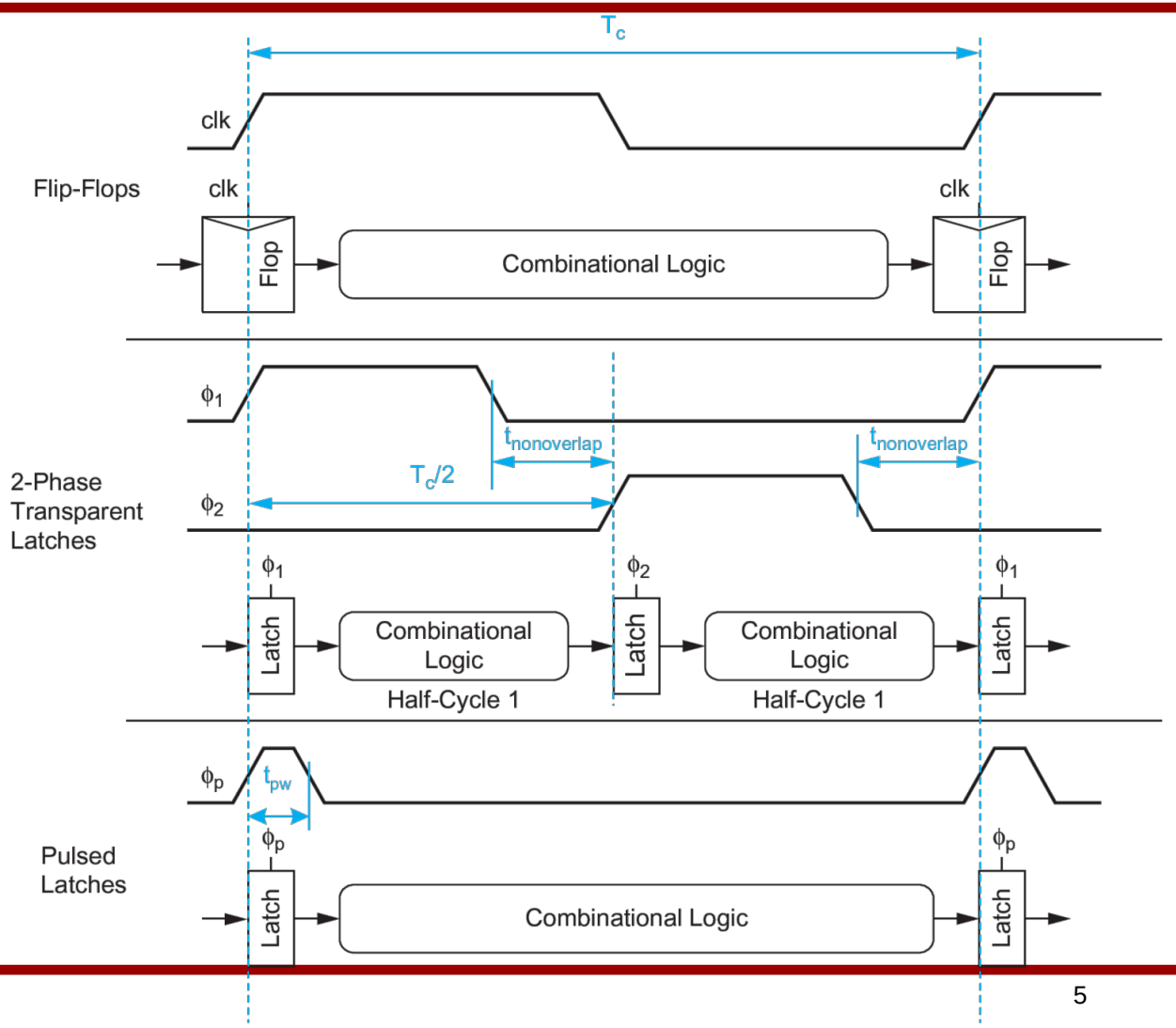
Sequencing w/ 2-Phase Latches



- **At any given time, at least one clock is low and the corresponding clock is opaque, preventing one token from catching up with another.**

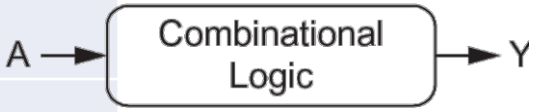
Sequencing w/ Pulsed Latch

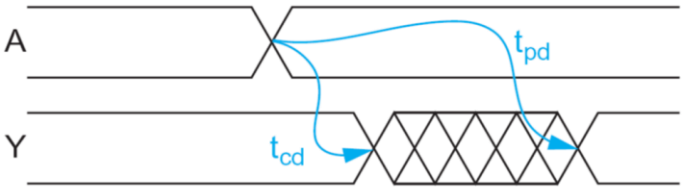
- **Eliminate one of the latches from each cycle and apply a brief pulse to the remaining latch.**
- **If the pulse is shorter than the delay through the combinational logic, a token will only advance through one clock cycle on each pulse.**

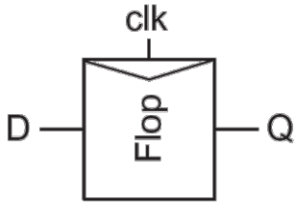


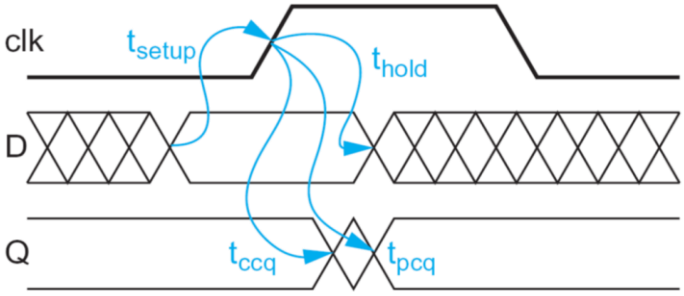
Contamination & Propagation Delays (Definitions)

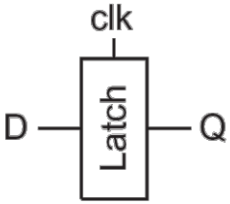
t_{pd}	Logic Prop. Delay
t_{cd}	Logic Cont. Delay
t_{pcq}	Latch/Flop Clk→Q Prop. Delay
t_{ccq}	Latch/Flop Clk→Q Cont. Delay
t_{pdq}	Latch D→Q Prop. Delay
t_{cdq}	Latch D→Q Cont. Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time

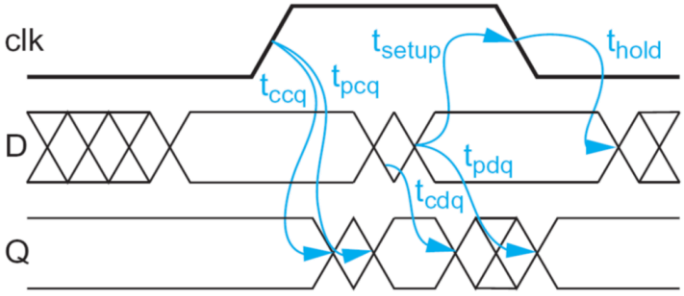








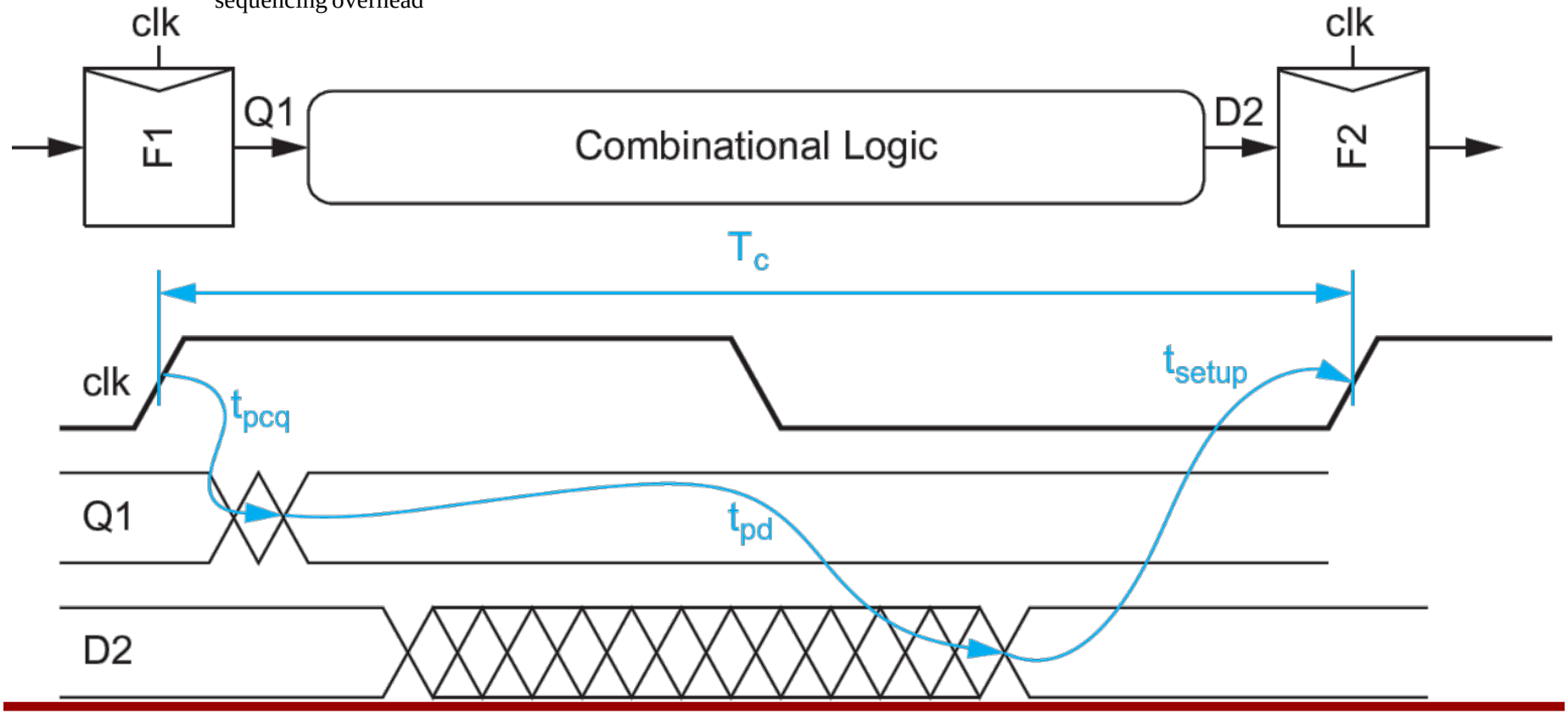




Max-Delay: Flip-Flops

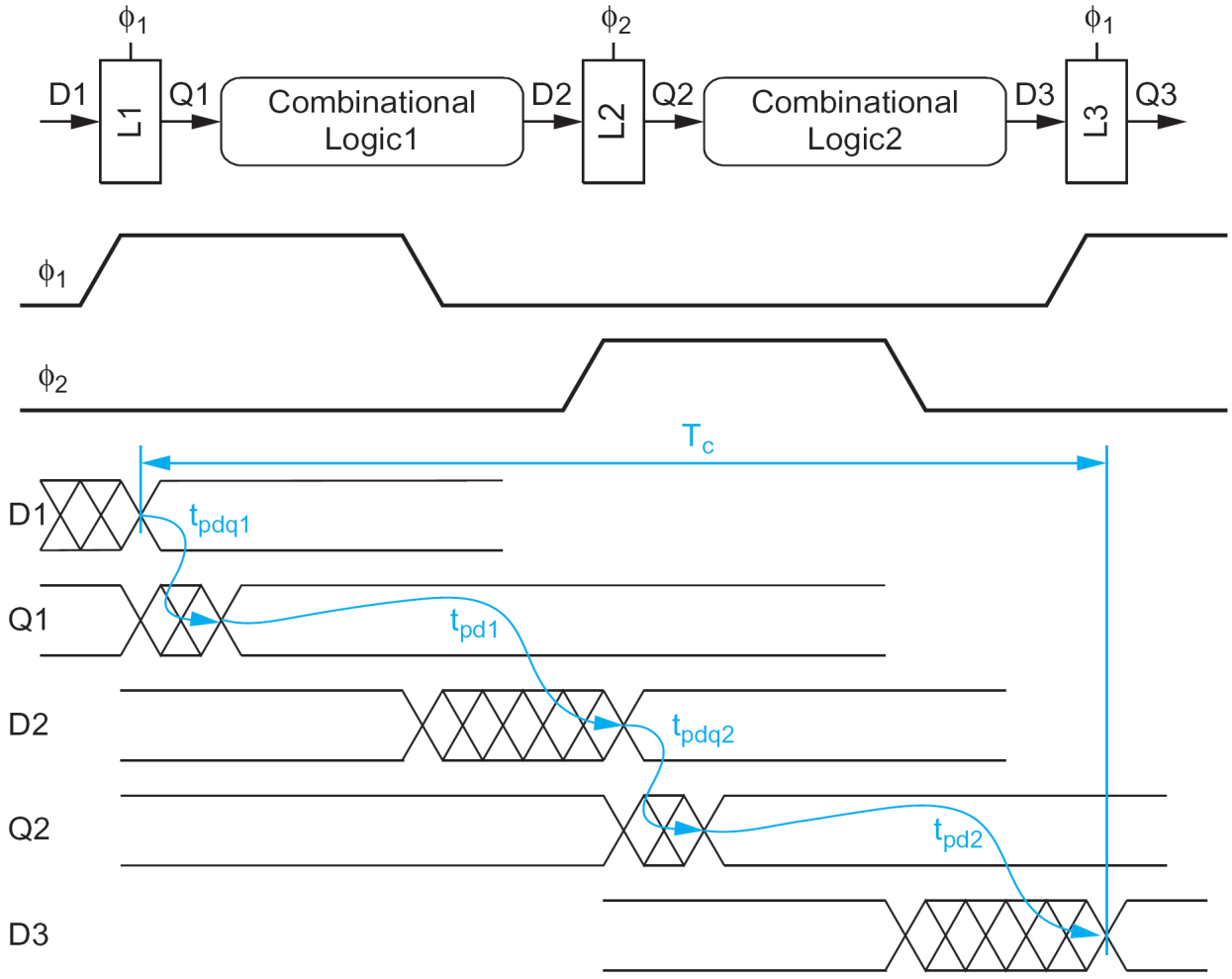
$$t_{pd} \leq T_c - \underbrace{\left(t_{\text{setup}} + t_{pcq}\right)}_{\text{sequencing overhead}}$$

Token must be ready at D2 before the arrival of next rising edge of clock. This sets the maximum delay through combinational logic

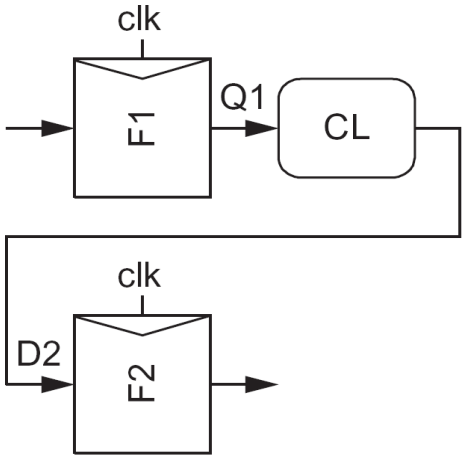


Max-Delay: Two Phase Latches

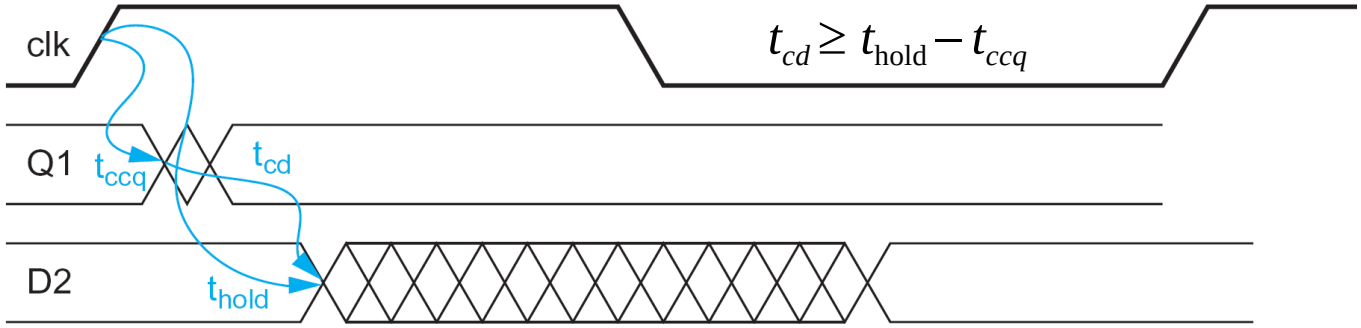
$$t_{pd} = t_{pd1} + t_{pd2} \le T_c - \underbrace{(2t_{pdq})}_{\text{sequencing overhead}}$$



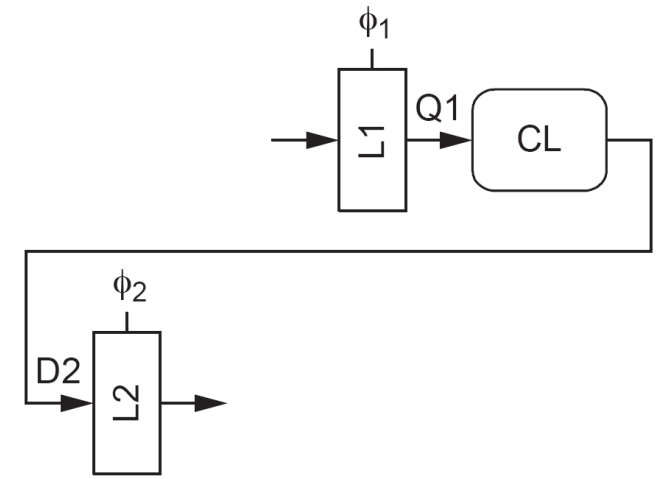
Min-Delay: Flip-Flops

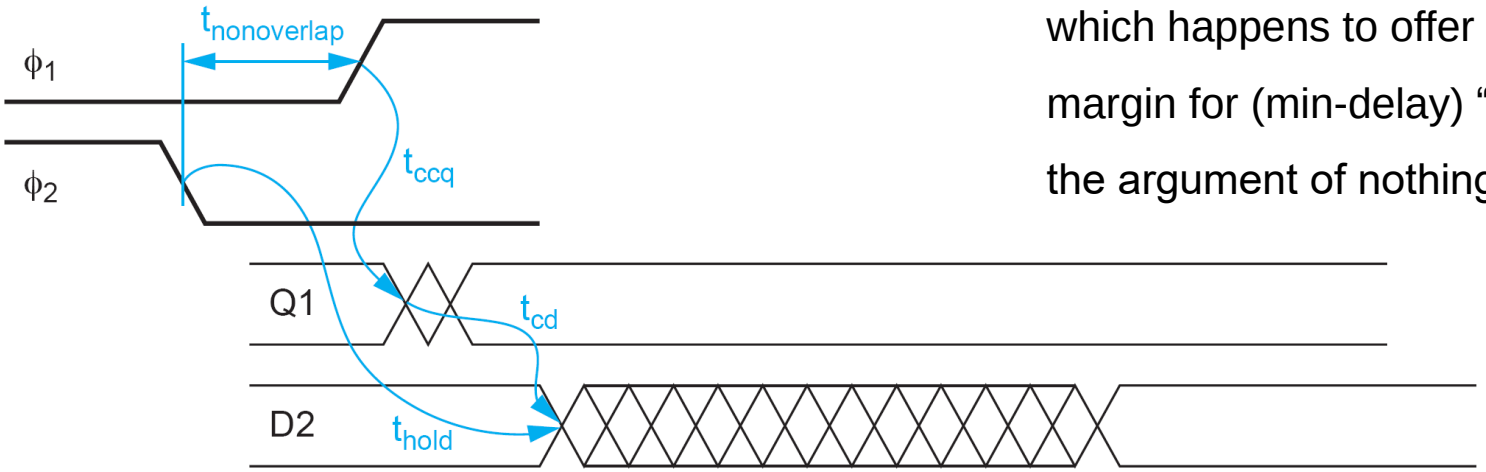


If delay between consecutive FF is too Small, tokens can accidentally pass through two registers in one clock cycle and distort data path (to avoid we can insert delay lines between them)



Min-Delay: 2-Phase Latches





$$t_{cd1}, t_{cd2} \geq t_{\text{hold}} - t_{ccq} - t_{\text{nonoverlap}}$$

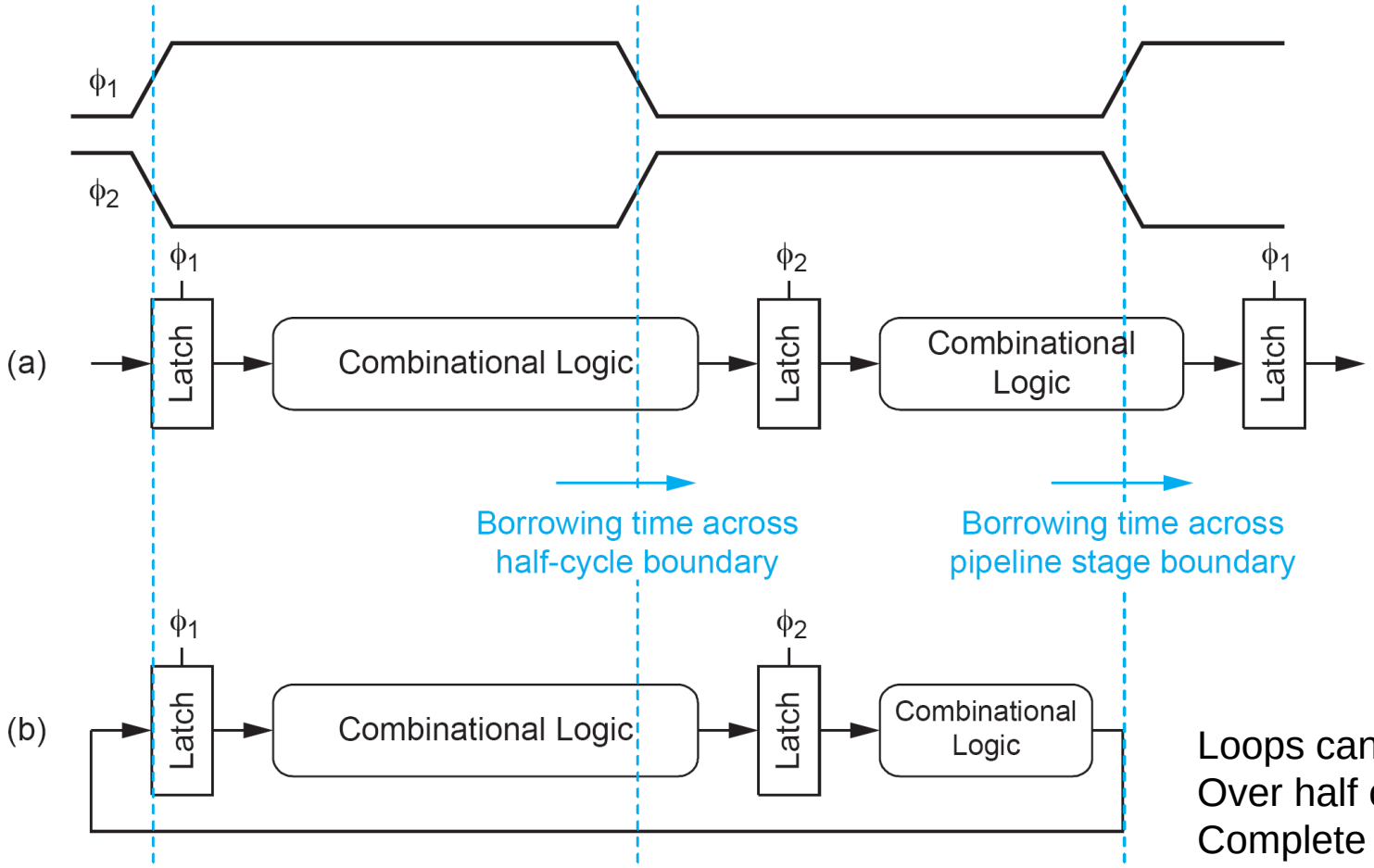
Hold time reduced by nonoverlap

- There is a delay penalty when using non-overlapping clocks for 2-phase systems (max-delay) which happens to offer some extra margin for (min-delay) “manifesting the argument of nothing is perfect!”

Time Borrowing

- **In a flop-based system:**
  - **Data launches on one rising edge**
  - **Must setup before next rising edge**
  - **If it arrives late, system fails**
  - **If it arrives early, time is wasted**
  - **Flops have hard edges**
- **In a latch-based system**
  - **Data can pass through latch while transparent**
  - **Long cycle of logic can borrow time into next**
  - **As long as each loop completes in one cycle**

Time Borrowing Example

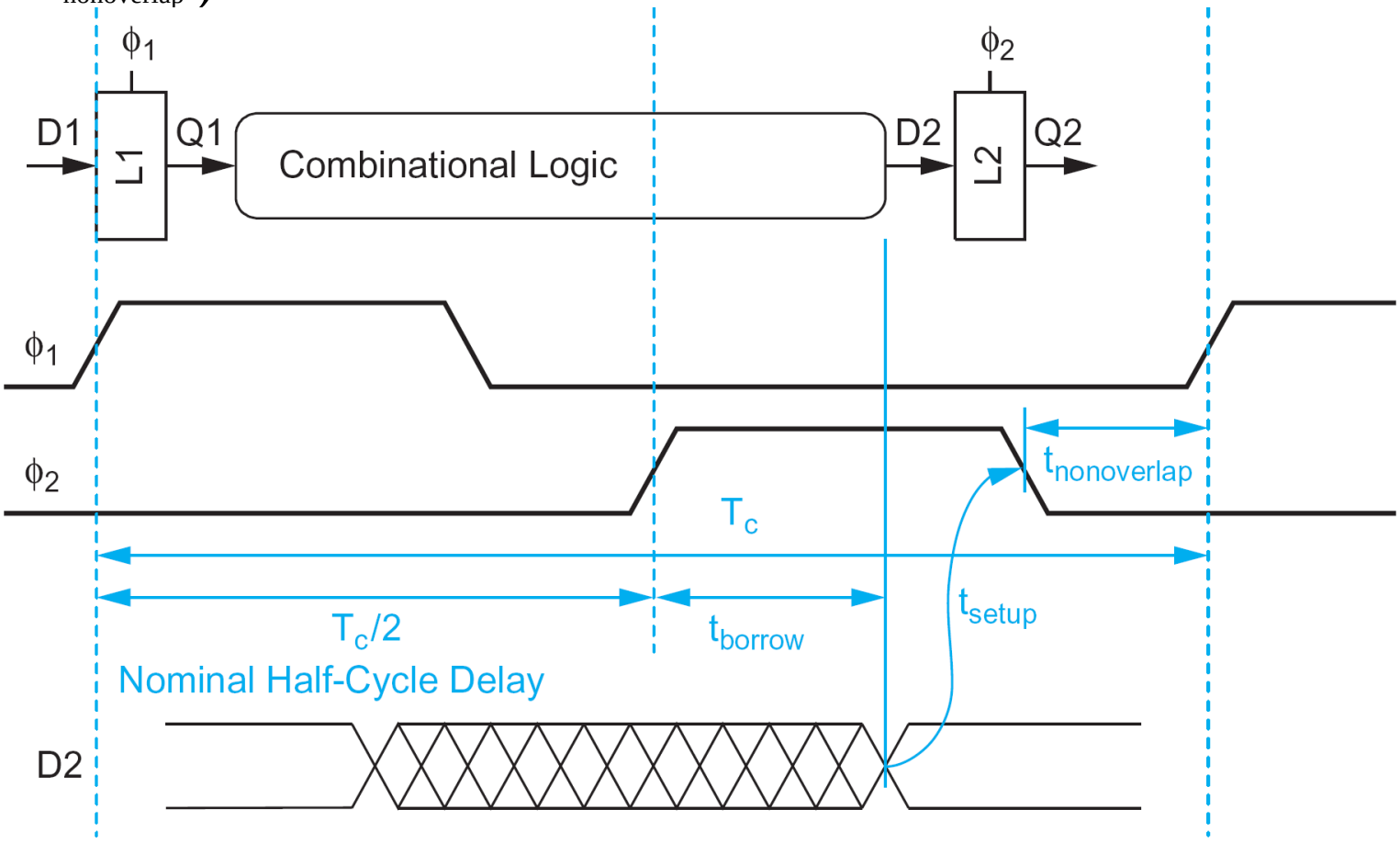


Loops can borrow time
Over half cycles but must
Complete within one cycle

How Much Borrowing?

$$t_{borrow} \leq \frac{T_c}{2} - \left(t_{setup} + t_{nonoverlap}\right)$$

2-Phase Latches



Clock Skew

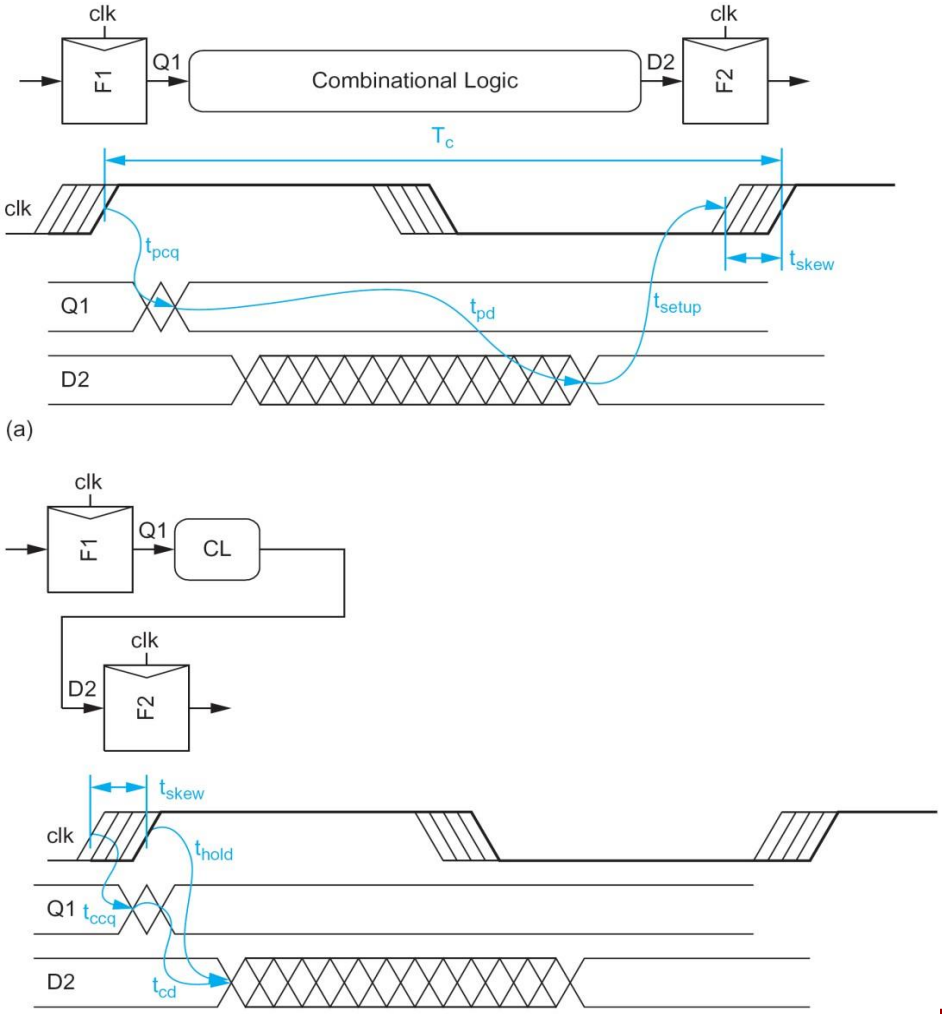
- **We have assumed zero clock skew**
- **Clocks really have uncertainty in arrival time (worsening overall performance)**
  - **Decreases maximum propagation delay**
  - **Increases minimum contamination delay**
  - **Decreases time borrowing**

Skew: Flip-Flops

$$t_{pd} \le T_c - \underbrace{\left(t_{pcq} + t_{\text{setup}} + t_{\text{skew}}\right)}_{\text{sequencing overhead}}$$

$$t_{cd} \ge t_{\text{hold}} - t_{ccq} + t_{\text{skew}}$$

Skew affects both max-delay and Min-delay margins, i.e. you may afford less combinational logic between your Registers (max-delay margin) or need more delay between your gates (min-delay margin)



Skew: Latches

$$t_{pd} \le T_c - \underbrace{\left(2t_{pdq}\right)}_{\text{sequencing overhead}}$$

2-Phase Latches

$$t_{cd1}, t_{cd2} \ge t_{\text{hold}} - t_{ccq} - t_{\text{nonoverlap}} + t_{\text{skew}}$$

$$t_{\text{borrow}} \le \frac{T_c}{2} - \left(t_{\text{setup}} + t_{\text{nonoverlap}} + t_{\text{skew}}\right)$$