ELEC 402

MOS Basics
Lecture 4

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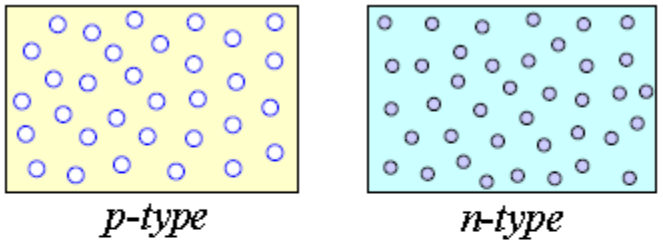
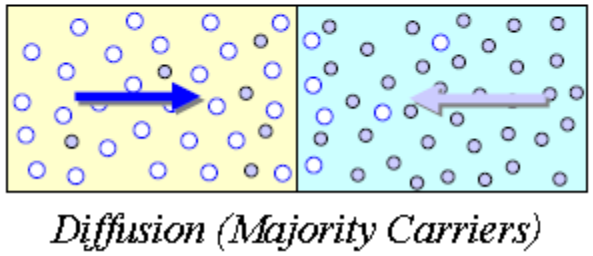
PN Junction and Diodes

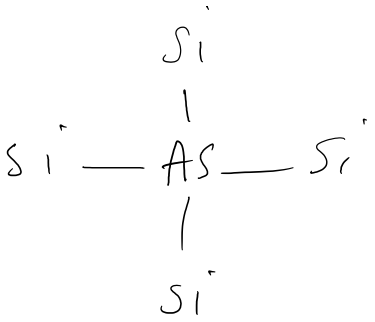
p-type semi-conductor heavily doped with acceptor atoms, e.g. boron



n-type semi-conductor is heavily doped with donor atoms, e.g. arsenic and phosphorus

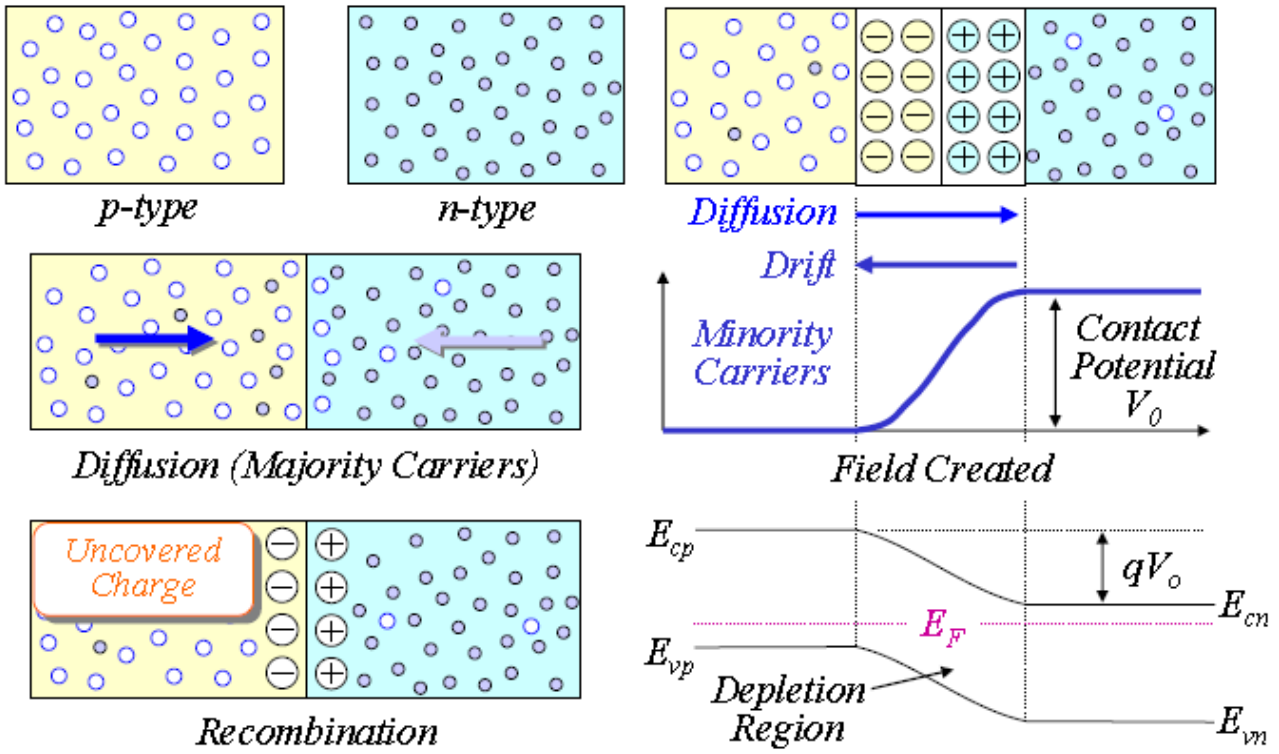
PN Junction





- The concentration of different carrier in p, and n-type semi-conductors (also called gradient) causes diffusion of electrons from *n* to *p* and holes from *p* to *n* leaving immobile ions behind
- The region at junction where majority carriers are removed, is called the *depletion* or *space-charge region*

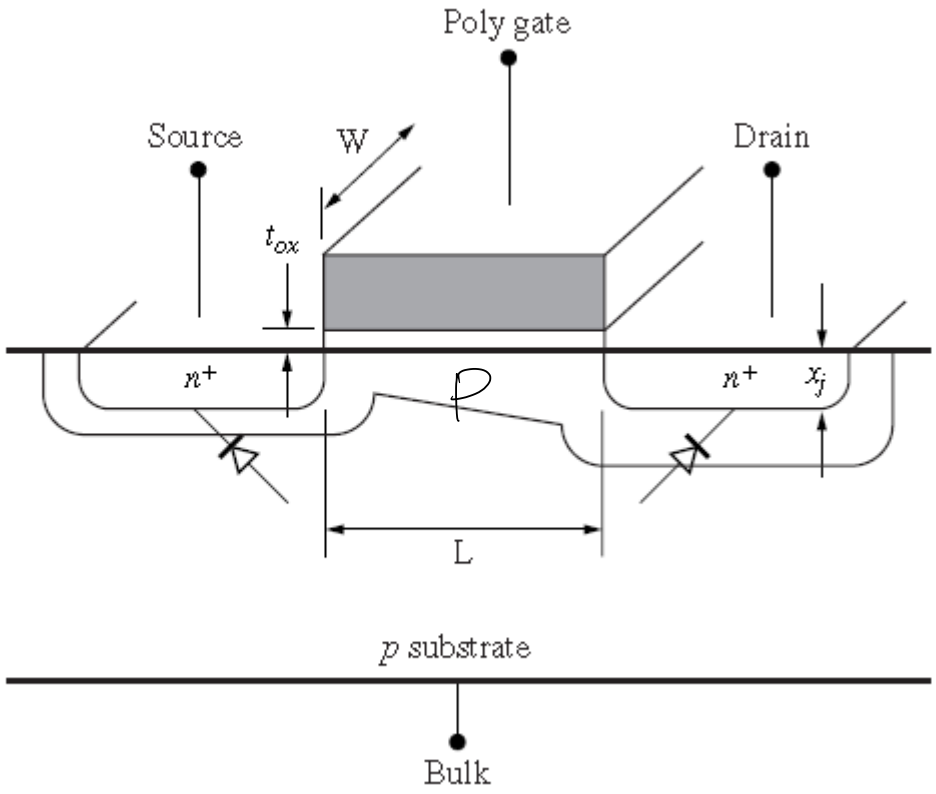
PN Junction Basics

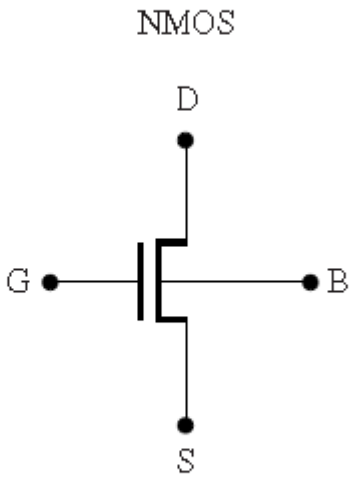


- The charges in each region create an electric field across the boundary of junction to counteract the diffusion of majority carriers

-This electric field creates a potential across the junction called *contact* or *barrier potential*

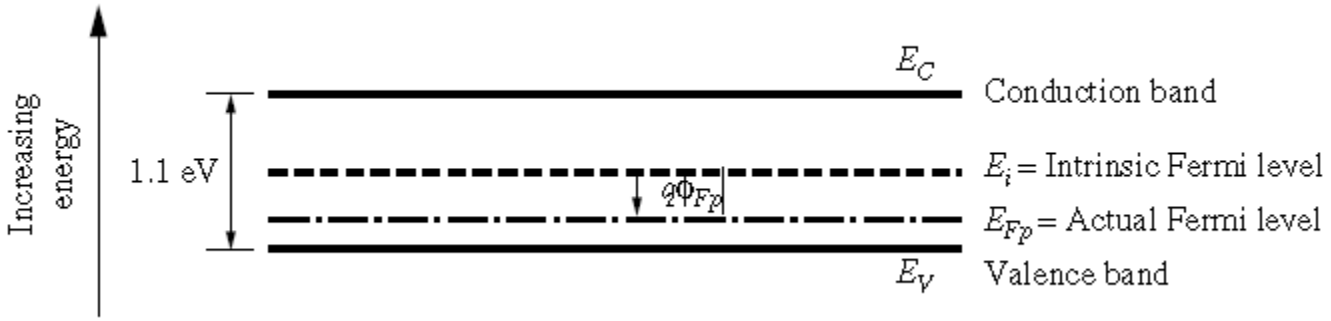
MOS Transistor Basics





The source and drain regions (*n*+) and substrate (*p*) in NMOS transistor create two back-to-back diodes at equilibrium (therefore, requires external stimulus for any conduction)

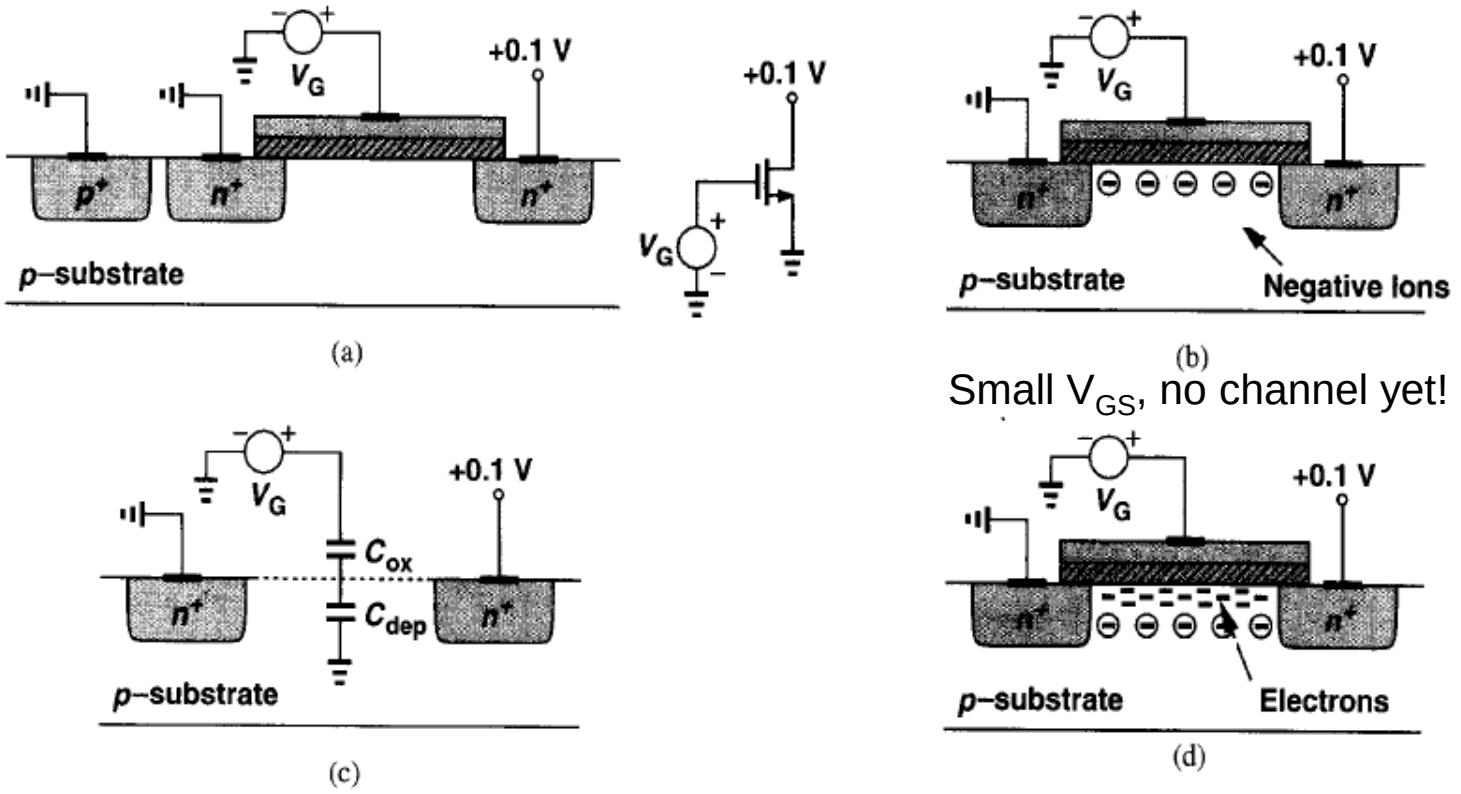
Definition of Threshold Voltage



Energy-band diagram for doped *p*-type silicon.

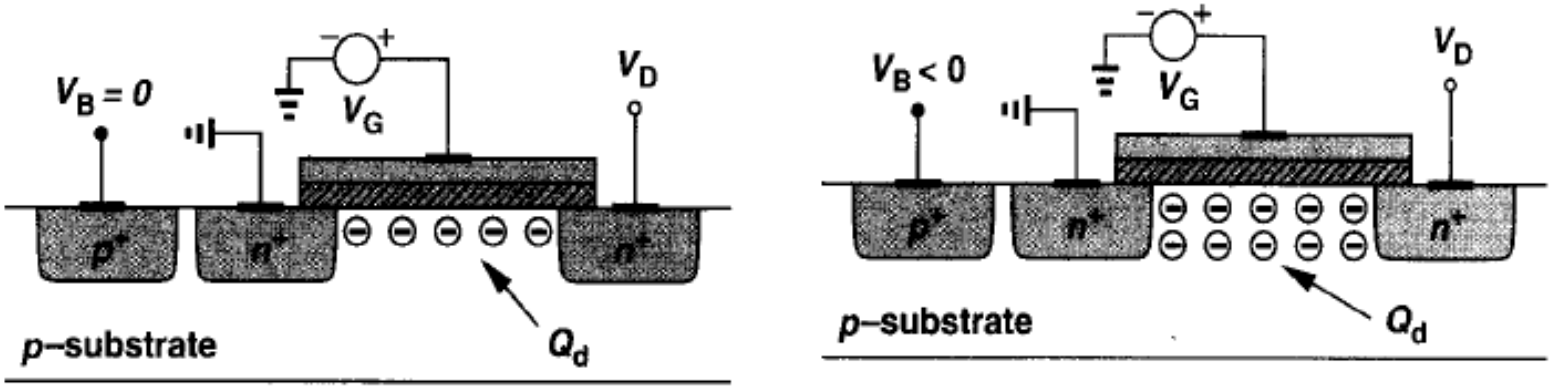
- We need to apply an external voltage to turn the *p*-type substrate into an *n*-type substrate to create a channel for conduction
- As we apply a positive V_{GS} the substrate is first depleted under the gate area (immobile ions)
- Further increase of V_{GS} creates a conducting layer of minority carriers under the gate
- The V_{GS} voltage required to make the surface of the substrate "as much *n*-type as the rest of substrate is *p*" is called Threshold Voltage

Definition of Threshold Voltage



The onset of inversion in NMOS transistor (creation of channel under the gate in (d)

Effect of Body bias on Threshold Voltage

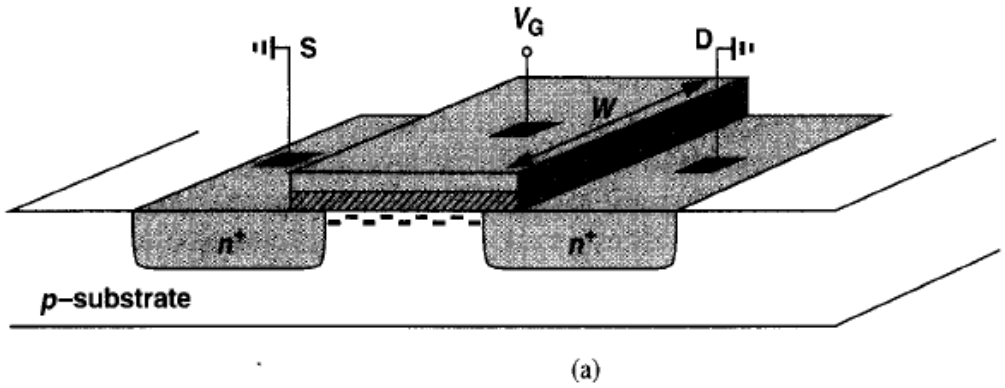


- Application of negative voltage to bulk attracts holes and leaves behind “negatively charged ions”
- As a result, there should be more positive charge on gate plate to mirror the negative ions in the substrate and more positive voltage is required to create the channel, i.e. V_{TH} increases

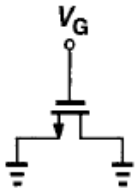
$$V_{T0} + \gamma\left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

where $\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_A}$ *body-effect coefficient*

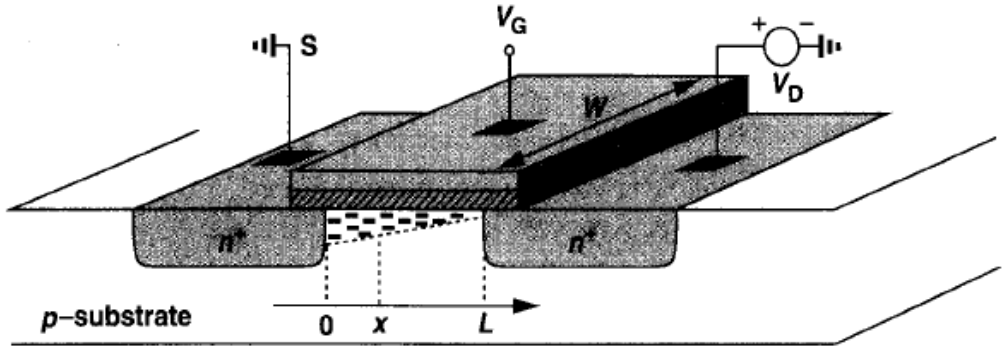
MOS Current Calculation



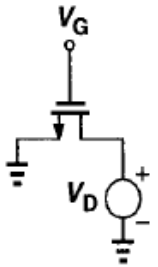
(a)



$V_{GS} > V_{th}$ channel created, no current yet!



(b)



$V_{DS} > 0$ carriers start flowing From source into the drain

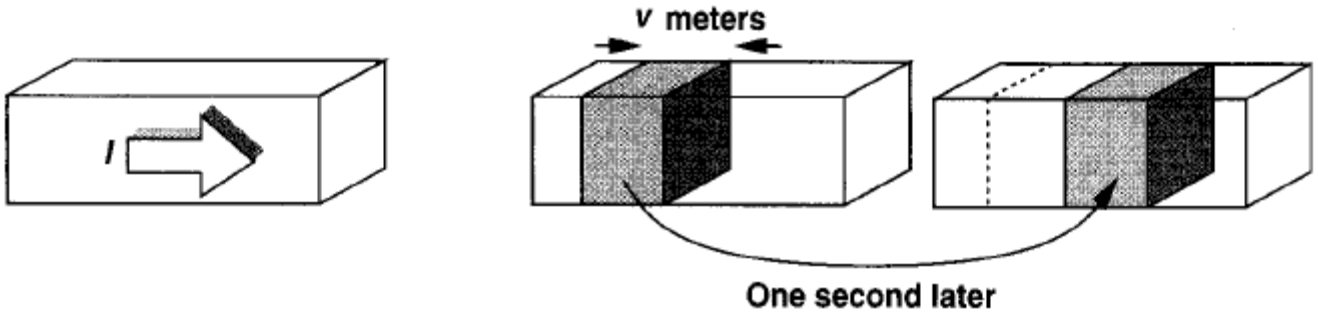
$$Q_n(y) = C_{ox}\left[V_{GS} - V(y) - V_T\right]$$

Charge per unit area

MOS Current Calculation

$$Q_d = W Q_n(y)$$

Charge density along direction of current



$$I = Q_d \cdot v.$$

Total charge in the grey box (amount of charge hat passes through the channel in 1 second)

$$v = \mu E \quad \text{where } E = \frac{dV(y)}{dy}$$

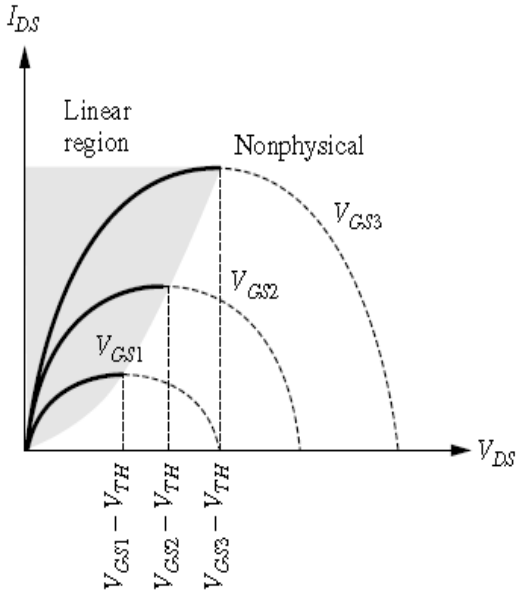
Velocity of carriers is a function of the horizontal electric field

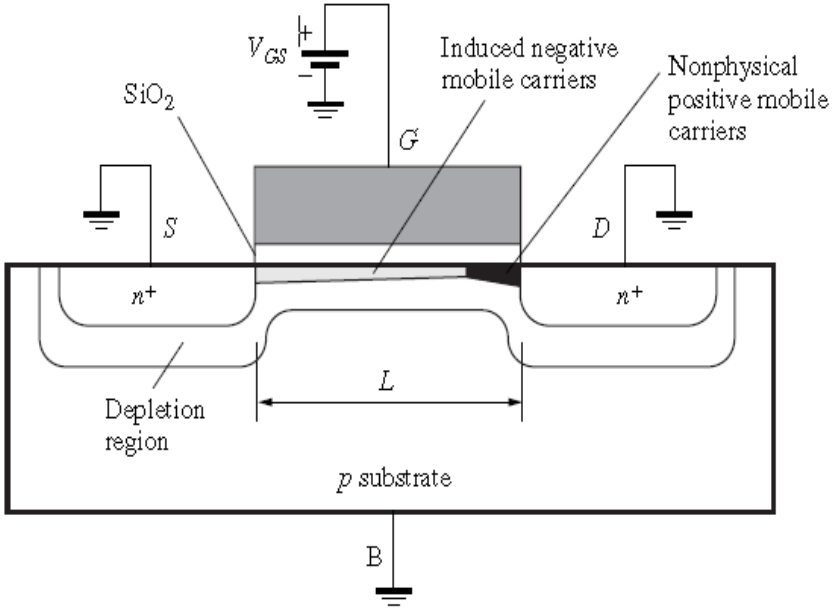
$$I_{DS} = C_{ox}\left[(V_{GS} - V(y)) - V_T\right] \times \mu_n E \times W$$

MOS Current Calculation

$$I_{DS} = k' \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

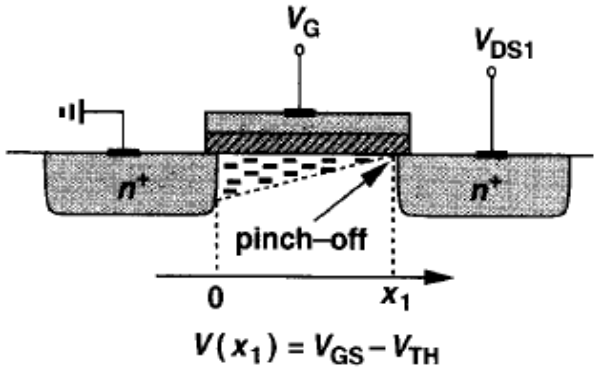
$$k' = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

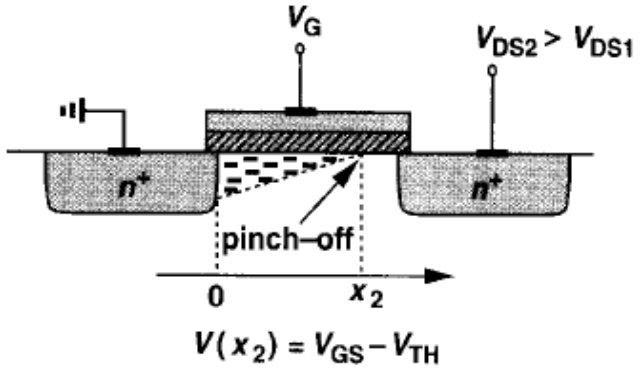


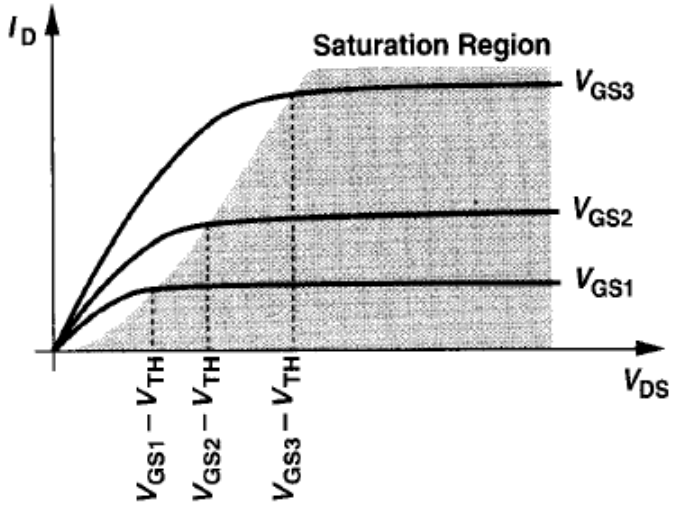


This equation predicts roll-off after reaching a peak due to the existence of non-physical positive carriers. Therefore, the equation must be adjusted after V_{DS} reaches V_{GS}-V_T

MOS Current in Saturation







If we increase V_{DS} beyond V_{GS}-$V_{T,}$ The local potential difference is not enough to sustain the inverted channel. The channel is “pinched-off “

After the pinch-off is reached, the current stays relatively constant!

Ideal Transistor I-V Characteristics

NMOS	CutOff	Linear	Saturation
I_{ds}	0	$\beta_n[(V_{gs}-V_{Tn})V_{ds} - V_{ds}^2/2]$	$\beta_n[(V_{gs}-V_{Tn})^2/2]$
V_{gs}	$V_{gs} < V_{Tn}$	$V_{gs} > V_{Tn}$	$V_{gs} > V_{Tn}$
V_{gd}		$V_{gd} > V_{Tn}$	$V_{gd} < V_{Tn}$

PMOS	CutOff	Linear	Saturation
I_{ds}	0	$\beta_p[(V_{sg}-\lvert V_{Tp}\rvert)V_{sd} - V_{sd}^2/2]$	$\beta_p[(V_{sg}-\lvert V_{Tp}\rvert)^2/2]$
V_{sg}	$V_{sg} < \lvert V_{Tp}\rvert$	$V_{sg} > \lvert V_{Tp}\rvert$	$V_{sg} > \lvert V_{Tp}\rvert$
V_{dg}		$V_{dg} > \lvert V_{Tp}\rvert$	$V_{dg} < \lvert V_{Tp}\rvert$

nMOS I-V (65nm)

L = 50nm W = 100nm

μ_n = 80 cm²/V-s

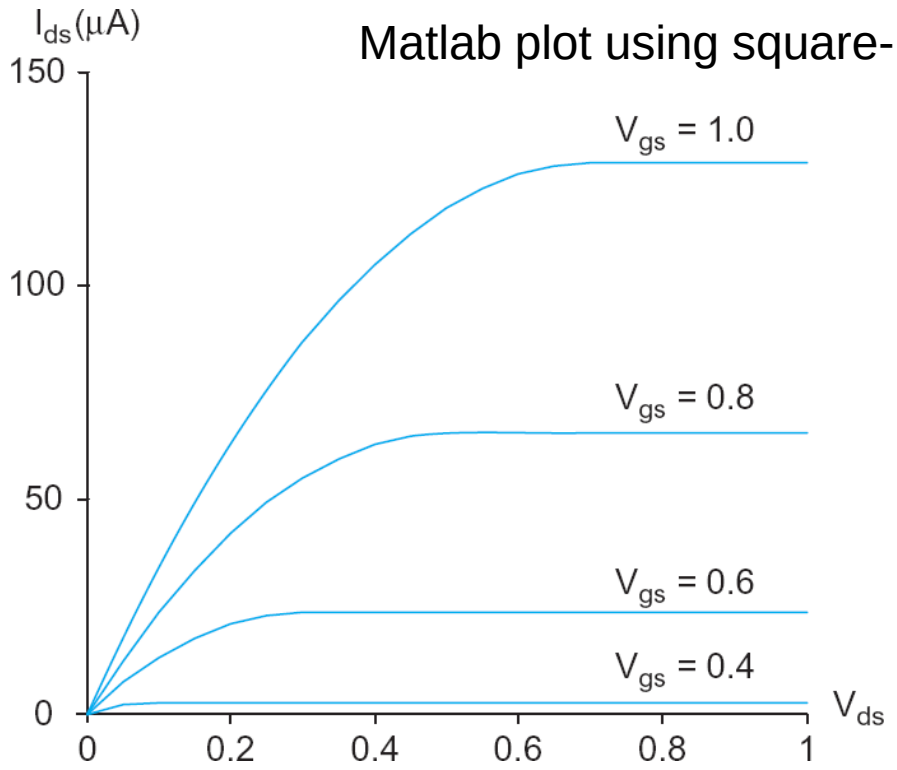
Temp = 70˚C

V_{tn} = 0.3V

t_{ox} = 10.5Å

Calculate β_n

Matlab plot using square-law model

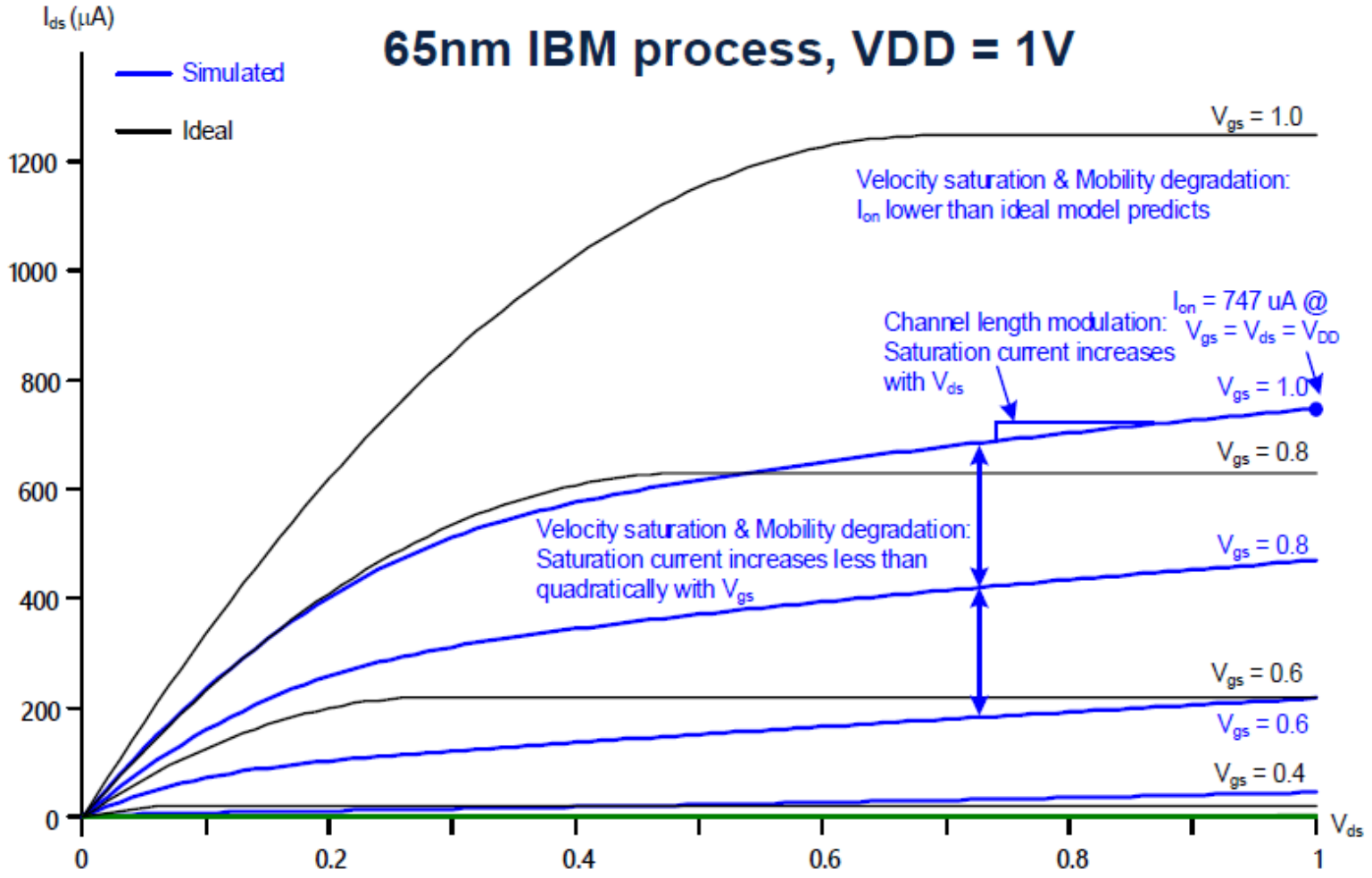


- Overestimates current at high voltages

pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 40 $cm^2/V\text{-}s$ in 65nm process
- Thus pMOS must be wider to provide same current
  - Assume $\mu_n / \mu_p = 2$

Ideal vs Real Transistor I-V Characteristics (Short-Channel Effects)

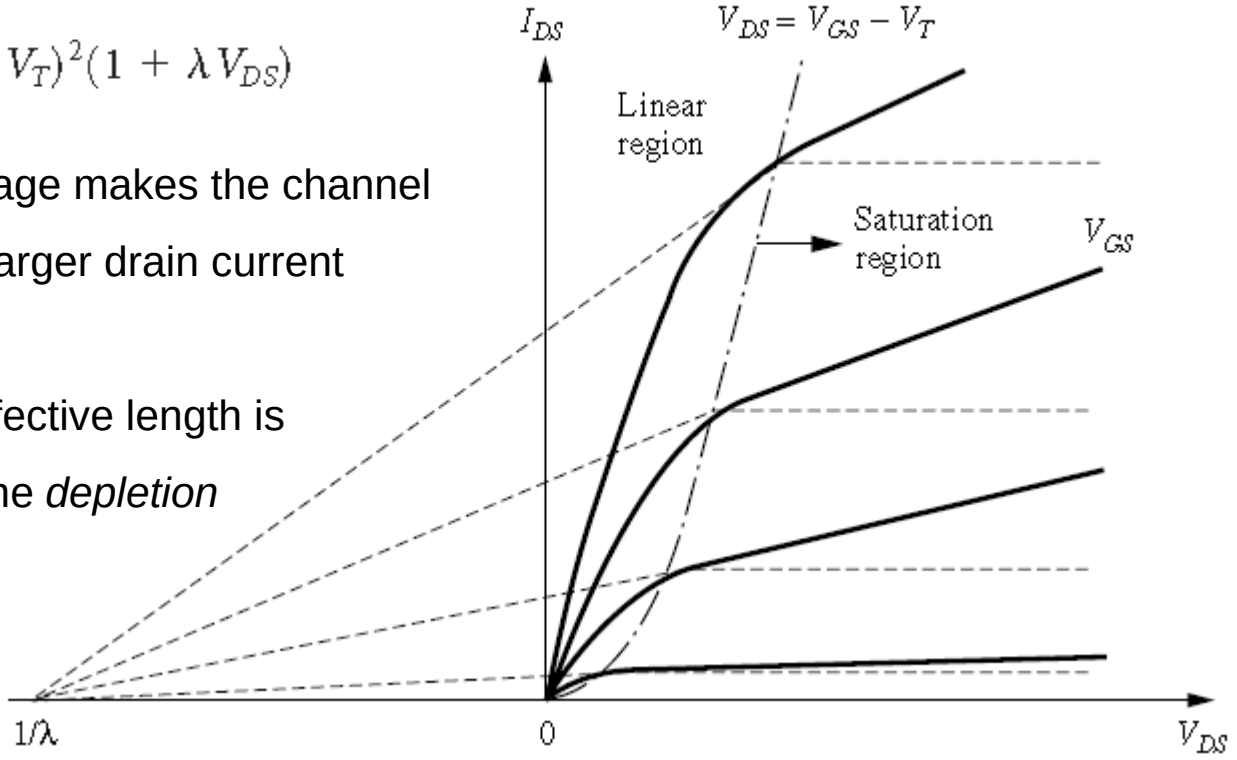


Channel-length Modulation (I_{DS} dependence on V_{DS})

$$I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Large drain-source voltage makes the channel effectively smaller, i.e. larger drain current

The reduction in the effective length is due to the increase in the *depletion width* of reverse-biased pn junction.



Mobility Degradation

- Vertical electric field: $E_{vert} = V_{gs} / t_{ox}$
  - Attracts carriers into channel
  - Long channel: $Q_{channel} \propto E_{vert}$

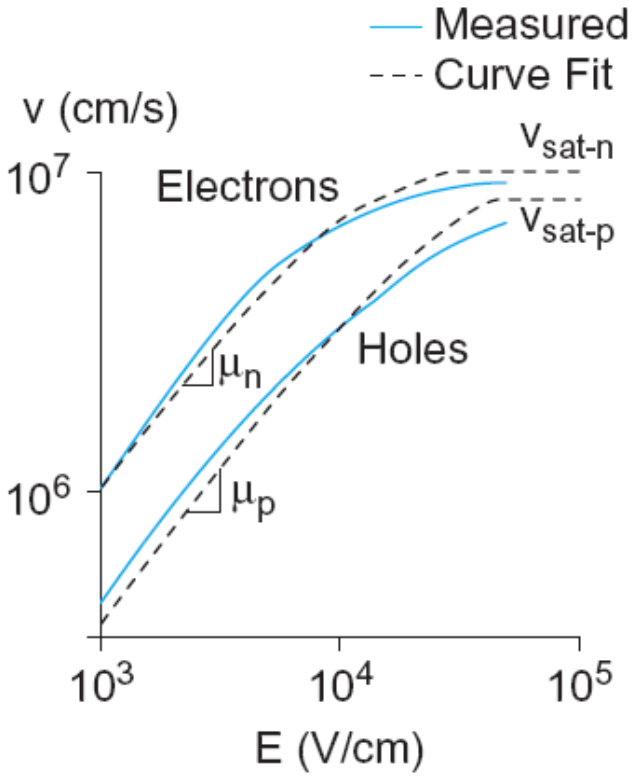
- High E_{vert} effectively reduces mobility
  - Collisions with oxide interface

$$\mu_{\text{eff}-n} = \frac{540 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}}{1 + \left(\frac{V_{gs} + V_t}{0.54 \frac{\text{V}}{\text{nm}} t_{\text{ox}}} \right)^{1.85}} \qquad \mu_{\text{eff}-p} = \frac{185 \frac{\text{cm}^2}{\text{V} \cdot \text{s}}}{1 + \frac{\left| V_{gs} + 1.5 V_t \right|}{0.338 \frac{\text{V}}{\text{nm}} t_{\text{ox}}}}$$

Velocity Saturation

- Lateral electric field: $E_{lat} = V_{ds} / L$
  - Accelerates carriers from drain to source
  - Long channel: $v = \mu E_{lat}$
- At high E_{lat}, carrier velocity rolls off
  - Carriers scatter off atoms in silicon lattice
  - Velocity reaches v_{sat} Electrons: 10^7 cm/s Holes: 8 x cm/s
  - Better model

$$v = \begin{cases} \dfrac{\mu_{\text{eff}} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ v_{\text{sat}} & E \geq E_c \end{cases} \qquad E_c = \frac{2 v_{\text{sat}}}{\mu_{\text{eff}}}$$



What Happens to MOS current due to SCE?

$$I_{DS} = W \times Q_n \times v$$

General current of short channel MOS

$$= W \times C_{ox}(V_{GS} - V_T - V(y))\left(\frac{\mu_e E_y}{1 + \frac{E_y}{E_c}}\right) \qquad \text{where } E_y = \frac{dV(y)}{dy}$$

Plugging in and re-arranging produces

$$I_{DS}dy = W\mu_e\left[C_{ox}(V_{GS} - V_T - V(y)) - \frac{I_{DS}}{W\mu_e E_c}\right]dV(y)$$

After integration, we obtain

$$I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_c L}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

Similar to long channel device except for an extra term in denominator

Short-Channel MOS Current - Derivation

$$I_{DS} = W \times Q_n \times \upsilon_{sat}$$

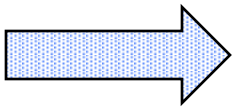
Current of short channel MOS in saturation

Since the current is the same throughout the channel we can set $V(y) = V_{DS}$ and write

$$I_{DS} = W \times C_{ox} (V_{GS} - V_T - V_{DS})\upsilon_{sat}$$

Equating this current and that of previous slide gives the required V_{DS} for saturation

$$V_{Dsat} = \frac{(V_{GS} - V_T)\, E_c L}{(V_{GS} - V_T) + E_c L}$$



Always smaller than V_{GS}-V_T

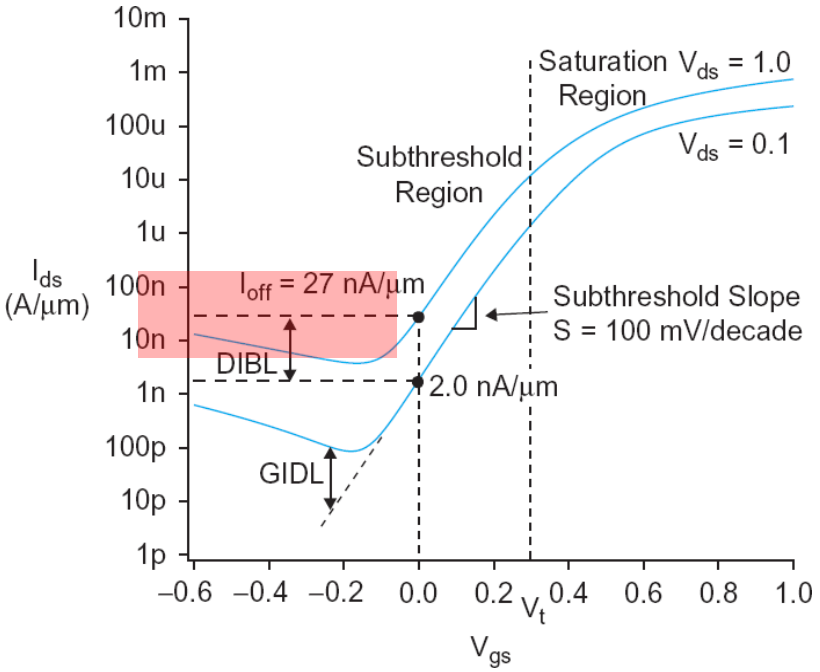
indicates early saturation

Drain Induced Barrier Lowering (DIBL)

- Electric field from drain affects channel
- More pronounced in small transistors where the drain is closer to the channel
- DIBL

– Drain voltage also affect V_t

$$V_t' = V_t - \eta V_{ds}$$



- High drain voltage causes current to increase.