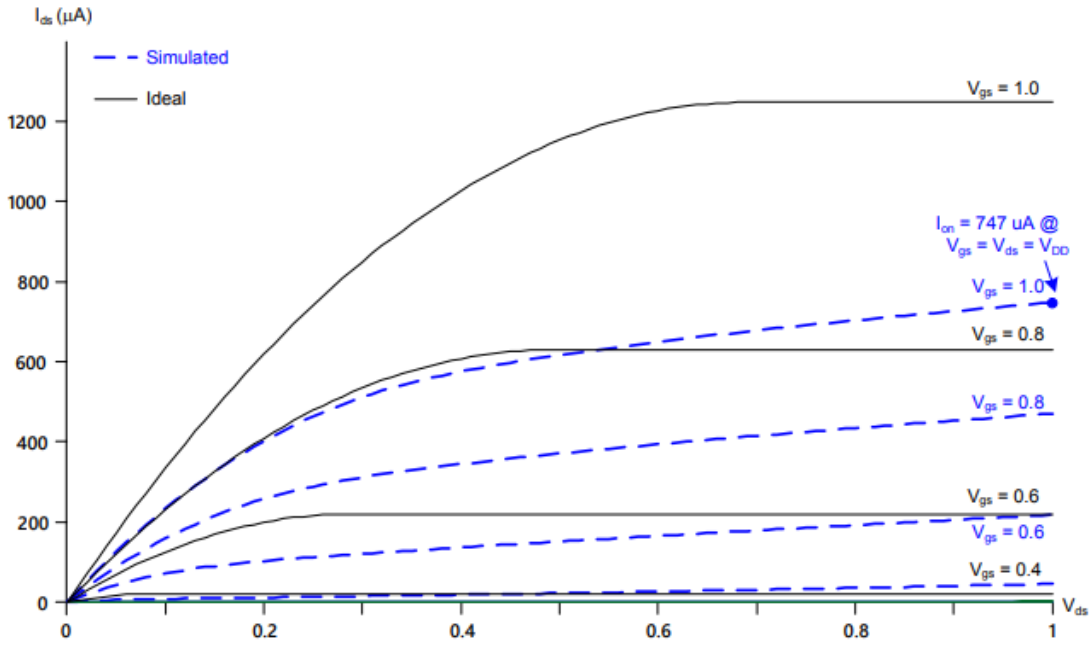
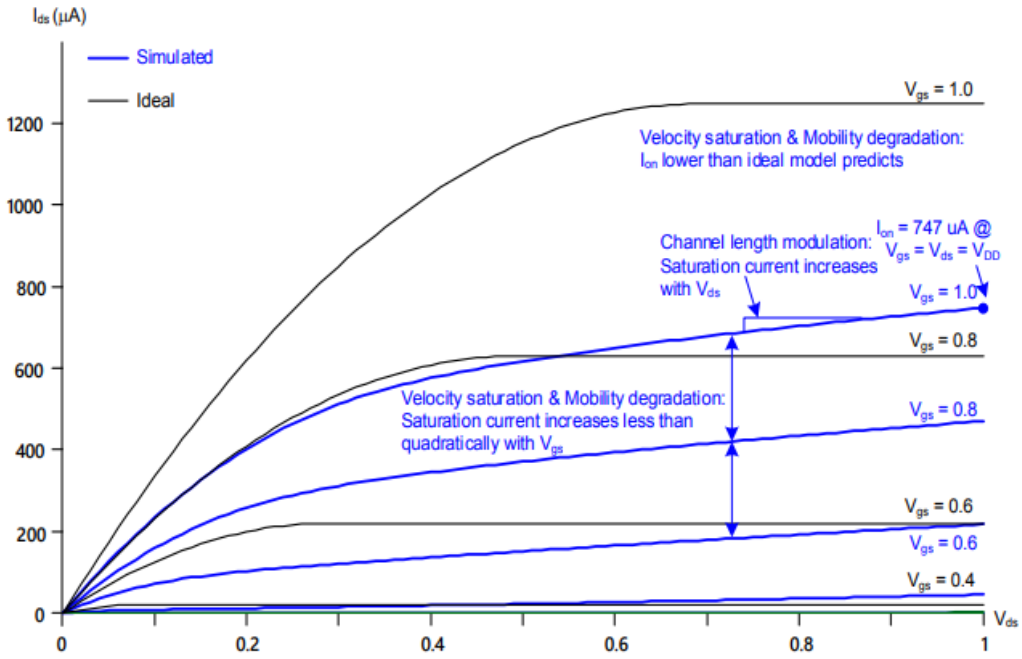
Sample Questions

1. I-V plot for an NMOS is shown below in a 65nm CMOS process with 1V of supply. The solid curve is the ideal Shockley curve, whereas the dashed curve is from simulation. Identify the non-idealities on the plot, and list the reasons for them. [3]



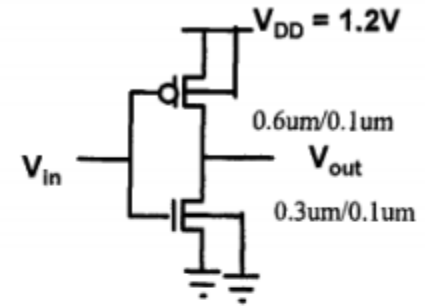


The slope in saturation region is due to the extra term $(1+\lambda V_{ds})$ in saturation current expression creating a linear dependence on V_{ds}

2. (a) (4pts) What is the effect of the changing the substrate-bias voltage, V_{SB} from 0V to 1V on the following characteristics? Answer can be: increases, decreases or no change. Use $2|\phi_F| = 0.8V$ if needed.

threshold voltage, V_T :	increases ✓	decreases ___	no change___
source junction cap., C_J :	increases___	decreases ✓	no change___
gate capacitance, C_G :	increases___	decreases ___	no change ✓
subthreshold current, I_{SUB}:	increases___	decreases ✓	no change___

3. (a) Compute the switching threshold of the inverter below and then sketch the voltage transfer characteristics.

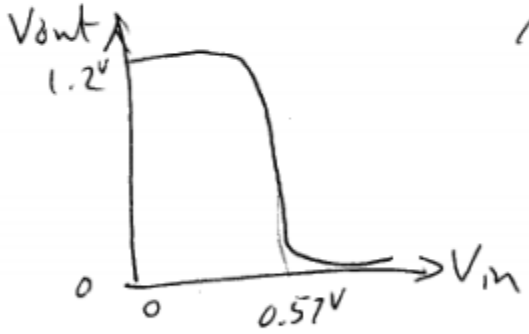


$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1+\chi}$$

$$= \frac{1.2 - 0.4 + \chi(0.4)}{1+\chi}$$

$$\chi = \sqrt{\frac{\mu_n W_n}{\mu_p W_p}} \cong 1.4$$

$$\therefore V_S \cong 0.57^V$$

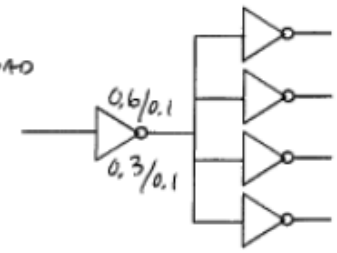


(b) (3pts) Re-design the inverter to produce a switching threshold of 0.6V.

$$0.6 = \frac{1.2 - 0.4 + 0.4\chi}{1+\chi} \quad \Rightarrow \boxed{\chi = 1}$$

(c) The inverter in part (a) drives 4 identical inverters as shown below. Compute t_{PHL} for the first inverter using simple hand calculations. **Input is a step function.**

$t = 0.69 R_{eq} C_{LOAD}$



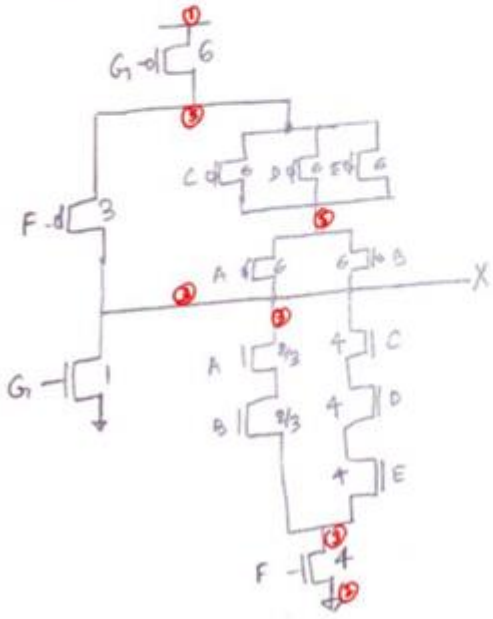
$$t_{PHL} = (0.69)\left(\frac{12.5K}{3}\right)(0.9fF + 4(2)(0.9)fF) = 23ps$$

$$t_{PLH} = (0.69)\left(\frac{30K}{6}\right)(0.9fF + 4(1.8)fF) = 28ps$$

4. Consider the logic function X =((A'+B')(C'+D'+E')+F')G', implemented using complementary CMOS.
(a) Draw the transistor level schematic.
(b) Size the transistors to produce same WC delay as standard inverter

$X = [(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})+\bar{F}]\bar{G}$

As each i/p is complemented, while the o/p is not, we can draw the transistor schematic by using the series-shunt connection of NMOS in PMOS!



Aliter: De-Morgan's law

$$X = \overline{\left[(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})+\bar{F}\right]\bar{G_1}} = \overline{(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})+\bar{F}} + G_1 = \overline{(\bar{A}+\bar{B})(\bar{C}+\bar{D}+\bar{E})}\,F + G_1$$

$$= \overline{(\bar{A}+\bar{B})}+\overline{(\bar{C}+\bar{D}+\bar{E})}\cdot F + G_1 = (AB+CDE)F + G_1$$

(c) Which input pattern(s) would give the worst and best equivalent HL or LH delay? [4*1=4]

① Worst case HL Pulldown: All paths have equal resistance ⇒ worst case charges max^{on} # of internal caps. Assume $F = G_1 = 0$ initially such that both pdn paths OFF.

$F=0$; $A=B=C=D=E=1$ (internal nodes charged to VDD); $G_1: 0 \to 1$ ⇒ charge on X and all internal nodes discharging through "G_1" transistor.

② Worst case LH Pullup: $(X: 0 \to 1)$

$F=0$; $G_1=1$; $A=B=C=D=E=1$ (all internal nodes discharged to zero); $G_1: 1 \to 0$ ⇒ G_1 must charge up internal nodes both in pu and pdn network!

③ Best case HL Pulldown $(X: 1 \to 0)$:

Make as many paths ON as possible to minimize resistance.

(G_1, A, B, C, D, E, F) all $0 \to 1$

④ Best case LH Pullup $(X: 0 \to 1)$

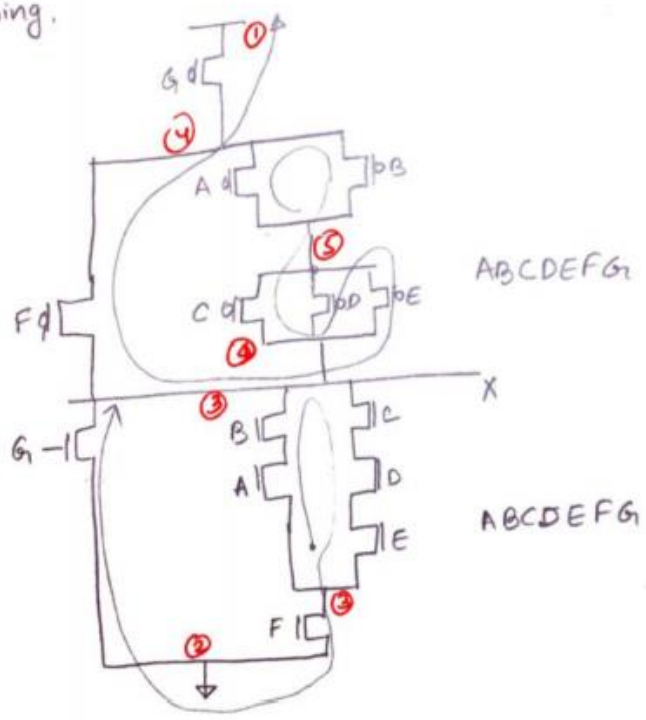
(G_1, F, C, D, E, A, B) all $1 \to 0$

(e) Sketch the layout (using stick diagrams) in minimum area (i.e. fewest diffusion breaks).
[20 (Correct layouts for NMOS & PMOS – 5 each, minimum breaks – 10)]

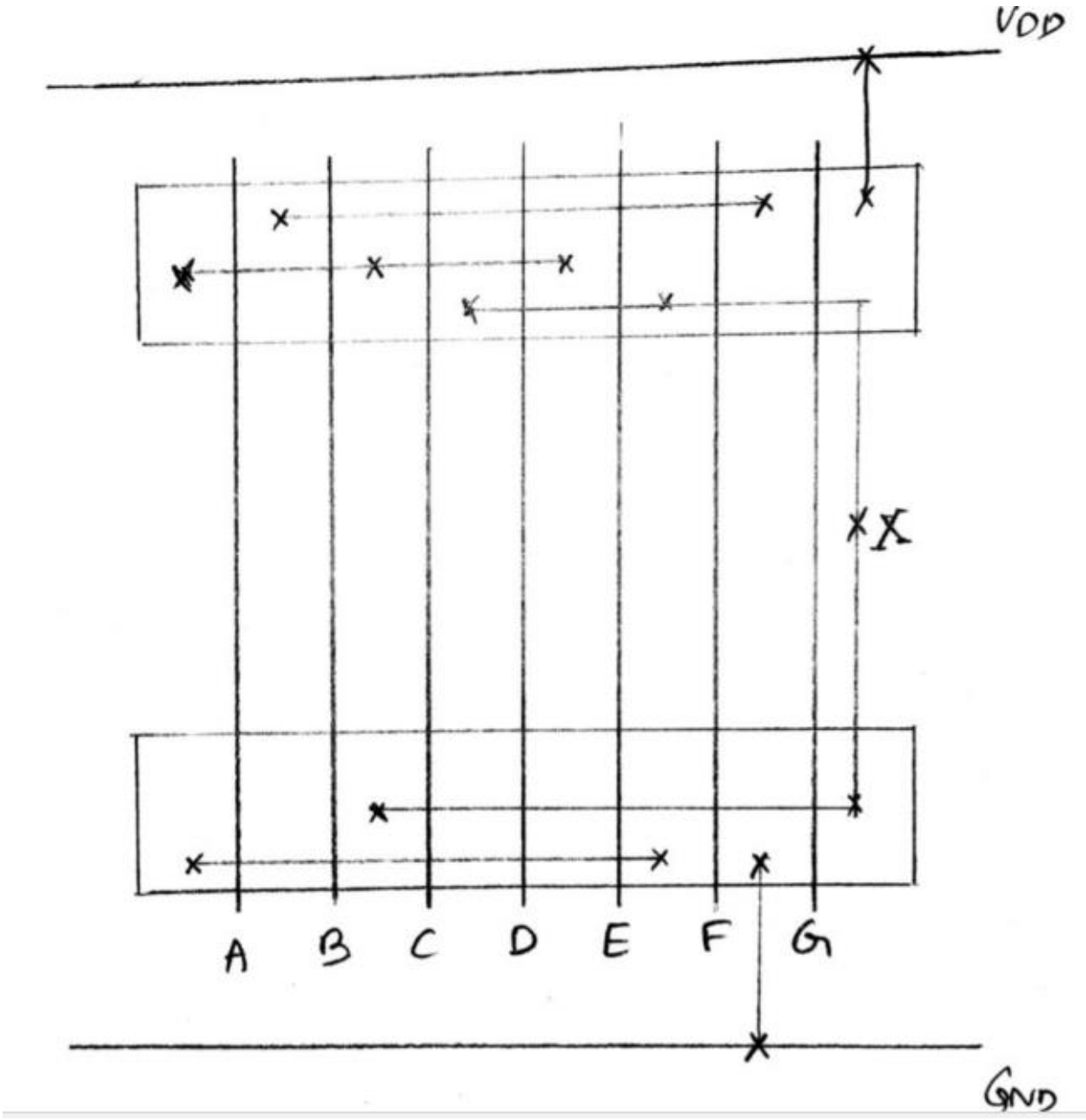
In 2(a), as shown in red, the pmos path has 4 odd nodes
⇒ will have diffusion breaks

The nmos path seems fine

Redrawing.



No diffusion break.


VDD
X
A
B
C
D
E
F
G
GND