ELEC 402 – December 5, 2021

Project 5 Report

Martin Chua – 35713411

1. Cell Library Layout; Synthesize proj1/2 verilog with 45nm, layout using Cadence Innovus. Assume 10fF load capacitance for all output simulations.

FSM Function (taken from Proj 1)

The Finite State Machine (FSM) is of a generic bank ATM for withdrawing and depositing money. The FSM is intended to be instantiated with parameter settings for CORRECT_PIN, SAVINGS_FUNDS_AMOUNT, and CHEQUING_FUNDS_AMOUNT, which are then stored locally in the instantiation following a cycle with reset high. If left default, the pin will be 1234, savings will contain 1000, and chequing will contain 25. States consist of 4 major sections with a total of 13 states:

- Initial phase (Initial startup, pin validation, and selecting deposit/withdrawals)
- Deposit phase (Account selection, depositing cash vs check, open atm deposit slot)
- Withdrawal phase (Account selection, withdraw amount, checking for insufficient funds, open atm withdrawal slot)
- End phase (Withdrawal of card)

The states are controlled based on inputs to the module and outputs allow for ATM to signal ready, open atm out (deposit), or open atm in (withdrawal). For more information on the states, see below sections.

Disclaimer: as this is a basic bank ATM FSM to demonstrate FSM rather than bank ATM functionality, there may be some differences in the bank ATM FSM function compared to ones in real life. I.e. this bank ATM FSM is not realistic.

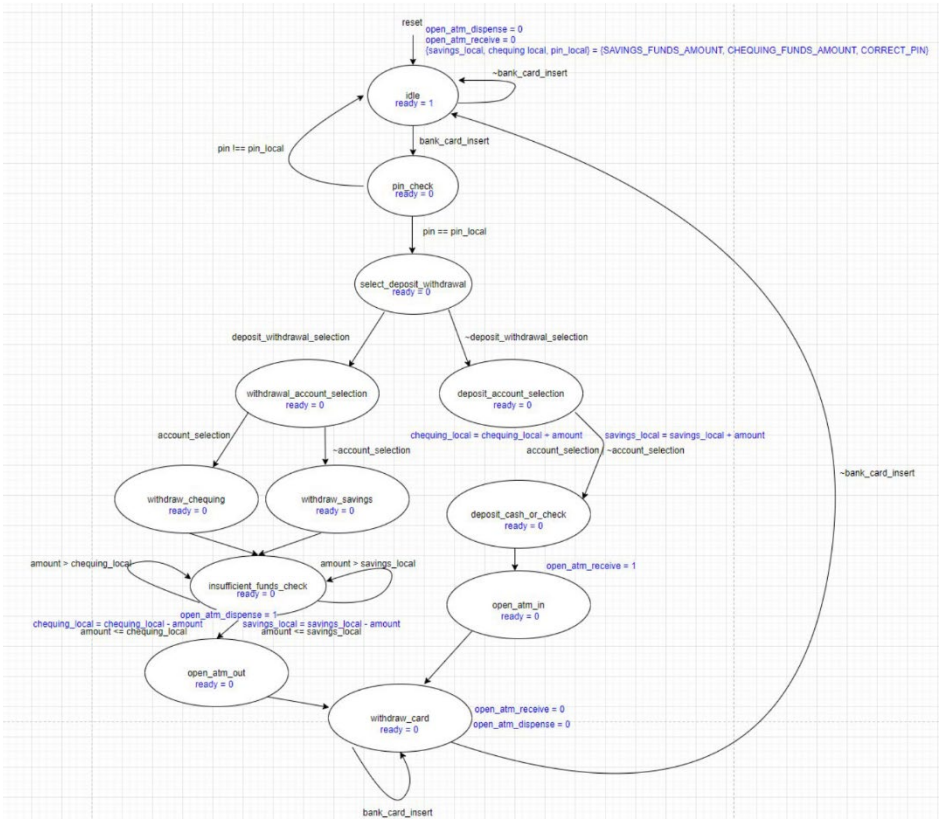


Figure 1: State Diagram

Inputs and outputs (Taken from Proj 1)

IO + FSM Modules + Testbench

Input/outputs definitions and the purpose/description of each state are below. Unless otherwise specified, inputs/outputs are one bit width in size.

Testbench is commented within the code as specified within the project documentation.

FSM Inputs

- clk ○ Basic clock to drive entire FSM module

- rst ○ Basic reset to initialize entire FSM module, and to reset it if anything happens, which resets local chequing and savings values to the instantiated parameters of the module.

- bank_card_insert ○ Signal to indicate that a bank card has been inserted, thus starting the various FSM states

- deposit_withdrawal_selection ○ Signal to select a deposit or withdrawal, indicated by 0 – Withdrawal, 1 – Deposit

- account_selection ○ Signal to select account, either 0 – Chequing, 1 – Savings

- amount[13:0] ○ Bus to indicate amount for withdrawing or depositing.

- pin[13:0] ○ Bus to indicate input pin, there is validation for correct pin vs input pin.

FSM outputs

- open_atm_out ○ Signal to open the ATM deposit out slot for dispensing cash

- open_atm_in ○ Signal to open the ATM withdrawal in slot for receiving cash or check

- ready ○ Signal to indicate that the ATM is ready to be used (and not used by another)

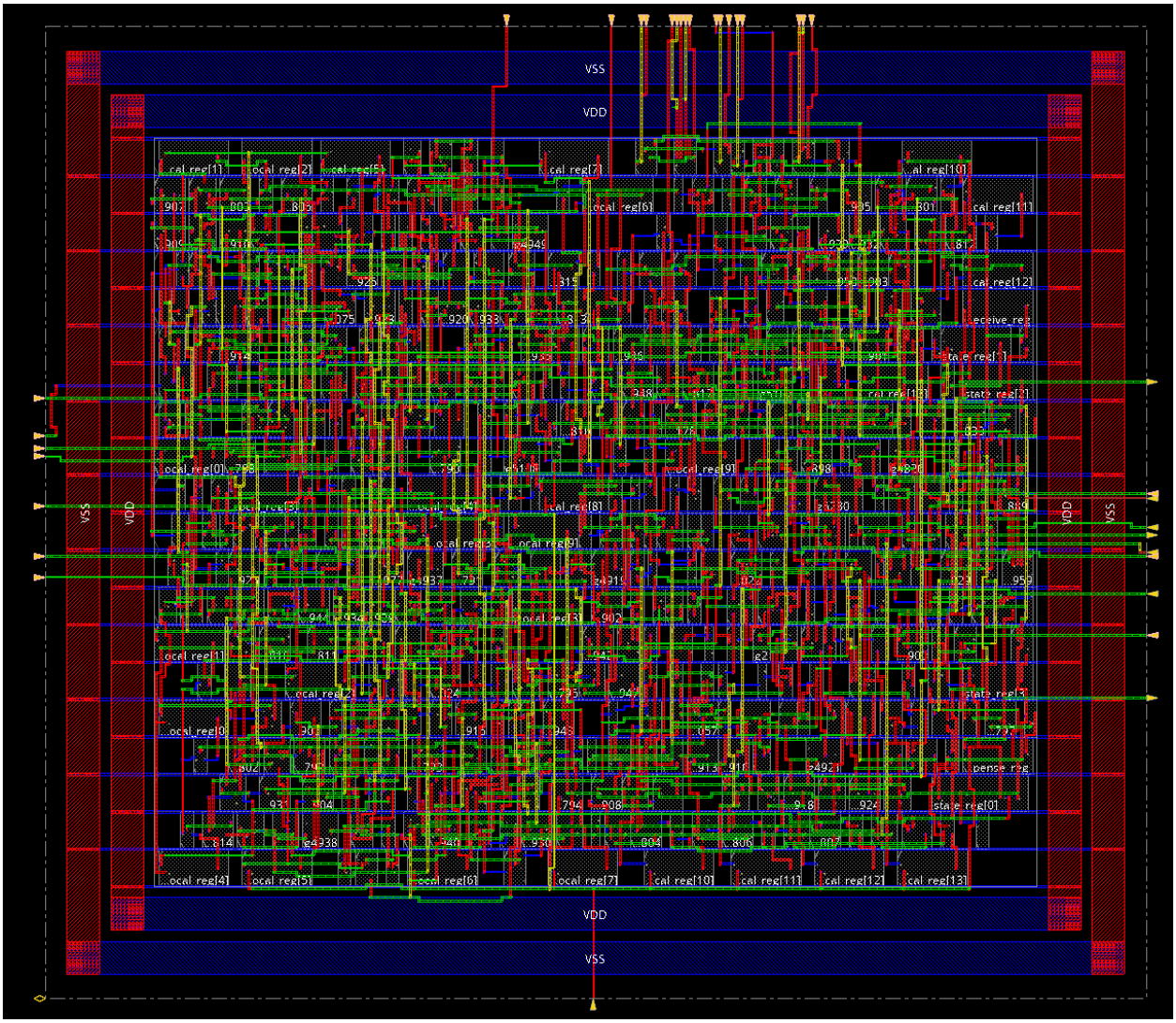


Figure 2: Innovus Place and Route for FSM

```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Sat Dec  4 17:24:27 2021

Design Name: fsm
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (50.4000, 44.4600)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Sat Dec  4 17:24:27 2021
Time Elapsed: 0:00:00.0
```

Figure 3: Verify Connectivity in Innovus (LVS equivalent)

```
innovus 1>  *** Starting Verify Geometry (MEM: 1129.5) ***

**WARN: (IMPVFG-257):   verifyGeometry command is replaced by verify_drc command. It still works in this release but
will be removed in future release. Please update your script to use the new command.
  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 1920
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 1.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.4  MEM: 171.2M)
```

Figure 4: Verify Geometry in Innovus (DRC Equivalent)

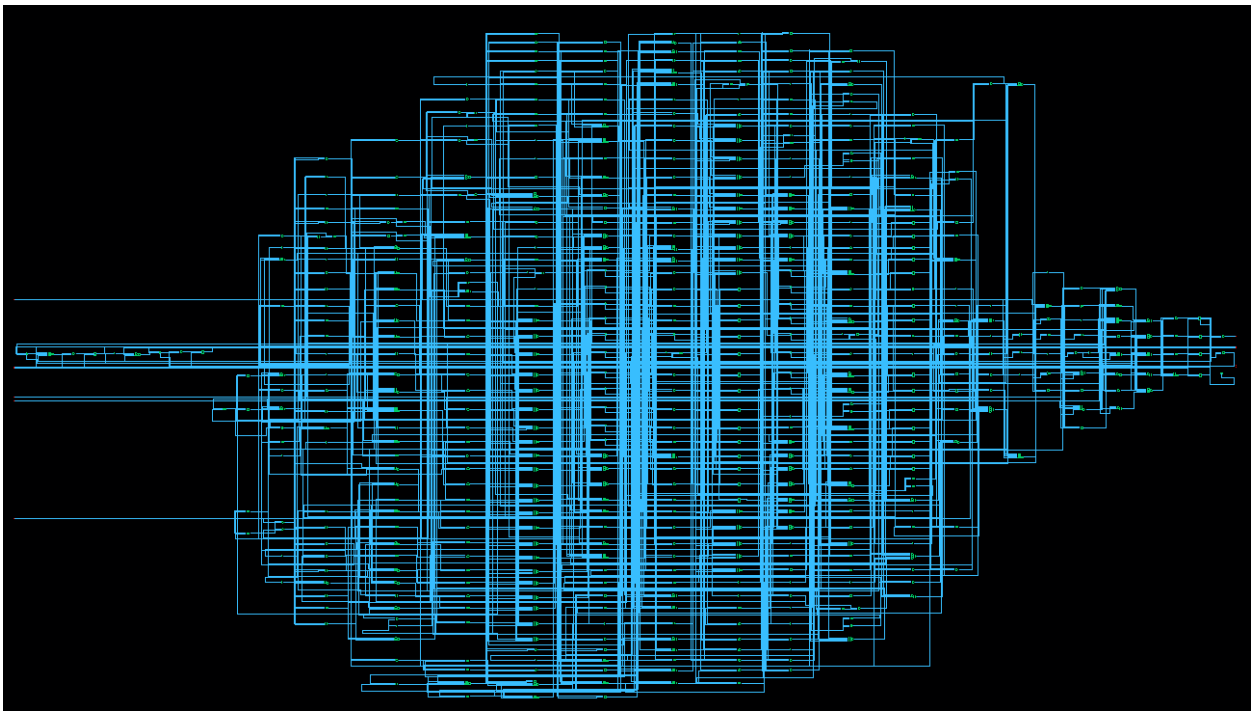


Figure 5: Generated Schematic in Virtuoso

Figure 6: FSM Symbol for schematic

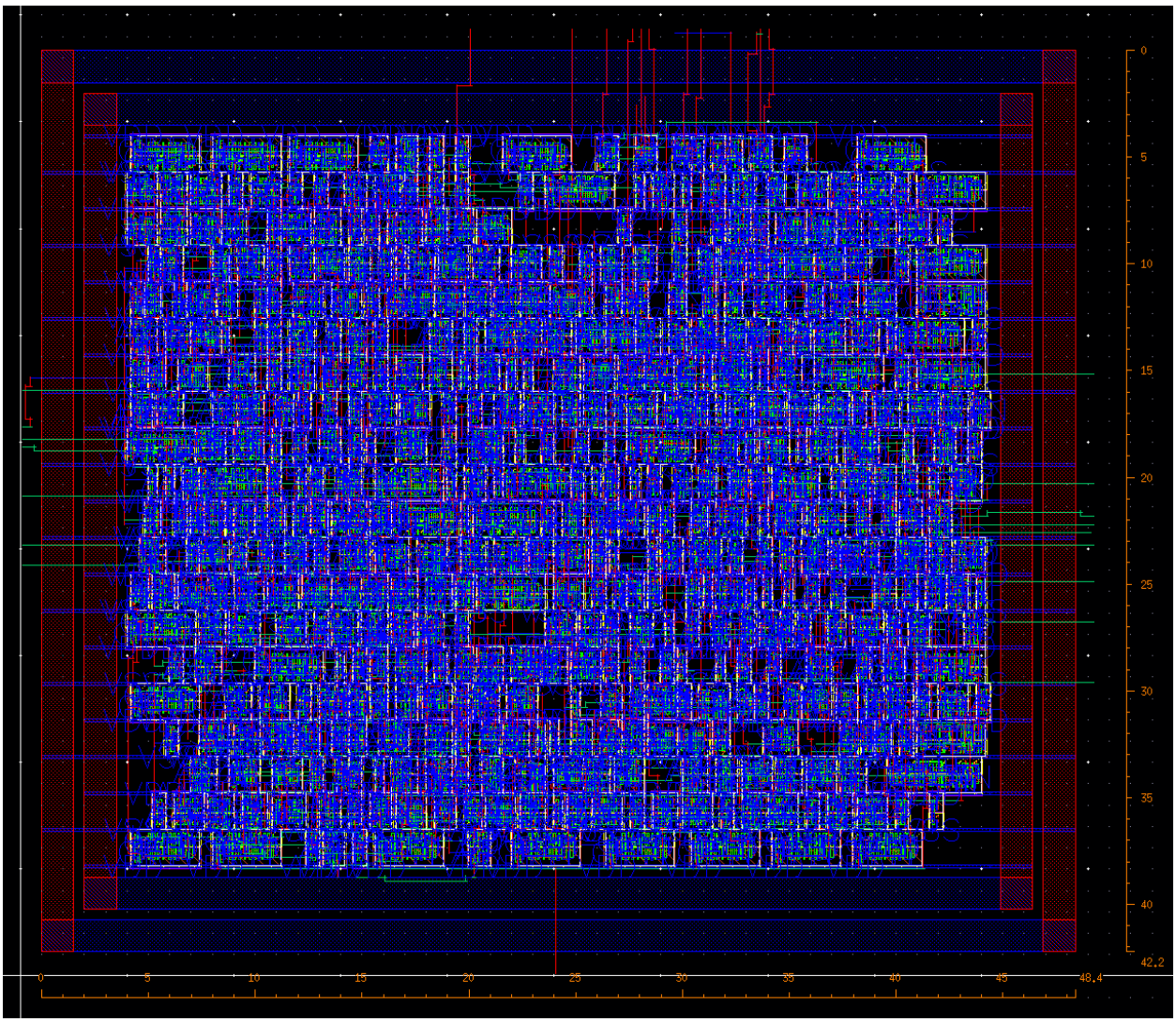


*Figure 7: Virtuoso layout w/ dimensions **48.4 by 42.2 um***

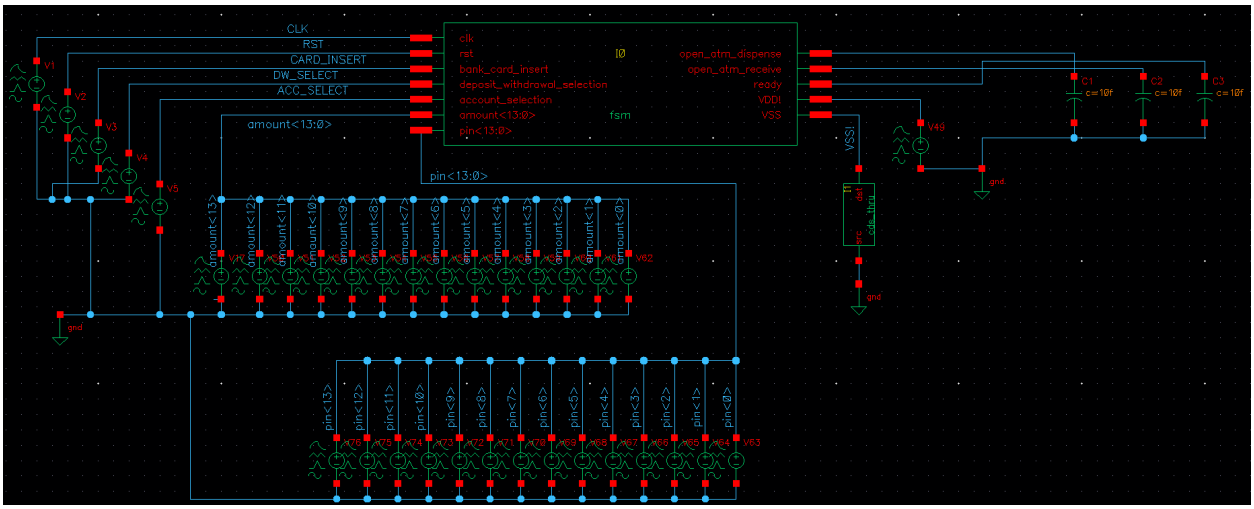


Figure 8: FSM circuit + testbench schematic

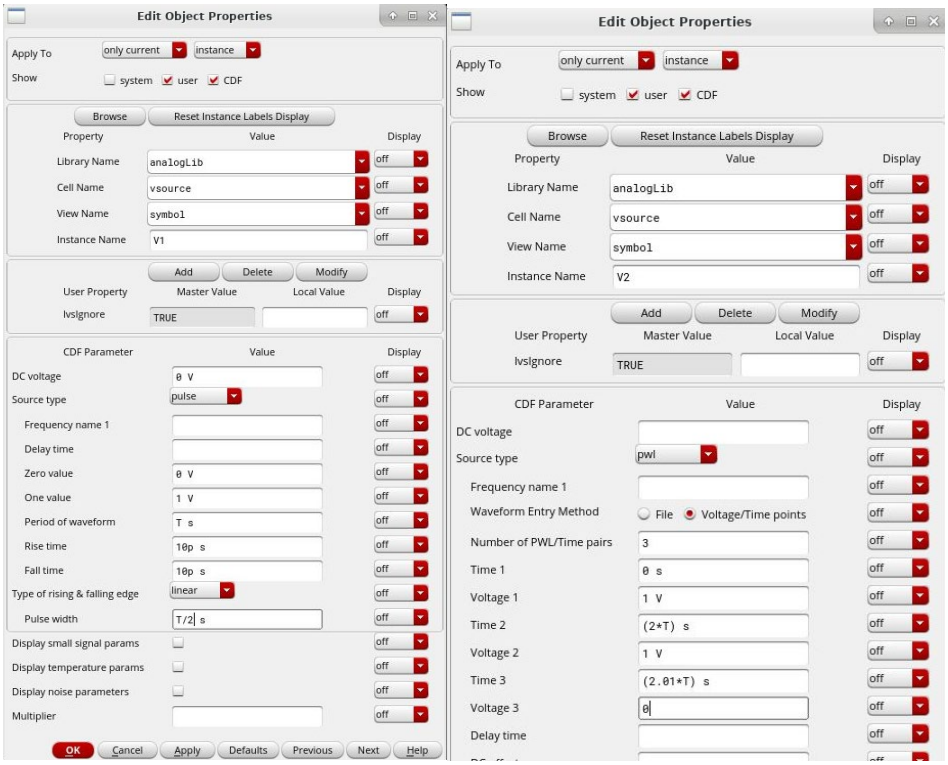


Figure 9: Object properties for (left) CLK and (right) RST

The entire testing procedure consists of:

- Assert ready for when bank card isn't inserted
- Incorrect pin test using a pin that does not match the correct pin
- Correct pin test using the correct pin for state transition
- Withdrawal selection test for selecting withdrawal or deposit
- Deposit selection tests for correct resetting and deposit account selection
- Deposit funds amount test for the correct record of funds deposited
- Withdrawal amount test for correct record of funds withdrawn

- Insufficient funds test using an amount greater than what is present in the specified account
- Withdraw card test to make sure card is withdrawn
- Test that state loops back to idle after card is withdrawn

To minimize space, only the netlist for test 1 is attached in Appendix A. Simulation time takes a while. This is due to the complexity of the circuit, as seen in Figure 7. To minimize simulation time, only certain signals are traced for each test.

For reference, project 1 and 2 waveforms are located here:
https://github.com/mchuahua/ELEC402/blob/master/Proj1/ELEC%20402%20Report.pdf

https://github.com/mchuahua/ELEC402/blob/master/Proj2/ELEC%20402%20Report.pdf

Tests that were run:

1. Test 1 is in IDLE. Ready is asserted. Card is not inserted. This is correct.

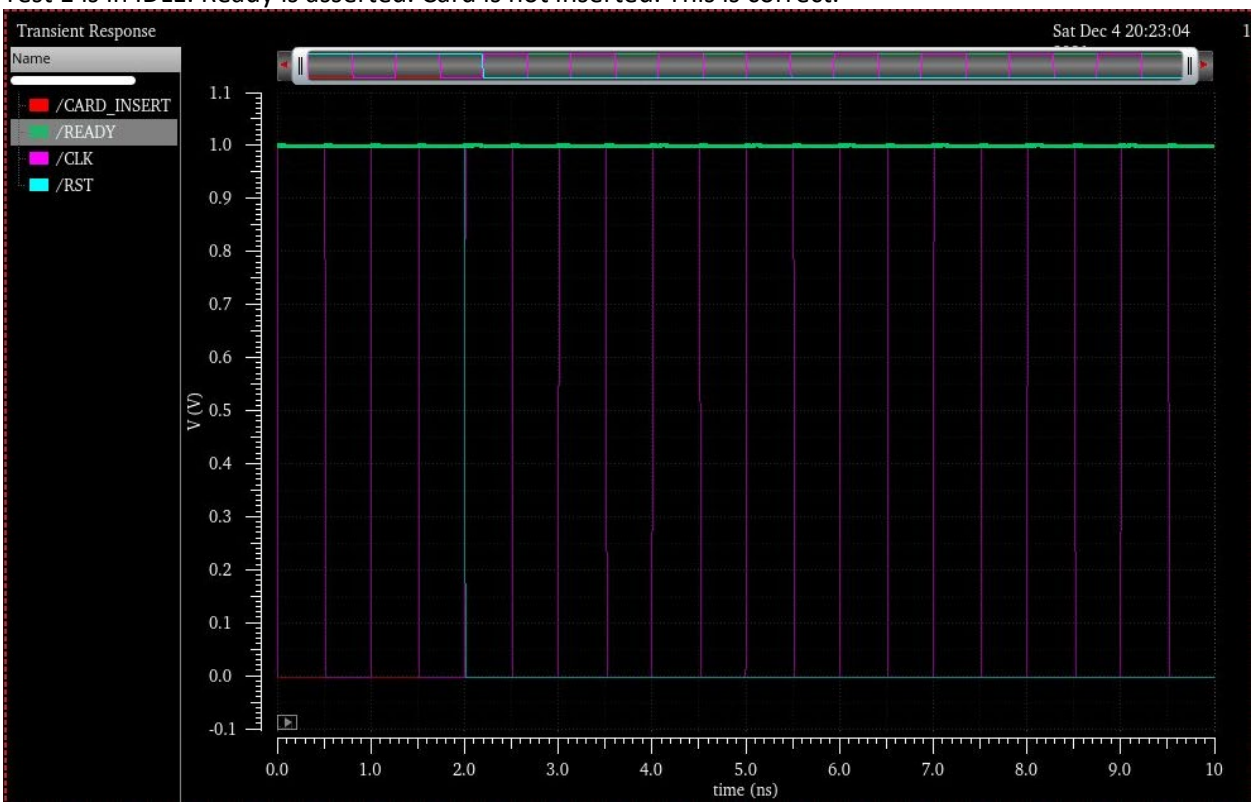


Figure 10: Test 1 (Netlist in Appendix A)

2. Test 2 sees that ready is asserted and deasserted when card is inserted, as it transitions back and forth due to invalid PIN (0). This is correct.

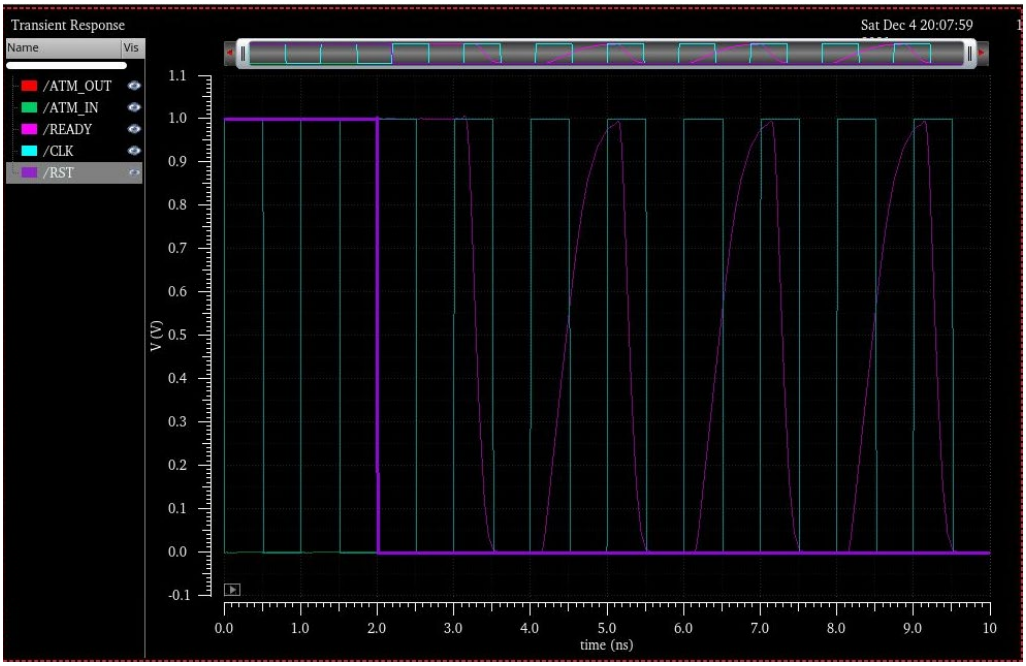


Figure 11: Test 2

3. Test 3 sees that after a valid PIN (14’d1234, 14’b010011010010) and card inserted, state should not be in IDLE. This is correct. If it wasn’t the ready signal should be asserted just as in test_num 1.

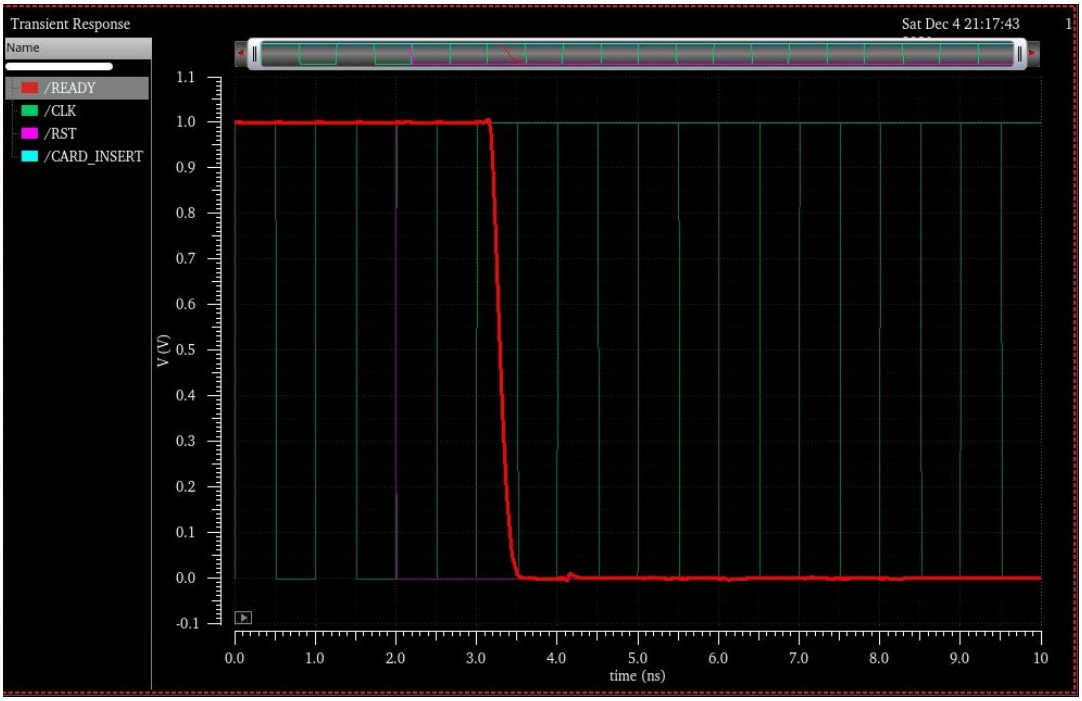


Figure 12: Test 3

4. Test 4 checks to see if deposited correct. Deposit is selected so ATM IN should be on. Notice the open atm in is being correctly triggered. This is correct.

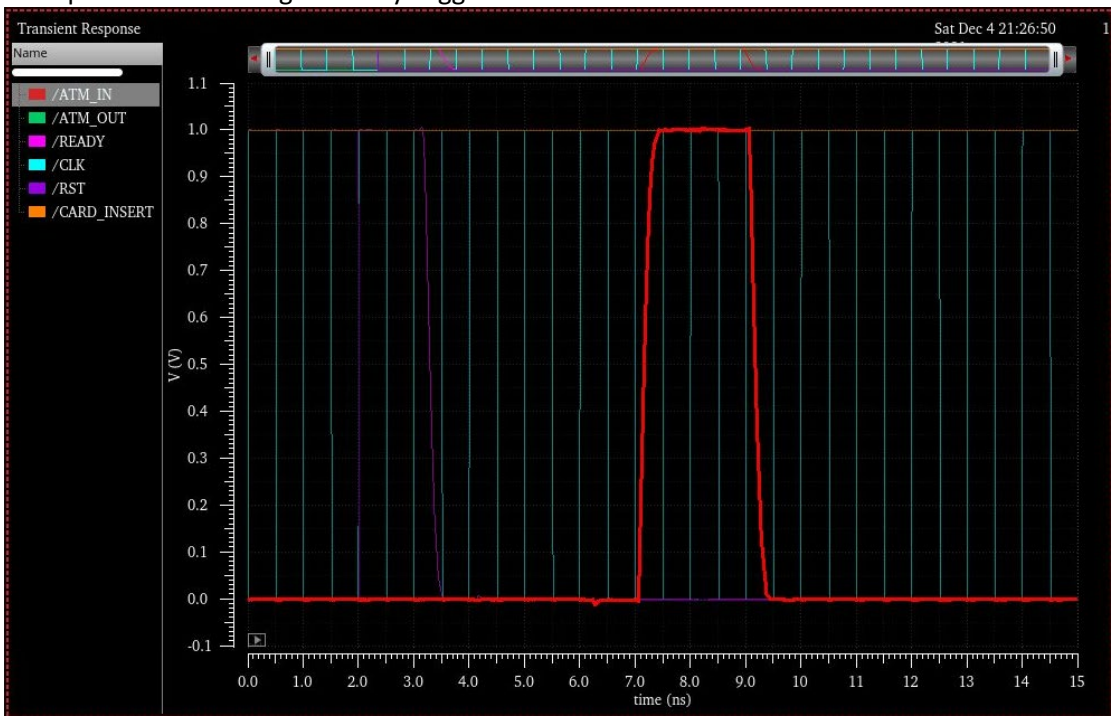


Figure 13: Test 4

5. Test 5 checks to see if deposit was correct. Withdrawal is selected and so ATM OUT should be triggered. This is correct.

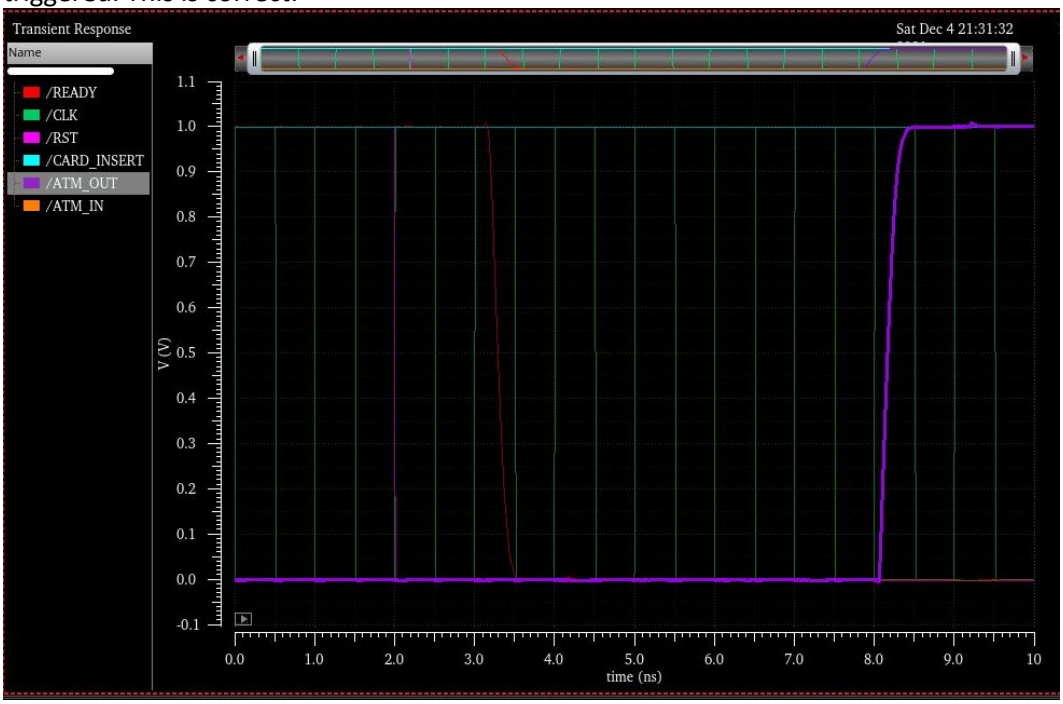


Figure 14: Test 5

6. The next test can be understood by understanding the state functionality. When selecting withdrawal, and when the withdrawal amount is changed to a number higher than 14'd1000 (amount in bank), i.e. {1'b1, 13'b0}, this should trigger an indefinite loop, as there are insufficient funds. We can see this by going to over 15ns as each state will be one cycle so it's doing nothing. This is correct.

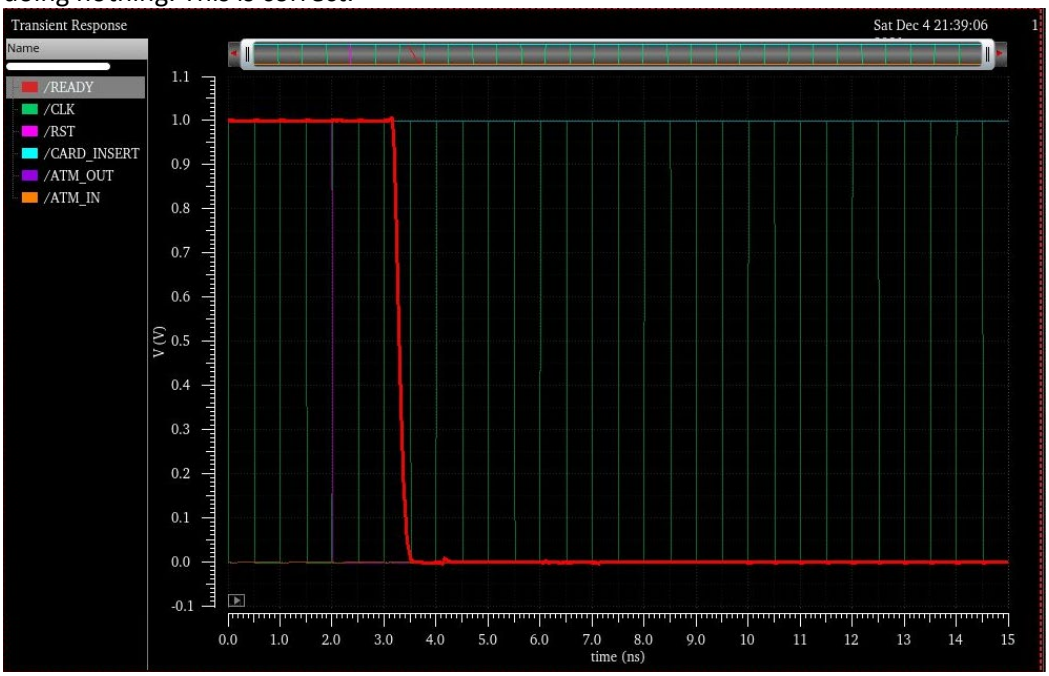


Figure 15: Test 6

7. Now if we change the input amount back to 1 and restart, the states should continue along and if bank card is withdrawn, we should see ready being asserted, completing an entire loop. This is correct.

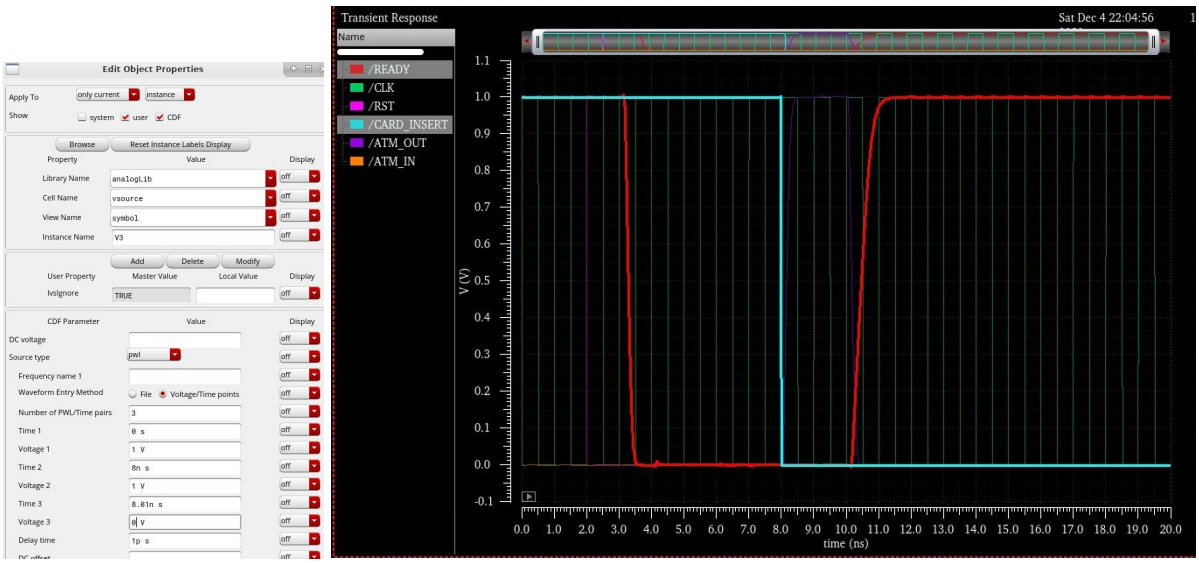
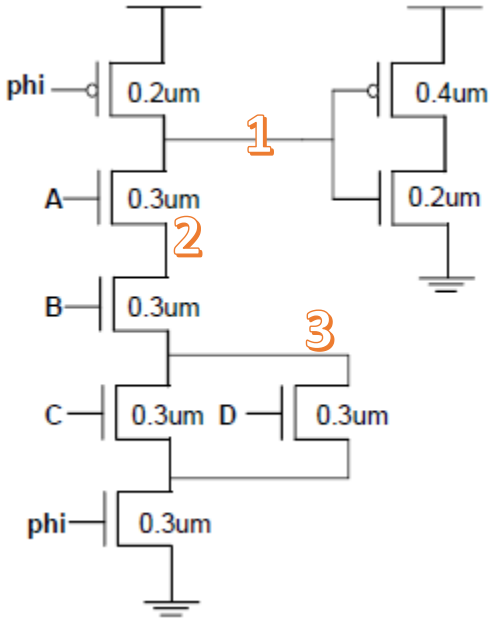


Figure 16: Card insert properties (left) Test 7 (right)

2. Domino Logic (12 points)

1. (a) Determine the logic function OUT (3 points)
2. (b) Determine the reduction in voltage at the input of the inverter under the worst case charge sharing condition. C_{eff} = 1fF/um and C_g = 2 fF/um technology. (9 points)



a) By domino logic we see PMOS and NMOS with phi as input clock. OUT can be defined as the output of the output inverter. We can see the pull down NMOS consisting of A+B+CD, as AB are series with CD parallel. Since this is the dual, the resulting logic is OUT = AB(C+D)

b) Voltage reduction. Worst case charge sharing requires the combination of ABCD = 1100. Then, to calculate capacitance we can do nodal calculations. For node 1, we have Ceff of phi PMOS, A NMOS, and Cgate of inverter input. This gives us $C_1 = C_{eff}W_{phi} + C_{eff}W_A + C_g(W_p+W_n)$ = 1.7 fF. For node 2, we have $C_2 = C_{eff}W_B$ = 0.3 fF. For node 3 we have $C_3 = C_{eff}(W_c + W_d)$ = 0.6 fF.

Now that we have all three node capacitances, we can calculate V*, the resulting voltage across all these nodes that share charge. BCD are charged when AB are 1. Therefore, the equation we use is $V^* = C_{out} * V_{DD} / (C_x + C_{out})$, where C_x is $C_2 + C_3$ and $C_{out} = C_1$. We assume output is sitting at 1.2V. So V* = 1.7 * 1.2 / (0.6 + 1.7 + 0.3) = 0.785 V.

However this voltage is not possible at node 3 as $V_{max} = V_{DD} - 2V_{tn}$ = 0.4V. We can find voltage at node 3 using $Q_{final} = Q_{3og} - (Q_1 + Q_2)$, where $Q_{final} = 1.7 * V_{final}$, $Q_{3og} = 1.7 * 1.2$, $Q_1 + Q_2 = C_1 * (V_{DD} - V_T) + C_2 * (V_{DD}-2V_T) = 0.3*0.8 + 0.6*0.4$. So, V_{final} = 0.9176 V.

Thus, $V_{reduction} = V_{DD} - V_{final}$ = 1.2 – 0.912 = 0.3 V

3. In the circuit of Figure **4** , determine the capacitance of each node and calculate the minimum and maximum delay. (All transistors are minimum size, $L = 2\lambda$ and $W = 2\lambda$, unless otherwise specified.)

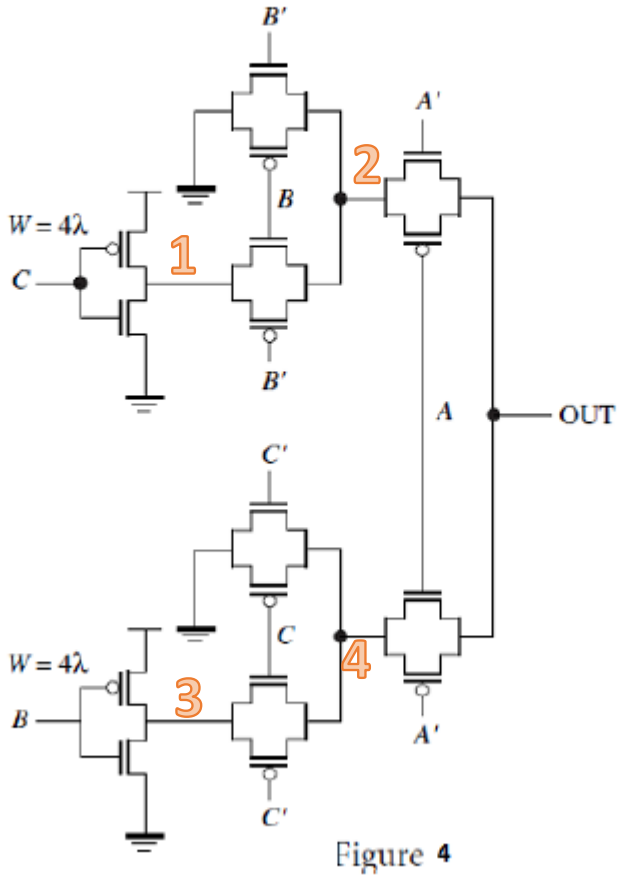
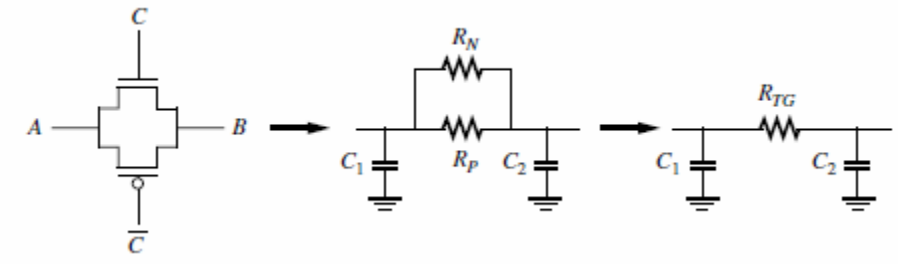


Figure **4**

(14 points)



This is a transmission gate (tg) question. Assume R is the NMOS transistor equivalent resistance = 45nm, 34kohm. C_{eff} = 1fF/um, C_g = 2fF/um.

Here we first denote 5 nodes as seen in the diagram above (incl OUT). From observing the circuit, we can equate node 1 = node 3 and node 2 = node 4.

First we look at node 1/3. We see self capacitance of the inverter PMOS/NMOS + tg, and gate capacitance of tg. So, $C_1 = C_3 = C_{eff}(W + 2W) + C_{eff}W + C_gW = 5C_{eff}W + C_gW$

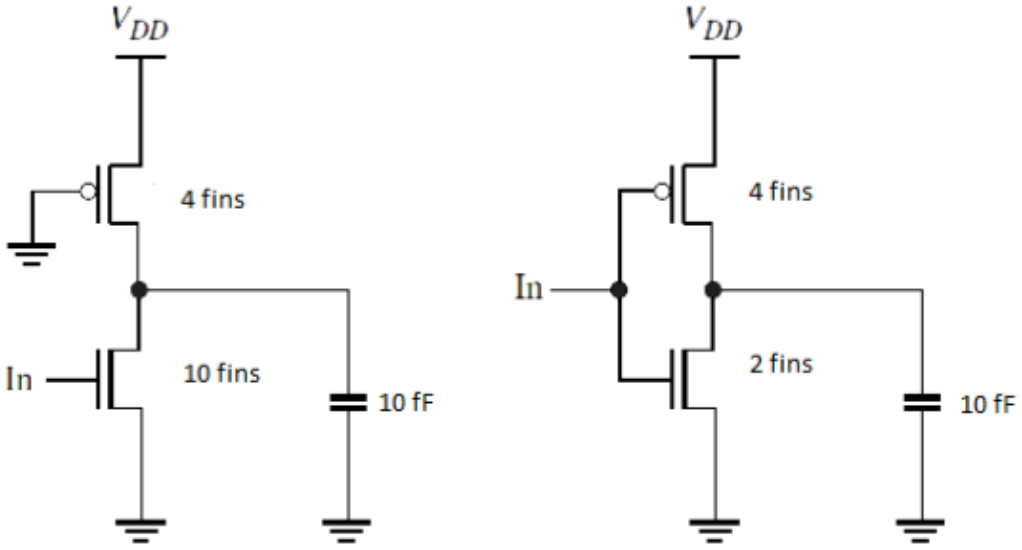
Second we look at node 2/4. We see self and gate capacitance of the 2 tg on left and 1 tg on right. So, $C_2 = C_4 = 3(2C_{eff}W + C_gW) = 6C_{eff}W + 3C_gW$

Lastly we look at OUT. We see self and gate capacitance of the 2 tg on left. So, $C_{OUT} = 4C_{eff}W + 2C_gW$

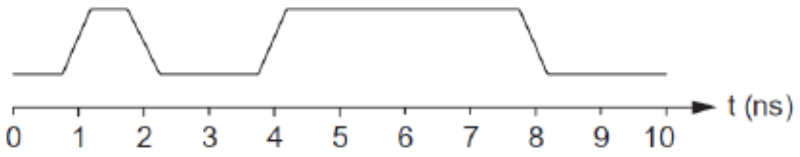
For minimum delay we go from ground at top tg (input 0 of B) to OUT. So this passes only through node 2 and OUT, $T_{min} = C_2R + 2C_{OUT}R = R(6C_{eff}W + 3C_gW) + 2R(4C_{eff}W + 2C_gW) = RW(14C_{eff} + 17C_g) = 34k * (14 + 17*2) = 1.632$ ns

For maximum delay we go from C to OUT. So this passes through both node 1 and 2 and OUT, $T_{max} = C_1R + 2C_2R + 3RC_{OUT} = R(5C_{eff}W + C_gW) + 2R(6C_{eff}W + 3C_gW) + 3R(4C_{eff}W + 2C_gW) = RW(29C_{eff} + 13C_g) = 34k (29 + 13*2) = 1.87$ ns

4) (**Power consumption**) Analytically estimate the static (only for left circuit) and dynamic power consumption of the two inverters below (**8 points**) and compare your analytical results with that of simulation (**8 points**). Sketch VTC and show on the graph in which region we have power due to DC current, subthreshold current and short circuit current (**4 points**). Use 15 nm simulations and use an input frequency of 100 MHz for calculation/simulation. 10 fF is an explicit capacitor at the output of inverters.



2 Determine the activity factor for the signal shown The clock rate is 1GHz.



2*lambda = 1 fin.

Static power: $P_{DC} = I_{DC}V_{DD}$.

$$I_{DC} = \frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1+\frac{V_{OL}}{E_{CN}L_N}\right)}\left[(V_{DD}-V_{TN})(V_{OL}) - \frac{(V_{OL})^2}{2}\right]$$

I_{DC} = … skipped.

Simulation: skipped

Sketch: skipped

Activity Factor. 1Ghz = 1ns period = 10 clock cycles. Toggles (transition from high to low and low to high) at output = 4. Two toggles are required for power dissipation. So, activity factor = # of toggles / 2 / # of clock cycles = 4 / 2 / 10 = 1/5 = 20%

6. (15 points) Interconnects

Consider an 18 mm Metal 7 wire in a 40 nm technology. Assume the wire is 0.4 μm wide and 0.8 μm thick with a spacing to adjacent wires of 2 μm. The height above and below to Metal 8 and Metal 6 is 0.5 μm. Assume Cu for interconnect ($\rho = 0.017\ \Omega$-μm) and a low-k dielectric material ($\epsilon_r = 3.0$). Assume a worst-case coverage of Metal 6 below, Metal 8 above, and Metal 7 for adjacent lines that are shielding the wire of interest.

(a) Compute the resistance per unit length and capacitance per unit length for this wire.

(b) Estimate the delay of the distributed *RC* wire, assuming that the driver is a perfect voltage source and that the load capacitance is 50 fF.

(c) Assume that the wire is being driven by a 25X inverter. What is the new delay?

To get resistance per unit length we can use the following formula: $R = \frac{\rho L}{A} = \frac{\rho L}{TW}$

R = (0.017 ohm-um) * (0.8um) / (0.4 um * 0.5 um) = 0.068 ohm / um

For capacitance per unit length we need to first get each specific capacitance (area/lateral/fringe).

$C_{area} = E_{ox} * W / H = 3 * 88.5E\text{-}4$ fF/um * 0.4/0.5 = 0.02124 fF/um

$C_{lat} = E_{ox} * T/S = 3 * 88.5E\text{-}4$ fF/um * 0.8/2 = 0.01062 fF/um

$C_{fringe} = E_{ox} * \ln(1 + T/H) = 3 * 88.5E\text{-}4$ fF/um * ln(1 + 0.8/0.5) = 0.02537 fF/um

To get total capacitance we multiply by two because of top and bottom and sum them altogether. Both fringe and lateral capacitances are considered (although lateral can be disregarded as it is smaller):

$C_{int} = 2(C_{area} + C_{lat} + C_{fringe}) = 0.11446$ fF/um

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For delay, assuming 40nm -> 45nm, R_{eqn} = 34kohm. W = 0.1um. Assuming ramp input.

To get the wire resistance and capacitance we can simply multiply R/C per unit length by length:

$R_{wire} = R * 18mm = 0.068$ ohm/um * 18000um = 1224 ohm

C_{wire} = C * 18mm = 0.11446 fF/um * 18000um = 2060.28 fF = 2.06 pF

To get R for 25x we divide, and to get C we multiply:

$R_{eff25} = R_{eqn}/25$ = 12.5kohm/25 = 500 ohm

$C_{self25} = C_{eff}(2W + W)25$ = 1 fF/um * 0.6um * 25 = 15 fF

C_{load} = 50 fF

Thus, we get the following delay calculations:

T_{elmore} = 34kohm * L/W * C_{load} = 34kohm * ½ * 50fF = 0.85 ns

$T_{elmore25}$ = (500ohm)(2.06pF) + (500 + 1224 ohm)(2.06pF) = 4.58 ns

Notes:

- For T_elmore, wire resistance can be ignored
- For T_elmore25, C_self and C_load are small and can be ignored.

Appendix A: Netlist (Test 1)

```
// Generated for: spectre
// Generated on: Dec  4 20:21:48 2021
// Design library name: fsm_tb
// Design cell name: fsm_tb
// Design view name: schematic
simulator lang=spectre
global 0 VDD! VSS!
parameters T=1n
include
"/ubc/ece/data/cmc2/kits/GPDK45/gpdk045_v_5_0/gpdk045/../models/spectre/gpdk045.scs"
section=mc

// Library name: gsclib045
// Cell name: NAND2X1
// View name: schematic
subckt NAND2X1 A B Y inh_VDD inh_VSS
   mn1 (Y B n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp1 (Y B inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (Y A inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends NAND2X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NOR2X1
// View name: schematic
subckt NOR2X1 A B Y inh_VDD inh_VSS
   mn1 (Y B inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (Y A inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp1 (Y B net41 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (net41 A inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends NOR2X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI221X1
// View name: schematic
subckt OAI221X1 A0 A1 B0 B1 C0 Y inh_VDD inh_VSS
   mn4 (Y C0 net132 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (net128 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn1 (net128 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (net132 B0 net128 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn3 (net132 B1 net128 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp3 (Y B1 net123 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (net115 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (Y A1 net115 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp2 (net123 B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp4 (Y C0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI221X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: DFFHQX1
// View name: schematic
subckt DFFHQX1 CK D Q inh_VDD inh_VSS
   mn26 (n20 CKb n21 inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn25 (n21 D inh_VSS inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn55 (Q qbint inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn50 (net172 qbint inh_VSS inh_VSS) g45n1svt w=(205n) l=45n nf=1 \
      as=28.7f ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m \
      sa=140n sb=140n sd=160n sca=166.60249 scb=0.10864 scc=0.02069 \
      m=(1)
   mn51 (n30 CKb net172 inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn30 (mout n20 inh_VSS inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn36 (n20 CKbb net192 inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn20 (CKb CK inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn45 (qbint n30 inh_VSS inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn40 (mout CKbb n30 inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
      ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
      sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
   mn21 (CKbb CKb inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn35 (net192 mout inh_VSS inh_VSS) g45n1svt w=(205n) l=45n nf=1 \
      as=28.7f ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m \
      sa=140n sb=140n sd=160n sca=166.60249 scb=0.10864 scc=0.02069 \
      m=(1)
   mp26 (n20 CKbb n22 inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp25 (n22 D inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp51 (n30 CKbb net123 inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp50 (net123 qbint inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 \
      as=43.4f ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m \
      sa=140n sb=140n sd=160n sca=130.90642 scb=0.09728 scc=0.01590 \
      m=(1)
   mp55 (Q qbint inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp35 (net147 mout inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 \
      as=43.4f ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m \
      sa=140n sb=140n sd=160n sca=130.90642 scb=0.09728 scc=0.01590 \
      m=(1)
   mp36 (n20 CKb net147 inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp45 (qbint n30 inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp20 (CKb CK inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp40 (mout CKb n30 inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp30 (mout n20 inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
      ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
      sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
   mp21 (CKbb CKb inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends DFFHQX1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI22XL
// View name: schematic
subckt AOI22XL A0 A1 B0 B1 Y inh_VDD inh_VSS
   mn3 (Y B1 net98 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (net106 A0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (net98 B0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (Y A1 net106 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp3 (Y B1 net89 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (net89 A0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
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    mp1 (net89 A1 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (Y B0 net89 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AOI22XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI21XL
// View name: schematic
subckt OAI21XL A0 A1 B0 Y inh_VDD inh_VSS
    mn2 (Y B0 n0 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn1 (n0 A1 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (n0 A0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp0 (n1 A0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (Y B0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp1 (Y A1 n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OAI21XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: XNOR2X1
// View name: schematic
subckt XNOR2X1 A B Y inh_VDD inh_VSS
    mn1 (n2 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn2 (net145 n1 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn3 (n0 n2 net145 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn5 (Y n0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (n1 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn4 (n0 B n1 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp4 (n1 n2 n0 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (net112 n1 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp1 (n2 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp3 (n0 B net112 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp5 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends XNOR2X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: INVX1
// View name: schematic
subckt INVX1 A Y inh_VDD inh_VSS
    mp0 (Y A inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mn0 (Y A inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
ends INVX1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: MX2XL
// View name: schematic
subckt MX2XL A B S0 Y inh_VDD inh_VSS
    mn3 (n5 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn4 (n0 S0 n5 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (S0b S0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn1 (n3 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn5 (Y n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn2 (n0 S0b n3 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp4 (n0 S0b n6 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp3 (n6 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp5 (Y n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp0 (S0b S0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (n0 S0 n4 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp1 (n4 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends MX2XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI21X1
// View name: schematic
subckt OAI21X1 A0 A1 B0 Y inh_VDD inh_VSS
    mn2 (Y B0 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn1 (n0 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (n0 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp0 (n1 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp2 (Y B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp1 (Y A1 n1 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI21X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NAND2BX1
// View name: schematic
subckt NAND2BX1 AN B Y inh_VDD inh_VSS
    mn2 (Y B n1 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (n0 AN inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn1 (n1 n0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp1 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp2 (Y B inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (n0 AN inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends NAND2BX1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI221X1
// View name: schematic
subckt AOI221X1 A0 A1 B0 B1 C0 Y inh_VDD inh_VSS
    mn2 (net120 B0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn3 (Y B1 net120 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn4 (Y C0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
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    mn1 (Y A1 net128 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (net128 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp3 (net108 B1 net111 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp2 (net108 B0 net111 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (net111 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp1 (net111 A1 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp4 (Y C0 net108 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends AOI221X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI2BB1XL
// View name: schematic
subckt AOI2BB1XL A0N A1N B0 Y inh_VDD inh_VSS
    mn2 (Y B0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn1 (net100 A1N inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn3 (Y net100 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (net100 A0N inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp3 (Y net100 net79 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (net79 B0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp1 (net100 A1N net87 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp0 (net87 A0N inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AOI2BB1XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OA21X1
// View name: schematic
subckt OA21X1 A0 A1 B0 Y inh_VDD inh_VSS
    mn1 (net107 A1 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (net107 A0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn3 (Y net95 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn2 (net95 B0 net107 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp1 (net95 A1 net98 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp0 (net98 A0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp3 (Y net95 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp2 (net95 B0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OA21X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI31X1
// View name: schematic
subckt OAI31X1 A0 A1 A2 B0 Y inh_VDD inh_VSS
    mn3 (Y B0 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (n0 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn2 (n0 A2 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn1 (n0 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp2 (Y A2 n2 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp1 (n2 A1 n1 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp3 (Y B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (n1 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI31X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI22X1
// View name: schematic
subckt AOI22X1 A0 A1 B0 B1 Y inh_VDD inh_VSS
    mn3 (Y B1 net98 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (net102 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn2 (net98 B0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn1 (Y A1 net102 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp3 (Y B1 net89 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (net89 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp1 (net89 A1 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp2 (Y B0 net89 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends AOI22X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OR2XL
// View name: schematic
subckt OR2XL A B Y inh_VDD inh_VSS
    mn2 (Y n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn1 (n0 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp1 (n0 B n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (Y n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OR2XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NOR2BX1
// View name: schematic
subckt NOR2BX1 AN B Y inh_VDD inh_VSS
    mn1 (Y net76 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn2 (Y B inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (net76 AN inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp2 (Y B net59 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp1 (net59 net76 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 \
      as=54.6f ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m \
      sa=140n sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 \
      m=(1)
    mp0 (net76 AN inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
```

```
ends NOR2BX1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AND2X1
// View name: schematic
subckt AND2X1 A B Y inh_VDD inh_VSS
   mn2 (Y n0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (net127 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n0 A net127 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp1 (n0 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n0 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends AND2X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI21XL
// View name: schematic
subckt AOI21XL A0 A1 B0 Y inh_VDD inh_VSS
   mn2 (Y B0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (net74 A0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (Y A1 net74 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp2 (Y B0 net70 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp1 (net70 A1 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (net70 A0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AOI21XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI2BB1X1
// View name: schematic
subckt OAI2BB1X1 A0N A1N B0 Y inh_VDD inh_VSS
   mn3 (Y n0 n2 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (n2 B0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (n1 A0N inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n0 A1N n1 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp2 (Y B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (n0 A1N inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n0 A0N inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp3 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI2BB1X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI31X1
// View name: schematic
subckt AOI31X1 A0 A1 A2 B0 Y inh_VDD inh_VSS
   mn3 (Y B0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn1 (net97 A1 net93 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (Y A2 net97 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (net93 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp2 (net81 A2 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp3 (Y B0 net81 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (net81 A1 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (net81 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends AOI31X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI21X1
// View name: schematic
subckt AOI21X1 A0 A1 B0 Y inh_VDD inh_VSS
   mn2 (Y B0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (net78 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn1 (Y A1 net78 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp2 (Y B0 net62 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (net62 A1 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (net62 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends AOI21X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AND2XL
// View name: schematic
subckt AND2XL A B Y inh_VDD inh_VSS
   mn2 (Y net57 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (net73 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (net57 B net73 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp1 (net57 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (net57 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (Y net57 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AND2XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI211X1
// View name: schematic
subckt OAI211X1 A0 A1 B0 C0 Y inh_VDD inh_VSS
   mn1 (n0 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (n0 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (n1 B0 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn3 (Y C0 n1 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp1 (Y A1 n2 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (n2 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp3 (Y C0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp2 (Y B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI211X1
// End of subcircuit definition.
```

```
// Library name: gsclib045
// Cell name: NAND3X1
// View name: schematic
subckt NAND3X1 A B C Y inh_VDD inh_VSS
   mn1 (n0 B n1 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (Y C n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (n1 A inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp0 (Y A inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (Y B inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp2 (Y C inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends NAND3X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI222X1
// View name: schematic
subckt OAI222X1 A0 A1 B0 B1 C0 C1 Y inh_VDD inh_VSS
   mn5 (Y C1 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn4 (Y C0 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn3 (n0 B1 n1 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (n0 B0 n1 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn0 (n1 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn1 (n1 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp5 (Y C1 n4 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp4 (n4 C0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp3 (Y B1 n3 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp2 (n3 B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (Y A1 n2 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (n2 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI222X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NAND3BXL
// View name: schematic
subckt NAND3BXL AN B C Y inh_VDD inh_VSS
   mn3 (Y C n1 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (n0 AN inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (n1 B n2 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n2 n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp1 (Y n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp3 (Y C inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n0 AN inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (Y B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends NAND3BXL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NAND2BXL
// View name: schematic
subckt NAND2BXL AN B Y inh_VDD inh_VSS
   mn2 (Y B n1 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (n0 AN inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n1 n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp1 (Y n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (Y B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n0 AN inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends NAND2BXL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: XOR2XL
// View name: schematic
subckt XOR2XL A B Y inh_VDD inh_VSS
   mn1 (n2 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (n1 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn5 (Y n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn3 (n0 B net131 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn4 (n0 n2 n1 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (net131 n1 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp3 (n0 n2 net130 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp1 (n2 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp4 (n1 B n0 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp5 (Y n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (net130 n1 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends XOR2XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OR3XL
// View name: schematic
subckt OR3XL A B C Y inh_VDD inh_VSS
   mn3 (Y n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n0 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (n0 C inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp3 (Y n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp1 (n2 B n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (n0 C n2 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OR3XL
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// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OR4X1
// View name: schematic
subckt OR4X1 A B C D Y inh_VDD inh_VSS
   mn4 (Y n0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn3 (n0 D inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (n0 C inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n0 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp4 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp3 (n0 D n3 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp1 (n2 B n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (n3 C n2 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OR4X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AND3XL
// View name: schematic
subckt AND3XL A B C Y inh_VDD inh_VSS
   mn3 (Y net87 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (net107 B net103 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (net103 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (net87 C net107 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp1 (net87 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp2 (net87 C inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (net87 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp3 (Y net87 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AND3XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI22X1
// View name: schematic
subckt OAI22X1 A0 A1 B0 B1 Y inh_VDD inh_VSS
   mn0 (net102 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn3 (Y B1 net102 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn1 (net102 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn2 (Y B0 net102 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mp3 (Y B1 net85 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp1 (Y A1 net93 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp0 (net93 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp2 (net85 B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI22X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: ADDHX1
// View name: schematic
subckt ADDHX1 A B CO S inh_VDD inh_VSS
   mn8 (CO COb inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn7 (COb B n4 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn6 (n4 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn5 (S Sb inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
   mn3 (Sb B n2 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn2 (n2 n0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn1 (n1 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn4 (Sb n1 n0 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mp8 (CO COb inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp5 (S Sb inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
   mp2 (n3 n0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp3 (Sb n1 n3 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp4 (Sb B n0 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp1 (n1 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp7 (COb B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp0 (n0 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
   mp6 (COb A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends ADDHX1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: DFFQXL
// View name: schematic
subckt DFFQXL CK D Q inh_VDD inh_VSS
   mn26 (n20 CKb n21 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn25 (n21 D inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn55 (Q qbint inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn50 (n35 qbint inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn51 (n30 CKb n35 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn35 (n25 mout inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn30 (mout n20 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn40 (n30 CKbb mout inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn45 (qbint n30 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
   mn21 (CKbb CKb inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
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    mn36 (n20 CKbb n25 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn20 (CKb CK inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp26 (n20 CKbb n22 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp25 (n22 D inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp51 (n30 CKbb n36 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp50 (n36 qbint inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp55 (Q qbint inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp35 (n26 mout inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp36 (n20 CKb n26 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp21 (CKbb CKb inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp20 (CKb CK inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp45 (qbint n30 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp40 (n30 CKb mout inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp30 (mout n20 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends DFFQXL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: MXI2XL
// View name: schematic
subckt MXI2XL A B S0 Y inh_VDD inh_VSS
    mn3 (n5 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn4 (Y S0 n5 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn2 (Y S0b n3 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn1 (n3 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (S0b S0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp4 (Y S0b n6 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp3 (n6 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (Y S0 n4 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
      ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
      sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp1 (n4 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp0 (S0b S0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends MXI2XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AND4X1
// View name: schematic
subckt AND4X1 A B C D Y inh_VDD inh_VSS
    mn3 (net116 D net132 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn2 (net132 C net128 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn4 (Y net116 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn1 (net128 B net124 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn0 (net124 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
      ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
      sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mp3 (net116 D inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp2 (net116 C inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp1 (net116 B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
    mp4 (Y net116 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (net116 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
      ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
      sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AND4X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OAI32X1
// View name: schematic
subckt OAI32X1 A0 A1 A2 B0 B1 Y inh_VDD inh_VSS
    mn3 (Y B0 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn4 (Y B1 n0 inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f ad=36.4f \
      ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n sd=160n \
      sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn2 (n0 A2 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (n0 A0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn1 (n0 A1 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp2 (Y A2 n2 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp3 (n4 B0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (n1 A0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp4 (Y B1 n4 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp1 (n2 A1 n1 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OAI32X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NOR4X1
// View name: schematic
subckt NOR4X1 A B C D Y inh_VDD inh_VSS
    mn2 (Y C inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn3 (Y D inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn0 (Y A inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mn1 (Y B inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
      ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
      sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
    mp1 (n1 B n0 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp3 (Y D n2 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp2 (n2 C n1 inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f ad=54.6f \
      ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n sb=140n \
      sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
    mp0 (n0 A inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
      ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
      sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends NOR4X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NAND4XL
// View name: schematic
subckt NAND4XL A B C D Y inh_VDD inh_VSS
    mn1 (n1 B n2 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
      sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
    mn3 (Y D n0 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
      ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
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    sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn2 (n0 C n1 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f ad=20.3f \
    ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n sd=160n \
    sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn0 (n2 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp3 (Y D inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp2 (Y C inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp1 (Y B inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp0 (Y A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends NAND4XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NOR2XL
// View name: schematic
subckt NOR2XL A B Y inh_VDD inh_VSS
  mn1 (Y B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn0 (Y A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp1 (Y B net41 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
    ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
    sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp0 (net41 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends NOR2XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: AOI211XL
// View name: schematic
subckt AOI211XL A0 A1 B0 C0 Y inh_VDD inh_VSS
  mn2 (Y B0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn3 (Y C0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn1 (Y A1 net95 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn0 (net95 A0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp3 (Y C0 net82 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp2 (net82 B0 net91 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp1 (net91 A1 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp0 (net91 A0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends AOI211XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: INVXL
// View name: schematic
subckt INVXL A Y inh_VDD inh_VSS
  mp0 (Y A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mn0 (Y A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
ends INVXL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OR3X1
// View name: schematic
subckt OR3X1 A B C Y inh_VDD inh_VSS
  mn3 (Y n0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
    ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
    sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
  mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn1 (n0 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn2 (n0 C inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp3 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
    ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
    sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
  mp1 (n2 B n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
    ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
    sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp2 (n0 C n2 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
    ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
    sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OR3X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: NOR3XL
// View name: schematic
subckt NOR3XL A B C Y inh_VDD inh_VSS
  mn0 (Y A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn1 (Y B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn2 (Y C inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp1 (n1 B n0 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
    ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
    sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp2 (Y C n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
    ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
    sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp0 (n0 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends NOR3XL
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OA22X1
// View name: schematic
subckt OA22X1 A0 A1 B0 B1 Y inh_VDD inh_VSS
  mn3 (net128 B1 net124 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn2 (net128 B0 net124 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn1 (net124 A1 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn0 (net124 A0 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn4 (Y net128 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
    ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
    sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
  mp3 (net128 B1 net115 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp2 (net115 B0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp1 (net128 A1 net119 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp0 (net119 A0 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp4 (Y net128 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
    ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
    sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
ends OA22X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: OR2X1
// View name: schematic
subckt OR2X1 A B Y inh_VDD inh_VSS
  mn2 (Y n0 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 as=36.4f \
    ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m sa=140n sb=140n \
    sd=160n sca=144.98299 scb=0.10251 scc=0.01780 m=(1)
  mn0 (n0 A inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn1 (n0 B inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp1 (n0 B n1 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f ad=30.1f \
    ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n sd=160n \
    sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp2 (Y n0 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
    ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
```

```
    sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
  mp0 (n1 A inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
ends OR2X1
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: DFFRX2
// View name: schematic
subckt DFFRX2 CK D Q QN RN inh_VDD inh_VSS
  mn36 (n25 mout n27 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn35 (n27 RN inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn37 (n20 CKbb n25 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn26 (n20 CKb n21 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn25 (n21 D inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn57 (QN qint inh_VSS inh_VSS) g45n1svt w=(520n) l=45n nf=1 as=72.8f \
    ad=72.8f ps=1.32u pd=1.32u nrd=269.231m nrs=269.231m sa=140n \
    sb=140n sd=160n sca=98.28759 scb=0.08111 scc=0.01166 m=(1)
  mn55 (Q qbint inh_VSS inh_VSS) g45n1svt w=(520n) l=45n nf=1 as=72.8f \
    ad=72.8f ps=1.32u pd=1.32u nrd=269.231m nrs=269.231m sa=140n \
    sb=140n sd=160n sca=98.28759 scb=0.08111 scc=0.01166 m=(1)
  mn45 (n35 RN inh_VSS inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
    ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
    sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
  mn46 (qbint n30 n35 inh_VSS) g45n1svt w=(205n) l=45n nf=1 as=28.7f \
    ad=28.7f ps=690n pd=690n nrd=682.927m nrs=682.927m sa=140n sb=140n \
    sd=160n sca=166.60249 scb=0.10864 scc=0.02069 m=(1)
  mn51 (n30 CKb n40 inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn50 (n40 qbint inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn21 (CKbb CKb inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn40 (n30 CKbb mout inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn30 (mout n20 inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mn56 (qint qbint inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 \
    as=20.3f ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m \
    sa=140n sb=140n sd=160n sca=203.41795 scb=0.11509 scc=0.02523 \
    m=(1)
  mn20 (CKb CK inh_VSS inh_VSS) g45n1svt w=(145n) l=45n nf=1 as=20.3f \
    ad=20.3f ps=570n pd=570n nrd=965.517m nrs=965.517m sa=140n sb=140n \
    sd=160n sca=203.41795 scb=0.11509 scc=0.02523 m=(1)
  mp26 (n20 CKbb n22 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp25 (n22 D inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp51 (n30 CKbb n41 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp50 (n41 qbint inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp57 (QN qint inh_VDD inh_VDD) g45p1svt w=(780n) l=45n nf=1 as=109.2f \
    ad=109.2f ps=1.84u pd=1.84u nrd=179.487m nrs=179.487m sa=140n \
    sb=140n sd=160n sca=80.49887 scb=0.07059 scc=0.00954 m=(1)
  mp55 (Q qbint inh_VDD inh_VDD) g45p1svt w=(780n) l=45n nf=1 as=109.2f \
    ad=109.2f ps=1.84u pd=1.84u nrd=179.487m nrs=179.487m sa=140n \
    sb=140n sd=160n sca=80.49887 scb=0.07059 scc=0.00954 m=(1)
  mp20 (CKb CK inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp21 (CKbb CKb inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp36 (n26 mout inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp30 (mout n20 inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp35 (n26 RN inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp37 (n20 CKb n26 inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp46 (qbint n30 inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
    ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
    sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
  mp40 (n30 CKb mout inh_VDD) g45p1svt w=(215n) l=45n nf=1 as=30.1f \
    ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m sa=140n sb=140n \
    sd=160n sca=162.02845 scb=0.10751 scc=0.02009 m=(1)
  mp45 (qbint RN inh_VDD inh_VDD) g45p1svt w=(310n) l=45n nf=1 as=43.4f \
    ad=43.4f ps=900n pd=900n nrd=451.613m nrs=451.613m sa=140n sb=140n \
    sd=160n sca=130.90642 scb=0.09728 scc=0.01590 m=(1)
  mp56 (qint qbint inh_VDD inh_VDD) g45p1svt w=(215n) l=45n nf=1 \
    as=30.1f ad=30.1f ps=710n pd=710n nrd=651.163m nrs=651.163m \
    sa=140n sb=140n sd=160n sca=162.02845 scb=0.10751 scc=0.02009 \
    m=(1)
ends DFFRX2
// End of subcircuit definition.

// Library name: gsclib045
// Cell name: TIEHI
// View name: schematic
subckt TIEHI Y inh_VDD inh_VSS
  mp0 (Y net25 inh_VDD inh_VDD) g45p1svt w=(390n) l=45n nf=1 as=54.6f \
    ad=54.6f ps=1.06u pd=1.06u nrd=358.974m nrs=358.974m sa=140n \
    sb=140n sd=160n sca=114.89040 scb=0.09003 scc=0.01377 m=(1)
  mn0 (net25 net25 inh_VSS inh_VSS) g45n1svt w=(260n) l=45n nf=1 \
    as=36.4f ad=36.4f ps=800n pd=800n nrd=538.462m nrs=538.462m \
    sa=140n sb=140n sd=160n sca=144.98299 scb=0.10251 scc=0.01780 \
    m=(1)
ends TIEHI
// End of subcircuit definition.

// Library name: fsm_sch
// Cell name: fsm
// View name: schematic
subckt fsm clk rst bank_card_insert deposit_withdrawal_selection \
    account_selection amount\<13\> amount\<12\> amount\<11\> \
    amount\<10\> amount\<9\> amount\<8\> amount\<7\> amount\<6\> \
    amount\<5\> amount\<4\> amount\<3\> amount\<2\> amount\<1\> \
    amount\<0\> pin\<13\> pin\<12\> pin\<11\> pin\<10\> pin\<9\> \
    pin\<8\> pin\<7\> pin\<6\> pin\<5\> pin\<4\> pin\<3\> pin\<2\> \
    pin\<1\> pin\<0\> open_atm_dispense open_atm_receive ready VDD! \
    VSS inh_VDD inh_VSS
  g5027 (n_553 n_191 n_233 inh_VDD inh_VSS) NAND2X1
  g5067 (n_140 n_168 n_169 inh_VDD inh_VSS) NAND2X1
  g5212 (n_25 chequing_local\<8\> n_111 inh_VDD inh_VSS) NAND2X1
  g5095 (n_161 n_364 n_208 inh_VDD inh_VSS) NAND2X1
  g5080 (amount\<11\> chequing_local\<11\> n_74 inh_VDD inh_VSS) NAND2X1
  g4956 (state\<1\> state\<2\> n_86 inh_VDD inh_VSS) NAND2X1
  g5114 (amount\<10\> chequing_local\<10\> n_229 inh_VDD inh_VSS) \
    NAND2X1
  g5056 (n_334 n_140 n_195 inh_VDD inh_VSS) NAND2X1
  g5118 (amount\<9\> chequing_local\<9\> n_65 inh_VDD inh_VSS) NAND2X1
  g5145 (amount\<8\> chequing_local\<8\> n_99 inh_VDD inh_VSS) NAND2X1
  g4983 (n_564 n_111 n_324 inh_VDD inh_VSS) NAND2X1
  g5148 (amount\<4\> savings_local\<4\> n_54 inh_VDD inh_VSS) NAND2X1
  g5158 (amount\<1\> savings_local\<1\> n_77 inh_VDD inh_VSS) NAND2X1
  g5116 (amount\<6\> chequing_local\<6\> n_251 inh_VDD inh_VSS) NAND2X1
  g5153 (amount\<2\> chequing_local\<2\> n_80 inh_VDD inh_VSS) NAND2X1
  g5223 (amount\<9\> n_37 n_116 inh_VDD inh_VSS) NAND2X1
  g5199 (n_39 savings_local\<9\> n_115 inh_VDD inh_VSS) NAND2X1
  g4978 (n_116 n_115 n_378 inh_VDD inh_VSS) NAND2X1
  g4974 (state\<1\> n_296 n_136 inh_VDD inh_VSS) NAND2X1
  g5121 (amount\<10\> savings_local\<10\> n_82 inh_VDD inh_VSS) NAND2X1
  g5208 (n_146 n_555 n_157 inh_VDD inh_VSS) NAND2X1
  g5193 (n_24 savings_local\<3\> n_113 inh_VDD inh_VSS) NAND2X1
  g5054 (n_337 n_141 n_192 inh_VDD inh_VSS) NAND2X1
  g5181 (amount\<0\> chequing_local\<0\> n_94 inh_VDD inh_VSS) NAND2X1
  g5157 (amount\<4\> chequing_local\<4\> n_79 inh_VDD inh_VSS) NAND2X1
  g5147 (amount\<8\> savings_local\<8\> n_98 inh_VDD inh_VSS) NAND2X1
  g5037 (amount\<12\> savings_local\<12\> n_85 inh_VDD inh_VSS) NAND2X1
  g5149 (amount\<2\> savings_local\<2\> n_46 inh_VDD inh_VSS) NAND2X1
  g5084 (amount\<7\> chequing_local\<7\> n_70 inh_VDD inh_VSS) NAND2X1
  g5155 (amount\<1\> chequing_local\<1\> n_84 inh_VDD inh_VSS) NAND2X1
  g5079 (amount\<7\> savings_local\<7\> n_72 inh_VDD inh_VSS) NAND2X1
  g5038 (amount\<12\> chequing_local\<12\> n_68 inh_VDD inh_VSS) NAND2X1
  g4824 (state\<3\> state\<0\> n_22 inh_VDD inh_VSS) NAND2X1
  g5117 (amount\<6\> savings_local\<6\> n_253 inh_VDD inh_VSS) NAND2X1
  g5182 (amount\<0\> savings_local\<0\> n_95 inh_VDD inh_VSS) NAND2X1
  g4970 (n_137 state\<1\> n_120 inh_VDD inh_VSS) NAND2X1
  g5218 (n_38 savings_local\<2\> n_89 inh_VDD inh_VSS) NAND2X1
  g4982 (n_555 n_113 n_264 inh_VDD inh_VSS) NAND2X1
  g5213 (n_38 chequing_local\<2\> n_158 inh_VDD inh_VSS) NAND2X1
  g4823 (n_97 n_402 n_172 inh_VDD inh_VSS) NAND2X1
  g5198 (amount\<11\> n_33 n_123 inh_VDD inh_VSS) NAND2X1
  g5188 (amount\<10\> n_30 n_178 inh_VDD inh_VSS) NAND2X1
  g5133 (n_27 chequing_local\<12\> n_90 inh_VDD inh_VSS) NAND2X1
  g5168 (n_123 n_178 n_163 inh_VDD inh_VSS) NAND2X1
  g5204 (n_35 savings_local\<5\> n_108 inh_VDD inh_VSS) NAND2X1
  g5186 (amount\<4\> n_26 n_131 inh_VDD inh_VSS) NAND2X1
  g5176 (n_108 n_104 n_285 inh_VDD inh_VSS) NAND2X1
  g5183 (n_40 chequing_local\<6\> n_246 inh_VDD inh_VSS) NAND2X1
  g4979 (n_148 n_246 n_306 inh_VDD inh_VSS) NAND2X1
  g4987 (n_563 n_108 n_304 inh_VDD inh_VSS) NAND2X1
  g4976 (n_569 n_567 n_243 inh_VDD inh_VSS) NAND2X1
  g5221 (n_25 savings_local\<8\> n_88 inh_VDD inh_VSS) NAND2X1
  g4779 (rst n_477 n_497 inh_VDD inh_VSS) NOR2X1
  g4764 (rst n_479 n_501 inh_VDD inh_VSS) NOR2X1
  g4892 (state\<1\> n_296 n_150 inh_VDD inh_VSS) NOR2X1
  g4767 (rst n_451 n_487 inh_VDD inh_VSS) NOR2X1
  g4784 (rst n_469 n_481 inh_VDD inh_VSS) NOR2X1
  g5227 (n_39 chequing_local\<9\> n_96 inh_VDD inh_VSS) NOR2X1
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g5112 (amount\<11\> chequing_local\<11\> n_75 inh_VDD inh_VSS) NOR2X1
g5115 (amount\<10\> chequing_local\<10\> n_335 inh_VDD inh_VSS) NOR2X1
g5092 (n_335 n_75 n_140 inh_VDD inh_VSS) NOR2X1
g5064 (n_64 n_66 n_334 inh_VDD inh_VSS) NOR2X1
g5154 (amount\<9\> chequing_local\<9\> n_66 inh_VDD inh_VSS) NOR2X1
g5082 (amount\<8\> chequing_local\<8\> n_64 inh_VDD inh_VSS) NOR2X1
g5150 (amount\<5\> chequing_local\<5\> n_48 inh_VDD inh_VSS) NOR2X1
g5146 (amount\<5\> savings_local\<5\> n_55 inh_VDD inh_VSS) NOR2X1
g5129 (amount\<4\> savings_local\<4\> n_61 inh_VDD inh_VSS) NOR2X1
g5130 (amount\<4\> chequing_local\<4\> n_78 inh_VDD inh_VSS) NOR2X1
g5152 (amount\<2\> chequing_local\<2\> n_81 inh_VDD inh_VSS) NOR2X1
g5123 (n_44 n_81 n_50 inh_VDD inh_VSS) NOR2X1
g5128 (n_44 n_80 n_45 inh_VDD inh_VSS) NOR2X1
g4785 (rst n_330 n_367 inh_VDD inh_VSS) NOR2X1
g5086 (n_59 n_82 n_60 inh_VDD inh_VSS) NOR2X1
g5126 (n_41 n_46 n_47 inh_VDD inh_VSS) NOR2X1
g4776 (rst n_490 n_510 inh_VDD inh_VSS) NOR2X1
g4778 (rst n_489 n_509 inh_VDD inh_VSS) NOR2X1
g4763 (rst n_207 n_245 inh_VDD inh_VSS) NOR2X1
g4958 (state\<1\> state\<2\> n_52 inh_VDD inh_VSS) NOR2X1
g5120 (amount\<10\> savings_local\<10\> n_338 inh_VDD inh_VSS) NOR2X1
g5088 (n_59 n_338 n_141 inh_VDD inh_VSS) NOR2X1
g5224 (n_24 chequing_local\<3\> n_159 inh_VDD inh_VSS) NOR2X1
g5065 (n_63 n_62 n_337 inh_VDD inh_VSS) NOR2X1
g5053 (amount\<12\> savings_local\<12\> n_193 inh_VDD inh_VSS) NOR2X1
g5156 (amount\<3\> chequing_local\<3\> n_44 inh_VDD inh_VSS) NOR2X1
g5119 (amount\<7\> savings_local\<7\> n_73 inh_VDD inh_VSS) NOR2X1
g5160 (amount\<3\> savings_local\<3\> n_41 inh_VDD inh_VSS) NOR2X1
g5083 (amount\<8\> savings_local\<8\> n_63 inh_VDD inh_VSS) NOR2X1
g5151 (amount\<9\> savings_local\<9\> n_62 inh_VDD inh_VSS) NOR2X1
g5179 (amount\<1\> savings_local\<1\> n_76 inh_VDD inh_VSS) NOR2X1
g5110 (amount\<11\> savings_local\<11\> n_59 inh_VDD inh_VSS) NOR2X1
g5055 (amount\<12\> chequing_local\<12\> n_196 inh_VDD inh_VSS) NOR2X1
g5122 (amount\<6\> chequing_local\<6\> n_256 inh_VDD inh_VSS) NOR2X1
g5111 (amount\<6\> savings_local\<6\> n_273 inh_VDD inh_VSS) NOR2X1
g5127 (amount\<7\> chequing_local\<7\> n_69 inh_VDD inh_VSS) NOR2X1
g5180 (amount\<1\> chequing_local\<1\> n_83 inh_VDD inh_VSS) NOR2X1
g4984 (n_146 n_145 n_218 inh_VDD inh_VSS) NOR2X1
g5215 (n_38 savings_local\<2\> n_145 inh_VDD inh_VSS) NOR2X1
g5226 (n_38 chequing_local\<2\> n_212 inh_VDD inh_VSS) NOR2X1
g4988 (n_107 n_559 n_392 inh_VDD inh_VSS) NOR2X1
g5042 (n_231 n_230 n_232 inh_VDD inh_VSS) NOR2X1
g4955 (n_120 n_296 n_121 inh_VDD inh_VSS) NOR2X1
g4975 (n_400 state\<2\> n_401 inh_VDD inh_VSS) NOR2X1
g4786 (rst n_473 n_496 inh_VDD inh_VSS) NOR2X1
g4772 (rst n_493 n_515 inh_VDD inh_VSS) NOR2X1
g4770 (rst n_494 n_512 inh_VDD inh_VSS) NOR2X1
g4774 (rst n_491 n_511 inh_VDD inh_VSS) NOR2X1
g4773 (rst n_492 n_513 inh_VDD inh_VSS) NOR2X1
g5163 (amount\<11\> n_33 n_147 inh_VDD inh_VSS) NOR2X1
g5200 (amount\<10\> n_30 n_224 inh_VDD inh_VSS) NOR2X1
g5136 (n_27 savings_local\<12\> n_231 inh_VDD inh_VSS) NOR2X1
g5094 (n_163 n_177 n_183 inh_VDD inh_VSS) NOR2X1
g5096 (n_559 n_231 n_269 inh_VDD inh_VSS) NOR2X1
g5085 (n_61 n_55 n_278 inh_VDD inh_VSS) NOR2X1
g5113 (n_55 n_54 n_56 inh_VDD inh_VSS) NOR2X1
g4780 (rst n_498 n_508 inh_VDD inh_VSS) NOR2X1
g4769 (rst n_495 n_514 inh_VDD inh_VSS) NOR2X1
g5203 (n_34 chequing_local\<7\> n_106 inh_VDD inh_VSS) NOR2X1
g4977 (n_557 n_124 n_308 inh_VDD inh_VSS) NOR2X1
g5177 (n_557 n_126 n_289 inh_VDD inh_VSS) NOR2X1
g5124 (n_48 n_79 n_49 inh_VDD inh_VSS) NOR2X1
g5090 (n_48 n_78 n_103 inh_VDD inh_VSS) NOR2X1
g5214 (n_35 chequing_local\<5\> n_124 inh_VDD inh_VSS) NOR2X1
g5216 (amount\<4\> n_26 n_125 inh_VDD inh_VSS) NOR2X1
g5166 (n_106 n_105 n_165 inh_VDD inh_VSS) NOR2X1
g5195 (n_40 chequing_local\<6\> n_105 inh_VDD inh_VSS) NOR2X1
g5190 (n_40 savings_local\<6\> n_110 inh_VDD inh_VSS) NOR2X1
g4985 (n_556 n_110 n_314 inh_VDD inh_VSS) NOR2X1
g5087 (n_256 n_69 n_185 inh_VDD inh_VSS) NOR2X1
g5081 (n_273 n_73 n_187 inh_VDD inh_VSS) NOR2X1
g4981 (n_561 n_159 n_281 inh_VDD inh_VSS) NOR2X1
g4766 (rst n_454 n_478 inh_VDD inh_VSS) NOR2X1
g4783 (rst n_468 n_480 inh_VDD inh_VSS) NOR2X1
g4782 (rst n_470 n_482 inh_VDD inh_VSS) NOR2X1
g4781 (rst n_471 n_483 inh_VDD inh_VSS) NOR2X1
g4777 (rst n_472 n_484 inh_VDD inh_VSS) NOR2X1
g4775 (rst n_447 n_485 inh_VDD inh_VSS) NOR2X1
g4768 (rst n_450 n_488 inh_VDD inh_VSS) NOR2X1
g4771 (rst n_448 n_486 inh_VDD inh_VSS) NOR2X1
g4986 (n_144 n_143 n_355 inh_VDD inh_VSS) NOR2X1
g5161 (n_25 savings_local\<8\> n_143 inh_VDD inh_VSS) NOR2X1
g4791 (n_458 n_505 n_301 state\<0\> n_504 n_507 inh_VDD inh_VSS) \
  OAI221X1
g4989 (n_194 n_351 n_193 n_321 n_85 n_352 inh_VDD inh_VSS) OAI221X1
g4793 (n_455 n_505 n_358 state\<0\> n_504 n_503 inh_VDD inh_VSS) \
  OAI221X1
g4792 (n_456 n_505 n_332 state\<0\> n_504 n_506 inh_VDD inh_VSS) \
  OAI221X1
g4794 (n_453 n_505 n_399 state\<0\> n_504 n_502 inh_VDD inh_VSS) \
  OAI221X1
g5019 (n_197 n_323 n_196 n_250 n_68 n_341 inh_VDD inh_VSS) OAI221X1
g4788 (n_441 n_505 n_238 state\<0\> n_504 n_476 inh_VDD inh_VSS) \
  OAI221X1
g4790 (n_434 n_505 n_303 state\<0\> n_504 n_474 inh_VDD inh_VSS) \
  OAI221X1
g4789 (n_435 n_505 n_313 state\<0\> n_504 n_475 inh_VDD inh_VSS) \
  OAI221X1
g4796 (n_449 n_505 n_411 state\<0\> n_504 n_499 inh_VDD inh_VSS) \
  OAI221X1
g4795 (n_452 n_505 n_386 state\<0\> n_504 n_500 inh_VDD inh_VSS) \
  OAI221X1
chequing_local_reg\[11\] (clk n_497 chequing_local\<11\> inh_VDD \
  inh_VSS) DFFHQX1
state_reg\[3\] (clk n_235 state\<3\> inh_VDD inh_VSS) DFFHQX1
chequing_local_reg\[10\] (clk n_487 chequing_local\<10\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[9\] (clk n_481 chequing_local\<9\> inh_VDD \
  inh_VSS) DFFHQX1
savings_local_reg\[3\] (clk n_507 savings_local\<3\> inh_VDD inh_VSS) \
  DFFHQX1
state_reg\[1\] (clk n_367 state\<1\> inh_VDD inh_VSS) DFFHQX1
savings_local_reg\[1\] (clk n_510 savings_local\<1\> inh_VDD inh_VSS) \
  DFFHQX1
savings_local_reg\[2\] (clk n_509 savings_local\<2\> inh_VDD inh_VSS) \
  DFFHQX1
state_reg\[2\] (clk n_268 state\<2\> inh_VDD inh_VSS) DFFHQX1
savings_local_reg\[11\] (clk n_515 savings_local\<11\> inh_VDD \
  inh_VSS) DFFHQX1
savings_local_reg\[10\] (clk n_512 savings_local\<10\> inh_VDD \
  inh_VSS) DFFHQX1
savings_local_reg\[13\] (clk n_511 savings_local\<13\> inh_VDD \
  inh_VSS) DFFHQX1
savings_local_reg\[12\] (clk n_513 savings_local\<12\> inh_VDD \
  inh_VSS) DFFHQX1
savings_local_reg\[6\] (clk n_503 savings_local\<6\> inh_VDD inh_VSS) \
  DFFHQX1
savings_local_reg\[5\] (clk n_506 savings_local\<5\> inh_VDD inh_VSS) \
  DFFHQX1
savings_local_reg\[4\] (clk n_508 savings_local\<4\> inh_VDD inh_VSS) \
  DFFHQX1
savings_local_reg\[0\] (clk n_514 savings_local\<0\> inh_VDD inh_VSS) \
  DFFHQX1
savings_local_reg\[7\] (clk n_502 savings_local\<7\> inh_VDD inh_VSS) \
  DFFHQX1
chequing_local_reg\[0\] (clk n_476 chequing_local\<0\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[4\] (clk n_474 chequing_local\<4\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[3\] (clk n_475 chequing_local\<3\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[13\] (clk n_478 chequing_local\<13\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[12\] (clk n_480 chequing_local\<12\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[8\] (clk n_482 chequing_local\<8\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[7\] (clk n_483 chequing_local\<7\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[6\] (clk n_484 chequing_local\<6\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[5\] (clk n_485 chequing_local\<5\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[1\] (clk n_488 chequing_local\<1\> inh_VDD \
  inh_VSS) DFFHQX1
chequing_local_reg\[2\] (clk n_486 chequing_local\<2\> inh_VDD \
  inh_VSS) DFFHQX1
savings_local_reg\[9\] (clk n_499 savings_local\<9\> inh_VDD inh_VSS) \
  DFFHQX1
savings_local_reg\[8\] (clk n_500 savings_local\<8\> inh_VDD inh_VSS) \
  DFFHQX1
g4875 (n_415 n_439 n_438 chequing_local\<11\> n_429 inh_VDD inh_VSS) \
  AOI22XL
g4866 (n_405 n_439 n_438 chequing_local\<10\> n_431 inh_VDD inh_VSS) \
  AOI22XL
g4884 (n_404 n_439 n_438 chequing_local\<9\> n_427 inh_VDD inh_VSS) \
  AOI22XL
g4861 (n_418 n_265 n_417 savings_local\<3\> n_301 inh_VDD inh_VSS) \
  AOI22XL
g4862 (n_280 n_465 n_464 savings_local\<3\> n_458 inh_VDD inh_VSS) \
  AOI22XL
g4855 (n_418 n_176 n_417 savings_local\<1\> n_234 inh_VDD inh_VSS) \
  AOI22XL
g4857 (n_418 n_220 n_417 savings_local\<2\> n_275 inh_VDD inh_VSS) \
  AOI22XL
g4872 (n_331 n_465 n_464 savings_local\<6\> n_455 inh_VDD inh_VSS) \
  AOI22XL
g4869 (n_316 n_465 n_464 savings_local\<5\> n_456 inh_VDD inh_VSS) \
  AOI22XL
g4832 (n_239 n_418 n_417 savings_local\<0\> n_240 inh_VDD inh_VSS) \
  AOI22XL
g4864 (n_418 n_244 n_417 savings_local\<4\> n_300 inh_VDD inh_VSS) \
  AOI22XL
g4876 (n_327 n_465 n_464 savings_local\<7\> n_453 inh_VDD inh_VSS) \
  AOI22XL
g4886 (n_398 n_439 n_438 chequing_local\<13\> n_426 inh_VDD inh_VSS) \
  AOI22XL
g4878 (n_369 n_439 n_438 chequing_local\<8\> n_428 inh_VDD inh_VSS) \
  AOI22XL
g4836 (n_385 n_439 n_438 chequing_local\<12\> n_440 inh_VDD inh_VSS) \
  AOI22XL
g4834 (n_237 n_439 n_438 chequing_local\<0\> n_441 inh_VDD inh_VSS) \
  AOI22XL
g4835 (n_237 n_422 n_421 chequing_local\<0\> n_238 inh_VDD inh_VSS) \
  AOI22XL
g4849 (n_422 n_267 n_421 chequing_local\<4\> n_303 inh_VDD inh_VSS) \

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AOI22XL
g4851 (n_299 n_439 n_438 chequing_local\<4\> n_434 inh_VDD inh_VSS) \
AOI22XL
g4844 (n_422 n_283 n_421 chequing_local\<3\> n_313 inh_VDD inh_VSS) \
AOI22XL
g4847 (n_282 n_439 n_438 chequing_local\<3\> n_435 inh_VDD inh_VSS) \
AOI22XL
g4854 (n_422 n_309 n_421 chequing_local\<5\> n_342 inh_VDD inh_VSS) \
AOI22XL
g4859 (n_329 n_439 n_438 chequing_local\<5\> n_433 inh_VDD inh_VSS) \
AOI22XL
g4838 (n_182 n_422 n_421 chequing_local\<1\> n_236 inh_VDD inh_VSS) \
AOI22XL
g4840 (n_181 n_439 n_438 chequing_local\<1\> n_437 inh_VDD inh_VSS) \
AOI22XL
g4867 (n_422 n_354 n_421 chequing_local\<7\> n_387 inh_VDD inh_VSS) \
AOI22XL
g4871 (n_375 n_439 n_438 chequing_local\<7\> n_430 inh_VDD inh_VSS) \
AOI22XL
g4860 (n_422 n_307 n_421 chequing_local\<6\> n_340 inh_VDD inh_VSS) \
AOI22XL
g4863 (n_328 n_439 n_438 chequing_local\<6\> n_432 inh_VDD inh_VSS) \
AOI22XL
g4841 (n_422 n_202 n_421 chequing_local\<2\> n_263 inh_VDD inh_VSS) \
AOI22XL
g4842 (n_222 n_439 n_438 chequing_local\<2\> n_436 inh_VDD inh_VSS) \
AOI22XL
g4880 (n_357 n_465 n_464 savings_local\<8\> n_452 inh_VDD inh_VSS) \
AOI22XL
g4883 (n_384 n_465 n_464 savings_local\<9\> n_449 inh_VDD inh_VSS) \
AOI22XL
g5012 (n_177 n_347 n_203 n_343 inh_VDD inh_VSS) OAI21XL
g4996 (n_230 n_347 n_271 n_348 inh_VDD inh_VSS) OAI21XL
g4991 (n_208 n_310 n_248 n_350 inh_VDD inh_VSS) OAI21XL
g5002 (n_143 n_347 n_88 n_346 inh_VDD inh_VSS) OAI21XL
g4939 (n_414 n_388 n_424 inh_VDD inh_VSS) XNOR2X1
g4950 (n_414 n_374 n_415 inh_VDD inh_VSS) XNOR2X1
g4932 (n_382 n_365 n_405 inh_VDD inh_VSS) XNOR2X1
g4905 (n_382 n_349 n_383 inh_VDD inh_VSS) XNOR2X1
g4931 (n_376 n_320 n_377 inh_VDD inh_VSS) XNOR2X1
g4948 (n_376 n_366 n_404 inh_VDD inh_VSS) XNOR2X1
g4909 (n_155 n_180 n_181 inh_VDD inh_VSS) XNOR2X1
g4927 (n_156 n_174 n_175 inh_VDD inh_VSS) XNOR2X1
g4926 (n_95 n_174 n_176 inh_VDD inh_VSS) XNOR2X1
g4929 (n_218 n_199 n_220 inh_VDD inh_VSS) XNOR2X1
g4944 (n_218 n_217 n_219 inh_VDD inh_VSS) XNOR2X1
g4934 (n_264 n_211 n_280 inh_VDD inh_VSS) XNOR2X1
g4907 (n_94 n_180 n_182 inh_VDD inh_VSS) XNOR2X1
g4924 (n_392 n_362 n_406 inh_VDD inh_VSS) XNOR2X1
g4908 (n_395 n_345 n_397 inh_VDD inh_VSS) XNOR2X1
g4922 (n_392 n_352 n_393 inh_VDD inh_VSS) XNOR2X1
g4918 (n_380 n_322 n_381 inh_VDD inh_VSS) XNOR2X1
g4913 (n_552 n_389 n_425 inh_VDD inh_VSS) XNOR2X1
g4916 (n_552 n_360 n_408 inh_VDD inh_VSS) XNOR2X1
g4912 (n_395 n_343 n_396 inh_VDD inh_VSS) XNOR2X1
g4930 (n_326 n_312 n_370 inh_VDD inh_VSS) XNOR2X1
g4941 (n_353 n_317 n_375 inh_VDD inh_VSS) XNOR2X1
g4943 (n_326 n_286 n_327 inh_VDD inh_VSS) XNOR2X1
g4915 (n_314 n_293 n_331 inh_VDD inh_VSS) XNOR2X1
g4940 (n_314 n_279 n_315 inh_VDD inh_VSS) XNOR2X1
g4906 (n_304 n_287 n_316 inh_VDD inh_VSS) XNOR2X1
g4936 (n_243 n_294 n_295 inh_VDD inh_VSS) XNOR2X1
g4904 (n_243 n_242 n_244 inh_VDD inh_VSS) XNOR2X1
g4935 (n_306 n_291 n_328 inh_VDD inh_VSS) XNOR2X1
g4933 (n_306 n_259 n_307 inh_VDD inh_VSS) XNOR2X1
g4928 (n_308 n_288 n_329 inh_VDD inh_VSS) XNOR2X1
g4925 (n_308 n_262 n_309 inh_VDD inh_VSS) XNOR2X1
g4920 (n_266 n_261 n_267 inh_VDD inh_VSS) XNOR2X1
g4923 (n_266 n_298 n_299 inh_VDD inh_VSS) XNOR2X1
g4901 (n_371 n_350 n_385 inh_VDD inh_VSS) XNOR2X1
g4903 (n_371 n_318 n_372 inh_VDD inh_VSS) XNOR2X1
g4898 (n_390 n_363 n_398 inh_VDD inh_VSS) XNOR2X1
g4951 (n_390 n_341 n_391 inh_VDD inh_VSS) XNOR2X1
g4946 (n_324 n_368 n_369 inh_VDD inh_VSS) XNOR2X1
g4945 (n_324 n_323 n_325 inh_VDD inh_VSS) XNOR2X1
g4917 (n_281 n_213 n_282 inh_VDD inh_VSS) XNOR2X1
g4914 (n_281 n_214 n_283 inh_VDD inh_VSS) XNOR2X1
g4910 (n_201 n_198 n_202 inh_VDD inh_VSS) XNOR2X1
g4911 (n_201 n_221 n_222 inh_VDD inh_VSS) XNOR2X1
g4942 (n_355 n_347 n_357 inh_VDD inh_VSS) XNOR2X1
g4902 (n_378 n_346 n_384 inh_VDD inh_VSS) XNOR2X1
g5099 (n_168 n_139 inh_VDD inh_VSS) INVX1
g5258 (chequing_local\<11\> n_10 inh_VDD inh_VSS) INVX1
g5170 (n_161 n_162 inh_VDD inh_VSS) INVX1
g5046 (n_323 n_333 inh_VDD inh_VSS) INVX1
g5211 (n_111 n_58 inh_VDD inh_VSS) INVX1
g5265 (chequing_local\<9\> n_6 inh_VDD inh_VSS) INVX1
g4896 (n_422 n_421 inh_VDD inh_VSS) INVX1
g4893 (n_417 n_418 inh_VDD inh_VSS) INVX1
g4952 (n_438 n_439 inh_VDD inh_VSS) INVX1
g4899 (n_465 n_464 inh_VDD inh_VSS) INVX1
g5264 (state\<2\> n_296 inh_VDD inh_VSS) INVX1
g5245 (savings_local\<9\> n_37 inh_VDD inh_VSS) INVX1
g5271 (chequing_local\<4\> n_26 inh_VDD inh_VSS) INVX1
g5260 (state\<3\> n_402 inh_VDD inh_VSS) INVX1
g5263 (chequing_local\<7\> n_16 inh_VDD inh_VSS) INVX1
g5243 (savings_local\<11\> n_33 inh_VDD inh_VSS) INVX1
g5242 (state\<1\> n_215 inh_VDD inh_VSS) INVX1
g5272 (chequing_local\<13\> n_93 inh_VDD inh_VSS) INVX1
g5250 (savings_local\<10\> n_30 inh_VDD inh_VSS) INVX1
g5217 (n_89 n_146 inh_VDD inh_VSS) INVX1
g4891 (n_150 n_51 inh_VDD inh_VSS) INVX1
g5102 (n_189 n_138 inh_VDD inh_VSS) INVX1
g5173 (n_223 n_203 inh_VDD inh_VSS) INVX1
g5167 (n_163 n_164 inh_VDD inh_VSS) INVX1
g4969 (n_120 n_71 inh_VDD inh_VSS) INVX1
g5070 (n_347 n_361 inh_VDD inh_VSS) INVX1
g5093 (n_183 n_230 inh_VDD inh_VSS) INVX1
g5044 (n_351 n_344 inh_VDD inh_VSS) INVX1
g5132 (n_90 n_91 inh_VDD inh_VSS) INVX1
g5165 (n_165 n_166 inh_VDD inh_VSS) INVX1
g5074 (n_261 n_204 inh_VDD inh_VSS) INVX1
g5189 (n_110 n_170 inh_VDD inh_VSS) INVX1
g5194 (n_105 n_148 inh_VDD inh_VSS) INVX1
g5076 (n_242 n_277 inh_VDD inh_VSS) INVX1
g5089 (n_103 n_255 inh_VDD inh_VSS) INVX1
g5072 (n_310 n_368 inh_VDD inh_VSS) INVX1
g5106 (n_359 n_248 inh_VDD inh_VSS) INVX1
g5060 (n_249 n_250 inh_VDD inh_VSS) INVX1
g5140 (n_198 n_135 inh_VDD inh_VSS) INVX1
g5220 (n_88 n_144 inh_VDD inh_VSS) INVX1
g4812 (n_429 n_442 n_505 n_477 inh_VDD inh_VSS) MX2XL
g4801 (n_431 n_420 n_505 n_451 inh_VDD inh_VSS) MX2XL
g4817 (n_427 n_410 n_505 n_469 inh_VDD inh_VSS) MX2XL
g4810 (n_460 n_234 n_505 n_490 inh_VDD inh_VSS) MX2XL
g4811 (n_459 n_275 n_505 n_489 inh_VDD inh_VSS) MX2XL
g4830 (open_atm_receive n_402 n_150 n_149 inh_VDD inh_VSS) MX2XL
g4808 (n_461 n_416 n_505 n_491 inh_VDD inh_VSS) MX2XL
g4806 (n_463 n_443 n_505 n_493 inh_VDD inh_VSS) MX2XL
g4804 (n_466 n_419 n_505 n_494 inh_VDD inh_VSS) MX2XL
g4807 (n_462 n_413 n_505 n_492 inh_VDD inh_VSS) MX2XL
g4947 (n_351 n_344 n_355 n_356 inh_VDD inh_VSS) MX2XL
g4802 (n_467 n_240 n_505 n_495 inh_VDD inh_VSS) MX2XL
g4814 (n_457 n_300 n_505 n_498 inh_VDD inh_VSS) MX2XL
g4800 (n_426 n_423 n_505 n_454 inh_VDD inh_VSS) MX2XL
g4816 (n_428 n_373 n_505 n_470 inh_VDD inh_VSS) MX2XL
g4818 (n_440 n_409 n_505 n_468 inh_VDD inh_VSS) MX2XL
g4809 (n_433 n_342 n_505 n_447 inh_VDD inh_VSS) MX2XL
g4803 (n_437 n_236 n_505 n_450 inh_VDD inh_VSS) MX2XL
g4815 (n_430 n_387 n_505 n_471 inh_VDD inh_VSS) MX2XL
g4813 (n_432 n_340 n_505 n_472 inh_VDD inh_VSS) MX2XL
g4805 (n_436 n_263 n_505 n_448 inh_VDD inh_VSS) MX2XL
g4888 (bank_card_insert n_296 state\<3\> n_67 inh_VDD inh_VSS) OAI21X1
g4821 (state\<3\> n_150 n_505 n_153 inh_VDD inh_VSS) OAI21X1
g4998 (n_64 n_323 n_99 n_320 inh_VDD inh_VSS) OAI21X1
g5100 (n_66 n_99 n_65 n_168 inh_VDD inh_VSS) OAI21X1
g5141 (n_83 n_94 n_84 n_198 inh_VDD inh_VSS) OAI21X1
g4999 (n_63 n_351 n_98 n_319 inh_VDD inh_VSS) OAI21X1
g4828 (n_402 n_150 n_136 n_151 inh_VDD inh_VSS) OAI21X1
g5014 (n_145 n_217 n_89 n_211 inh_VDD inh_VSS) OAI21X1
g5139 (n_76 n_95 n_77 n_199 inh_VDD inh_VSS) OAI21X1
g4995 (n_192 n_351 n_321 n_322 inh_VDD inh_VSS) OAI21X1
g5001 (n_61 n_242 n_54 n_260 inh_VDD inh_VSS) OAI21X1
g4992 (n_78 n_261 n_79 n_262 inh_VDD inh_VSS) OAI21X1
g4994 (n_81 n_135 n_80 n_214 inh_VDD inh_VSS) OAI21X1
g5050 (n_225 n_566 n_191 inh_VDD inh_VSS) NAND2BX1
g5312 (chequing_local\<1\> amount\<1\> n_554 inh_VDD inh_VSS) NAND2BX1
g5318 (savings_local\<1\> amount\<1\> n_560 inh_VDD inh_VSS) NAND2BX1
g5324 (chequing_local\<10\> amount\<10\> n_566 inh_VDD inh_VSS) \
NAND2BX1
g5311 (amount\<10\> chequing_local\<10\> n_553 inh_VDD inh_VSS) \
NAND2BX1
g4967 (n_75 n_74 n_414 inh_VDD inh_VSS) NAND2BX1
g5327 (savings_local\<4\> amount\<4\> n_569 inh_VDD inh_VSS) NAND2BX1
g5326 (savings_local\<7\> amount\<7\> n_568 inh_VDD inh_VSS) NAND2BX1
g5325 (amount\<4\> savings_local\<4\> n_567 inh_VDD inh_VSS) NAND2BX1
g5322 (chequing_local\<8\> amount\<8\> n_564 inh_VDD inh_VSS) NAND2BX1
g5321 (savings_local\<5\> amount\<5\> n_563 inh_VDD inh_VSS) NAND2BX1
g5316 (chequing_local\<12\> amount\<12\> n_558 inh_VDD inh_VSS) \
NAND2BX1
g5313 (savings_local\<3\> amount\<3\> n_555 inh_VDD inh_VSS) NAND2BX1
g4973 (n_66 n_65 n_376 inh_VDD inh_VSS) NAND2BX1
g5206 (n_145 n_555 n_128 inh_VDD inh_VSS) NAND2BX1
g5138 (n_143 n_116 n_177 inh_VDD inh_VSS) NAND2BX1
g5069 (n_271 n_269 n_270 inh_VDD inh_VSS) NAND2BX1
g5097 (n_559 n_562 n_101 inh_VDD inh_VSS) NAND2BX1
g4961 (n_193 n_85 n_380 inh_VDD inh_VSS) NAND2BX1
g5205 (n_567 n_563 n_104 inh_VDD inh_VSS) NAND2BX1
g4964 (n_81 n_80 n_201 inh_VDD inh_VSS) NAND2BX1
g5075 (amount\<3\> chequing_local\<3\> n_50 n_198 n_45 n_261 inh_VDD \
inh_VSS) AOI221X1
g5057 (amount\<11\> savings_local\<11\> n_141 n_189 n_60 n_321 inh_VDD \
inh_VSS) AOI221X1
g5077 (amount\<3\> savings_local\<3\> n_43 n_199 n_47 n_242 inh_VDD \
inh_VSS) AOI221X1
g4959 (deposit_withdrawal_selection state\<1\> bank_card_insert n_215 \
state\<2\> n_119 inh_VDD inh_VSS) AOI221X1
g5022 (n_178 n_223 n_179 n_361 n_224 n_360 inh_VDD inh_VSS) AOI221X1
g5051 (n_205 n_359 n_206 n_368 n_184 n_403 inh_VDD inh_VSS) AOI221X1
g5109 (n_224 n_123 n_164 n_223 n_147 n_271 inh_VDD inh_VSS) AOI221X1
g5024 (n_170 n_285 n_171 n_294 n_556 n_286 inh_VDD inh_VSS) AOI221X1
g5020 (n_558 n_359 n_210 n_368 n_91 n_363 inh_VDD inh_VSS) AOI221X1
g5000 (n_195 n_323 n_249 n_318 inh_VDD inh_VSS) AOI2BB1XL
g5175 (n_159 n_158 n_561 n_160 inh_VDD inh_VSS) AOI2BB1XL
g5009 (n_255 n_261 n_258 n_259 inh_VDD inh_VSS) OA21X1
g5013 (n_212 n_221 n_158 n_213 inh_VDD inh_VSS) OA21X1
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g5142 (n_212 n_159 n_221 n_160 n_298 inh_VDD inh_VSS) OAI31X1
g4874 (n_422 n_424 n_421 chequing_local\<11\> n_442 inh_VDD inh_VSS) \
  AOI22X1
g4799 (n_446 state\<0\> n_505 n_87 n_479 inh_VDD inh_VSS) AOI22X1
g4837 (n_422 n_383 n_421 chequing_local\<10\> n_420 inh_VDD inh_VSS) \
  AOI22X1
g4882 (n_422 n_377 n_421 chequing_local\<9\> n_410 inh_VDD inh_VSS) \
  AOI22X1
g5210 (n_554 n_155 n_154 chequing_local\<1\> n_221 inh_VDD inh_VSS) \
  AOI22X1
g5209 (n_560 n_156 n_154 savings_local\<1\> n_217 inh_VDD inh_VSS) \
  AOI22X1
g4881 (n_418 n_379 n_417 savings_local\<9\> n_411 inh_VDD inh_VSS) \
  AOI22X1
g4819 (n_297 n_505 state\<0\> n_151 n_330 inh_VDD inh_VSS) AOI22X1
g4856 (n_175 n_465 n_464 savings_local\<1\> n_460 inh_VDD inh_VSS) \
  AOI22X1
g4858 (n_219 n_465 n_464 savings_local\<2\> n_459 inh_VDD inh_VSS) \
  AOI22X1
g4798 (state\<0\> n_149 open_atm_receive n_505 n_207 inh_VDD inh_VSS) \
  AOI22X1
g4853 (n_406 n_465 n_464 savings_local\<13\> n_461 inh_VDD inh_VSS) \
  AOI22X1
g4852 (n_418 n_393 n_417 savings_local\<13\> n_416 inh_VDD inh_VSS) \
  AOI22X1
g4845 (n_418 n_425 n_417 savings_local\<11\> n_443 inh_VDD inh_VSS) \
  AOI22X1
g4846 (n_408 n_465 n_464 savings_local\<11\> n_463 inh_VDD inh_VSS) \
  AOI22X1
g4839 (n_418 n_397 n_417 savings_local\<10\> n_419 inh_VDD inh_VSS) \
  AOI22X1
g4843 (n_396 n_465 n_464 savings_local\<10\> n_466 inh_VDD inh_VSS) \
  AOI22X1
g4848 (n_418 n_381 n_417 savings_local\<12\> n_413 inh_VDD inh_VSS) \
  AOI22X1
g4850 (n_394 n_465 n_464 savings_local\<12\> n_462 inh_VDD inh_VSS) \
  AOI22X1
g4879 (n_418 n_356 n_417 savings_local\<8\> n_386 inh_VDD inh_VSS) \
  AOI22X1
g4870 (n_418 n_315 n_417 savings_local\<6\> n_358 inh_VDD inh_VSS) \
  AOI22X1
g4868 (n_418 n_305 n_417 savings_local\<5\> n_332 inh_VDD inh_VSS) \
  AOI22X1
g4833 (n_239 n_465 n_464 savings_local\<0\> n_467 inh_VDD inh_VSS) \
  AOI22X1
g4865 (n_295 n_465 n_464 savings_local\<4\> n_457 inh_VDD inh_VSS) \
  AOI22X1
g4873 (n_418 n_370 n_417 savings_local\<7\> n_399 inh_VDD inh_VSS) \
  AOI22X1
g5144 (n_556 n_568 n_34 savings_local\<7\> n_134 inh_VDD inh_VSS) \
  AOI22X1
g4831 (n_422 n_391 n_421 chequing_local\<13\> n_423 inh_VDD inh_VSS) \
  AOI22X1
g4877 (n_422 n_325 n_421 chequing_local\<8\> n_373 inh_VDD inh_VSS) \
  AOI22X1
g4885 (n_422 n_372 n_421 chequing_local\<12\> n_409 inh_VDD inh_VSS) \
  AOI22X1
g5159 (amount\<2\> savings_local\<2\> n_42 inh_VDD inh_VSS) OR2XL
g5039 (n_193 n_192 n_194 inh_VDD inh_VSS) OR2XL
g5035 (n_196 n_195 n_197 inh_VDD inh_VSS) OR2XL
g5323 (amount\<11\> chequing_local\<11\> n_565 inh_VDD inh_VSS) \
  NOR2BX1
g5171 (n_566 n_565 n_161 inh_VDD inh_VSS) NOR2BX1
g5320 (savings_local\<12\> amount\<12\> n_562 inh_VDD inh_VSS) NOR2BX1
g5319 (chequing_local\<3\> amount\<3\> n_561 inh_VDD inh_VSS) NOR2BX1
g5317 (amount\<13\> savings_local\<13\> n_559 inh_VDD inh_VSS) NOR2BX1
g5315 (chequing_local\<5\> amount\<5\> n_557 inh_VDD inh_VSS) NOR2BX1
g5314 (savings_local\<6\> amount\<6\> n_556 inh_VDD inh_VSS) NOR2BX1
g5137 (n_564 n_96 n_364 inh_VDD inh_VSS) NOR2BX1
g4960 (n_229 n_335 n_382 inh_VDD inh_VSS) NOR2BX1
g5131 (n_42 n_41 n_43 inh_VDD inh_VSS) NOR2BX1
g4966 (n_77 n_76 n_174 inh_VDD inh_VSS) NOR2BX1
g5091 (savings_local\<13\> amount\<13\> n_107 inh_VDD inh_VSS) NOR2BX1
g4962 (n_84 n_83 n_180 inh_VDD inh_VSS) NOR2BX1
g4765 (n_241 rst n_268 inh_VDD inh_VSS) NOR2BX1
g4963 (n_82 n_338 n_395 inh_VDD inh_VSS) NOR2BX1
g5049 (n_178 n_177 n_179 inh_VDD inh_VSS) NOR2BX1
g5068 (n_205 n_208 n_206 inh_VDD inh_VSS) NOR2BX1
g2 (n_123 n_147 n_552 inh_VDD inh_VSS) NOR2BX1
g5098 (n_558 n_167 n_205 inh_VDD inh_VSS) NOR2BX1
g4971 (n_70 n_69 n_353 inh_VDD inh_VSS) NOR2BX1
g5164 (n_568 n_110 n_227 inh_VDD inh_VSS) NOR2BX1
g5207 (n_125 n_124 n_126 inh_VDD inh_VSS) NOR2BX1
g5169 (n_131 n_124 n_290 inh_VDD inh_VSS) NOR2BX1
g4965 (n_79 n_78 n_266 inh_VDD inh_VSS) NOR2BX1
g5041 (n_558 n_208 n_210 inh_VDD inh_VSS) NOR2BX1
g4972 (n_68 n_196 n_371 inh_VDD inh_VSS) NOR2BX1
g5172 (n_563 n_569 n_292 inh_VDD inh_VSS) AND2X1
g5003 (n_564 n_368 n_58 n_366 inh_VDD inh_VSS) AOI21XL
g5005 (n_292 n_294 n_285 n_293 inh_VDD inh_VSS) AOI21XL
g5015 (n_131 n_298 n_125 n_288 inh_VDD inh_VSS) AOI21XL
g4825 (state\<2\> state\<3\> n_86 n_87 inh_VDD inh_VSS) OAI2BB1X1
g4822 (n_67 n_86 state\<0\> n_173 inh_VDD inh_VSS) OAI2BB1X1
g5017 (n_364 n_368 n_225 n_365 inh_VDD inh_VSS) OAI2BB1X1
g4997 (n_42 n_199 n_46 n_200 inh_VDD inh_VSS) OAI2BB1X1
g5232 (n_122 chequing_local\<0\> n_155 n_237 inh_VDD inh_VSS) \
  OAI2BB1X1
g5231 (n_122 savings_local\<0\> n_156 n_239 inh_VDD inh_VSS) OAI2BB1X1
g5174 (n_144 n_116 n_115 n_223 inh_VDD inh_VSS) OAI2BB1X1
g4827 (n_51 open_atm_dispense n_444 n_445 inh_VDD inh_VSS) OAI2BB1X1
g5105 (n_227 n_285 n_134 n_228 inh_VDD inh_VSS) OAI2BB1X1
g5011 (n_278 n_277 n_276 n_279 inh_VDD inh_VSS) OAI2BB1X1
g5016 (n_569 n_294 n_567 n_287 inh_VDD inh_VSS) OAI2BB1X1
g5006 (n_290 n_298 n_289 n_291 inh_VDD inh_VSS) OAI2BB1X1
g5023 (n_566 n_364 n_368 n_233 n_374 inh_VDD inh_VSS) AOI31X1
g5052 (n_269 n_183 n_361 n_311 n_400 inh_VDD inh_VSS) AOI31X1
g5045 (n_278 n_187 n_277 n_254 n_351 inh_VDD inh_VSS) AOI31X1
g5073 (n_165 n_290 n_298 n_247 n_310 inh_VDD inh_VSS) AOI31X1
g5071 (n_227 n_292 n_294 n_228 n_347 inh_VDD inh_VSS) AOI31X1
g5047 (n_103 n_185 n_204 n_252 n_323 inh_VDD inh_VSS) AOI31X1
g4787 (n_173 n_153 rst n_235 inh_VDD inh_VSS) AOI21X1
g4993 (n_334 n_333 n_168 n_349 inh_VDD inh_VSS) AOI21X1
g5010 (n_337 n_344 n_189 n_345 inh_VDD inh_VSS) AOI21X1
g5101 (amount\<5\> savings_local\<5\> n_56 n_276 inh_VDD inh_VSS) \
  AOI21X1
g5104 (amount\<5\> chequing_local\<5\> n_49 n_258 inh_VDD inh_VSS) \
  AOI21X1
g5048 (n_170 n_292 n_171 inh_VDD inh_VSS) AND2XL
g5018 (n_335 n_139 n_229 n_336 n_388 inh_VDD inh_VSS) OAI211X1
g5061 (n_75 n_229 n_74 n_169 n_249 inh_VDD inh_VSS) OAI211X1
g5143 (n_128 n_217 n_113 n_157 n_294 inh_VDD inh_VSS) OAI211X1
g4820 (n_52 state\<0\> n_57 n_172 n_241 inh_VDD inh_VSS) OAI211X1
g4887 (bank_card_insert state\<1\> state\<2\> state\<3\> n_57 inh_VDD \
  inh_VSS) OAI211X1
g5004 (n_338 n_138 n_82 n_339 n_389 inh_VDD inh_VSS) OAI211X1
g5007 (n_256 n_258 n_251 n_257 n_302 inh_VDD inh_VSS) OAI211X1
g5059 (n_69 n_251 n_70 n_186 n_252 inh_VDD inh_VSS) OAI211X1
g5058 (n_73 n_253 n_72 n_188 n_254 inh_VDD inh_VSS) OAI211X1
g5008 (n_273 n_276 n_253 n_274 n_312 inh_VDD inh_VSS) OAI211X1
g5025 (n_105 n_289 n_246 n_284 n_317 inh_VDD inh_VSS) OAI211X1
g4895 (n_412 state\<1\> n_296 n_444 inh_VDD inh_VSS) NAND3X1
g5028 (n_148 n_290 n_298 n_284 inh_VDD inh_VSS) NAND3X1
g5107 (n_553 n_565 n_162 n_225 amount\<11\> n_10 n_359 inh_VDD \
  inh_VSS) OAI222X1
g4826 (n_402 n_32 n_216 state\<2\> n_215 n_296 n_297 inh_VDD inh_VSS) \
  OAI222X1
g5108 (n_246 n_106 n_166 n_289 amount\<7\> n_16 n_247 inh_VDD inh_VSS) \
  OAI222X1
g5030 (n_335 n_334 n_333 n_336 inh_VDD inh_VSS) NAND3BXL
g5062 (n_107 n_101 n_270 n_311 inh_VDD inh_VSS) NAND3BXL
g5029 (n_338 n_337 n_344 n_339 inh_VDD inh_VSS) NAND3BXL
g5032 (n_273 n_278 n_277 n_274 inh_VDD inh_VSS) NAND3BXL
g5040 (pin\<13\> pin\<7\> n_21 inh_VDD inh_VSS) NAND2BXL
g5066 (n_258 n_185 n_186 inh_VDD inh_VSS) NAND2BXL
g4968 (n_73 n_72 n_326 inh_VDD inh_VSS) NAND2BXL
g5063 (n_276 n_187 n_188 inh_VDD inh_VSS) NAND2BXL
g4919 (n_378 n_319 n_379 inh_VDD inh_VSS) XOR2XL
g4937 (n_264 n_200 n_265 inh_VDD inh_VSS) XOR2XL
g4921 (n_380 n_348 n_394 inh_VDD inh_VSS) XOR2XL
g4949 (n_353 n_302 n_354 inh_VDD inh_VSS) XOR2XL
g4938 (n_304 n_260 n_305 inh_VDD inh_VSS) XOR2XL
g5031 (n_256 n_255 n_261 n_257 inh_VDD inh_VSS) OR3XL
g4953 (n_120 n_403 state\<2\> n_402 n_438 inh_VDD inh_VSS) OR4X1
g4897 (n_71 n_296 n_402 n_422 inh_VDD inh_VSS) AND3XL
g5103 (n_62 n_98 n_39 n_37 n_189 inh_VDD inh_VSS) OAI22X1
g5026 (account_selection n_403 n_137 n_400 n_412 inh_VDD inh_VSS) \
  OAI22X1
g5078 (n_167 n_90 amount\<13\> n_93 n_184 inh_VDD inh_VSS) OAI22X1
g5230 (amount\<13\> n_93 n_167 n_390 inh_VDD inh_VSS) ADDHX1
open_atm_receive_reg (clk n_245 open_atm_receive inh_VDD inh_VSS) \
  DFFQXL
open_atm_dispense_reg (clk n_496 open_atm_dispense inh_VDD inh_VSS) \
  DFFQXL
g4797 (n_445 open_atm_dispense n_22 n_473 inh_VDD inh_VSS) MXI2XL
g4900 (account_selection n_401 state\<1\> state\<3\> n_465 inh_VDD \
  inh_VSS) AND4X1
g4889 (deposit_withdrawal_selection state\<2\> n_215 state\<1\> n_296 \
  n_97 inh_VDD inh_VSS) OAI32X1
g4829 (n_119 n_121 state\<3\> n_444 n_402 n_446 inh_VDD inh_VSS) \
  OAI32X1
g5034 (pin\<8\> pin\<9\> pin\<11\> pin\<12\> n_28 inh_VDD inh_VSS) \
  NOR4X1
g4990 (pin\<0\> pin\<2\> n_21 n_29 n_142 inh_VDD inh_VSS) NOR4X1
g4954 (n_23 n_28 n_142 n_215 n_216 inh_VDD inh_VSS) NAND4XL
g5033 (pin\<1\> pin\<10\> pin\<4\> pin\<6\> n_29 inh_VDD inh_VSS) \
  NAND4XL
g5043 (n_231 n_271 n_272 inh_VDD inh_VSS) NOR2XL
g5036 (pin\<3\> pin\<5\> n_23 inh_VDD inh_VSS) NOR2XL
g5021 (n_232 n_361 n_562 n_272 n_362 inh_VDD inh_VSS) AOI211XL
g5259 (amount\<9\> n_39 inh_VDD inh_VSS) INVXL
g5268 (amount\<8\> n_25 inh_VDD inh_VSS) INVXL
g5239 (amount\<3\> n_24 inh_VDD inh_VSS) INVXL
g5257 (amount\<12\> n_27 inh_VDD inh_VSS) INVXL
g5251 (amount\<2\> n_38 inh_VDD inh_VSS) INVXL
g5240 (amount\<6\> n_40 inh_VDD inh_VSS) INVXL
g5270 (amount\<5\> n_35 inh_VDD inh_VSS) INVXL
g5273 (amount\<0\> n_122 inh_VDD inh_VSS) INVXL
g5269 (amount\<7\> n_34 inh_VDD inh_VSS) INVXL
g5274 (rst n_504 inh_VDD inh_VSS) INVXL
g5253 (amount\<1\> n_154 inh_VDD inh_VSS) INVXL
g5310 (n_52 n_32 inh_VDD inh_VSS) INVXL
g5261 (account_selection n_137 inh_VDD inh_VSS) INVXL
g4894 (n_137 state\<3\> n_136 n_417 inh_VDD inh_VSS) OR3X1
g4762 (state\<3\> n_32 n_505 ready inh_VDD inh_VSS) NOR3XL
g5178 (n_96 n_111 amount\<9\> n_6 n_225 inh_VDD inh_VSS) OA22X1
g5233 (n_122 chequing_local\<0\> n_155 inh_VDD inh_VSS) OR2X1
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   g5234 (n_122 savings_local\<0\> n_156 inh_VDD inh_VSS) OR2X1
   state_reg\[0\] (clk n_501 n_505 state\<0\> logic_1_1_net inh_VDD \
       inh_VSS) DFFRX2
   tie_1_cell (logic_1_1_net inh_VDD inh_VSS) TIEHI
ends fsm
// End of subcircuit definition.

// Library name: fsm_tb
// Cell name: fsm_tb
// View name: schematic
I0 (CLK RST CARD_INSERT DW_SELECT ACC_SELECT amount\<13\> amount\<12\> \
        amount\<11\> amount\<10\> amount\<9\> amount\<8\> amount\<7\> \
        amount\<6\> amount\<5\> amount\<4\> amount\<3\> amount\<2\> \
        amount\<1\> amount\<0\> pin\<13\> pin\<12\> pin\<11\> pin\<10\> \
        pin\<9\> pin\<8\> pin\<7\> pin\<6\> pin\<5\> pin\<4\> pin\<3\> \
        pin\<2\> pin\<1\> pin\<0\> ATM_OUT ATM_IN READY VDD! VSS! VDD! \
        VSS!) fsm
I1 (0 VSS!) iprobe
C3 (READY 0) capacitor c=10f
C2 (ATM_IN 0) capacitor c=10f
C1 (ATM_OUT 0) capacitor c=10f
V1 (CLK 0) vsource dc=0 type=pulse edgetype=linear val0=0 val1=1 period=T \
        rise=10p fall=10p width=T/2
V2 (RST 0) vsource type=pwl wave=[ 0 1 ((2*T)) 1 ((2.01*T)) 0 ]
V49 (VDD! 0) vsource dc=1 type=dc
V76 (pin\<13\> 0) vsource dc=0 type=dc
V75 (pin\<12\> 0) vsource dc=0 type=dc
V74 (pin\<11\> 0) vsource dc=0 type=dc
V63 (pin\<0\> 0) vsource dc=0 type=dc
V73 (pin\<10\> 0) vsource dc=0 type=dc
V64 (pin\<1\> 0) vsource dc=0 type=dc
V72 (pin\<9\> 0) vsource dc=0 type=dc
V65 (pin\<2\> 0) vsource dc=0 type=dc
V71 (pin\<8\> 0) vsource dc=0 type=dc
V70 (pin\<7\> 0) vsource dc=0 type=dc
V66 (pin\<3\> 0) vsource dc=0 type=dc
V67 (pin\<4\> 0) vsource dc=0 type=dc
V68 (pin\<5\> 0) vsource dc=0 type=dc
V69 (pin\<6\> 0) vsource dc=0 type=dc
V62 (amount\<0\> 0) vsource dc=0 type=dc
V61 (amount\<1\> 0) vsource dc=0 type=dc
V60 (amount\<2\> 0) vsource dc=0 type=dc
V59 (amount\<3\> 0) vsource dc=0 type=dc
V58 (amount\<4\> 0) vsource dc=0 type=dc
V57 (amount\<5\> 0) vsource dc=0 type=dc
V56 (amount\<6\> 0) vsource dc=0 type=dc
V55 (amount\<7\> 0) vsource dc=0 type=dc
V54 (amount\<8\> 0) vsource dc=0 type=dc
V53 (amount\<9\> 0) vsource dc=0 type=dc
V52 (amount\<10\> 0) vsource dc=0 type=dc
V51 (amount\<11\> 0) vsource dc=0 type=dc
V17 (amount\<13\> 0) vsource dc=0 type=dc
V50 (amount\<12\> 0) vsource dc=0 type=dc
V5 (ACC_SELECT 0) vsource dc=1 type=dc
V4 (DW_SELECT 0) vsource dc=1 type=dc
V3 (CARD_INSERT 0) vsource dc=0 type=dc
simulatorOptions options psfversion="1.1.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=25 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=10n errpreset=liberal write="spectre.ic" \
    writefinal="spectre.fc" annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```