1) Choose the right answer (3 pts):

DIBL reduces Vth

a) Threshold voltage increases as we increase V_{ds} in short channel devices — T (F)

b) Pesudo NMOS design draws static current when output is low — (T) F

It is an exponential dependence

c) Gate leakage quadratically increases with decreasing gate oxide thickness — T (F)

c) What is the effect of changing the substrate bias voltage, V_{SB} from 1 V to 0 V for a MOS device. Answer either increase, decrease or no change. Estimate the percentage change if you picked "increase" or "decrease" and show your work for estimates. Use $2|\phi_F| = 0.8V$ and $\phi_B = 0.9V$ (built-in junction potential), Vdd = 1.2V (4pts).

a) Source junction cap, C_J (increase by 45 %) decrease by _____% no change

b) Threshold voltage, Vth : increase by ___% (decrease by 18 %) no change

a) $C_J = \frac{C_{j0} A}{(1 - \frac{V_J}{\varphi_B})^{1/2}} \Rightarrow \frac{C_{J2}}{C_{J1}} = \sqrt{\frac{(1 - V_{J1}/\varphi_B)}{(1 - V_{J2}/\varphi_B)}}$

$V_{SB} = \phi \Rightarrow V_J = \phi$

$V_{SB} = 1 \Rightarrow V_J = -1$

* V_J is forward bias Voltage

$\frac{C_{J2}(V_{SB}=\phi)}{C_{J1}(V_{SB}=1)} = \sqrt{\frac{(1 - (-1)/0.9}{1}} \simeq 1.45 \Rightarrow 45\%$ increase

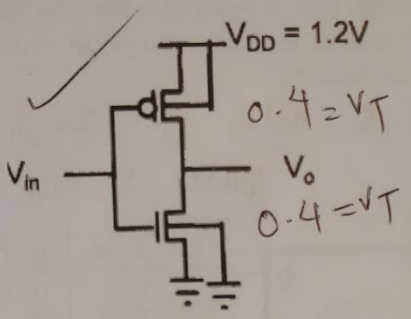
b) $V_T = V_{T\phi} + \gamma\left(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F}\right)$

$V_{T1} = 0.4 + 0.2\left(\sqrt{1 + 0.8} - \sqrt{0.8}\right) \simeq 0.49V$

$V_{T2} = V_{T\phi} = 0.4V$

$\frac{V_{T2}}{V_{T1}} = \frac{0.4}{0.49} \simeq 0.82 \Rightarrow 18\%$ decrease

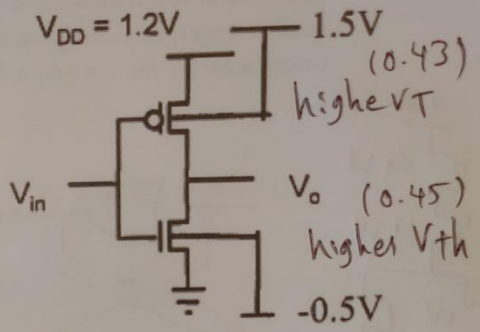
2. Which of the following two circuits switches faster as the input toggles? And Why (one sentence only) (2 points)



0.4 = V_T

0.4 = V_T

↓ more current when switching (smaller V_T)

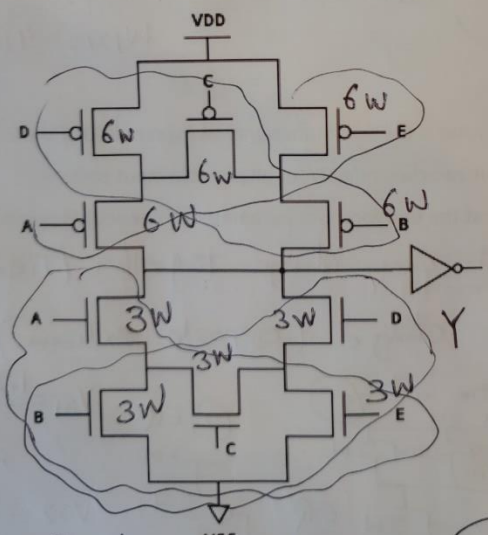


(0.43) higher V_T

(0.45) higher V_{th}

using V_T ↑ formula

b) What is the function implemented by the following circuit (after the inverter) (3 pts) size transistors to achieve the minimum delay (4 pts)



WC PU

WC PU or PD is 3 transistor

Since there is an inverter we can simply find PD & declare as F

method 1

↳ $X = A \cdot (B + CE)$

$Y = D \cdot (E + BC)$

$F = X + Y = A \cdot (B + CE) + D(E + BC)$

method 2 if $C = \emptyset$ (NMOS OFF)

$PD \Rightarrow AB + DE$

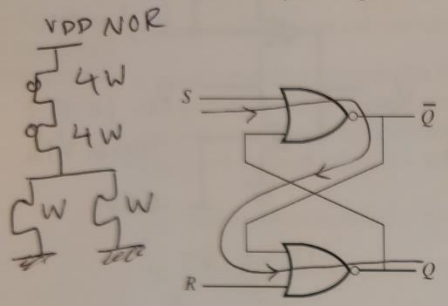
if $C = 1$ (NMOS ON)

$PD \Rightarrow (A + D) \cdot (B + E)$

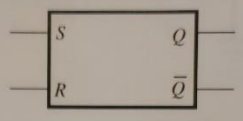
Combine

So, $F = \overline{C}(AB + DE) + C(A + D)(B + E)$

3. The following pictures show SR-latch implementation using NOR gates (and truth table just for your reference). Design the size of devices (i.e. Widths of transistors) in NOR to deliver a worst-case delay of 400 ps from S to Q in a 90 nm technology (you can assume L = 100nm for simplicity). Assume there is an external capacitance of 200 fF attached to both Q and Q_bar which dominates capacitance, i.e. you can ignore device capacitance. (6 points)



S-Q delay goes through TWO NOR gates so each delay $\frac{400ps}{2} = 200ps$



S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

$T_{PHL} = T_{PLH} = 0.7RC = 200PS$

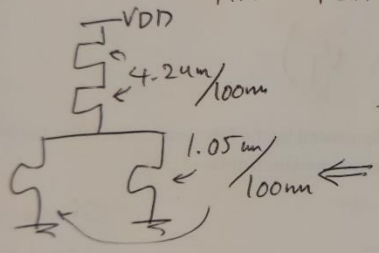
$= 0.7 \times 200fF \times R = 200PS$

$= 0.7 \times 200 \times 15 \frac{k\Omega}{fF} \times \frac{100nm}{W} = 200PS$

$W = 1050\,nm = 1.05\mu m$

NMOS

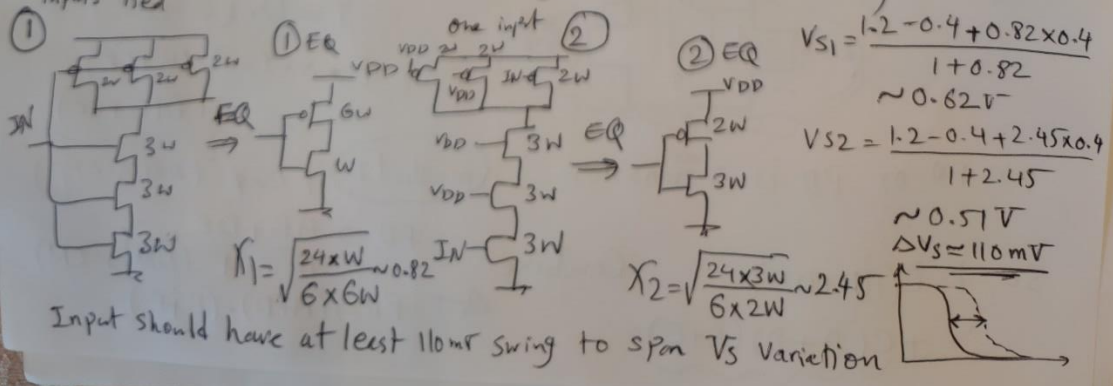
$W_{PMOS} = 4W = 4.2\mu m$



b) Assuming a noise-free environment what is the minimum signal swing required at the input of a 3-input NAND gate to ensure the output switches reliably for all possible input pattern combinations (Wn = 300 nm, use table at the end for more parameters if needed) (4 points)

① For a NAND3 All inputs can change together (Tied) one extreme

② Or only one input change (opposite extreme)



$V_{S1} = \frac{1.2 - 0.4 + 0.82 \times 0.4}{1 + 0.82} \sim 0.62V$

$V_{S2} = \frac{1.2 - 0.4 + 2.45 \times 0.4}{1 + 2.45} \sim 0.51V$

$\Delta V_S \simeq 110mV$

Input should have at least 110mV swing to span V_S variation

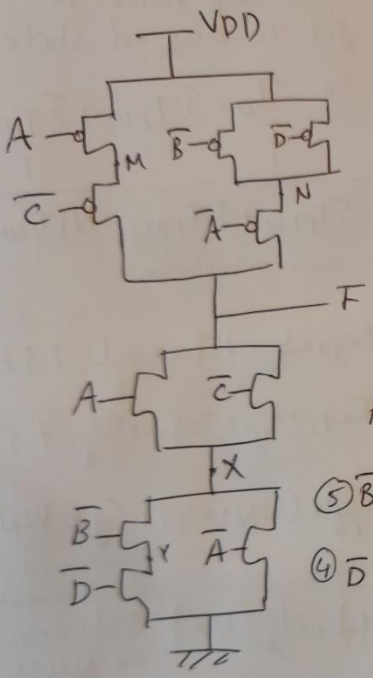
4. Implement the function A.(B+D)+C.A_bar using CMOS static logic to minimize worst-case delay knowing that input "C" is the latest arriving signal and show the stick diagram layout (no break in diffusion – no sizing required)(6pts).

$$F = A(B+D) + C\bar{A}$$

$$\bar{F} = \overline{A(B+D)} \cdot \overline{(C\bar{A})}$$

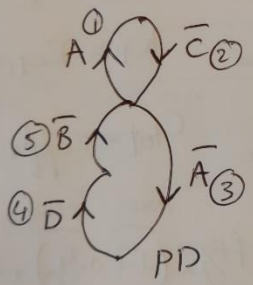
$$= (\bar{A} + \bar{B}\bar{D}) \cdot (A + \bar{C})$$

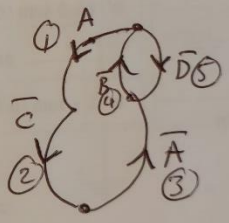
⇐ C late arrival, keep it close to the output



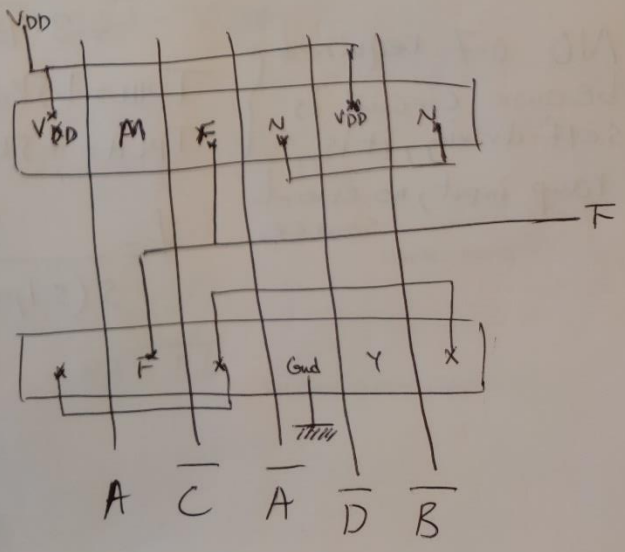
One Euler path is

$A\bar{C}\bar{A}\bar{D}\bar{B}$



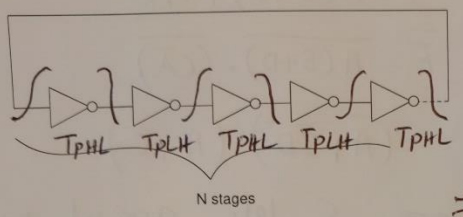


There are other possible Euler path such as $\bar{A}CA\bar{B}\bar{D}$, etc...



N=5

5. If the rise and fall propagation delay for the inverters in the following figure are different and denoted by T_{PHL} and T_{PLH}, respectively, what is the frequency of oscillation for the ring oscillator with "N" inverters in the loop? (3pts)

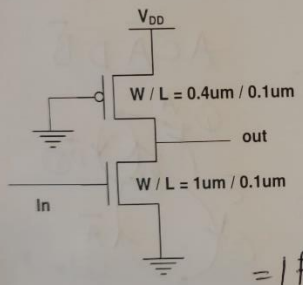


It has to go through the loop twice to get to original state

so $T_D = 5T_{PHL} + 5T_{PLH}$

$$f = \frac{1}{5T_{PLH} + 5T_{PHL}} = \frac{1}{N(T_{PLH} + T_{PHL})}$$

Calculate the frequency of oscillation if each inverter is built as shown below (6pts).



$$R_{PD} = R_{eqn} \times \frac{L}{W} = 15k\Omega \times \frac{0.1}{1} = 1.5k\Omega$$

$$R_{PU} = R_{eqp} \times \frac{L}{W} = 30k\Omega \times \frac{0.1}{0.4} = 7.5k\Omega$$

$$C_{tot} = C_{eff} \times (W_N + W_P) + C_g \times W_N$$

NMOS PMOS — each inverter only drives an NMOS

$$= 1fF/\mu m\left(1\mu + 0.4\mu\right) + 2fF/\mu\left(1\mu\right)$$

$$= 3.4fF$$

NO 0.7 required because circuit is self driving, it is ramp input, no external source

$$T_{PHL} = 1.5k\Omega \times 3.4fF = 5.1ps$$

$$T_{PLH} = 7.5k\Omega \times 3.4fF = 25.5ps$$

$$f = \frac{1}{5(5.1ps + 25.5ps)} \approx 6.53GHz$$