ELEC 402

Design of CMOS Inverter

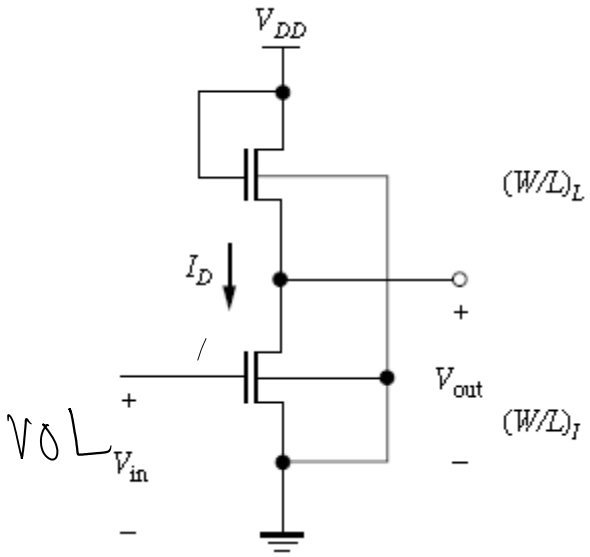
(Noise-margin-centric approach)

Lecture 7

Reza Molavi
Dept. of ECE
University of British Columbia
reza@ece.ubc.ca

Slides Courtesy : Dr. Res Saleh (UBC), Dr. D. Sengupta (AMD), Prof. B. Razavi (UCLA)

Saturated-enhancement-load Inverter



To alleviate the area problem we replace the resistor

With a diode-connected transistor (always in saturation)

This performance of this logic gate is affected by the ratio

Of devices, hence called *ratioed* inverter

$$K_R = \frac{k_{\text{invert}}}{k_{\text{load}}} = \frac{k'(W/L)_I}{k'(W/L)_L} = \frac{(W/L)_I}{(W/L)_L}$$

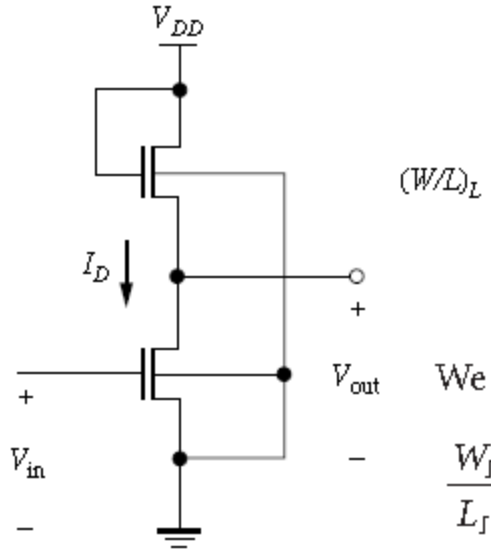
The output voltage does not quite reach V_{DD}

(The Load device requires at least VT drop on its V_{GS})

$$V_{OH} = V_{DD} - V_T(V_{OH})$$

$$= V_{DD} - [V_{T0} + \gamma(\sqrt{V_{OH} + 2|\phi_F|} - \sqrt{2|\phi_F|})]$$

Saturated-enhancement-load Inverter – cont'd



To derive the V_{OL} again it is important to find the proper region of operation for each transistor

$$I_{DI}(\text{lin}) = I_{DL}(\text{sat})$$

We can substitute in the current equations to obtain

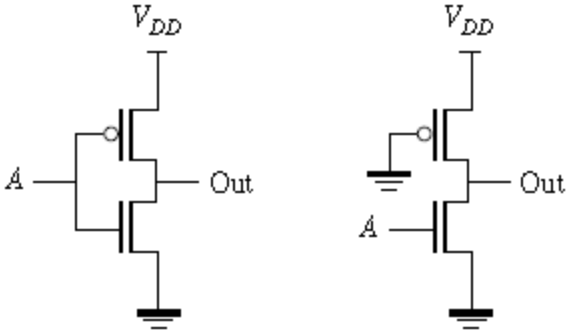
$$\frac{W_I}{L_I}\frac{\mu_n C_{ox}}{\left(1+\frac{V_{out}}{E_{CN}L_I}\right)}\left[(V_{in}-V_{TI})V_{out}-\frac{V_{out}^2}{2}\right]=\frac{W_L v_{sat} C_{ox}(V_{DD}-V_{out}-V_{TL})^2}{(V_{DD}-V_{out}-V_{TL})+E_{CN}L_L}$$

Note that V_{in} should be the output of previous stage (ideally $V_{DD} – V_T$), however, to keep Things simple we occasionally assume $V_{in} = V_{DD}$

Pseudo-NMOS Inverter

To address issues with NMOS loads

- Saturated NMOS load, a.k.a diode connected load, has degraded V_{OH}
- Linear NMOS load requires two supplies and extra area/interconnects
- CMOS gates require multiple loads for multi fanin inputs (?)



Solves the abovementioned problems, However

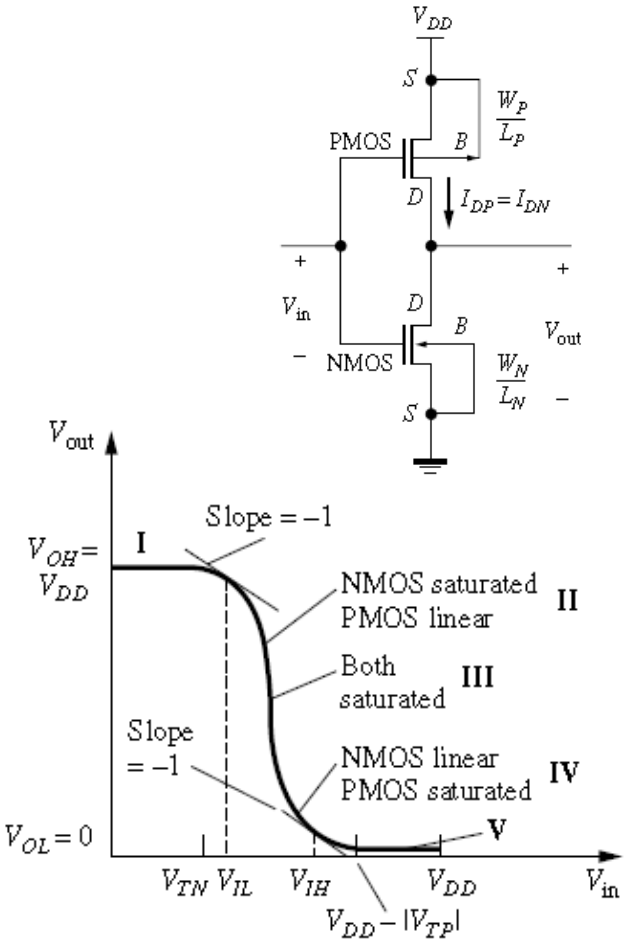
-*Ratioed* inverter, i.e. V_{OL} a function of two device ratios

- Large T_{PLH} (why?)

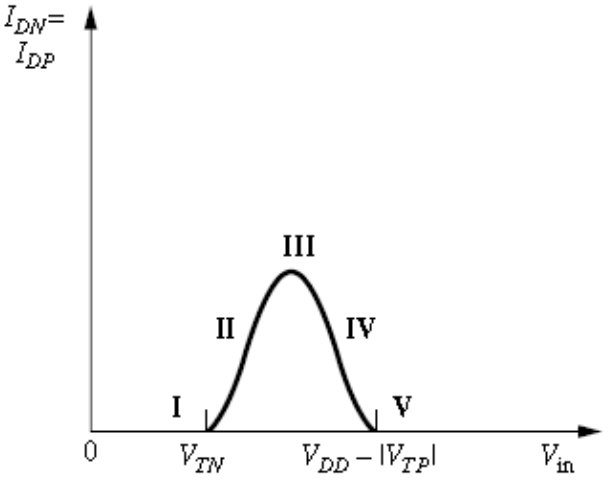
$$I_{DP}(\text{sat}) = I_{DN}(\text{lin})$$

$$\frac{W_P v_{sat} C_{ox}(V_{DD} - |V_{TP}|)^2}{(V_{DD} - |V_{TP}|) + E_{CP}L_P} = \frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1 + \frac{V_{OL}}{E_{CN}L_N}\right)}\left[(V_{DD} - V_{TN})(V_{OL}) - \frac{(V_{OL})^2}{2}\right] \Rightarrow V_{OL} = \frac{I_{DP}(\text{sat})}{k_N(V_{DD} - V_{TN})}$$

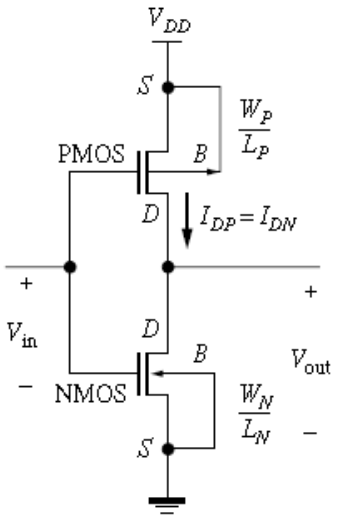
CMOS Inverter



- Address both issues of area and static power consumption
- Load that is complementary to the inverting device
- 5 distinct regions of operation can be detected



CMOS Inverter



Region II: NMOS saturation, PMOS Linear

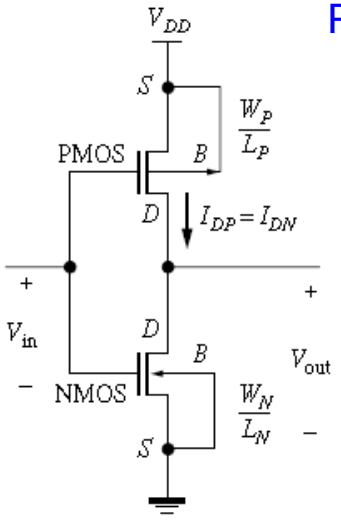
V_{IL} falls in this region (why?)

$$\frac{W_N \mu_{sat} C_{ox} (V_{in} - V_{TN})^2}{(V_{in} - V_{TN}) + E_{CN} L_N} = \frac{W_P}{L_P} \frac{\mu_p C_{ox}}{\left(1 + \frac{V_{DD} - V_{out}}{E_{CP} L_P}\right)}$$

$$\times \left[(V_{DD} - V_{in} - |V_{TP}|)(V_{DD} - V_{out}) - \frac{(V_{DD} - V_{out})^2}{2} \right]$$

$$V_{IL} = \frac{2V_{out} - V_{DD} - |V_{TP}| + (k_N/k_P)(V_{TN})}{1 + (k_N/k_P)}$$

CMOS Inverter – Switching Point



Region III: NMOS saturation, PMOS saturation

V_S falls in this region (why?)

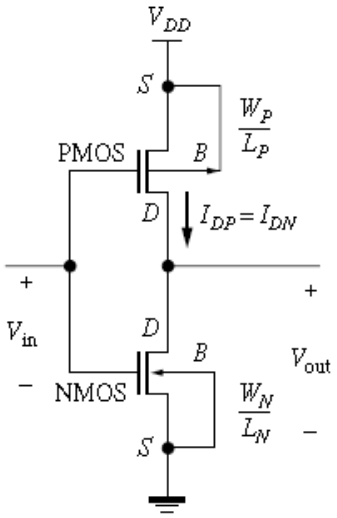
$$\frac{W_N \upsilon_{sat} C_{ox}(V_S - V_{TN})^2}{(V_S - V_{TN}) + E_{CN} L_N} = \frac{W_P \upsilon_{sat} C_{ox}(V_{DD} - V_S - |V_{TP}|)^2}{(V_{DD} - V_S - |V_{TP}|) + E_{CP} L_P}$$

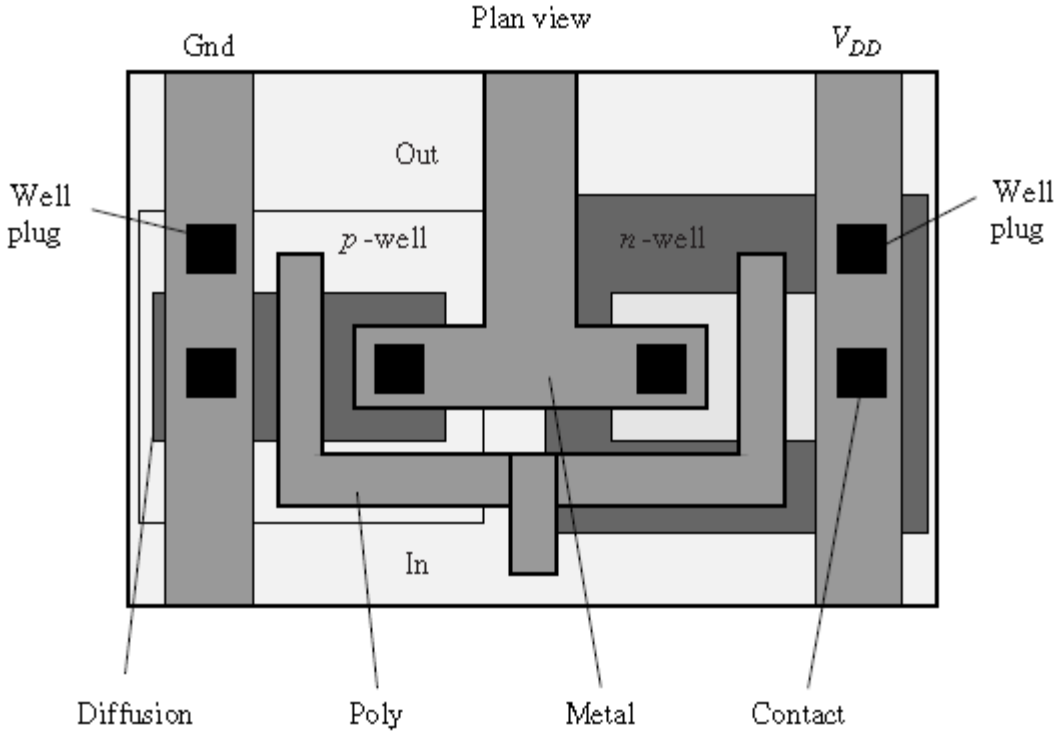
(Board Discussion)

$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1 + \chi}$$

$$\chi = \sqrt{\frac{\frac{W_N}{E_{CN} L_N}}{\frac{W_P}{E_{CP} L_P}}} = \sqrt{\frac{\mu_n W_N}{\mu_p W_P}}$$

CMOS Inverter - Layout





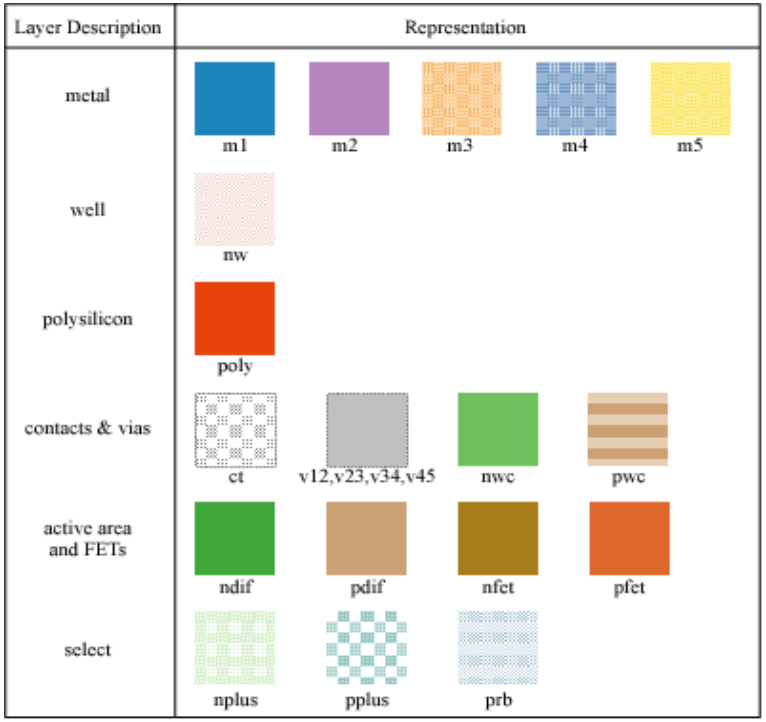
Note Minimum size, well-plugs, design rules

Design Rules

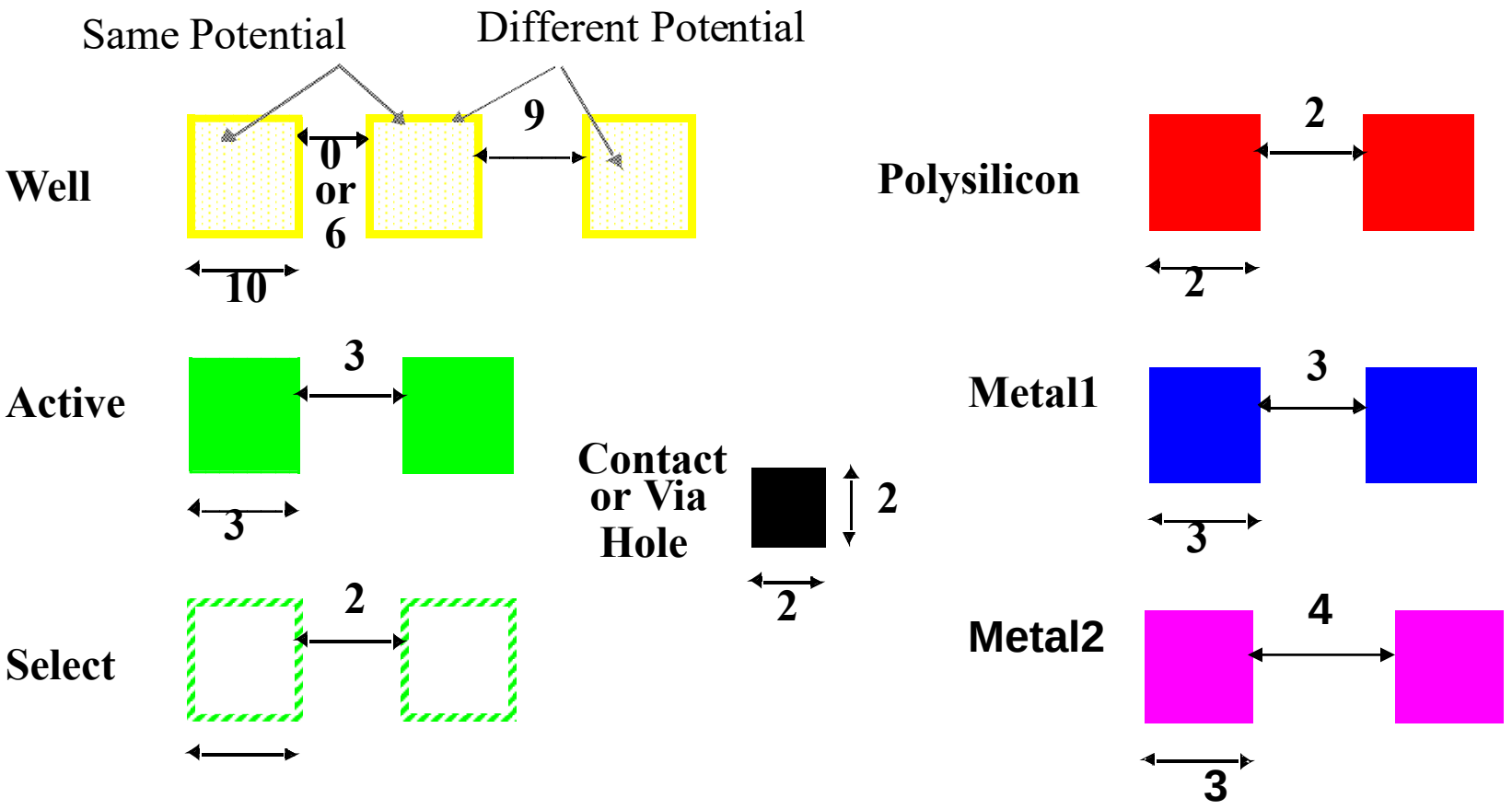
- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum

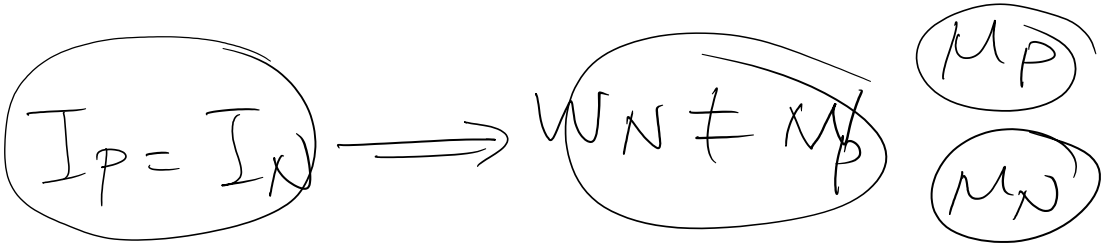
  line width

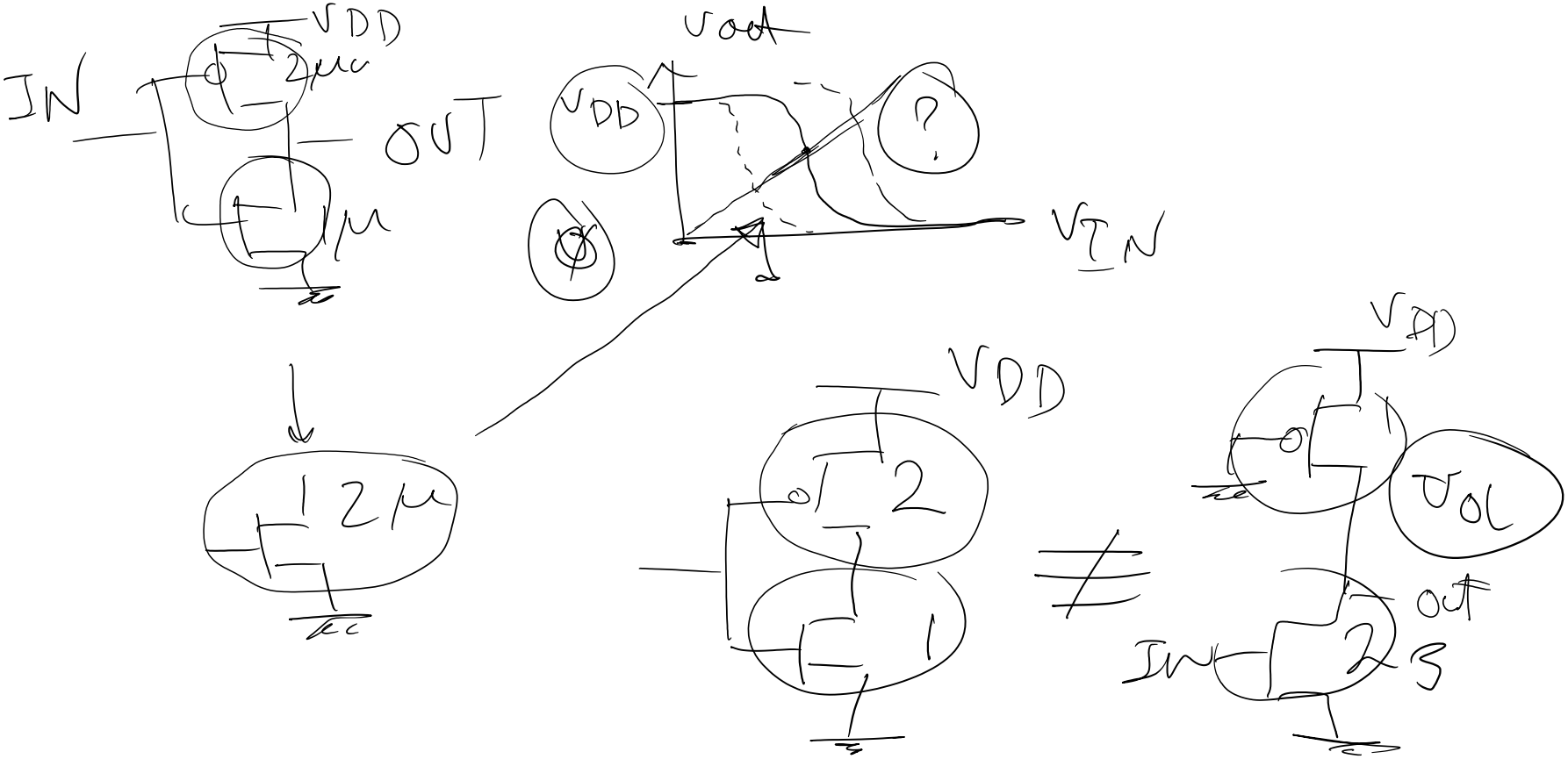
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)



DRC Rules - II


Same Potential
Different Potential
Well
0
or
6
9
10
Polysilicon
2
2
Active
3
3
Contact
or Via
Hole
2
2
Metal1
3
3
Select
2
Metal2
4
3


$I_P = I_N$
$W_N \neq W_P$
μ_P
μ_N


VDD
IN
2μ
OUT
1μ
VDD
?
V_{TN}
1
2μ
VDD
2
1
VDD
1
V_{OL}
out
IN
2
3