ELEC 402

Project 2 Report

Synthesized Version of Project 1;
https://github.com/mchuahua/ELEC402/tree/master/Proj2

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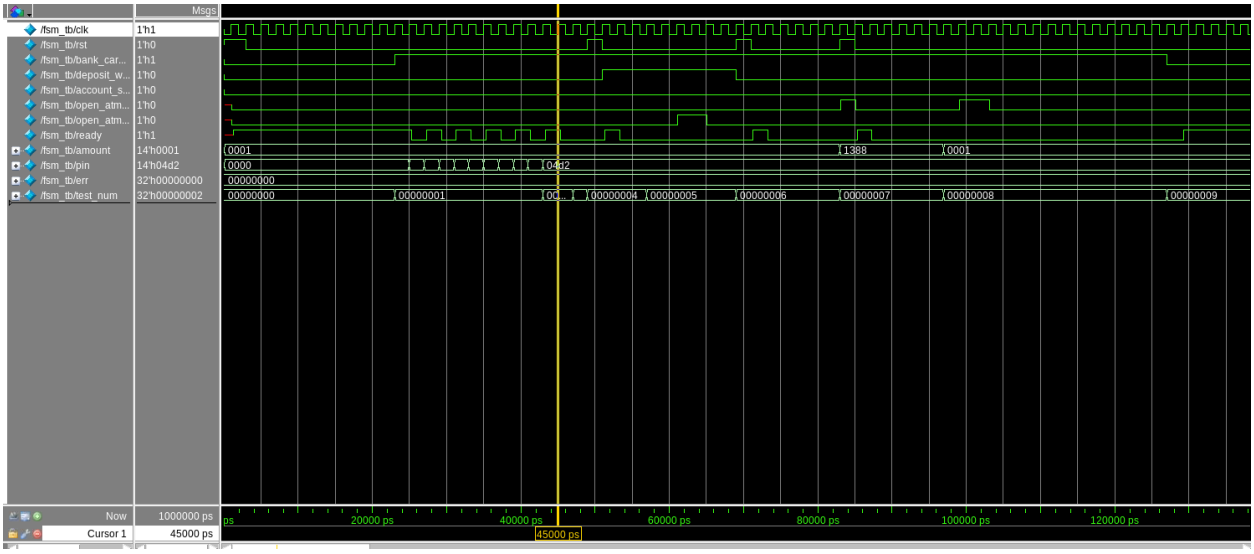
Mapped Verilog generated by RTL Compiler

See ./fsm_map.v (or appendix A)

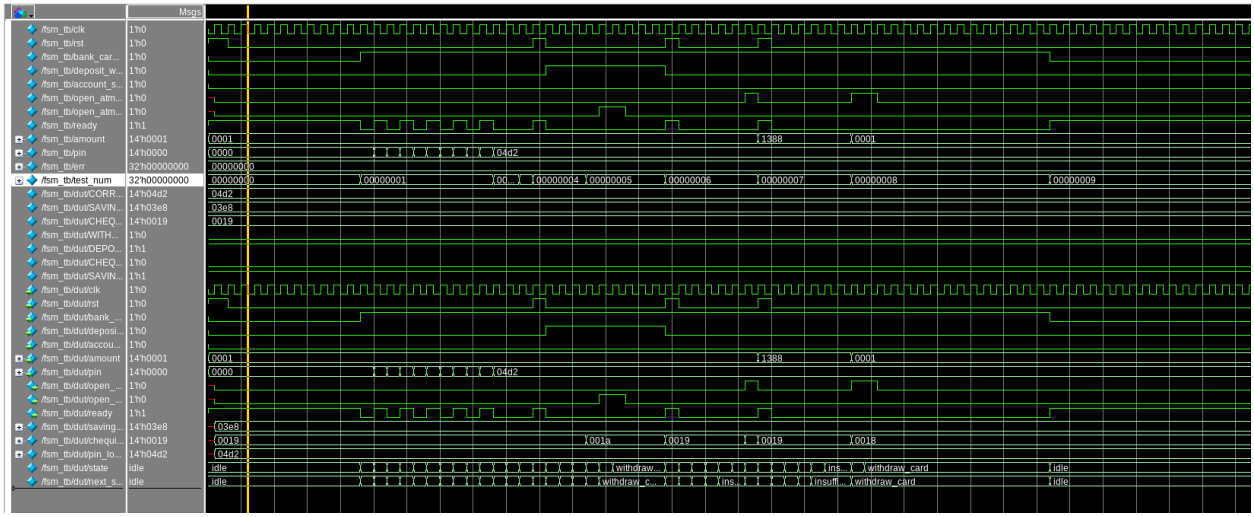
Visual Waveforms showing state transitions from mapped Verilog:

As the synthesized mapped Verilog doesn't contain enum from the Proj1 testbench, it was decided that in order to verify the state transitions, the simplest method would be to utilize a visual comparison between the Proj1 waveforms and Proj2 waveforms. This was also the easiest method to confirm the state transitions, as the output/input signals of the DUT depend on the states and state transitions. Therefore, although assertions were not used in the Proj2 tb, just by having the waveforms match (disregarding delay) means that the state transitions also match, and work correctly.

Below is the waveform for the mapped Verilog (first):



And below is the Proj1 waveform with verifiable states:



There are various signals to note that will be listed below. One major point is that the Ready signal is asserted when state is in IDLE. The test_num signal can also allow the user to glean information about what is happening. To explain why this is possible:

1. Test num 0 is in IDLE. Ready is asserted. This is correct.
2. Test num 1 sees that ready is asserted and deasserted, as it transitions back and forth due to invalid PIN (0-9). This is correct.
3. Test num 2 sees that after a valid PIN, state should not be in IDLE. This is correct. If it wasn't the ready signal should be asserted just as in test_num 1.
4. Test num 3 sees that withdrawal (0) makes FSM go to the correct state. Seeing that ready isn't asserted, the state is not in IDLE and is proceeding along.
5. Test num 4 sees that reset works and if deposit (1) goes to correct state. Notice that the two waveforms are the same (albeit Proj2 waveform has delay). Therefore the deposit states are correctly being transitioned to.
6. Test num 5 checks to see if deposited correct. Notice the open atm output is being correctly triggered in the proj 2 waveform, matching the proj 1 waveform.
7. Test num 6 checks to see if reset + withdrawal was correct. Again, both waveforms match. At the end of test num 6, we see the open_atm_dispense was triggered properly, just as in proj 1 waveform. This suggests that the withdrawal states are correctly being transitioned to.
8. The next three tests can be understood by understanding the state functionality. The state for looping an amount check is before the state for looping the withdraw card check, which then goes to IDLE if card is withdrawn. Notice in test num 7 the input amount is changed. This should trigger a loop, as there are insufficient funds. This matches proj1 waveform. Now, if we change the input amount back to 1, the state should continue along and wait for the bank card to be withdrawn. In test num 8, the card is never withdrawn, and our waveforms match. Likewise, the bank card is then withdrawn, and in test num 9 we see Ready being asserted, indicating that we are indeed in IDLE.

Report from RTL Compiler showing total number of cells in project

See ./fsm_area.rpt

```
1  ====================================================================
2    Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
3    Generated on:           Oct 06 2021  08:48:08 pm
4    Module:                 fsm
5    Technology library:     NanGate_15nm_OCL revision 1.0
6    Operating conditions:   worst_low (balanced_tree)
7    Wireload mode:          enclosed
8    Area mode:              timing library
9  ====================================================================
10
11 Instance  Cells  Cell Area  Net Area  Total Area  Wireload
12 --------------------------------------------------------------------
13 fsm         463        153         0         153    <none> (D)
14
15  (D) = wireload is default in technology library
```

Seems as expected; passing above minimum threshold requirement of 100 cells. Expected to be relatively larger than 100 cells because FSM was slightly above trivial (10+ states, various state transitions), as well as the amount of logic statements used (regs/wires).

See ./fsm_timing.rpt

```
  Generated By:            Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:            Oct 06 2021  08:48:08 pm
  Module:                  fsm
  Technology library:      NanGate_15nm_OCL revision 1.0
  Operating conditions:    worst_low (balanced_tree)
  Wireload mode:           enclosed
  Area mode:               timing library
============================================================

          Pin               Type      Fanout Load Slew Delay Arrival
                                             (fF) (ps)  (ps)   (ps)
-------------------------------------------------------------------------
(clock clk)               launch                                    0 R
savings_local_reg[0]/CLK                                 0          0 R
savings_local_reg[0]/Q    DFFSNQ_X1       3  2.6    5   +15       15 F
g12742/A1                                              +0       15
g12742/ZN                 NOR2_X1         3  3.8   12    +8       23 R
g12691/A1                                              +0       23
g12691/ZN                 OAI21_X1        2  2.5    8    +7       30 F
g12667/A1                                              +0       30
g12667/ZN                 AOI22_X1        2  2.5   10    +8       39 R
g12652/A1                                              +0       39
g12652/ZN                 OAI21_X1        2  2.3    8    +6       45 F
g12639/A1                                              +0       45
g12639/ZN                 AOI21_X1        2  2.5    9    +7       52 R
g12631/A1                                              +0       52
g12631/ZN                 OAI21_X1        2  2.3    8    +6       59 F
g12627/B                                               +0       59
g12627/ZN                 OAI21_X1        1  1.0    5    +5       64 R
g12620/B                                               +0       64
g12620/ZN                 OAI21_X1        2  2.3    7    +6       70 F
g12610/A1                                              +0       70
g12610/ZN                 AOI22_X1        2  2.5   10    +8       78 R
g12601/A1                                              +0       78
g12601/ZN                 OAI22_X1        2  2.3    8    +7       85 F
g12591/A1                                              +0       85
g12591/ZN                 AOI22_X1        2  2.5   10    +8       93 R
g12582/A1                                              +0       93
g12582/ZN                 OAI21_X1        2  2.3    8    +6       99 F
g12574/A1                                              +0       99
g12574/ZN                 AOI22_X1        2  2.5   10    +8      107 R
g12565/A1                                              +0      107
g12565/ZN                 OAI22_X1        2  1.6    7    +6      113 F
g12557/A1                                              +0      113
g12557/ZN                 OAI22_X1        2  2.0    9    +6      120 R
g12555/A2                                              +0      120
g12555/Z                  OR3_X2          3  3.1    4    +8      128 R
g12550/A2                                              +0      128
g12550/ZN                 NOR2_X1         7  6.2   10    +7      135 F
g12535/A1                                              +0      135
g12535/ZN                 NOR2_X1         7  7.1   21   +14      149 R
g12534/I                                               +0      149
g12534/ZN                 INV_X1          2  1.7    7    +6      155 F
g12511/A1                                              +0      155
g12511/ZN                 NAND2_X1        1  0.9    3    +4      159 R
g12461/B1                                              +0      159
g12461/ZN                 AOI22_X1        1  0.8    5    +4      163 F
g12433/A1                                              +0      163
g12433/ZN                 NOR2_X1         1  0.6    4    +3      166 R
savings_local_reg[0]/D    DFFSNQ_X1                    +0      166
savings_local_reg[0]/CLK  setup                        0    +8    175 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)               capture                                 500 R
-------------------------------------------------------------------------
Cost Group   : 'clk' (path_group 'clk')
Timing slack :     325ps
Start-point  : savings_local_reg[0]/CLK
End-point    : savings_local_reg[0]/D
```

Timing slack is positive, which is good. Initial following according to the tutorial document gave a timing slack of 1ps, but after following Sean's advice on piazza on how to change the timing unit, the slack increased. This is good because it allows more leeway for signals to propagate.

See ./fsm_gates.rpt

```
====================================================================
  Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:           Oct 06 2021  08:48:08 pm
  Module:                 fsm
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   worst_low (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================


   Gate    Instances   Area         Library
------------------------------------------------
AND2_X1            4    1.180    NanGate_15nm_OCL
AND3_X1            1    0.393    NanGate_15nm_OCL
AOI21_X1          13    3.834    NanGate_15nm_OCL
AOI22_X1          39   13.418    NanGate_15nm_OCL
DFFSNQ_X1         34   43.450    NanGate_15nm_OCL
HA_X1              1    0.639    NanGate_15nm_OCL
INV_X1            81   11.944    NanGate_15nm_OCL
NAND2_X1         114   22.413    NanGate_15nm_OCL
NAND3_X1           2    0.590    NanGate_15nm_OCL
NAND4_X1           8    2.753    NanGate_15nm_OCL
NOR2_X1           51   10.027    NanGate_15nm_OCL
NOR3_X1            2    0.590    NanGate_15nm_OCL
NOR4_X1            2    0.688    NanGate_15nm_OCL
OAI21_X1          41   12.091    NanGate_15nm_OCL
OAI22_X1          12    4.129    NanGate_15nm_OCL
OR2_X1             7    2.064    NanGate_15nm_OCL
OR3_X2             1    0.393    NanGate_15nm_OCL
XNOR2_X1           9    3.981    NanGate_15nm_OCL
XOR2_X1           41   18.137    NanGate_15nm_OCL
------------------------------------------------
total            463  152.715


   Type    Instances   Area  Area %
-----------------------------------
sequential        34  43.450   28.5
inverter          81  11.944    7.8
logic            348  97.321   63.7
-----------------------------------
total            463 152.715  100.0
```

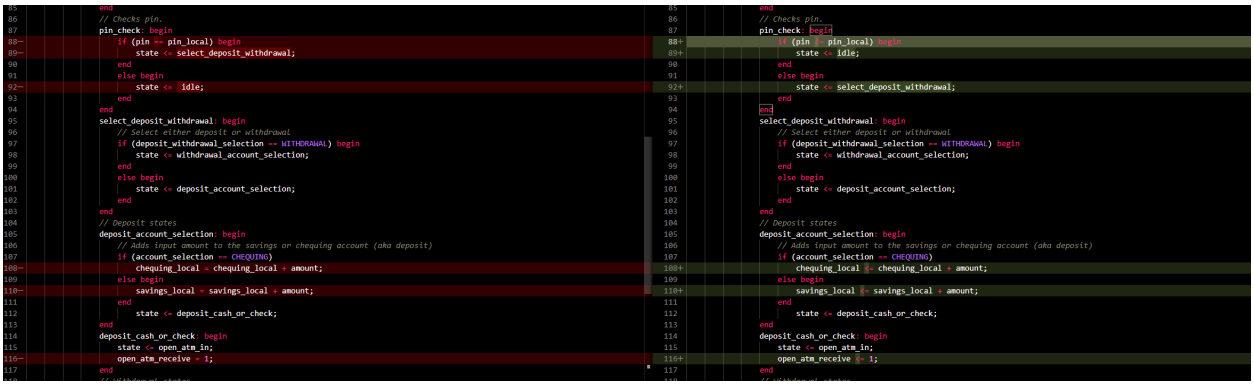
This is expected and matches expectations. NAND and NOR should be the highest because they are considered as universal gates and are easier and more economical to fabricate. There is more logic instances than sequential or inverter because Cadence is able to optimize some of the unused sequential logic to logic constants (LUTs). This effectively reduces power (for propagating unnecessary

buses) and reduces size of area that might otherwise be used. Additionally, the AOI (AND-OR-Invert) gates are used as complex gates can be more efficiently built than discrete representations, as the discrete representation is usually more expensive in cost and slower in propagation time from input to output.

Changed Designs from Project 1

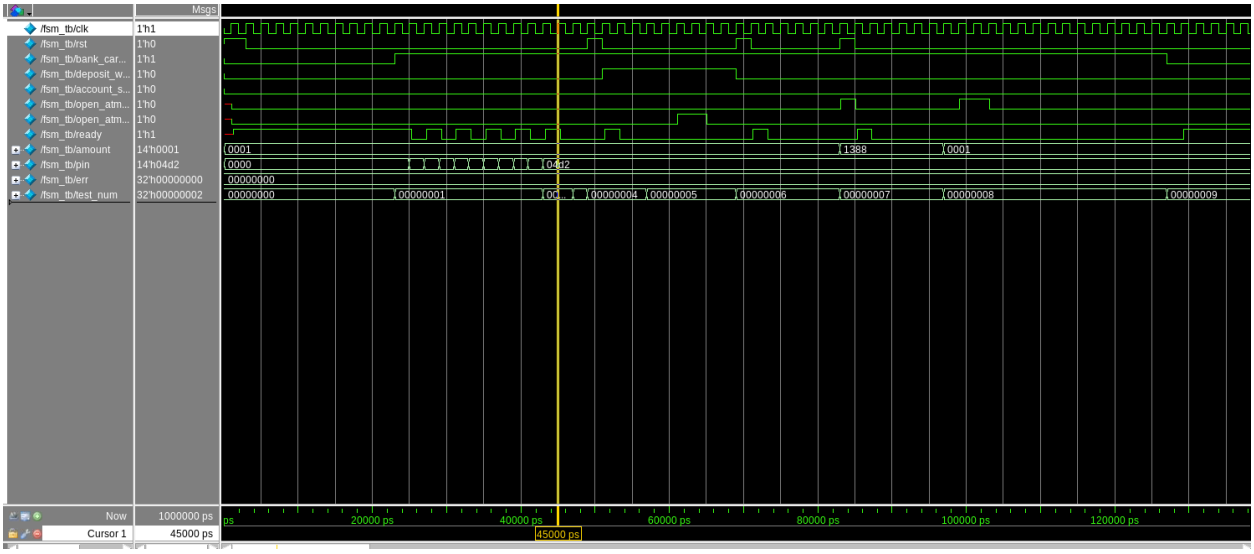
For testbench, all assertions were commented out. This can be seen in fsm_tb.sv.

For fsm, 2 small changes were made:

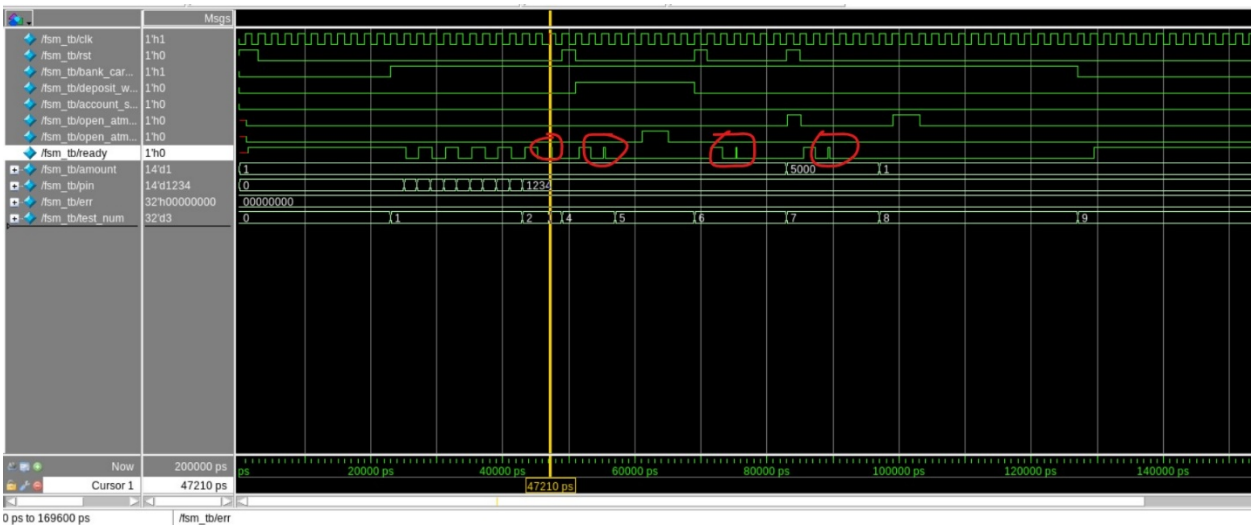


1. Last three coloured lines were fixes to allow the system Verilog to be able to be synthesized. Blocking assignments were incorrectly used (typo) instead of non-blocking, as it is a sequential logic block rather than combinational.
2. First three coloured lines switched to allow correct functionality in waveform. See below:

Working with fixes mentioned above:



Not working without fixes:



Without the fixes, as indicated by the red circles there were some unintended assertions of the ready signal. From intuition and clarifying with the TA, it turns out that using the "==" produces a longer enough propagation time (cascading transistor delay) in comparison to "!=" such that the states are not propagating fast enough for the state machine to function correctly. And as such the bits that correspond to the correct state are not being flipped fast enough, causing this spike as ready is being incorrectly asserted.

Alternatively, this could also suggest that rather than changing the code, the clock period may also be increased, although this has not been attempted as the fix has worked.

Appendix A – fsm_map.v code

```
// Generated by Cadence Encounter(R) RTL Compiler RC14.13 -
v14.10-s027_1

// Verification Directory fv/fsm

module fsm(clk, rst, bank_card_insert,
deposit_withdrawal_selection,
    account_selection, amount, pin, open_atm_dispense,
    open_atm_receive, ready);
 input clk, rst, bank_card_insert, deposit_withdrawal_selection,
     account_selection;
 input [13:0] amount, pin;
 output open_atm_dispense, open_atm_receive, ready;
 wire clk, rst, bank_card_insert, deposit_withdrawal_selection,
     account_selection;
 wire [13:0] amount, pin;
 wire open_atm_dispense, open_atm_receive, ready;
 wire [13:0] savings_local;
 wire [13:0] chequing_local;
 wire [31:0] state;
 wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
 wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
 wire n_16, n_17, n_18, n_19, n_20, n_21, n_22, n_23;
 wire n_24, n_25, n_26, n_27, n_28, n_29, n_30, n_31;
 wire n_32, n_33, n_34, n_35, n_36, n_37, n_38, n_39;
 wire n_40, n_41, n_42, n_43, n_44, n_45, n_46, n_47;
 wire n_48, n_49, n_50, n_51, n_52, n_53, n_54, n_55;
 wire n_56, n_57, n_58, n_59, n_60, n_61, n_62, n_63;
 wire n_64, n_65, n_66, n_67, n_68, n_69, n_70, n_71;
 wire n_72, n_73, n_74, n_75, n_76, n_77, n_78, n_79;
 wire n_80, n_81, n_82, n_83, n_84, n_85, n_86, n_87;
 wire n_88, n_89, n_90, n_91, n_92, n_93, n_94, n_95;
 wire n_96, n_97, n_98, n_99, n_100, n_101, n_102, n_103;
 wire n_104, n_105, n_106, n_107, n_108, n_109, n_110, n_111;
 wire n_112, n_113, n_114, n_115, n_116, n_117, n_118, n_119;
 wire n_120, n_121, n_122, n_123, n_124, n_125, n_126, n_127;
 wire n_128, n_129, n_130, n_132, n_133, n_134, n_135, n_136;
 wire n_137, n_138, n_139, n_140, n_141, n_142, n_143, n_144;
 wire n_145, n_146, n_147, n_148, n_149, n_150, n_151, n_152;
 wire n_153, n_154, n_155, n_156, n_157, n_158, n_159, n_160;
 wire n_161, n_162, n_163, n_164, n_165, n_166, n_167, n_168;
 wire n_169, n_170, n_171, n_172, n_173, n_174, n_175, n_176;
 wire n_177, n_178, n_179, n_180, n_181, n_182, n_183, n_184;
 wire n_185, n_186, n_187, n_188, n_189, n_190, n_191, n_192;
 wire n_193, n_194, n_195, n_196, n_197, n_198, n_199, n_200;
 wire n_201, n_202, n_203, n_204, n_205, n_206, n_207, n_208;
 wire n_209, n_210, n_211, n_212, n_213, n_214, n_215, n_216;
 wire n_217, n_218, n_219, n_220, n_221, n_222, n_223, n_224;
 wire n_225, n_226, n_227, n_228, n_229, n_230, n_231, n_232;
 wire n_233, n_234, n_235, n_236, n_237, n_238, n_239, n_240;
 wire n_241, n_242, n_243, n_244, n_245, n_246, n_247, n_248;
 wire n_249, n_250, n_251, n_252, n_253, n_254, n_255, n_256;
 wire n_257, n_258, n_259, n_260, n_261, n_262, n_263, n_264;
```

```
  wire n_265, n_266, n_267, n_268, n_269, n_270, n_271, n_272;
  wire n_273, n_274, n_275, n_276, n_277, n_278, n_279, n_280;
  wire n_281, n_282, n_283, n_284, n_285, n_286, n_287, n_288;
  wire n_289, n_290, n_291, n_292, n_293, n_294, n_295, n_296;
  wire n_297, n_298, n_299, n_300, n_301, n_302, n_303, n_304;
  wire n_305, n_306, n_307, n_308, n_309, n_310, n_311, n_312;
  wire n_313, n_314, n_315, n_316, n_317, n_318, n_319, n_320;
  wire n_321, n_322, n_323, n_324, n_325, n_326, n_327, n_328;
  wire n_329, n_330, n_331, n_332, n_333, n_334, n_335, n_336;
  wire n_337, n_338, n_339, n_340, n_341, n_342, n_343, n_344;
  wire n_345, n_346, n_347, n_348, n_349, n_350, n_351, n_352;
  wire n_353, n_354, n_355, n_356, n_357, n_358, n_359, n_360;
  wire n_361, n_362, n_363, n_364, n_365, n_366, n_367, n_368;
  wire n_369, n_370, n_371, n_372, n_373, n_374, n_375, n_376;
  wire n_377, n_378, n_379, n_380, n_381, n_382, n_383, n_384;
  wire n_385, n_386, n_387, n_388, n_389, n_390, n_391, n_392;
  wire n_393, n_394, n_395, n_396, n_397, n_398, n_399, n_400;
  wire n_401, n_402, n_403, n_404, n_405, n_406, n_407, n_408;
  wire n_409, n_410, n_411, n_412, n_413, n_414, n_415, n_416;
  wire n_417, n_418, n_419, n_420, n_421, n_422, n_423, n_424;
  wire n_425, n_426, n_427, n_428, n_430;
  DFFSNQ_X1 \savings_local_reg[0] (.SN (1'b1), .CLK (clk), .D
(n_430),
     .Q (savings_local[0]));
  NOR2_X1 g12433(.A1 (n_428), .A2 (rst), .ZN (n_430));
  DFFSNQ_X1 \chequing_local_reg[0] (.SN (1'b1), .CLK (clk), .D
(n_423),
     .Q (chequing_local[0]));
  DFFSNQ_X1 \savings_local_reg[3] (.SN (1'b1), .CLK (clk), .D
(n_427),
     .Q (savings_local[3]));
  DFFSNQ_X1 \savings_local_reg[5] (.SN (1'b1), .CLK (clk), .D
(n_426),
     .Q (savings_local[5]));
  DFFSNQ_X1 \savings_local_reg[6] (.SN (1'b1), .CLK (clk), .D
(n_424),
     .Q (savings_local[6]));
  DFFSNQ_X1 \savings_local_reg[7] (.SN (1'b1), .CLK (clk), .D
(n_422),
     .Q (savings_local[7]));
  DFFSNQ_X1 \savings_local_reg[8] (.SN (1'b1), .CLK (clk), .D
(n_421),
     .Q (savings_local[8]));
  DFFSNQ_X1 \savings_local_reg[9] (.SN (1'b1), .CLK (clk), .D
(n_420),
     .Q (savings_local[9]));
  AOI22_X1 g12461(.A1 (n_401), .A2 (n_163), .B1 (n_402), .B2
     (savings_local[0]), .ZN (n_428));
  DFFSNQ_X1 \chequing_local_reg[10] (.SN (1'b1), .CLK (clk), .D
     (n_411), .Q (chequing_local[10]));
  DFFSNQ_X1 \chequing_local_reg[5] (.SN (1'b1), .CLK (clk), .D
(n_418),
     .Q (chequing_local[5]));
  DFFSNQ_X1 \chequing_local_reg[6] (.SN (1'b1), .CLK (clk), .D
(n_417),
     .Q (chequing_local[6]));
  DFFSNQ_X1 \chequing_local_reg[7] (.SN (1'b1), .CLK (clk), .D
(n_416),
     .Q (chequing_local[7]));
  DFFSNQ_X1 \chequing_local_reg[8] (.SN (1'b1), .CLK (clk), .D
(n_415),
     .Q (chequing_local[8]));
  DFFSNQ_X1 \chequing_local_reg[9] (.SN (1'b1), .CLK (clk), .D
(n_414),
     .Q (chequing_local[9]));
  DFFSNQ_X1 \chequing_local_reg[12] (.SN (1'b1), .CLK (clk), .D
     (n_412), .Q (chequing_local[12]));
  DFFSNQ_X1 \chequing_local_reg[11] (.SN (1'b1), .CLK (clk), .D
     (n_413), .Q (chequing_local[11]));
  DFFSNQ_X1 \chequing_local_reg[1] (.SN (1'b1), .CLK (clk), .D
(n_410),
     .Q (chequing_local[1]));
  DFFSNQ_X1 \chequing_local_reg[13] (.SN (1'b1), .CLK (clk), .D
     (n_419), .Q (chequing_local[13]));
  DFFSNQ_X1 \chequing_local_reg[2] (.SN (1'b1), .CLK (clk), .D
(n_409),
     .Q (chequing_local[2]));
  NAND4_X1 g12486(.A1 (n_393), .A2 (n_347), .A3 (n_201), .A4
(n_425),
     .ZN (n_427));
  NAND4_X1 g12487(.A1 (n_392), .A2 (n_346), .A3 (n_234), .A4
(n_425),
     .ZN (n_426));
  NAND4_X1 g12488(.A1 (n_390), .A2 (n_344), .A3 (n_245), .A4
(n_425),
     .ZN (n_424));
  NAND2_X1 g12460(.A1 (n_394), .A2 (n_404), .ZN (n_423));
  NAND4_X1 g12489(.A1 (n_389), .A2 (n_343), .A3 (n_255), .A4
(n_425),
     .ZN (n_422));
  NAND4_X1 g12490(.A1 (n_388), .A2 (n_342), .A3 (n_268), .A4
(n_425),
     .ZN (n_421));
  NAND4_X1 g12491(.A1 (n_387), .A2 (n_341), .A3 (n_280), .A4
(n_425),
     .ZN (n_420));
  DFFSNQ_X1 \chequing_local_reg[4] (.SN (1'b1), .CLK (clk), .D
(n_399),
     .Q (chequing_local[4]));
  DFFSNQ_X1 \chequing_local_reg[3] (.SN (1'b1), .CLK (clk), .D
(n_400),
     .Q (chequing_local[3]));
  DFFSNQ_X1 \savings_local_reg[4] (.SN (1'b1), .CLK (clk), .D
(n_407),
     .Q (savings_local[4]));
  DFFSNQ_X1 \savings_local_reg[11] (.SN (1'b1), .CLK (clk), .D
(n_405),
     .Q (savings_local[11]));
  DFFSNQ_X1 \savings_local_reg[12] (.SN (1'b1), .CLK (clk), .D
(n_397),
     .Q (savings_local[12]));
  DFFSNQ_X1 \savings_local_reg[13] (.SN (1'b1), .CLK (clk), .D
(n_398),
     .Q (savings_local[13]));
  DFFSNQ_X1 \savings_local_reg[1] (.SN (1'b1), .CLK (clk), .D
(n_396),
     .Q (savings_local[1]));
  DFFSNQ_X1 \savings_local_reg[2] (.SN (1'b1), .CLK (clk), .D
(n_395),
     .Q (savings_local[2]));
  DFFSNQ_X1 \savings_local_reg[10] (.SN (1'b1), .CLK (clk), .D
(n_408),
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    .Q (savings_local[10]));
 INV_X1 g12465(.I (n_403), .ZN (n_419));
 NAND2_X1 g12469(.A1 (n_385), .A2 (n_371), .ZN (n_418));
 NAND2_X1 g12470(.A1 (n_382), .A2 (n_368), .ZN (n_417));
 NAND2_X1 g12471(.A1 (n_381), .A2 (n_369), .ZN (n_416));
 NAND2_X1 g12472(.A1 (n_380), .A2 (n_367), .ZN (n_415));
 NAND2_X1 g12473(.A1 (n_379), .A2 (n_366), .ZN (n_414));
 NAND2_X1 g12474(.A1 (n_378), .A2 (n_365), .ZN (n_413));
 NAND2_X1 g12475(.A1 (n_377), .A2 (n_364), .ZN (n_412));
 NAND2_X1 g12476(.A1 (n_386), .A2 (n_361), .ZN (n_411));
 NAND2_X1 g12477(.A1 (n_376), .A2 (n_363), .ZN (n_410));
 NAND2_X1 g12478(.A1 (n_375), .A2 (n_362), .ZN (n_409));
 OAI21_X1 g12484(.A1 (n_44), .A2 (n_406), .B (n_349), .ZN
(n_408));
 OAI21_X1 g12483(.A1 (n_406), .A2 (n_204), .B (n_350), .ZN
(n_407));
 OAI21_X1 g12485(.A1 (n_41), .A2 (n_406), .B (n_348), .ZN
(n_405));
 AOI21_X1 g12492(.A1 (n_340), .A2 (n_156), .B (rst), .ZN (n_404));
 AOI21_X1 g12466(.A1 (chequing_local[13]), .A2 (n_370), .B
(n_356),
    .ZN (n_403));
 NAND2_X1 g12511(.A1 (n_401), .A2 (amount[0]), .ZN (n_402));
 NAND2_X1 g12467(.A1 (n_360), .A2 (n_374), .ZN (n_400));
 NAND2_X1 g12468(.A1 (n_359), .A2 (n_372), .ZN (n_399));
 OAI21_X1 g12479(.A1 (n_98), .A2 (n_406), .B (n_357), .ZN
(n_398));
 OAI21_X1 g12480(.A1 (n_313), .A2 (n_406), .B (n_355), .ZN
(n_397));
 OAI21_X1 g12481(.A1 (n_406), .A2 (n_105), .B (n_352), .ZN
(n_396));
 OAI21_X1 g12482(.A1 (n_406), .A2 (n_32), .B (n_351), .ZN
(n_395));
 OAI21_X1 g12464(.A1 (n_373), .A2 (n_67), .B
(chequing_local[0]), .ZN
    (n_394));
 NAND2_X1 g12505(.A1 (n_391), .A2 (savings_local[3]), .ZN
(n_393));
 NAND2_X1 g12506(.A1 (n_391), .A2 (savings_local[5]), .ZN
(n_392));
 NAND2_X1 g12507(.A1 (n_391), .A2 (savings_local[6]), .ZN
(n_390));
 NAND2_X1 g12508(.A1 (n_391), .A2 (savings_local[7]), .ZN
(n_389));
 NAND2_X1 g12509(.A1 (n_391), .A2 (savings_local[8]), .ZN
(n_388));
 NAND2_X1 g12510(.A1 (n_391), .A2 (savings_local[9]), .ZN
(n_387));
 AOI22_X1 g12524(.A1 (n_384), .A2 (n_288), .B1 (n_290), .B2
(n_383),
    .ZN (n_386));
 DFFSNQ_X1 open_atm_dispense_reg(.SN (1'b1), .CLK (clk), .D
(n_338),
    .Q (open_atm_dispense));
 AOI22_X1 g12525(.A1 (n_384), .A2 (n_225), .B1 (n_227), .B2
(n_383),
    .ZN (n_385));
 DFFSNQ_X1 \state_reg[0] (.SN (1'b1), .CLK (clk), .D (n_339), .Q
    (state[0]));
 AOI22_X1 g12526(.A1 (n_384), .A2 (n_236), .B1 (n_242), .B2
(n_383),
    .ZN (n_382));
 AOI22_X1 g12527(.A1 (n_384), .A2 (n_254), .B1 (n_250), .B2
(n_383),
    .ZN (n_381));
 AOI22_X1 g12528(.A1 (n_384), .A2 (n_263), .B1 (n_265), .B2
(n_383),
    .ZN (n_380));
 AOI22_X1 g12529(.A1 (n_384), .A2 (n_273), .B1 (n_275), .B2
(n_383),
    .ZN (n_379));
 AOI22_X1 g12530(.A1 (n_384), .A2 (n_296), .B1 (n_298), .B2
(n_383),
    .ZN (n_378));
 AOI22_X1 g12531(.A1 (n_384), .A2 (n_306), .B1 (n_308), .B2
(n_383),
    .ZN (n_377));
 AOI22_X1 g12532(.A1 (n_384), .A2 (n_158), .B1 (n_383), .B2
(n_159),
    .ZN (n_376));
 AOI22_X1 g12533(.A1 (n_384), .A2 (n_176), .B1 (n_383), .B2
(n_169),
    .ZN (n_375));
 NAND2_X1 g12493(.A1 (n_373), .A2 (chequing_local[3]), .ZN
(n_374));
 NAND2_X1 g12494(.A1 (n_373), .A2 (chequing_local[4]), .ZN
(n_372));
 NAND2_X1 g12495(.A1 (n_370), .A2 (chequing_local[5]), .ZN
(n_371));
 NAND2_X1 g12496(.A1 (n_370), .A2 (chequing_local[7]), .ZN
(n_369));
 NAND2_X1 g12497(.A1 (n_370), .A2 (chequing_local[6]), .ZN
(n_368));
 NAND2_X1 g12498(.A1 (n_370), .A2 (chequing_local[8]), .ZN
(n_367));
 NAND2_X1 g12499(.A1 (n_370), .A2 (chequing_local[9]), .ZN
(n_366));
 NAND2_X1 g12500(.A1 (chequing_local[11]), .A2 (n_370), .ZN
(n_365));
 NAND2_X1 g12501(.A1 (chequing_local[12]), .A2 (n_370), .ZN
(n_364));
 NAND2_X1 g12502(.A1 (n_370), .A2 (chequing_local[1]), .ZN
(n_363));
 NAND2_X1 g12503(.A1 (n_370), .A2 (chequing_local[2]), .ZN
(n_362));
 NAND2_X1 g12504(.A1 (chequing_local[10]), .A2 (n_370), .ZN
(n_361));
 AOI21_X1 g12514(.A1 (n_358), .A2 (n_197), .B (n_207), .ZN
(n_360));
 AOI21_X1 g12515(.A1 (n_358), .A2 (n_213), .B (n_228), .ZN
(n_359));
 AOI22_X1 g12516(.A1 (n_354), .A2 (n_318), .B1 (n_323), .B2
(n_353),
    .ZN (n_357));
 OAI22_X1 g12517(.A1 (n_334), .A2 (n_320), .B1 (n_321), .B2
(n_182),
    .ZN (n_356));
 AOI22_X1 g12518(.A1 (n_354), .A2 (n_311), .B1 (n_312), .B2
(n_353),
    .ZN (n_355));
 AOI22_X1 g12519(.A1 (n_354), .A2 (n_164), .B1 (n_162), .B2
(n_353),
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    .ZN (n_352));
 AOI22_X1 g12520(.A1 (n_354), .A2 (n_174), .B1 (n_172), .B2
(n_353),
    .ZN (n_351));
 AOI22_X1 g12521(.A1 (n_354), .A2 (n_211), .B1 (n_215), .B2
(n_353),
    .ZN (n_350));
 AOI22_X1 g12522(.A1 (n_354), .A2 (n_283), .B1 (n_285), .B2
(n_353),
    .ZN (n_349));
 AOI22_X1 g12523(.A1 (n_354), .A2 (n_300), .B1 (n_293), .B2
(n_353),
    .ZN (n_348));
 INV_X1 g12534(.I (n_391), .ZN (n_401));
 NAND2_X1 g12536(.A1 (n_345), .A2 (n_194), .ZN (n_347));
 NAND2_X1 g12537(.A1 (n_345), .A2 (n_220), .ZN (n_346));
 NAND2_X1 g12538(.A1 (n_345), .A2 (n_238), .ZN (n_344));
 NAND2_X1 g12539(.A1 (n_345), .A2 (n_252), .ZN (n_343));
 NAND2_X1 g12540(.A1 (n_345), .A2 (n_260), .ZN (n_342));
 NAND2_X1 g12541(.A1 (n_345), .A2 (n_277), .ZN (n_341));
 INV_X1 g12543(.I (n_373), .ZN (n_340));
 NAND2_X1 g12512(.A1 (n_337), .A2 (n_187), .ZN (n_339));
 NAND2_X1 g12513(.A1 (n_337), .A2 (n_181), .ZN (n_338));
 NOR2_X1 g12535(.A1 (n_345), .A2 (n_279), .ZN (n_391));
 OAI22_X1 g12544(.A1 (state[0]), .A2 (n_336), .B1 (n_332), .B2
    (n_335), .ZN (n_373));
 AOI22_X1 g12545(.A1 (n_331), .A2 (n_333), .B1 (n_186), .B2
(n_166),
    .ZN (n_406));
 OAI22_X1 g12546(.A1 (n_336), .A2 (n_330), .B1 (n_216), .B2
(n_335),
    .ZN (n_370));
 INV_X1 g12548(.I (n_334), .ZN (n_384));
 NAND4_X1 g12542(.A1 (n_143), .A2 (n_328), .A3 (n_326), .A4
(n_333),
    .ZN (n_337));
 AND2_X1 g12547(.A1 (n_332), .A2 (n_336), .Z (n_358));
 NAND2_X1 g12549(.A1 (n_336), .A2 (n_333), .ZN (n_334));
 NOR2_X1 g12550(.A1 (state[0]), .A2 (n_331), .ZN (n_345));
 NOR2_X1 g12551(.A1 (n_331), .A2 (n_330), .ZN (n_354));
 NOR3_X1 g12554(.A1 (n_329), .A2 (n_325), .A3
(account_selection), .ZN
    (n_336));
 OR3_X2 g12555(.A1 (n_329), .A2 (n_327), .A3 (n_324), .Z
(n_331));
 NAND2_X1 g12552(.A1 (n_327), .A2 (account_selection), .ZN
(n_328));
 NAND2_X1 g12553(.A1 (n_325), .A2 (n_324), .ZN (n_326));
 XOR2_X1 g12558(.A1 (n_315), .A2 (n_316), .Z (n_323));
 OAI22_X1 g12556(.A1 (n_319), .A2 (n_111), .B1
(chequing_local[13]),
    .B2 (n_322), .ZN (n_325));
 OAI22_X1 g12557(.A1 (n_317), .A2 (n_73), .B1
(savings_local[13]), .B2
    (n_322), .ZN (n_327));
 XNOR2_X1 g12559(.A1 (n_314), .A2 (n_144), .ZN (n_321));
 NAND2_X1 g12560(.A1 (n_319), .A2 (n_145), .ZN (n_320));
 AND2_X1 g12561(.A1 (n_317), .A2 (n_316), .Z (n_318));
 OAI21_X1 g12563(.A1 (n_303), .A2 (n_125), .B (n_47), .ZN
(n_315));
 AOI22_X1 g12562(.A1 (n_307), .A2 (n_21), .B1
(chequing_local[12]),
    .B2 (amount[12]), .ZN (n_314));
 OAI21_X1 g12564(.A1 (n_305), .A2 (n_80), .B (n_135), .ZN
(n_319));
 OAI22_X1 g12565(.A1 (n_310), .A2 (n_36), .B1 (n_313), .B2
    (amount[12]), .ZN (n_317));
 XOR2_X1 g12566(.A1 (n_302), .A2 (n_309), .Z (n_312));
 XOR2_X1 g12567(.A1 (n_310), .A2 (n_309), .Z (n_311));
 XOR2_X1 g12568(.A1 (n_307), .A2 (n_304), .Z (n_308));
 XOR2_X1 g12569(.A1 (n_305), .A2 (n_304), .Z (n_306));
 INV_X1 g12570(.I (n_302), .ZN (n_303));
 OAI21_X1 g12571(.A1 (n_292), .A2 (n_51), .B (n_126), .ZN
(n_302));
 OAI21_X1 g12572(.A1 (n_297), .A2 (n_57), .B (n_122), .ZN
(n_307));
 AOI22_X1 g12573(.A1 (n_295), .A2 (n_27), .B1
(chequing_local[11]),
    .B2 (n_301), .ZN (n_305));
 AOI22_X1 g12574(.A1 (n_299), .A2 (n_42), .B1
(savings_local[11]), .B2
    (n_301), .ZN (n_310));
 XOR2_X1 g12575(.A1 (n_299), .A2 (n_291), .Z (n_300));
 XOR2_X1 g12576(.A1 (n_297), .A2 (n_294), .Z (n_298));
 XOR2_X1 g12577(.A1 (n_295), .A2 (n_294), .Z (n_296));
 XOR2_X1 g12578(.A1 (n_292), .A2 (n_291), .Z (n_293));
 AOI22_X1 g12579(.A1 (n_289), .A2 (n_19), .B1
(chequing_local[10]),
    .B2 (amount[10]), .ZN (n_297));
 AOI22_X1 g12580(.A1 (n_284), .A2 (n_45), .B1
(savings_local[10]), .B2
    (amount[10]), .ZN (n_292));
 OAI21_X1 g12581(.A1 (n_287), .A2 (n_109), .B (n_137), .ZN
(n_295));
 OAI21_X1 g12582(.A1 (n_282), .A2 (n_90), .B (n_134), .ZN
(n_299));
 XOR2_X1 g12583(.A1 (n_289), .A2 (n_286), .Z (n_290));
 XOR2_X1 g12584(.A1 (n_287), .A2 (n_286), .Z (n_288));
 XOR2_X1 g12585(.A1 (n_284), .A2 (n_281), .Z (n_285));
 XOR2_X1 g12586(.A1 (n_282), .A2 (n_281), .Z (n_283));
 NAND2_X1 g12587(.A1 (n_270), .A2 (n_279), .ZN (n_280));
 OAI21_X1 g12588(.A1 (n_274), .A2 (n_76), .B (n_123), .ZN
(n_289));
 OAI21_X1 g12589(.A1 (n_267), .A2 (n_121), .B (n_55), .ZN
(n_284));
 AOI22_X1 g12590(.A1 (n_272), .A2 (n_25), .B1
(chequing_local[9]), .B2
    (n_278), .ZN (n_287));
 AOI22_X1 g12591(.A1 (n_276), .A2 (n_35), .B1
(savings_local[9]), .B2
    (n_278), .ZN (n_282));
 XNOR2_X1 g12593(.A1 (n_276), .A2 (n_269), .ZN (n_277));
 XOR2_X1 g12594(.A1 (n_274), .A2 (n_271), .Z (n_275));
 XOR2_X1 g12595(.A1 (n_272), .A2 (n_271), .Z (n_273));
 XOR2_X1 g12592(.A1 (n_266), .A2 (n_269), .Z (n_270));
 NAND2_X1 g12596(.A1 (n_258), .A2 (n_279), .ZN (n_268));
 INV_X1 g12597(.I (n_266), .ZN (n_267));
 OAI21_X1 g12599(.A1 (n_262), .A2 (n_99), .B (n_141), .ZN
(n_272));
 AOI22_X1 g12600(.A1 (n_264), .A2 (n_17), .B1
(chequing_local[8]), .B2
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    (amount[8]), .ZN (n_274));
 OAI22_X1 g12601(.A1 (n_259), .A2 (n_37), .B1 (n_11), .B2
(amount[8]),
    .ZN (n_276));
 XOR2_X1 g12603(.A1 (n_264), .A2 (n_261), .Z (n_265));
 XOR2_X1 g12604(.A1 (n_262), .A2 (n_261), .Z (n_263));
 XNOR2_X1 g12605(.A1 (n_259), .A2 (n_256), .ZN (n_260));
 OAI21_X1 g12598(.A1 (n_257), .A2 (n_63), .B (n_120), .ZN
(n_266));
 XOR2_X1 g12602(.A1 (n_257), .A2 (n_256), .Z (n_258));
 NAND2_X1 g12606(.A1 (n_248), .A2 (n_279), .ZN (n_255));
 NAND2_X1 g12607(.A1 (n_244), .A2 (n_24), .ZN (n_264));
 AOI21_X1 g12608(.A1 (n_253), .A2 (n_112), .B (n_89), .ZN
(n_262));
 AOI22_X1 g12610(.A1 (n_251), .A2 (n_29), .B1
(savings_local[7]), .B2
    (n_68), .ZN (n_259));
 XNOR2_X1 g12613(.A1 (n_253), .A2 (n_249), .ZN (n_254));
 XNOR2_X1 g12614(.A1 (n_251), .A2 (n_246), .ZN (n_252));
 AOI21_X1 g12609(.A1 (n_247), .A2 (n_50), .B (n_118), .ZN
(n_257));
 XOR2_X1 g12611(.A1 (n_243), .A2 (n_249), .Z (n_250));
 XOR2_X1 g12612(.A1 (n_247), .A2 (n_246), .Z (n_248));
 NAND2_X1 g12616(.A1 (n_240), .A2 (n_279), .ZN (n_245));
 OAI21_X1 g12615(.A1 (chequing_local[7]), .A2 (amount[7]), .B
(n_243),
    .ZN (n_244));
 OAI21_X1 g12619(.A1 (n_10), .A2 (amount[6]), .B (n_233), .ZN
(n_253));
 OAI21_X1 g12620(.A1 (n_12), .A2 (amount[6]), .B (n_231), .ZN
(n_251));
 OAI21_X1 g12618(.A1 (n_239), .A2 (n_74), .B (n_114), .ZN
(n_247));
 OAI21_X1 g12617(.A1 (n_241), .A2 (n_78), .B (n_116), .ZN
(n_243));
 XOR2_X1 g12621(.A1 (n_241), .A2 (n_235), .Z (n_242));
 XOR2_X1 g12622(.A1 (n_239), .A2 (n_237), .Z (n_240));
 XOR2_X1 g12623(.A1 (n_229), .A2 (n_237), .Z (n_238));
 XOR2_X1 g12624(.A1 (n_232), .A2 (n_235), .Z (n_236));
 NAND2_X1 g12625(.A1 (n_222), .A2 (n_279), .ZN (n_234));
 OAI21_X1 g12626(.A1 (chequing_local[6]), .A2 (n_230), .B
(n_232), .ZN
    (n_233));
 OAI21_X1 g12627(.A1 (savings_local[6]), .A2 (n_230), .B
(n_229), .ZN
    (n_231));
 DFFSNQ_X1 \state_reg[1] (.SN (1'b1), .CLK (clk), .D (n_217), .Q
    (state[1]));
 AOI22_X1 g12628(.A1 (n_226), .A2 (n_18), .B1
(chequing_local[5]), .B2
    (amount[5]), .ZN (n_241));
 AOI22_X1 g12629(.A1 (n_221), .A2 (n_15), .B1
(savings_local[5]), .B2
    (amount[5]), .ZN (n_239));
 OAI21_X1 g12630(.A1 (n_224), .A2 (n_84), .B (n_142), .ZN
(n_232));
 OAI21_X1 g12631(.A1 (n_219), .A2 (n_86), .B (n_133), .ZN
(n_229));
 OAI21_X1 g12632(.A1 (n_214), .A2 (n_206), .B (n_425), .ZN
(n_228));
 XOR2_X1 g12633(.A1 (n_226), .A2 (n_223), .Z (n_227));
 XOR2_X1 g12634(.A1 (n_224), .A2 (n_223), .Z (n_225));
 XOR2_X1 g12635(.A1 (n_221), .A2 (n_218), .Z (n_222));
 XOR2_X1 g12636(.A1 (n_219), .A2 (n_218), .Z (n_220));
 OAI22_X1 g12643(.A1 (n_200), .A2 (n_216), .B1 (n_148), .B2
(n_330),
    .ZN (n_217));
 XOR2_X1 g12644(.A1 (n_205), .A2 (n_210), .Z (n_215));
 XOR2_X1 g12645(.A1 (n_209), .A2 (n_212), .Z (n_214));
 XNOR2_X1 g12646(.A1 (n_203), .A2 (n_212), .ZN (n_213));
 XOR2_X1 g12647(.A1 (n_208), .A2 (n_210), .Z (n_211));
 OAI21_X1 g12638(.A1 (n_209), .A2 (n_119), .B (n_70), .ZN
(n_226));
 AOI21_X1 g12639(.A1 (n_208), .A2 (n_107), .B (n_138), .ZN
(n_219));
 OAI21_X1 g12640(.A1 (n_199), .A2 (n_206), .B (n_425), .ZN
(n_207));
 OAI22_X1 g12641(.A1 (n_205), .A2 (n_20), .B1 (n_204), .B2
(n_202),
    .ZN (n_221));
 AOI22_X1 g12642(.A1 (n_203), .A2 (n_34), .B1
(chequing_local[4]), .B2
    (n_202), .ZN (n_224));
 NAND2_X1 g12648(.A1 (n_192), .A2 (n_279), .ZN (n_201));
 DFFSNQ_X1 \state_reg[2] (.SN (1'b1), .CLK (clk), .D (n_189), .Q
    (state[2]));
 AOI21_X1 g12650(.A1 (n_188), .A2 (n_185), .B (n_154), .ZN
(n_200));
 AOI22_X1 g12651(.A1 (n_191), .A2 (n_22), .B1
(savings_local[3]), .B2
    (amount[3]), .ZN (n_205));
 OAI21_X1 g12652(.A1 (n_193), .A2 (n_94), .B (n_139), .ZN
(n_208));
 OAI21_X1 g12653(.A1 (n_196), .A2 (n_82), .B (n_136), .ZN
(n_203));
 AOI22_X1 g12654(.A1 (n_198), .A2 (n_23), .B1
(chequing_local[3]), .B2
    (amount[3]), .ZN (n_209));
 XNOR2_X1 g12655(.A1 (n_198), .A2 (n_195), .ZN (n_199));
 XOR2_X1 g12656(.A1 (n_196), .A2 (n_195), .Z (n_197));
 XOR2_X1 g12657(.A1 (n_193), .A2 (n_190), .Z (n_194));
 XOR2_X1 g12658(.A1 (n_191), .A2 (n_190), .Z (n_192));
 OAI22_X1 g12660(.A1 (n_165), .A2 (rst), .B1 (n_188), .B2
(n_216), .ZN
    (n_189));
 DFFSNQ_X1 open_atm_receive_reg(.SN (1'b1), .CLK (clk), .D
(n_184), .Q
    (open_atm_receive));
 DFFSNQ_X1 \state_reg[3] (.SN (1'b1), .CLK (clk), .D (n_183), .Q
    (state[3]));
 AOI22_X1 g12661(.A1 (n_177), .A2 (n_160), .B1 (n_103), .B2
(n_186),
    .ZN (n_187));
 OAI21_X1 g12665(.A1 (n_149), .A2 (n_147), .B (n_150), .ZN
(n_185));
 INV_X1 g12669(.I (n_179), .ZN (n_184));
 OAI21_X1 g12675(.A1 (n_113), .A2 (n_216), .B (n_155), .ZN
(n_183));
 INV_X1 g12680(.I (n_182), .ZN (n_383));
 OAI21_X1 g12663(.A1 (n_178), .A2 (n_16), .B
(open_atm_dispense), .ZN
    (n_181));
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  OAI21_X1 g12664(.A1 (n_170), .A2 (n_61), .B (n_124), .ZN
(n_191));
  OAI21_X1 g12666(.A1 (n_167), .A2 (n_53), .B (n_115), .ZN
(n_198));
  AOI22_X1 g12667(.A1 (n_173), .A2 (n_33), .B1
(savings_local[2]), .B2
      (n_180), .ZN (n_193));
  AOI22_X1 g12668(.A1 (n_175), .A2 (n_30), .B1
(chequing_local[2]), .B2
      (n_180), .ZN (n_196));
  AOI22_X1 g12670(.A1 (open_atm_receive), .A2 (n_178), .B1
(n_146), .B2
      (n_177), .ZN (n_179));
  XOR2_X1 g12671(.A1 (n_168), .A2 (n_175), .Z (n_176));
  XOR2_X1 g12672(.A1 (n_171), .A2 (n_173), .Z (n_174));
  XOR2_X1 g12673(.A1 (n_171), .A2 (n_170), .Z (n_172));
  XOR2_X1 g12674(.A1 (n_168), .A2 (n_167), .Z (n_169));
  NOR2_X1 g12676(.A1 (n_332), .A2 (n_166), .ZN (n_279));
  NOR2_X1 g12677(.A1 (n_216), .A2 (n_166), .ZN (n_353));
  NAND2_X1 g12678(.A1 (state[0]), .A2 (n_335), .ZN (n_206));
  AOI21_X1 g12679(.A1 (n_153), .A2 (n_7), .B (n_152), .ZN
(n_165));
  NAND2_X1 g12681(.A1 (n_186), .A2 (n_335), .ZN (n_182));
  XOR2_X1 g12683(.A1 (n_161), .A2 (n_163), .Z (n_164));
  XNOR2_X1 g12684(.A1 (n_161), .A2 (n_104), .ZN (n_162));
  NAND3_X1 g12682(.A1 (n_151), .A2 (n_101), .A3 (n_128), .ZN
(n_160));
  XOR2_X1 g12685(.A1 (n_157), .A2 (n_129), .Z (n_159));
  XNOR2_X1 g12686(.A1 (n_157), .A2 (n_156), .ZN (n_158));
  AOI21_X1 g12694(.A1 (n_154), .A2 (n_333), .B (n_132), .ZN
(n_155));
  NAND2_X1 g12687(.A1 (n_153), .A2 (account_selection), .ZN
(n_166));
  AND2_X1 g12688(.A1 (n_153), .A2 (n_324), .Z (n_335));
  OAI22_X1 g12692(.A1 (n_151), .A2 (n_43), .B1 (n_150), .B2
(n_102),
      .ZN (n_152));
  NAND4_X1 g12695(.A1 (n_97), .A2 (n_14), .A3 (pin[7]), .A4
(pin[6]),
      .ZN (n_149));
  AOI21_X1 g12698(.A1 (n_151), .A2 (state[3]), .B (n_127), .ZN
(n_148));
  INV_X1 g12689(.I (n_130), .ZN (n_167));
  OAI21_X1 g12691(.A1 (n_163), .A2 (n_92), .B (n_140), .ZN
(n_173));
  NAND3_X1 g12693(.A1 (n_96), .A2 (n_4), .A3 (pin[1]), .ZN
(n_147));
  OAI21_X1 g12696(.A1 (n_146), .A2 (rst), .B (n_216), .ZN (n_178));
  AOI21_X1 g12699(.A1 (savings_local[1]), .A2 (amount[1]), .B
(n_106),
      .ZN (n_170));
  OAI22_X1 g12700(.A1 (n_156), .A2 (n_38), .B1 (n_8), .B2
(amount[1]),
      .ZN (n_175));
  INV_X1 g12701(.I (n_144), .ZN (n_145));
  INV_X1 g12720(.I (n_329), .ZN (n_143));
  NAND2_X1 g12722(.A1 (n_142), .A2 (n_85), .ZN (n_223));
  NAND2_X1 g12723(.A1 (n_141), .A2 (n_100), .ZN (n_261));
  NAND2_X1 g12724(.A1 (n_140), .A2 (n_93), .ZN (n_161));
  NAND2_X1 g12725(.A1 (n_139), .A2 (n_95), .ZN (n_190));
  NOR2_X1 g12727(.A1 (n_108), .A2 (n_138), .ZN (n_210));
  NAND2_X1 g12728(.A1 (n_137), .A2 (n_110), .ZN (n_286));
  NAND2_X1 g12729(.A1 (n_136), .A2 (n_83), .ZN (n_195));
  NAND2_X1 g12730(.A1 (n_135), .A2 (n_81), .ZN (n_304));
  NAND2_X1 g12731(.A1 (n_134), .A2 (n_91), .ZN (n_281));
  NAND2_X1 g12732(.A1 (n_133), .A2 (n_87), .ZN (n_218));
  NOR3_X1 g12735(.A1 (n_150), .A2 (n_66), .A3 (rst), .ZN (n_132));
  AND3_X1 g12697(.A1 (n_332), .A2 (n_150), .A3 (n_188), .Z
(ready));
  OAI21_X1 g12690(.A1 (n_59), .A2 (n_129), .B (n_117), .ZN
(n_130));
  NAND2_X1 g12703(.A1 (n_127), .A2
(deposit_withdrawal_selection), .ZN
      (n_128));
  NAND2_X1 g12704(.A1 (n_52), .A2 (n_126), .ZN (n_291));
  NOR2_X1 g12705(.A1 (n_48), .A2 (n_125), .ZN (n_309));
  NAND2_X1 g12706(.A1 (n_62), .A2 (n_124), .ZN (n_171));
  NAND2_X1 g12707(.A1 (n_77), .A2 (n_123), .ZN (n_271));
  NAND2_X1 g12708(.A1 (n_58), .A2 (n_122), .ZN (n_294));
  NOR2_X1 g12709(.A1 (n_56), .A2 (n_121), .ZN (n_269));
  NAND2_X1 g12710(.A1 (n_64), .A2 (n_120), .ZN (n_256));
  NOR2_X1 g12711(.A1 (n_71), .A2 (n_119), .ZN (n_212));
  NOR2_X1 g12712(.A1 (n_118), .A2 (n_49), .ZN (n_246));
  NAND2_X1 g12713(.A1 (n_60), .A2 (n_117), .ZN (n_157));
  NAND2_X1 g12714(.A1 (n_79), .A2 (n_116), .ZN (n_235));
  NAND2_X1 g12715(.A1 (n_54), .A2 (n_115), .ZN (n_168));
  NAND2_X1 g12716(.A1 (n_75), .A2 (n_114), .ZN (n_237));
  AND2_X1 g12717(.A1 (n_127), .A2 (n_150), .Z (n_153));
  NOR2_X1 g12718(.A1 (n_146), .A2 (state[3]), .ZN (n_113));
  NOR2_X1 g12719(.A1 (state[3]), .A2 (n_330), .ZN (n_177));
  NAND2_X1 g12721(.A1 (n_127), .A2 (state[3]), .ZN (n_329));
  NAND2_X1 g12726(.A1 (n_88), .A2 (n_112), .ZN (n_249));
  HA_X1 g12702(.A (n_322), .B (chequing_local[13]), .CO
(n_111), .S
      (n_144));
  INV_X1 g12820(.I (n_109), .ZN (n_110));
  INV_X1 g12847(.I (n_107), .ZN (n_108));
  AOI21_X1 g12733(.A1 (n_105), .A2 (n_46), .B (n_104), .ZN
(n_106));
  OAI21_X1 g12734(.A1 (n_150), .A2 (n_65), .B (n_102), .ZN
(n_103));
  AOI22_X1 g12736(.A1 (n_40), .A2 (bank_card_insert), .B1
(state[2]),
      .B2 (account_selection), .ZN (n_101));
  INV_X1 g12816(.I (n_99), .ZN (n_100));
  AOI22_X1 g12737(.A1 (n_98), .A2 (n_322), .B1
(savings_local[13]), .B2
      (amount[13]), .ZN (n_316));
  NOR4_X1 g12738(.A1 (n_0), .A2 (pin[5]), .A3 (pin[3]), .A4 (pin[2]),
      .ZN (n_97));
  NOR4_X1 g12739(.A1 (n_1), .A2 (pin[11]), .A3 (pin[13]), .A4
      (pin[12]), .ZN (n_96));
  INV_X1 g12840(.I (n_94), .ZN (n_95));
  INV_X1 g12802(.I (n_146), .ZN (n_151));
  INV_X1 g12811(.I (n_92), .ZN (n_93));
  INV_X1 g12813(.I (n_90), .ZN (n_91));
  INV_X1 g12818(.I (n_88), .ZN (n_89));
  INV_X1 g12824(.I (n_86), .ZN (n_87));
  INV_X1 g12833(.I (n_84), .ZN (n_85));
  INV_X1 g12843(.I (n_82), .ZN (n_83));
  INV_X1 g12850(.I (n_216), .ZN (n_186));
  INV_X1 g12804(.I (n_80), .ZN (n_81));
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  INV_X1 g12799(.I (n_330), .ZN (n_333));
  NAND2_X1 g12851(.A1 (state[0]), .A2 (n_425), .ZN (n_216));
  NOR2_X1 g12825(.A1 (savings_local[5]), .A2 (n_72), .ZN (n_86));
  NOR2_X1 g12821(.A1 (chequing_local[10]), .A2 (n_69), .ZN
(n_109));
  INV_X1 g12781(.I (n_78), .ZN (n_79));
  INV_X1 g12794(.I (n_76), .ZN (n_77));
  INV_X1 g12761(.I (n_74), .ZN (n_75));
  NOR2_X1 g12829(.A1 (n_98), .A2 (amount[13]), .ZN (n_73));
  NAND2_X1 g12842(.A1 (chequing_local[8]), .A2 (n_39), .ZN
(n_141));
  NOR2_X1 g12834(.A1 (chequing_local[5]), .A2 (n_72), .ZN
(n_84));
  INV_X1 g12789(.I (n_70), .ZN (n_71));
  NAND2_X1 g12810(.A1 (chequing_local[10]), .A2 (n_69), .ZN
(n_137));
  NOR2_X1 g12774(.A1 (n_28), .A2 (n_68), .ZN (n_118));
  NOR2_X1 g12740(.A1 (chequing_local[0]), .A2 (n_67), .ZN
(n_156));
  NOR2_X1 g12741(.A1 (n_65), .A2 (bank_card_insert), .ZN
(n_66));
  NOR2_X1 g12742(.A1 (savings_local[0]), .A2 (n_67), .ZN (n_163));
  INV_X1 g12746(.I (n_63), .ZN (n_64));
  INV_X1 g12751(.I (n_61), .ZN (n_62));
  INV_X1 g12753(.I (n_59), .ZN (n_60));
  INV_X1 g12757(.I (n_57), .ZN (n_58));
  NOR2_X1 g12844(.A1 (chequing_local[3]), .A2 (n_31), .ZN
(n_82));
  INV_X1 g12763(.I (n_55), .ZN (n_56));
  INV_X1 g12766(.I (n_53), .ZN (n_54));
  INV_X1 g12769(.I (n_51), .ZN (n_52));
  INV_X1 g12771(.I (n_49), .ZN (n_50));
  NAND2_X1 g12819(.A1 (chequing_local[7]), .A2 (n_68), .ZN
(n_88));
  INV_X1 g12779(.I (n_47), .ZN (n_48));
  NOR2_X1 g12812(.A1 (savings_local[1]), .A2 (n_46), .ZN (n_92));
  NAND2_X1 g12788(.A1 (n_44), .A2 (n_69), .ZN (n_45));
  INV_X1 g12792(.I (n_102), .ZN (n_154));
  NAND2_X1 g12848(.A1 (n_204), .A2 (amount[4]), .ZN (n_107));
  NOR2_X1 g12743(.A1 (n_150), .A2 (bank_card_insert), .ZN
(n_43));
  NAND2_X1 g12801(.A1 (n_41), .A2 (amount[11]), .ZN (n_42));
  NOR2_X1 g12803(.A1 (n_65), .A2 (state[1]), .ZN (n_146));
  NOR2_X1 g12806(.A1 (n_40), .A2 (state[2]), .ZN (n_127));
  NAND2_X1 g12809(.A1 (savings_local[1]), .A2 (n_46), .ZN
(n_140));
  NOR2_X1 g12814(.A1 (savings_local[10]), .A2 (n_69), .ZN (n_90));
  NOR2_X1 g12815(.A1 (n_204), .A2 (amount[4]), .ZN (n_138));
  NOR2_X1 g12817(.A1 (chequing_local[8]), .A2 (n_39), .ZN
(n_99));
  NAND2_X1 g12822(.A1 (n_5), .A2 (amount[7]), .ZN (n_112));
  NOR2_X1 g12823(.A1 (chequing_local[1]), .A2 (n_46), .ZN
(n_38));
  NOR2_X1 g12827(.A1 (savings_local[8]), .A2 (n_39), .ZN (n_37));
  NOR2_X1 g12830(.A1 (savings_local[12]), .A2 (n_26), .ZN (n_36));
  NAND2_X1 g12832(.A1 (n_2), .A2 (amount[9]), .ZN (n_35));
  NAND2_X1 g12836(.A1 (n_3), .A2 (amount[4]), .ZN (n_34));
  NAND2_X1 g12837(.A1 (n_32), .A2 (amount[2]), .ZN (n_33));
  NAND2_X1 g12838(.A1 (chequing_local[5]), .A2 (n_72), .ZN
(n_142));
  NAND2_X1 g12839(.A1 (savings_local[5]), .A2 (n_72), .ZN
(n_133));
  NOR2_X1 g12841(.A1 (savings_local[3]), .A2 (n_31), .ZN (n_94));
  NAND2_X1 g12846(.A1 (n_9), .A2 (amount[2]), .ZN (n_30));
  NAND2_X1 g12835(.A1 (savings_local[10]), .A2 (n_69), .ZN
(n_134));
  NAND2_X1 g12808(.A1 (n_28), .A2 (amount[7]), .ZN (n_29));
  NAND2_X1 g12845(.A1 (savings_local[3]), .A2 (n_31), .ZN
(n_139));
  NAND2_X1 g12807(.A1 (chequing_local[3]), .A2 (n_31), .ZN
(n_136));
  NAND2_X1 g12826(.A1 (n_13), .A2 (amount[11]), .ZN (n_27));
  NAND2_X1 g12831(.A1 (chequing_local[12]), .A2 (n_26), .ZN
(n_135));
  NOR2_X1 g12805(.A1 (chequing_local[12]), .A2 (n_26), .ZN
(n_80));
  NAND2_X1 g12800(.A1 (n_332), .A2 (n_425), .ZN (n_330));
  NAND2_X1 g12828(.A1 (n_6), .A2 (amount[9]), .ZN (n_25));
  NAND2_X1 g12783(.A1 (chequing_local[11]), .A2
(amount[11]), .ZN
      (n_122));
  NAND2_X1 g12778(.A1 (chequing_local[7]), .A2 (amount[7]), .ZN
(n_24));
  NOR2_X1 g12782(.A1 (chequing_local[6]), .A2 (amount[6]), .ZN
(n_78));
  NAND2_X1 g12797(.A1 (savings_local[8]), .A2 (amount[8]), .ZN
(n_120));
  NAND2_X1 g12793(.A1 (state[1]), .A2 (state[2]), .ZN (n_102));
  OR2_X1 g12765(.A1 (chequing_local[3]), .A2 (amount[3]), .Z
(n_23));
  OR2_X1 g12755(.A1 (savings_local[3]), .A2 (amount[3]), .Z
(n_22));
  NOR2_X1 g12747(.A1 (savings_local[8]), .A2 (amount[8]), .ZN
(n_63));
  OR2_X1 g12791(.A1 (chequing_local[12]), .A2 (amount[12]), .Z
(n_21));
  NAND2_X1 g12780(.A1 (savings_local[12]), .A2 (amount[12]), .ZN
      (n_47));
  NOR2_X1 g12762(.A1 (savings_local[6]), .A2 (amount[6]), .ZN
(n_74));
  NOR2_X1 g12796(.A1 (savings_local[4]), .A2 (amount[4]), .ZN
(n_20));
  NAND2_X1 g12785(.A1 (chequing_local[9]), .A2 (amount[9]), .ZN
      (n_123));
  OR2_X1 g12784(.A1 (chequing_local[10]), .A2 (amount[10]), .Z
(n_19));
  NAND2_X1 g12773(.A1 (savings_local[2]), .A2 (amount[2]), .ZN
(n_124));
  NAND2_X1 g12790(.A1 (chequing_local[4]), .A2 (amount[4]), .ZN
(n_70));
  NAND2_X1 g12745(.A1 (chequing_local[2]), .A2 (amount[2]), .ZN
      (n_115));
  OR2_X1 g12748(.A1 (chequing_local[5]), .A2 (amount[5]), .Z
(n_18));
  NOR2_X1 g12750(.A1 (savings_local[12]), .A2 (amount[12]), .ZN
      (n_125));
  NOR2_X1 g12770(.A1 (savings_local[11]), .A2 (amount[11]), .ZN
(n_51));
  NOR2_X1 g12752(.A1 (savings_local[2]), .A2 (amount[2]), .ZN
(n_61));
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  NOR2_X1 g12758(.A1 (chequing_local[11]), .A2
(amount[11]), .ZN
      (n_57));
  NAND2_X1 g12759(.A1 (savings_local[6]), .A2 (amount[6]), .ZN
(n_114));
  NOR2_X1 g12795(.A1 (chequing_local[9]), .A2 (amount[9]), .ZN
(n_76));
  NAND2_X1 g12768(.A1 (savings_local[0]), .A2 (amount[0]), .ZN
(n_104));
  NAND2_X1 g12775(.A1 (chequing_local[1]), .A2 (amount[1]), .ZN
      (n_117));
  NOR2_X1 g12786(.A1 (state[2]), .A2 (state[1]), .ZN (n_188));
  OR2_X1 g12749(.A1 (chequing_local[8]), .A2 (amount[8]), .Z
(n_17));
  NAND2_X1 g12756(.A1 (chequing_local[6]), .A2 (amount[6]), .ZN
      (n_116));
  NOR2_X1 g12754(.A1 (chequing_local[1]), .A2 (amount[1]), .ZN
(n_59));
  NOR2_X1 g12849(.A1 (state[3]), .A2 (rst), .ZN (n_16));
  NOR2_X1 g12798(.A1 (savings_local[9]), .A2 (amount[9]), .ZN
(n_121));
  NAND2_X1 g12744(.A1 (savings_local[11]), .A2 (amount[11]), .ZN
      (n_126));
  OR2_X1 g12776(.A1 (savings_local[5]), .A2 (amount[5]), .Z
(n_15));
  NOR2_X1 g12787(.A1 (chequing_local[4]), .A2 (amount[4]), .ZN
(n_119));
  NOR2_X1 g12760(.A1 (pin[9]), .A2 (pin[8]), .ZN (n_14));
  NOR2_X1 g12767(.A1 (chequing_local[2]), .A2 (amount[2]), .ZN
(n_53));
  NAND2_X1 g12764(.A1 (savings_local[9]), .A2 (amount[9]), .ZN
(n_55));
  NOR2_X1 g12772(.A1 (savings_local[7]), .A2 (amount[7]), .ZN
(n_49));
  NAND2_X1 g12777(.A1 (chequing_local[0]), .A2 (amount[0]), .ZN
      (n_129));
  INV_X1 g12867(.I (savings_local[12]), .ZN (n_313));
  INV_X1 g12885(.I (amount[4]), .ZN (n_202));
  INV_X1 g12883(.I (amount[7]), .ZN (n_68));
  INV_X1 g12886(.I (amount[11]), .ZN (n_301));
  INV_X1 g12859(.I (state[2]), .ZN (n_65));
  INV_X1 g12873(.I (chequing_local[11]), .ZN (n_13));
  INV_X1 g12852(.I (savings_local[6]), .ZN (n_12));
  INV_X1 g12892(.I (amount[9]), .ZN (n_278));
  INV_X1 g12855(.I (savings_local[2]), .ZN (n_32));
  INV_X1 g12857(.I (savings_local[8]), .ZN (n_11));
  INV_X1 g12862(.I (chequing_local[6]), .ZN (n_10));
  INV_X1 g12884(.I (amount[6]), .ZN (n_230));
  INV_X1 g12879(.I (amount[2]), .ZN (n_180));
  INV_X1 g12890(.I (amount[3]), .ZN (n_31));
  INV_X1 g12868(.I (savings_local[11]), .ZN (n_41));
  INV_X1 g12860(.I (chequing_local[2]), .ZN (n_9));
  INV_X1 g12858(.I (chequing_local[1]), .ZN (n_8));
  INV_X1 g12887(.I (deposit_withdrawal_selection), .ZN (n_7));
  INV_X1 g12853(.I (state[0]), .ZN (n_332));
  INV_X1 g12893(.I (amount[12]), .ZN (n_26));
  INV_X1 g12891(.I (amount[10]), .ZN (n_69));
  INV_X1 g12889(.I (amount[13]), .ZN (n_322));
  INV_X1 g12874(.I (amount[8]), .ZN (n_39));
  INV_X1 g12869(.I (savings_local[10]), .ZN (n_44));
  INV_X1 g12854(.I (state[3]), .ZN (n_150));
  INV_X1 g12856(.I (chequing_local[9]), .ZN (n_6));
  INV_X1 g12882(.I (rst), .ZN (n_425));
  INV_X1 g12863(.I (chequing_local[7]), .ZN (n_5));
  INV_X1 g12877(.I (pin[0]), .ZN (n_4));
  INV_X1 g12870(.I (chequing_local[4]), .ZN (n_3));
  INV_X1 g12865(.I (savings_local[9]), .ZN (n_2));
  INV_X1 g12888(.I (pin[10]), .ZN (n_1));
  INV_X1 g12875(.I (pin[4]), .ZN (n_0));
  INV_X1 g12876(.I (amount[1]), .ZN (n_46));
  INV_X1 g12864(.I (savings_local[7]), .ZN (n_28));
  INV_X1 g12881(.I (amount[5]), .ZN (n_72));
  INV_X1 g12878(.I (account_selection), .ZN (n_324));
  INV_X1 g12880(.I (amount[0]), .ZN (n_67));
  INV_X1 g12866(.I (savings_local[4]), .ZN (n_204));
  INV_X1 g12871(.I (state[1]), .ZN (n_40));
  INV_X1 g12861(.I (savings_local[13]), .ZN (n_98));
  INV_X1 g12872(.I (savings_local[1]), .ZN (n_105));
endmodule
```