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| ELEC 402 – October 24, 2021 |
| Project 3 Report |
| Martin Chua - 35713411 |

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Diagram, schematic

Description automatically generated



1. **Resistive load inverter**

At one extreme, V­in is high, transistor is off and no current flows because MOS is in cut-off region, VOH = VDD. At the other extreme, Vin = VOH = VDD substituted into IOUT = Iload g IR = I­DS(lin), and the transistor operates in linear region. Using the useful formula for linear current:

Now we can also just straight up plug-in everything (taken from question):

* Vin = VGS = VOH = VDD = 1.2 V
* VDS = Vout = VOL = 0.1 V
* L = 0.1 µm
* RL = 10 kΩ
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Equating for W and throwing into wolfram:

1. **Saturated-enhancement-load inverter**

With this layout, we know the top pull-up transistor is the load and bottom pull-down transistor is the inverter. We know the load is always in saturation and the inverter should be linear because we want Vout = VOL = 0.1 V. Using the useful formulas for linear (left) and saturated (right) current, we can equate the two and get:

Using the following substitutions (inverter):

* Vin = VGS = VOH = VDD = 1.2 V
* VDS = Vout = VOL = 0.1 V
* L = 0.1 µm
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Using the following substitutions (load):

* Vin = VOH = VDD = 1.2 V
* VGS = 1.2 – 0.1 = 1.1 V
* vsat = 8E6 cm/s
* Wload = 0.1 µm
* L = 0.1 µm
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Note that although the left side units cancel out nicely due to the cm2/cm2, we need to convert the right-side units from cm (1E-2) to µm (1E-6) after the Coxvsat cancellation as there is still a cm unit left, done by multiplying the right side with 1E-4.

Equating for Winverter and throwing into wolfram:

1. **Linear-Enhancement-Load inverter**

To overcome low VOH, in the saturated-enhancement-load inverter, instead of VDD for both gate and drain of the load transistor, it is separated with VGG = 1.6 V and VDD = 1.2 V. Its linear region of operation is then VGG > VDD + VTL(VDD). Again, we equate currents but this time, the right side is not in saturation, but linear operation as well:

Using the following substitutions (inverter):

* Vin = VGS = VOH = VDD = 1.2 V
* VDS = Vout = VOL = 0.1 V
* L = 0.1 µm
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Using the following substitutions (load):

* Vin = VDS = VOH = VDD = 1.2 V
* Vout = VOL = 0.1 V
* VGS = 1.6 – 0.1 = 1.5 V
* L = 0.1 µm
* µn = 270 cm2V-1s-1
* Cox = 1.0E-6 F/cm2
* EC = 6 V/µm
* VT = 0.4 V

Note that the difference this time between linear-enhancement and saturated-enhancement is VGS of the load pull-up transistor. Also note that Vin for the linear region inverter pull-down transistor remains at 1.2 V.

Equating for Winverter and throwing into wolfram (no need to simplify if wolfram does it all 😊):

1. **Results explanation**

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| Resistive Load | Saturated-Enhancement-Load | Linear-Enhancement-Load |
| 0.634 µm | 0.174 µm | 0.140 µm |

Table 1. Calculated widths for each inverter.

The resistive load inverter appears to have the highest width, followed by Saturated-Enhancement, then Linear-Enhancement. The resistor in digital design is probably worse than using a MOSFET due to area which in turn means a slower and larger circuit area. The Saturated-Enhancement load inverter replaces the resistor with a MOSFET, where the max input voltage is limited by VDD – VT., which has tradeoffs such a lower saturation operation threshold. The Linear-Enhancement load inverter introduces a higher V­GG, which means that biasing the gate voltage to exactly VT above drain voltage allows linear operation and increases the saturation operation threshold.

Diagram, schematic

Description automatically generated

1. The intended function of the circuit should be as a buffer. It resembles an inverter except the PMOS and NMOS are switched, with the Vout at the source. If we set logic in to be HIGH, we get HIGH as output, and vice-versa setting logic in to LOW, gets LOW as output, with VOH being at most VDD – VT due to NMOS pull-up and VOL being at least VT due to PMOS pull-down, assuming same threshold voltage for both MOSFETs.

If you tie the source of the PMOS to VDD and apply a gate voltage of 0 V, the PMOS pull-up device will always be fully on for all values of the drain/output voltage since |VGS|=VDD>|VTP|. The PMOS is an effective pull-up device since it conducts for all values of V\_{out} given V\_{g} = 0 V.

Now imagine if the PMOS device is acting as the pull-down device with its source node connected to the output, as is the case with question 2 for the non-inverting buffer. If I apply a gate voltage of 0 V, what happens to the PMOS if the source/output voltage drops too low? It will "turn off" before Vout reaches 0 V. Therefore, the PMOS is ineffective at pulling the output low.

Diagram

Description automatically generated

Graphical user interface, text, application

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1. First we need C­ox, computed using:

ɛox is the SiO2 permittivity \* free space permissibility (F/m). Thickness (m), tox, is given in the question.

We also need Cov computed using:

L­diffusion is given in the question (m), and we’ve just previously solved for Cox, (F/m2). We can also assume fringe capacitance Cf is 0 since Tpoly is not given.

We also need worst total gate capacitance Cg per unit width:

L is given in question (m). Overlap is not included.

If we include overlap, then it becomes:

There is two of Cov due to parallel capacitances. Width isn’t in calculation because this is in terms of unit width.

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|  | Cutoff | Linear | Saturation |
| **CGS** | Cov | 1/2CgW + Cov | 2/3CgW + Cov |
| **CGD** | Cov | 1/2CgW + Cov | Cov |
| **CGB** | CgW | 0 | 0 |

Table 4a. Capacitance equations for gate-source, gate-drain, gate-bulk.

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| --- | --- | --- | --- |
|  | Cutoff | Linear | Saturation |
| **CGS** | 0.19 | 0.89 | 1.12 |
| **CGD** | 0.19 | 0.89 | 0.19 |
| **CGB** | 1.4 | 0 | 0 |

Table 4b. Capacitance values for gate-source, gate-drain, gate-bulk. Units in fF/µm

1. Now we want to find Cj in units of fF/µm. We first need the voltage asymptote φB:

These constants are from the question.

Now we want Cjb:

We use Si permittivity \* free space permissibility.

Now we can solve for C­j­:

M is 0.5. Worst case takes into account both sides as well as Vj = 0 V. Y is given in the question, and so is x­j and W.

1. Drain junction capacitance equation is the same as in b, but just single xj:
   1. With Vj = -1.8 V, we get Cj = 0.299 fF.
2. With Vj = 0 V, we get Cj = 0.511 fF.

Text

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1. Inverter delay with four identical inverters at output. Pull-up means PMOS W/L 8λ:2λ, pull-down means NMOS W/L 4λ:2λ. Assuming Cg = 1fF/um from the useful formulas, knowing that 2λ = 45nm:

The 4 times is for the parallel capacitances at the output of the inverter. Similarly:

And then we can sum the two to get the total capacitance:

For delay, as given in class we can approximate the resistance as R = Reqn (L/W), where 45nm Rn is 34k Ω µm and Rp is 68 kΩ µm. We also know that ramp is just RC:

1. Inverter delay with series of 4 identical inverters, so 5 inverters in total in series.

Each inverter would have an equivalent Cself = 0.27 fF. Since its cascading, we can simply multiply by 5 to get the equivalent Ctotal = 5Cself = 1.35 fF. The load here is a wire. Thus:

**References:**

Useful physical constants: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/9781119009597.app3>