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| ELEC 402 – November 14, 2021 |
| Project 4 Report |
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| |  |  |  | | --- | --- | --- | | Area | Delay (avg) | Area X Delay | | 0.25978 um­2 | 23.636ps | 6.14 ps\*um2 | |

1. NAND3

A picture containing text, light, red

Description automatically generated

NAND3 Schematic using default widths (2 fingers)

A picture containing graphical user interface

Description automatically generated

NAND3 Layout. Layout planned using the stick layout method / euler path taught in class, rather than directly translating from schematic to layout. In hindsight, it’s possible to use 3 fingers for a two shared diffusion in the center.

Graphical user interface, text, application, email

Description automatically generated

DRC Results. DRC Summary can be found in Appendix A.

Graphical user interface, table

Description automatically generated

LVS Results pass!

A screenshot of a computer

Description automatically generated with low confidence

Testbench schematic with 12 fF capacitor. V2 = V3 = VDD = 1 VDC. V1:

Table

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Rise and fall time is specified (slew rate) in the assignment as 10ps.

A computer screen capture

Description automatically generated with low confidence

Tau with all parasitics from PEX. TpLH = 25.875 ps. TpHL = 51.17 ps.

This clearly does not match (not equal +-5ps) as specified by the assignment. Widths must be changed. Let’s try doubling the width of the NMOS to 4 fingers (default 2):

A screenshot of a computer

Description automatically generated with medium confidence

I also managed to shrink it a little bit more and re-ran with DRC, LVS , and PEX.

Graphical user interface

Description automatically generated

Now**, TpLH = 23.872 ps and TpHL = 23.4 ps.** They match (equal)!

Avg worst case delay is: 23.636ps.

1. Diagram, engineering drawing, schematic

   Description automatically generatedSizing and Timing of:
   1. The logic function (Boolean) can be obtained by observing the pull-down NMOS. We see A and B in parallel, followed by a series C and D. Hence: Y\_bar = (A + B)CD and Y = (AB)\_bar + C\_bar + D\_bar
   2. Sizing can be obtained by finding the worst case, then going off from there. We are told NMOS W/L is 4 lambda and PMOS W/L is 8 lambda.
      1. NMOS: Worst case is through A or B to C to D. There are three transistors, so all their widths are 4 \* 3 = 12 lambda
      2. PMOS: Worst case is through B to A. There are two transistors, so A and B are 8 \* 2 = 16 lambda. Single branch for C and D makes them 8 lambda.
   3. Timing to get worst case tpHL and tpLH:
      1. tpHL: For high to low, we need the pull-down network to pull from high to low. So, D should be off initially and on afterwards. For the other ones, we want to maximize capacitance and as many to be up to VDD so that discharging takes the longest, so: ABCD = 1010 -> 1011
      2. tlLH: For low to high, we need the pull-up network to pull from low to high. So, C and D should be on, and either B or A should also be on. This means that the PMOS side is not pulling up initially. As delay propagates, we want the most delay to be at the beginning, so A should be off and B should be on, then go off: ABCD = 0111 -> 0011.
      3. Simulation:

**15nm pdk** circuit: A picture containing text, light, red, black

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For the TB images below, V2 pulse (left) and ADE L settings (right):

Table

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VDD = V1 = V0 = 1V DC

Output cap = 10fF

High to low: ABCD = 1010 -> 1011:

A screenshot of a computer

Description automatically generated with low confidence

Graphical user interface

Description automatically generated

Low to high: ABCD = 0111 -> 0011:

A screenshot of a computer

Description automatically generated with low confidence

Graphical user interface

Description automatically generated

|  |  |
| --- | --- |
| TpHL | TpLH |
| 42.7ps | **34.2ps** |

Schematic Netlist is in Appendix B.

Diagram, schematic

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1. Transmission Gates
   1. Expression for output function in terms of A, B, sel, selB. OUT is C’. A’ is controlled by sel, B’ is controlled by selB. C is A’ and sel or B’ and selB, so: OUT = (Asel’) + (BselB’)
   2. Equivalent RC circuit model from A to C, given sel is high. A passes through an inverter, then a transmission gate:
      1. Text, letter

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      2. Resistances approximation: R\_inv = R\_TG = R\_eqn (L/W), R\_inv = R\_TG = 12.5k (2/4) = 6.25k ohms
      3. C1 Capacitance (Ceff -> 1, Cg -> 2 from formula):
         1. Cinv = Ceff(4 + 8) = 12Ceff
         2. Ctg = Ceff \* 2 \* (4) + Cg (4) = 8Ceff + 4Cg
         3. C1 = Cinv + Ctg = (20Ceff + 4Cg) 0.1= 2.4 fF
      4. C2 Capacitances (Ceff -> 1, Cg -> 2 from formula), x multiplier from load inverter **(I use x since I already use f for femto for clarity)**:
         1. Cinv = Cg(4 + 8) = 12Cg \* x
         2. Ctg = Ceff \* 2 \* (4) + Cg (4) = 8Ceff + 4Cg
         3. C2 = Cinv + Ctg = (8Ceff + 12fCg ) 0.1= (2.4x + 1.6) fF
   3. A to C delay. Since the resistances are the same, Elmore delay telmore = RC1 + 2RC2, where R is 6.25 k ohms and C1, C2 are above. This can simplify to telmore = 6.25k \* 2.4f + 2\*6.25k\*(2.4x + 1.6)f = 15 + 30x + 10.4 ps = 25.4 + 30x ps
   4. RC Delay, Load is 50fF, R becomes R/x, and C becomes (4 + 8) \* x \* Ceff + 50fF. Step (0.7) is used because it’s RC delay, which is the most ideal case for the output inverter.

So, trc = 0.7 \*6.25k/x (50 + 1.2x)f = 4.375 (1.2x + 50) / x ps

* 1. Optimal output inverter size to minimize A to OUT: elmore + rc delay and minimize:

25.4 + 30x + 4.375 (1.2x + 50) / x

Diagram

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This is at Text

Description automatically generated with medium confidence

So optimal multiplier x (aka f) is 2.7.

Appendix A: DRC Summary

Table

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Table

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ACT009 and NW004A as mentioned can be ignored.

Appendix B: Schematic Netlist of Q2

Text

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