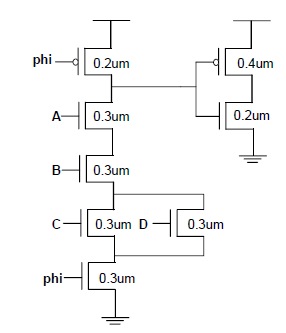
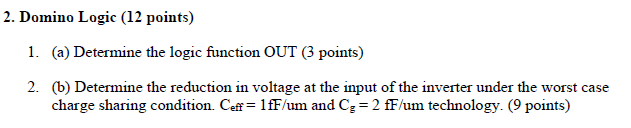
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| ELEC 402 – December 3, 2021 |
| Project 5 Report |
| Martin Chua – 35713411 |

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1. Cell Library Layout; Synthesize proj1/2 verilog with 45nm, layout using Cadence Innovus. Assume 10fF load capacitance for all output simulations.



**3**

**2**

**1**

1. By domino logic we see PMOS and NMOS with phi as input clock. OUT can be defined as the output of the output inverter. We can see the pull down NMOS consisting of A+B+CD, as AB are series with CD parallel. Since this is the dual, the resulting logic is OUT = AB(C+D)
2. Voltage reduction. Worst case charge sharing requires the combination of ABCD = 1100. Then, to calculate capacitance we can do nodal calculations. For node 1, we have Ceff of phi PMOS, A NMOS, and Cgate of inverter input. This gives us C1 = CeffWphi + CeffWA + Cg(Wp+Wn) = 1.7 fF.

For node 2, we have C2 = CeffWB = 0.3 fF. For node 3 we have C3 = Ceff(Wc + Wd) = 0.6 fF.

Now that we have all three node capacitances, we can calculate V\*, the resulting voltage across all these nodes that share charge. Since BCD are charged when AB are 1, we ta

