SC20&SC200x&SC206E Series PCB Design Guide

Smart Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-07-17	Swee Tat CHAN	Creation of the document
1.0	2023-10-10	Swee Tat CHAN	First official release

Contents

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1 Introduction

This document mainly introduces the PCB reference design for Quectel Smart SC20 series, SC200x series and SC206E series modules, and it takes SC200E-TE-A and Smart EVB-G2-V1.3 as examples to illustrate interface design in PCB.

NOTE

Please note that the pin names in the text are listed using the SC200E series module as an example, and the pin names of the same function are not listed one by one, refer to the corresponding hardware design document for details.

1.1. Applicable Modules

Table 1: Applicable Modules

Module Family	Modules Series	Module Model
SC200x Series	SC200E series	SC200E-CE/-EM/-NA/-WF/-JP/-GL
	SC200R series	SC200R-CE/-EM/-NA/-WF
-	SC206E series	SC206E-EM/-NA/-WF/-GL
-	SC20 series	● Android version: SC20-CE R1.1, SC20-E/-A/-AU/-J ● Linux version: SC20-CEL R1.1, SC20-EL/-AL/-AUL/-JL/-AX/-EX

2 PCB Design Overview

2.1. Basic Check Items

- A 6-layer PCB is strongly recommended.
- Check whether there is an interference between layout components.
- Check whether there is any isolated copper skin, single-ended network or spacing issue.
- Check whether copper in each layer of the PCB is complete and whether the size of the solder layer is appropriate (generally 2 mils larger than the actual pad).
- Check whether the space between parts and components on PCB is appropriate.
- Check whether the SC20 series, SC200x series and SC206E series module's footprint is of the latest version provided by Quectel. For the specific footprint of each module, see ***documents [1]***, ***[2]*** and ***[3]***.

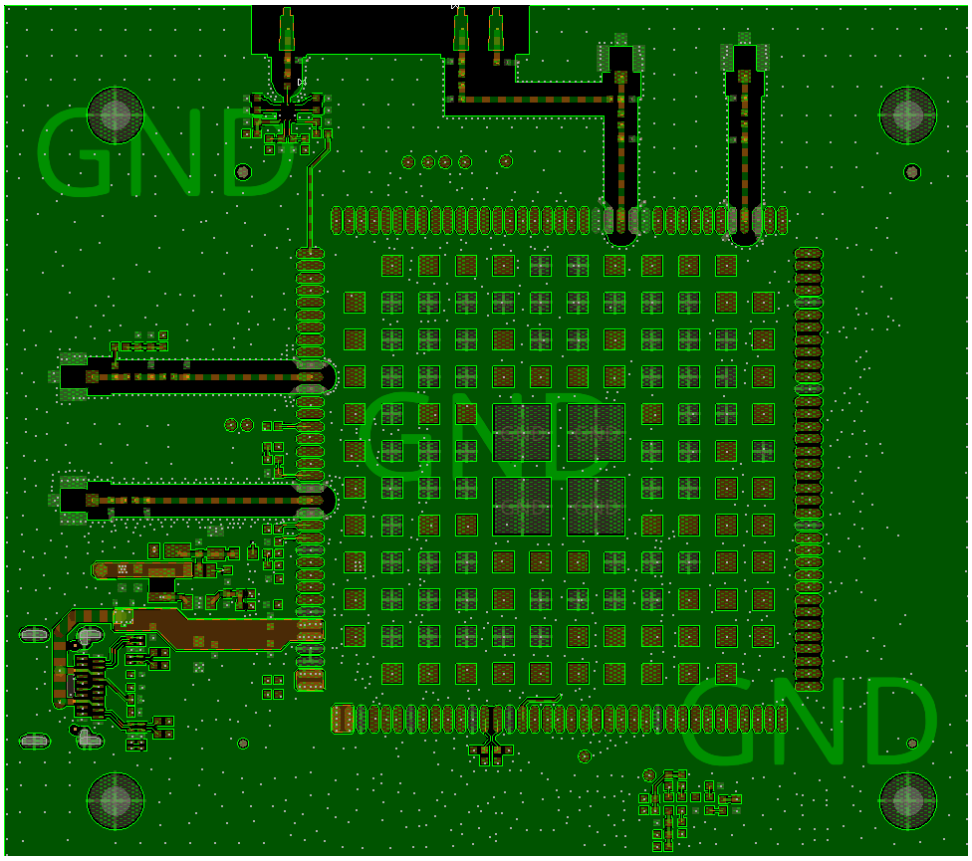

Figure 1: Overview of SC200E-TE-A 1st Layer

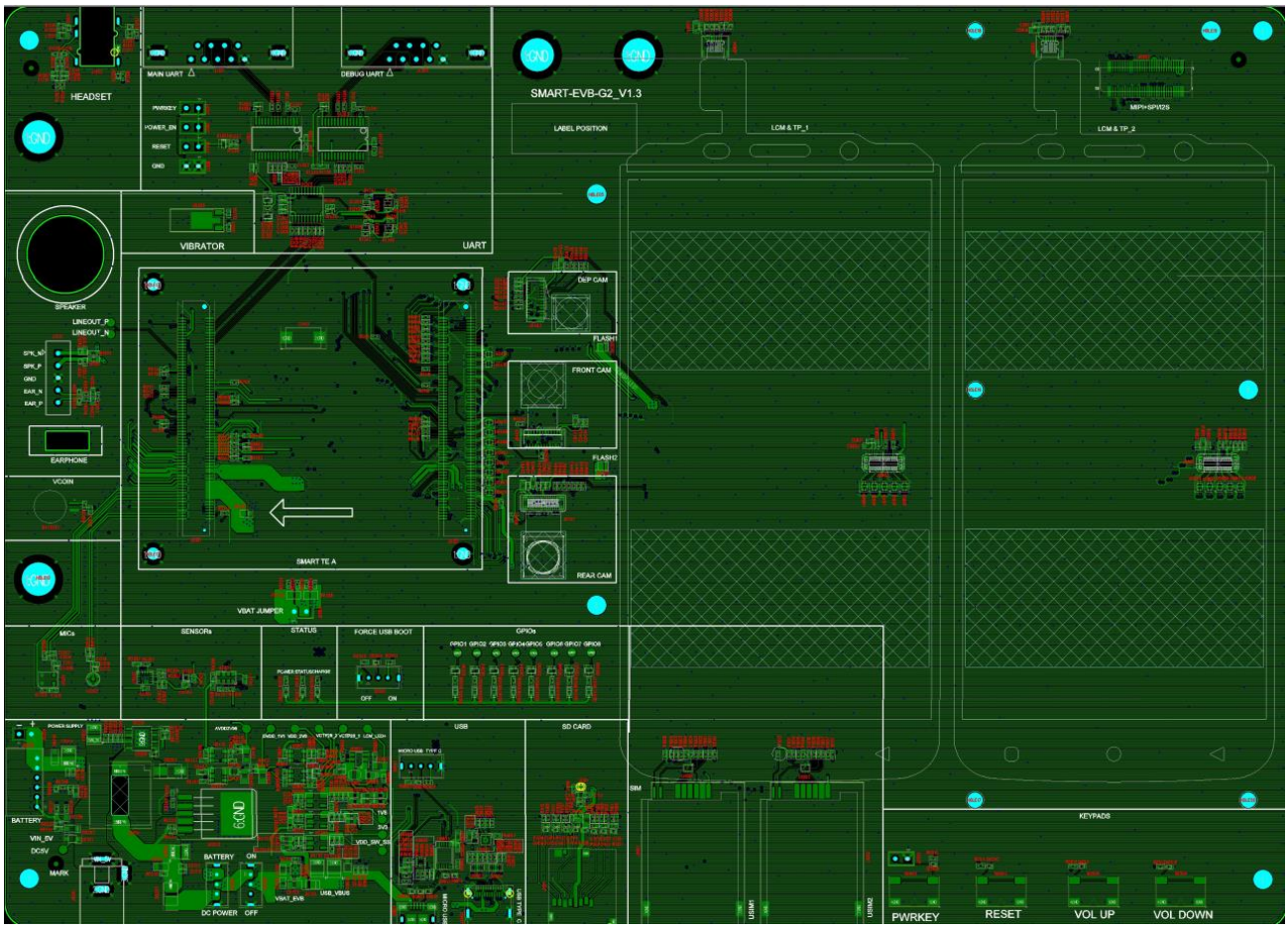

Figure 2: Overview of EVB-G2-V1.3 1st Layer

2.2. Design Priorities and Considerations for PCB Traces

2.2.1. Design Priorities

Design the PCB traces according to the recommended order as follows:

- Antenna traces
- High-speed signal (MIPI, SDIO, and USB, etc.) traces
- Sensitive signal (I2C, PWM, audio, SPI and ADC) traces
- Power supply (VBAT/VBAT_BB/VBAT_RF, USB_VBUS, USIM_VDD, SD_LDO, VPH_PWR [1]) traces
- Other traces

[1] SC20 series and SC200R series do not have VPH_PWR pins.

2.2.2. Design Considerations

- The radiation of PWM, USB, (U)SIM and SD interfaces and their power supply could affect RF performance, so keep them away from RF signal traces and components.
- Drill as fewer vias as possible for high-speed signal traces, such as MIPI, SDIO and USB interfaces, since vias will affect the continuity of the impedance. Route differential pair traces on the same layer.
- To minimize the signal return path, the GND vias for signals such as USB, SDIO, MIPI, PWRKEY and RESET_N should be close to the vias where the traces change layers.

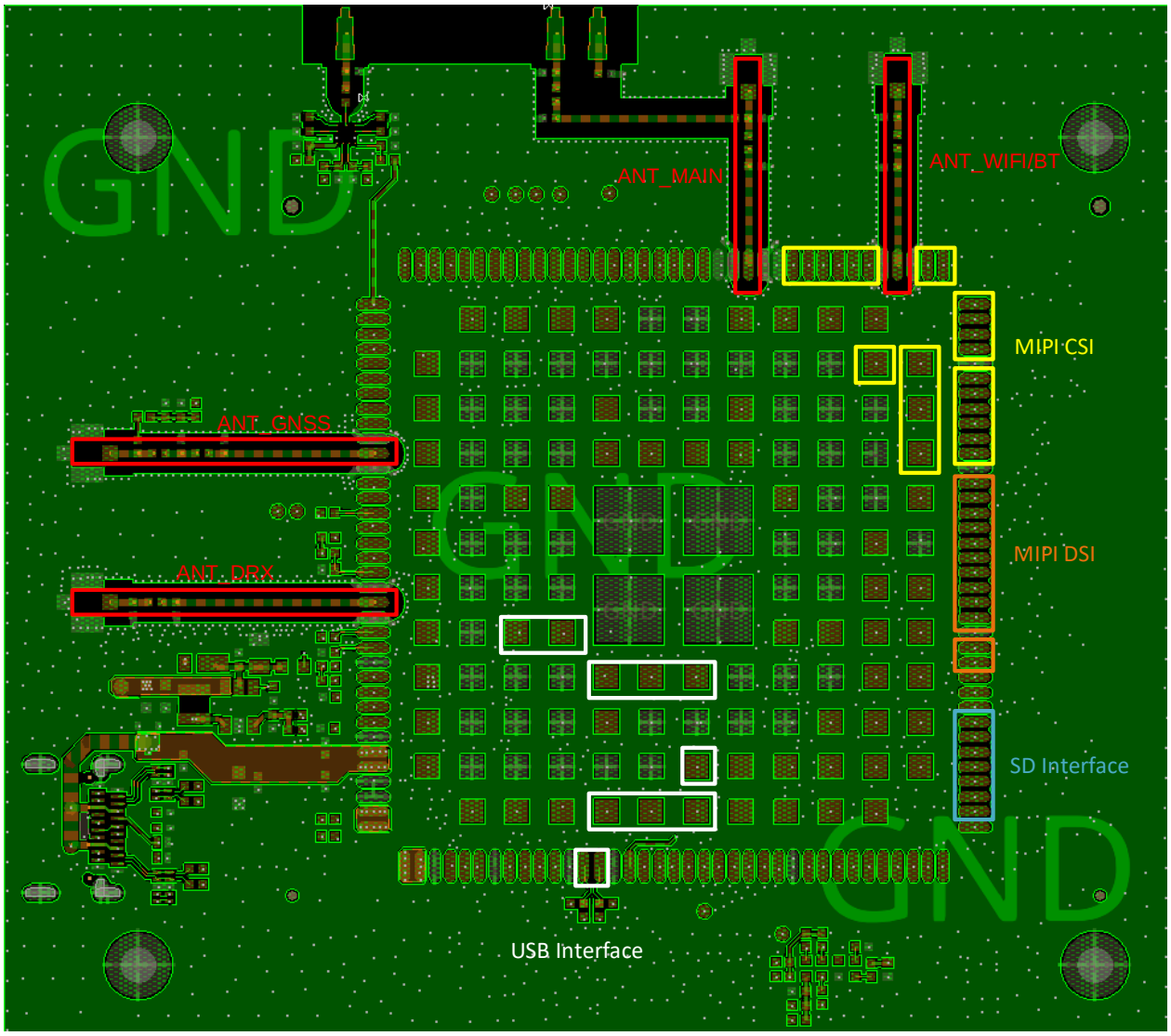

Figure 3: High-priority Signals to be Designed (SC200E-TE-A 1st Layer)

3 Interface Design

3.1. Power Supply

3.1.1. DC-DC Converter

- Place the DC-DC converter away from the sensitive signal traces such as MIPI, SDIO, USB, audio and RF signals. If possible, shield DC-DC converter with shielding cover and reserve spacing for shielding frame.
- Place the capacitor and inductor for the DC-DC converter as close as possible to the corresponding pins of the DC-DC converter to minimize the loop area.
- Place output capacitors near input capacitors to share common ground area on outer layers.
- Provide adequate thermal relief area at the ground area on outer layers and any additional inner ground planes.

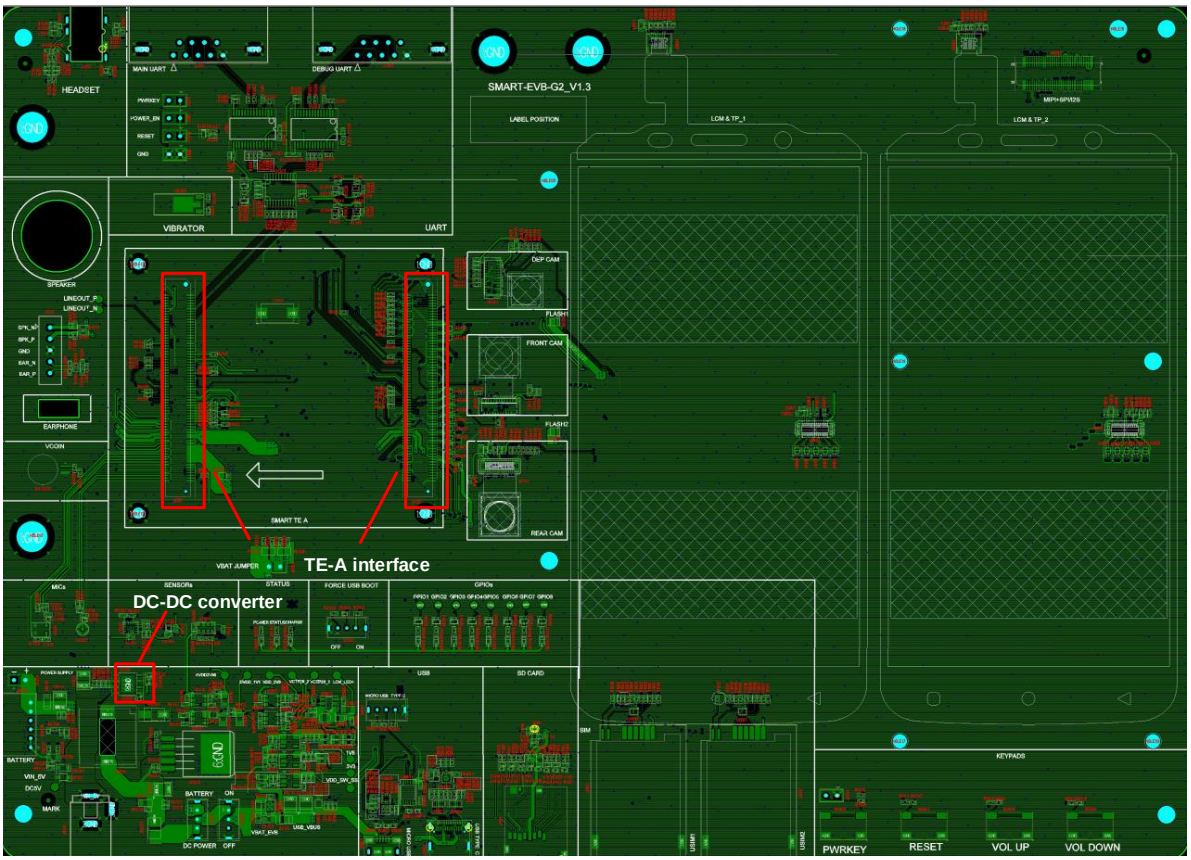

Figure 4: DC-DC Converter and Module Interfaces of TE-A (EVB-G2-V1.3 1st Layer)

3.1.2. VBAT

- For SC200E & SC206E series, place 100 μF, 4.7 μF, 100 nF, 33 pF and 10 pF capacitors for VBAT. The smaller the capacitance is, the closer the capacitors are to the VBAT pins.
- For SC200E&SC200R series, VBAT trace width is recommended to be not less than 3 mm. Moreover, pay attention to the capability and quantity of vias in the VBAT traces. The GND vias of the filter capacitors for VBAT and should be drilled down to the nearest main ground.
- As for SC200R&SC20 series, place 100 μF, 100 nF, 33 pF and 10 pF capacitors for VBAT_BB and VBAT_RF respectively. (while for SC200R series, an additional 4.7 μF capacitor should be added for VBAT_BB).
- The width of VBAT_BB trace should be not less than 1.5 mm, and the width of VBAT_RF trace should be not less than 2 mm.

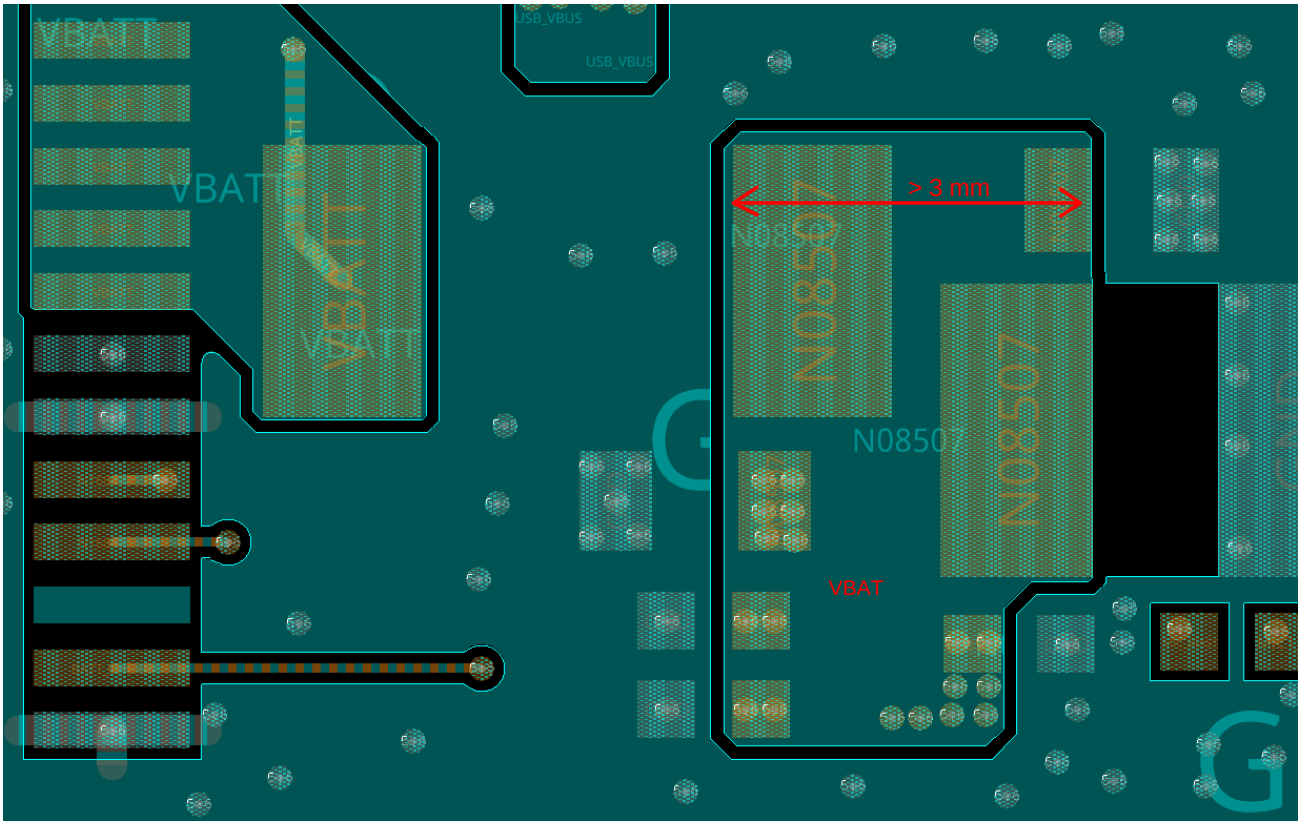

Figure 5: VBAT Traces (SC200E-TE-A 6th Layer)

- Place the TVS components for VBAT close to the module's VBAT pins.
- VBAT traces should be away from sensitive signal traces such as SDIO, USB, audio and RF to avoid paralleling or crossing with them.
- A layer with VBAT traces and reference ground plane is recommended. When a power plane is used, a complete ground plane should be added in adjacent layer as the reference plane.

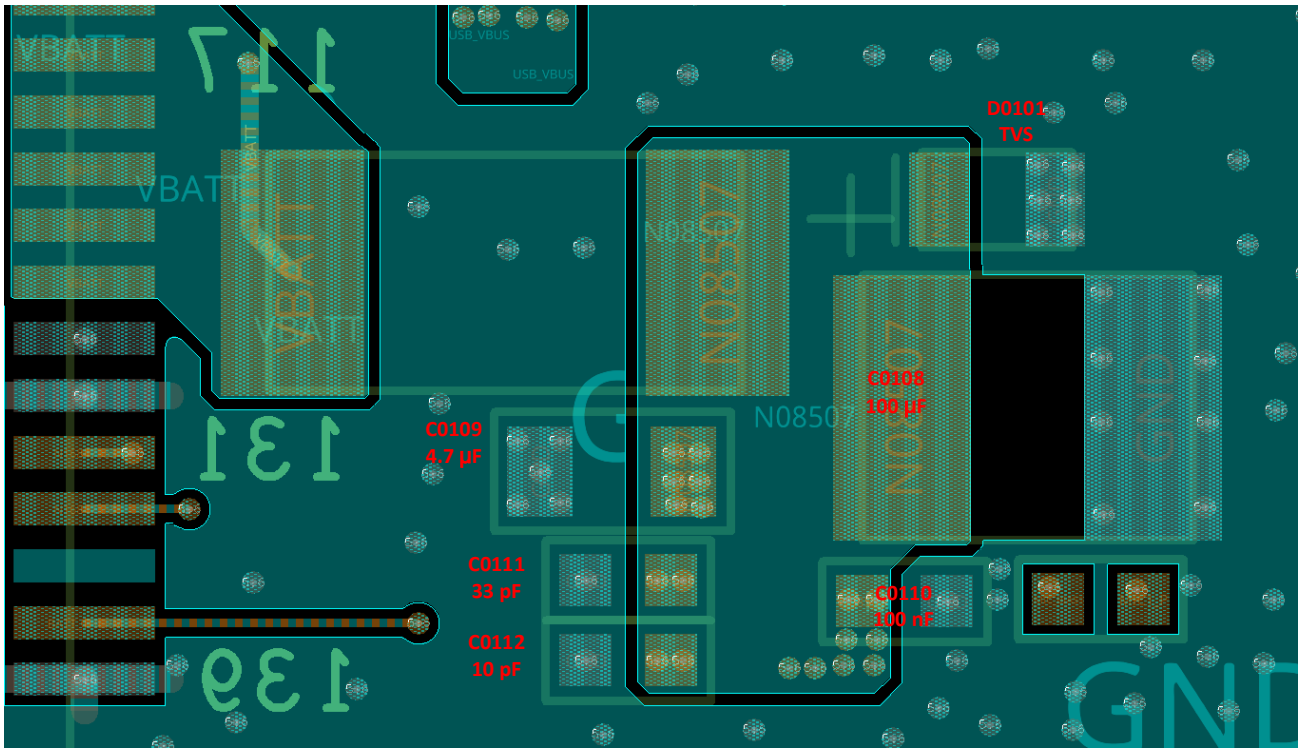

Figure 6: Traces of VBAT with a TVS (SC200E-TE-A 6th Layer)

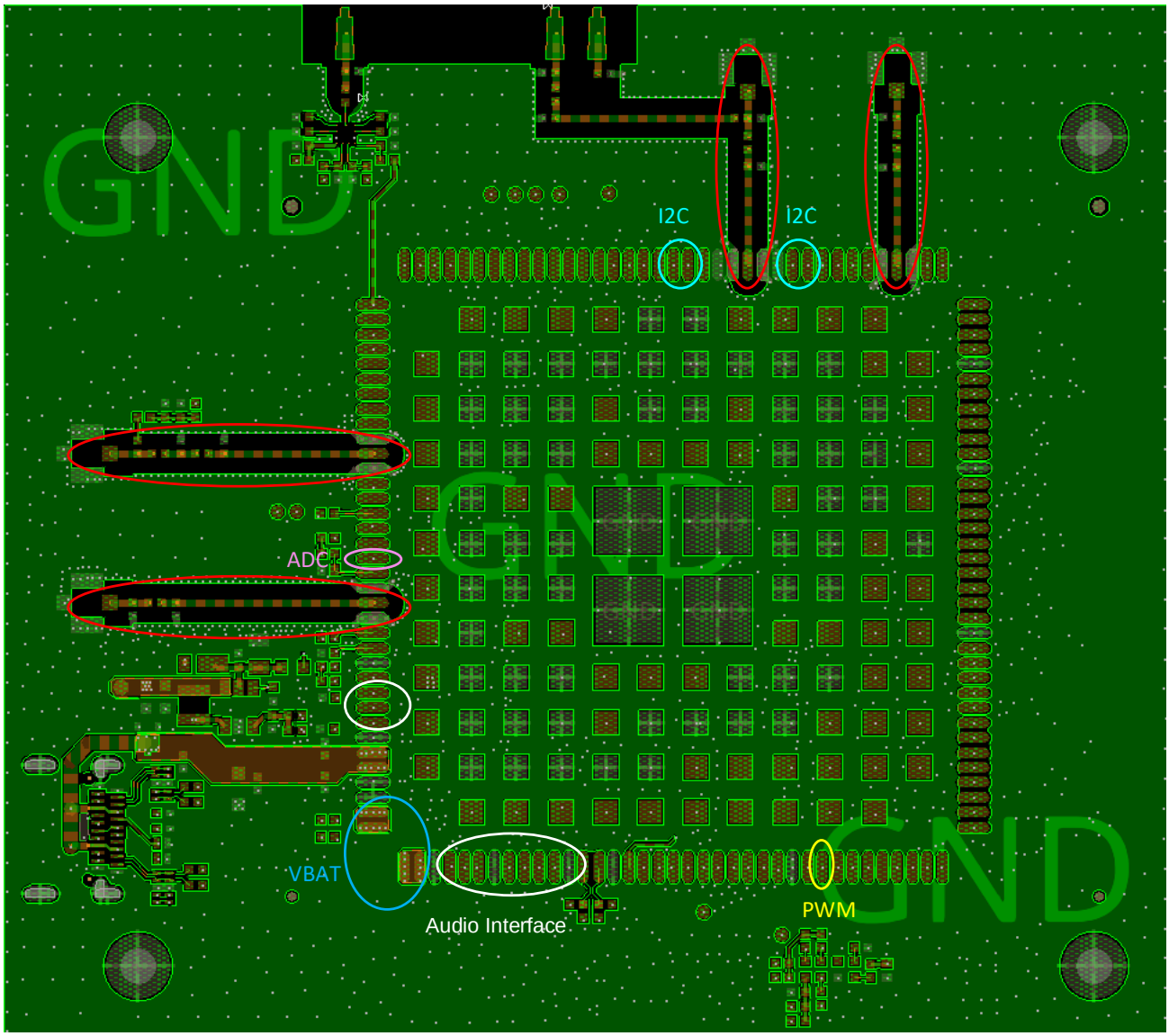

Figure 7: VBAT & Sensitive Signal Traces (SC200E-TE-A 1st Layer)

3.2. Charging Interfaces

3.2.1. USB_VBUS

USB_VBUS is used for USB charging, and the trace width should be at least 3 mm.

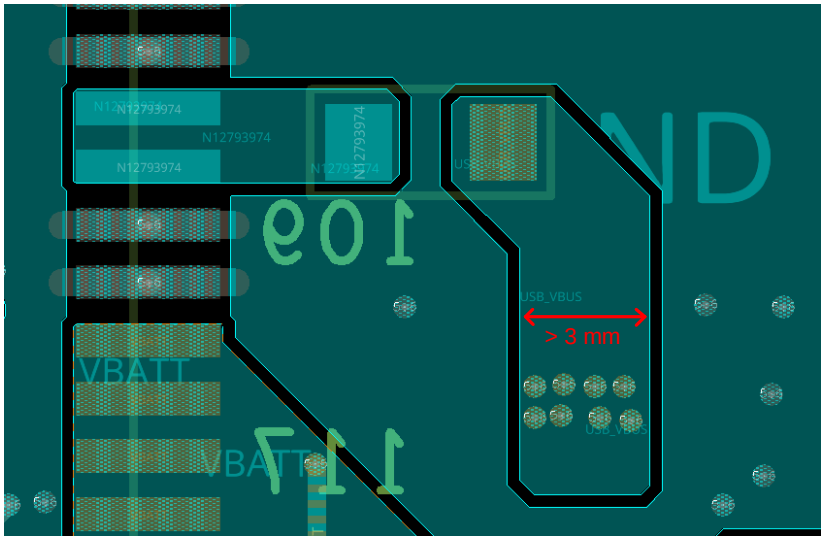

Figure 8: Overview of USB_VBUS Signal Trace (SC200E-TE-A Bottom Layer)

NOTE

For the module without charging function, USB_VBUS is used for USB detection only, the trace width for USB_VBUS is recommended to be 0.15 mm.

3.2.2. BAT_P/M (For SC200R Series Only) [2]

- BAT_P/M are used for battery voltage detection. They should be routed with total grounding as a differential pair.
- BAT_P/M should be connected to the battery connector directly to ensure accuracy of battery voltage detection.

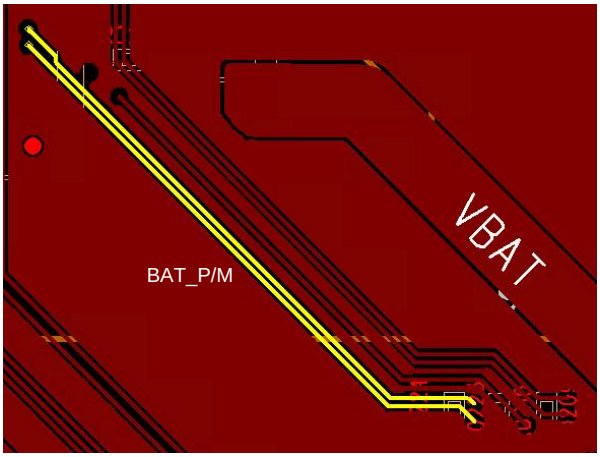

Figure 9: Overview of BAT_P/M Signal Traces (EVB-G2-V1.3 4th Layer)

[2] SC20 series, SC200E and SC206E series do not support BAT_P/M.

3.2.3. BAT_THERM

BAT_THERM is an analog input signal, which should be routed with total grounding.

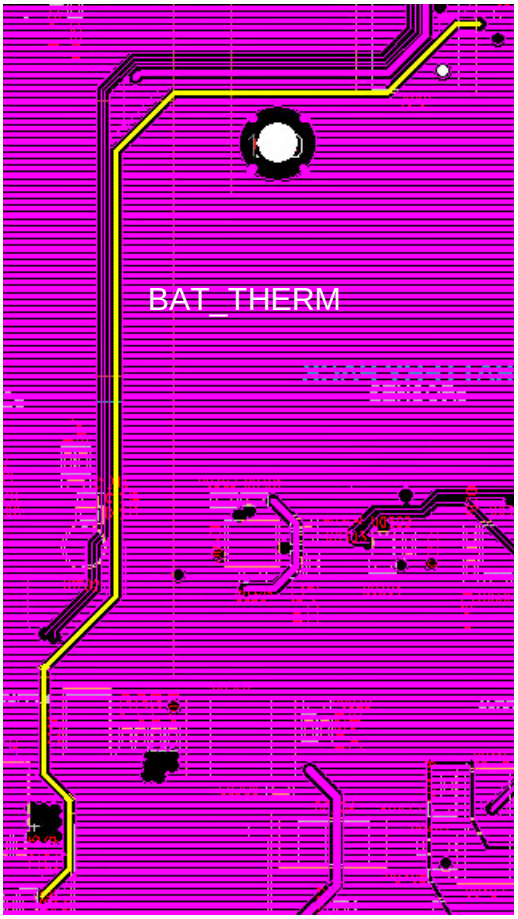

Figure 10: Overview of BAT_THERM Signal Trace (EVB-G2-V1.3 2nd Layer)

3.3. PWRKEY & RESET_N & VOL_UP & VOL_DOWN

- Surround PWRKEY, RESET_N and VOL_UP and VOL_DOWN signal traces with ground.
- Keep PWRKEY, RESET_N and VOL_UP and VOL_DOWN signal traces away from high current and interference sources.
- Make sure all signals should pass through TVS before connecting to the module's pin.
- ESD protection components for those signals needs to be placed near the keypad.

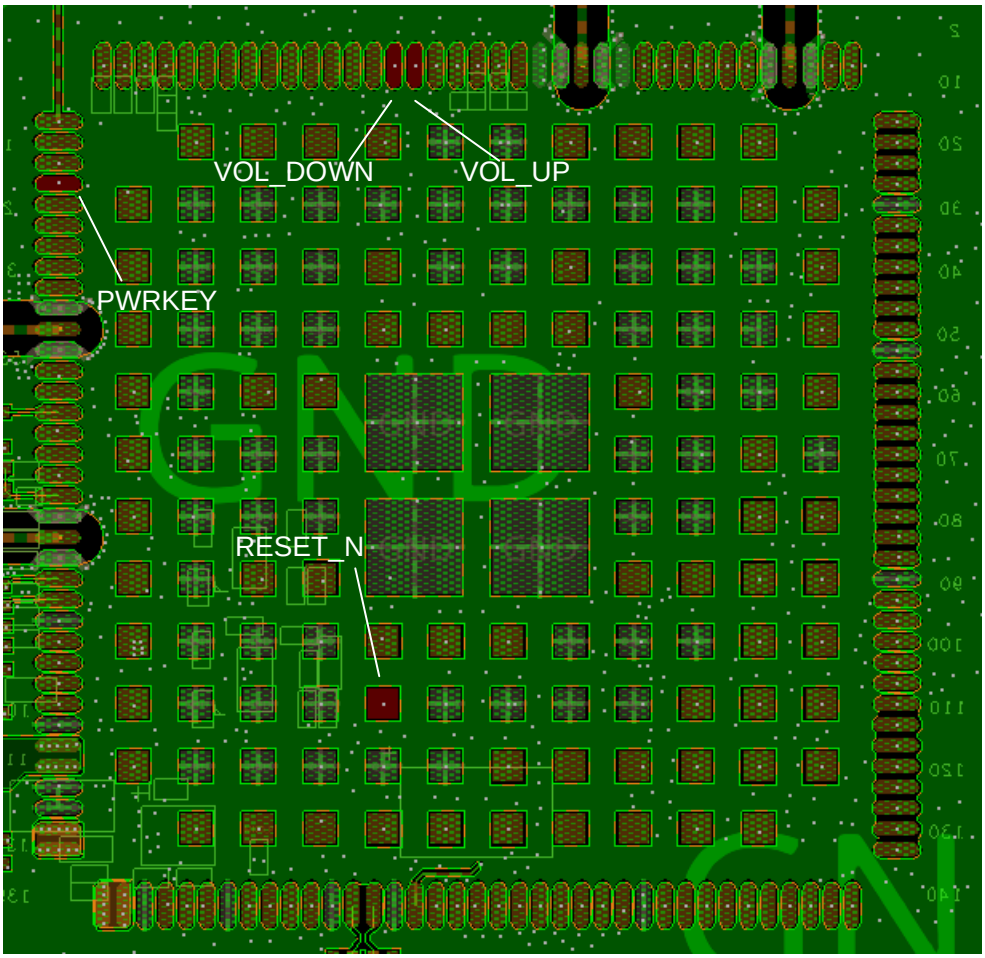

Figure 11: PWRKEY, RESET_N and VOL_UP/DOWN Traces (SC200E-TE-A 1st Layer)

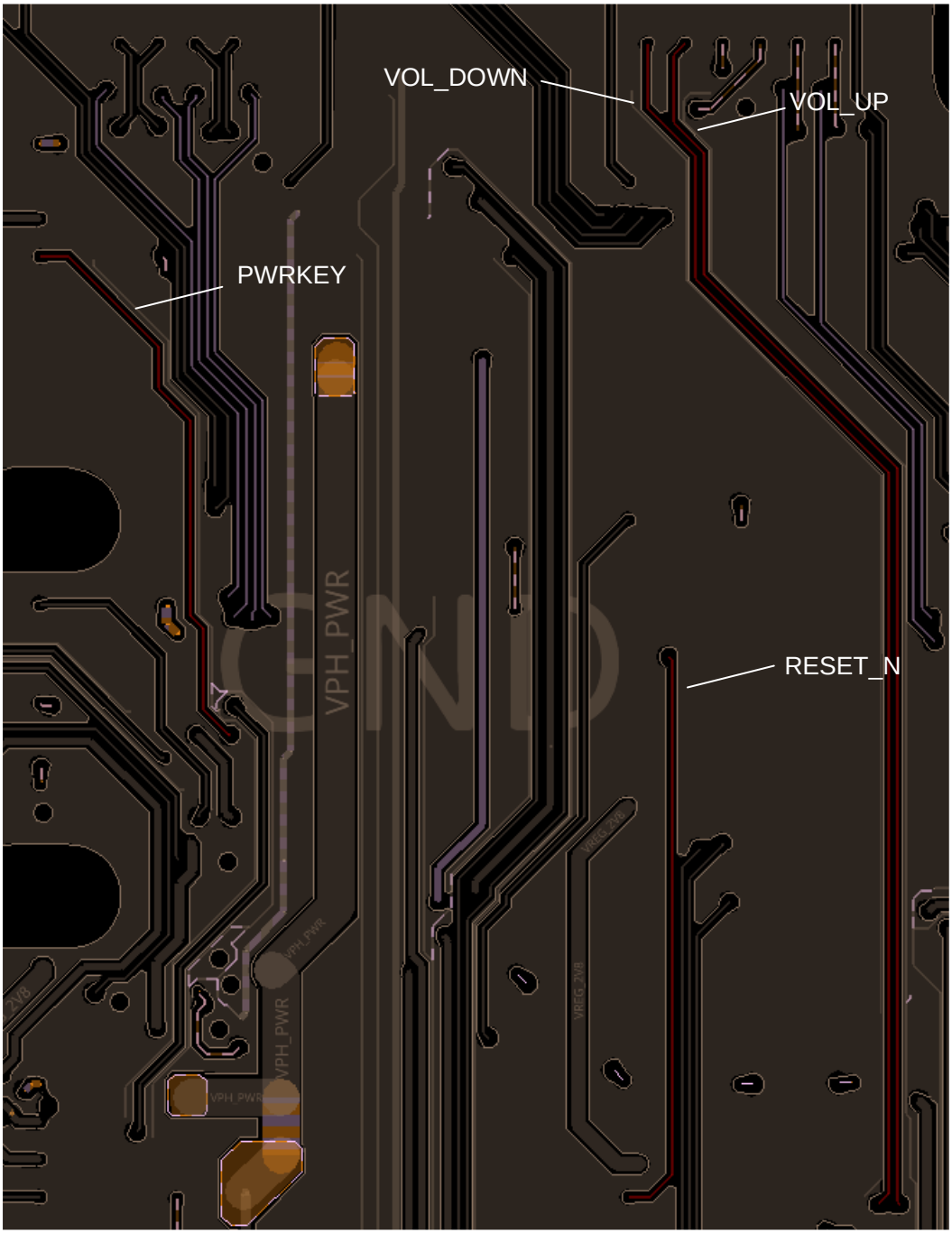

Figure 12: PWRKEY, RESET_N and VOL_UP/DOWN Traces (SC200E-TE-A 2nd Layer)

3.4. Power Supply Output

- If one LDO has multiple outputs, a star structure should be applied for those output traces.
- The filter capacitor for LDO shall be closed to the module pin.
- The trace width of an LDO is depended on the capability of its load current.

The following table takes SC200E series as an example. For the details of LDOs corresponding load current about SC200R series, SC20 series and SC206E series, see ***document [4]***, ***document [5]*** and ***document [6].***

Table 2: LDOs Corresponding Load Current (SC200E Series as an Example)

LDOs Name	Load Current
LDO15A_1V8	200 mA
LDO_IOVDD	300 mA
VDD_2V8	500 mA
LDO17A_3V0	192 mA

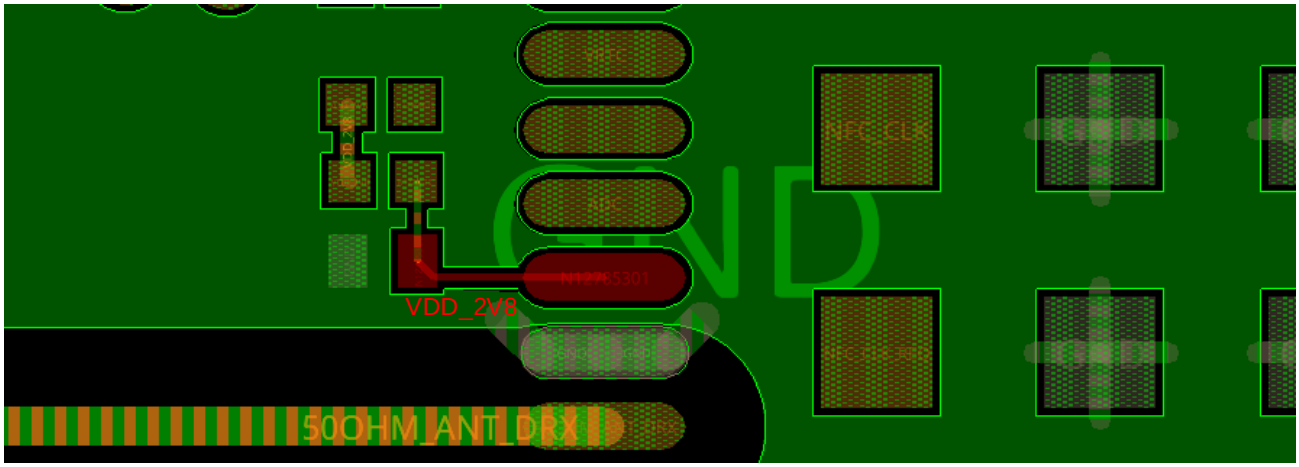

Figure 13: LDOs Traces (SC200E Series TE-A 1st Layer)

3.5. USB Interfaces

3.5.1. USB 2.0 Signals

- The spacing between USB_DP/USB_DM and other signal traces should be larger than 0.5 mm.
- Maintain the integrity of the reference plane and avoid crossing with signal traces on adjacent layers.
- Route USB_DP and USB_DM traces on the inner layer, with the differential impedance controlled to 90 Ω ±10 %.
- Keep the spacing and length between traces comparatively equal, with the length tolerance less than 6.6 mm (SC20 series), less than 2 mm (SC200E & SC206E series) and less than 7 mm (SC200R series).
- When a TVS needs to be added for USB_DP and USB_DM signal traces, place it close to USB connector and use a TVS with a junction capacitance of less than 2 pF.
- The USB 2.0 signal traces and interfaces should maintain a certain isolation from the RF antenna traces and layout.

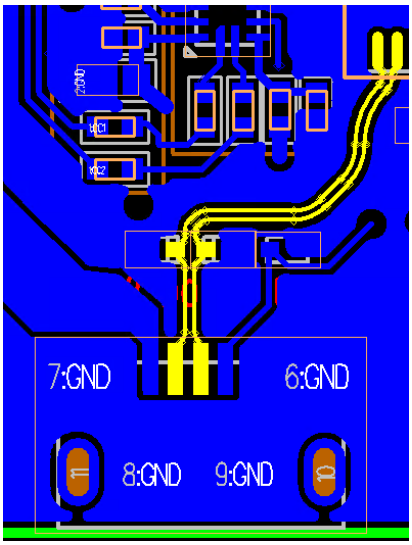

Figure 14: Overview of USB_DP/DM Signal Traces (EVB-G2-V1.3 1st Layer)

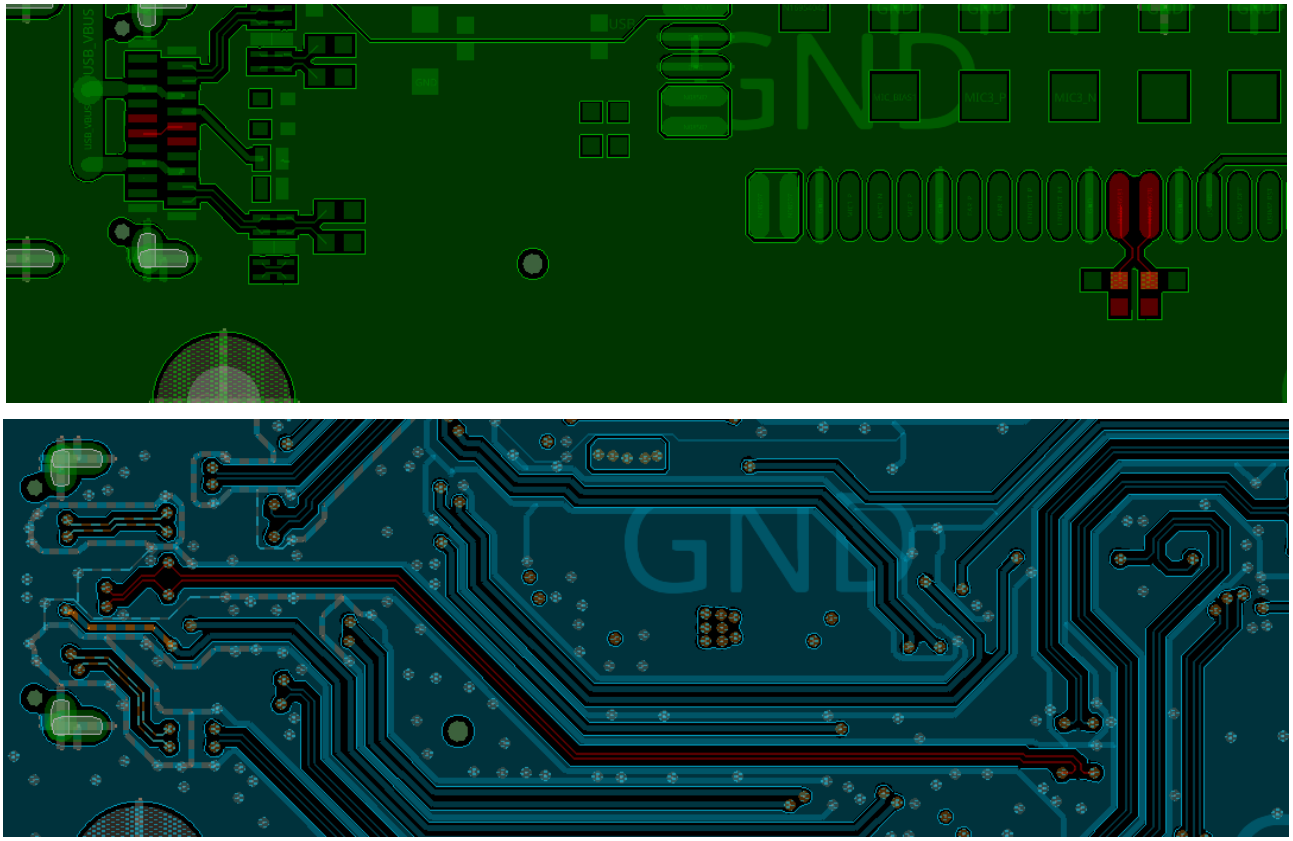

Figure 15: Overview of USB 2.0 Signal Traces (SC200E-TE-A 1st & 4th Layer)

3.5.2. USB 3.1 Signals (For SC200E & SC206E Series Only)

- The USB 3.1 signal traces and interfaces should maintain a certain isolation from the RF signal traces and the layout.
- Route the USB signal traces in the middle layer of the PCB and surround them with total grounding. Keep the USB trace away from RF, audio and clock traces.
- Place the peripheral devices as close to the module as possible. The general sequence: interfaces/connector→test points→TVS→common mode choke→module.
- Make sure the trace difference between USB 3.1 Tx/Rx differential pairs do not exceed 0.7 mm.
- Keep the impedance as 90 Ω ±10 % for differential pairs USB_TX_P/M and USB_RX_P/M. Spacing between the two differential pairs should be four times of the trace width to meet the isolation requirement.
- Ensure the isolation between the traces of USB 2.0 and USB 3.1 interfaces and the components of the two interfaces sufficient to avoid interference.
- Decrease the number of vias to avoid interference radiation. It is recommended to add more ground vias near the signal vias when the layer is changed.
- When a TVS needs to be added for USB_DP and USB_DM signal traces, place it close to USB connector and use a TVS with a junction capacitance of less than 0.5 pF for USB 3.1.

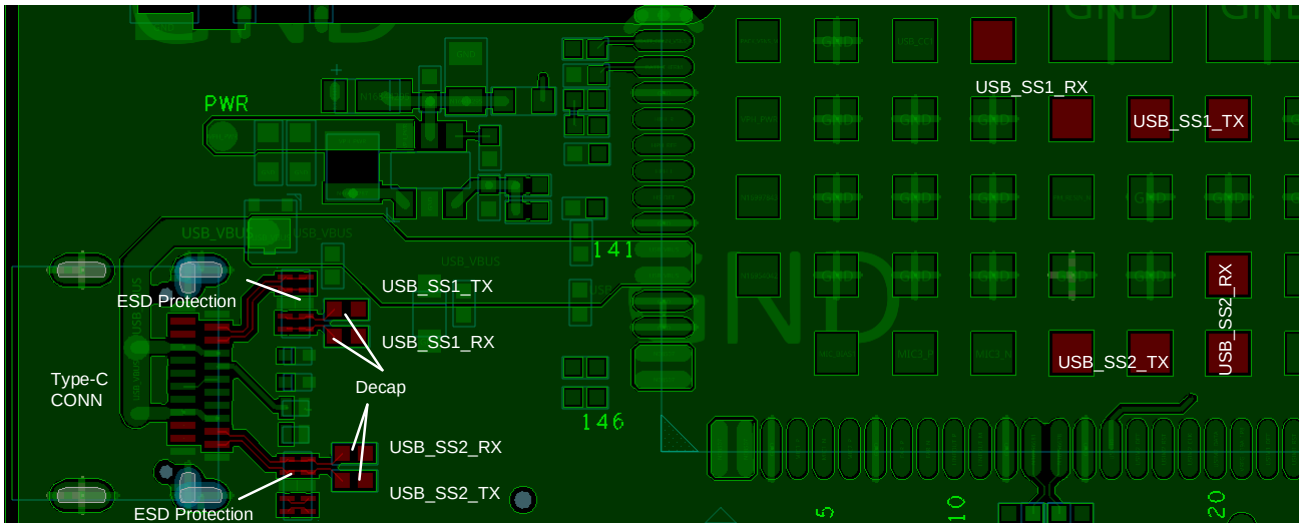

Figure 16: Overview of USB 3.1 Signal Trace (SC200E-TE-A 1st Layer)

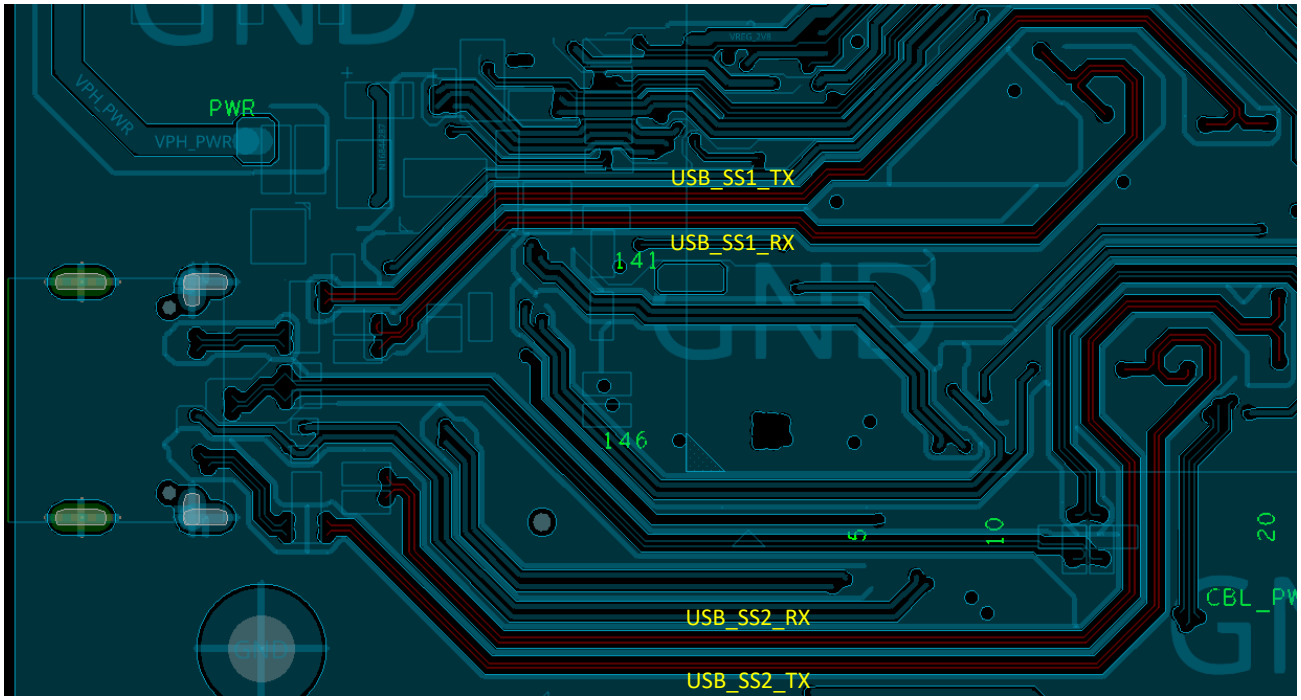

Figure 17: Overview of USB 3.1 Signal Traces (SC200E-TE-A 4th layer)

3.6. UART Interfaces

The recommended trace width for UART is 0.15 mm. Surround the UART traces with ground as much as possible.

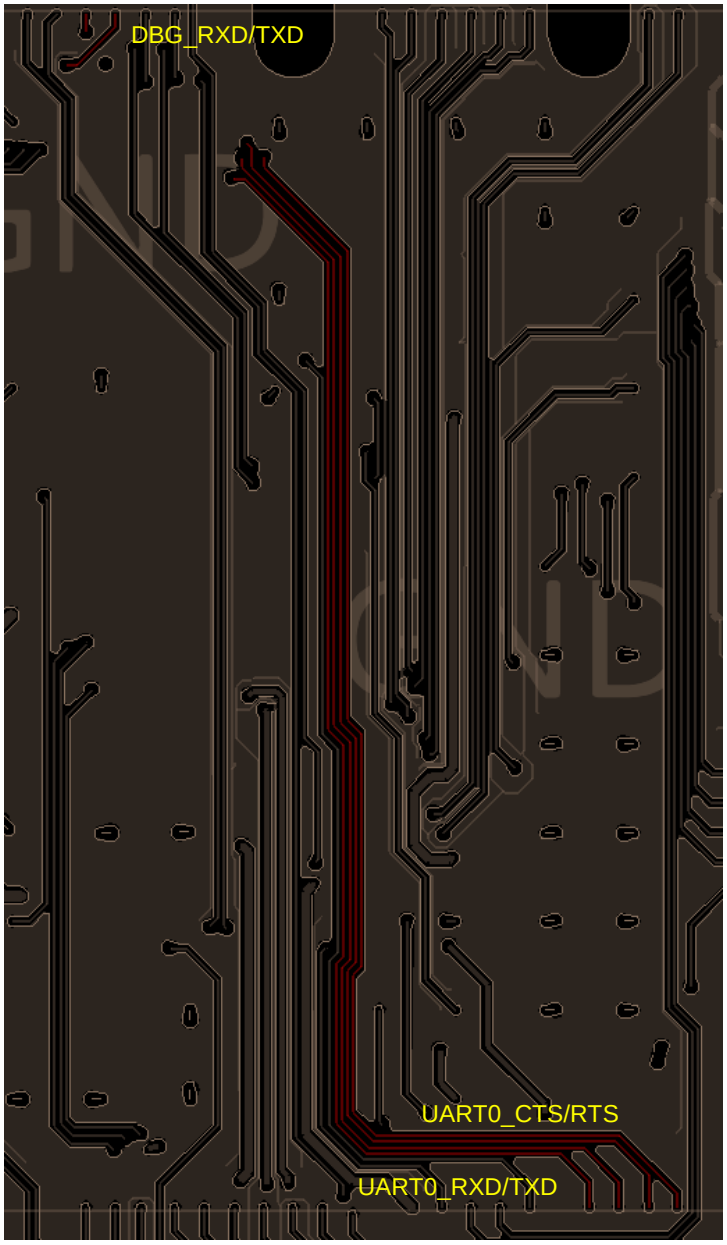

Figure 18: Overview of UART Signal Traces (SC200E-TE-A 2nd Layer)

3.7. TP Interface

- Keep TP connector away from RF antenna as far as possible to avoid RF interference.
- The ESD protection components are recommended to be close to corresponding pins of TP connector.
- Route I2C signal traces as a group and shield them with ground.
- The filter capacitors for TP power supply should be placed near the TP connector.

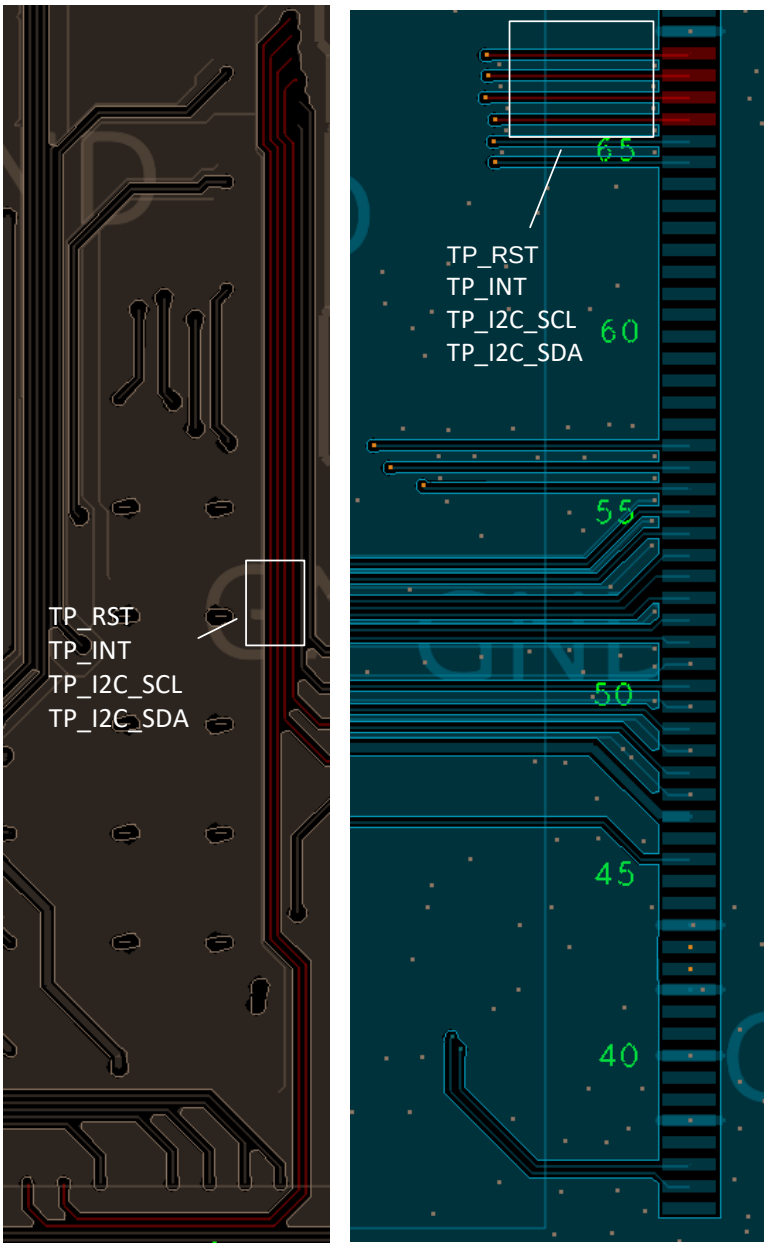

Figure 19: Overview of TP Signal Traces (SC200E-TE-A 2nd Layer, Bottom Layer)

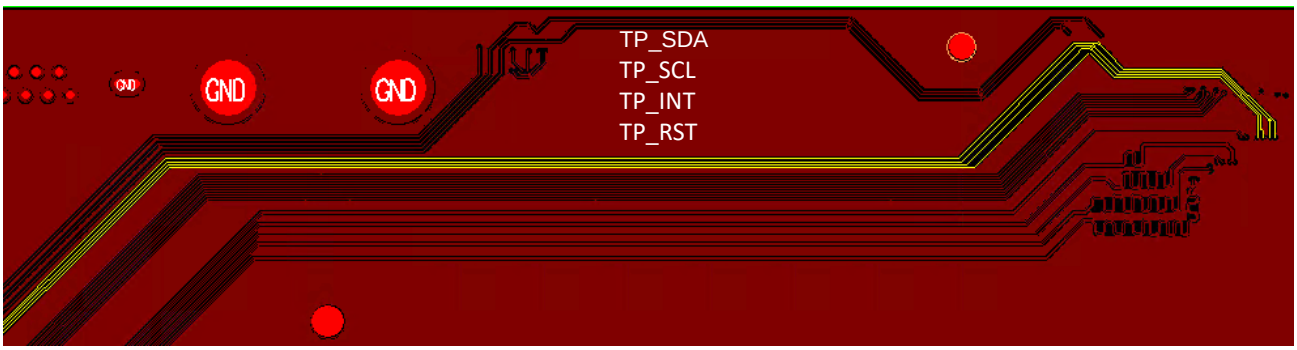

Figure 20: Overview of TP Signal Traces (EVB-G2-V1.3 Bottom Layer)

3.7.1. PWM

PWM should be shielded with ground to avoid interference.

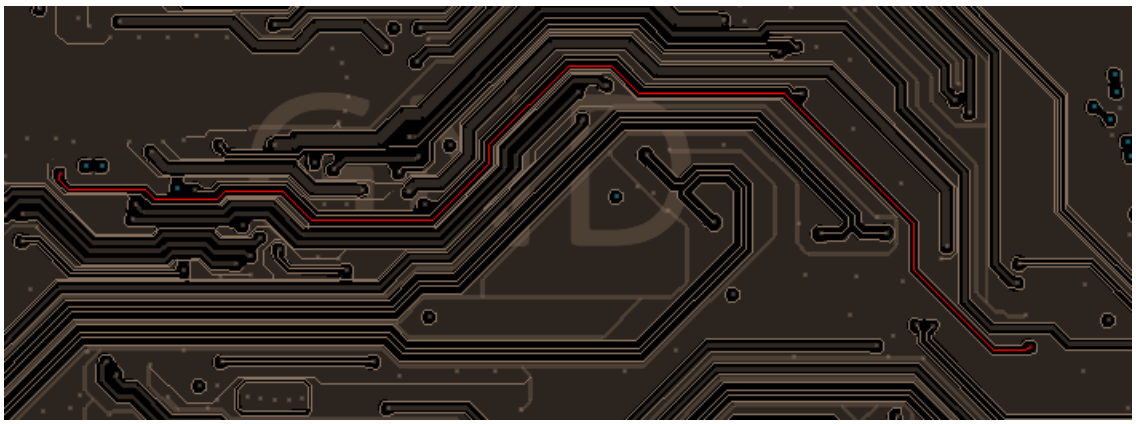

Figure 21: Overview of PWM Trace (SC200E-TE-A 4th Layer)

3.7.2. MIPI_DSI

- Keep the differential impedance of MIPI_DSI signal traces as 100 Ω ±10 %. To decrease EMI interference, route the MIPI_DSI signal traces in the inner layer of PCB with total grounding.
- To maintain a consistent differential impedance, try not to refer to different ground layers when keeping 100 Ω signal differential impedance.
- The total trace length of each MIPI_DSI signal is recommended to be less than 305 mm (SC20 & SC200R series) and less than 240 mm (SC200E & SC206E series).
- The intra-lane trace length matching of two differential MIPI_DSI pairs is recommended to be less than 0.67 mm (SC200R & SC20 series)/0.7 mm (SC200E & SC206E series).
- The inter-lane length difference of MIPI_DSI traces is recommended to be less than 1.3 mm (SC200R & SC20 series)/1.4 mm (SC200E & SC206E series).
- TVS and EMI protection components need to be added for MIPI signal traces, place it close to the connector and keep its junction capacitance less than 1 pF.

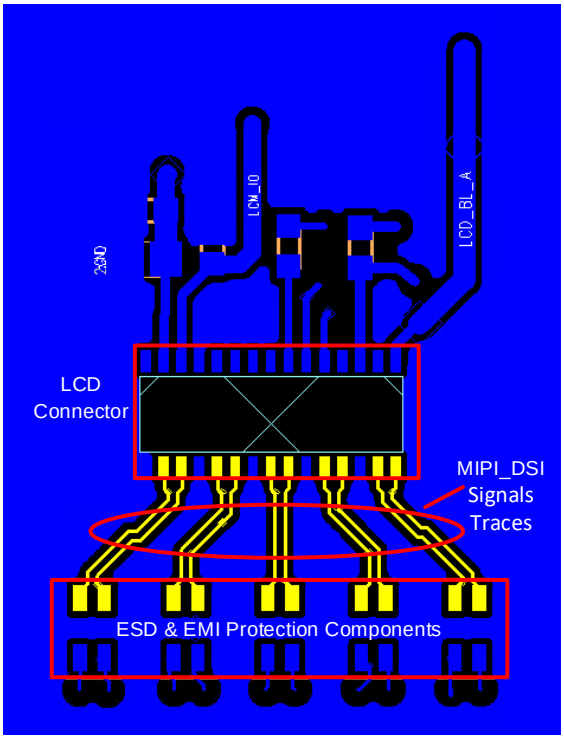

Figure 22: Overview of LCD MIPI_DSI Signal Traces (EVB-G2-V1.3 1st Layer)

3.8. Camera Interface

3.8.1. Camera Power Supply

- The trace width of the camera power supply depends on the camera requirements.
- All filter capacitors for the power supply should be placed near the camera connector.

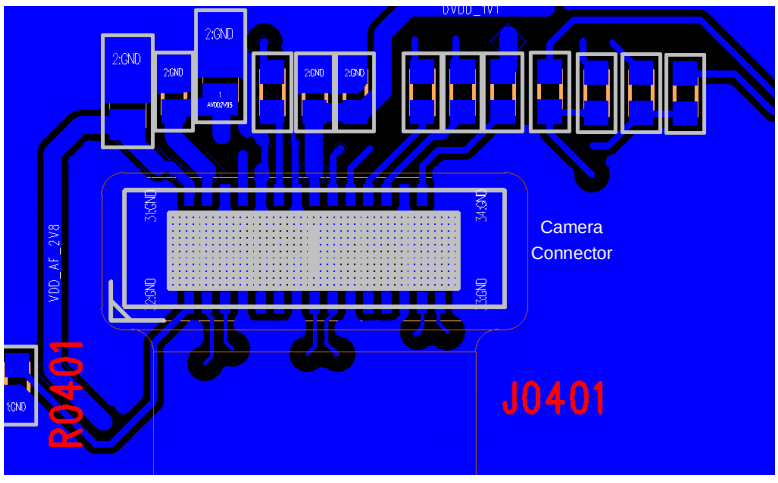

Figure 23: Overview of Camera Signal Traces (EVB-G2-V1.3 1st Layer)

3.8.2. Flashlight

- The recommended width of the flashlight's main current-carrying trace is at least 1 mm.
- Keep the flashlight's current trace ground shielded. Meanwhile, keep it away from sensitive signal traces such as high-speed signal traces, analog signal traces and I2C signal traces.

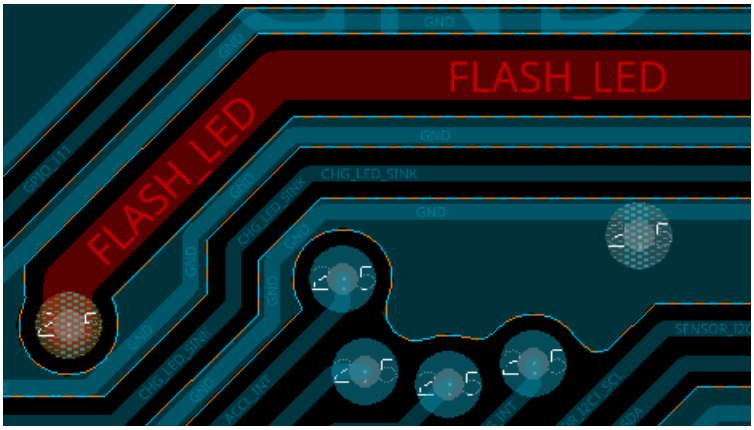

Figure 24: Overview of Flashlight Traces (SC200E-TE-A 4th Layer)

3.8.3. MIPI_CSI

- Keep the differential impedance of MIPI_CSI signal traces as 100 Ω ±10 %.
- To decrease EMI interference, try to route the MIPI_CSI signal traces in the inner layer of PCB with total grounding.
- To maintain a consistent differential impedance, try not to refer to different ground layers when keeping 100 Ω signal differential impedance.
- The total trace length of each MIPI_CSI signal is recommended to be less than 305 mm (SC20 & SC200R series) and less than 240 mm (SC200E & SC206E series).
- The intra-lane trace length matching of two differential MIPI_CSI pairs is recommended to be less than 0.67 mm (SC200R & SC20 series)/0.7 mm (SC200E & SC206E series).
- The inter-lane trace length matching of MIPI_CSI pairs is recommended to be less than 1.3 mm (SC200R & SC20 series)/1.4 mm (SC200E & SC206E series).
- TVS and EMI protection components need to be added for MIPI signal traces, place them close to the connector and keep their junction capacitance less than 1 pF.

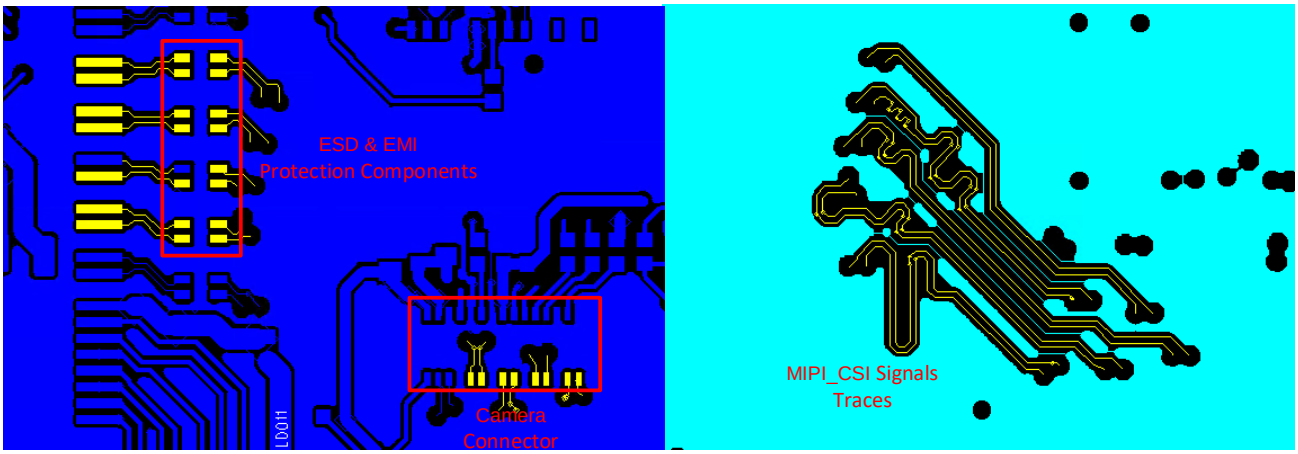

Figure 25: Overview of Camera MIPI_CSI Signal Traces (EVB-G2-V1.3 1st and 3rd Layer)

3.9. SPI and I2C Interface

As a pair, I2C_SDA and I2C_SCL should be surrounded with ground.

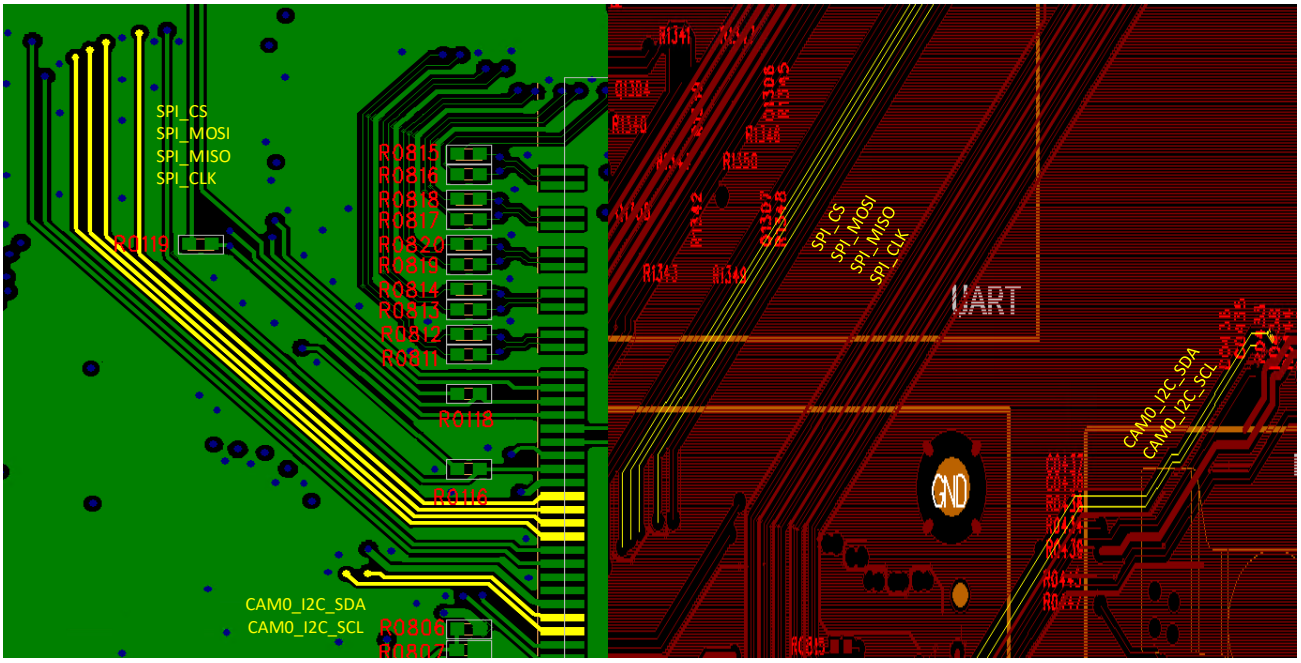

Figure 26: Overview of I2C and SPI Signal Traces (EVB-G2-V1.3 1st and 3rd Layer)

3.10. Audio Interfaces Design

- ESD protection components should be placed near the audio devices or audio interfaces.
- The capacitors for filtering out RF interference signals on PCB should be placed as close to the audio devices or audio interfaces as possible.
- The recommended trace width for the MIC differential pair (SC200E & SC206E series) is at least 0.15 mm, and the traces should be ground shielded.
- The recommended trace width for the EAR_P/M differential pair is at least 0.25 mm, and the trace should be ground shielded.
- The recommended trace width for the LINEOUT_P/M (SC200E & SC206E series) differential pair is at least 0.2 mm. The traces should be as wide and short as possible and should be ground shielded.
- The recommended trace width for the SPK_P/N (SC20 & SC200R series) differential pair is at least 0.6 mm. The traces should be as wide and short as possible and should be ground shielded.
- HPH_R/L should be ground shielded separately, or HPH_GND should be routed between HPH_R and HPH_L. The trace width of HPH_GND is recommended to be at least 0.25 mm.
- Keep RF antenna traces away from the traces of audio devices to reduce radiation interference.
- Keep power supply traces far away from the audio traces and do not route them in parallel.

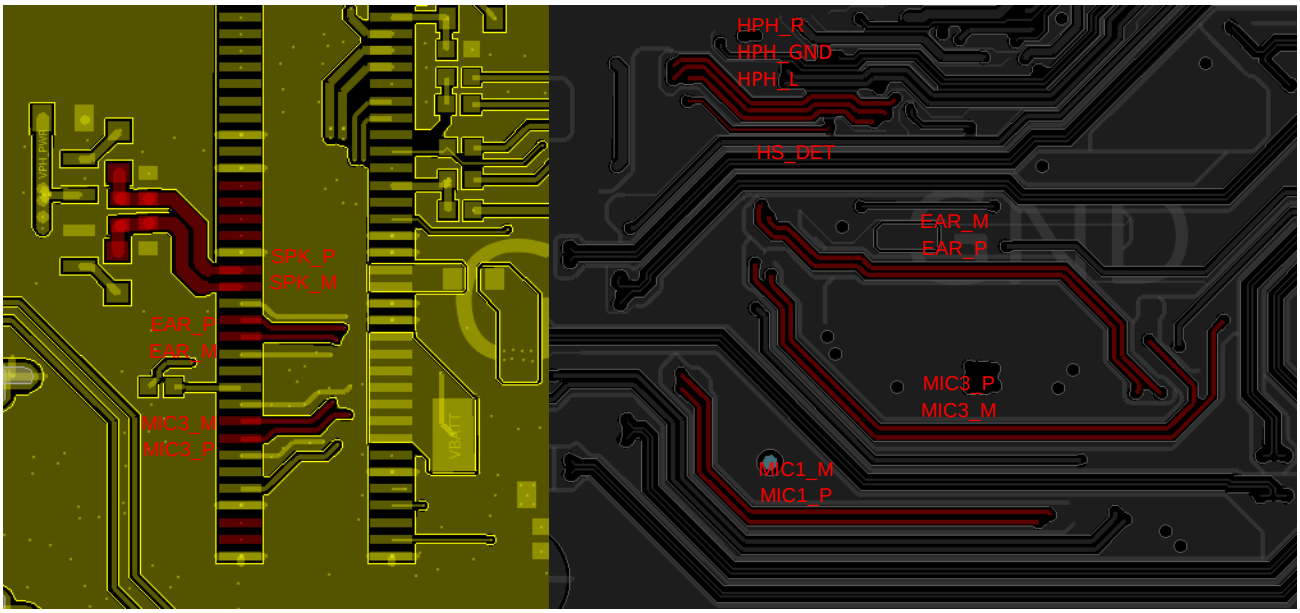

Figure 27: Overview of Analog Audio Signal Traces (SC200E-TE-A 4th and Bottom Layer)

3.11. SD Card Interface

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and Analog signals, as well as noisy signals such as clock and DC-DC signals.
- Keep the impedance of SDIO signal traces between 50 Ω ±10 %, maintaining the integrity of the reference plane. SD_CLK and SD_CMD should be surrounded with ground on the layer and ground planes above and below. If the space is limited, the SD_DATA0 to SD_DATA3 could be surrounded with ground together.
- Trace length requirements:
  1) If data rate reaches to 50 Mbps, the length should be less than 70 mm;
  2) If data rate is up to 104 Mbps, the length should be less than 50 mm.
- If a SD card is applied, place a TVS close to the SD card connector, and the junction capacitance of ESD protection components should be smaller than 3 pF.
- The capacitive reactance of data signal trace should be less than 5 pF.
- The total trace length difference between CLK and other signal traces should not exceed 1 mm.

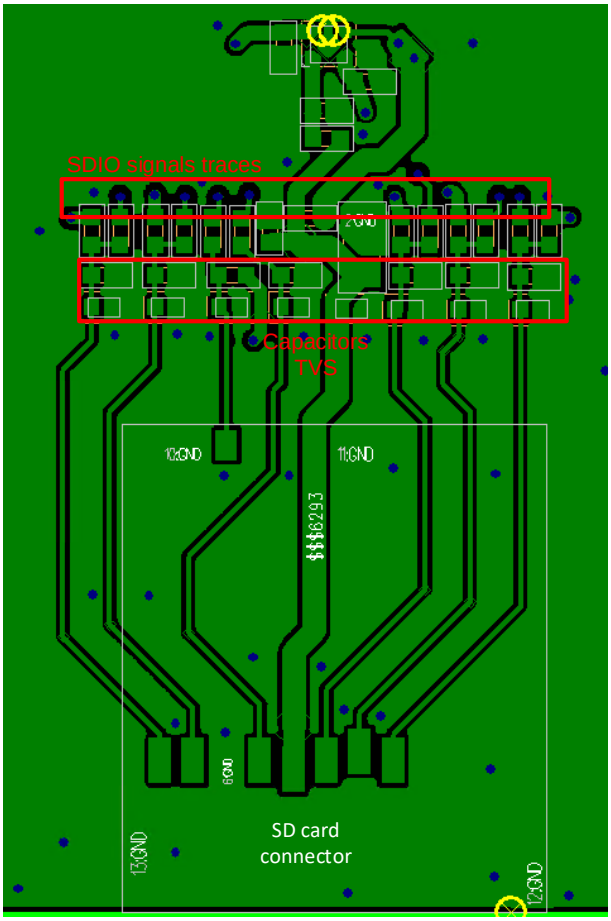

Figure 28: Overview of SD Card Signal Traces (EVB-G2-V1.3 1st Layer)

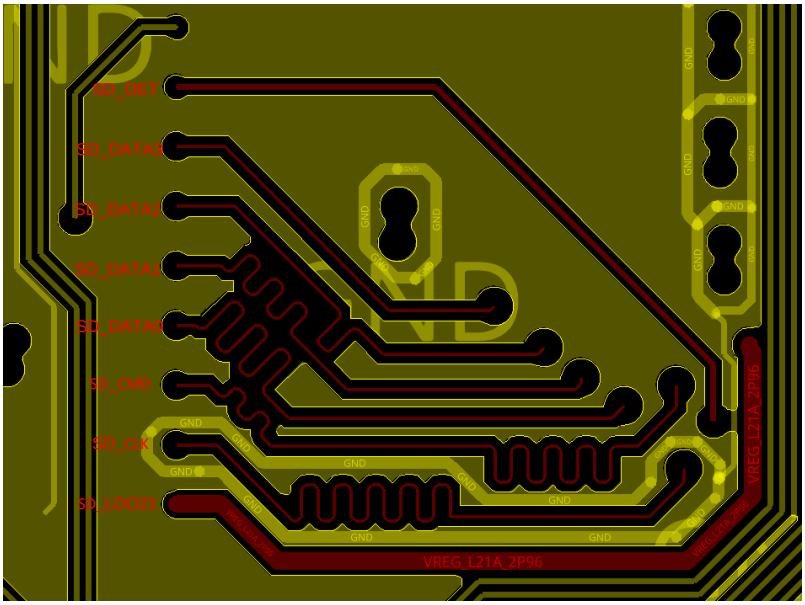

Figure 29: Overview of SD Card Signal Traces (SC200E-TE-A 2nd Layer)

3.12. (U)SIM Interface

- The total length of each (U)SIM signal trace should be less than 200 mm.
- Isolate USIM_CLK and USIM_DATA with ground plane to avoid the interference between each other.
- Put the peripheral components such as a TVS, capacitors and resistors near the (U)SIM card connector. The junction capacitance of the USIM signal trace should be less than 50 pF (SC200R & SC20 series) and less than 10 pF (SC200E & SC206E series).

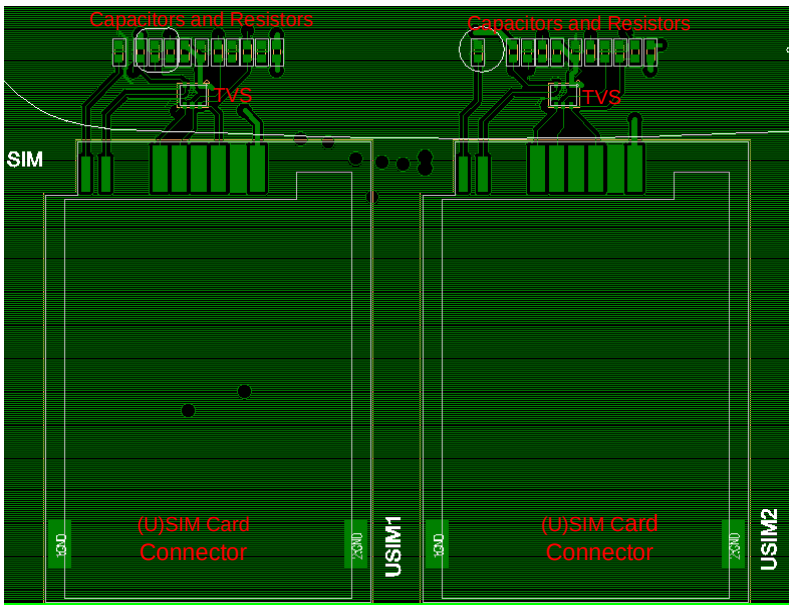

Figure 30: Overview of (U)SIM Signal Traces (EVB-G2-V1.3 4th Layer)

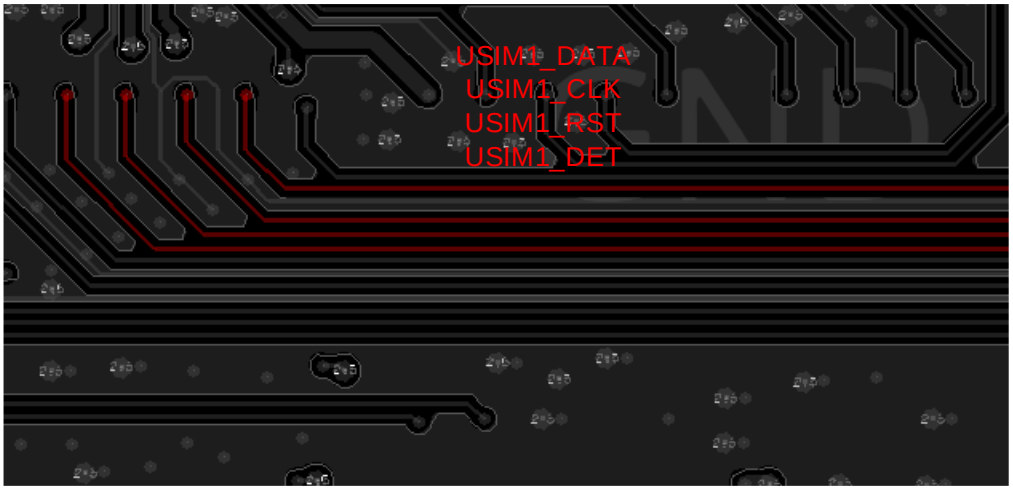

Figure 31: Overview of (U)SIM Signal Traces (SC200E-TE-A 2nd Layer)

3.13. ADC Interface

ADC signal traces should be surrounded with ground.

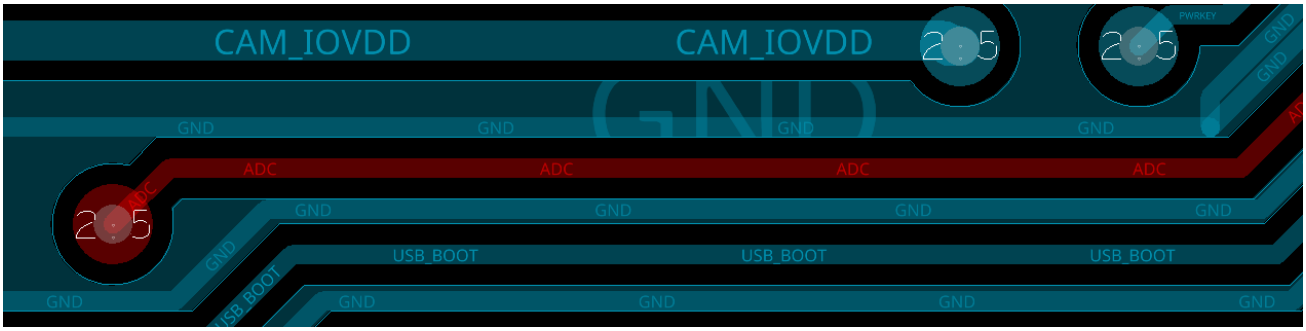

Figure 32: Overview of ADC Signal Traces (SC200E-TE-A 4th Layer)

3.14. USB_BOOT

- The recommended trace width for USB_BOOT is 0.15 mm.
- Place the TVS for USB_BOOT close to USB_BOOT interface.

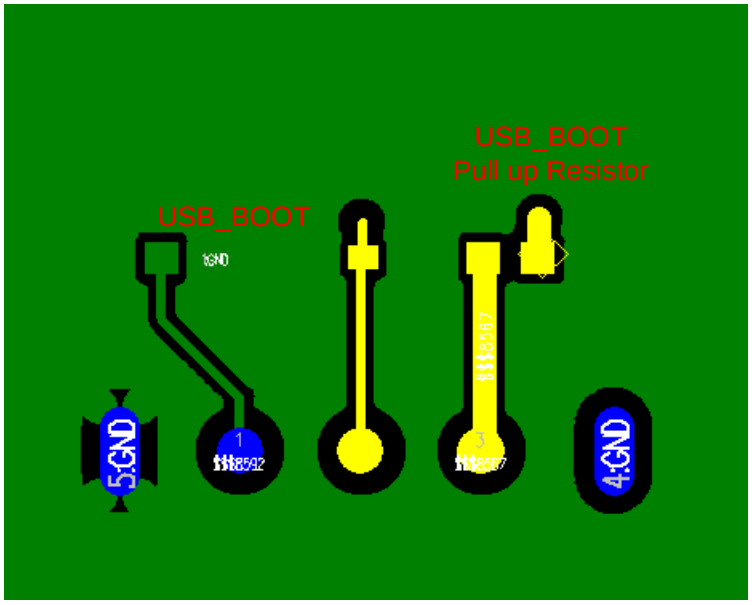

Figure 33: Overview of USB_BOOT Signal Traces (EVB-G2-V1.3 1st Layer)

3.15. RF Interfaces

3.15.1. PCB Structures of Microstrip and Coplanar Waveguide (CPWG)

3.15.1.1. PCB Structure of Microstrip Waveguide

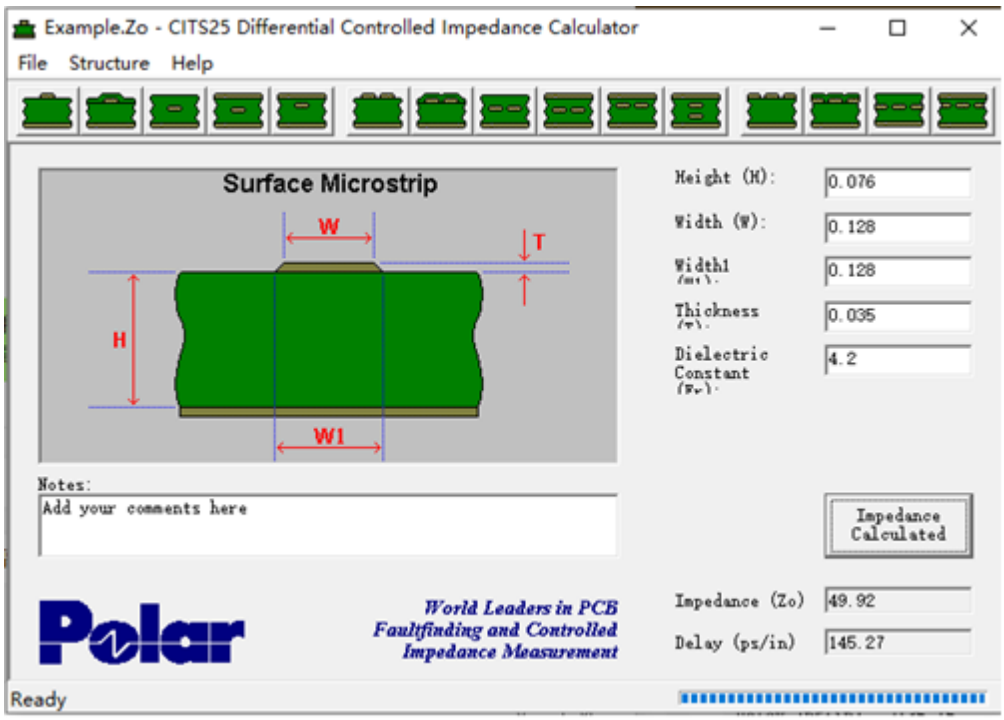

Figure 34: PCB Structure of Microstrip Waveguide

3.15.1.2. PCB Structure of CPWG

Factors affecting impedance include dielectric constant (4.2–4.6 usually, 4.4 here), dielectric layer height (H), RF trace width (W), spacing(S) between RF traces and ground, and copper thickness (T). When T = 0.035 mm, the following table lists the recommended values of W and S for 50 Ω CPWG under different PCB structures.

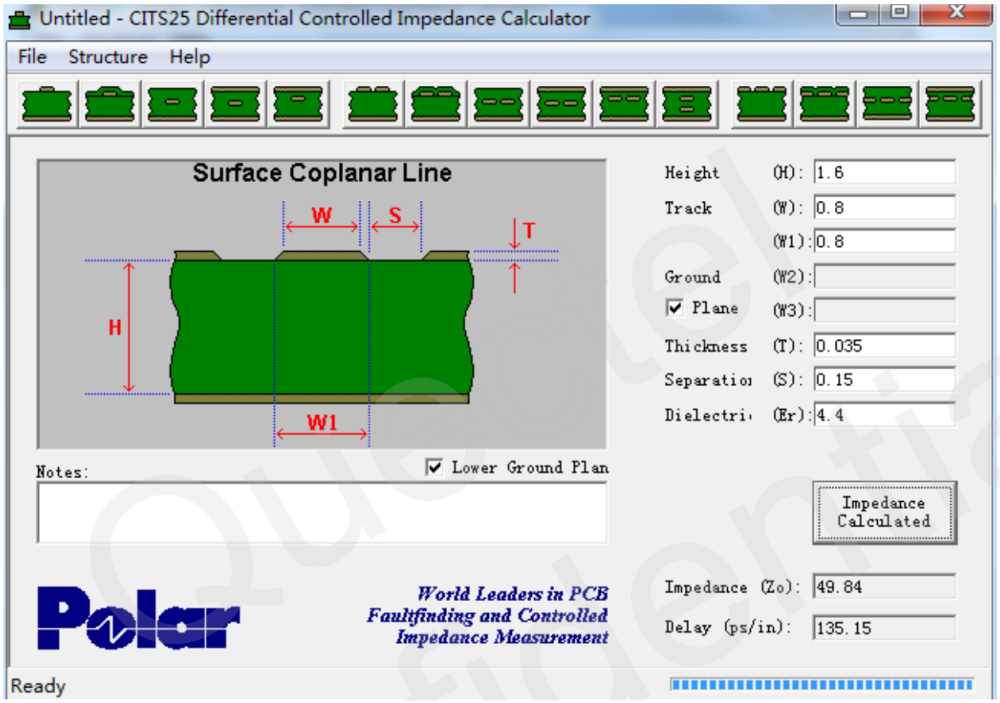

Figure 35: PCB Structure of CPWG

Table 3: Recommended Values of W and S for 50 Ω CPWG Under Different PCB Structures (Unit: mm, Dk = 4.4)

Dielectric Height (H)	RF Trace Width (W)	Spacing Between RF Trace and the Ground (S)
0.076	0.1188	0.15
0.1	0.1623	0.2
0.15	0.24	0.2
0.8	0.8	0.18
1.0	0.8	0.17
1.2	0.8	0.16
1.6	0.8	0.15
2	0.8	0.14

3.15.2. Reference Design of RF Layout

The characteristic impedance of all RF traces should be controlled at 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or CPWG is typically used in RF layout to control characteristic impedance.

Figure 36 and ***Figure 37*** show the examples of using the second layer as the reference ground layer for microstrip and CPWG respectively. In a multi-layer reference ground scenario, the inner layers should have a keepout area of width not less than 5 times the trace width. ***Figure 38*** and ***Figure 39*** show the examples of using the third layer for reference ground and fourth layer for reference ground respectively.

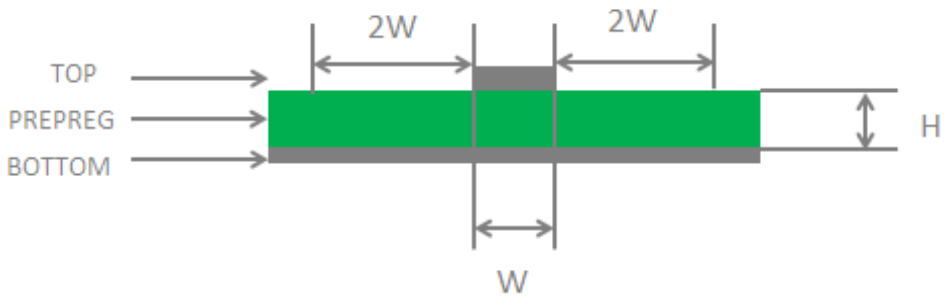

Figure 36: Microstrip Design on a 2-layer PCB

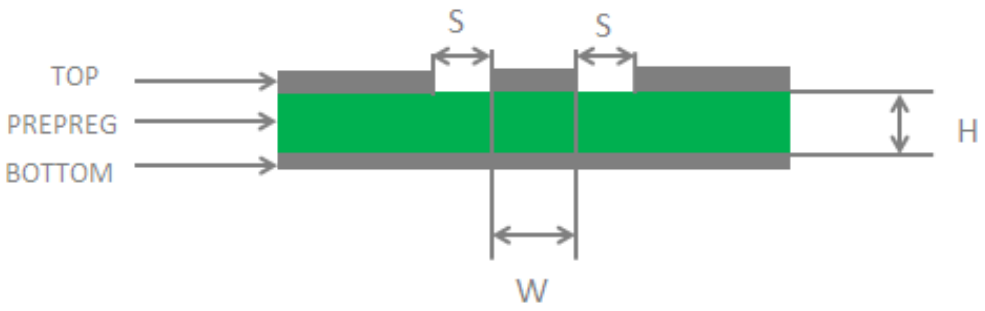

Figure 37: CPWG Design on a 2-layer PCB

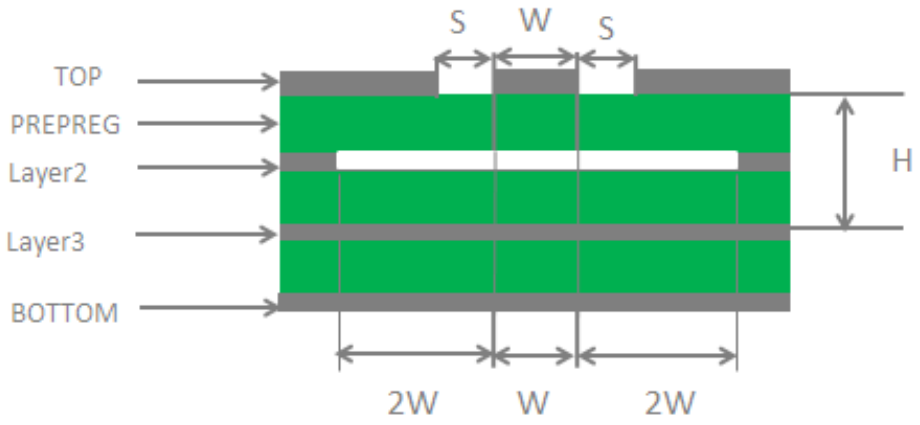

Figure 38: CPWG Design with Layer 3 as Reference Ground

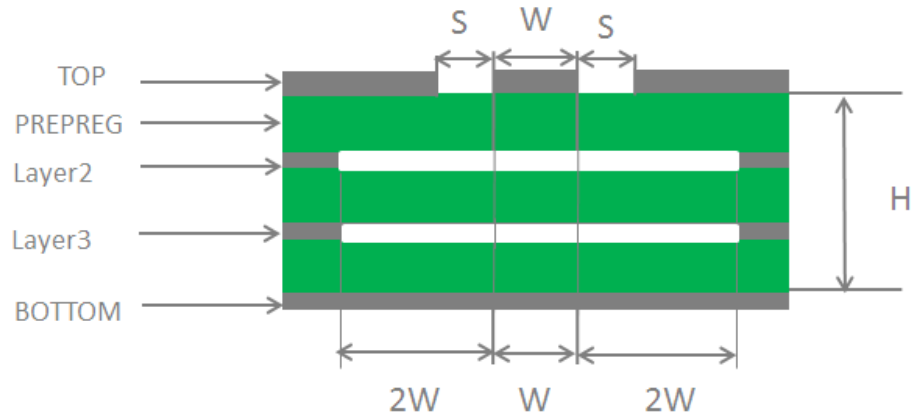

Figure 39: CPWG Design with Layer 4 as Reference Ground

3.15.3. Recommended Component Placement

- Keep the RF ports at the edge of the PCB, and away from other circuits.
- Avoid vias and layer changes when routing RF traces.
- Keep the RF traces and components as far away as possible from CPU, DRAM, Flash, DC-DC converters and Display FPC connectors.
- Keep the high-speed traces between CPU and SDRAM/Flash/Display FPC connectors as short as possible, and surround these traces in inner layers with ground on that layer and with ground planes above and below. Using GND vias around RF traces leading to antenna could improve RF performance.

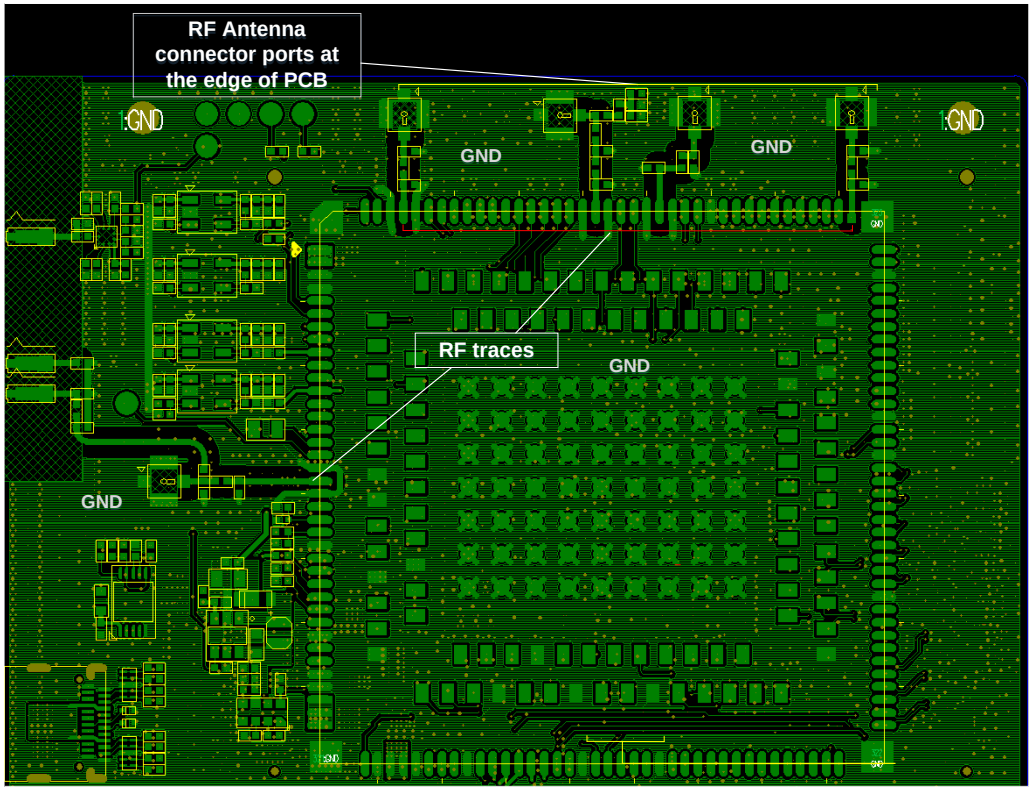

Figure 40: CPWG Design On a 2-layer PCB

3.15.4. PCB Layout Considerations of CPWG

There are a few PCB layout guidelines that should be taken into consideration for CPWG. Each guideline corresponds to the marks in the following two figures respectively.

1. Control the trace width (W) and the spacing between RF traces and ground (S) corresponding to the 50 Ω CPWG. Extra care should be taken by the PCB manufacturers in controlling the accuracy of W and S.

2. Avoid thermal relief pads along the reference ground of the RF traces.

3. Keep RF traces as short as possible. Avoid right-angle routing for RF traces, a 135 degrees turn is recommended.

4. Follow the recommended layout from the RF connector's manufacturer. The recommended PCB land pattern should dictate the distance between the signal pad and ground.

5. The CPWG RF trace should be fully surrounded by reference ground plane. Increase the number of GND vias for better return current of RF signal. Generally, the spacing between GND vias and RF traces should be less than two times of trace width. Both the planar and backed reference ground

planes for the RF traces should be complete, and ideally kept as large as possible.

6. The pads for π-type matching circuit consisting of a resistor and two capacitors should be near the module's antenna pins.

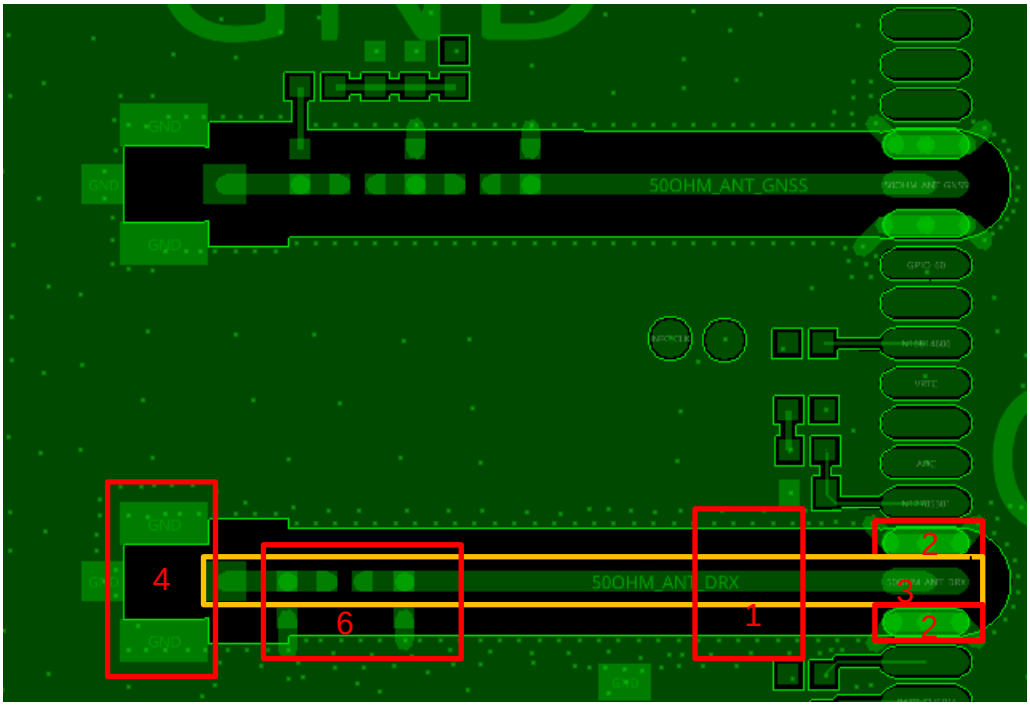

Figure 41: Overview of RF Traces (SC200E-TE-A 1st Layer)

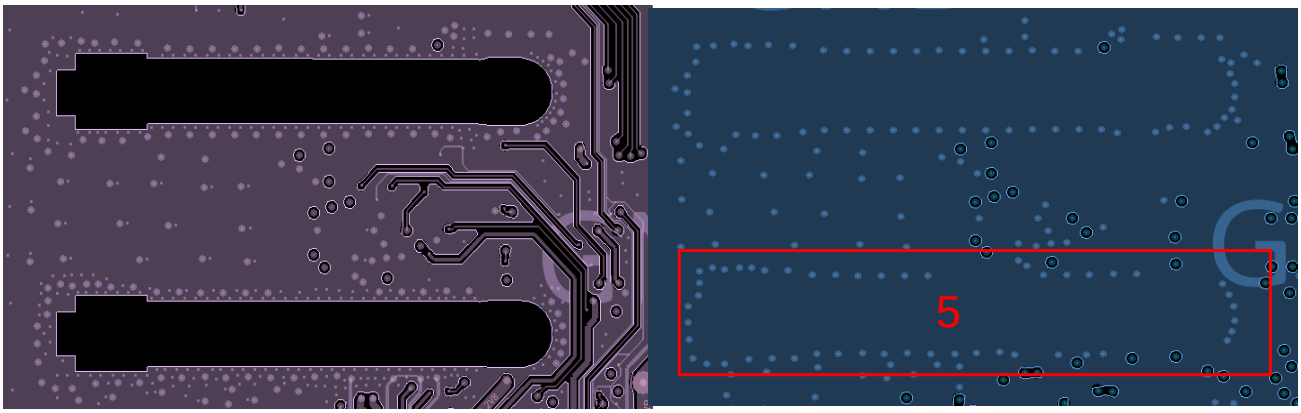

Figure 42: Overview of RF Traces (SC200E-TE-A 2nd and 3rd Layers)

4 Thermal Design

For more details of the thermal design of the PCB, see ***document [7].***

5 Appendix References

Table 4: Related Documents

Document Name
[1] Quectel_SC200E&SC206E_Series_Footprint&Part
[2] Quectel_SC200R_Footprint&Part
[3] Quectel_SC20_Footprint&Part
[4] Quectel_SC200R_Series_Hardware_Design
[5] Quectel_SC20_Series_Hardware_Design
[6] Quectel_SC200E&SC206E_Series_Hardware_Design
[7] Quectel_Module_Thermal_Design_Guide
[8] Quectel_RF_Layout_Application_Note

Table 5: Terms and Abbreviations

Abbreviation	Description
AC	Alternating Current
ADC	Analog-to-Digital Converter
CPU	Central Processing Unit
DRAM	Dynamic Random Access Memory
Dk	Dielectric Constant
DSI	Display Serial Interfaces
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge

EVB	Evaluation Board
FPC	Flexible Printed Circuit Board
I2C	Inter-Integrated Circuit
LCD	Liquid Crystal Display
LDO	Low Dropout Regulator
MIPI	Mobile Industry Processor Interfaces
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RF	Radio Frequency
SD	Secure Digital
SDIO	Secure Digital Input and Output Card
SDRAM	Synchronous Dynamic Random-Access Memory
SMD	Surface Mount Device
SPI	Serial Peripheral Interfaces
TP	Touch Panel
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery