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 1 // Simple SPI interface example
 2 // for now only supports Master->Save communication for 2 devices
 3 interface SPIbus;
 4   logic mosi,sck;
 5   wire miso;
 6   logic [1:0] ss;
 7   modport Master (input miso, output mosi, sck, ss);
 8   modport Slave (input mosi, sck, ss, inout miso);
 9 endinterface
10
11 interface SPIctrl;
12   logic [7:0] toXmit;   // value to be transmitted by master or slave
13   reg [7:0] Rcvd;       // data value recieved by master or slave
14   logic strobe;         // tell device that there is data on toXmit available
15   reg Ready;            // slave or master indicates data on Rcvd is ready to use
16   reg XmitFull;         // = 1 if input buffer already full, not ready for new data
17   logic [1:0] ss;       // tell master how to set slave select lines
18   logic busy;           // 1 if master or slave already busy transmitting current
byte
19   modport Master (input toXmit, strobe, ss, output Rcvd, Ready, XmitFull, busy);
20   modport Slave  (input toXmit, strobe, output Rcvd, Ready, XmitFull, busy);
21   modport System (output toXmit, strobe, input Rcvd, Ready, XmitFull);
22 endinterface
```