Project Objective

- Learning how to program the 7-segments in DE2-115 Board.
- Writing an application code that operates the counter and pattern on the 7-segments.
- Writing an application code that operates the BCD to 7-segments, where A, B, C, D are the input lines and a, b, c, d, e, f, g are the output lines, and this output will be given to the 7-segment which displays the decimal number depending on the inputs.

Hardware Requirements

a. Use the same system that you designed in project2 and only remove the counter and pattern LEDs PIO components from the design.

b. Add five new PIO components to your system which represent the first five 7-segment in FPGA board. Add two more PIO components, one for the decoder input which represents the BCD inputs and the other for speed controller for the pattern and counter operation. Table.1 shows the components' features that you need to set it up.

   1. The first column shows that I/O pins that will be used in the Verilog code and connected with the exported signal of your nios system.
   2. The second and third columns show the PIO direction and width respectively that you need to specify when you select the component from IP Catalog.
   3. The fourth column shows the name that you need to rename the component with when you add it to your nios system. The fifth column shows the signal name that will be exported in the conduit signal.

c. Update the Verilog code as shown in the attached Verilog file.

Table 1: Hardware Settings

PIO board device	Direction	Width	Name	Conduit name
HEX0[7:0]	output	8-bit	segment0	seg0
HEX1[7:0]	output	8-bit	segment1	seg1
HEX2[7:0]	output	8-bit	segment2	seg2
HEX3[7:0]	output	8-bit	segment3	seg3
HEX4[7:0]	output	8-bit	segment4	seg4
PIO	input	4-bit	bcd_input	bcdin
PIO	input	1-bit	speed_controller	spcont

Software Requirements

a. You are required to write an application software that executes the functions described in Table.2 based on the values of the system mode as explained in the table.

Table 2: Software Functions

System Mode	SW [1:0]	Function
1	01	Decoder operation. Your decoder input is 4-bit, and the output is 8-bit. The decoder inputs are implemented by the four switches (SW5, SW4, SW3, SW2). The output of the decoder should be displayed on the fifth 7-segment unit in the board.
2	10	A counter starts incrementing from 0x00 to 0xFF, and the value displays on the first two 7-segments. If the mode changes, the counter stops on latest number. If the mode changes back to 1, the counter restarts.
3	11	A random pattern starts, and the value displays on the second two 7-segments. If the mode changes, the pattern stops on latest value.

b. Both of the counter and random operations can be run on two different speeds based on the value of SW6.

1. If SW[6] is ON, the speed is *300ms*.
2. If SW[6] is OFF, the speed is *125ms*.

Project Report (70%)

The project report will be graded out of 100, and the points will be distributed as following:

1.0 (*20 points total, each value is 5 points*) After you compiled and synthesized your system, read the summary report from Quartus, and fill out the below table with the numbers from the report.

Logical Elements	Registers	Total Pins	Memory Bits

2.0 (*30 points*) Briefly, compare the hardware results between the table above and Table.1 of project 2.

3.0 (*50 points*) Answer the following questions:

1. (*10 points*) What is the maximum width that the PIO components can have and why?
2. (*5 points*) What is the hardware the function that is used to display the value 0x55 on LEDs?
3. (*5 points*) What is the total number of I/O pins that is used in a system which includes four seven-segment and four push button switches, in addition to clock and reset?
4. (10 points) You have an FPGA chip which consists of 2000 LEs. How many LABs (Logical Array Block) are there?
5. (20 points) Briefly explain the difference between Bare-Metal software and General-Purpose software (has Windows and Linux OS).

Project Demo (30%)

- The main purpose of the demo is to test your project functionality and execution.
- Demos will be checked and graded by the TA.
- Demos will be graded out of 100, but worth 30% of total project grade.
- Both partners must show up in that day. If a member didn't show up, he/she receives 0 unless an excused absence was provided.
- Demos will be conducted during the lab time on the following dates:
  - **Section 001**: Wed. Feb 15th or Wed. Feb 22nd
  - **Section 002**: Fri Feb 17th or Fri. March 24th
  - Demo dates will be decided by the groups.
- Below are how the demo points will be distributed.

Tasks	Point
Mode 1 operation	/25
Mode 2 operation	/25
Mode 3 operation	/25
Questions	/25

Project Submission

1. Save the project report as **r3_username1_username2.pdf**, username of both students in the group.
2. For this project, you are required to submit only the project report (No project submission is required). Submission date is Sunday Feb 19th by midnight.
3. **Only one attempt** is allowed.
4. **Only one group member** can submit the report.
5. **Remember:** Any grade dispute must be raised within one week of the grade posting.