VIDEO SYSTEM-CONNECTIONS

REFERENCE FOR PROJECT 4

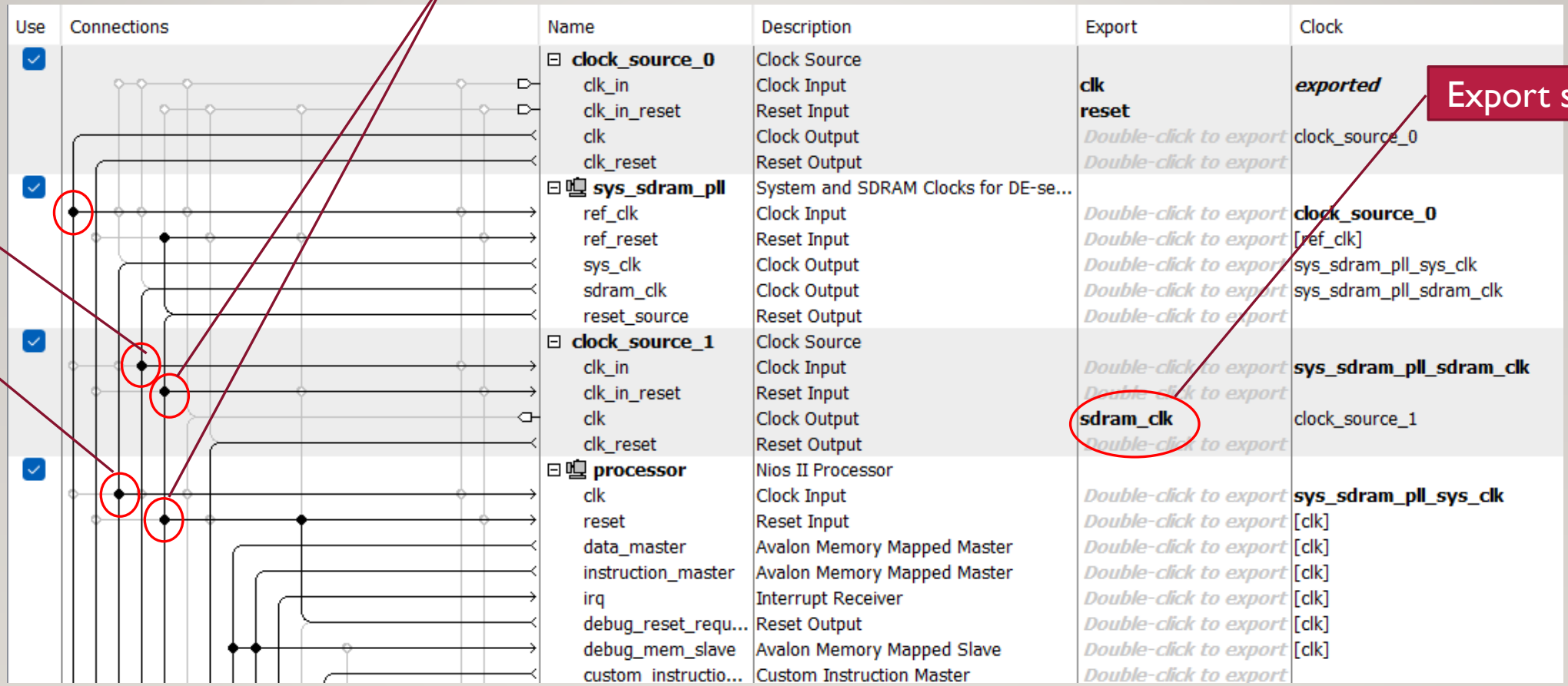
BY RASHA KARAKCHI

reset_source

sdram_clk

sys_clk

Export sdram_clk



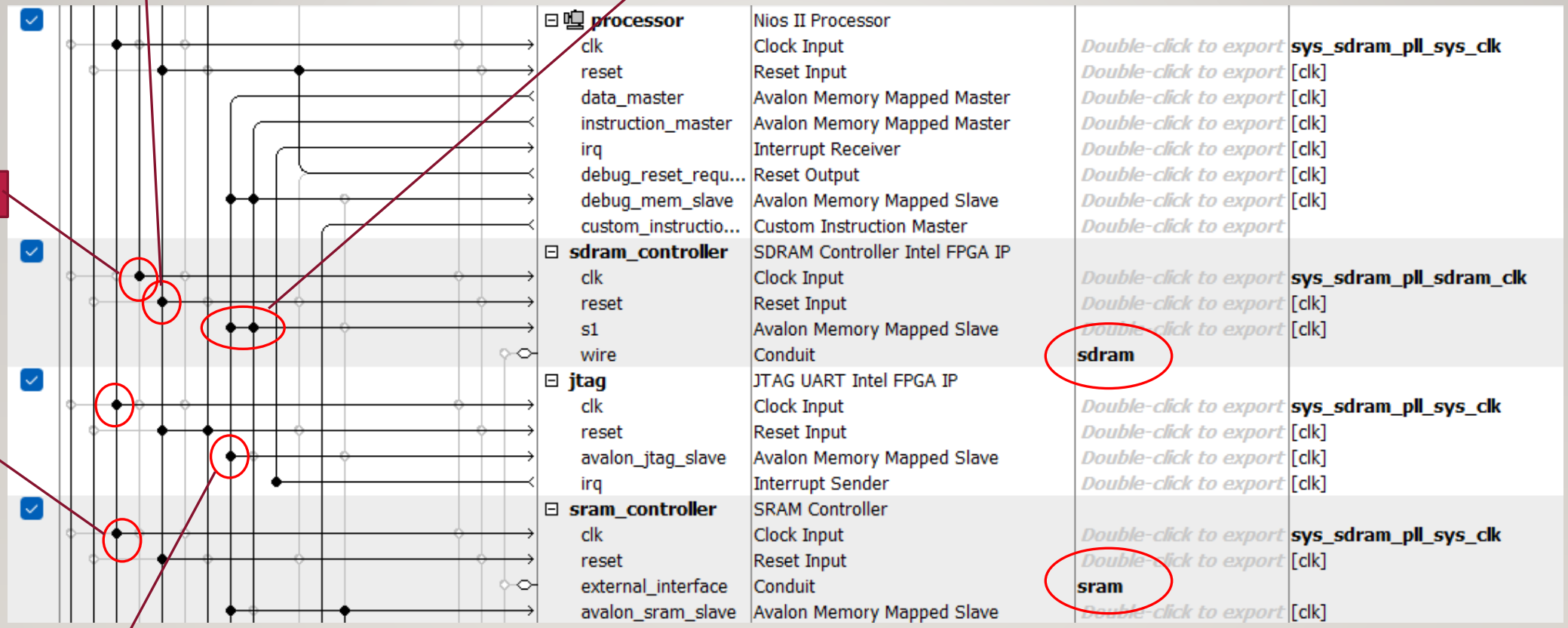
reset_source

Connect to processor data and instruction master

sdram_clk

sys_clk

Connect to processor data master



⊟ **processor**	Nios II Processor		
clk	Clock Input	*Double-click to export*	**sys_sdram_pll_sys_clk**
reset	Reset Input	*Double-click to export*	[clk]
data_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]
instruction_master	Avalon Memory Mapped Master	*Double-click to export*	[clk]
irq	Interrupt Receiver	*Double-click to export*	[clk]
debug_reset_requ...	Reset Output	*Double-click to export*	[clk]
debug_mem_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]
custom_instructio...	Custom Instruction Master	*Double-click to export*	
⊟ **sdram_controller**	SDRAM Controller Intel FPGA IP		
clk	Clock Input	*Double-click to export*	**sys_sdram_pll_sdram_clk**
reset	Reset Input	*Double-click to export*	[clk]
s1	Avalon Memory Mapped Slave	*Double-click to export*	[clk]
wire	Conduit	**sdram**	
⊟ **jtag**	JTAG UART Intel FPGA IP		
clk	Clock Input	*Double-click to export*	**sys_sdram_pll_sys_clk**
reset	Reset Input	*Double-click to export*	[clk]
avalon_jtag_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]
irq	Interrupt Sender	*Double-click to export*	[clk]
⊟ **sram_controller**	SRAM Controller		
clk	Clock Input	*Double-click to export*	**sys_sdram_pll_sys_clk**
reset	Reset Input	*Double-click to export*	[clk]
external_interface	Conduit	**sram**	
avalon_sram_slave	Avalon Memory Mapped Slave	*Double-click to export*	[clk]

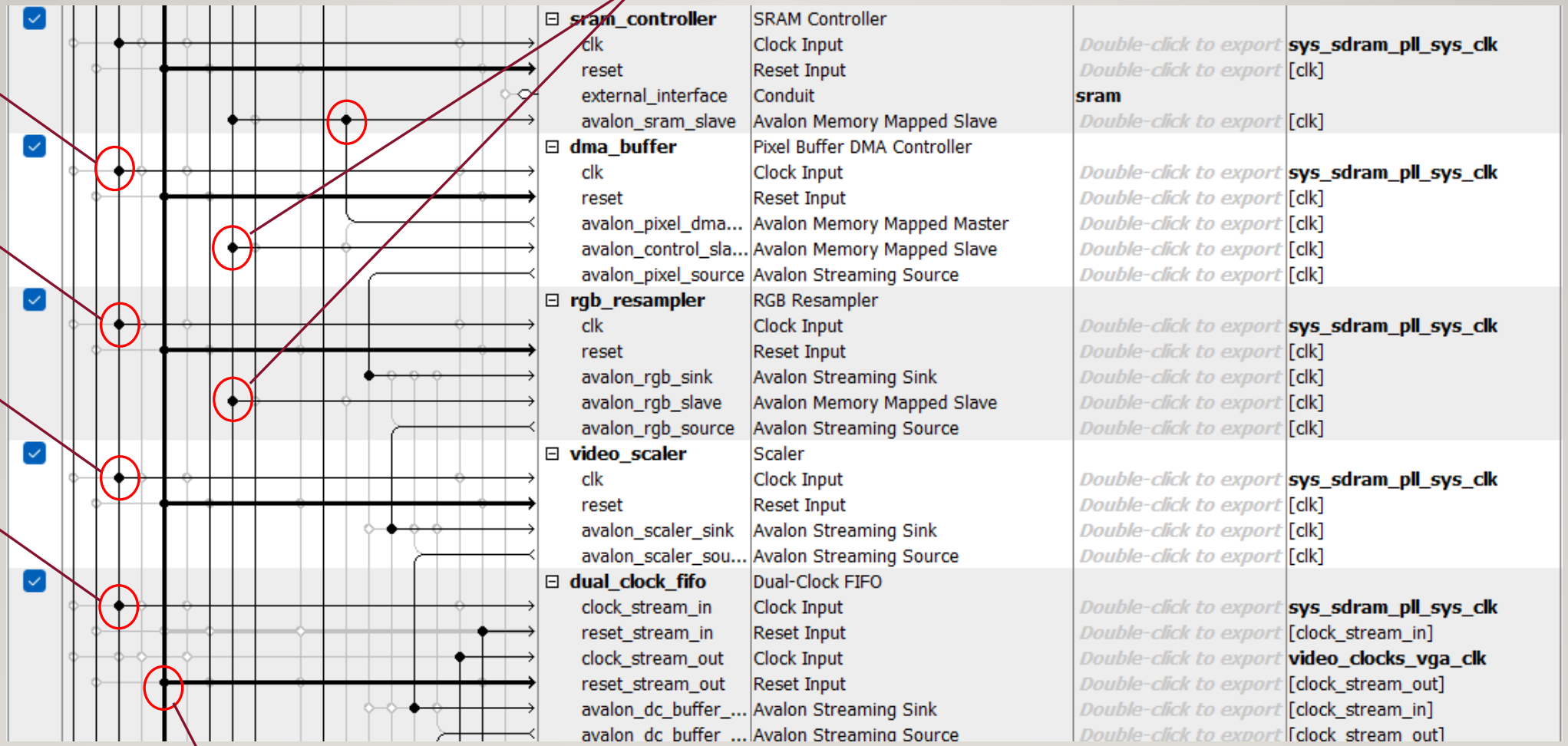
Connect to processor data master

sys_clk

sys_clk

sys_clk

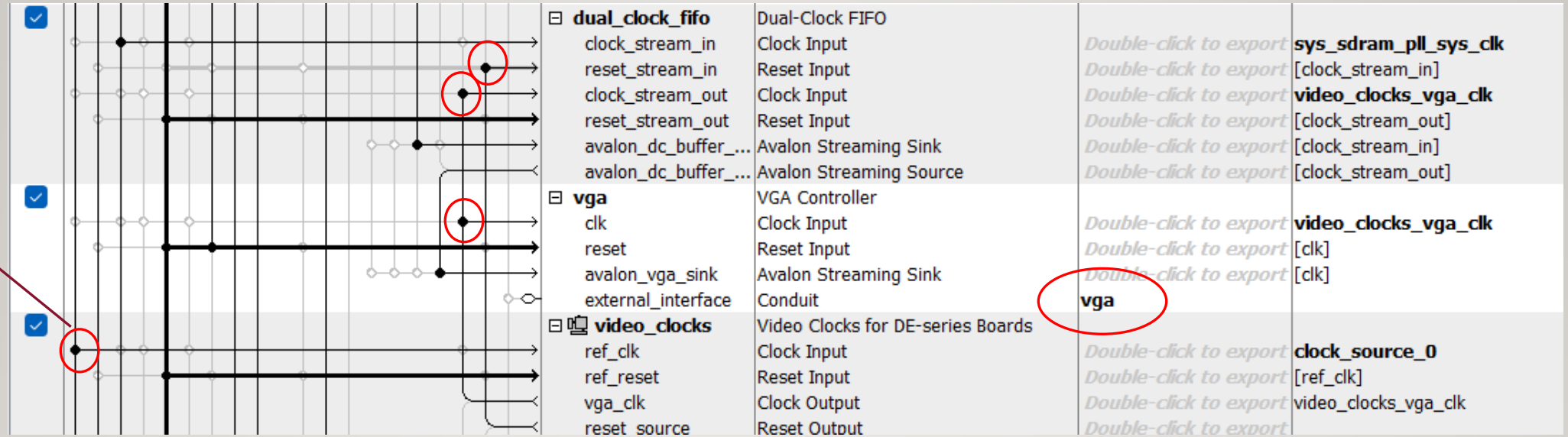
sys_clk



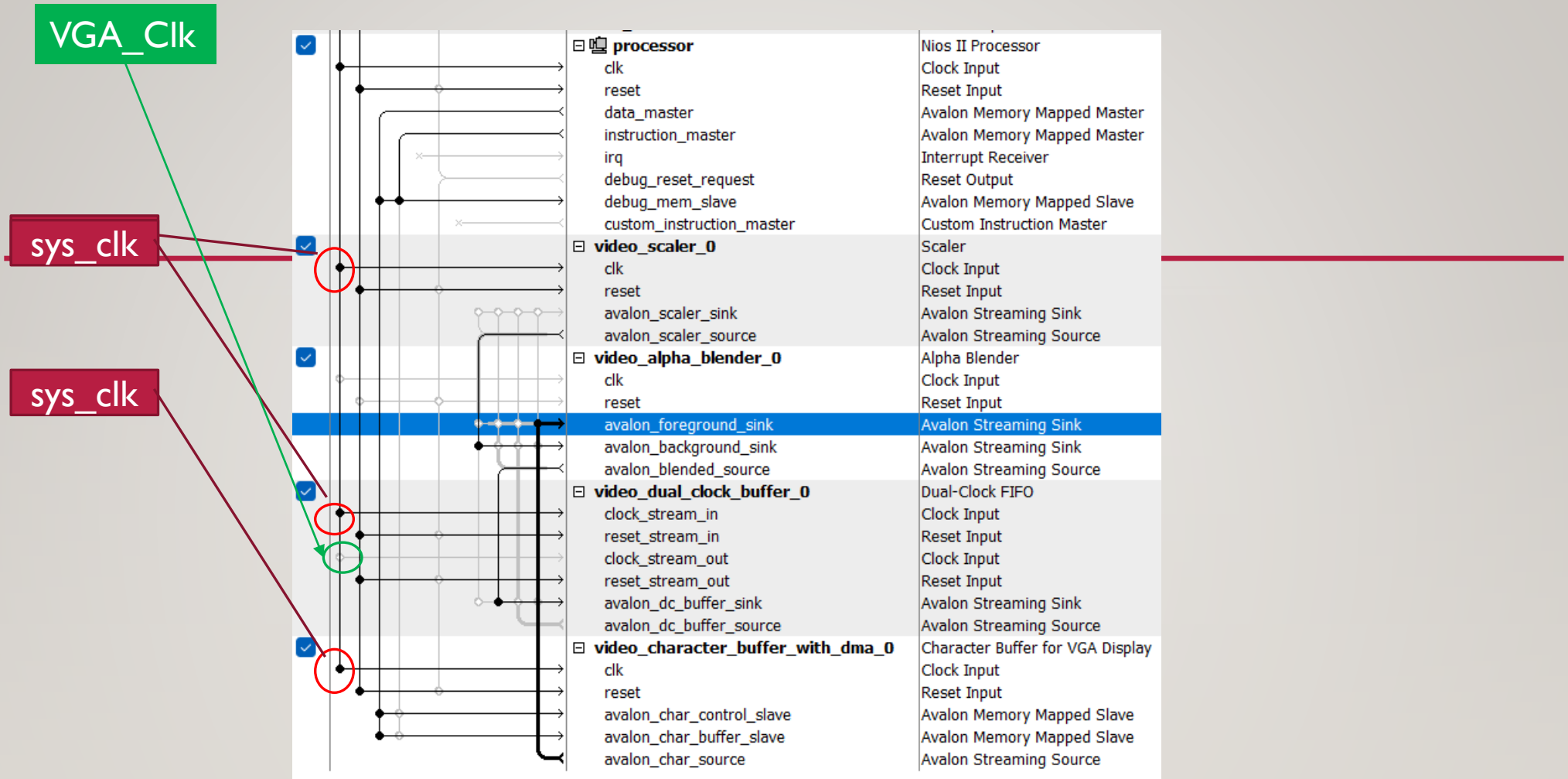
sram_controller	SRAM Controller		
clk	Clock Input	Double-click to export	**sys_sdram_pll_sys_clk**
reset	Reset Input	Double-click to export	[clk]
external_interface	Conduit	**sram**	
avalon_sram_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]
dma_buffer	Pixel Buffer DMA Controller		
clk	Clock Input	Double-click to export	**sys_sdram_pll_sys_clk**
reset	Reset Input	Double-click to export	[clk]
avalon_pixel_dma...	Avalon Memory Mapped Master	Double-click to export	[clk]
avalon_control_sla...	Avalon Memory Mapped Slave	Double-click to export	[clk]
avalon_pixel_source	Avalon Streaming Source	Double-click to export	[clk]
rgb_resampler	RGB Resampler		
clk	Clock Input	Double-click to export	**sys_sdram_pll_sys_clk**
reset	Reset Input	Double-click to export	[clk]
avalon_rgb_sink	Avalon Streaming Sink	Double-click to export	[clk]
avalon_rgb_slave	Avalon Memory Mapped Slave	Double-click to export	[clk]
avalon_rgb_source	Avalon Streaming Source	Double-click to export	[clk]
video_scaler	Scaler		
clk	Clock Input	Double-click to export	**sys_sdram_pll_sys_clk**
reset	Reset Input	Double-click to export	[clk]
avalon_scaler_sink	Avalon Streaming Sink	Double-click to export	[clk]
avalon_scaler_sou...	Avalon Streaming Source	Double-click to export	[clk]
dual_clock_fifo	Dual-Clock FIFO		
clock_stream_in	Clock Input	Double-click to export	**sys_sdram_pll_sys_clk**
reset_stream_in	Reset Input	Double-click to export	[clock_stream_in]
clock_stream_out	Clock Input	Double-click to export	**video_clocks_vga_clk**
reset_stream_out	Reset Input	Double-click to export	[clock_stream_out]
avalon_dc_buffer_...	Avalon Streaming Sink	Double-click to export	[clock_stream_in]
avalon_dc_buffer_...	Avalon Streaming Source	Double-click to export	[clock_stream_out]

sys_sdram_pll_reset_source

ref_clk



dual_clock_fifo	Dual-Clock FIFO		
clock_stream_in	Clock Input	Double-click to export	**sys_sdram_pll_sys_clk**
reset_stream_in	Reset Input	Double-click to export	[clock_stream_in]
clock_stream_out	Clock Input	Double-click to export	**video_clocks_vga_clk**
reset_stream_out	Reset Input	Double-click to export	[clock_stream_out]
avalon_dc_buffer_...	Avalon Streaming Sink	Double-click to export	[clock_stream_in]
avalon_dc_buffer_...	Avalon Streaming Source	Double-click to export	[clock_stream_out]
vga	VGA Controller		
clk	Clock Input	Double-click to export	**video_clocks_vga_clk**
reset	Reset Input	Double-click to export	[clk]
avalon_vga_sink	Avalon Streaming Sink	Double-click to export	[clk]
external_interface	Conduit	**vga**	
video_clocks	Video Clocks for DE-series Boards		
ref_clk	Clock Input	Double-click to export	**clock_source_0**
ref_reset	Reset Input	Double-click to export	[ref_clk]
vga_clk	Clock Output	Double-click to export	video_clocks_vga_clk
reset_source	Reset Output	Double-click to export	


VGA_Clk
sys_clk
sys_clk
processor
Nios II Processor
clk
Clock Input
reset
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
irq
Interrupt Receiver
debug_reset_request
Reset Output
debug_mem_slave
Avalon Memory Mapped Slave
custom_instruction_master
Custom Instruction Master
video_scaler_0
Scaler
clk
Clock Input
reset
Reset Input
avalon_scaler_sink
Avalon Streaming Sink
avalon_scaler_source
Avalon Streaming Source
video_alpha_blender_0
Alpha Blender
clk
Clock Input
reset
Reset Input
avalon_foreground_sink
Avalon Streaming Sink
avalon_background_sink
Avalon Streaming Sink
avalon_blended_source
Avalon Streaming Source
video_dual_clock_buffer_0
Dual-Clock FIFO
clock_stream_in
Clock Input
reset_stream_in
Reset Input
clock_stream_out
Clock Input
reset_stream_out
Reset Input
avalon_dc_buffer_sink
Avalon Streaming Sink
avalon_dc_buffer_source
Avalon Streaming Source
video_character_buffer_with_dma_0
Character Buffer for VGA Display
clk
Clock Input
reset
Reset Input
avalon_char_control_slave
Avalon Memory Mapped Slave
avalon_char_buffer_slave
Avalon Memory Mapped Slave
avalon_char_source
Avalon Streaming Source