**University of Nevada Las Vegas. Department of Electrical and Computer Engineering Laboratories.**

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| Class: | **CPE300L - Digital System Architecture and Design Lab** | | | Semester: | **Fall 2025** |
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|  | | | |
| Document topic: | **Postlab 3** | | |
| Instructor's comments: | | | | | |

1. **Hours spent on this lab**

About 10 hours (could not get the DE2 usb blaster to work)

1. **Reaction timer black box diagram**

**A diagram of a reaction

AI-generated content may be incorrect.**

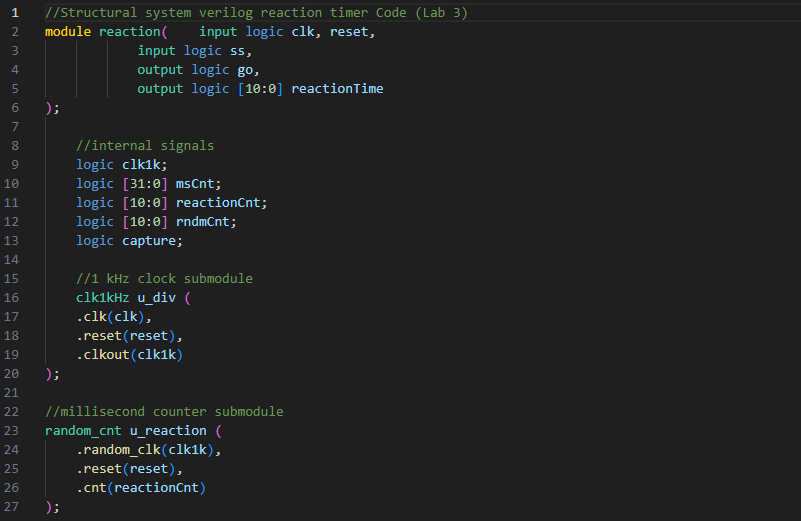
1. **Reaction timer block diagram**

**A diagram of a random counter

AI-generated content may be incorrect.**

1. **System Verilog code and submodules**

Reaction sv code (reaction.sv)

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**A screen shot of a computer program

AI-generated content may be incorrect.**

1kHz clock sv code (clk1kHz.sv)

A screen shot of a computer program

AI-generated content may be incorrect.

Random counter sv code (random\_cnt.sv)

**A computer screen shot of a program code

AI-generated content may be incorrect.**

Reaction FSM code (reaction\_FSM.sv)

**A screen shot of a computer program

AI-generated content may be incorrect.**

**A screenshot of a computer program

AI-generated content may be incorrect.**

**A computer screen shot of a black screen

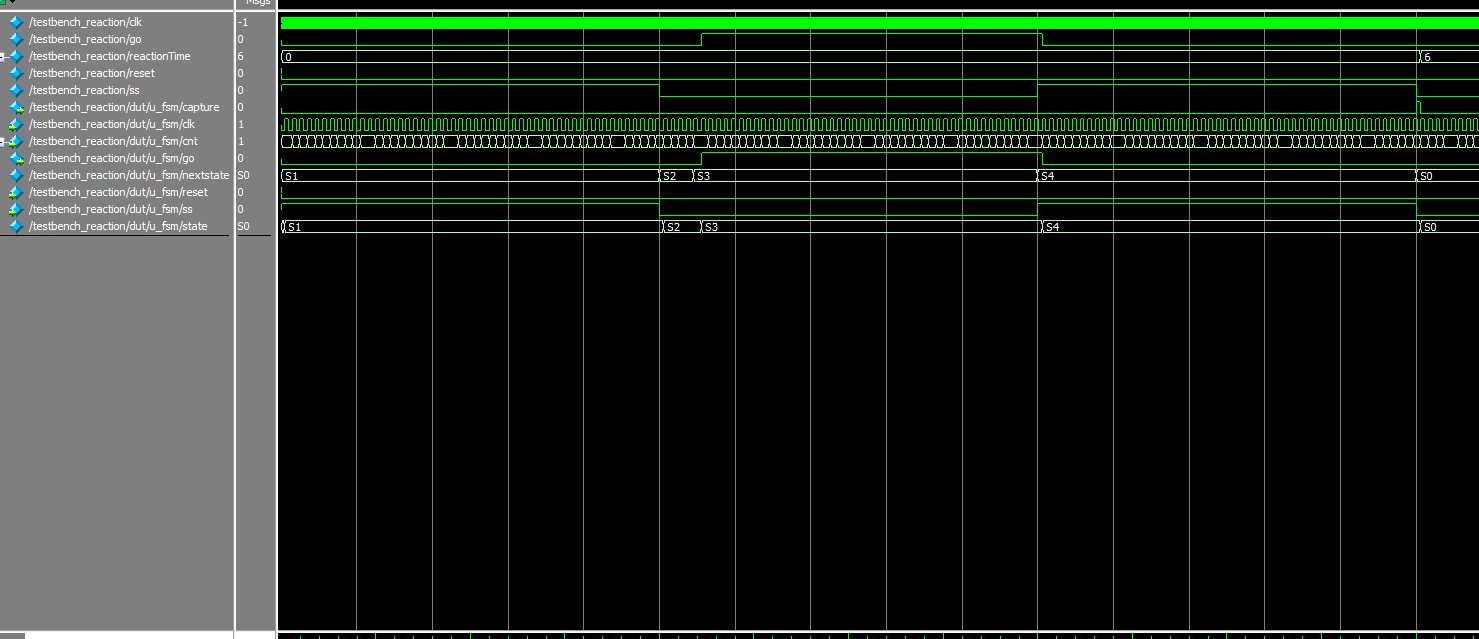
AI-generated content may be incorrect.**

Reaction timer testbench (testbench\_reaction.sv)

A screen shot of a computer program

AI-generated content may be incorrect.

1. **Reaction timer simulated waveform**

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1. **Screenshot of binary reaction time on DE2-115 board**

**A close up of a circuit board

AI-generated content may be incorrect.**

**Video demonstration:** [**https://youtu.be/7MMEMc39STY?si=XSUWIVGCfESqhqm5**](https://youtu.be/7MMEMc39STY?si=XSUWIVGCfESqhqm5)

1. **Feedback**

Would recommend a video demonstration or screenshots of expected outcomes on DE2 board within the assignment instruction PDF.