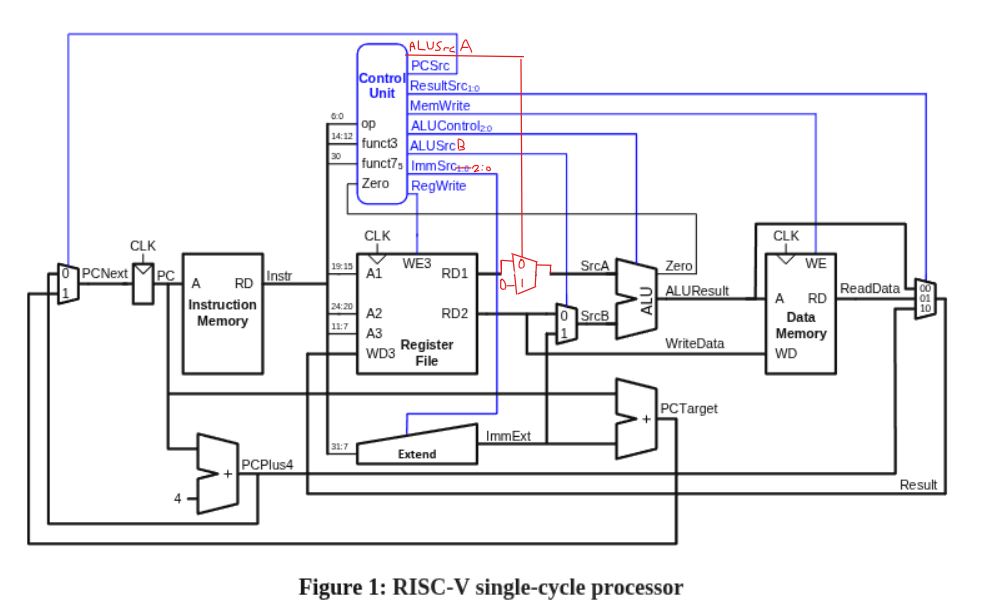
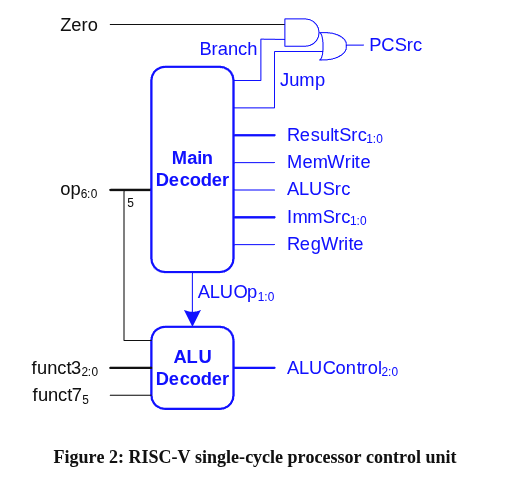
**University of Nevada Las Vegas. Department of Electrical and Computer Engineering Laboratories.**

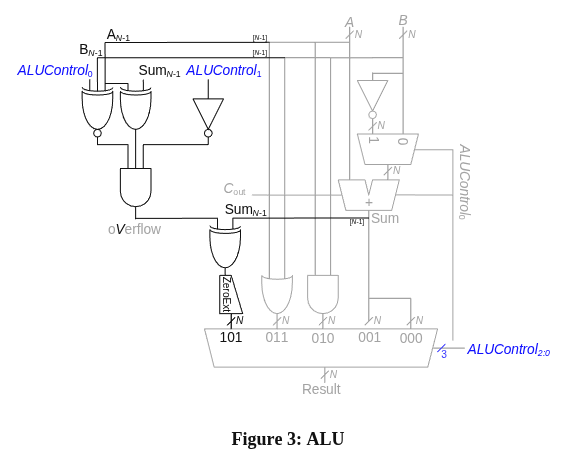
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| --- | --- | --- | --- | --- | --- |
| Class: | **CPE300L - Digital System Architecture and Design Lab** | | | Semester: | **Fall 2025** |
|  | | | | | |
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|  | | | |
| Document topic: | **Postlab 7** | | |
| Instructor's comments: | | | | | |

1. **Lab submissions**

This lab took around 7 hours

**2. Marked Figure 1:**

1. **Marked Figure 2:** 

**Marked Figure 3:** 

1. **Amended Tables**

**Main Decoder Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | Opcode | RegWrite | ImmSrc | ALUSrcA | ALUSrcB | MemWrite | ResultSrc | Branch | ALUOp | Jump |
| lw | 0000011 | 1 | 000 | 0 | 1 | 0 | 01 | 0 | 00 | 0 |
| sw | 0100011 | 0 | 001 | 0 | 1 | 1 | 00 | 0 | 00 | 0 |
| R-type | 0110011 | 1 | xxx | 0 | 0 | 0 | 00 | 0 | 10 | 0 |
| beq | 1100011 | 0 | 010 | 0 | 0 | 0 | 00 | 1 | 01 | 0 |
| I-type ALU | 0010011 | 1 | 000 | 0 | 1 | 0 | 00 | 0 | 10 | 0 |
| jal | 1101111 | 1 | 011 | 0 | 0 | 0 | 10 | 0 | 00 | 1 |
| lui | 0110111 | 1 | 100 | 1 | 1 | 0 | 00 | 0 | 00 | 0 |

**ALU Decoder Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| ALUOp1:0 | funct32:0 | {op5, funct75} | ALUControl2:0 | Operation |
| 00 | x | x | 000 | Add |
| 01 | x | x | 001 | Subtract |
| 10 | 000 | 00, 01, 10 | 000 | Add |
| 000 | 11 | 001 | Subtract |
| 010 | x | 101 | SLT |
| 110 | x | 011 | OR |
| 111 | x | 010 | AND |
|  | 100 | x | 100 | XOR |

**ImmSrc Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| ImmSrc | ImmExt | Type | Description |
| 000 | {{20{Instr[31]}}, Instr[31:20]} | I | 12-bit signed immediate |
| 001 | {{20{Instr[31]}}, Instr[31:25], Instr[11:7]} | S | 12-bit signed immediate |
| 010 | {{20{Instr[31]}}, Instr[7], Instr[30:25], Instr[11:8], 1’b0} | B | 12-bit signed immediate |
| 011 | {{12{Instr[31]}}, Instr[19:12], Instr[20], Instr[30:21], 1’b0} | J | 12-bit signed immediate |
| 100 | {Instr[31:12], 12’b0} | U | 20-bit signed immediate |

1. **Amended System Verilog Code For Lui:**

* Made 4 modifications to riscvsingle module, adding ALUsrcA/B, increased ImmSrc to 3 bits.

A screenshot of a computer program

AI-generated content may be incorrect.



* Increased ImmSrc to 3 bits and added ALUsrcA/B within controller module.

**A screenshot of a computer program

AI-generated content may be incorrect.**



* Increased ImmSrc to 3 bits, increased and updated controls to 13 bits, and updated all control values with addition of lui. Added ALUSrcA/B to maindec module.

**A screenshot of a computer program

AI-generated content may be incorrect.**



* Modified datapath to include ALUSrcA/B, increased ImmSrc to 3 bits, addeed rd1 logic, added mux for lui.

A screenshot of a computer program

AI-generated content may be incorrect.



* Added lui immext, increased immsrc to 3 bits.

A computer screen shot of a program

AI-generated content may be incorrect.



**Amended System Verilog Code For XOR:**

* Added XOR function to aludec module.

A screenshot of a computer program

AI-generated content may be incorrect.



**Ammended System Verilog Code for DE2 Board**

* Modified top module to include 7-seg decoder to display instruction, moved PC/Instr to output logic.

A screenshot of a computer program

AI-generated content may be incorrect.



A screenshot of a computer code

AI-generated content may be incorrect.

1. **Modified Assembly Instruction:**

A screenshot of a computer code

AI-generated content may be incorrect.



1. **Simulation Waveform:**

A screen shot of a computer

AI-generated content may be incorrect.



1. **DE2 Board Screenshot and Demo**

A close up of a circuit board

AI-generated content may be incorrect.

**Demo Link:** [**https://youtu.be/LvzOv1TrRXI?si=6XC6et\_URz\_6zXoA**](https://youtu.be/LvzOv1TrRXI?si=6XC6et_URz_6zXoA)