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RGB-to-DVI (Source) 1.4 IP Core User Guide

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1 Introduction

This user guide describes the Digilent RGB-to-DVI Video Encoder Intellectual Property. This IP interfaces directly to raw transition-minimized differential signaling (TMDS) clock and data channel outputs as defined in DVI 1.0 specs for Source devices. It encodes 24-bit RGB video data along with the pixel clock and synchronization signals.

IP quick facts	
Supported device families	Zynq®-7000, 7 series
Supported user interfaces	Xilinx: vid_io Digilent: TMDS
Provided with core	
Design files	VHDL
Simulation model	VHDL Behavioral
Constraints file	XDC
Software driver	N/A
Tested design flows	
Design entry	Vivado™ Design Suite 2016.4
Synthesis	Vivado Synthesis 2016.4

2 Features

- Connects directly to top-level digital visual interface (DVI) port
- 24-bit video (clocked parallel video data with synchronization signals) input
- Resolutions supported: 1920x1080/60Hz down to 800x600/60Hz (148.5 MHz – 40 MHz)
- Digilent interfaces used: TMDS

3 Performance

The IP does not constrain the clocks it requires as inputs. The exception is out-of-context synthesis, when the rgb2dvi_ooc.xdc contains the necessary constraints. However, this file is not used in top-level synthesis. Therefore, clocks need to be constrained in the top-level design either manually or by relying on the auto-derived constraints, if using clock modifying blocks. For more information see [7].

Although the IP itself supports the maximum frequency outlined in DVI 1.0 specifications (165 MHz) for pixel clock, the actual maximum frequency might be lower depending on the actual FPGA part or speed grade. Check the part datasheet for F_{MAX_BUFIO}, which is the most likely reason for failed timing. RGB_PixelClk should be constrained for $F_{MAX\_BUFIO}/5$. Consequently, this is the maximum pixel clock frequency supported on that FPGA family and speed grade.

4 Overview

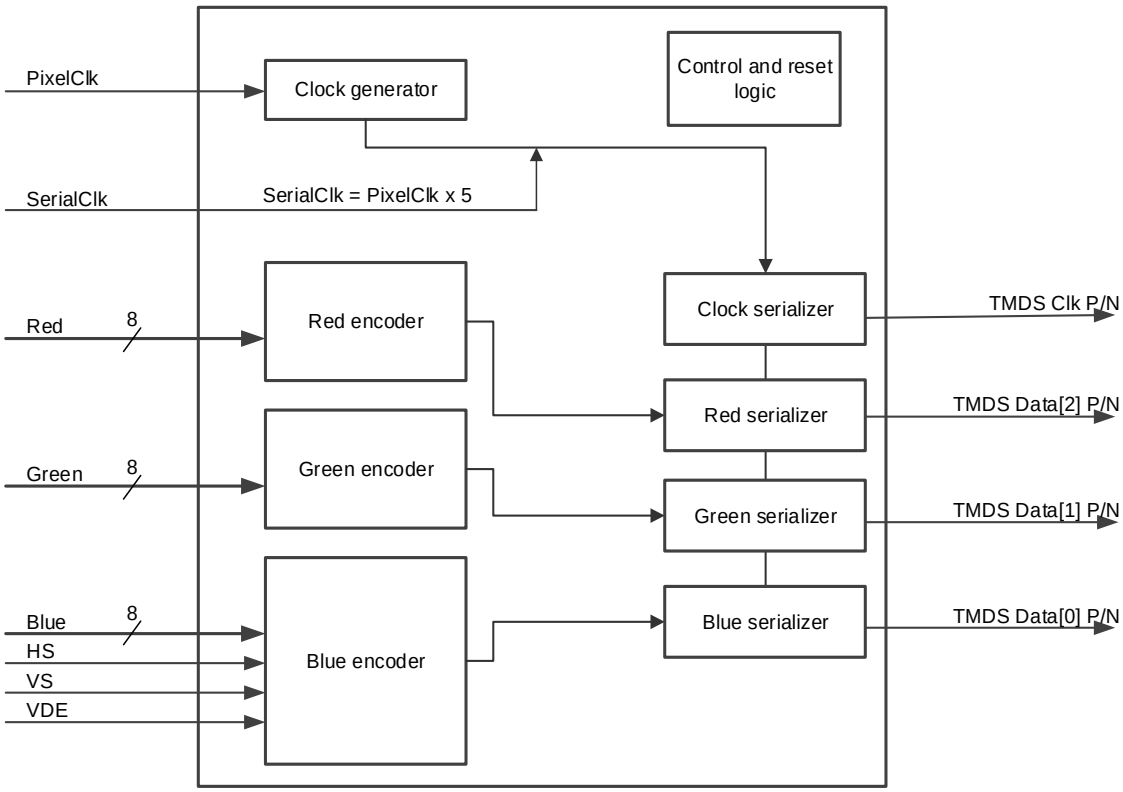

Figure 1. RGB to DVI converter block diagram.

The IP is built from multiple blocks: one encoder block for each data channel, one serializer block for each channel (clock and data), an optional clock generator and control/reset logic.

4.1 RGB input

The input to the core is a 24-bit RGB pixel bus. It has three 8-bit sub-pixel values for each color, a horizontal sync, a vertical sync, and a video data enable signal. All of them are synchronous to the pixel clock. Properly timing the synchronization signals for a specific display resolution according to industry standards is the responsibility of the user.

4.2 Clocking

In a DVI interface the clock channel carries a character-rate frequency reference. One character (or 10 bits) are transmitted every period on each data channel. Dedicated serializer primitives will be used to send data ten times faster than the pixel clock. These primitives require a fast serial clock five times the frequency of the pixel clock. If desired, the core can be configured to generate this clock internally. Furthermore, the user has the choice of PLL or MMCM as the primitive to be used. Since the clock must to be generated in the local clock region of the TMDS output pins and there is only one of each per region, this option helps to produce a valid placement.

The parameters of the MMCM/PLL must be chosen carefully so that frequency limits listed in the device datasheet are respected. These are input frequency-dependent and the whole range of common resolution cannot be covered with a single set of parameters. For this reason the IP needs to be customized for a high or low-range of pixel clock frequencies that will meet timing.

However, in most cases the pixel clock is already synthesized on the FPGA using dedicated clock primitives like MMCM or PLL. To avoid consuming an extra primitive, the existing one should be re-configured by the user to output not just the pixel clock, but a frequency five times higher too. This fast serial clock is then tied to the RGB-to-DVI core.

If generating the clocks outside the core, keep in mind that they have tight phase requirements and must use the same buffer type or a BUFIO/BUFR combination. The easiest approach is to use BUFGs for both clocks, but the clock frequencies will be limited by F_{MAX_BUFG}, specified in the part datasheet. The highest possible frequencies can be achieved by the BUFIO/BUFR combination. See the Digilent DVI-to-RGB core user guide and [1] section *OSERDESE2 Clocking Methods.*

4.3 Data encoding

The TMDS standard encodes data so that the serial data stream contains few transitions (0-to-1 or 1-to-0) and a DC balance (the same number of zeros and ones over a long time period). Every 8-bit pixel data is encapsulated in a 10-bit character. The control signals too are mapped to special 10-bit characters, called tokens. The encoder block applies the encoding algorithm as specified in the DVI 1.0 specifications.

4.4 Serialization

Clock and data are serialized 10:1 in the serializer blocks. Here, OSERDESE2 primitives are instantiated in a cascaded 10:1 DDR topology. Every pixel clock period an encoded 10-bit data arrives from the encoder and is output serially at rate ten times higher. The clock channel needs to be a character-wide pulse, which can be easily generated by serializing the 10-bit constant 1111100000.

5 Port descriptions

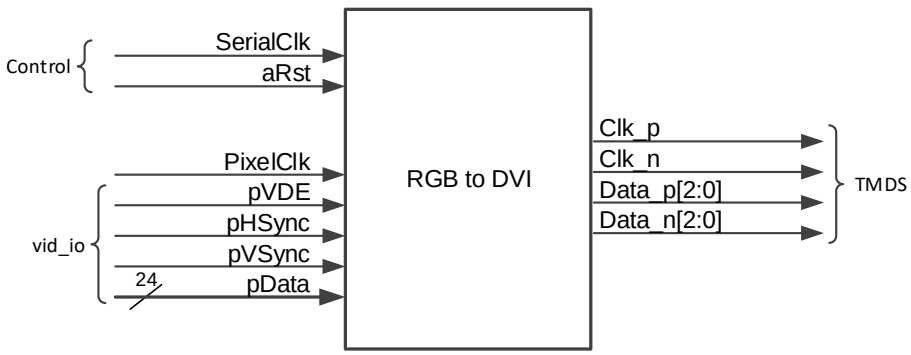

Figure 2. IP top-level diagram.

The signals of the RGB-to-DVI Core are listed and described in Table 1.

Signal Name	Interface	Signal Type	Init State	Description
SerialClk	-	I	N/A	Optional fast serial clock. Has five times the frequency of PixelClk and are phase-aligned. Can be generated internally.
aRst(_n)	-	I	N/A	Asynchronous reset of configurable polarity. Assert, if PixelClk and SerialClk are not within spec.
Clk_p/Clk_n	tmds	O	N/A	DVI Clock Channel.
Data_p[2:0]/Data_n[2:0]	tmds	O	N/A	DVI Data Channel 0.
PixelClk	-	I	N/A	Pixel clock.
pVDE	vid_io	I	N/A	Video data valid: • 1 = Active video. • 0 = Blanking period.
pHSync	vid_io	I	N/A	Horizontal synchronization video timing signal.
pVSync	vid_io	I	N/A	Vertical synchronization video timing signal.
pData (23:0)	vid_io	I	N/A	Video pixel data packed as RBG.

Table 1. Port descriptions.

6 Designing with the core

6.1 Customization

The IP provides some customizable parameters: the polarity of the reset signal and the option to generate SerialClk internally, among others. Upon enabling the latter, the user has the further option to choose the type of primitive (MMCM or PLL) to instantiate.

If the target board inverts one or more of the TMDS data or clock lanes by swapping the P and N sides, the lanes can be inverted back independently using the customization wizard.

7 References

The following documents provide additional information on the subjects discussed:

1. Xilinx Inc., *UG471: 7 Series FPGAs SelectIO Resources*, v1.4, May 13, 2014.
2. Xilinx Inc., *UG472: 7 Series FPGAs Clocking Resources*, v1.6, October 2, 2012.
3. Xilinx Inc., *XAPP460: Video Connectivity Using TMDS I/O in Spartan-3A FPGAs*, V1.1, June 24, 2011.
4. Xilinx Inc., *XAPP495: Implementing a TMDS Video Interface in the Spartan-6 FPGA*, v1.0, December 13, 2010.

5. Xilinx Inc., *WP249: SPI-4.2 Dynamic Phase Alignment*, v1.3, July 6, 2011.
6. DDWG: *Digital Visual Interface DVI*, Revision 1.0, April 2, 1999.
7. Xilinx Inc., UG903: Using Constraints, v2014.3, October 31, 2014