Fully FPGA-based Innovative Detection Setup for High-Resolution Time Resolved Experiments

F. Garzetti, N. Corna, N. Lusardi, A. Costa, E. Ronconi, S. Salgaro, A. Geraci, G. Brajnik, S. Carrato, G. Cautero, M. Cautero, R. Sergo, L. Stebel

***Abstract*—The usage of time-based approaches in modern physics experiments, have seen continuous growth thanks to the increasing performance of modern time–interval–meters (TIMs). In this context, Time–to–Digital Converters (TDCs), that are fully–digital TIMs, play a fundamental role. The digital approach makes the integration into measurement setups easier, while giving the possibility to investigate time–events with picosecond resolution over extended dynamic–ranges. Cross Delay-Lines (CDL) detectors are remarkably valuable, due to the fact that the position can be detected by measuring the time of arrival, obtaining both information at once. With the purpose of achieving both fast parallel computing and time precision, the conventional acquisition systems usually count on 4-channel Application Specific Integrated Circuit (ASIC) Time-to-Digital Converters (TDCs) preceding a Field Programmable Logic Array (FPGA), reaching state-of-the-art performance in time resolved experiments. In this kind of architecture, the lack of reconfigurability, given by the ASIC, is a tightly limiting factor when customization of the setup is demanded, even more so at present day, where state-of-the-art TDCs with similar performance to ASICs can be fully implemented in FPGAs; for this reason, we propose a fully-FPGA based approach in order to obtain a complete real-time system that can be completely reconfigured in function of the experimental setup. With the aim of improving the accuracy of the experiments, the time correlation between the CDL and the arrival time of other events occurring in conjunction is essential. For this reason, auxiliary TDC channels are needed. In this contribution, we present a compact, powerful and fully–configurable FPGA-based solution, where an 8–channel TDC with a precision of 12 ps r.m.s. and the related real–time image reconstruction algorithm take place on two different FPGA devices. In this sense, a spatial resolution on the CDL of 50/60 μm FWHM is achieved.**

***Index Terms*—Time-to-Digital Converter (TDC), Time-of-Fight (TOF), Cross Delay-Lines (CDL) Detector, Field Programmable Gate Array (FPGA), Free-Electron Laser (FEL), Synchrotron, 3D Imaging.**

I. Summary

In recent years, one of the sectors in which scientific research has been focusing is the study of the temporal evolution of chemical-physical phenomena. The strong interest in the so-called "time-resolved measurements" has led to the creation of light sources such as free electron lasers, third generation synchrotrons and lasers based on high harmonic generation: these machines are characterized by the generation of electromagnetic pulses with a duration well below picosecond, feature which scientists exploit to investigate the dynamics of the phenomena that occur on these time scales. In this field of research, "correlated measurements" find an important space: in these experiments the researchers not only want to know the time in which a certain phenomenon occurs, or its duration, but they also want to correlate a main event, sometimes even down into the picosecond or femtosecond scale, with other events that are somehow related, according to the physics of the experiment. In this context, an acquisition system can no longer be based on detectors seen just as "imagers": what is needed is an instrument with the ability to manage multiple analogue and digital inputs and that, at the same time, would control a detector used to measure the arrival time of each event and to correlate it with what was detected on the other inputs. The main features demanded to these detectors are, thus, high spatial and time resolution, high count rate capability and single particle sensitivity, which can all be delivered by Cross Delay-Lines (CDL) detectors [1], [2]. These detectors, as a matter of fact, are becoming more and more targeted as an alternative solution to pixel detectors, thanks to their proficiency in reconstructing bi-dimensional spatial information through the exploitation of the time difference between electromagnetic pulses emerging at the delay-line extremities. By accurately estimating these arrival times, the attainable target is a 3D time-resolved information (X, Y, t), where the time of arrival of the incoming particles corresponds to "t" and the space position on the detector is, instead, represented by "X, Y". A typical architecture for reading out the CDLs consists of a TAC (Time to Analog Converter) or, more recently, of an Application Specific Integrated Circuit (ASIC) based TDC, devoted to the timestamp generation, in conjunction with a Field Programmable Gate Array (FPGA) performing the image reconstruction. If on one side the high-performance time measurements and the reconfigurability offered, respectively, by the ASIC TDC and by the FPGA-based image-reconstruction algorithm are always satisfying, on the contrary many limiting factors emerge together with the need of adapting the ASIC to different experiments, most notably when considering that modern FPGA-based TDCs are able to produce results that are largely comparable with the ones offered by ASIC TDCs. What we did was, essentially, moving the TDC into the FPGA device, with a huge improvement in terms of both overall performance and versatility of CDL detector systems [3], [4]. The most interesting benefits that the complete system gained from the migration to an innovative, fully-FPGA based, architecture is the opportunity to keep improving, progressively, the overall

Manuscript received May 5, 2021. Authors are with the Politecnico di Milano, Department of Electronics, Information and Bioengineering – DEIB, via Golgi 40, 20133 Milano MI, Italy, and Elettra Sincrotrone Trieste, S.S. 14 - km 163,5 in AREA Science Park, Basovizza, Trieste, 34149, Italy, and DIA, University of Trieste, Via A. Valerio 6/1, 34127 Trieste, Italy (fabio.garzetti@polimi.it).

TABLE I
COMPARISON BETWEEN FPGA-BASED TDC PERFORMANCES FROM 2017 TO 2021.

Feature	2021	2020	[5]	[4]	[3]
Num. of Chs (no SYNC)	8	8	4	4	4
Dead-Time ns	5	7	20	50	70
FSR μs	days	200	200	10	10
LSB ps	0.036	1	1	5	10
Precision ps $r.m.s.$	< 12	< 12	< 12	< 12	< 15
INL over $500ns$	4	4	4	40	80
Connection link $Msps$	200	100	10	10	10

architecture of both the algorithm that takes care of the 3D image reconstruction, but also the actual TDC. Indeed, the latter is the one who received, in the last few years, the greatest enhancements, surpassing in performance, expressed in terms of resolution, precision, full scale range and dead-time, the TACs or TDCs based on the classical ASIC approach [2], and becoming suitable for use in those applications that take advantage of the aforementioned new generation of photon sources [5]. We first presented an FPGA implementation of the CDL detection system in 2017 Nuclear Science Symposium (NSS) [3], with a 4-channel Tapped Delay-Line (TDL) TDC featuring a resolution (LSB) of 10 ps over a Full Scale-Range (FSR) of 10 μs, that already granted images on the level of the more classical solutions [2]. In the following releases we confirmed the quality of our approach: from 2018 edition [4] on we continued improving the TDC architecture, first lowering the resolution to 5 ps and the single-shot channel precision from 15 to 12 ps r.m.s.; then, in 2019 [5], Integral Non-Linearity took a step forward, going from 50 ps over a 50 ns of dynamic-range [4] down to 4 ps over 500 ns. It has to be noted that every resolution, precision, INL, and FSR improvement translates directly to a better image quality, that actually reached 80/110 μm FWHM (35/50 μm r.m.s.) with no local aberrations. In the following release, "Fully FPGA-based 3D (X,Y,t) imaging system with Cross Delay-Lines detectors and Eight-Channels High-Performance Time-to-Digital Converter", presented in 2020 NSS, we targeted the speed of the TDC acquisition chain, the number of channels (going from 4 to 8), and we gave the possibility to measure multi-hit events, granting a minimum dead-time improved up to 7 ns compared to the 100 ns available with the latest TDC ASIC working at maximum precision [6]. With these renewed characteristics we could afford to collect all the pulses coming from the CDL with no losses on 4 of the channels, taking advantage of the 4 extra channels for making time correlation. Additionally, we improved by a factor 10 the data transfer from the Xilinx 28–nm 7–Series Artix–7 (hosting the TDC) to the Intel 28–nm Cyc lone V (which accomodates the image reconstruction algorithm), moving from 10 Mmeasure/s to 100 Mmeasure/s by means of a Gigabit Transceiver between the two devices, which replaced the former 32-bit parallel approach.

In this latest work we have continued to speed up the system, reducing the dead–time of the TDC down to 5 ns and increasing throughput up to 200 Msps. This has been possible thanks to a complete hardware redesign. In fact, we replaced the Intel Cyclone-V FPGA with a modern Intel 20–nm Cyclone-X; moreover, the TDC–board was redesigned and made more compact. Furthermore, improvements on the TDC firmware have been achieved: the LSB is now reduced to 36.6 fs and a proper management of the timestamps makes it possible to extend indefinitely the full–scale range by counting the events of overflow. In Table I are summed up the system capabilities, highlighting the continuous improvements achieved year by year, which give us big optimism about future further enhancements. Fig.1 shows the complete readout system, consisting in 8 Radio Frequency (RF) preamplifiers that precede 8 optional Constant Fraction Discriminators (CFD), with the purpose of obtaining digital signals starting from analog pulses. The CFD output is then fed to the 8-channel, FPGA-based TDC, that performs the measurement of the arrival time of each one of the 8 CFD signals, with respect to a common START signal.

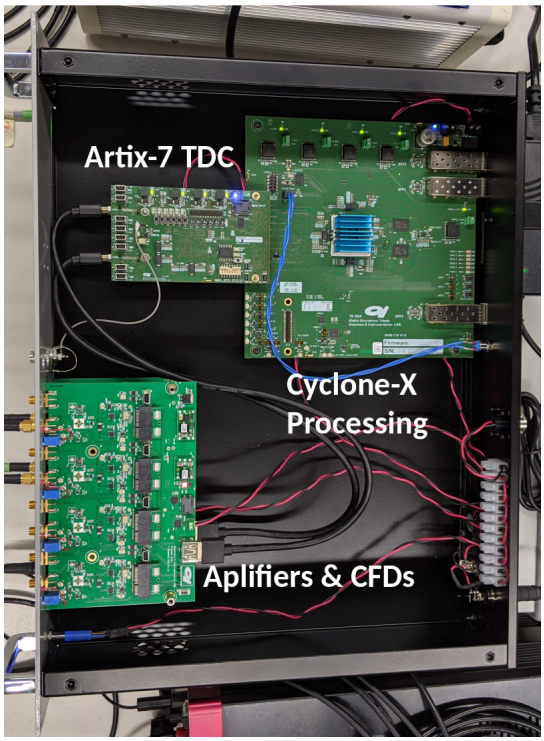

Fig. 1. Block diagram of the proposed experimental setup.

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