

# RF Circuit Design

Prof. Salvatore Levantino  
2020/21

# Course Outline

This course provides the fundamentals of radio-frequency (RF) front-ends for wireless systems, with particular emphasis to the integration in CMOS and BiCMOS processes. Topics covered include: review of architectures of RF receivers/transmitters and digital modulations, design of building blocks: low-noise amplifiers, mixers, oscillators, frequency synthesisers. The primary goal of the course is to provide students with the basic skills and knowledge required to analyse and design practical RF circuits.

## *a. Brief Review of Wireless System Fundamentals*

AM and PM modulations. Digital modulations and constellation plane. Coherent demodulation. Inter-symbol interference and pulse shaping. Error-vector magnitude and emission mask. Distortion and intercept points (IP2, IP3). Noise figure and sensitivity. Dynamic range. Heterodyne and direct-conversion receivers and transmitters.

## *b. Frequency Synthesiser Design*

Phase noise, reciprocal mixing and integrated phase noise. Phase-locked loop (PLL), lock range, continuous-time model. Charge-pump PLL. Integer-N frequency synthesisers. Phase noise in PLLs. Reference spur.

## *c. Design of RF Building Blocks*

Oscillator basics. Feedback and negative-resistance model. Startup and amplitude stabilisation. CMOS LC voltage-controlled oscillators (VCO). Phase noise and power trade-off. Power and noise matching. Lumped networks for impedance transformation. Low-noise amplifier (LNA) with inductive degeneration. Noise-cancelling LNAs. CMOS passive and active mixers, single- and double-balanced mixers.

# Learning Outcomes

By the end of this course, students will be able to:

- understand the issues of wireless systems in terms of system- and circuit-level specifications;
- design a frequency synthesiser to meet given specifications;
- design RF circuits such as low-noise amplifiers, mixers and oscillators to meet given specifications.

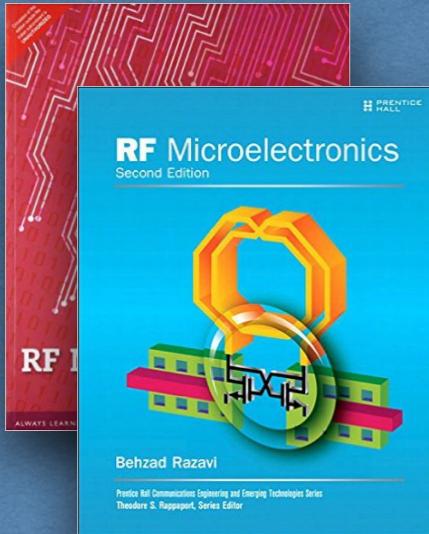
# Experimental Labs

- Radio transmitter design and simulation in **Matlab**
- System-level modeling, design and simulation of a simple PLL in **Simulink**.
- Design and simulation of charge-pump PLL in **Simulink**.
- Circuit-level design and simulation of a 1.5-GHz LNA in **Cadence Virtuoso**.
- Circuit-level design and simulation of a 1.5-GHz VCO in **Cadence Virtuoso**.
- Circuit-level design and simulation of a 1.5-GHz mixer in **Cadence Virtuoso**.

# Prerequisites

Communication Theory  
Control Theory  
Analog Circuit Design

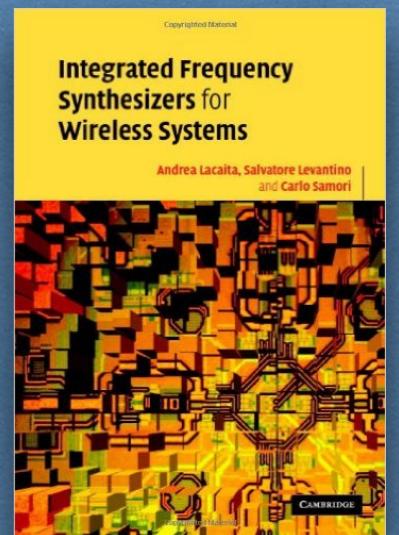
# Course Material



Razavi, *RF Microelectronics*,  
Pearson, II ed., 2011 or 2014

Lacaita/Levantino/Samori, *Integrated Frequency Synthesizers for Wireless Systems*, Cambridge Univ. Press, 2007

A screenshot of the BeeP platform interface. At the top, there are navigation links for "PRIVATE PERSONAL AREA", "PUBLIC PERSONAL AREA", and "MY COURSES". The main content area displays course information for "2016-17 - RF CIRCUIT DESIGN [ SALVATORE LEVANTINO ]". It includes a message from the professor: "IL TUO DOCENTE HA ATTIVATO IL CORSO IN BEEP MA NON LO TROVI TRA I TUOI CORSI? - non preoccuparti, da quando il docente attiva il corso, le operazioni di lettura dei piani di studi possono richiedere uno o due giorni.". Below this, there are tabs for "Home", "DOCUMENTS AND MEDIA", and "Homework". The "DOCUMENTS AND MEDIA" tab is selected, showing a list of files: "Excercises", "Labs", "Theory", "Information about the course of RF Circuit Design", "Summary of topics already covered", and "Tentative schedule of exercises and lab hours". Each item has details like size, user, last update, and download count.



Samples of last examination tests  
and other material available online:  
<http://beep.metid.polimi.it/>

# Timetable

# Class

Monday 14:30-16:00 (Webex)

Tuesday 14:30-17:00 (Webex)

Thursday 14:30-17:00 (26.02)

# Office Hours

Wednesday 10:00-11:00  
(Webex, *by appointment*)

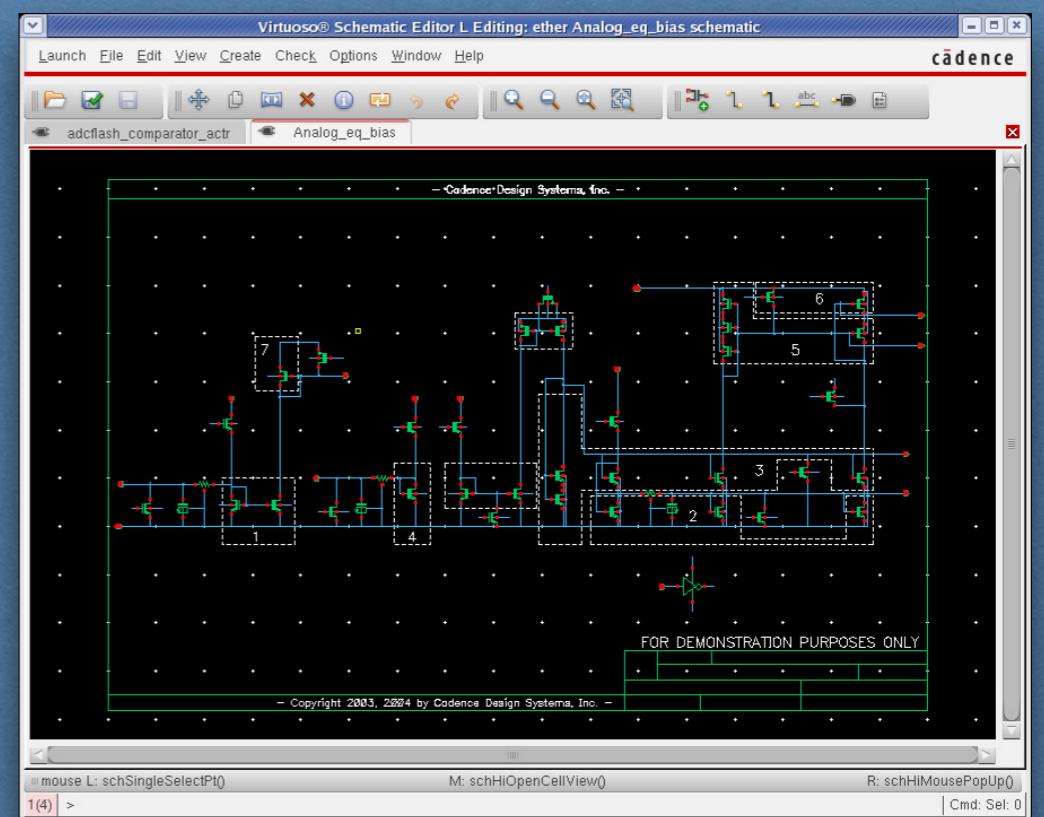
# Experimental Labs

On selected days

**You need a laptop!**

Notes of Lab available online  
<http://beep.metid.polimi.it/>

Cadence Lab  
will be in room **26.02**



# Calendar

Tentative schedule published on BeeP

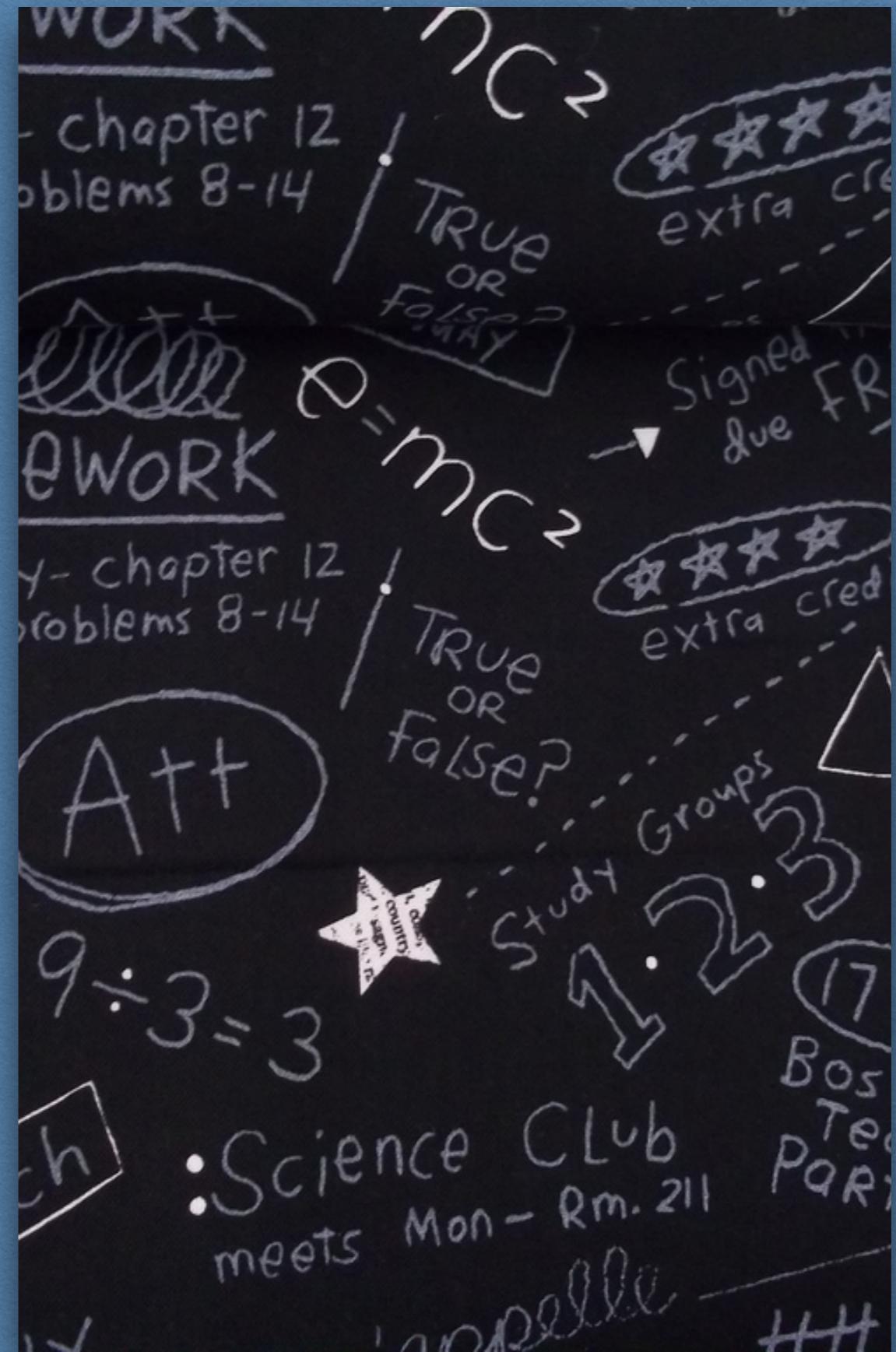
## **RF Circuit Design - Prof. Salvatore Levantino - 2020/21**

### **Syllabus (Lectures and Tutorials)**

- |    |       |   |  |
|----|-------|---|--|
| L1 | 22/02 | 2 | Course overview. Overview on wireless communications.  |
| L2 | 23/02 | 3 | Multiple access to channel (FDMA/TDMA). Example of early mobile phones. TX leakage. Diplexer and antenna switch. Example of modern smartphones. AM modulation: time domain, frequency domain, phasors.   |
| L3 | 25/02 | 3 | PM/FM modulations: time domain, frequency domain, phasors. Narrow-band FM approximation. Impairments of a Local Oscillator (LO): Spurious tones. Phase noise: white and random-walk. Link between oscillator power spectral density (PSD) and phase PSD. Definition of $L$ (script) or SSCR. |
| L4 | 01/03 | 2 | Digital communications: BPSK. Inter-symbol interference. Pulse shaping, Nyquist signalling, Raised cosine. Baseband equivalent, constellation plane. Quadrature modulations: QPSK.   |
| L5 | 02/03 | 3 | Modulator and demodulator architectures. Definition of EVM. Impact of LO phase noise on EVM. Impact of amplitude and phase error on EVM. Heterodyne receiver architecture.   |
| L6 | 04/03 | 3 | Reciprocal mixing: impact of phase noise on receiver   |

# Teaching Assistants

Mr. Francesco Tesolin  
[francesco.tesolin@polimi.it](mailto:francesco.tesolin@polimi.it)



# Final Examination



**Two-hour written examination**  
(containing 6 open-ended questions on  
2 or 3 numerical designs).

Max. Score 28+/30

**One-hour** written examination (containing  
3 open-ended questions on 1 or 2  
numerical designs) at mid-term

Max. Score 14+/30

+

**One-hour** written examination  
(containing 3 open-ended questions on 1  
or 2 numerical designs)

Max. Score 14+/30

Students who pass the written exam could  
take an **oral exam** (consisting of a single  
theoretical question).

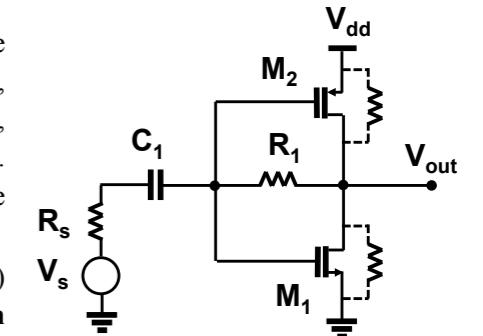
Max Score 2/30

# Written Examination

## Sample

**RF Circuit Design****Prof. Salvatore Levantino**Available time: 2 hoursMar. 1<sup>st</sup>, 2016**Problem #1**

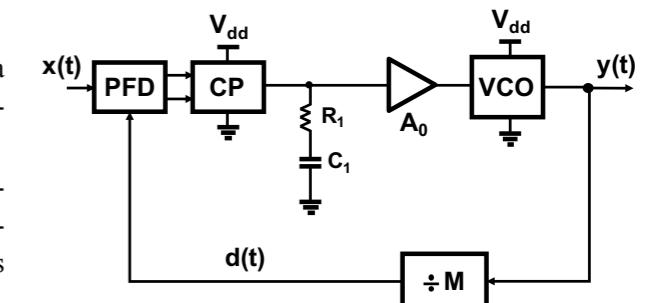
For the low-noise amplifier in figure, let assume  $V_{dd}=1.2V$ ,  $C_1=30pF$ ,  $R_s=50\Omega$ ,  $R_1=500\Omega$ ,  $(W/L)_{M1}=200$ ,  $(W/L)_{M2}=400$ . For the FETs: quadratic I-V characteristic, threshold  $|V_t|=0.35V$ , neglect body effect,  $\gamma=2/3$  and  $\alpha=1$ . For the nMOS device:  $1/2\mu_nC_{ox}=160\mu A/V^2$ , and for the pMOS device:  $1/2\mu_pC_{ox}=80\mu A/V^2$ .



- Neglecting the channel-length modulation effect ( $r_0$ ) and the parasitic capacitances, compute the **Return Loss**,  $S_{11}$ , (in dB) of the stage at 1GHz, the **Forward Gain**  $V_{out}/V_s$  (in dB) in the unloaded condition shown in the figure, and the **Noise Figure** at 1GHz.
- Taking into account the channel-length modulation of the MOSFETs and assuming  $\lambda=0.5V^{-1}$ , compute again **Return Loss**, **Forward Gain**, and **Noise Figure** at 1GHz.

**Problem #2**

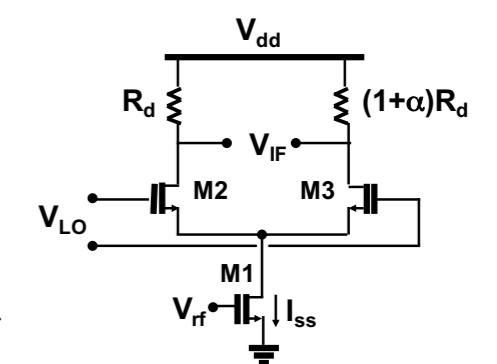
A student decides to precede a VCO in a PLL with an amplifier as shown below. Assume the amplifier has voltage gain  $A_0$ .



- Suppose the amplifier has an input-referred offset voltage equal to  $V_{os}$ . Calculate the **phase error** caused by this offset.
- Now suppose the amplifier is free from offset but has noise. Modelling the input-referred noise by a voltage  $V_n$ , find the **transfer function** from  $V_n$  to the output phase. Sketch the magnitude of this transfer function to show its general behaviour.

**Problem #3**

Consider the active mixer shown in figure, where the LO has abrupt edges and a 50% duty cycle, and no transistor enters the triode region. Also, channel-length modulation and body effect are negligible. The load resistors exhibit mismatch but the circuit is otherwise symmetric. Assume  $M_1$  carries a bias current of  $I_{ss}$ .



- Determine the **output offset voltage**.
- Determine the **input IP2 of the circuit** in terms of the overdrive and bias current of  $M_1$ .

# Oral Examination

## 1 out of 40 Questions

### 40 Questions for RF Circuit Design

Salvatore Levantino

Dipartimento di Elettronica e Informazione  
Politecnico di Milano

Year 2014/2015

#### **RF Front-end Architectures**

1. Effects of distortion. Two-tone test and IIP3.
2. Theorem of maximum power transfer and its application to the input impedance matching of amplifiers. Definition of power gains.
3. Matching networks: resonant networks and transformers.
4. Noise figure of lossy circuits and NF of cascaded systems. Noise matching.
5. Sensitivity and dynamic range calculation.
6. Basics in receivers and transceivers: Loss/filtering trade-off. Linearity/filtering trade-off. Duplexer filtering and leakage. Use of automatic gain control in receivers. Required number of bits in ADC.
7. Heterodyne receivers: advantages, image problem and filtering, choice of IF frequency. Selectivity/Sensitivity trade-off. Filtering/linearity trade-off. Block schematic from antenna to matched filter.
8. Problem of IF/2 and second-order nonlinearity. IIP2 and link with 2nd-order harmonic distortion.
9. Dual-IF receiver architecture and comparison with single-IF.
10. Zero-IF receiver architecture: filtering before/after amplification, DC offsets and cancellation techniques, I/Q mismatches and effect on SNR. Effect of even-order distortion. Flicker noise. LO leakage.
11. Image-reject receivers: Shift-by-90 operation. Hartley architecture and effect of mismatches and Image-Rejection Ratio (IRR).
12. Weaver architecture: advantages and drawbacks.
13. Transmitters: Digital I/Q transmitter, effect of mismatches on quadrature modulator. Direct-conversion and two-step transmitters. Use of Single-Sideband (SSB) mixer.