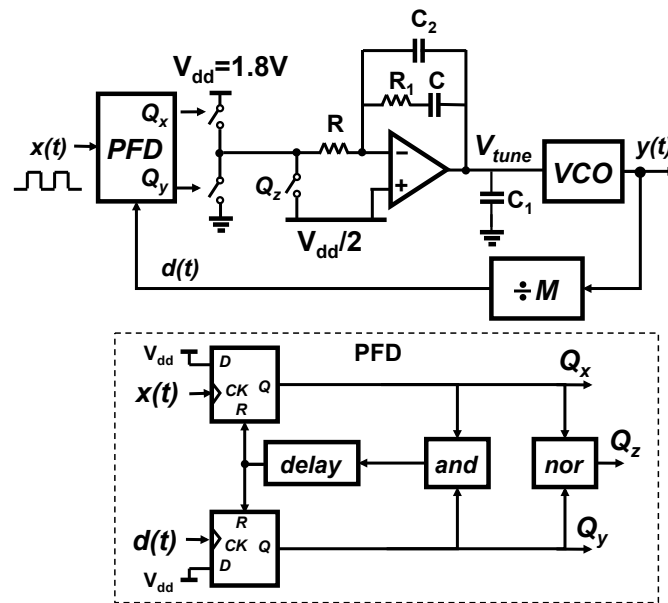


Tutorial T4

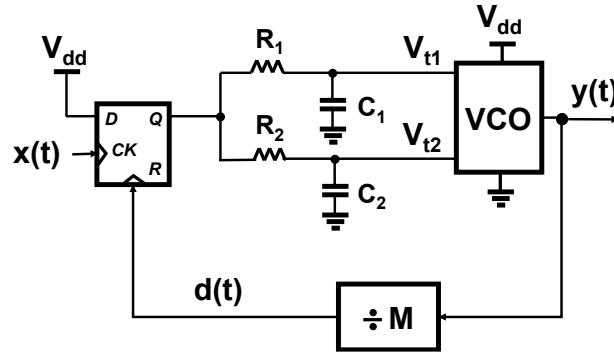
T4.1 The PLL in the figure embeds the PFD in the inset, where the block “delay” introduces a delay of 0.5 ns. The switches have infinite resistance (when off) and $10\ \Omega$ (when on). The reference clock $x(t)$ has 50 MHz frequency. The frequency-division factor is $M = 55$ and the VCO frequency varies in the range between 2650 and 2850 MHz, sweeping the V_{tune} from 0 to $V_{dd} = 1.8\text{ V}$. Let the capacitors be $C_1 = 100\text{ pF}$ and the resistor $R_1 = 100\ \Omega$.



- Assuming an ideal Op-Amp (with infinite gain and bandwidth), set the value of R and C to get two complex dominant (closed-loop) poles at 100 kHz located at 45 degree on the Gauss plane.
- If the resistance of the switch driven by Q_x is $15\ \Omega$ (when on), set the minimum value of C_2 , to get the level of the spur at 50 MHz in the spectrum of $y(t)$ lower than -80 dBc.
- Assuming all the switches with resistance $10\ \Omega$ (when on), but an offset voltage of 100 mV for the Op-Amp, can the loop lock? If yes, what is the value of the output frequency, the delay between $x(t)$ and $d(t)$ at steady state, the reference-spur level?

[Solution: a. $R = 195\ \Omega$, $C = 22.5\text{ nF}$; b. $I_{OS} = -0.92\text{ mA}$, $t_e = 105\text{ ps}$, $C_2 = 154\text{ pF}$; c. $I_L = 0.49\text{ mA}$, $t_e = 2.2\text{ ns}$, SFDR = -32.8 dBc]

T4.2. Let $V_{dd} = 1.8\text{V}$, $R_1 = 1\text{ k}\Omega$, $C_1 = 300\text{ pF}$, $R_2 = 10\text{ k}\Omega$, $C_2 = 120\text{ nF}$, $x(t)$ a 10-MHz periodic signal and $M = 135$. The D flip-flop has rails 0 and V_{dd} , and synchronous reset (clock samples data even when reset is “1”). The VCO has two tuning voltages V_{t1} and V_{t2} , which varies linearly VCO frequency, and a free-running frequency of $f_{fr} = 1200\text{ MHz}$ at $V_{t1} = V_{t2} = 0$.



- After deriving the continuous-time phase model of the system, compute the VCO tuning frequency ranges through control voltages V_{t1} and V_{t2} (when varied from 0 to V_{dd}) to set the unity-gain bandwidth of loop gain equal to 100 kHz and phase margin equal to 60 degrees.
- What is the value of V_{t1} and V_{t2} at steady state? Calculate the delay relationship between $x(t)$ and $d(t)$ in seconds at steady state.
- Do you expect any reference spur? If so, compute the level of the spurious tone in the spectrum of $y(t)$ in dBc.

[Solutions: a. $\tau = 4.65\text{ }\mu\text{s}$, $\Delta f_{VCO1} = 80\text{ MHz}$, $\Delta f_{VCO2} = 22.0\text{ GHz}$; b. $V_{t1} = V_{t2} = 12.2\text{ mV}$, $t_e = 0.68\text{ ns}$; c. SFDR = -50 dBc]