RF Circuit Design **Prof. Salvatore Levantino**

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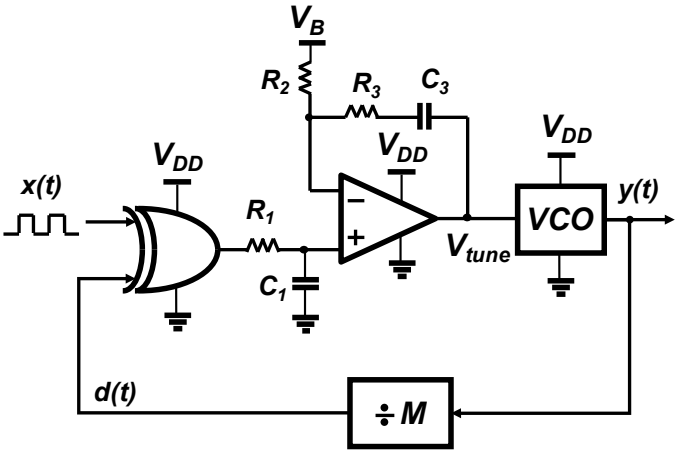
Mid-term Test

The XOR gate has CMOS levels 0 and V_{DD} = 1.8 V and zero output impedance. Let $x(t)$ be a squarewave with frequency f_x = 50 MHz, the frequency-division factor M = 45, and the VCO frequency linearly increase in the range between 2245 and 2265 MHz with V_{tune} between 0 to V_{DD}. Let C_1 = 150 pF, C_3 = 1 nF, and V_B = 0.45 V. Let the OpAmp be ideal with infinte gain.



a) Set the **value of R_1, R_2, and R_3** to get (i) crossover frequency of the loop gain at 200 kHz, (ii) phase margin of 60 degree, (iii) phase noise ($\mathcal{L}$) of $y(t)$ at 100 kHz equal to -131 dBc/Hz, considering for simplicity **only** the thermal noise of R_1.

b) Being V_B = 0.45 V, calculate the **time delay** between $x(t)$ and $d(t)$, the **average value of V_{tune},** and the **level (in dBc) and frequency of the dominant spur** in the spectrum of $y(t)$.

c) Let us assume that the PLL is used as the local oscillator of an RF receiver, whose input is given by a wanted signal at 1800 MHz with -100dBm power of over a bandwidth of 1 MHz and an interferer at 1825 MHz with -30dBm power. Calculate the **phase noise ($\mathcal{L}$)** required to the PLL to guarantee SNR = 20 dB at the receiver output. **Considering the thermal noise of R_1, R_2, and R_3, evaluate** whether the PLL designed in a) fulfills the phase noise specification.

[Sol. a) R_1 = 1.8kΩ, R_2 = 2.8kΩ, R_3 = 1.16kΩ; b) t_e = 2.5ns, V_{tune} = 0.45V, $\mathcal{L}$(100MHz) = -68.5dBc; c) $\mathcal{L}$(25MHz) = -150dBc/Hz (specification), -176dBc/Hz (PLL).]