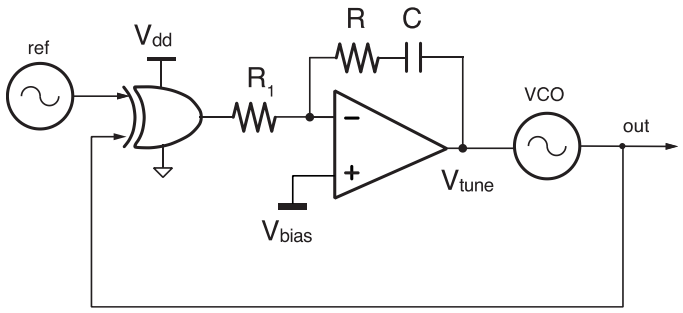
Tutorial T2

T2.1 Regarding the PLL in figure, assume that $V_{DD} = 3.3\ V$ and the frequency of the square-wave reference signal is 200 kHz, let the output impedance of the XOR gate be equal to zero, assume the operational amplifier to be an ideal one, and the VCO with linear tuning characteristic the 0-3.3 V tuning voltage range.



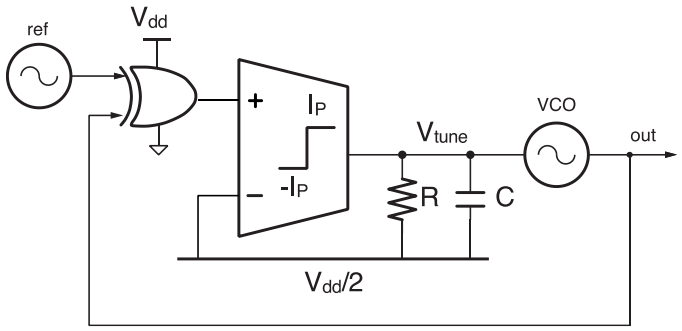
a. Setting $V_{bias} = 1.65\ V$, draw the equivalent phase model and set the parameter R_1, R, C, K_{VCO} for
   i. a maximum output current of the XOR gate equal to 1 mA,
   ii. a tuning range Δf_{VCO} = 50 kHz,
   iii. a phase margin of 60°,
   iv. a crossover frequency of the loop gain equal to 1 kHz.

b. Find the time shift at steady state (t_ϵ^∞) between reference and VCO signals as a function of V_{bias}.

c. Assuming $V_{bias} = 1.65\ V$ and considering a voltage offset (V_o) of 10 mV and a bias current (I_b) of 10μA for the operational amplifier, evaluate the effect on the loop. What is the time shift between reference and VCO?

[Solution: a. K_{VCO} = 95.15 krad/(Vs), R_1 = 1.65 kΩ, R = 104 Ω, C = 2.66 μF; b. t_ε has a linear dependence on V_{bias} and goes from 0 to -2.5 μs when V_{bias} is swept from 0 to V_{dd}; c. At V_{bias} = 1.65V, the time shift is t_ε = = -1.25 μs (with an ideal Op-Amp), and it increases by 20 ns (considering the voltage offset and the bias current of the Op-Amp).]

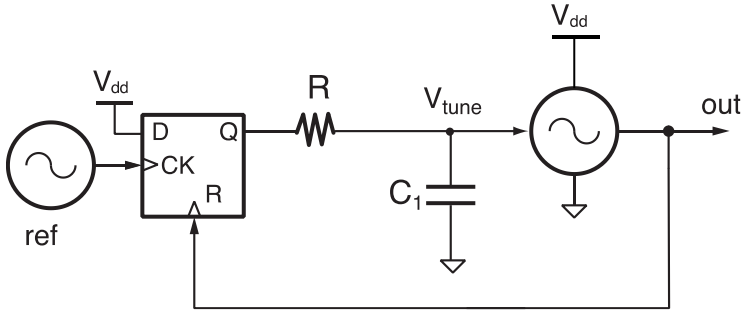
T2.2. Consider the PLL in the following figure, where $V_{DD} = 3\ V$ and the reference signal is a square-wave signal with a frequency of 200 MHz (f_{ref}). The XOR gate drives a transconductor behaving as a comparator. Its output is either I_P or $-I_P$, with I_P = 0.5 μA. Let the resistor R = 2 kΩ, and the capacitance C = 1.4 nF. The VCO has a linear tuning range from 155 to 245 MHz when the tuning voltage V_{tune} is swept from 0 to V_{dd}.



a. Draw the equivalent model of the PLL in the phase variables.
b. Draw the Bode diagram of the loop gain magnitude.
c. Evaluate the natural frequency (ω_p) and the damping factor ζ of the closed-loop poles.

[Solution: a. The equivalent phase model has $K_{pd} = 2I_p/\pi$ and $G(s) = R/(1+sRC)$; b. Loop gain is $LG(s) = K_{pd}K_{vco}G(s)/s$, that has one integrator and a pole at $1/RC$ = 357 krad/s, unity gain frequency is $\omega_u \approx K_{pd}K_{vco}R$ = 120 krad/s; c. The natural frequency of closed-loop poles is 207 krad/s and ζ is 0.862.]

T2.3. Considering the PLL in figure, assume a square-wave reference signal with a frequency of 100 MHz (f_{ref}). The circuit has a single power supply $V_{dd} = 3\ V$ and a VCO with a free-running frequency of 99.85 MHz (f_{fr}) and a tuning range of 450 kHz (Δf_{VCO}) between 0 and V_{dd}. The D-type flip-flop has 0 and V_{dd} voltage rails and a synchronous reset (clock samples data even when reset is "1").



a. Draw the phase-domain model and the phase characteristic of the phase detector (i.e. output average voltage versus input phase delay).
b. Find the time shift between reference and output signal at steady state.
c. Set the time constant $\tau = RC_1$ to get maximally-flat frequency response.

[Solution: a. The equivalent phase model is conventional with $K_{pd} = V_{dd}/(2\pi)$ and $G(s) = 1/(1+sRC_1)$, the characteristic of the phase detector is linear between 0 and 2π and goes from 0 to V_{dd}; b. the time shift at steady state is 3.33 ns; c. τ = 1.1 μs.]

T2.4. Consider a receiver chain where the RF signal has a power of $P_S^{dB} = -50$ dBm over a $B_{RF} = 200$ kHz, and the blocker has a power of $P_B^{dB} = -30$ dBm. Compute the $\mathcal{L}(f)$ of the local oscillator to guarantee $SNR_{\text{dB}} > 50$ dB due to reciprocal mixing effect in the following cases:

- **a.** Suppose $f_{LO} = 2$ GHz, $f_{RF} = 2.1$ GHz and $f_B = 2.7$ GHz.
- **b.** Suppose $f_{LO} = 2.5$ GHz, $f_{RF} = 2.1$ GHz and $f_B = 2.7$ GHz.

[Sol: a. $\mathcal{L}$ (600 MHz) = -123 dBc/Hz; b. $\mathcal{L}$ (200 MHz) = -123 dBc/Hz.]

T2.5. Let us consider a QPSK signal:

- **a.** Prove that the signal can be written as: $x(t) = A \cdot \cos\left[\omega_c t + (2k+1)\frac{\pi}{4}\right]$.
- **b.** Plot the constellation of a QPSK signal affected by phase noise.
- **c.** Calculate the EVM (in dB) of the modulation, assuming the carrier at 1 GHz with integrated jitter equal to 1 ps RMS.

[Sol: c. EVM = -44 dB.]