RF Circuit Design

Prof. Salvatore Levantino

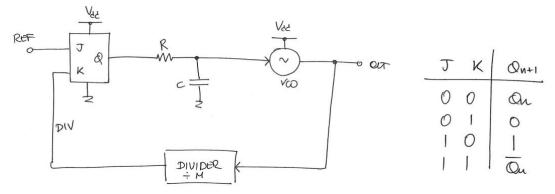
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Mid-term Test

Exercise 1

In the PLL in figure, the JK latch (a.k.a. "level-triggered" flip-flop) has CMOS levels 0V and V_{DD} = 1.2V, zero output impedance, and truth table shown below. Let the REF signal be a squarewave with frequency f_{ref} = 10 MHz, the frequency-division factor M = 100, and let the VCO have freerunning frequency 957MHz and linear tuning range over input voltage between 0V and V_{DD} .

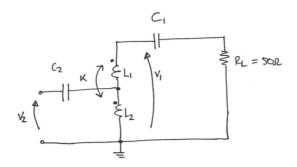


- a) Calculate and plot the voltage-vs-phase characteristic of the JK latch and calculate its gain.
- b) Set the value of R, C, and VCO tuning range to get (i) closed-loop poles at 100kHz, (ii) maximally flat PLL input-output frequency response, (iii) contribution of R thermal noise to the output phase noise \mathcal{L} equal to -146dBc/Hz at 1MHz offset.
- c) Calculate the **time delay (in seconds)** between two positive edges of REF and DIV signals at steady state, and the **level of the reference spur** in the output spectrum (in dBc).

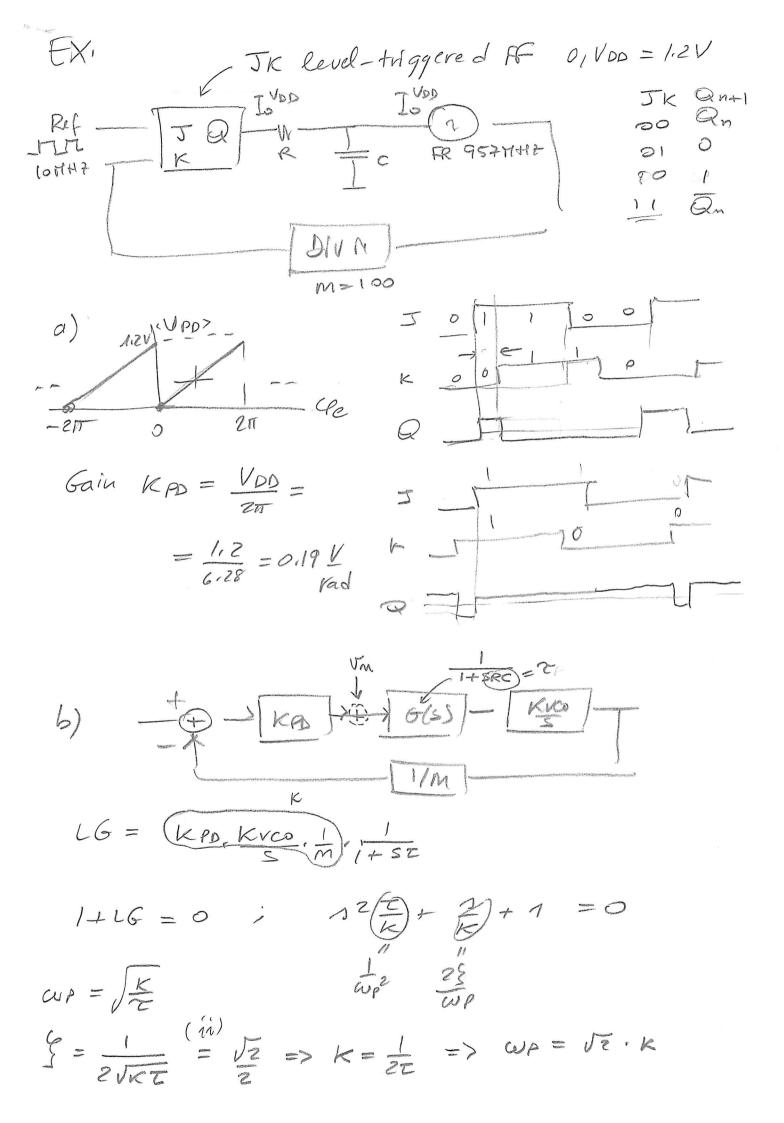
[Sol: a) PD gain = 0.19 V/rad; b) $R = 11 \text{ k}\Omega$, C = 100 pF, TR = 44.3 MHz; c) Delay = 96 ns; Spur at 10MHz offset = -54 dBc]

Exercise 2

The circuit in figure is used to transform the impedance $R_L = 50\Omega$. Given $C_1 = 1$ pF, $L_1 = 0.8$ nH, find **the values of** L_2 , k, C_2 to have an input impedance of $Z_{in} = 5\Omega + j0\Omega$ at 5GHz frequency.



[Sol: $L_2 = 317$ pH, k = 0.43, $C_2 = 3.78$ pF]



(2)
$$f = \frac{1}{22} \cdot \frac{K_B \ K_V co}{M} = 100 \ K$$

$$\Rightarrow K_V co = \frac{2\pi \cdot 100 \times 100}{0.19 \cdot 12} = 73.37 \cdot 10^2 \frac{1}{100} = 141.4 \times 147$$

$$\Rightarrow K_V co = \frac{2\pi \cdot TR}{V_{OD}} = 73.37 \cdot 10^2 \frac{1}{V_{CO}} = \frac{1}{200} \cdot \frac{1}$$

C) Delay $f_{ont} = M \cdot f_{exf} = 16H^2$ $\Delta f = f_{out} - f_{fn} = 1000 - 957 = 4311H^2$ $V_{tune} = \frac{2\pi \cdot \Delta f}{kveo} = 1,155V$

$$\begin{aligned}
\varphi_{\mathcal{E}} &= \frac{V + nne}{V \rho D} &= \frac{1.155}{0.19} = 6.079 \, rad \\
& + \varepsilon &= \frac{\varphi_{\mathcal{E}}}{2\pi} \cdot T_{\mathcal{R}} &= \frac{6.079}{6.079} \cdot 100 \, as &= \frac{96.2 \, ns}{6.28} \\
& + v_{DD} &= \frac{6.079}{6.28} = 96.87 \\
& + v_{DD} &= \frac$$