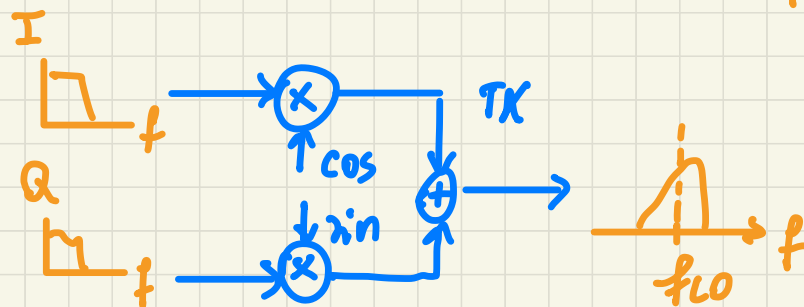
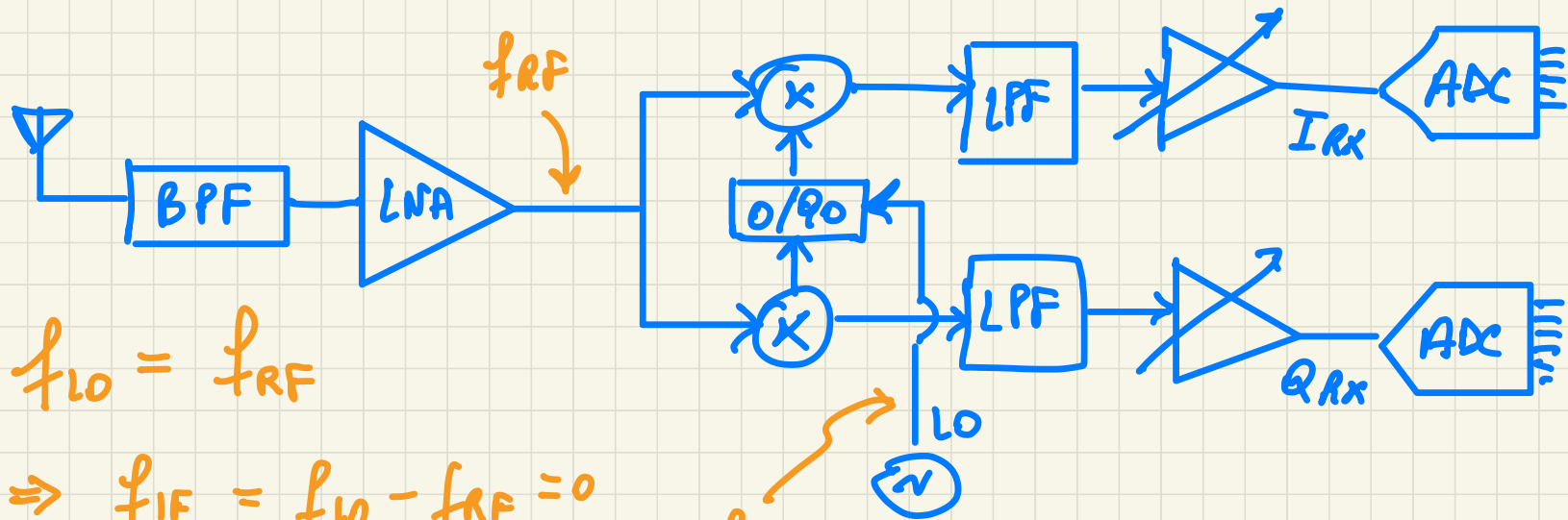


RF Circuit Design

L22



Direct - Conversion RX (or zero-IF RX)



2 mixers needed at RX
Otherwise:



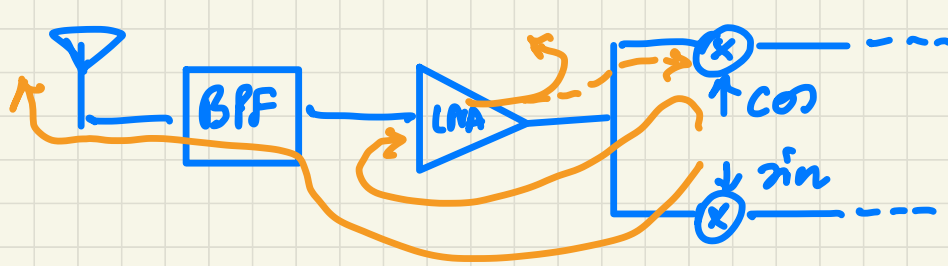
Advantages :

Direct - conv.
RK architect.
suitable for
fully integration
in silicon

- Image problem apparently solved
→ no need for an IR filter
- Channel selection is performed with LPF (rather than BPF)
→ no need for offchip SAW filters
LPF filters can be implemented in silicon (SC active filters)

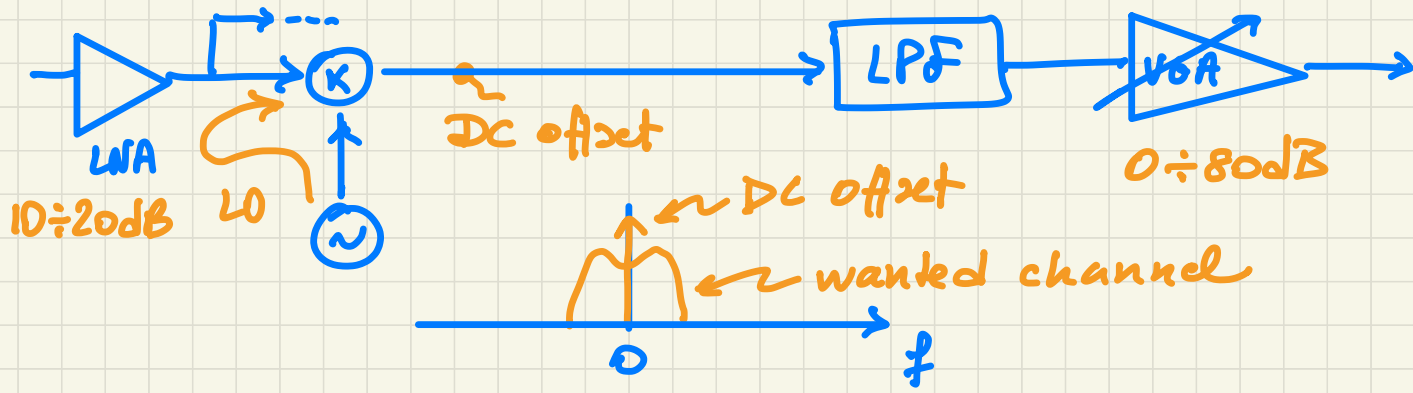
Critical issues :

- LO leakage :
 - $f_{LO} = f_{RF} \Rightarrow$ LO is in LNA BW
 - LO signal has large power



↓
LO signal can be emitted and Rx might violate radiation limits ($< -50 \div -80$ dBm)

- DC offsets :
 - * LO leakage \Rightarrow self mixing of LO
 - * Interfer leakage \Rightarrow self mixing of interferer

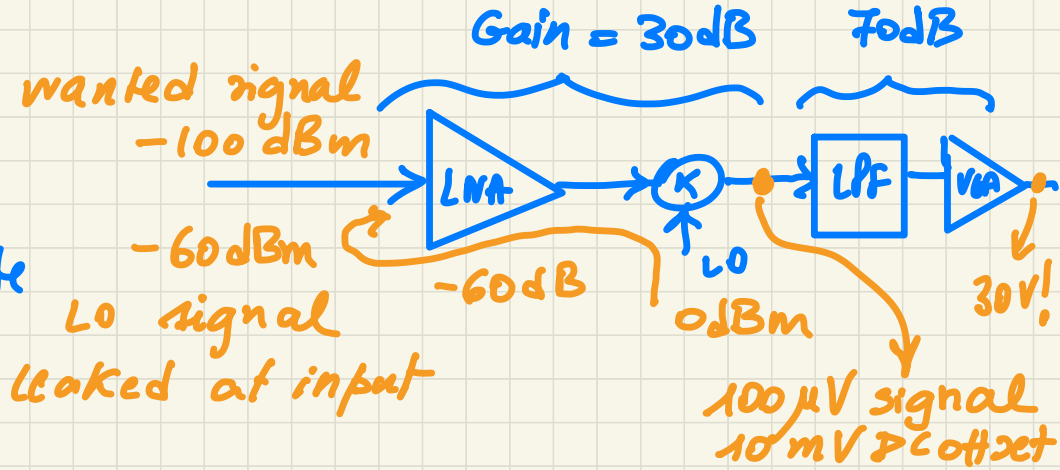


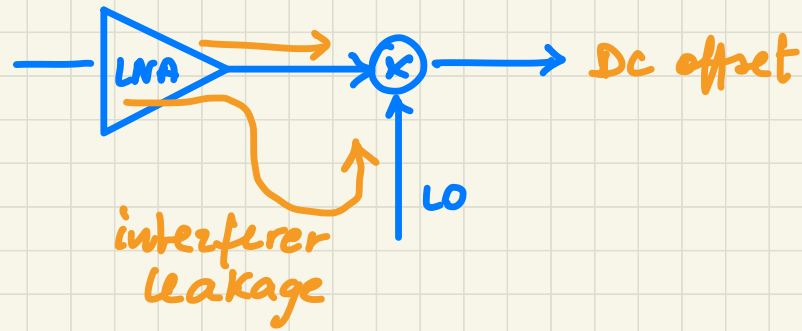
few mV of DC offset can saturate the VGA

$$P_s = -100 \text{ dBm}$$

$$P_{LO} = 0 \text{ dBm}$$

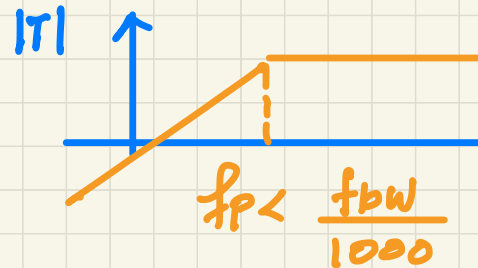
VGA would saturate
due to the 10mV
DC offset





How can we filter DC offsets?

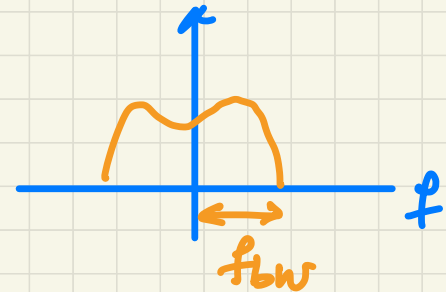
1) AC coupling

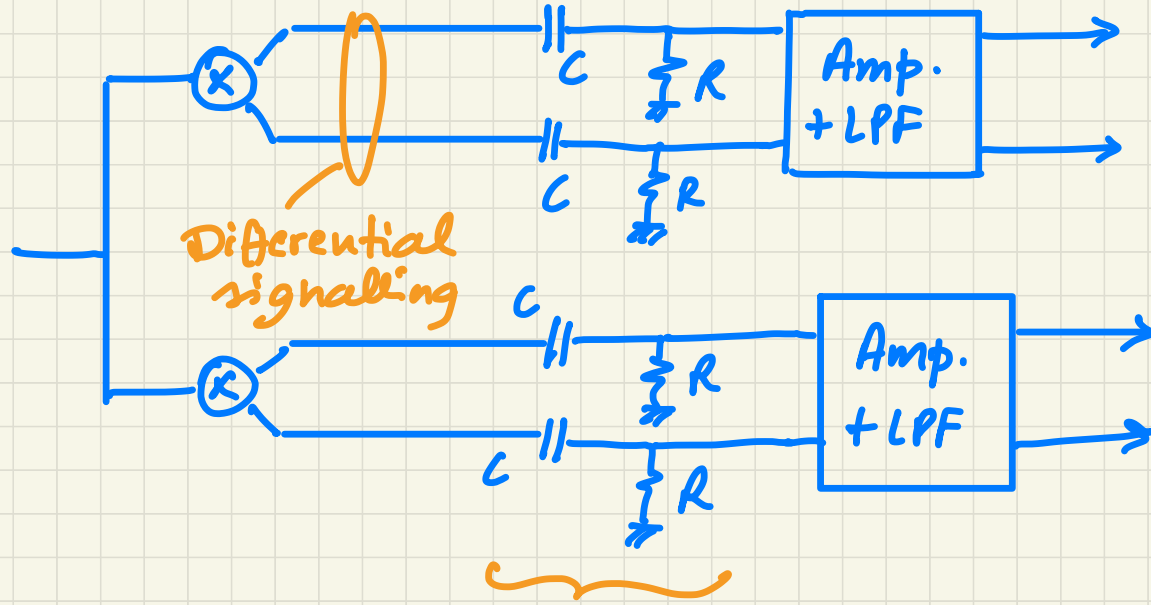


$$f_{bw} = 100 \text{ kHz}$$

\Rightarrow

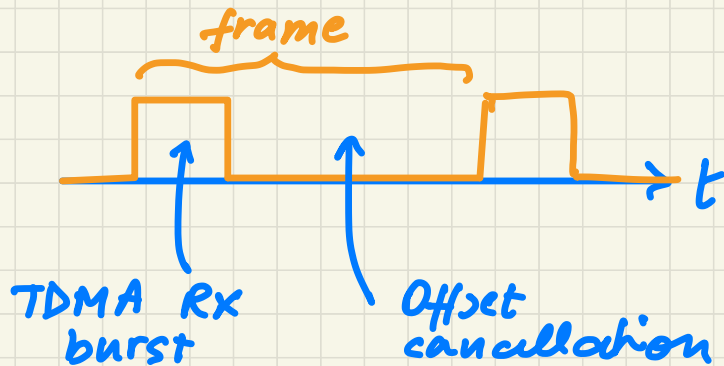
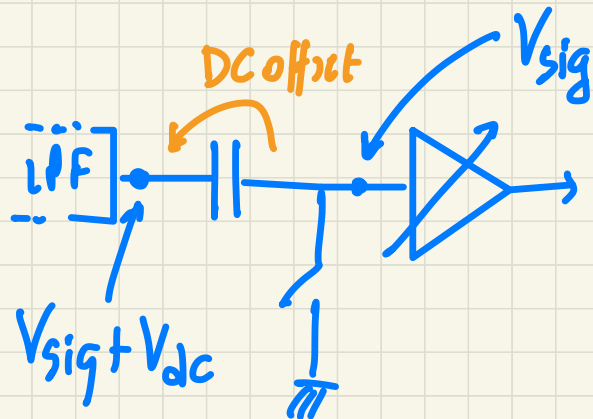
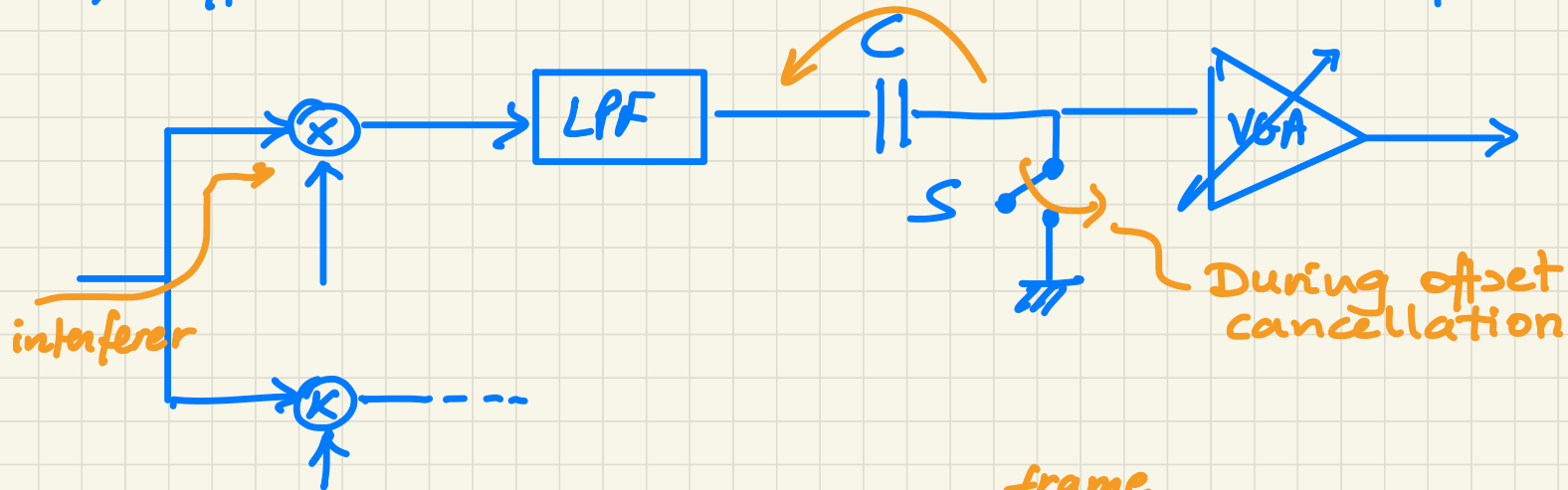
$$f_p = 100 \text{ Hz}$$

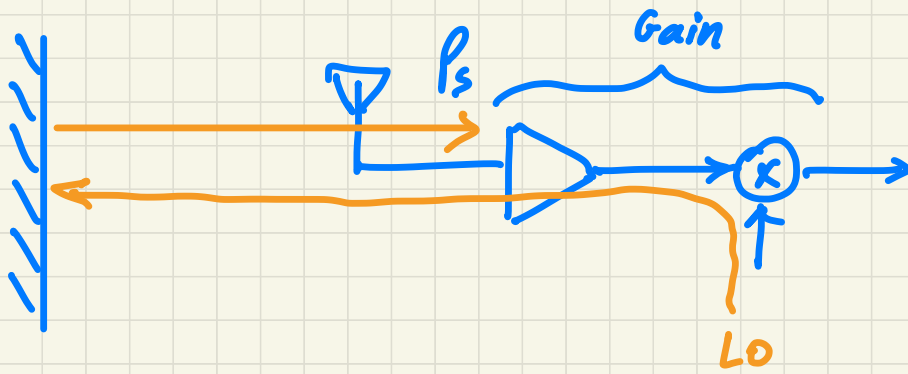




- AC coupling requires 4 capacitances
- R resistors introduce noise (degrading SNR)
↳ very large capacitances to make LF poles

2) Offset cancellation in TDMA systems

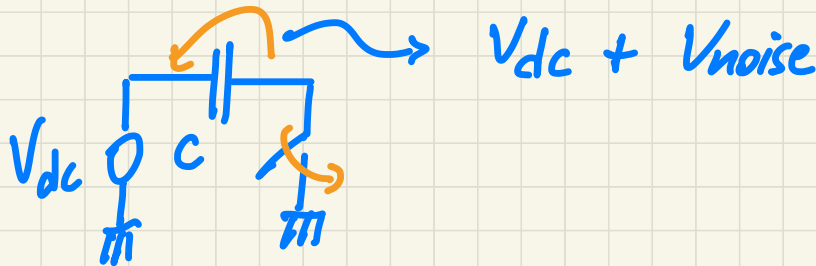




LO leakage and
Dc offset will
depend on reflections
 \Rightarrow variable on time

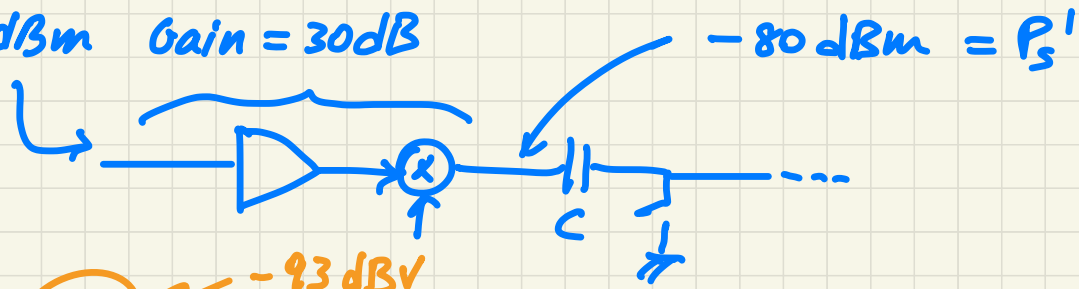
switched cap offset cancellation :

- solves the low-frequency pole issue
- does not solve the noise issue :



$$\overline{V_{noise}^2} = \frac{KT}{C}$$

e.g. $P_s = -110 \text{ dBm}$ Gain = 30 dB

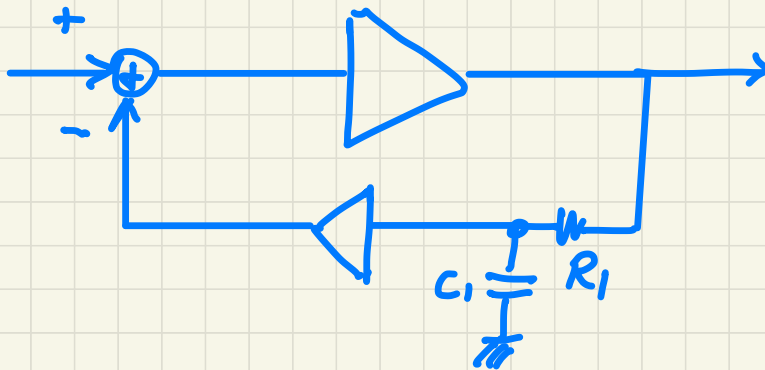


$$\text{SNR} = \frac{P_s'}{KT/C} > 15 \text{ dB} \Rightarrow C > 250 \text{ pF}$$

$KT/C \text{ [V}^2\text{]} \sim -108 \text{ dBV}$

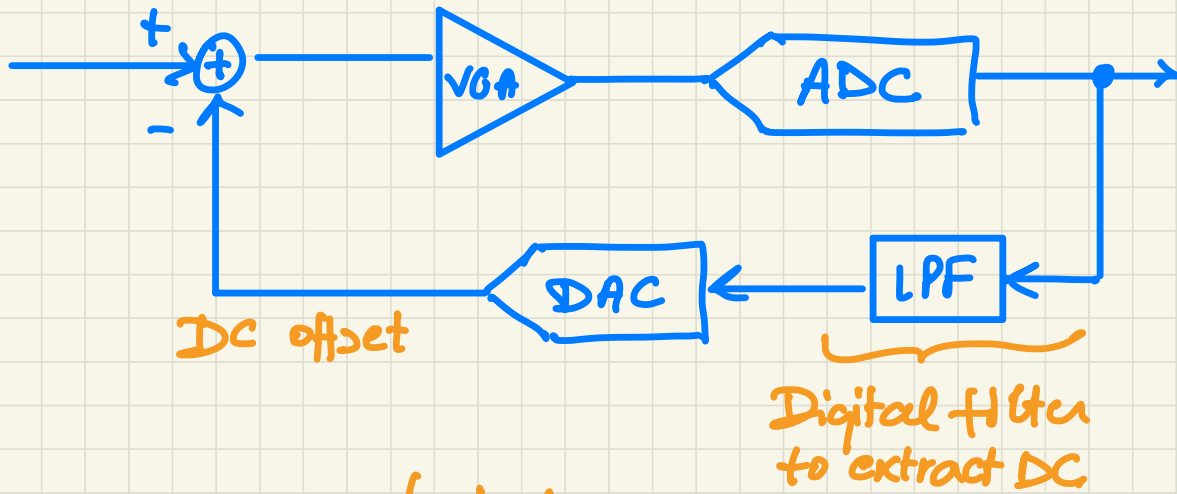
$P_s' \sim -93 \text{ dBV}$

3) Offset cancellation with feedback



requires larger C_1 than C of the ac-coupling

4)

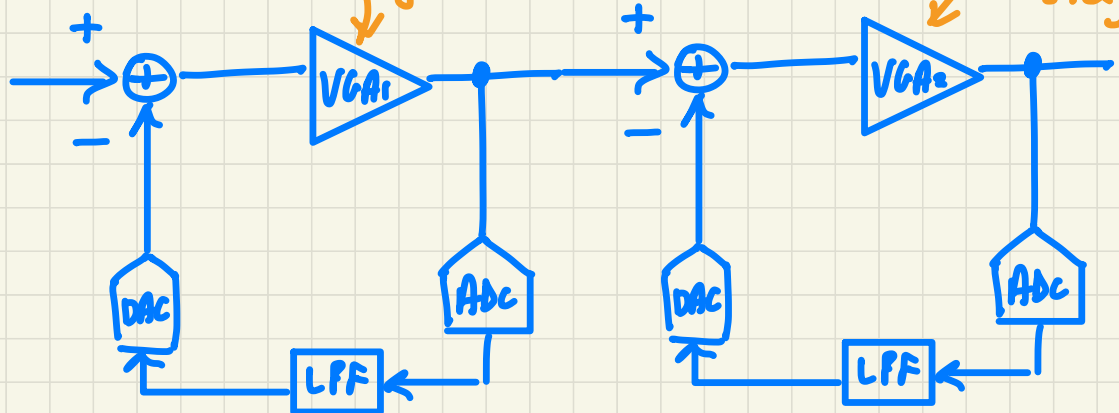


two-step :

to avoid
saturation
of VGA

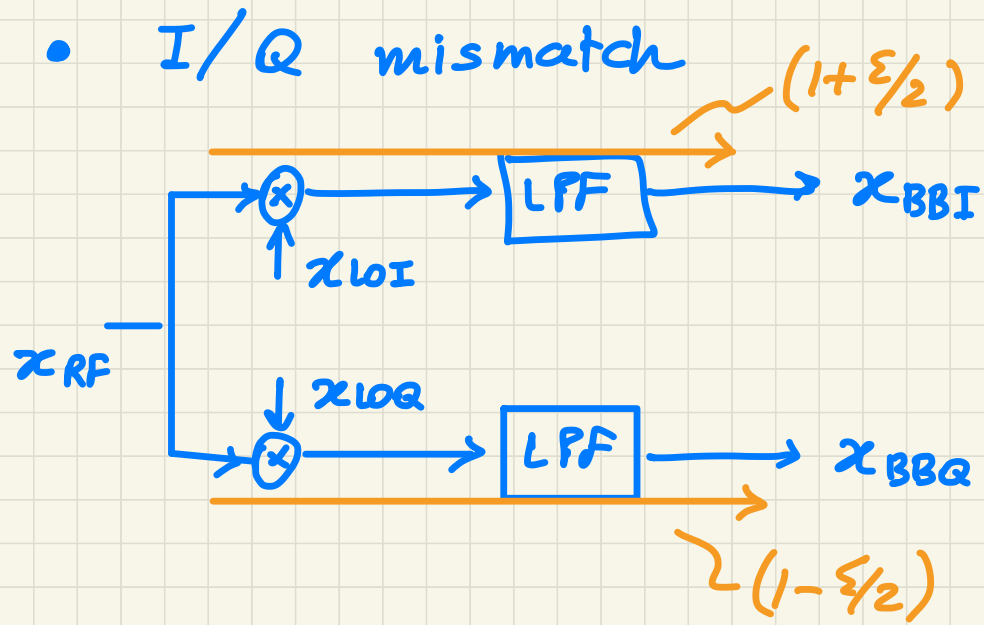
first stage

second stage



Most used in CMOS

- I/Q mismatch



two paths

- amplitude mismatch ϵ
- phase mismatch ϑ

$$x_{RF}(t) = x_I(t) \cdot \cos \omega_0 t + x_Q(t) \sin \omega_0 t$$

$$\begin{cases} x_{LOI}(t) = 2 \left(1 + \epsilon/2 \right) \cos \left(\omega_0 t + \vartheta/2 \right) \\ x_{LOQ}(t) = 2 \left(1 - \epsilon/2 \right) \sin \left(\omega_0 t - \vartheta/2 \right) \end{cases}$$

⇒

$$x_{\text{BBI}} = \underbrace{x_I(t) \cdot (1 + \varepsilon/2) \cos \frac{\theta}{2}}_{\text{wanted signal component}} - \underbrace{x_Q(t) \cdot (1 - \varepsilon/2) \cdot \sin \frac{\theta}{2}}_{\text{image leakage}}$$

Q component leaking into the I path for non-zero θ

$$x_{\text{BBQ}} = \underbrace{x_Q(t) \cdot (1 - \varepsilon/2) \cdot \cos \frac{\theta}{2}}_{\text{wanted signal component}} - \underbrace{x_I(t) \cdot (1 - \varepsilon/2) \cdot \sin \frac{\theta}{2}}_{\text{image leakage}}$$

$\varepsilon \Rightarrow$ gain error

$\theta \Rightarrow$ crosstalk
or image leakage

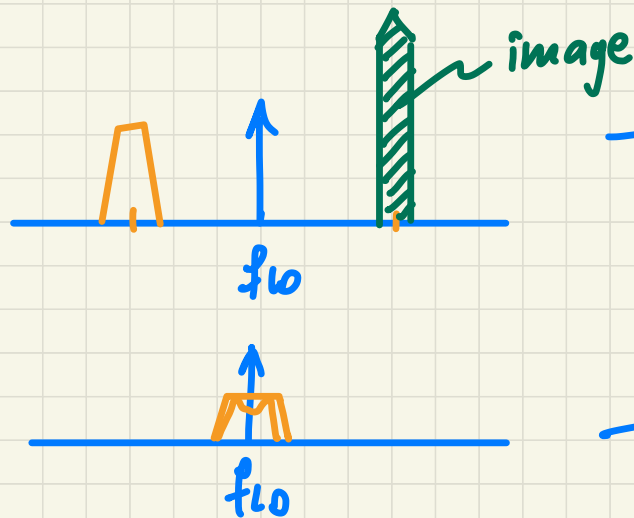
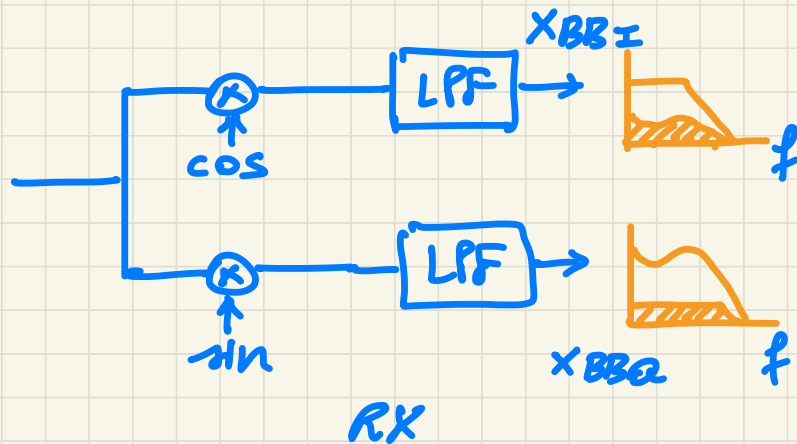
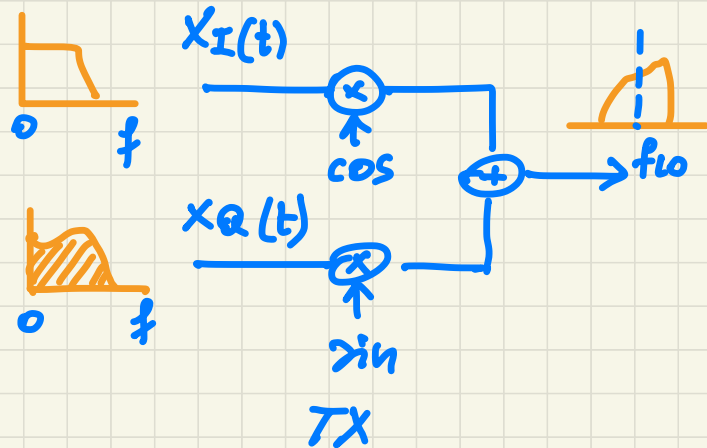


image problem in heterodyne

to IF



image problem in zero-IF

I

Q



to BB

$$x_{LOI}(t)$$

$$x_{LOQ}(t)$$

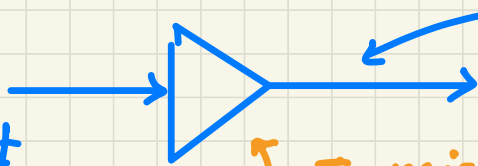
θ delay error

$$\sin\left(\omega_0 t - \frac{\theta}{2}\right) = \sin\left(\omega_0 t - \frac{\omega_0 \tau}{2}\right)$$

$$\theta = \omega_0 \tau = 2\pi f_0 \cdot \tau$$

e.g.

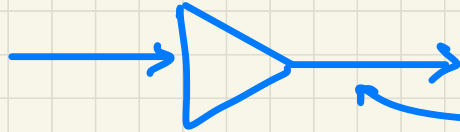
$\cos \omega_0 t$



$$\tau_1 = R_1 C_1$$

τ mismatch in delay

$\sin \omega_0 t$



$$\tau_2 = R_2 C_2$$

$$\tau = \tau_1 - \tau_2$$

$$\Delta \tau / \tau \cong \Delta R / R + \frac{\Delta C}{C}$$

\Rightarrow the larger ω_0 , the higher will be the phase error