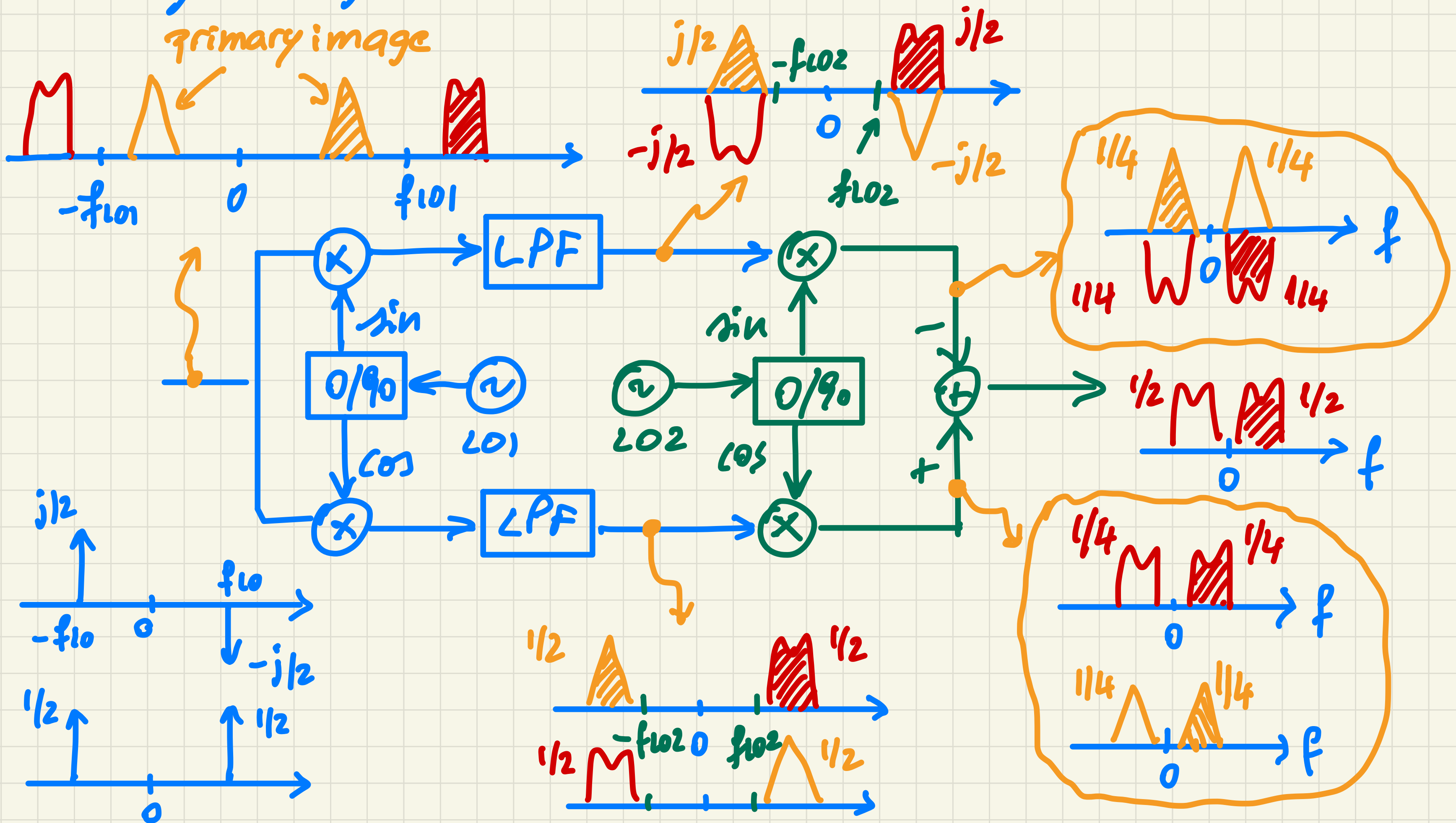
RF Circuit Design

L24

2020/21

Image-reject Rx : Weaver architecture



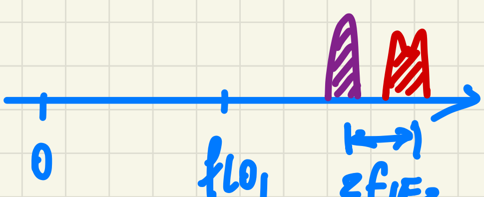
Comparison of Hartley vs. Weaver arch.

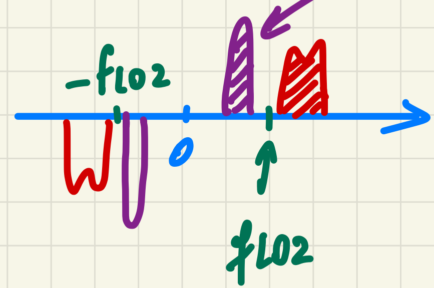
- **Hartley** : phase shifter has limited BW + sensitive to RC absolute accuracy $\Rightarrow$ limited IRR

  phase shifter introduces thermal noise and power loss

- **Weaver** : problem of secondary image

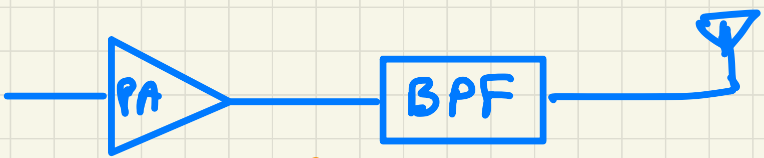
  sol: * IR filter * $IF_2 = 0$



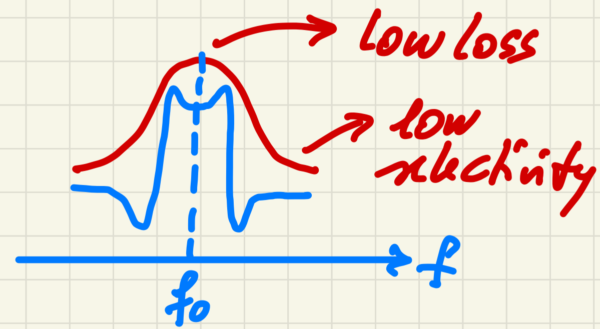


TRANSMITTER Architectures

ACPR : TX has to limit emissions
↓
linearity to avoid spectral regrowth in non-constant envelope modulations



Filter loss ⟺ selectivity



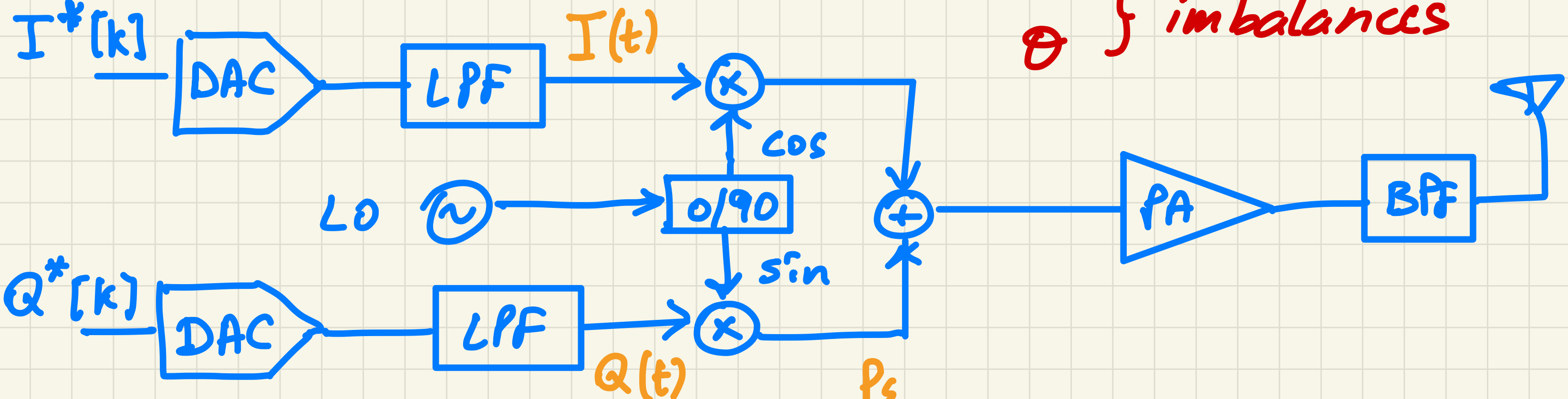
$$L = \frac{P_{ANT}}{P_{PA}}$$

power loss degrades efficiency of TX

e.g. $L = 2\,dB$
$P_{ANT} = 1\,W$
$P_{diss} = 370\,mW$ (dissipated in the filter)

- Direct-conversion TX

$\left.\begin{matrix}\varepsilon\\ \theta\end{matrix}\right\}$ imbalances



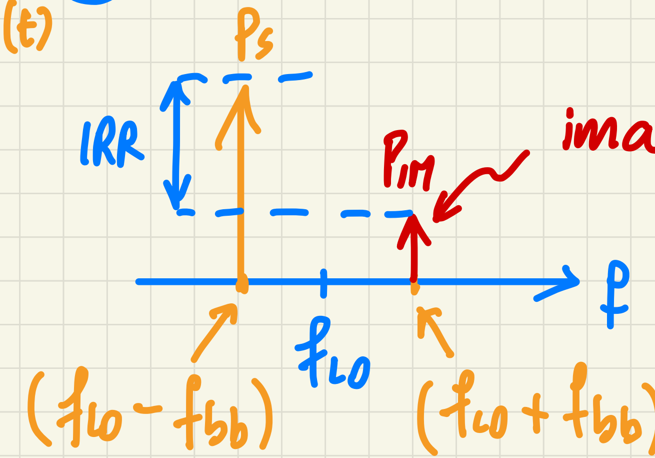


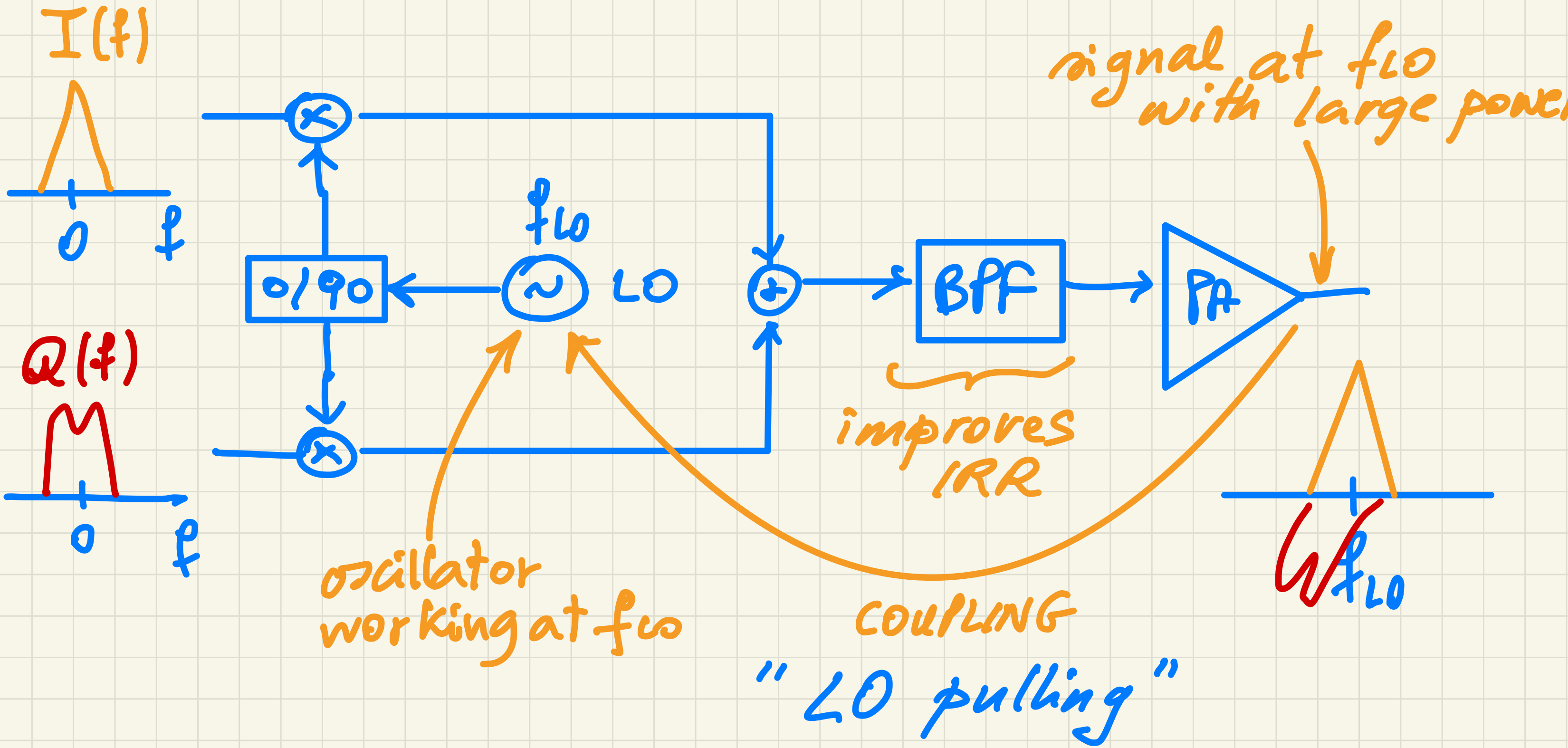
image signal induced by imbal.

$$I(t) = \cos \omega_{bb} t$$

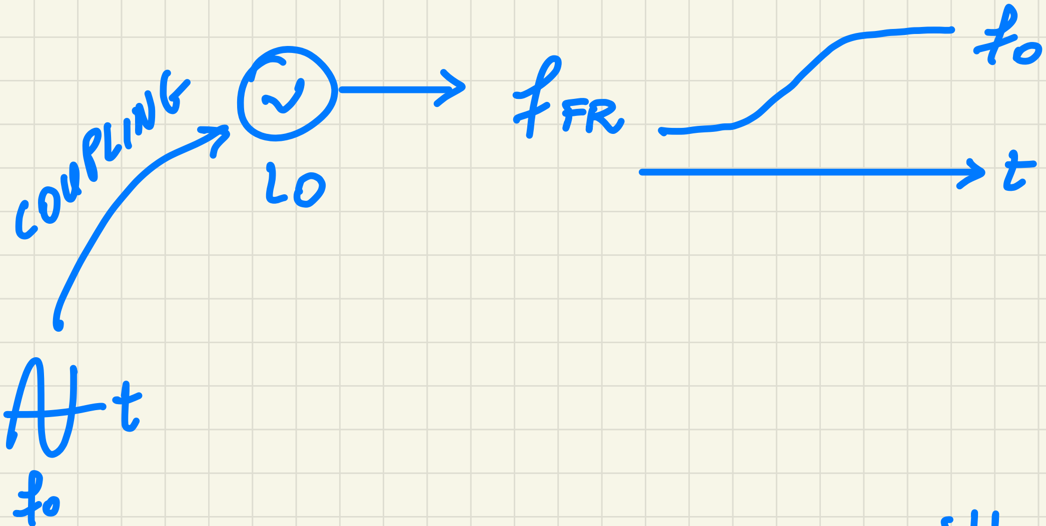
$$Q(t) = \sin \omega_{bb} t$$

$$\cos \omega_{bb} t \cos \omega_{LO} t - \sin \omega_{bb} t \sin \omega_{LO} t = \cos(\omega_{LO} - \omega_{bb}) t$$

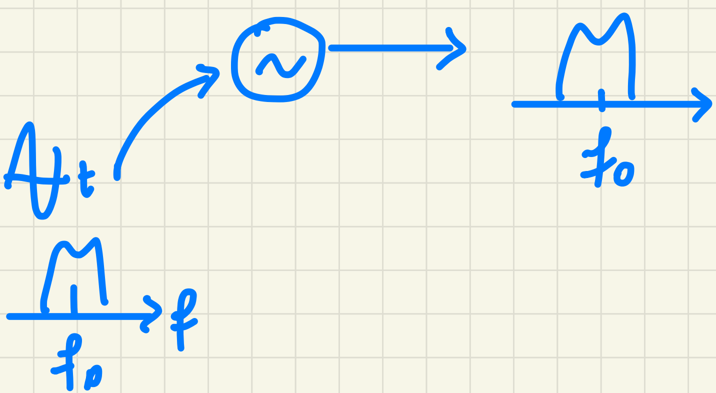
$$IRR = \frac{P_s}{P_{im}} = \frac{4}{\varepsilon^2 + \theta^2}$$



Oscillators are subject to INJECTION LOCKING



oscillator "locks" to the injected signal

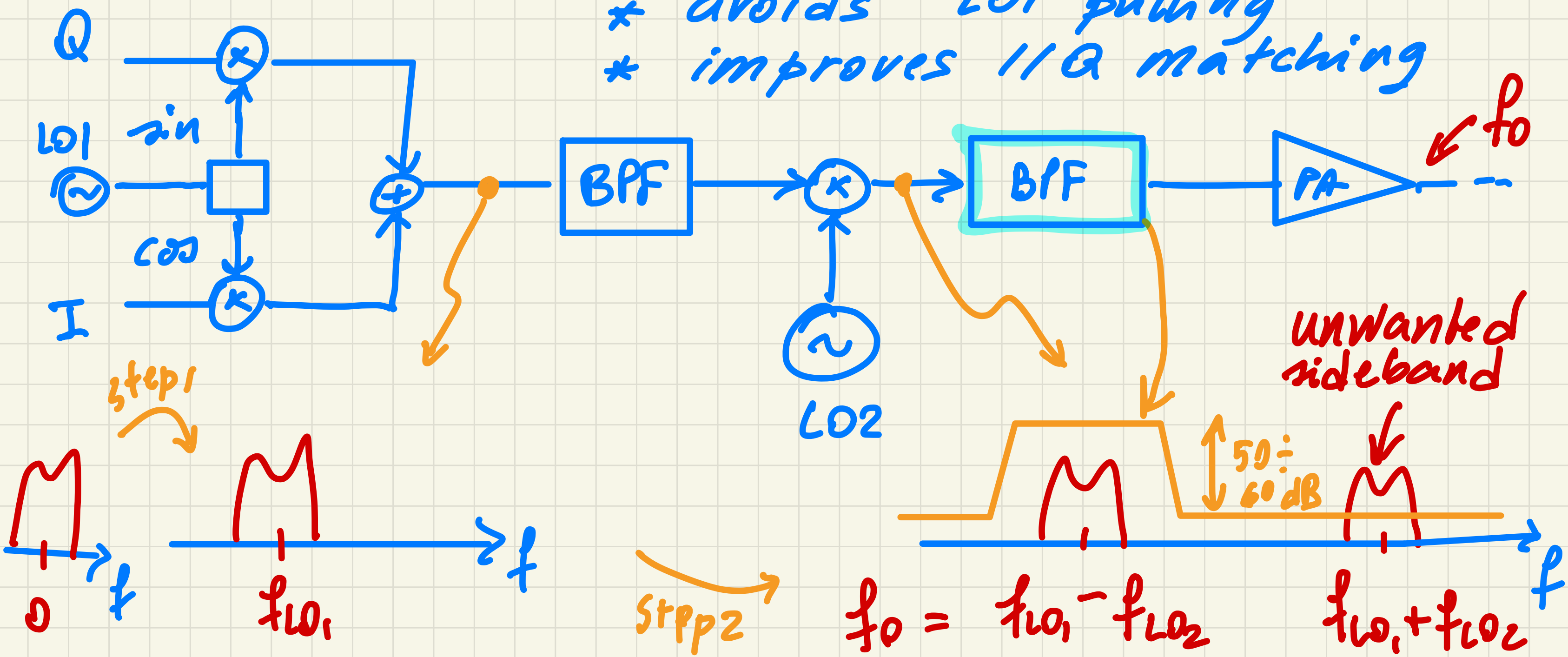


oscillator (locked) follows the input phase/frequency modulation

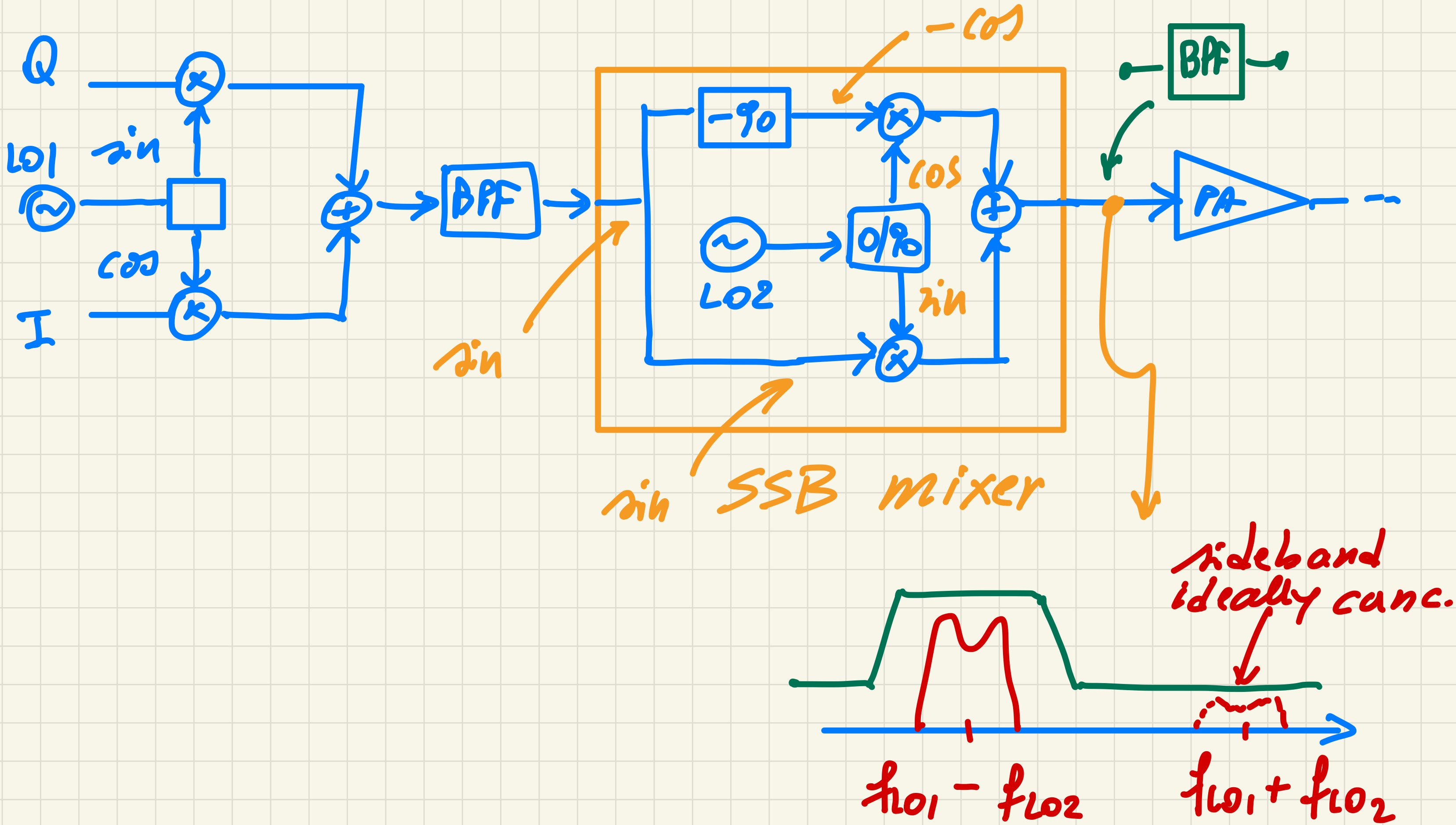
Solution : offsetting LO freq. w.r.t. PA frequency

- Two-step TX architecture :

  * avoids LO1 pulling
  * improves I/Q matching



Single-side band mixer (SSB mixer)



Examination :

- Written test   max. score 28+

- Oral test*   score $\dfrac{0 \div 2}{\text{max. score } 30+}$ 1 single question out of 40

- midterm test + final test (June 14th)

  or

- full test (June 14th, July 22nd, ...)

* I provide 40 questions to be published

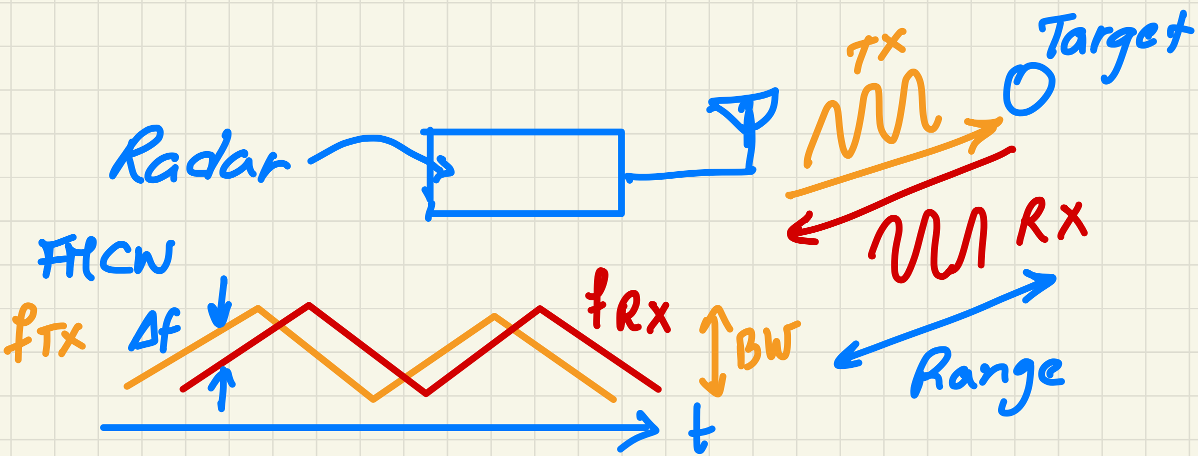
Theses

- Sensors and microsystems
  ↳ electronics in (3.3V) 0.35 μm CMOS
  or 0.18 μm CMOS (1.8V)
- In analog / RF circuit design
  28 nm CMOS (1V) or 22 nm CMOS
  or FinFET 16 nm CMOS

Communication System → pushes operating frequency to have higher bit rates

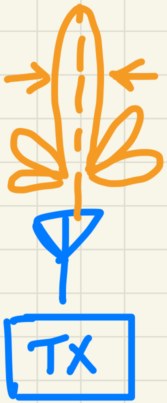
→ mm waves $\lambda \approx 1 \div 10$ mm
(wide BW available)

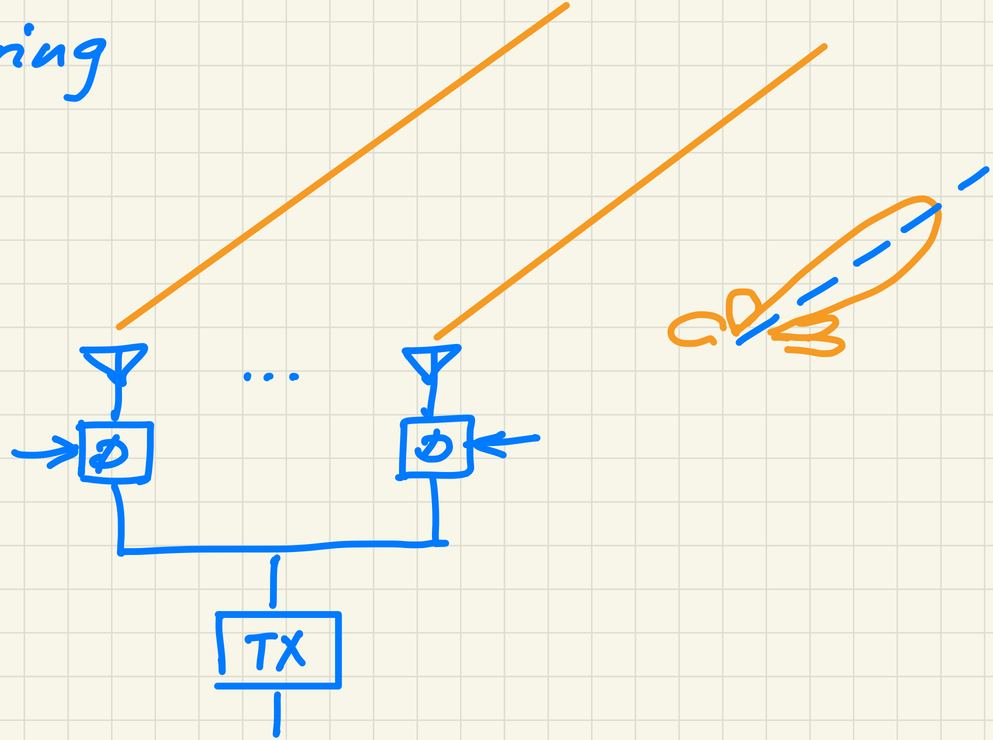
- enable high bit rate wireless ($1 \div 10$ Gb/s)
- enable ranging applications with fine resolution (cm)



Delay $\div$ Range $\Delta f \div$ Delay

Beam steering





higher f

$\downarrow$

narrower beam

Digitally assisted analog design

Topics:

- Frequency synthesizers in CMOS
  10 ÷ 100 GHz   28 nm → 22 nm

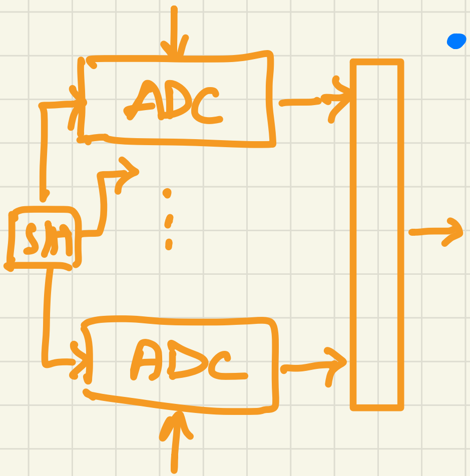
- RF TX for beam steering in CMOS

- A/D converters for 5G commun.
  BW ≃ 500 ÷ 800 MHz

  → GS/s ADCs

  ADC
  ENOB ≳ 10 bit

  → Time-interleaving



People : - myself RF
- prof. Samori ADC
- prof. Lacaita RF
- prof. Bonfanti ADC
- 10 PhD students

LO phase shifting