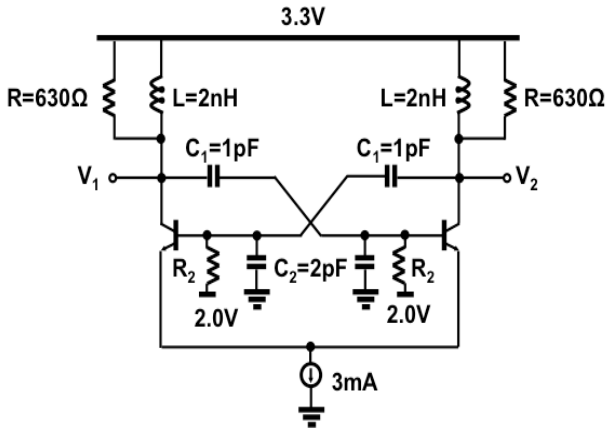
Tutorial T8

T8.1 Let us consider the oscillator in the figure. Assume infinite ß and $V_{BE,on}$ = 0.7V, $V_{BC,sat}$ = 0.5V for the BJTs.



a) Derive the circuit bias point.

b) Neglecting R_2 and r_π of the BJTs, evaluate both oscillation frequency and start-up margin.

c) Assuming full-switching of the differential pair, evaluate the oscillation amplitude and provide a plot of base and collector voltages of the BJTs over one period. Analyze the operating regions of the BJTs during the oscillation period and discuss the purpose of C_1 and C_2.

d) How is the tank resistance modified by a finite value of R_2? Size R_2 in order to worsen the quality factor of the resonant network by maximum 10%.

[Sol. a) I_C = 1.5mA, V_E = 1.3V, V_B = 2.0V, V_C = 3.3V, g_m = 60mS; b) f_0 = 4.36 GHz, $g_m RC_1/(C_1+C_2)$ = 12.6 > 1; c) A = 2.4V; the base-collector voltage, V_{BC}, ranges between -2.9V and +0.3V; the BJTs go from cut-off to forward active region. C_1 and C_2 help reduce the oscillation amplitude of the base voltage, allowing for a higher oscillation amplitude before incurring in saturation of the BJTs; d) R_2 = 630Ω.]

T8.2 Let V_b = 0.15V, L = 1nH, R = 10Ω, C = 250fF, C1 = 1pF, R1 = 1kΩ, $\mu C_{ox}(W/L)$=120mA/V^2 (nMOS), $\mu C_{ox}(W/L)$=56mA/V^2 (pMOS) and V_t=0.45V for all transistors.

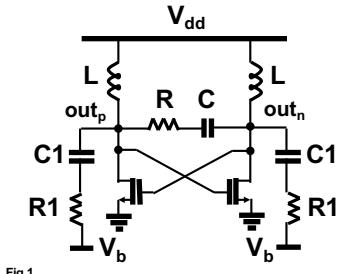


Fig.1

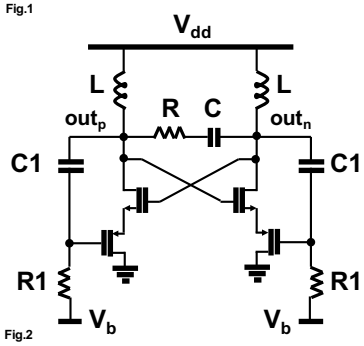


Fig.2

a) With reference to the circuit in Fig. 1 (let V_{dd} = 0.55V), after deriving the bias current flowing into the FETs, calculate the frequency of oscillation and the gain margin for the oscillation start-up (i.e. the loop gain at the oscillation frequency).

b) With reference to the circuit in Fig. 2 (let V_{dd} = 1.5V), after deriving the bias current flowing into the FETs, calculate the frequency of oscillation and the gain margin for the oscillation startup.

[Sol. a) I = 600 uA, f_0=7.114GHz, $|LG(j\omega_0)|$=3.4; b) I=2mA, f_0=7.114GHz, $|LG(j\omega_0)|$=5]