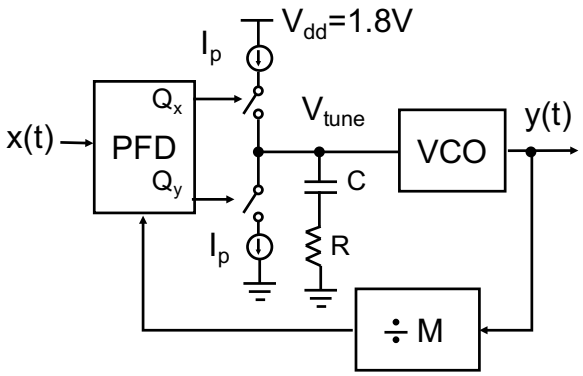
Tutorial T3

T3.1. In the PLL in figure, the VCO has a free-running frequency of 3 GHz and a sensitivity of 300 MHz/V, with M = 100 and I_p = 0.1 mA.



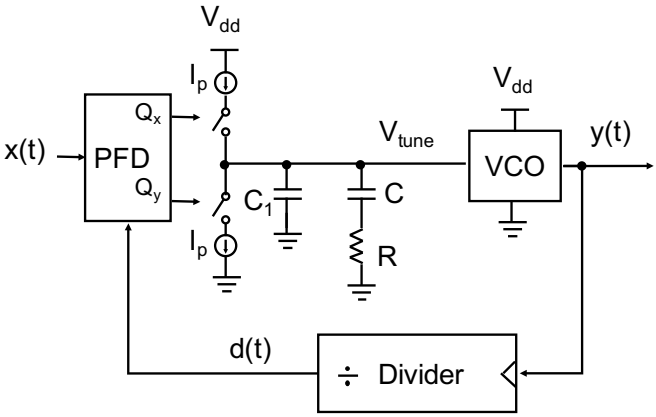
a. Derive the linear equivalent model of the PLL and the values of R and C to have closed-loop poles at 10 kHz and at 45 degrees on the Gauss plane.

b. What is the contribution of the thermal noise of the resistor R to the phase noise $\mathcal{L}_y(f)$ at the output $y(t)$ at 1 MHz? (Please provide the value in dBc/Hz)

c. Taking into account the contributions of (i) a white phase noise $\mathcal{L}_x(f)$ of -140dBc/Hz, affecting the reference $x(t)$, and (ii) the thermal noise of R, plot the phase noise $\mathcal{L}_y(f)$ at the output $y(t)$ (Please provide the relevant values on the x and y axes).

[Solution: a. R = 296 Ω, C = 76 nF; b. $\mathcal{L}_y$(1MHz) = -126.7 dBc/Hz; c. Spectrum has $\mathcal{L}_y$(0) = -100 dBc/Hz, zero at 3 kHz, two poles at 10 kHz, with peak $\mathcal{L}_y$(10 kHz) = -89.6 dBc/Hz]

T3.2. In the PLL in figure, V_{dd} = 3V, R = 1.6 kΩ, C = 100 nF. The PLL should synthesize all the frequencies from 1900 to 2100 MHz in steps of 1 MHz.



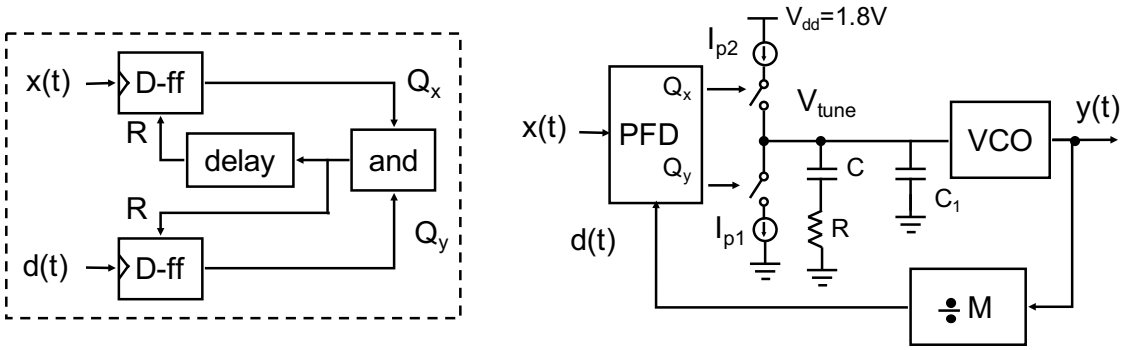
a. Describe the behavior of the circuit in the case of a constant current drained from the VCO input and describe the steady state condition of the PLL.

b. If this leakage current is 100 nA (assuming it is much smaller than the charge-pump current), set the value of C_1 to limit the spur in the output spectrum to -50 dBc, and derive the minimum K_{vco} to cover the whole frequency range with the given supply voltage.

c. Calculate the cross-over frequency of the loop gain that maximizes the phase margin. Derive the value of the maximum phase margin and the charge-pump current I_p.

[Sol. a. M = 2000, $t_e/T_x = I_L/I_P$; b. K_{vco} = 418.7 Mrad/(Vs), C_1 = 336 pF, f_z = 1 kHz, f_p = 296 kHz; c. f_u = 17.2 kHz, PM = 83 deg, I_p = 2 mA.]

T3.3. In the PLL in figure, we are using a *modified* PFD schematic which is shown inside the dashed box. Unlike a conventional PFD, the block "delay" after the "and" gate introduces a delay t_d in the reset signal of just one of the two D-type flip-flops.



a. Derive and plot the input-output characteristic of the PFD (i.e. input phase vs. output average voltage), drawing the voltage waveforms of all PFD nodes (x, d, Q_x, Q_y, R) for both positive and negative input phase delays. Explain whether the PFD acts as a phase and frequency detector.

b. Using the PFD in the PLL in figure, where $K_{VCO}/2\pi$ = 20 MHz/V, I_P = 8 mA, f_x = 2 MHz, t_d = 2 ns, M = 1024, calculate the time delay between $x(t)$ and $d(t)$ at steady state.

c. Set the values of R, C, and C_1 to have (i) a maximum spurious tone at y output with -70 dBc level, (ii) a cross-over frequency of the loop gain at 20 kHz and (iii) phase margin of 60 degrees.

d. Keeping the same values of K_{VCO}, I_P, f_x, t_d, M and the same stability margin, which one of the design parameters you would modify to reduce the level of the reference spur? Illustrate the inherent drawbacks of your choice.

[Sol. a. The PFD/CP block has time offset -t_d and current $I_P t_d f_x$ at t_e = 0; b. t_e = -2 ns; c. C_1 = 2 nF, R = 804 Ω, C = 28.7 nF; d. After some manipulation, SFDR can be re-written as a function of the unity-gain frequency: SFDR = $(M\omega_u\omega_p t_d^2)^2$. Thus, the only free parameters are ω_u and ω_p. Reducing both of them, I would trade the loop bandwidth with the level of the spur.]