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EXECUTIVE SUMMARY OF THE THESIS

High-Performance Time-to-Digital Converter IP-Core for Xilinx Ultrascale/Ultrascale+ FPGAs

LAUREA MAGISTRALE IN ELECTRONICS ENGINEERING - INGEGNERIA ELETTRONICA

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1. Introduction

The increasing demand for very precise time measurements in scientific research applications, ranging from the biomedical field to the industrial one, has led to the need for instruments, called Time Interval Meters (TIMs), characterized by features such as a resolution and single-shot precision in the picoseconds (ps) order, and a sampling rate in the order of hundreds of megahertz (MHz) to correctly process the detected physical events. Several TIM solutions are already present in the literature, implemented both in Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). To cope with features such as fast-prototyping and low time-to-market, the FPGA approach has been chosen for this work, and a fully-digital TIM, a.k.a. Time-to-Digital Converter (TDC), has been implemented. To exploit the benefits of the scaling, the 20-nm Xilinx Ultrascale (XUS) technology has been investigated in this work, allowing achieving high measurement rates, low Dead-Time, high-resolution, and excellent single-shot precision. In particular, a single-shot precision in the order of 3 ps has been achieved, along with a maximum measurement rate of 200 Msps per channel, thus satisfying the high count-rate capability requirement of state-of-the-art detectors. From the design point of view, the TDC has been implemented exploiting a Tapped Delay-Line (TDL) structure, and it has been fully tested on a Kintex Ultrascale FPGA, hosted in the KCU105 Evaluation Board. To better investigate the power/precision and area/precision trade-offs, two different TDL solutions have been tested. The first solution is more performant in terms of single-shot precision at the expense of higher area occupancy, and it is based on the CARRY primitives (i.e., CARRY8) available in the fabric of the Xilinx FPGA (i.e., a single-shot precision of 2.8 ps, a power con-

sumption of 0.596 W, and a maximum number of channels, which is used as the index of area occupancy, equal to 62). The second solution is instead less performant but more power/hardware-efficient, and it relies on Digital Signal Processor (DSP) primitives (i.e., DSP48E2) (i.e., a single-shot precision of 44 ps , a power consumption of 0.343 W, and a maximum number of channels equal to 150). Finally, a hybrid architecture exploiting both CARRY and DSP resources has been tested, leading to results that show the best features of both TDL types (i.e., a single-shot precision of 3.8 ps, a power consumption of 0.49 W, and a maximum number of channels equal to 74).

1.1. TDC architectures

FPGA implementations are characterized by lower time-to-market and costs with respect to the ASIC, at the expense of lower performances (especially in terms of power consumption and area occupancy) due to the impossibility of perfectly tuning the design. The main TDC architectures are reported in [4], the most common being: Ring Delay-Line (RDL) TDC, Shift-Clock Fast-Counter (SCFC) TDC, Vernier Delay-Line (VDL) TDC, and Tapped Delay-Line (TDL) TDC. The RDL is implementable only in ASIC since in FPGA it is not possible to compensate the PVT variations of the ring oscillator. RDL-TDCs generally achieve excellent measurement precision and almost null power consumption since ASICs make it possible to perfectly tailor the TDC. The SCFC is a very compact architecture but suffers from a limited resolution due to the limited number of available clock lines on the FPGA fabric. Even VDL-TDCs are not so suitable for highly-scaled FPGAs (e.g., 28-nm) due to the mismatches. The TDC architecture that best fits with the FPGA is the TDL-TDC. The TDL consists of a chain of buffers on which the first asynchronous signal (i.e., START) propagates with a certain delay t_p on each buffer (or "tap", also called "bin"), and the second asynchronous event (i.e., STOP) is a clock that samples the state of the chain by saving the taps' values into a battery of flip-flops (FFs). The time measurement will thus be a thermometric code provided by the FFs, representing the number of crossed bins and, therefore, the time distance between START and STOP. Figure 1 shows the structure of a TDL.

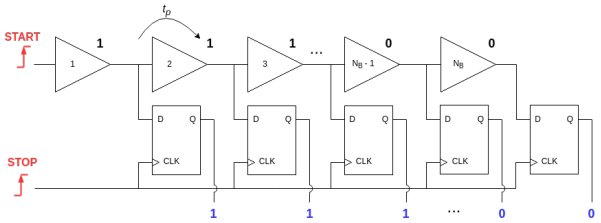

Figure 1: TDL structure and propagation mechanism.

This architecture achieves a high-resolution at the cost of high area occupancy due to the long chain structure and to the Calibration algorithm needed to compensate process, voltage, and temperature (PVT) variations the buffers suffer from. Besides, a direct trade-off exists between LSB and FSR; in fact, considering a TDL composed of N_B bins, the LSB is equal to t_p and the FSR is equal to $N_B \cdot t_p$. We will see in Section 2.1 how to break this trade-off.

1.2. State of the Art

Table 1 reports several FPGA and ASIC TDC implementations existing in the literature, classifying them according to the main Figures of Merit (FoMs).

We can see from the Table that all the reported TDL-based implementations achieve LSBs and single-shot precisions in the order of tens of picoseconds, alongside good linear behaviors (i.e., DNL, INL < 20 LSBs); FoMs that are comparable to ASIC solutions. This is achieved thanks to Sub-Intepolation and the bin-by-bin calibration procedure to overcome PVT variations, which will be described in Sections 2.2 and 2.3. However, as said in Section 1.1, the TDL-TDC suffers from a trade-off between FSR and LSB. For example, we can see in the [6] implementation that the achieved resolution is very good (i.e., 1.14 ps), but it is paid with a low FSR (i.e., 10 s). Furthermore, we can observe that the FPGA implementations offer power consumptions in the order of mW instead of the ASIC ones, which are in the μW order.

2. TDL-TDC Design rules

The TDL-TDC suffers from three main problems:

Feature	ASIC TDCs			FPGA TDCs		
	[2]	[1]	[7]	[8]	[9]	[6]
Technology	180 nm	350 nm	130 nm	Kintex-7	Actel 130-nm	Spartan-6
Architecture	RDL	RDL	SCFC	SCFC	VDL	TDL
Application	TOF	Laser R.F.	Spectroscopy	TOF	Nuclear	TOF
LSB [ps]	2	40	781	89.3	42	1.14
Precision [ps r.m.s.]	1.44	2.2	300	56.2	16.4	6
DNL [LSB]	[-1:1]	N.A.	[-0.05:0.05]	[0.44:0.87]	[-1:0.9]	N.A.
INL [LSB]	[-1:1.3]	[-0.6:0.6]	[-0.05:0.05]	[0.44:0.82]	[-1:3.5]	19.36
FSR [ns]	130	22	N.A.	N.A.	6.5e+05	1e+10
Dead-Time [ns]	303	N.A.	N.A.	4.3	100	2000
Power [mW]	18	0.0016	6.5	N.A.	N.A.	750
Num. of Chs	N.A.	N.A.	48	256	N.A.	N.A.

Table 1: Comparison of different TDC solutions, both in ASIC and FPGA.

1. a trade-off between LSB and FSR is present (see Section 1.1);
2. if the TDC is implemented in a certain technological node, there is a minimum possible t_p that limits the resolution;
3. PVT variations cause dispersion in the t_p value, thus requiring working in a calibrated mode to maximize the precision and the linearity of the system.

In this Chapter, we will describe the proposed solutions to solve each problem: Nutt-Interpolation, to solve 1; Sub-Interpolation, to solve 2; Calibration, to solve 3.

2.1. Nutt-Interpolation

To break the LSB vs. FSR trade-off, Nutt-Interpolation has been implemented. This technique consists of composing the timestamp of a Fine part and a Coarse one [5]. T_{FINE} is equal to the time distance from the START event to the following clock rising-edge (i.e., the STOP signal); hence, it is managed by the TDL itself. T_{COARSE} is equal to the number (N_{COARSE}) of clock cycles elapsed from the power-on of the instrument to Fine measurement generation, multiplied by the clock period T_{CLK}. The time measurement will be equal to:

$$T_{MEAS} = N_{COARSE} \cdot T_{CLK} - T_{FINE} \qquad (1)$$

Figure 2 shows the explained concept.
If a BIT_COARSE-wide counter is used to count the elapsed clock cycles, the achieved FSR is equal to $2^{BIT\_COARSE} \cdot T_{CLK}$; on the other hand, the LSB is equal to t_p. Therefore, FSR and LSB are no more dependent, and the trade-off is solved.

2.2. Sub-Interpolation

The Sub-Interpolation is a technique that exploits redundancy in the measurements to reduce the quantization error of the TDC, thus improving its resolution [3]. In fact, it allows lowering the LSB as much as the desired delay, beyond the minimum one offered by the technological node. In this work, the Super Wave Union (SuperWU) Sub-Interpolation algorithm, characterized by placing more physical TDLs in parallel, has been implemented. M TDLs have been placed in parallel, each one with a real number N_B of buffers, resulting in the so-called Virtual Tapped Delay-Line (V-TDL), composed of $N_V = N_B \cdot M$ virtual-taps with a M-time faster propagation delay. In fact, considering $m \in [1;M]$ replicas of the measurement of the same time interval, performed using M TDLs with $n_B \ \epsilon \ [1;N_B]$ real bins characterized by the propagation delays $t_{p,B}[n_B]$, a V-TDL with $n_V \ \epsilon \ [1;N_V\ ]$ "virtual" bins with $t_{p,V}[n_V]$ propagation delays is obtained, where:

$$\begin{cases} t_{p,V}[n_V] = \frac{1}{M} \sum_{m=1}^{m=M} t_{p,B}[n_B[m]] \\ n_V = \sum_{m=1}^{m=M} n_B[m] \end{cases} \qquad (2)$$

To achieve an effective reduction of the propagation delays on the virtual-bins, the replicas of the TDLs should be as uncorrelated as possible. Using the SuperWU algorithm, the achieved resolution is M-times better than the case without Sub-Interpolation.

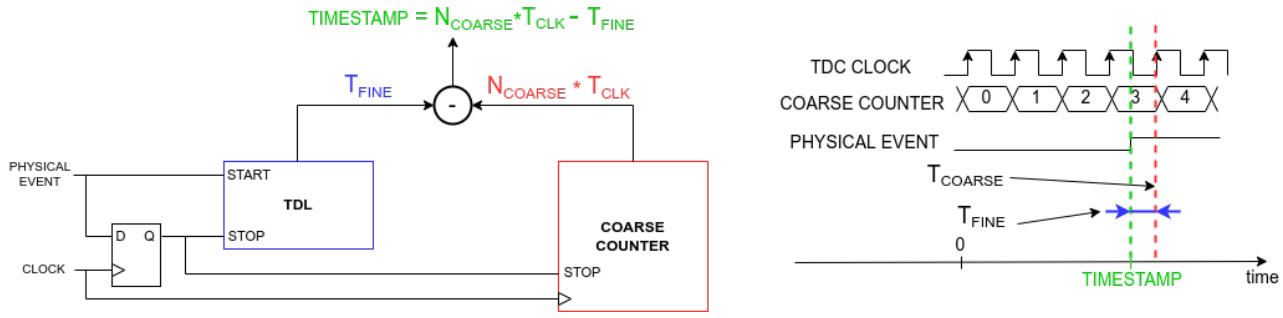

Figure 2: Nutt-Interpolation working principle.

2.3. Calibration

Since each buffer composing the TDL (or V-TDL, if Sub-Interpolation is performed) is affected by PVT variations, a periodic bin-by-bin calibration process is required, otherwise, the system would suffer from unacceptable non-linearities. This process consists of building a Calibration Table (CT) listing all the propagation delays $t_p(n)$ of each bin n (or "virtual" bin) composing the TDL (or V-TDL), thus allowing us to always know their exact value and obtain a reliable measurement. The CT is built by performing a Code Density Test (CDT) on the TDL (or V-TDL), which is T_{CLK}-wide if the Nutt-Interpolation is implemented and composed of a total of N real (or virtual) bins. The CDT consists of sending a set of random input signals (N_C in total), characterized by a uniform distribution, to the TDL (or V-TDL) and counting how many samples $N_X(n)$ fall into each real (or virtual) bin. The higher the count on a particular bin, the slower the bin. Finally, the $t_p(n)$ of each bin is obtained thanks to a normalization to T_{CLK}:

$$t_p(n) = \frac{N_X(n)}{N_C} \cdot T_{CLK}\ ,\ n \in [1; N] \qquad (3)$$

Figure 3 graphically explains the procedure just described.
Due to the crossing of different clock regions, some bins can be particularly slow. They will be referred to as "ultra-bins" and are responsible for worsening the single-shot precision of the TDC. Once the CT is built, the Characteristic Curve (CC) of the device can be derived. The CC is nothing but the integration of the CT, thus representing, for each bin, the corresponding time measurement in picoseconds.

3. Architecture

Figure 4 shows the block diagram of a single channel of the TDC.
The TDC implemented in this work is composed of three channels. Let's now describe each module composing a generic channel.

3.1. Virtual Tapped Delay-Line

The Virtual Tapped Delay-Line (V-TDL) is the result of the SuperWU Sub-Interpolation, where four 512-tap-long TDLs have been placed in parallel to perform the Fine measurement of the timestamp. In FPGA, a TDL is created by cascading the available logic blocks on the fabric, which are usually the carry chains of the adders [6][3][4]. Two different solutions have been implemented in this work:

- CARRY-chain, which is a cascade of Xilinx's CARRY8 primitives. The START signal propagates along the carry logic, and a thermometric code is produced by the FFs.
- DSP-chain, which is a cascade of Xilinx's DSP48E2 blocks. All the DSP blocks are used in Dual 24-bit mode, meaning that the internal 48-bit ALU works as two independent 24-bit ALUs to propagate the START signal, thus generating two thermometric codes rather than one.

Figure 5 shows the structure of both TDLs.
The difference between the two types of TDL is that the CARRY-chain is characterized by more homogeneous propagation delays on the bins, allowing us to achieve good single-shot precision; however, it needs external FF resources to sample the TDL, thus leading to high hardware occupancy. On the other hand, the DSP-chain is a more compact structure that avoids using external FFs since the internal registers of the DSP blocks are used to sample the TDL; however,

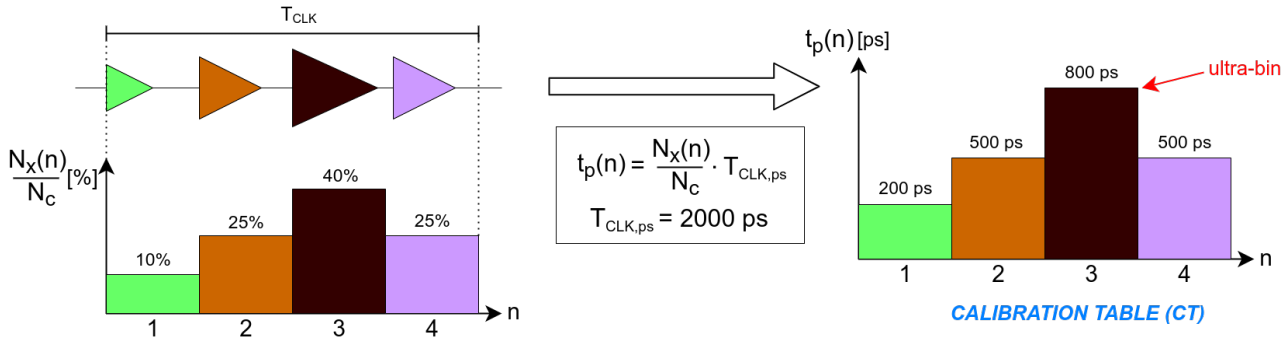

Figure 3: CDT and resulting CT, in the example case with $N = 4$ and $T_{CLK} = 2000\ ps$.

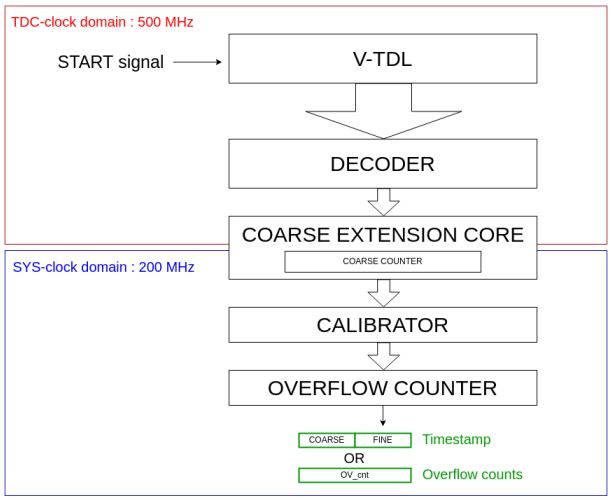

Figure 4: Block diagram of a single channel of the TDC.

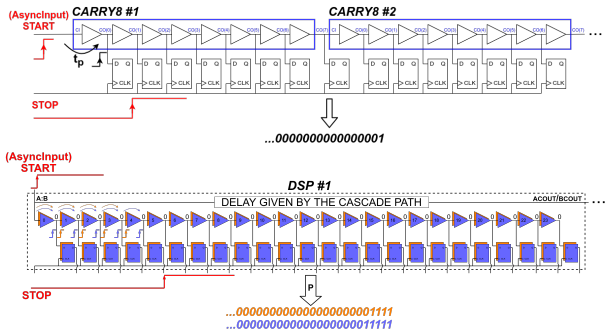

Figure 5: Structure of a CARRY-chain (at the top) and DSP-chain (at the bottom).

it is characterized by huge "ultra-bins" due to the delays of the cascade path from one DSP block to the following one and, therefore, by a worse single-shot precision. We will see from the experimental results in Chapter 4 that the best performances are reached by performing a "hybrid" Sub-Interpolation exploiting the best features of both types of TDL.

3.2. Decoder

The Decoder has the task of converting the thermometric codes, provided by the V-TDL, into binary codes. The conversion is performed with a Thermo-to-Binary (T2B) Engine, which sums all the '1's ('0's) in the case of channel's sensitivity to the rising-edge (falling-edge) of the START signal. This module also contains another sub-module called "Sub-Interpolation Matrix", which allows selecting, at run-time, how many TDLs to involve in the Sub-Interpolation process.

3.3. Coarse Extension Core

The Coarse Extension Core (CEC) implements the Nutt-Interpolation (see Section 2.1) by attaching the Coarse information to the already-calculated Fine one.

3.4. Calibrator

This module is in charge of performing the calibration process, already described in Section 2.3, on the Fine data. Once built the CT and the CC, the Calibrator receives the Fine field from the CEC, and the precise propagation delay up to the hit bin is read from the CC; therefore, the Fine time measurement, in ps, is retrieved.

Feature	4 CARRY-chains	2 CARRY-chains + 1 DSP-chain
Clock TDC Freq.	500 MHz	
$N_B/M/N_V$	512/4/2048	
Full-Scale Range	some days	
Max. Channel Rate	200 MHz	
Dead-Time	2 ns	
Single-Shot Precision	2.8 ps	3.8 ps
TDL mean propagation delay ($\overline{t_{p,V}}$)	1.2 ps	1.7 ps
TDC ultra-bin	7 ps	11.3 ps
DNL_{max}	0.22 ps	0.3 ps
INL_{max}	5.8 ps	12 ps
LUT/FF/BRAM (for one ch.)	5431/7716/3.5	5429/6691/3.5
Number of Chs (*)	up to 62	up to 74
Power Consumption (for one ch.)	0.596 W	0.49 W

Table 2: Performances and hardware occupancy of a V-TDL composed of 4 CARRY-chains in parallel and of 2 CARRY-chains + 1 DSP-chain in parallel. (*) in the xcku040-ffva1156-2-e.

3.5. Overflow Counter

The Overflow Counter (OC) counts the number of the overflows coming from the CEC.

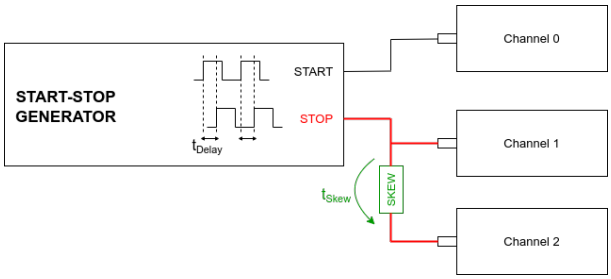

Figure 6: Measurement setup of the Precision experiment.

4. Measurements

Two different TDC implementations have been tested on the KCU105 Evaluation Board. Both implementations rely on a V-TDL resulting from a 4th order Sub-Interpolation. In the first implementation, the V-TDL is composed of 4 CARRY-chains in parallel, while, in the second implementation, it is composed of 2 CARRY-chains + 1 DSP-chain in parallel. It is worth noting that also in the second case the Sub-Interpolation is of 4th order, since one single DSP-chain generates two thermometric codes. The first experiment has been focused on comparing the single-shot precision and the hardware occupancy of the two implementations, while the second experiment consisted of studying the non-linearities the two implementations suffer from. Figure 6 shows the measurement setup used to compute the precision. Figure 7 shows the measurement setup used to test the linearity, consisting of two external, uncorrelated, Waveform Generators.

Figure 7: Measurement setup of the Linearity experiment.

We can see from Table 2 that, in the "hybrid" TDC, we achieve 12 channels more (thanks to a 20% reduction in the area) and we save 0.1 W for each channel, at the expense of a slightly worse single-shot precision (i.e., just 1 ps), compared to the TDC based on CARRY-chains only.

Conclusions

To cope with the increasing performances required in time-resolved experiments, a high-resolution TDL-TDC for XUS/XUS+ FPGAs has been implemented. Two different TDC implementations have been tested, both exploiting the Super Wave Union (SuperWU) Sub-Interpolation algorithm with four TDLs in parallel. The first implementation consists of a V-TDL composed of 4 CARRY-chains in parallel, while the second consists of a V-TDL resulting from 2 CARRY-chains + 1 DSP-chain in parallel. Both implementations have been tested on a Xilinx's KCU105 Evaluation Board, hosting a Kintex-UltraScale™ FPGA (xcku040-ffva1156-2-e). The following experimental results have been obtained:

- a better single-shot precision has been achieved on the 4 CARRY-chains implementation (i.e., 2.8 ps) than on the 2 CARRY-chains + 1 DSP-chain one (i.e., 3.8 ps), making the former more suitable for those applications requiring very high precision;
- lower power consumption (i.e., 0.1 W less) and hardware occupancy (i.e., 1000 FFs less) have been achieved on the 2 CARRY-chains + 1 DSP-chain implementation than in the 4 CARRY-chains, allowing the former to have a greater number of channels (i.e., 74). It is thus more suitable for those applications requiring a higher number of physical events to be detected;
- both implementations have negligible non-linearity since the DNLs are equal to 0.22 ps and 0.3 ps for the 4 CARRY-chains and the 2 CARRY-chains + 1 DSP-chain implementation, respectively, and the INLs are equal to 5.8 ps and 12 ps, respectively.

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