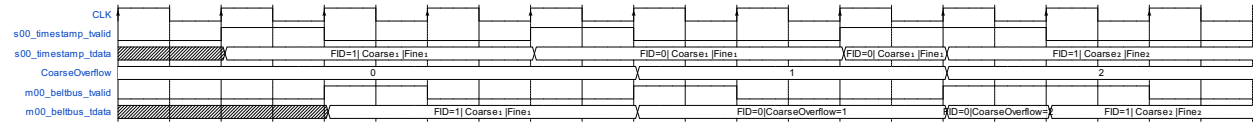
AXI4Stream_OverflowCounter

This is a Vivado 2017.3 Project, used to counting the number of Overflow which occur in the timestamps coming from the TDC.
The input of the Overflow Counter is a AXI4-Stream interface consisting of a Valid and a Data channel, *s00_timestamp_tvalid* and *s00_timestamp_tdata*.
The output depends on the value of the most significant bits(*FID*) of the input.
The timestamps in output of the Overflow Counter is an AXI4 Stream interface.

If *BIT_FID = 0* the Belt Bus is removed and the output is a standard Axi4 Stream. In this case the module is transparent and the input is transferred unchanged to the output (*beltbus_tvalid <= timestamp_tvalid< em>, beltbus_tdata <= timestamp_tdata< em>). Moreover the Counter of Overflow(CoarseOverflow_cnt) is not enabled.*
If BIT_FID /= 0 and timestamp_tvalid = '1', the output corresponds exactly to the input (beltbus_tdata <= timestamp_tdata< em>) if you have a measure (fid = '1'), otherwise if you have an Overflow (fid = 0) the CoarseOverflow_cnt is increased by one and the output contains the fid & CoarseOverflow_cnt.

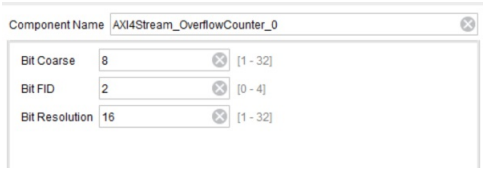


IP-Core

Overflow Counter for AXI4-Stream interface IP-Core.

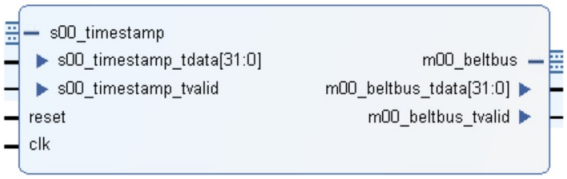
Generic

- **BIT_FID**: Bit Dimension of the Fid part of the Timestamp, *NATURAL* type. If *BIT_FID = 0* the belt bus is removed and it is a standard axi4 stream.
- **BIT_COARSE**: Bit Dimension of the Coarse part of the Timestamp, *NATURAL* type *RANGE 0 TO 32*.
- **BIT_RESOLUTION**: Bit Dimension of the Fine part of the Timestamp, *POSITIVE* type *RANGE 1 TO 32*.



Port

- **reset**: Asynchronous system reset active high (if '1' goto reset state).
- **clk**: System clock.
- **s00_timestamp**: AXI4 Stream Slave (Input) interface, uncalibrated data coming from the previous module().
  - **s00_timestamp_tvalid**: Valid of the input data, *STD_LOGIC* type.
  - **s00_timestamp_tdata**: Input data (timestamp) padded to upper byte dimension, *STD_LOGIC_VECTOR((((BIT_FID + BIT_COARSE + BIT_RESOLUTION-1)/8+1) * 8)-1 DOWNTO 0)* type, used only *STD_LOGIC_VECTOR(BIT_FID + BIT_COARSE + BIT_RESOLUTION-1 downto 0)* type.
- **m00_beltbus**: AXI4 Stream master (Output) interface, containing the value of the input data (*s00_timestamp_tdata*) or the number of Overflow depending on the value of the FID.
  - **m00_beltbus_tvalid**: Valid of the output data, *STD_LOGIC* type.
  - **m00_beltbus_tdata**: Output data with the proper FID padded to upper byte dimension *STD_LOGIC_VECTOR((((BIT_FID + BIT_COARSE + BIT_RESOLUTION-1)/8+1) * 8)-1 DOWNTO 0)* type, used only *STD_LOGIC_VECTOR(BIT_FID + BIT_COARSE + BIT_RESOLUTION-1 downto 0)* type.



Sources

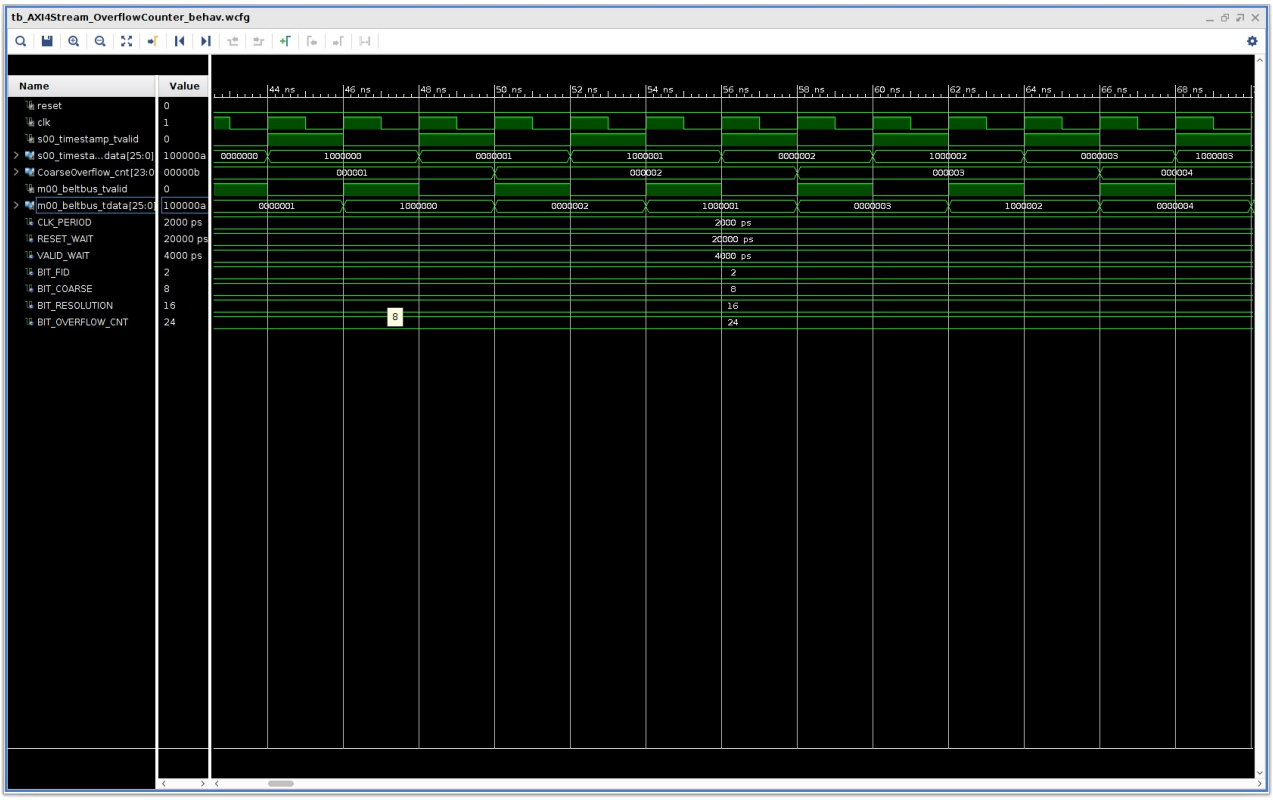
We can find in *hdl/* the following module directory:

- **AXI4Stream_OverflowCounter**: Wrapper used for rename the input and output interfaces with AXI4-Stream for IP-Core, input as slave and output as a master.
- **AXI4Stream_OverflowCounterWrapper**: Wrapper used for rename the input and output interfaces with pseudo AXI4-Stream for HDL, input as slave and output as a master.
- **OverflowCounter**: Count the number of Overflow in the input data(*s00_timestamp_tdata*).

Simulation

We can find in *src/* the following module directory:

- **tb_AXI4Stream_OverflowCounter**: HDL simulation of *AXI4Stream_OverflowCounter*.
- **tb_AXI4Stream_OverflowCounter_behav**: Waveform of *tb_AXI4Stream_OverflowCounter*.


tb_AXI4Stream_OverflowCounter_behav.wcfg
Name
Value
reset
0
clk
1
s00_timestamp_tvalid
0
s00_timesta...data[25:0]
100000a
CoarseOverflow_cnt[23:0
00000b
m00_beltbus_tvalid
0
m00_beltbus_tdata[25:0]
100000a
CLK_PERIOD
2000 ps
RESET_WAIT
20000 ps
VALID_WAIT
4000 ps
BIT_FID
2
BIT_COARSE
8
BIT_RESOLUTION
16
BIT_OVERFLOW_CNT
24
44 ns
46 ns
48 ns
50 ns
52 ns
54 ns
56 ns
58 ns
60 ns
62 ns
64 ns
66 ns
68 ns
0000000
1000000
0000001
1000001
0000002
1000002
0000003
1000003
000001
000002
000003
000004
0000001
1000000
0000002
1000001
0000003
1000002
0000004
2000 ps
20000 ps
4000 ps
2
8
16
24
8